EE214 - Digital Circuits Lab

Serial Adder

14th Oct 2022

Instructions:

1. Use **Behavioural** modeling for writing VHDL description
2. Perform RTL simulation using the provided testbench and tracefile.
3. Demonstrate the simulations to your TA
4. Submit the entire project files in .zip format in moodle.

Problem Statement: Serial Adder

- Design state diagram for Serial Adder. [5 Marks]
- Use behavioural modelling for this experiment.
- Reset is asynchronous in nature i.e. reset effects the output sequence irrespective of the input clock arrival.
- Write VHDL Description of serial adder using Behavioural modelling.[10 Marks]
  Assume that the circuit is in an initial state at time instant m. Then for any $n \geq m$, the output sequences $[s(k)]_{k=m}^{n}$ is related to the input sequences $[a(k)]_{k=m}^{n}$ and $[b(k)]_{k=m}^{n}$ by the following relations

$$
\begin{array}{ll}
 & a(n)a(n-1)a(n-2)....a(m) \\
+ & b(n)b(n-1)b(n-2)....b(m) \\
- - - - - - - - - - - - - - - - - \\
= & s(n)s(n-1)s(n-2)....s(m)
\end{array}
$$

1. **Code Snippet:**

```
library ieee;
use ieee.std_logic_1164.all;

entity Serial_Adder is
port (reset, a, b, clock: in std_logic; s: out std_logic);
end entity;

architecture BHV of Serial_Adder is

////// WRITE CODE /////////

end BHV;
```

- Tracefile format: ($< reset\ a\ b\ clock >\ \ < s >\ \ < Maskbit >$)
  Tracefile