Homework 1

Wadhwani Electronics Lab, IIT Bombay
Thursday 4th August, 2021
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Instructions

1. **Please complete the following assignment before your next lab turn**
2. **Use structural modelling for this assignment; means instantiate components and use port map to connect those components**

4-bit Adder-Subtractor

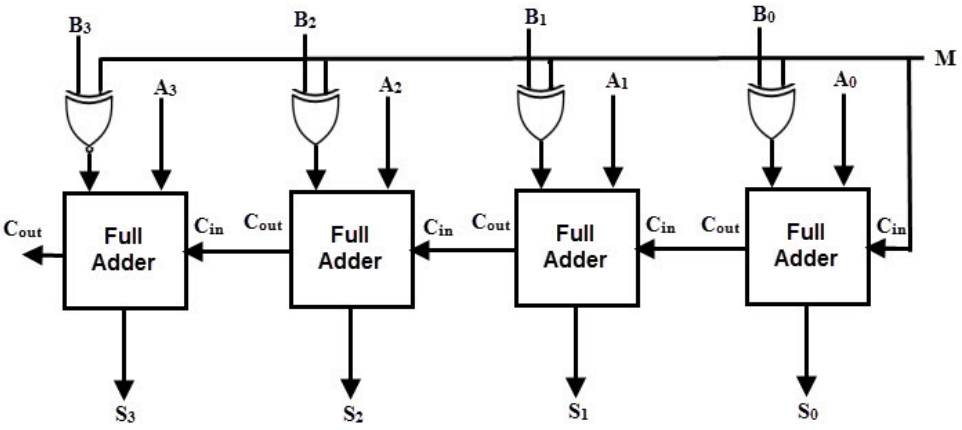
(A) VHDL Description [5 Marks]

You have been given a full adder description as the reference design. Using this full adder and XOR gate (from `Gates.vhdl`) as a component, describe a
4-bit ripple carry adder-subtractor in VHDL.

4-bit ripple carry adder-subtractor has following ports

- Two 4-bit inputs : A (A_3 A_2 A_1 A_0) , B (B_3 B_2 B_1 B_0)
- One 1-bit input: M
- One 4-bit output : S (S_3 S_2 S_1 S_0)
- One 1-bit output: Cout

> **NOTE**
>
> It is a simple binary adder-subtractor that can be implemented by cascading four full adders such that the the carry generated by the addition of lower significant bits forms the incoming carry for addition of the next significant bits.



(B) Explain briefly. How the functionality of the above circuit changes for different values of M ? [2 Marks]

(C) Simulation [5 Marks]

Perform RTL and Gate level simulation of your dsign using the generic testbench to confirm the correctness of your description.

> **NOTE**
>
> To do this, note that you need to use the given tracefile and modify the testbench given to you appropriately.

Tracefile format<a3 a2 a1 a0><b3 b2 b1 b0><M> <Cout><S> 11111Tracefile