EE23BTECH11217 - Prajwal M*

EE 16

The steady state output V_{out} of the circuit shown below, will

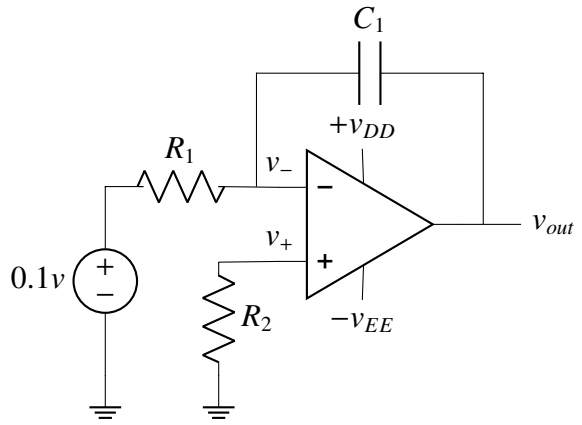

Fig. 0. circuit

1) saturate to $+V_{DD}$
2) saturate to $-V_{EE}$
3) become equal to $0.1V$
4) become equal to $-0.1V$

Solution:

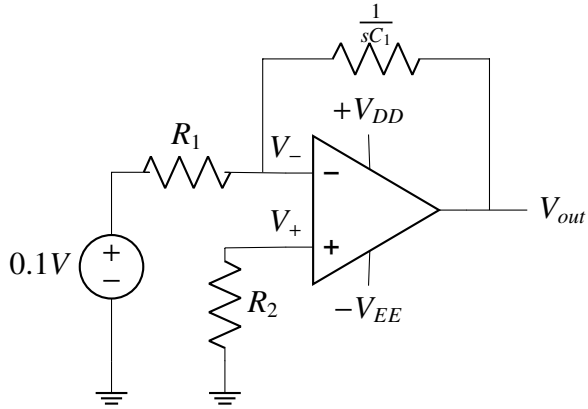

Fig. 4. s-domain circuit

for an ideal OP amp,

$$V_+ = 0V \tag{1}$$
$$V_- = 0V \tag{2}$$

using KVL,

$$0 = \frac{V_- - 0.1}{R_1} + C_1 s\,(V_- - V_{out}) \tag{3}$$
$$V_{out} = \frac{V_- - 0.1}{R_1 C_1 s} + V_- \tag{4}$$
$$= -\frac{0.1}{R_1 C_1 s} \quad \text{using (2)} \tag{5}$$
$$V_{out} \overset{\mathcal{L}^-}{\longleftrightarrow} v_{out} \tag{6}$$
$$v_{out} = -\frac{0.1}{R_1 C_1} t \tag{7}$$
$$v_{out} = max\left\{-v_{EE}, -\frac{1}{R_1 C_1} t\right\} \tag{8}$$

Hence, v_{out} saturates to $-v_{EE}$