Laser Communication using Digital Logic

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Lab Project

EE1200: Electrical Circuits Lab

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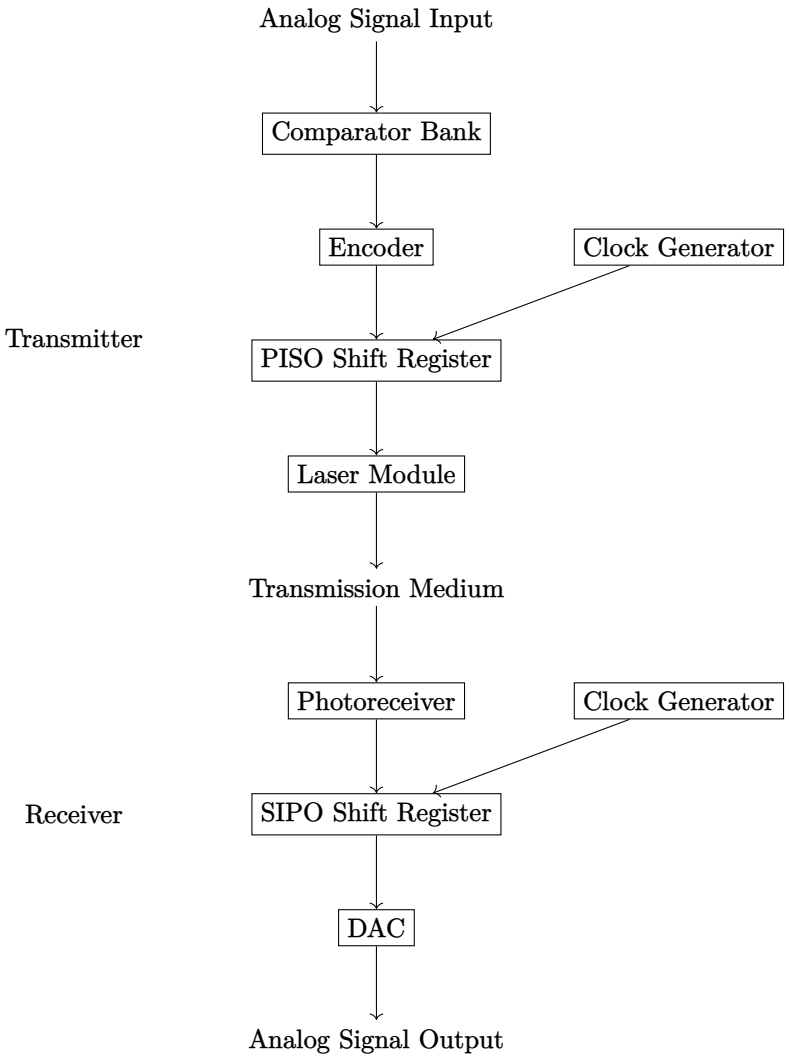
1 | Aim

- To communicate using IR signals.
- To infer data transfer using digital logic.

2 | Equipments Used

IC: 7404, 74166, 386, 311, 74595, 347, 555, 7474, 4532, 7447, laser diode, LDR, Speaker, LED

3 | Block diagram



4 | Circuit Diagram

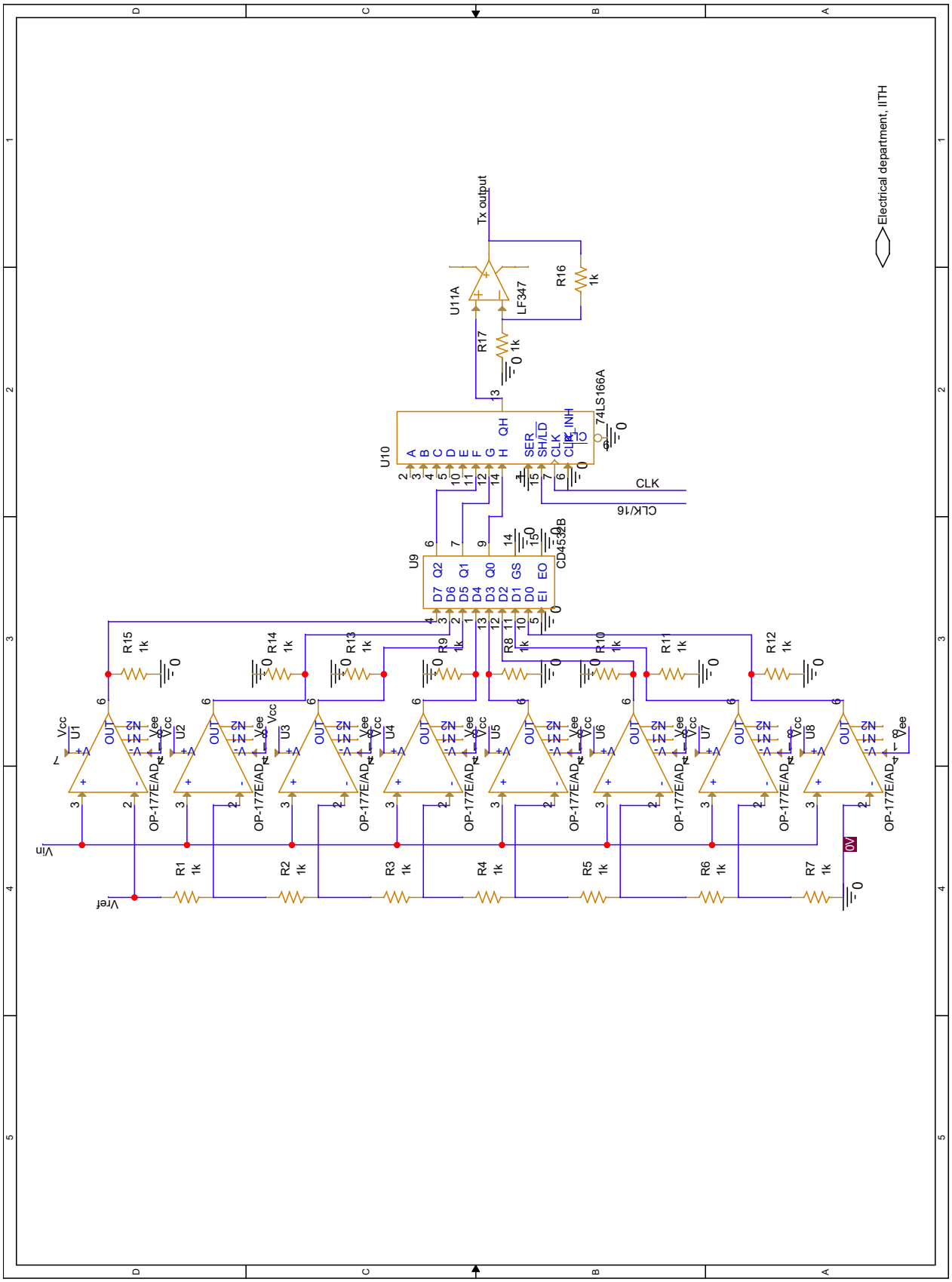


Figure 4.1: transmitter circuit built using CaptureCIS

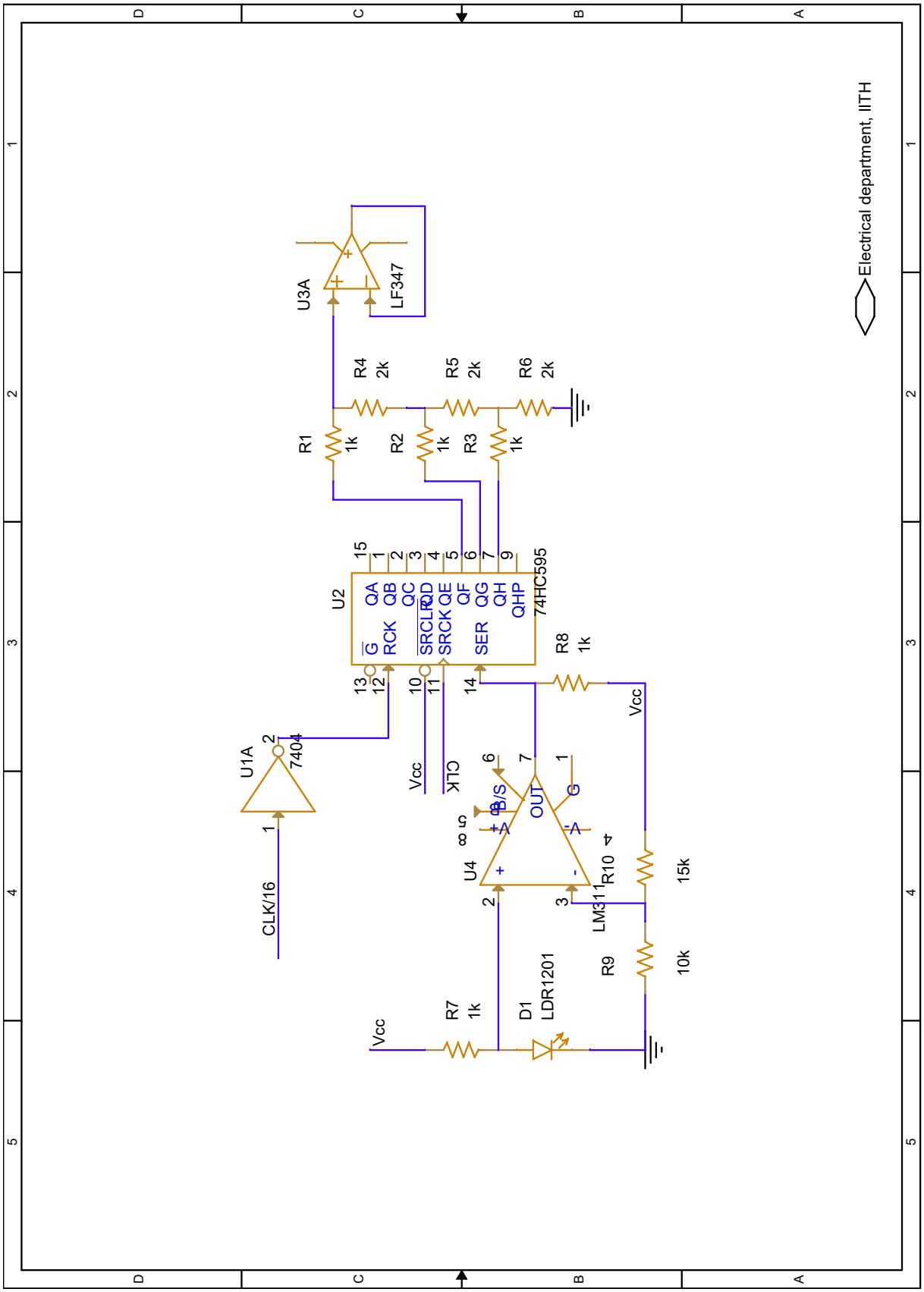


Figure 4.2: receiver circuit built using CaptureCIS

5 | ADC

1. The below figure shows the circuit implemented for 3bit Flash ADC.

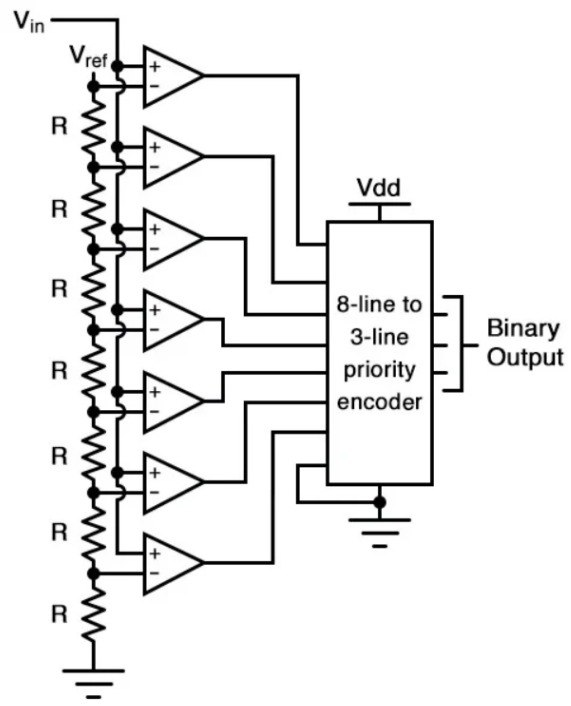


Figure 5.1: 3Bit Flash ADC Circuit Diagram

2. The equal resistors we used in 470Ω
3. 7 compratators have been used. The V_{ref} voltage is given as $5V$ and V_{in} is the input voltage.

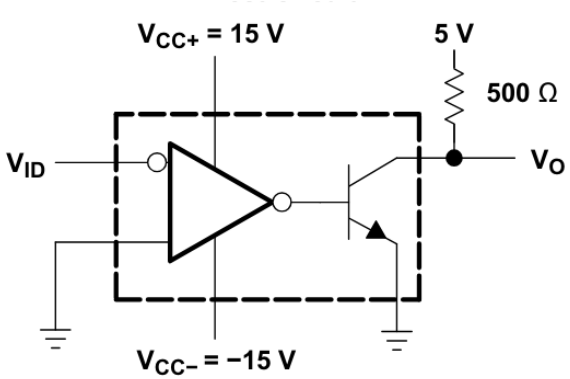


Figure 5.2: Comparator circuit for ADC

8 Bit Priority Encoder

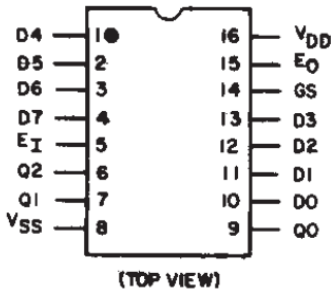


Figure 5.3: Comparator IC Pin Out Diagram

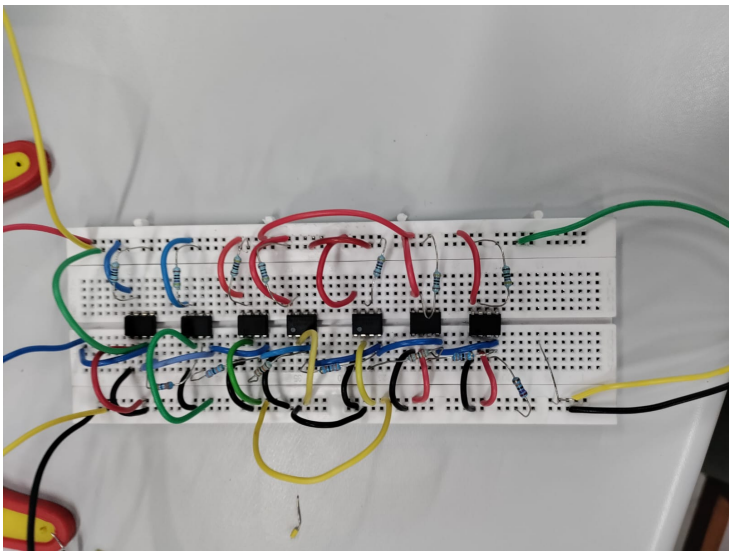


Figure 5.4: Comparator circuit for ADC

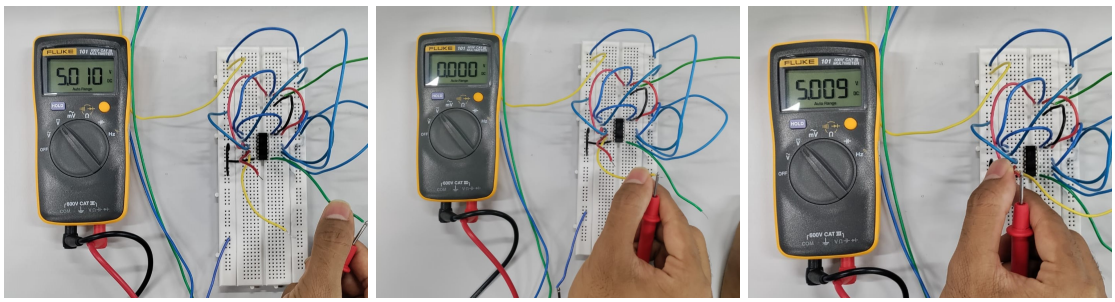


Figure 5.5: ADC (output - 101) successfully Demonstrated

6 | DAC

1. **Initialization:** The R-2R DAC is initialized with all its input bits set to a known digital value, usually in binary format.
2. **Binary Input:** The digital input signal is provided in binary format, with each bit representing a specific voltage level (reference voltage is 5V).
3. **R-2R Ladder Network:** The R-2R ladder network consists of two types of resistors: R and 2R. The resistors are arranged in a ladder-like structure, with each bit controlling the connection of a resistor to the output.

4. **Voltage Division:** Based on the digital input, the corresponding resistors in the ladder network are either connected or disconnected from the output. This creates different voltage levels at the output node.

5. **Analog Output:** The voltage at the output node of the ladder network represents the analog equivalent of the digital input signal. This analog output signal is continuous and proportional to the digital input.

6. **Accuracy and Linearity:** The accuracy and linearity of the R-2R DAC depend on the precision of the resistors used and the matching between them. Higher precision resistors result in better accuracy and linearity of the DAC.

R-2R DACs are commonly used in various applications such as audio processing, instrumentation, and communication systems due to their simplicity, accuracy, and ease of implementation.

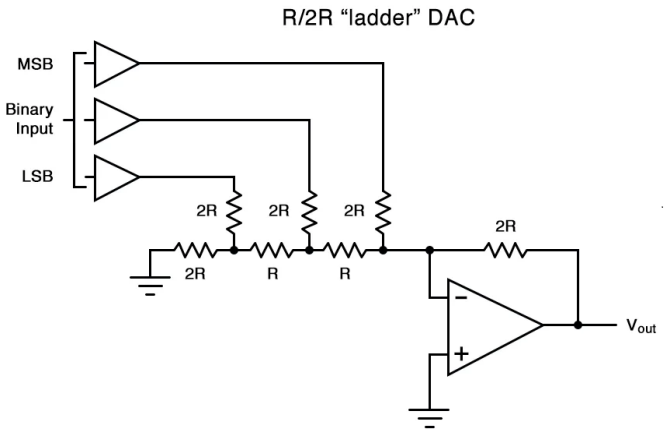


Figure 6.1: DAC

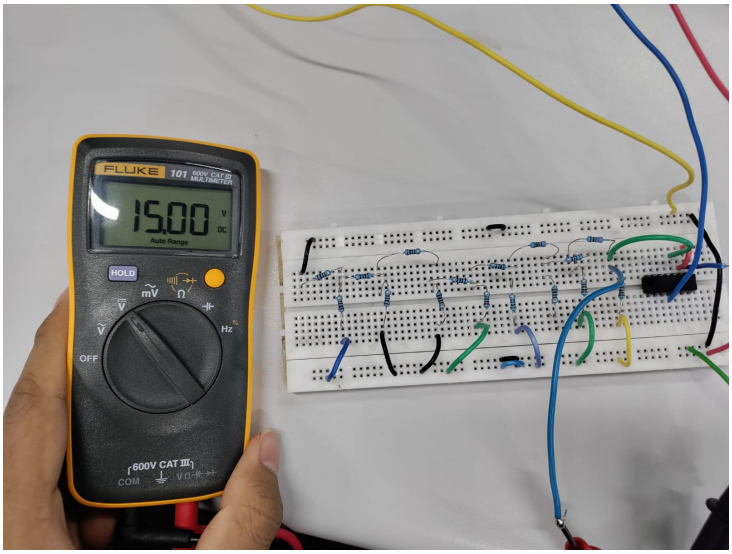


Figure 6.2: DAC

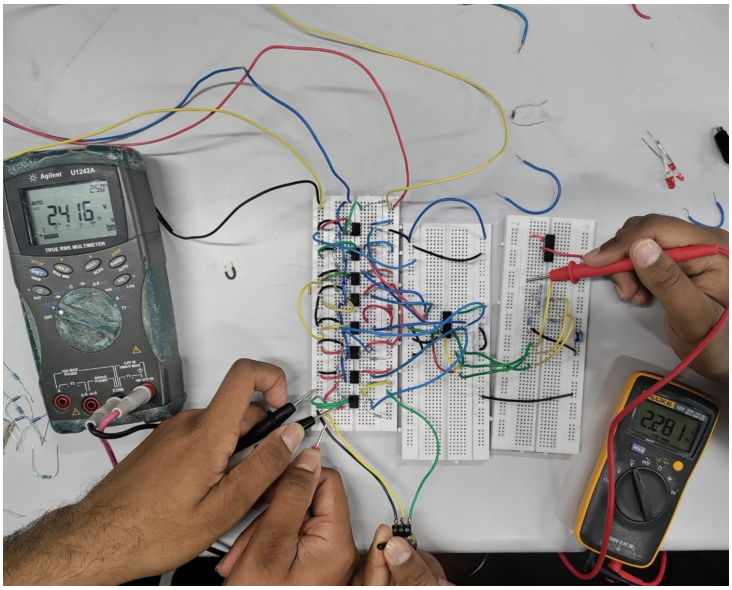
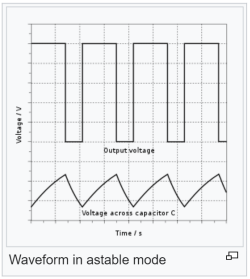
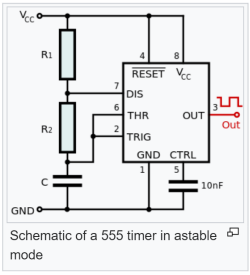


Figure 6.3: ADC-DAC verification

7 | Clock

NE555 IC is used for creating a clock with the required frequency. It has many modes and one of the modes is Astable Mode which is used here. In the astable configuration, the 555 timer puts out a continuous stream of rectangular pulses having a specific period.





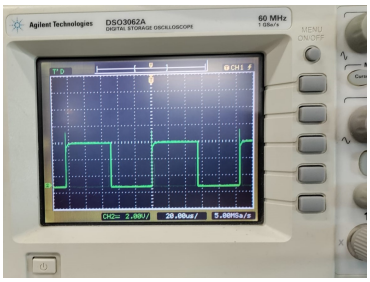


Figure 7.1: 555-Timer Circuit with the observed waveform

Frequency Division

1. The clock frequency driving the shift registers is not the clock frequency its a multiple of the clock. Here we need a frequency of $\frac{f}{16}$ where f is the clock frequency.
2. The outputs of the encoder is parallel input and when PISO gives the output we want the data to load fully then SIPO should start its function. So wait for 16 clock cycles.
3. This frequency division is achieved by using four D-flipflops in asynchronous mode.

Dual D-Type Positive Edge Triggered FlipFlop

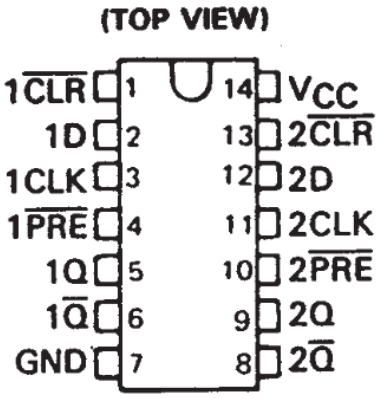


Figure 7.2: D-Flip Flop IC

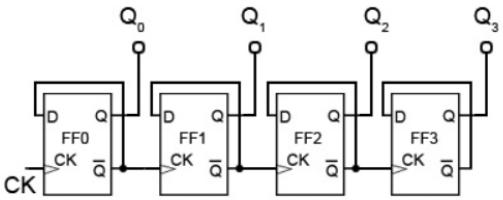


Figure 7.3: The output of the last flipflop has the frequency of $\frac{f}{16}$

8 | PISO shift register

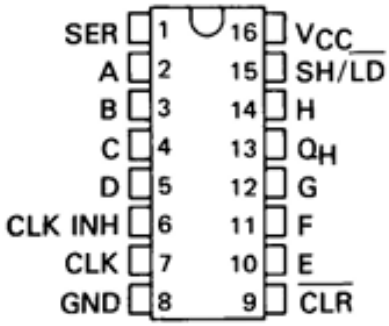


Figure 8.1: 4166 PISO shift register

An **SN4166** PISO (Parallel-In Serial-Out) shift register efficiently converts data between parallel and serial formats. It consists of flip-flops that store data bits. It simplifies data transmission.
Key Functions:

1. Parallel Input(A, B, C, D, E, F, G, H): Loads 8 data bits simultaneously.

2. Serial Output (O_H): Transmits data one bit at a time.

3. Clock-Driven Shifting (CLK): Shifts data on each clock pulse for serial output.

9 | SIPO shift register

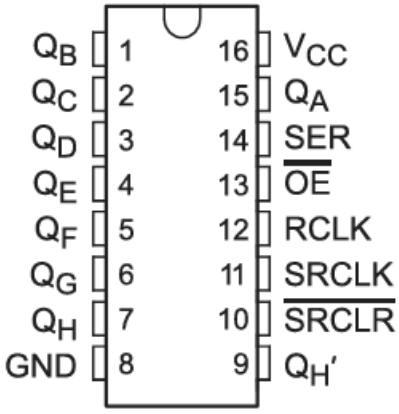


Figure 9.1: 74595 SIPO shift register

An **SN74595** Serial-In, Parallel-Out (SIPO) shift register is an IC used for storing and shifting binary data serially, then outputting it in parallel 8-bits.

- Serial Input (SER): Input for serial data.
- Parallel Output ($Q_A, Q_B ... Q_H$): Output for parallel data.
- Clock (RCLK): Input for clock signal to synchronize shifting.
- Clear ($SR\bar{C}LR$): Input for clearing the shift register.
- Output Enable (OE): Input for enabling/disabling the parallel outputs.

Data is input serially through the serial input (SI) line. On each clock pulse, the data is shifted through the shift register. Once all the data is shifted in, it is available in parallel form at the parallel output (PO) lines. The output can be enabled or disabled using the Output Enable (OE) line. The shift register can be cleared using the Clear (CLR) line. In our case, the serial input is obtained from the receiver and then passed to the SIPO register. As we have used 8 to 3 encoder, we will get 3 bits at the receiver output, which we have obtained at the 3 bits from MSB.

10 | Transmitter

1. An analog signal is the input.
2. The signal is sampled and converted to 3bits using the ADC we built using the comparators and Encoder.
3. The 3bits are in parallel which are sent to PISO shift register which output the bits serially one after the other. We have used clock (frequency f) for CLK and clock (frequency $\frac{f}{16}$) for the $\bar{load}$
4. This serial output is sent to a an amplifier with unity gain. The output is connected to a LDR diode which transmits our data by switching on (1) and off (0).

11 | Receiver

1. For receiving the signals transmitted using the IR laser, we will use a photoresistor. A photoresistor is a passive component that decreases in resistance as a result of increasing luminosity (light) on its sensitive surface.

2. We will provide supply voltage to the photoresistor and then connect it with a resistor which is then grounded. We will pass the voltage on the common terminal of the photoresistor and this resistor to a comparator and then compare it with a reference voltage obtained using voltage divider.

3. The basic principle here is that if the laser is transmitting bit 0, then it is turned off due to which the resistance of the photoresistor is high and the voltage on the common terminal of the resistors is very less. Due to this the comparator output is 0.

4. On the other hand, when the bit 1 is transmitted the laser is on and the resistance of the photoresistor decreases due to which the volatge is higher at the common terminal. In this case, the comparator will give the output 1.

5. In this way, the bits are received from the transmitter and then are passed on to the serial input pin of the SIPO shift register.

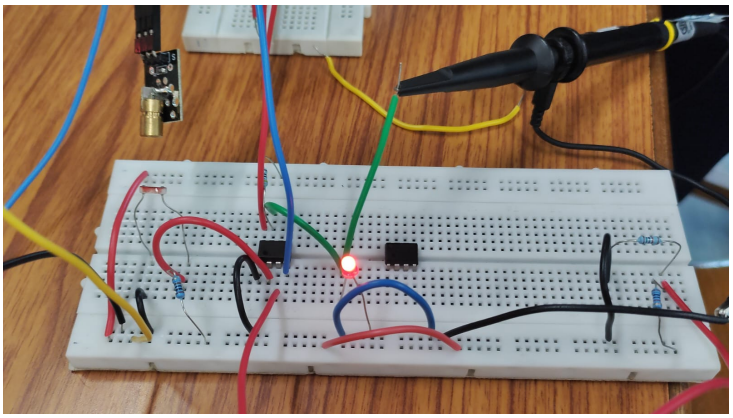


Figure 11.1: receiver-photoresistor

12 | Observations

Parameter	Readings
V_{ref}	5V
Power Dissipated Across Laser	20mW
Qunatization Level	0.6V

Table 12.1: Observations

13 | Conclusion

We have successfully built a communication module using infrared LDRs using digital logic. This is a proof of concept for such communication, which is scalable when built using better components.