

7 Series FPGAs Packaging and Pinout

Product Specification

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/2011	1.0	Initial Xilinx release.
04/06/2011	1.1	<p>Removed the SBG324 package from the entire document. Added three Kintex®-7 devices: XC7K355T, XC7K420T, and XC7K480T.</p> <p>Updated disclaimer and copyright on page 2. Updated package size of FF1156 in Table 1-1. Updated DXP_0, DXN_0 in Table 1-11.</p> <p>The Table 2-2 single ASCII device files have been updated for both the XC7K70T and XC7K160T. All ASCII TXT files and the overall ZIP file have been updated on the web.</p> <p>Updated the XC7K70TFBG676 figures: Figure 3-49, Figure 3-50, Figure 3-51, and Figure 3-52.</p> <p>Added information to Chapter 4, Mechanical Drawings, Chapter 5, Thermal Specifications, and Chapter 6, Package Marking.</p>
06/14/2011	1.2	<p>Added Virtex®-7 device information including updating Table 1-1, adding Table 1-3, Table 1-9, Table 2-3, and Table 3-3. In Table 1-11, updated Note 3, the Configuration Pins section, and the Analog to Digital Converter (XADC) Pins section.</p> <p>Updated Figure 3-47, Figure 3-48, Figure 3-51, Figure 3-52, Figure 3-55, Figure 3-56, Figure 3-59, Figure 3-60, Figure 3-63, Figure 3-64, Figure 3-67, and Figure 3-68. Added Figure 3-68 through Figure 3-132.</p> <p>Added Figure 4-28 the mechanical drawing for the Kintex-7 devices FFG1156 package. Also added some Virtex-7 device mechanical drawings in Figure 4-28 through Figure 4-35.</p> <p>Added thermal resistance data to Table 5-1.</p>
10/03/2011	1.3	<p>Added Artix®-7 device information including updating Table 1-1, adding Table 1-3, Table 1-7, Table 2-1, and Table 3-1.</p> <p>Clarified the interposer in Figure-12 and Figure 1-14. Revised horizontal center for the XC7VX415T in Figure 1-16. Updated the DXP_0, DXN_0 description and notes in Table 1-11. Added devices to the Die Level Bank Numbering Overview section. Clarified the I/O banks summary section.</p> <p>Added Artix-7 device diagrams in the CSG324 package. Added XC7V585T device diagrams Figure 3-81 through Figure 3-88.</p> <p>Moved AD4P/N, AD12P/N, and AD5P/N pins from [IO_L2P_T0_35:IO_L4N_T0_35] to [IO_L1P_T0_35:IO_L3N_T0_35] in Figure 3-89, Figure 3-93, Figure 3-113, Figure 3-117, Figure 3-121, Figure 3-125, and Figure 3-129.</p> <p>Fixed the labeling for EMCCLK in Figure 3-73, Figure 3-81, Figure 3-89, Figure 3-93, Figure 3-113, Figure 3-117, Figure 3-121, Figure 3-125, and Figure 3-129.</p> <p>Updated the mechanical drawings for Figure 4-32 and Figure 4-35.</p> <p>Updated thermal resistance data in Table 5-1.</p> <p>Updated Chapter 6, Package Marking.</p>
10/17/2011	1.4	<p>Revised the FBG484 and FBV484 Packages section describing XC7K160T Banks.</p> <p>Added the mechanical drawings: Figure 4-32 and Figure 4-36. Updated Figure 4-35 to include the FF(G)1928 package.</p> <p>Added thermal resistance data to Table 5-1.</p>

Date	Version	Revision
02/03/2012	1.5	<p>Updated Table 1-3 and Table 1-5 and added Table 1-6. Updated Table 1-7 and Table 1-8 and added Table 1-9. Revised Note 2 in Table 1-11. Removed Figures 1-1 and 1-2 along with references to the XC7A8, XC7A15, XC7A30T, and XC7A50T. Added Figure 1-5 and Figure 1-3. Clarified Figure 1-9 though Figure 1-12, Figure 1-14, Figure 1-18, and Figure 1-21.</p> <p>Updated Table 2-3 and added Table 2-4.</p> <p>Added devices to Table 3-1 and revised Table 3-2 (XC7K420T and XC7K480T). Updated Table 3-3 and added Table 3-4 and Table 3-5.</p> <p>Revised specifications in:</p> <ul style="list-style-type: none"> • Figure 4-15: FB484, FBG484, and FBV484 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch) • Figure 4-18: FB676, FBG676, and FBV676 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch). • Figure 4-23: FB900, FBG900, and FBV900 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch) and combined with Figure 4-6. • Figure 4-31: FF1157, FFG1157, FFV1157, FF1158, FFG1158, and FFV1158 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch). <p>Added thermal resistance data to Table 5-1 and added Soldering Guidelines section.</p> <p>Added Appendix B.</p>
05/24/2012	1.6	<p>Removed the FFG1933 and FLG1933 packages throughout. Added the FLG1926 package where appropriate.</p> <p>Updated the Introduction in Chapter 1. Updated XC7K420T in Table 1-9. Added Note 7 to Table 1-11. Updated the description and figure in the XC7K420T Banks and XC7VX550T Banks sections.</p> <p>Updated Figure 3-34, Figure 3-38, Figure 3-42, and Figure 3-34. Added Figure 3-157 through Figure 3-160.</p> <p>Added Figure 4-7: FB676, FBG676, and FBV676 Flip-Chip Lidless BGA Package Specifications for Artix-7 FPGAs. Revised specifications and added capacitor location figures for:</p> <ul style="list-style-type: none"> • Figure 4-18: FB676, FBG676, and FBV676 Flip-Chip Lidless BGA Package Specifications for Kintex-7 FPGAs <ul style="list-style-type: none"> • Figure 4-21: XC7K325T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations • Figure 4-22: XC7K410T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations • Figure 4-23: FB900, FBG900, and FBV900 Flip-Chip Lidless BGA Package Specifications for Kintex-7 FPGAs <ul style="list-style-type: none"> • Figure 4-24: XC7K325T FB900, FBG900, and FBV900 Die Dimensions with Capacitor Locations • Figure 4-25: XC7K410T FB900, FBG900, and FBV900 Die Dimensions with Capacitor Locations • Figure 4-28: FF1156, FFG1156, and FFV1156 Flip-Chip BGA Package Specification for Kintex-7 FPGAs • Figure 4-31: FF1157, FFG1157, FFV1157, FF1158, FFG1158, and FFV1158 Flip-Chip BGA Package Specification for Virtex®-7 FPGAs <p>Added Thermal Management Strategy, Heat Sink Removal Procedure, and updated Soldering Guidelines in Chapter 5.</p> <p>Updated Table A-1.</p>

Date	Version	Revision
07/20/2012	1.7	<p>In Table 1-11, updated the Other Pins section.</p> <p>Added the XC7VH290T, XC7VH580T, and XC7VH870T and associated HCG packages to all appropriate chapters, tables, and figures. Added the SBG484 package for the XC7A200T devices to all appropriate chapters, tables, and figures.</p> <p>Updated the XC7VX1140T-FLG1926 headings in Table 2-4, Figure 3-157 through Figure 3-160, and Figure 4-36.</p> <p>Updated GTP Quad numbers in Figure 1-4, Figure 3-22, and Figure 3-26. Also added numbers to Figure 3-25 and Figure 3-28. Updated the XC7V585T-FFG1761 figures: Figure 3-85 and Figure 3-88.</p> <p>Added new mechanical drawings for the Artix-7 FPGAs in Chapter 4 along with Figure 4-20, Figure 4-35, and Figure 4-36, and updated Figure 4-27.</p> <p>In Table 5-1, updated data throughout and added XC7VX1140T (FL1926) and XC7VH580T data.</p> <p>Added Figure 6-3: Artix-7 Device Package Marking.</p>
10/15/2012	1.8	<p>Removed the following devices: XC7A350T, XC7V1500T, XC7VH290T.</p> <p>Added Figure 4-19 and updated drawing in Figure 4-20. Added Note 5 to Figure 4-31. Updated A2 dimension in Figure 4-35. Updated aaa dimension in Figure 4-34 and Figure 4-36.</p> <p>Updated the JEDEC Moisture Sensitivity Level (MSL) for the Flip-Chip packages on page 271.</p>
02/14/2013	1.9	<p>Clarified pins in Figure 3-37.</p> <p>Updated Figure 4-11 and Figure 4-15 and added Figure 4-16 and Figure 4-17. Revised Figure 4-27 and Figure 4-31.</p> <p>In Table 5-1, updated data for Artix®-7 FPGAs, XC7K160T FF/FFG/FFV676, Virtex®-7 T FPGAs and XC7VX1140T.</p> <p>Updated Appendix B.</p>
11/15/2013	1.10	<p>Updated disclaimer on page 2.</p> <p>Added the XQ devices and RB/RF/RS package information throughout document.</p> <p>Added Note 1 to Table 1-2 and Note 6 to Table 1-11. Revised the super logic region numbers in Figure 1-20.</p> <p>Removed the Virtex-7 HT devices (HCG packages). Before removal, revised the super logic region numbers in Figure 1-20: XC7VH870T Banks. For packaging and pinout information on the Virtex-7 HT devices see www.xilinx.com/member/gtz/index.htm.</p> <p>Updated the legend in Figure 3-89, Figure 3-92, Figure 3-93, Figure 3-96, Figure 3-157, Figure 3-160, Figure 3-161, Figure 3-164, Figure 3-165, and Figure 3-168.</p> <p>Updated the A and A2 dimensions in Figure 4-11: FF1156, FFG1156, and FFV1156 Flip-Chip BGA Package Specification for Artix-7 FPGAs, page 227.</p> <p>Added Note 1 and updated the data in Table 5-1. Updated the Pb-Free Reflow Soldering in Chapter 5 discussion.</p> <p>Removed the engineering sample notation from the top mark drawings in Figure 6-1, Figure 6-2, and Figure 6-3. Updated the L2E description in Table 6-1.</p> <p>Updated Appendix A.</p>

Date	Version	Revision
03/18/2014	1.11	<p>Added the XC7A35T, XC7A50T, and XC7A75T throughout document including Table 1-3, Table 1-7, Figure 1-1, Figure 1-2, Figure 1-3, Table 2-1, Table 3-1, Table 5-1, and added or updated Figure 3-1 through Figure 3-28. Also added the automotive XA Artix-7 FPGA versions (XA7A35T, XA7A50T, XA7A75T, and XA7A100T) and the defense-graded Artix-7Q device (XQ7A50T) with applicable packages.</p> <p>In Table 1-1, updated Note 1. In Table 1-11, updated Note 2 and the description of PUDC_B.</p> <p>Added links to all the ruggedized packages in Chapter 2, 7 Series FPGAs Package Files.</p> <p>Updated the DCI pin description in the legends for all the Memory Groupings diagrams in Chapter 3, Device Diagrams.</p> <p>Added CPG236 package to document including Figure 4-1, Table 5-1, and Table A-1. Added CSG325 to document including updating Figure 4-2. This update includes a change in the A₂ dimensions for the CSG324. Replaced Figure 4-9: FG484 and FGG484 Wire-bond Fine-Pitch BGA Package Specification for Artix-7 FPGAs, page 225 with a new drawing with updated dimensions. Replaced Figure 4-10: FG676 and FGG676 Wire-bond Fine-Pitch BGA Package Specification for Artix-7 FPGAs, page 226 with a new drawing with an updated mechanical drawing. Updated the M specification in Figure 4-12: RB484 Ruggedized Flip-Chip BGA Package Specifications for Artix-7 FPGAs, page 228. Replaced Figure 4-26: FF676, FFG676, and FFV676 Flip-Chip BGA Package Specifications for Kintex-7 FPGAs, page 242 with a new drawing where the lid is updated with four corner posts.</p> <p>Updated the References links in Chapter 5, Thermal Specifications.</p> <p>Revised the M diameter for FF/FFG, FB/FBG, FH/FHG, FL/FLG, and RF/RB/RS packages in Table A-1.</p>
10/28/2014	1.12	<p>Added a discussion on ULA materials on page 16. Added clarifications with regards to Artix-7 devices throughout the document including Pin Compatibility Between Packages and Note 1 to Table 3-1. Updated Note on page 61.</p> <p>In Table 5-2 and Figure 5-7, revised the Peak temperature (body) values and the Ramp-up rate and Ramp-down rate to 2°C/s. Removed references to CL/CLG packages in Table 5-3 and Table A-1. Updated Figure 5-4. Also added the Peak Package Reflow Body Temperature values to Table 5-3. Added Heat Sink Removal Procedure, Package Pressure Handling Capacity, Post Reflow/Cleaning/Washing, and Conformal Coating. Added Chapter 7, Packing and Shipping.</p>
11/13/2014	1.13	Added XC7A15T and XA7A15T devices throughout the specification.
03/23/2016	1.14	<p>Updated to add the XQ7VX690T in the RF1158 package. Added RoHS compliant options (FFV packages) where applicable.</p> <p>In Table 1-11, updated the SRCC description.</p> <p>Updated Figure 4-1 with solder ball composition changes. Refined the A2 dimensions in Figure 4-5 and Figure 4-15. Added the FFV1761 package (Figure 4-33). Added the RF1158 to Figure 4-37.</p> <p>Completely revised Chapter 5, Thermal Specifications with industry standard guidelines for all sections. Updated the Thermal Management Strategy section. Updated the Thermal Interface Material section previously in Appendix B. Added the Applied Pressure from Heat Sink to the Package via Thermal Interface Materials section.</p> <p>In Appendix B: Moved and renamed the Reasons for Thermal Management section to Chapter 5. Removed the Package Loading Specifications section.</p>

Table of Contents

Revision History	3
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Preface: About This Guide

Guide Contents	13
Additional Resources	13

Chapter 1: Packaging Overview

Summary	15
Introduction	15
Device/Package Combinations and Maximum I/Os	16
Serial Transceiver Channels by Device/Package	18
Pin Definitions	23
Pin Compatibility Between Packages	27
Die Level Bank Numbering Overview	28
Banking and Clocking Summary	28
XC7A15T, XC7A35T, XA7A15T, and XA7A35T Banks	30
CPG236 Package	30
FTG256 Package (XC7A15T and XC7A35T only)	30
CSG324 Package	30
CSG325 Package	30
FGG484 Package (XC7A15T and XC7A35T only)	30
XC7A50T, XA7A50T, and XQ7A50T Banks	31
CPG236 Package	31
FTG256 Package (XC7A50T only)	31
CSG324 Package	31
CSG325 Package	31
FGG484 Package (XC7A50T and XQ7A50T only)	31
XC7A75T and XA7A75T Banks	32
FTG256 Package (XC7A75T only)	32
CSG324 Package	32
FGG484 Package	32
FGG676 Package (XC7A75T only)	32
XC7A100T, XQ7A100T, and XA7A100T Banks	33
FTG256 Package (XC7A100T only)	33
CSG324 Package	33
FGG484 Package	33
FGG676 Package (XC7A100T only)	33
XC7A200T and XQ7A200T Banks	34
SBG484, SBV484, and RS484 Packages	34
FBG484, FBV484, and RB484 Packages	34
FBG676, FBV676, and RB676 Packages	34
FFG1156 and FFV1156 Packages (XC7A200T only)	34
XC7K70T Banks	35
FBG484 and FBV484 Packages	35
FBG676 and FBV676 Packages	35

XC7K160T Banks	36
FBG484 and FBV484 Packages	36
FBG676, FBV676, FFG676, and FFV676 Packages	36
XC7K325T and XQ7K325T Banks	37
FBG676, FBV676, FFG676, FFV676, and RF676 Packages	37
FBG900, FBV900, FFG900, FFV900, and RF900 Packages	37
XC7K355T Banks	38
FFG901 and FFV901 Packages.....	38
XC7K410T and XQ7K410T Banks	39
FBG676, FBV676, FFG676, FFV676, and RF676 Packages	39
FBG900, FBV900, FFG900, FFV900, and RF900 Packages	39
XC7K420T Banks	40
FFG901 and FFV901 Packages..	40
FFG1156 and FFV1156 Packages.....	40
XC7K480T Banks	41
FFG901 and FFV901 Packages.....	41
FFG1156 and FFV1156 Packages.....	41
XC7V585T and XQ7V585T Banks	42
FFG1157 and RF1157 Packages.....	42
FFG1761 and RF1761 Packages.....	42
XC7V2000T Banks	43
FHG1761 Package.....	43
FLG1925 Package	43
XC7VX330T and XQ7VX330T Banks.....	45
FFG1157, FFV1157, and RF1157 Packages.....	45
FFG1761, FFV1761, and RF1761 Packages.....	45
XC7VX415T Banks	46
FFG1157 and FFV1157 Packages.....	46
FFG1158 and FFV1158 Packages.....	46
FFC1927 and FFV1927 Packages.....	46
XC7VX485T and XQ7VX485T Banks.....	47
FFG1157 Package	47
FFG1158 and RF1158 Packages.....	47
FFG1761 and RF1761 Packages.....	47
FFG1927 Package	47
FFG1930 and RF1930 Packages.....	47
XC7VX550T Banks	49
FFG1158 Package	49
FFG1927 Package	49
XC7VX690T and XQ7VX690T Banks	50
FFG1157 and RF1157 Packages	50
FFG1158 and RF1158 Packages	50
FFG1761 and RF1761 Packages	50
FFG1926 Package	50
FFG1927 Package	50
FFG1930 and RF1930 Packages	50
XC7VX980T and XQ7VX980T Banks	52
FFG1926 Package	52
FFG1928 Package	52
FFG1930 and RF1930 Packages	52
XC7VX1140T Banks	54
FLG1926 Package	54
FLG1928 Package	54
FLG1930 Package	54

Chapter 2: 7 Series FPGAs Package Files

About ASCII Package Files.....	57
ASCII Pinout Files	58

Chapter 3: Device Diagrams

Summary	61
Artix-7 FPGAs Device Diagrams.....	62
CP236 and CPG236 Packages—XC7A15T, XC7A35T, and XC7A50T	62
CS324 and CSG324 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T	65
CS325 and CSG325 Packages—XC7A15T, XC7A35T, and XC7A50T.....	67
FT256 and FTG256 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T	69
FG484 and FGG484 Packages—XC7A15T, XC7A35T, and XC7A50T	71
FG484 and FGG484 Packages—XC7A75T and XC7A100T	74
FG676 and FGG676 Packages—XC7A75T and XC7A100T	77
SB484, SBG484, SBV484, and RS484 Packages—XC7A200T	80
FB484, FBG484, FBV484, and RB484 Packages—XC7A200T	83
FB676, FBG676, FBV676, and RB676 Packages—XC7A200T	86
FF1156, FFG1156, and FFV1156 Packages—XC7A200T	89
Kintex-7 FPGAs Device Diagrams	93
FB484, FBG484, and FBV484 Packages—XC7K70T and XC7K160T	93
FB676, FBG676, and FBV676 Packages—XC7K70T	96
FB676, FBG676, and FBV676 Packages—XC7K160T, XC7K325T, and XC7K410T ..	99
FB900, FBG900, and FBV900 Packages—XC7K325T and XC7K410T	102
FF676, FFG676, FFV676, and RF676 Packages—XC7K160T, XC7K325T, and XC7K410T	106
FF900, FFG900, FFV900, and RF900 Packages—XC7K325T and XC7K410T	110
FF901, FFG901, and FFV901 Packages—XC7K355T	114
FF901, FFG901, and FFV901 Packages—XC7K420T and XC7K480T	118
FF1156, FFG1156, and FFV1156 Packages—XC7K420T and XC7K480T	122
Virtex-7 FPGAs Device Diagrams.....	126
FF1157, FFG1157, and RF1157 Packages—XC7V585T	127
FF1761, FFG1761, and RF1761 Packages—XC7V585T	131
FL1925 and FLG1925 Packages—XC7V2000T	135
FH1761 and FHG1761 Packages—XC7V2000T	139
FF1157, FFG1157, FFV1157, and RF1157 Packages—XC7VX330T, XC7VX415T, and XC7VX690T	143
FF1761, FFG1761, FFV1761, and RF1761 Packages—XC7VX330T	147
FF1158, FFG1158, FFV1158, and RF1158 Packages—XC7VX415T, XC7VX550T, and XC7VX690T	151
FF1927, FFG1927, and FFV1927 Packages—XC7VX415T	155
FF1157 and FFG1157 Packages—XC7VX485T	159
FF1158 and FFG1158 Packages—XC7VX485T	163
FF1761, FFG1761, and RF1761 Packages—XC7VX485T	167
FF1927 and FFG1927 Packages—XC7VX485T	171
FF1930, FFG1930, and RF1930 Packages—XC7VX485T	175
FF1761, FFG1761, and RF1761 Packages—XC7VX690T	179
FF1926 and FFG1926 Packages—XC7VX690T and XC7VX980T	183
FF1927 and FFG1927 Packages—XC7VX550T and XC7VX690T	187
FF1930, FFG1930, and RF1930 Packages—XC7VX690T	191

FF1928 and FFG1928 Packages—XC7VX980T	195
FF1930, FFG1930, and RF1930 Packages—XC7VX980T	199
FL1926 and FLG1926 Packages—XC7VX1140T	203
FL1928 and FLG1928 Packages—XC7VX1140T	207
FL1930 and FLG1930 Packages—XC7VX1140T	211

Chapter 4: Mechanical Drawings

Summary	215
Artix-7 FPGAs	215
Kintex-7 FPGAs	216
Virtex-7 FPGAs	216
CP236 and CPG236 (Artix-7 FPGAs)	217
Wire-Bond Chip-Scale BGA (0.5 mm Pitch)	217
CS/CSG324 and CS/CSG325 (Artix-7 FPGAs)	218
Wire-Bond Chip-Scale BGA (0.8 mm Pitch)	218
FT/FTG256 (Artix-7 FPGAs) Wire-Bond Fine-Pitch Thin BGA (1.0 mm Pitch)	219
SB484, SBG484, and SBV484 (Artix-7 FPGAs)	220
Flip-Chip Lidless BGA (0.8 mm Pitch)	220
FB484, FBG484, and FBV484 (Artix-7 FPGAs)	221
Flip-Chip Lidless BGA (1.0 mm Pitch)	221
FB676, FBG676, and FBV676 (Artix-7 FPGAs)	223
Flip-Chip Lidless BGA (1.0 mm Pitch)	223
FG484 and FGG484 (Artix-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch)	225
FG676 and FGG676 (Artix-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch)	226
FF1156, FFG1156, and FFV1156 (Artix-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)	227
RB484 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA (1.0 mm Pitch)	228
RS484 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA (0.8 mm Pitch)	229
RB676 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA (1.0 mm Pitch)	230
FB484, FBG484, and FBV484 (Kintex-7 FPGAs)	231
Flip-Chip Lidless BGA (1.0 mm Pitch)	231
FB676, FBG676, and FBV676 (Kintex-7 FPGAs)	234
Flip-Chip Lidless BGA (1.0 mm Pitch)	234
FB900, FBG900, and FBV900 (Kintex-7 FPGAs)	239
Flip-Chip Lidless BGA (1.0 mm Pitch)	239
FF676, FFG676, and FFV676 (Kintex-7 FPGAs)	242
Flip-Chip BGA (1.0 mm Pitch)	242
FF900, FFG900, FFV900, FF901, FFG901, and FFV901 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)	243
FF1156, FFG1156, and FFV1156 (Kintex-7 FPGAs)	244
Flip-Chip BGA (1.0 mm Pitch)	244

RF676 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)	245
RF900 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)	246
FF1157, FFG1157, FFV1157, FF1158, FFG1158, and FFV1158 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)	247
FF1761 and FFG1761 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)	248
FFV1761 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)	249
FH1761 and FHG1761 (Virtex-7 T FPGAs) Flip-Chip BGA (1.0 mm Pitch)	250
FF1926, FFG1926, FF1927, FFG1927, FFV1927, FF1928, FFG1928, FF1930, and FFG1930 (Virtex-7 XT FPGAs) Flip-Chip BGA (1.0 mm Pitch)	251
FL1925, FLG1925, FL1926, FLG1926, FL1928, FLG1928, and FL1930, FLG1930 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)	252
RF1157 and RF1158 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch)	253
RF1761 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch)	254
RF1930 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch)	255

Chapter 5: Thermal Specifications

Summary	257
Introduction	257
Support for Compact Thermal Models (CTM)	261
Thermal Management Strategy	262
Cavity-Up Plastic BGA Packages	262
Wire-Bond Packages	263
Flip-Chip Packages	264
System Level Heat Sink Solutions	264
Thermal Interface Material	264
Types of TIM	265
Guidelines for Thermal Interface Materials	265
Thermal Conductivity of the Material	266
Electrical Conductivity of the Material	266
Spreading Characteristics of the Material	266
Long-Term Stability and Reliability of the Material	266
Ease of Application	266
Applied Pressure from Heat Sink to the Package via Thermal Interface Materials	266
Heat Sink Removal Procedure	267
Soldering Guidelines	268
Sn/Pb Reflow Soldering	268
Pb-Free Reflow Soldering	269
Post Reflow/Cleaning/Washing	272
Conformal Coating	272
References	273

Chapter 6: Package Marking

Chapter 7: Packing and Shipping

Introduction 279

Appendix A: Recommended PCB Design Rules for BGA Packages

Appendix B: Heat Sink Guidelines for Lidless Flip-Chip Packages

Heat Sink Attachments for Lidless Flip-chip BGA (FB/FBG/FBV)	283
Silicon and Decoupling Capacitors Height Consideration	283
Types of Heat Sink Attachments	283
Heat Sink Attachment	285
Component Pick-up Tool Consideration	285
Heat Sink Attachment Process Considerations.....	285

About This Guide

Xilinx® 7 series FPGAs include three unified FPGA families that are all designed for lowest power to enable a common design to scale across families for optimal power, performance, and cost. The Artix®-7 family is optimized for lowest cost and absolute power for the highest volume applications. The Virtex®-7 family is optimized for highest system performance and capacity. The Kintex®-7 family is an innovative class of FPGAs optimized for the best price-performance. This guide serves as a technical reference describing the 7 series packaging and pinout specifications.

This 7 series packaging and pinout specification, part of an overall set of documentation on the 7 series FPGAs, is available on the Xilinx website at www.xilinx.com/documentation.

Guide Contents

This manual contains the following chapters:

- [Chapter 1, Packaging Overview](#)
- [Chapter 2, 7 Series FPGAs Package Files](#)
- [Chapter 3, Device Diagrams](#)
- [Chapter 4, Mechanical Drawings](#)
- [Chapter 5, Thermal Specifications](#)
- [Chapter 6, Package Marking](#)
- [Chapter 7, Packing and Shipping](#)
- [Appendix A, Recommended PCB Design Rules for BGA Packages](#)
- [Appendix B, Heat Sink Guidelines for Lidless Flip-Chip Packages](#)

Additional Resources

To find additional documentation, see the Xilinx website at:

<http://www.xilinx.com/support/documentation/index.htm>

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

<http://www.xilinx.com/support>

Packaging Overview

Summary

This chapter covers the following topics:

- [Introduction](#)
- [Device/Package Combinations and Maximum I/Os](#)
- [Pin Definitions](#)
- [Pin Compatibility Between Packages](#)
- [Die Level Bank Numbering Overview](#)

Introduction

This section describes the pinouts for the 7 series FPGAs in various fine pitch and flip-chip 1.0 mm pitch BGA packages and 0.8 mm and 0.5 mm pitch chip-scale packages.

Artix®-7 and Kintex®-7 devices are offered in low-cost, space-saving packages that are optimally designed for the maximum number of user I/Os.

Virtex®-7 T and Virtex-7 XT devices are offered exclusively in high performance flip-chip BGA packages that are optimally designed for improved signal integrity and jitter.

For pinout and packaging information on the Virtex-7 HT devices see www.xilinx.com/member/gtz/index.htm.

Package inductance is minimized as a result of optimal placement and even distribution as well as an increased number of Power and GND pins.

Flip-chip packages (FFG, FLG, FHG, FBG, SBG, RFG) are RoHS 6 of 6 compliant, with exemption 15 where there is lead in the C4 bumps that are used to complete a viable electrical connection between the semiconductor die and the package substrate. Flip-chip packages (FFV, FBV, SBV) are RoHS 6 of 6 compliant without the use of exemption 15. Non-flip chip packages (CPG, CSG, FTG, FGG) are RoHS 6 of 6 compliant. Selected packages include a Pb-only option.

All of the 7 series devices supported in a particular package are pinout compatible. See [Pin Compatibility Between Packages, page 27](#). Pins that are available in a device but are not available in a smaller device with a compatible package are listed as “No Connects”.

Each device is split into I/O banks to allow for flexibility in the choice of I/O standards (see [UG471, 7 Series FPGAs SelectIO Resources User Guide](#)). [Table 1-11](#) provides definitions for all pin types.

7 series device's flip-chip assembly materials are manufactured using ultra-low alpha (ULA) materials defined as <0.002 cph/cm² or materials that emit less than 0.002 alpha-particles per square centimeter per hour.

Device/Package Combinations and Maximum I/Os

Table 1-1 shows the maximum number of user I/Os possible in the 7 series FPGAs BGA packages. Some devices are available in both Pb and Pb-free (additional G) packages as standard ordering options.

Table 1-1: 7 Series FPGAs Package Specifications

Packages ⁽¹⁾	Description	Package Specifications			
		Package Type	Pitch (mm)	Size (mm)	Maximum I/Os ⁽²⁾
CP236/CPG236	Wire-bond chip-scale	BGA	0.5	10 x 10	106
CS324/CSG324		BGA	0.8	15 x 15	210
CS325/CSG325		BGA	0.8	15 x 15	150
FT256/FTG256	Wire-bond fine-pitch	BGA	1.0	17 x 17	170
FG484/FGG484		BGA	1.0	23 x 23	285
FG676/FGG676		BGA	1.0	27 x 27	300
SB484/SBG484/SBV484	Flip-chip lidless	BGA	0.8	19 x 19	285
FB484/FBG484/FBV484	Flip-chip lidless	BGA	1.0	23 x 23	285
RS484	Ruggedized flip-chip	BGA	0.8	19 x 19	285
RB484	Ruggedized flip-chip	BGA	1.0	23 x 23	285
FB676/FBG676/FBV676	Flip-chip lidless	BGA	1.0	27 x 27	400
RB676	Ruggedized flip-chip	BGA	1.0	27 x 27	400
RF676	Ruggedized flip-chip fine-pitch	BGA	1.0	27 x 27	400
FB900/FBG900/FBV900	Flip-chip lidless	BGA	1.0	31 x 31	500
RF900	Ruggedized flip-chip fine-pitch	BGA	1.0	31 x 31	500

Table 1-1: 7 Series FPGAs Package Specifications (Cont'd)

Packages ⁽¹⁾	Description	Package Specifications			
		Package Type	Pitch (mm)	Size (mm)	Maximum I/Os ⁽²⁾
FF676/FFG676/FFV676	Flip-chip fine-pitch	BGA	1.0	27 x 27	400
FF900/FFG900/FFV900		BGA	1.0	31 x 31	500
FF901/FFG901/FFV901		BGA	1.0	31 x 31	380
FF1156/FFG1156/FFV1156		BGA	1.0	35 x 35	600
FF1157/FFG1157/FFV1157		BGA	1.0	35 x 35	600
FF1158/FFG1158/FFV1158		BGA	1.0	35 x 35	350
FF1761/FFG1761/FFV1761		BGA	1.0	42.5 x 42.5	850
FF1926/FFG1926		BGA	1.0	45 x 45	720
FF1927/FFG1927/FFV1927		BGA	1.0	45 x 45	600
FF1928/FFG1928		BGA	1.0	45 x 45	480
FF1930/FFG1930		BGA	1.0	45 x 45	1000
FL1925/FLG1925	SSI flip-chip fine-pitch	BGA	1.0	45 x 45	1200
FL1926/FLG1926		BGA	1.0	45 x 45	720
FL1928/FLG1928		BGA	1.0	45 x 45	480
FL1930/FLG1930		BGA	1.0	45 x 45	1100
FH1761/FHG1761	SSI flip-chip fine-pitch (overhang)	BGA	1.0	45 x 45	850
RF1157	Ruggedized flip-chip fine-pitch	BGA	1.0	35 x 35	600
RF1158		BGA	1.0	35 x 35	600
RF1761		BGA	1.0	42.5 x 42.5	850
RF1930		BGA	1.0	45 x 45	1000

Notes:

1. Leaded package options are available upon request for all packages listed in this table.
2. The maximum I/O numbers do not include pins in the configuration Bank 0 (Table 1-2) or the GT serial transceivers.

Table 1-2 lists the 21 dedicated I/O pins.

Table 1-2: 7 Series FPGAs I/O Pins in the Dedicated Configuration Bank (Bank0)

DXP_0	VCCBATT_0	INIT_B_0	M0_0	TDO_0	TDI_0	GNDADC_0 ⁽¹⁾
DXN_0	DONE_0	VN_0	M1_0	TCK_0	VREFN_0	VCCADC_0 ⁽¹⁾
PROGRAM_B_0	CCLK_0	VP_0	M2_0	TMS_0	VREFP_0	CFGBVS_0

Notes:

1. In SSI technology devices, GNDADC and VCCADC do not have an _0 in the pin name.

Serial Transceiver Channels by Device/Package

Table 1-3 lists the quantity of GTP serial transceiver channels for the Artix-7 FPGAs.

Table 1-3: Serial Transceiver Channels (GTPs) by Device/Package (Artix-7 FPGAs)

Device	GTP Channels by Package												
	CPG 236	CSG 324	CSG 325	FTG 256	SBG SBV 484	FGG 484	FGG 676	FBG FBV 484	FBG FBV 676	FFG FFV 1156	RS 484	RB 484	RB 676
XC7A15T	2	0	4	0	—	4	—	—	—	—	—	—	—
XC7A35T	2	0	4	0	—	4	—	—	—	—	—	—	—
XC7A50T	2	0	4	0	—	4	—	—	—	—	—	—	—
XC7A75T	—	0	—	0	—	4	8	—	—	—	—	—	—
XC7A100T	—	0	—	0	—	4	8	—	—	—	—	—	—
XC7A200T	—	—	—	—	4	—	—	4	8	16	—	—	—
XA7A15T	2	0	4	—	—	—	—	—	—	—	—	—	—
XA7A35T	2	0	4	—	—	—	—	—	—	—	—	—	—
XA7A50T	2	0	4	—	—	—	—	—	—	—	—	—	—
XA7A75T	—	0	—	—	—	4	—	—	—	—	—	—	—
XA7A100T	—	0	—	—	—	4	—	—	—	—	—	—	—
XQ7A50T	—	—	4	—	—	4	—	—	—	—	—	—	—
XQ7A100T	—	0	—	—	—	4	—	—	—	—	—	—	—
XQ7A200T	—	—	—	—	—	—	—	—	—	—	4	4	8

Table 1-4 lists the quantity of GTX serial transceiver channels for the Kintex-7 FPGAs.

Table 1-4: Serial Transceiver Channels (GTXs) by Device/Package (Kintex-7 FPGAs)

Device	GTX Channels by Package								
	FBG484 FBV484	FBG676 FBV676	FBG900 FBV900	FFG676 FFV676	FFG900 FFV900	FFG901 FFV901	FFG1156 FFV1156	RF676	RF900
XC7K70T	4	8	—	—	—	—	—	—	—
XC7K160T	4	8	—	8	—	—	—	—	—
XC7K325T	—	8	16	8	16	—	—	—	—
XC7K355T	—	—	—	—	—	24	—	—	—
XC7K410T	—	8	16	8	16	—	—	—	—
XC7K420T	—	—	—	—	—	28	32	—	—
XC7K480T	—	—	—	—	—	28	32	—	—
XQ7K325T	—	—	—	—	—	—	—	8	16
XQ7K410T	—	—	—	—	—	—	—	8	16

Table 1-5 lists the quantity of GTX serial transceiver channels for the Virtex-7 T FPGAs.

Table 1-5: Serial Transceiver Channels (GTX) by Device/Package (Virtex-7 T FPGAs)

Device	FFG1157	FFG1761	FLG1925	FHG1761	RF1157	RF1761
XC7V585T	20	36	–	–	–	–
XC7V2000T	–	–	16	36	–	–
XQ7V585T	–	–	–	–	20	36

Table 1-6 lists the quantity of GTX and GTH serial transceiver channels for the Virtex-7 XT FPGAs. In all devices, a serial transceiver channel is one set of MGTRXP, MGTRXN, MGTTXP, and MGTTXN pins.

Table 1-6: Serial Transceiver Channels (GTX/GTH) by Device/Package (Virtex-7 XT FPGAs)

Device	FFG1157		FFG1158		FFG1761		FFG1926		FFG1927		FFG1928		FFG1930		FLG1926		FLG1928		FLG1930	
	GTX	GTH																		
XC7VX330T	0	20	–	–	0	28	–	–	–	–	–	–	–	–	–	–	–	–	–	–
XC7VX415T	0	20	0	48	–	–	–	–	0	48	–	–	–	–	–	–	–	–	–	–
XC7VX485T	20	0	48	0	28	0	–	–	56	0	–	24	0	–	–	–	–	–	–	–
XC7VX550T	–	–	0	48	–	–	–	–	0	80	–	–	–	–	–	–	–	–	–	–
XC7VX690T	0	20	0	48	0	36	0	64	0	80	–	0	24	–	–	–	–	–	–	–
XC7VX980T	–	–	–	–	0	64	–	–	0	72	0	24	–	–	–	–	–	–	–	–
XC7VX1140T	–	–	–	–	–	–	–	–	–	–	–	0	64	0	96	0	24	–	–	–
XQ7VX330T	0	20	–	–	0	28	–	–	–	–	–	–	–	–	–	–	–	–	–	–
XQ7VX485T	–	–	–	–	28	0	–	–	–	–	24	0	–	–	–	–	–	–	–	–
XQ7VX690T	0	20	0	48	0	36	–	–	–	–	0	24	–	–	–	–	–	–	–	–
XQ7VX980T	–	–	–	–	–	–	–	–	–	–	0	24	–	–	–	–	–	–	–	–

Table 1-7 shows the number of available I/Os and the number of differential I/Os for each Artix-7 device/package combination.

Table 1-7: Available I/O Pin/Device/Package Combinations for Artix-7 FPGAs

Artix-7 Devices	User I/O Pins	Artix-7 FPGA Packages: HR I/O Banks Only											
		CPG 236	CSG 324	CSG 325	FTG 256	SBG SBV 484	FGG 484	FGG 676	FBG FBV 484	FBG FBV 676	FFG FFV 1156	RB484 RS484	RB676
XC7A15T	User I/O	106	210	150	170	—	250	—	—	—	—	—	—
	Differential	104	202	144	162	—	240	—	—	—	—	—	—
XC7A35T	User I/O	106	210	150	170	—	250	—	—	—	—	—	—
	Differential	104	202	144	162	—	240	—	—	—	—	—	—
XC7A50T	User I/O	106	210	150	170	—	250	—	—	—	—	—	—
	Differential	104	202	144	162	—	240	—	—	—	—	—	—
XC7A75T	User I/O	—	210	—	170	—	285	300	—	—	—	—	—
	Differential	—	202	—	162	—	274	288	—	—	—	—	—
XC7A100T	User I/O	—	210	—	170	—	285	300	—	—	—	—	—
	Differential	—	202	—	162	—	274	288	—	—	—	—	—
XC7A200T	User I/O	—	—	—	—	285	—	—	285	400	500	—	—
	Differential	—	—	—	—	274	—	—	274	384	480	—	—
XA7A15T	User I/O	106	210	150	—	—	—	—	—	—	—	—	—
	Differential	104	202	144	—	—	—	—	—	—	—	—	—
XA7A35T	User I/O	106	210	150	—	—	—	—	—	—	—	—	—
	Differential	104	202	144	—	—	—	—	—	—	—	—	—
XA7A50T	User I/O	106	210	150	—	—	—	—	—	—	—	—	—
	Differential	104	202	144	—	—	—	—	—	—	—	—	—
XA7A75T	User I/O	—	210	—	—	—	285	—	—	—	—	—	—
	Differential	—	202	—	—	—	274	—	—	—	—	—	—
XA7A100T	User I/O	—	210	—	—	—	285	—	—	—	—	—	—
	Differential	—	202	—	—	—	274	—	—	—	—	—	—
XQ7A50T	User I/O	—	—	150	—	—	250	—	—	—	—	—	—
	Differential	—	—	144	—	—	240	—	—	—	—	—	—
XQ7A100T	User I/O	—	210	—	—	—	285	—	—	—	—	—	—
	Differential	—	202	—	—	—	274	—	—	—	—	—	—
XQ7A200T	User I/O	—	—	—	—	—	—	—	—	—	—	285	400
	Differential	—	—	—	—	—	—	—	—	—	—	274	384

Table 1-8 shows the number of available I/Os and the number of differential I/Os for each Kintex-7 device/package combination.

Table 1-8: Available I/O Pin/Device/Package Combinations for Kintex-7 FPGAs

Kintex-7 Devices	User I/O Pins	Kintex-7 FPGA Packages: HR and HP I/O Banks																	
		FBG484		FBG676		FBG900		FFG676		FFG900		FFG901		FFG1156		RF676		RF900	
		HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR
XC7K70T	User I/O	100	185	100	200	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Differential	96	176	96	192	—	—	—	—	—	—	—	—	—	—	—	—	—	—
XC7K160T	User I/O	100	185	150	250	—	—	150	250	—	—	—	—	—	—	—	—	—	—
	Differential	96	176	144	240	—	—	144	240	—	—	—	—	—	—	—	—	—	—
XC7K325T	User I/O	—	—	150	250	150	350	150	250	150	350	—	—	—	—	—	—	—	—
	Differential	—	—	144	240	144	336	144	240	144	336	—	—	—	—	—	—	—	—
XC7K355T	User I/O	—	—	—	—	—	—	—	—	—	—	0	300	—	—	—	—	—	—
	Differential	—	—	—	—	—	—	—	—	—	—	0	288	—	—	—	—	—	—
XC7K410T	User I/O	—	—	150	250	150	350	150	250	150	350	—	—	—	—	—	—	—	—
	Differential	—	—	144	240	144	336	144	240	144	336	—	—	—	—	—	—	—	—
XC7K420T	User I/O	—	—	—	—	—	—	—	—	—	—	0	380	0	400	—	—	—	—
	Differential	—	—	—	—	—	—	—	—	—	—	0	366	0	384	—	—	—	—
XC7K480T	User I/O	—	—	—	—	—	—	—	—	—	—	0	380	0	400	—	—	—	—
	Differential	—	—	—	—	—	—	—	—	—	—	0	366	0	384	—	—	—	—
XQ7K325T	User I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	150	250	150	350
	Differential	—	—	—	—	—	—	—	—	—	—	—	—	—	—	144	240	144	336
XQ7K410T	User I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	150	250	150	350
	Differential	—	—	—	—	—	—	—	—	—	—	—	—	—	—	144	240	144	336

Table 1-9 and **Table 1-10** show the number of available I/Os and the number of differential I/Os for each Virtex-7 device/package combination. When applicable, it also lists the number of user I/Os in the 3.3V-capable high-range (HR) banks and the number of 1.8V-capable high-performance (HP) banks.

Table 1-9: Available I/O Pin/Device/Package Combinations for Virtex-7 T FPGAs

Virtex-7 T Devices	User I/O Pins	Virtex-7 T FPGA Packages: HR and HP I/O Banks											
		FFG		FFG		FLG		FHG		RF		RF	
		1157		1761		1925		1761		1157		1761	
		HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR
XC7V585T	User I/O	600	0	750	100	—	—	—	—	—	—	—	—
	Differential	576	0	720	96	—	—	—	—	—	—	—	—
XC7V2000T	User I/O	—	—	—	—	1200	0	850	0	—	—	—	—
	Differential	—	—	—	—	1152	0	816	0	—	—	—	—
XQ7V585T	User I/O	—	—	—	—	—	—	—	—	600	0	750	100
	Differential	—	—	—	—	—	—	—	—	576	0	720	96

Table 1-10: Available I/O Pin/Device/Package Combinations for Virtex-7 XT FPGAs

Virtex-7 XT Devices	User I/O Pins	Virtex-7 XT FPGA Packages: HR and HP I/O Banks																	
		FFG1157		FFG1158		FFG1761		FFG 1926		FFG1927		FFG 1928		FFG1930		FLG 1926		FLG 1928	
		HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR
XC7VX330T	User I/O	600	0	—	—	650	50	—	—	—	—	—	—	—	—	—	—	—	—
	Differential	576	0	—	—	624	48	—	—	—	—	—	—	—	—	—	—	—	—
XC7VX415T	User I/O	600	0	350	0	—	—	—	—	600	0	—	—	—	—	—	—	—	—
	Differential	576	0	336	0	—	—	—	—	576	0	—	—	—	—	—	—	—	—
XC7VX485T	User I/O	600	0	350	0	700	0	—	—	600	0	—	—	700	0	—	—	—	—
	Differential	576	0	336	0	672	0	—	—	576	0	—	—	672	0	—	—	—	—
XC7VX550T	User I/O	—	—	350	0	—	—	—	—	600	0	—	—	—	—	—	—	—	—
	Differential	—	—	336	0	—	—	—	—	576	0	—	—	—	—	—	—	—	—
XC7VX690T	User I/O	600	0	350	0	850	0	720	0	600	0	—	—	1000	0	—	—	—	—
	Differential	576	0	336	0	816	0	690	0	576	0	—	—	960	0	—	—	—	—
XC7VX980T	User I/O	—	—	—	—	720	0	—	—	480	0	900	0	—	—	—	—	—	—
	Differential	—	—	—	—	690	0	—	—	460	0	864	0	—	—	—	—	—	—
XC7VX1140T	User I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	720	0	480	0	110 0
	Differential	—	—	—	—	—	—	—	—	—	—	—	—	—	690	0	460	0	105 6

Table 1-10: Available I/O Pin/Device/Package Combinations for Virtex-7 XT FPGAs (Cont'd)

Virtex-7 XT Devices	User I/O Pins	Virtex-7 XT FPGA Packages: HR and HP I/O Banks																	
		FFG1157		FFG1158		FFG1761		FFG 1926		FFG1927		FFG 1928		FFG1930		FLG 1926		FLG 1928	
		FFV1157	RF1157	FFV1158	RF1158	FFV1761	RF1761	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR
XQ7VX330T	User I/O	600	0	—	—	650	50	—	—	—	—	—	—	—	—	—	—	—	
	Differential	576	0	—	—	624	48	—	—	—	—	—	—	—	—	—	—	—	
XQ7VX485T	User I/O	—	—	—	—	700	0	—	—	—	—	700	0	—	—	—	—	—	
	Differential	—	—	—	—	672	0	—	—	—	—	672	0	—	—	—	—	—	
XQ7VX690T	User I/O	600	0	350	0	850	0	—	—	—	—	1000	0	—	—	—	—	—	
	Differential	576	0	336	0	816	0	—	—	—	—	960	0	—	—	—	—	—	
XQ7VX980T	User I/O	—	—	—	—	—	—	—	—	—	—	900	0	—	—	—	—	—	
	Differential	—	—	—	—	—	—	—	—	—	—	864	0	—	—	—	—	—	

Pin Definitions

Table 1-11 lists the pin definitions used in 7 series FPGAs packages.

Note: There are dedicated general purpose user I/O pins listed separately in Table 1-11. There are also multi-function pins where the pin names start with either IO_LXXY_ZZZ_# or IO_XX_ZZZ_#, where ZZZ represents one or more functions in addition to being general purpose user I/O. If not used for their special function, these pins can be user I/O.

Table 1-11: 7 Series FPGAs Pin Definitions

Pin Name	Type	Direction	Description
User I/O Pins			
IO_LXXY_# IO_XX_#	Dedicated	Input/ Output	<p>Most user I/O pins are capable of differential signaling and can be implemented as pairs. The top and bottom I/O pins are always single ended. Each user I/O is labeled IO_LXXY_#, where:</p> <ul style="list-style-type: none"> • IO indicates a user I/O pin. • L indicates a differential pair, with XX a unique pair in the bank and Y = [P N] for the positive/negative sides of the differential pair. • # indicates a bank number.
Configuration Pins			
For more information, see the Configuration Pin Definitions table in UG470 , 7 Series FPGAs Configuration User Guide.			
CCLK_0	Dedicated ⁽¹⁾	Input/ Output	Configuration clock. Output in Master mode or input in Slave mode.
DONE_0	Dedicated ⁽¹⁾	Bidirectional	DONE indicates successful completion of configuration (active High).
INIT_B_0	Dedicated ⁽¹⁾	Bidirectional (open-drain)	Indicates initialization of configuration memory (active Low).

Table 1-11: 7 Series FPGAs Pin Definitions (Cont'd)

Pin Name	Type	Direction	Description
M0_0, M1_0, or M2_0	Dedicated ⁽¹⁾	Input	Configuration mode selection.
PROGRAM_B_0	Dedicated ⁽¹⁾	Input	Asynchronous reset to configuration logic (active Low).
TCK_0	Dedicated ⁽¹⁾	Input	JTAG clock.
TDI_0	Dedicated ⁽¹⁾	Input	JTAG data input.
TDO_0	Dedicated ⁽¹⁾	Output	JTAG data output.
TMS_0	Dedicated ⁽¹⁾	Input	JTAG mode select.
CFGBVS_0	Dedicated ⁽¹⁾	Input	This pin selects the preconfiguration I/O standard type for the dedicated and multi-function configuration banks 0, 14, and 15. If the V _{CCO} for banks 0, 14, or 15 is 2.5V or 3.3V, then this pin must be connected to V _{CCO_0} . If the V _{CCO} for banks 0, 14, and 15 are less than or equal to 1.8V, then this pin should be connected to GND. Note: To avoid device damage, this pin must be connected correctly. See the <i>Configuration Banks Voltage Select</i> section in UG470, 7 Series FPGAs Configuration User Guide for more information.
D00 through D31	Multi-function	Bidirectional	Configuration data pins.
ADV_B	Multi-function	Output	BPI Flash address valid output (active Low).
A00 through A28	Multi-function	Output	Address A00–A28 BPI address output.
RS0 or RS1	Multi-function	Output	RS0 and RS1 revision select output.
FCS_B	Multi-function	Output	BPI and SPI flash chip select (active Low).
FOE_B	Multi-function	Output	BPI flash output enable (active Low).
MOSI	Multi-function	Output	SPI flash command output. Also known as the SPI bus master output, slave input signal.
FWE_B	Multi-function	Output	BPI flash write enable (active Low).
DOUT	Multi-function	Output	Data output for serial daisy-chain configuration.
CSO_B	Multi-function	Output	Chip-select output for parallel daisy-chain (active Low).
CSI_B	Multi-function	Input	SelectMAP chip-select input (active Low).
PUDC_B	Multi-function	Input	Pull-Up During Configuration (bar) PUDC_B input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration (active Low). <ul style="list-style-type: none">• When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin.• When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin. PUDC_B must be tied either directly (or through a 1KΩ or less resistor) to V _{CCO_14} or GND. Do not allow this pin to float before and during configuration.

Table 1-11: 7 Series FPGAs Pin Definitions (Cont'd)

Pin Name	Type	Direction	Description
RDWR_B	Multi-function	Input	SelectMAP data bus direction control signal for reading (active High) or writing (active Low) configuration data.
EMCCLK	Multi-function	Input	External master configuration clock.
Power/Ground Pins			
GND	Dedicated	N/A	Ground.
VCCAUX	Dedicated	N/A	1.8V power-supply pins for auxiliary circuits.
VCCAUX_IO_G# ⁽²⁾	Dedicated	N/A	1.8V/2.0V power-supply pins for auxiliary I/O circuits.
VCCINT	Dedicated	N/A	0.9V/1.0V power-supply pins for the internal core logic.
VCCO_# ⁽³⁾	Dedicated	N/A	Power-supply pins for the output drivers (per bank).
VCCBRAM	Dedicated	N/A	1.0V power-supply pins for the FPGA logic block RAM.
VCCBATT_0	Dedicated	N/A	Decryptor key memory backup supply; this pin should be tied to the appropriate V _{CC} or GND when not used ⁽⁴⁾ .
VREF	Multi-function	N/A	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Analog to Digital Converter (XADC) Pins			
For more information, see the XADC Package Pins table in UG480, 7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide .			
VCCADC_0 ⁽⁵⁾⁽⁶⁾	Dedicated	N/A	XADC analog positive supply voltage.
GNDADC_0 ⁽⁵⁾⁽⁶⁾	Dedicated	N/A	XADC analog ground reference.
VP_0 ⁽⁵⁾	Dedicated	Input	XADC dedicated differential analog input (positive side).
VN_0 ⁽⁵⁾	Dedicated	Input	XADC dedicated differential analog input (negative side).
VREFP_0 ⁽⁵⁾	Dedicated	N/A	1.25V reference input.
VREFN_0 ⁽⁵⁾	Dedicated	N/A	1.25V reference GND reference.
AD0P through AD15P AD0N through AD15N	Multi-function	Input	XADC (analog-to-digital converter) differential auxiliary analog inputs 0–15. Auxiliary channels 6, 7, 13, 14, and 15 are not supported on Kintex-7 devices.
Multi-gigabit Serial Transceiver Pins (GTPE2, GTXE2, and GTHE2)			
For more information on the GTPE2 pins see the <i>Pin Description and Design Guidelines</i> section in UG482, 7 Series FPGAs GTP Transceivers User Guide . For more information on the GTXE2 and GTHE2 pins see the <i>Pin Description and Design Guidelines</i> section in UG476, 7 Series FPGAs GTX/GTH Transceivers User Guide .			
MGTPRXP[0:3]	Dedicated	Input	Positive differential receive port GTP Quad.
MGTPRXN[0:3]	Dedicated	Input	Negative differential receive port GTP Quad.
MGTPTXP[0:3]	Dedicated	Output	Positive differential transmit port GTP Quad.
MGTPTXN[0:3]	Dedicated	Output	Negative differential transmit port GTP Quad.

Table 1-11: 7 Series FPGAs Pin Definitions (Cont'd)

Pin Name	Type	Direction	Description
MGTXRXP[0:3]	Dedicated	Input	Positive differential receive port GTX Quad.
MGTXRXN[0:3]	Dedicated	Input	Negative differential receive port GTX Quad.
MGTXTP[0:3]	Dedicated	Output	Positive differential transmit port GTX Quad.
MGTXTN[0:3]	Dedicated	Output	Negative differential transmit port GTX Quad.
MGTHRXP[0:3]	Dedicated	Input	Positive differential receive port GTH Quad.
MGTHRXN[0:3]	Dedicated	Input	Negative differential receive port GTH Quad.
MGTHTXP[0:3]	Dedicated	Output	Positive differential transmit port GTH Quad.
MGTHTXN[0:3]	Dedicated	Output	Negative differential transmit port GTH Quad.
MGTAVCC_G# ⁽⁷⁾	Dedicated	Input	1.0V analog power-supply pin for the receiver and transmitter internal circuits.
MGTAVTT_G# ⁽⁷⁾	Dedicated	Input	1.2V analog power-supply pin for the transmit driver.
MGTVCVCAUX_G# ⁽⁷⁾	Dedicated	Input	1.8V auxiliary analog Quad PLL (QPLL) voltage supply for the transceivers.
MGTREFCLK0/1P	Dedicated	Input	Positive differential reference clock for the transceivers.
MGTREFCLK0/1N	Dedicated	Input	Negative differential reference clock for the transceivers.
MGTAVTTRCAL	Dedicated	N/A	Precision reference resistor pin for internal calibration termination. Not used for Artix-7 devices.
MGTRREF	Dedicated	Input	Precision reference resistor pin for internal calibration termination.
Other Pins			
MRCC	Multi-function	Input	These are the clock capable I/Os driving BUFRs, BUFIOs, BUFGs, and MMCMs/PLLs. In addition, these pins can drive the BUFMR for multi-region BUFIO and BUFR support. These pins become regular user I/Os when not needed as a clock. When connecting a single-ended clock to the differential CC pair of pins, it must be connected to the positive (P) side of the pair. The MRCC (multi-region) pins, when used as single region resource, can drive four BUFIOs and four BUFR in a single bank.
SRCC	Multi-function	Input	These are the clock capable I/Os driving BUFRs, BUFIOs, BUFGs, and MMCMs/PLLs. These pins become regular user I/Os when not needed for clocks. When connecting a single-ended clock to the differential CC pair of pins, it must be connected to the positive (P) side of the pair. The SRCC (single region) pins can drive four BUFIOs and four BUFRs in a single bank.
VRN ⁽⁸⁾	Multi-function	N/A	This pin is for the DCI voltage reference resistor of N transistor (per bank, to be pulled High with reference resistor).

Table 1-11: 7 Series FPGAs Pin Definitions (Cont'd)

Pin Name	Type	Direction	Description
VRP ⁽⁸⁾	Multi-function	N/A	This pin is for the DCI voltage reference resistor of P transistor (per bank, to be pulled Low with reference resistor).
DXP_0, DXN_0	Dedicated	Input	Temperature-sensing diode pins (Anode: DXP; Cathode: DXN). The thermal diode is accessed by using the DXP and DXN pins in bank 0. When not used, tie to GND. To use the thermal diode an appropriate external thermal monitoring IC must be added. Consult the external thermal monitoring IC data sheet for usage guidelines. The recommended temperature monitoring solution for 7 series FPGAs uses the temperature sensor in the XADC block.
T0, T1, T2, or T3	Multi-function	Input	This pin belongs to the memory byte group 0-3.
T0_DQS, T1_DQS, T2_DQS, or T3_DQS	Multi-function	Input	The DDR DQS strobe pin that belongs to the memory byte group T0-T3.

Notes:

1. All dedicated pins (JTAG and configuration) are powered by V_{CCO_0}.
2. For devices that do not include VCCAUX_IO_G# pins, auxiliary I/O circuits are powered by VCCAUX pins. As indicated in [Chapter 2, 7 Series FPGAs Package Files](#), some packages include VCCAUX_IO_G# pins but also have auxiliary I/O circuits powered by VCCAUX pins. In this case, the VCCAUX_IO_G# pins exist for migration purposes only and will not connect to any internal circuitry. When planning to migrate to a device that utilizes VCCAUX_IO_G#, these pins must be connected to the desired voltage (1.8V/2.0V). Otherwise, they can be tied to V_{CCAU}X or left unconnected.
3. V_{CCO} pins in unbonded banks must be connected to the V_{CCO} for that bank for package migration. Do NOT connect unbonded V_{CCO} pins to different supplies. Without a package migration requirement, V_{CCO} pins in unbonded banks can be tied to a common supply (V_{CCO} or ground).
4. Refer to the data sheet for V_{CCBATT_0} specifications.
5. See [UG480, 7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide](#) for the default connections required to support on-chip monitoring.
6. In SSI technology devices, GNDADC and VCCADC do not have an _0 in the pin name.
7. In packages with only one MGT power group, the MGTAVCC_G#, MGTAVTT_G#, and MGTVCXAUX_G# pins are labeled without the _G#. These pins also appear without a number in the power and GND placement diagrams in [Chapter 3, Device Diagrams](#).
8. The DCI guidelines in the 7 series FPGAs are different from previous Virtex device DCI guidelines. See the DCI sections in [UG471, 7 Series FPGAs SelectIO Resources User Guide](#) for more information on the VRN/VRP pins.

Pin Compatibility Between Packages

7 series FPGA devices are pin compatible only with other 7 series FPGA devices of the same family (Artix-7, Kintex-7, and Virtex-7) in the same package. In addition, FB/FBG/ FBV, FF/FFG/FFV, FH/FHG, FL/FLG, RB, RF, and RS packages of the same pin-count designator are pin compatible. Also, in Artix-7 devices the FGG and FBG packages are pin compatible.

Note: Pin compatible packages can have substantially different decoupling capacitor recommendations.

Some FB/FBG/FBV and RB packages include V_{CCAU}X_IO pins that are not utilized by the I/O. These pins are placeholders to ensure pin compatibility with FF/FFG/FFV and RF packages. In the FF/FFG/FFV and RF packages, when the high-performance option is chosen for the HP I/O banks, the V_{CCAU}X_IO pins must be connected to a separate power supply from V_{CCAU}X. Therefore, to allow for migration to the FF/FFG/FFV and RF packages, V_{CCAU}X_IO must be connected to the appropriate voltage/regulator.

Die Level Bank Numbering Overview

Banking and Clocking Summary

- The center clocking backbone contains all vertical clock tracks and clock buffer connectivity.
- The CMT backbone contains all vertical CMT connectivity and is located in the CMT column.
- Not all banks are bonded out in every part/package combination.
- GTP/GTX/GTH columns summary
 - One GT Quad = Four transceivers = Four GTPE2 or GTXE2 or GTHE2 primitives.
 - Not all GT Quads are bonded out in every package.
- I/O banks summary
 - Each bank has four pairs of clock capable (CC) inputs for four differential or four single ended clock inputs.
 - Can connect to the CMT in the same region and the region above and below (with restrictions).
 - Two MRCC pairs can connect to the BUFRs and BUFIOs in the same region/banks and the regions/banks above and below.
 - Two SRCC pairs can only connect to the BUFRs and BUFIOs in the same region/bank.
 - There are no global clock pins (GC pins) in the 7 series FPGAs.
 - Each user I/O bank has 50 single-ended I/Os or 24 differential pairs (48 differential I/Os). The top and bottom I/O pin are always single ended. All 50 pads of a bank are not always bonded out to pins.
 - Bank locations of dedicated and dual-purpose pins
 - In most devices, banks 14 and 15 always contain the dual-purpose configuration pins. Bank 15 and 35 contains the XADC auxiliary inputs; however, in Kintex-7 devices, the auxiliary inputs are only in bank 15. Bank 0 contains the dedicated configuration pins.
 - All dedicated configuration I/Os (bank 0) are 3.3V capable.
 - The multi-function configuration banks 14 and 15 are restricted during configuration. The SSI technology devices (XC7VX1140T and XC7V2000T) pins in banks 11, 12, 17, 18, 20, and 21 are restricted, similar to multi-function pins. Pins in these banks do not have configuration functions. Because there are architectural differences between these and other banks, special consideration must be taken. For more information, see the *State of I/Os During and After Configuration* and the *Special DCI Requirements for Some Banks* sections of [UG471, 7 Series FPGAs SelectIO Resources User Guide](#).
 - The physical XY locations for each IDELAYCTRL start at X0Y0 in the bottom left-most bank. The locations then increment by one starting with the lowest bank number in each column in the vertical Y direction and by one for each column in the horizontal X direction. IDELAYCTRLs are located in each of the HROWS.

This section visually describes the die level bank numbering.

- Artix-7 devices on [page 30](#) through [page 34](#)
- Kintex-7 devices on [page 35](#) through [page 41](#)
- Virtex-7 T devices (XC7V585T and XC7V2000T) on [page 42](#) through [page 44](#)
- Virtex-7 XT devices (XC7VX330T, XC7VX415T, XC7VX485T, XC7VX550T, XC7VX690T, XC7VX980T, and XC7VX1140T) on [page 45](#) through [page 55](#)

XC7A15T, XC7A35T, XA7A15T, and XA7A35T Banks

Figure 1-1 shows the I/O and transceiver banks.

CPG236 Package

- HR I/O bank 15 is not bonded out.
- HR I/O banks 16, 34, and 35 are partially bonded out.

FTG256 Package (XC7A15T and XC7A35T only)

- HR I/O bank 16 is not bonded out.
- HR I/O bank 34 is partially bonded out.
- The GTP Quad 216 is not bonded out.

CSG324 Package

- HR I/O bank 16 is partially bonded out.
- The GTP Quad 216 is not bonded out.

CSG325 Package

- HR I/O banks 16 and 35 are not bonded out.
- All GTP Quads are fully bonded out in this package.

FGG484 Package (XC7A15T and XC7A35T only)

- All HR I/O banks and the GTP Quads are fully bonded out in this package.

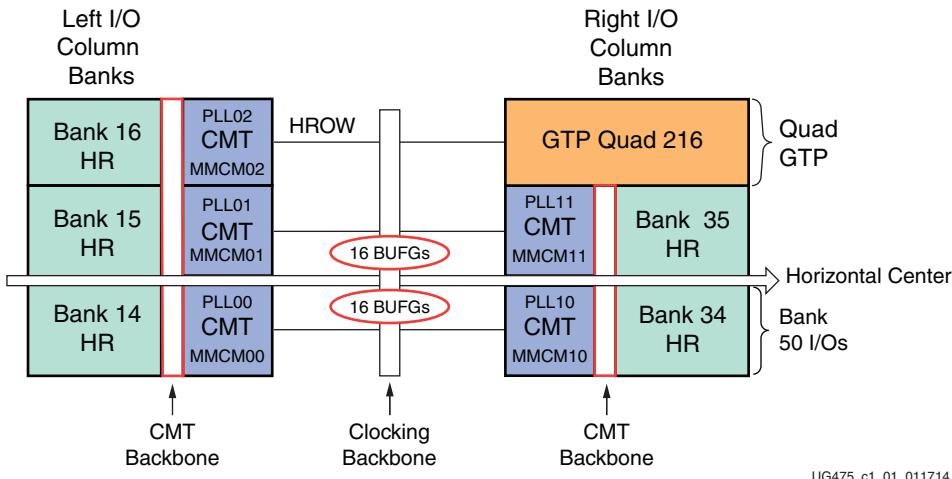


Figure 1-1: XC7A15T, XC7A35T, XA7A15T, and XA7A35T Banks

XC7A50T, XA7A50T, and XQ7A50T Banks

Figure 1-2 shows the I/O and transceiver banks.

CPG236 Package

- HR I/O bank 15 is not bonded out.
- HR I/O banks 16, 34, and 35 are partially bonded out.

FTG256 Package (XC7A50T only)

- HR I/O bank 16 is not bonded out.
- HR I/O bank 34 is partially bonded out.
- The GTP Quad 216 is not bonded out.

CSG324 Package

- HR I/O bank 16 is partially bonded out.
- The GTP Quad 216 is not bonded out.

CSG325 Package

- HR I/O banks 16 and 35 are not bonded out.
- All GTP Quads are fully bonded out in this package.

FGG484 Package (XC7A50T and XQ7A50T only)

- All HR I/O banks and the GTP Quads are fully bonded out in this package.

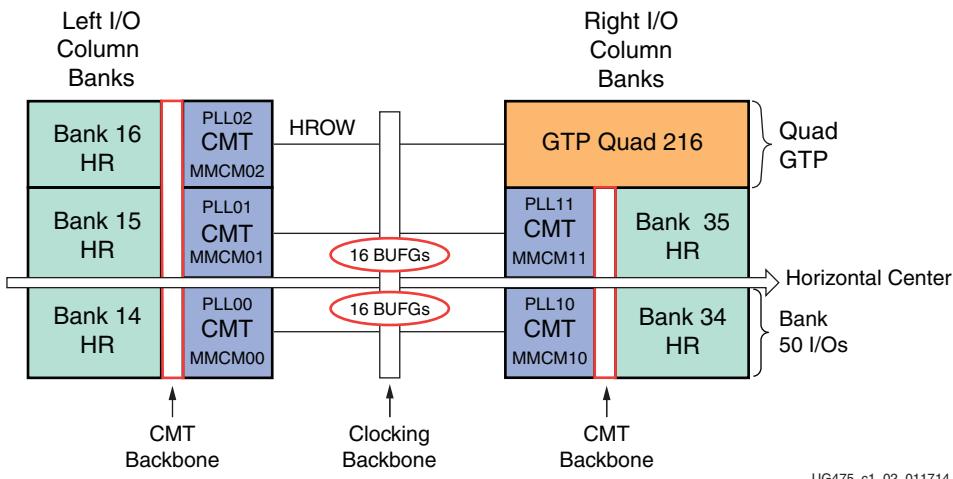


Figure 1-2: XC7A50T, XA7A50T, and XQ7A50T Banks

XC7A75T and XA7A75T Banks

Figure 1-3 shows the I/O and transceiver banks.

FTG256 Package (XC7A75T only)

- HR I/O banks 13 and 16 are not bonded out.
- HR I/O bank 34 is partially bonded out.
- The GTP Quads 213 and 216 are not bonded out.

CSG324 Package

- HR I/O bank 13 is not bonded out.
- HR I/O bank 16 is partially bonded out.
- The GTP Quads 213 and 216 are not bonded out.

FGG484 Package

- HR I/O bank 13 is partially bonded out.
- The GTP Quad 213 is not bonded out.

FGG676 Package (XC7A75T only)

- All HR I/O banks and the GTP Quads are fully bonded out in this package.

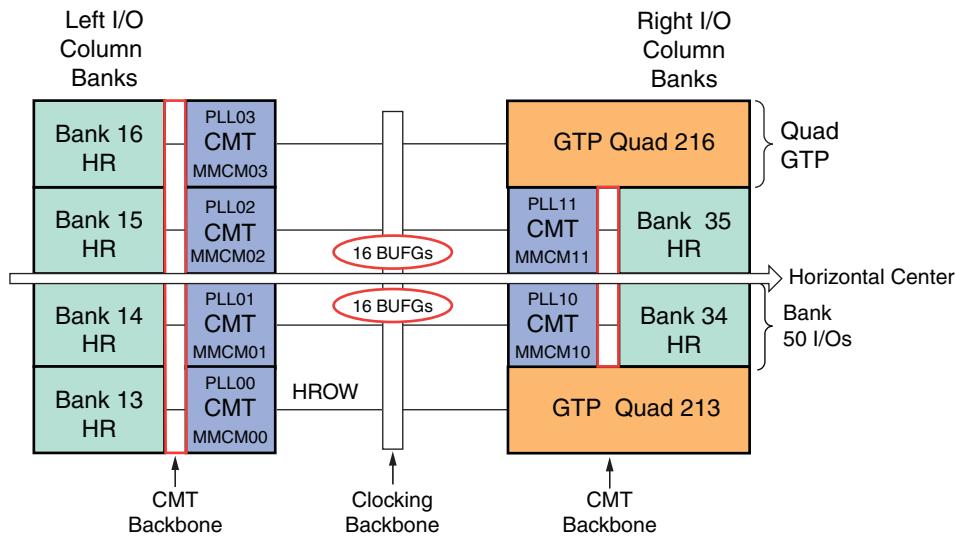


Figure 1-3: XC7A75T and XA7A75T Banks

XC7A100T, XQ7A100T, and XA7A100T Banks

Figure 1-4 shows the I/O and transceiver banks.

FTG256 Package (XC7A100T only)

- HR I/O banks 13 and 16 are not bonded out.
- HR I/O bank 34 is partially bonded out.
- The GTP Quads 213 and 216 are not bonded out.

CSG324 Package

- HR I/O bank 13 is not bonded out.
- HR I/O bank 16 is partially bonded out.
- The GTP Quads 213 and 216 are not bonded out.

FGG484 Package

- HR I/O bank 13 is partially bonded out.
- The GTP Quad 213 is not bonded out.

FGG676 Package (XC7A100T only)

- All HR I/O banks and the GTP Quads are fully bonded out in this package.

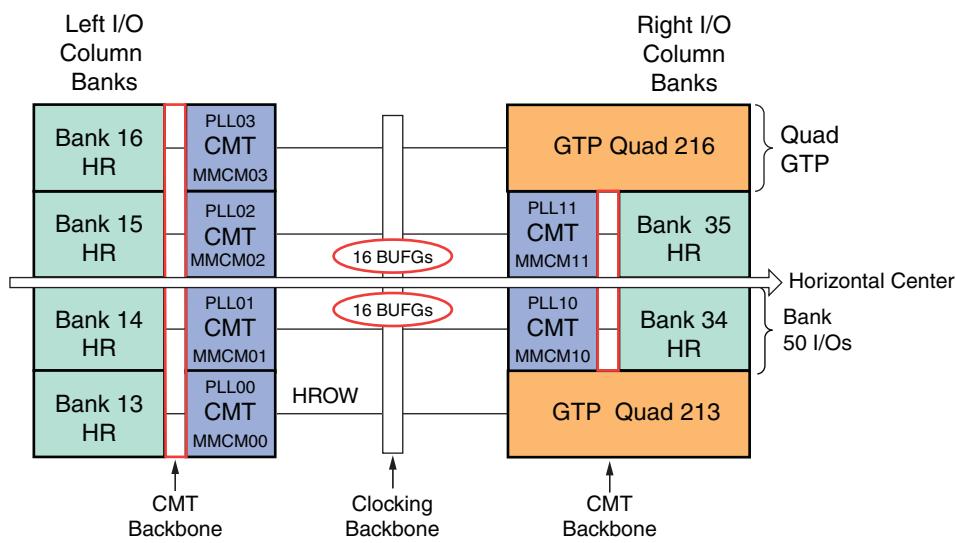


Figure 1-4: XC7A100T, XQ7A100T, and XA7A100T Banks

XC7A200T and XQ7A200T Banks

Figure 1-5 shows the I/O and transceiver banks.

SBG484, SBV484, and RS484 Packages

- HR I/O bank 13 is partially bonded out.
- HR I/O banks 12, 32, 33, and 36 are not bonded out.
- The GTP Quads 113, 116, and 213 are not bonded out.

FBG484, FBV484, and RB484 Packages

- HR I/O bank 13 is partially bonded out.
- HR I/O banks 12, 32, 33, and 36 are not bonded out.
- The GTP Quads 113, 116, and 213 are not bonded out.

FBG676, FBV676, and RB676 Packages

- HR I/O banks 32 and 36 are not bonded out.
- The GTP Quads 113 and 116 are not bonded out.

FFG1156 and FFV1156 Packages (XC7A200T only)

- All HR I/O banks and the GTP Quads are fully bonded out in this package.

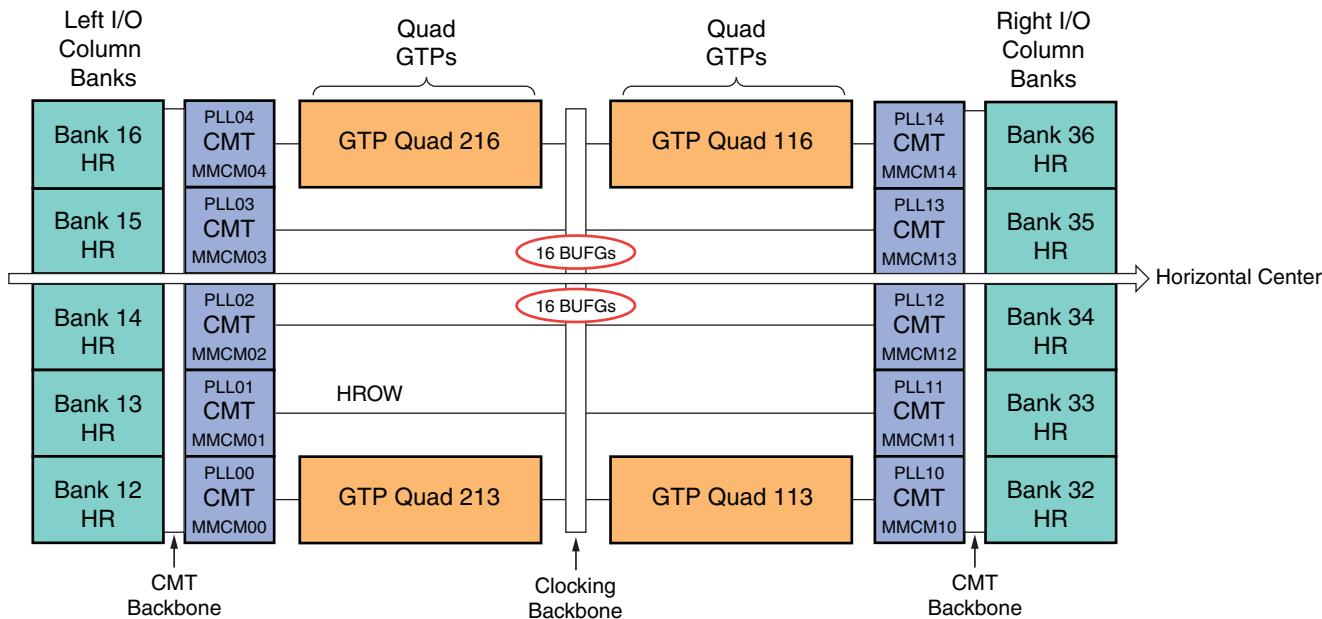


Figure 1-5: XC7A200T and XQ7A200T Banks

XC7K70T Banks

Figure 1-6 shows the I/O and transceiver banks for the XC7K70T.

FBG484 and FBV484 Packages

- HR I/O bank 16 is partially bonded out.
- All HP I/O banks are fully bonded out.
- The GTX Quad 116 is not bonded out.

FBG676 and FBV676 Packages

- All HR and HP I/O banks and the GTX Quads are fully bonded out in this package.

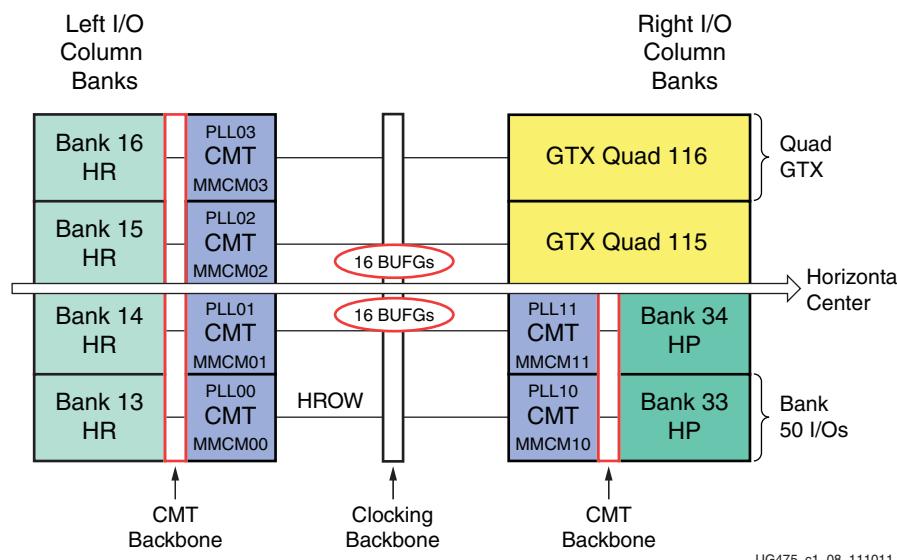


Figure 1-6: XC7K70T Banks

XC7K160T Banks

Figure 1-7 shows the I/O and transceiver banks for the XC7K160T.

FBG484 and FBV484 Packages

- HR I/O bank 12 is not bonded out and bank 16 is partially bonded out.
- HP I/O bank 32 is not bonded out.
- The GTX Quad 116 is not bonded out.

FBG676, FBV676, FFG676, and FFV676 Packages

- All HR and HP I/O banks and the GTX Quads are fully bonded out in these packages.

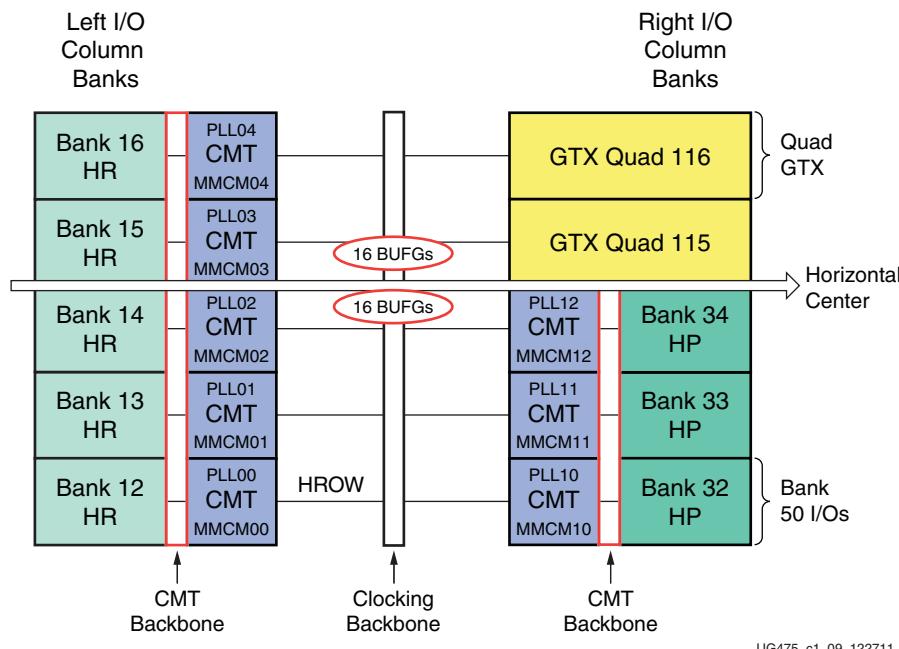


Figure 1-7: XC7K160T Banks

XC7K325T and XQ7K325T Banks

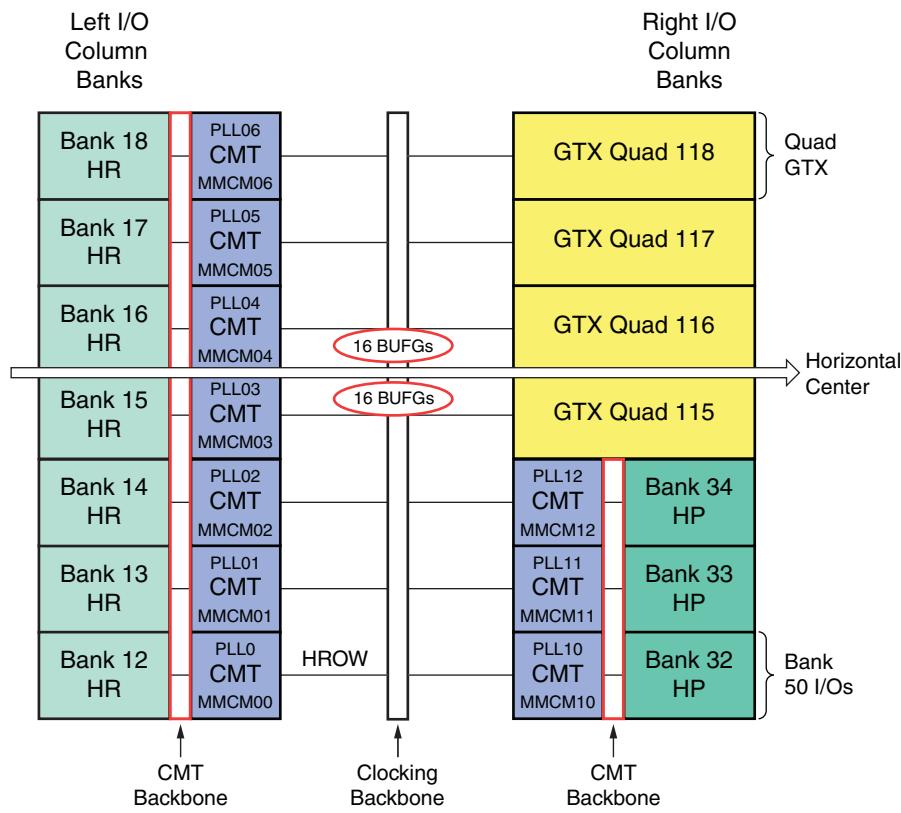
Figure 1-8 shows the I/O and transceiver banks for the XC7K325T and XQ7K325T.

FBG676, FBV676, FFG676, FFV676, and RF676 Packages

- HR I/O banks 17 and 18 are not bonded out.
- All HP I/O banks are fully bonded out.
- GTX Quads 117 and 118 are not bonded out.

FBG900, FBV900, FFG900, FFV900, and RF900 Packages

All HR and HP I/O banks and the GTX Quads are fully bonded out in these packages.



UG475_c1_10_081211

Figure 1-8: XC7K325T and XQ7K325T Banks

XC7K355T Banks

[Figure 1-9](#) shows the I/O and transceiver banks for the XC7K355T.

FFG901 and FFV901 Packages

All HR I/O banks and the GTX Quads are fully bonded out in this package.

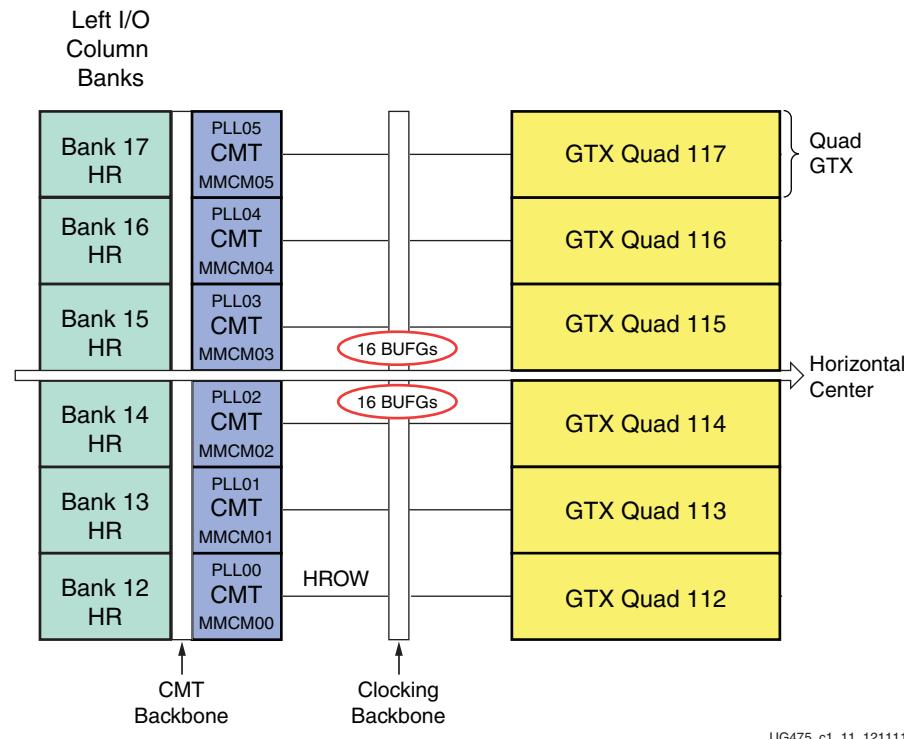


Figure 1-9: XC7K355T Banks

XC7K410T and XQ7K410T Banks

Figure 1-10 shows the I/O and transceiver banks for the XC7K410T and XQ7K410T.

FBG676, FBV676, FFG676, FFV676, and RF676 Packages

- HR I/O banks 17 and 18 are not bonded out.
- All HP I/O banks are fully bonded out.
- GTX Quads 117 and 118 are not bonded out.

FBG900, FBV900, FFG900, FFV900, and RF900 Packages

All HR and HP I/O banks and the GTX Quads are fully bonded out in these packages.

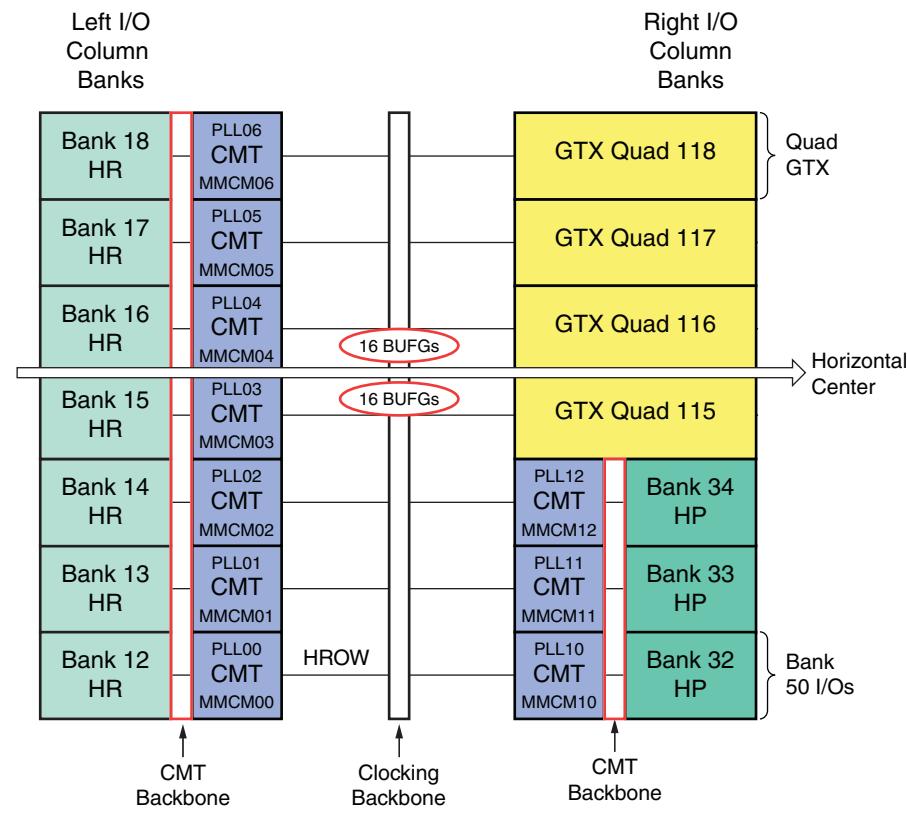


Figure 1-10: XC7K410T and XQ7K410T Banks

XC7K420T Banks

Figure 1-11 shows the I/O and transceiver banks for the XC7K420T.

FFG901 and FFV901 Packages

- HR I/O bank 18 is not fully bonded out.
- GTX Quad 118 is not bonded out.

FFG1156 and FFV1156 Packages

- All HR I/O banks and the GTX Quads are fully bonded out in this package.

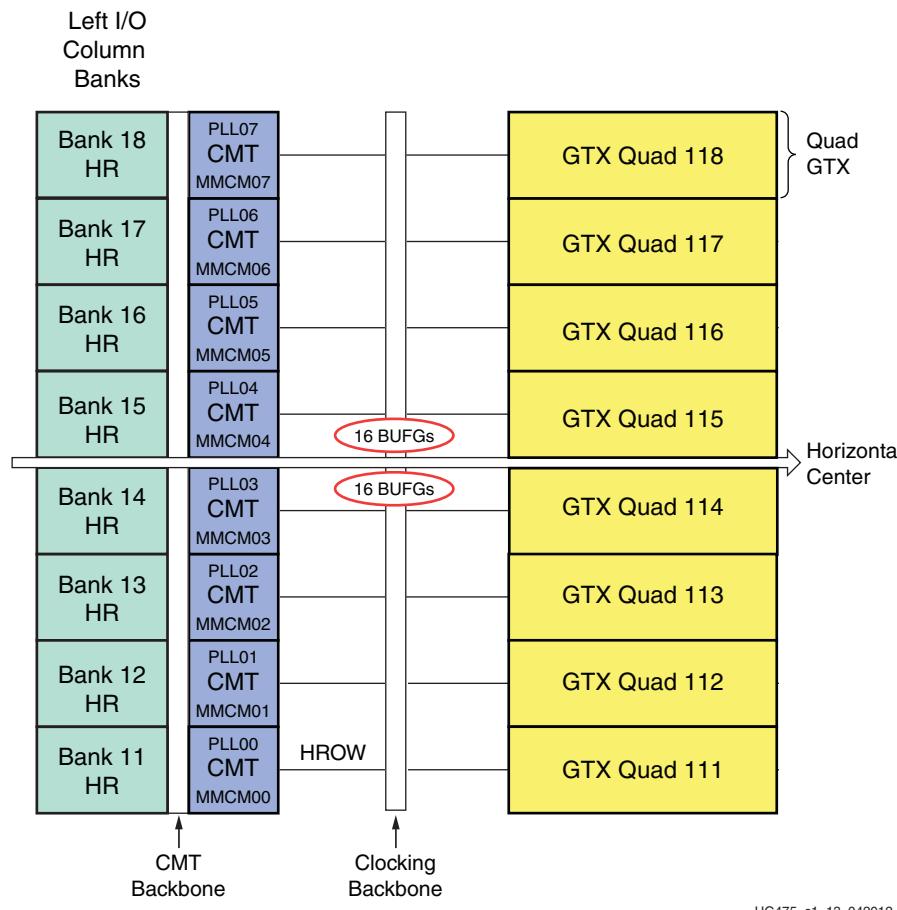


Figure 1-11: XC7K420T Banks

XC7K480T Banks

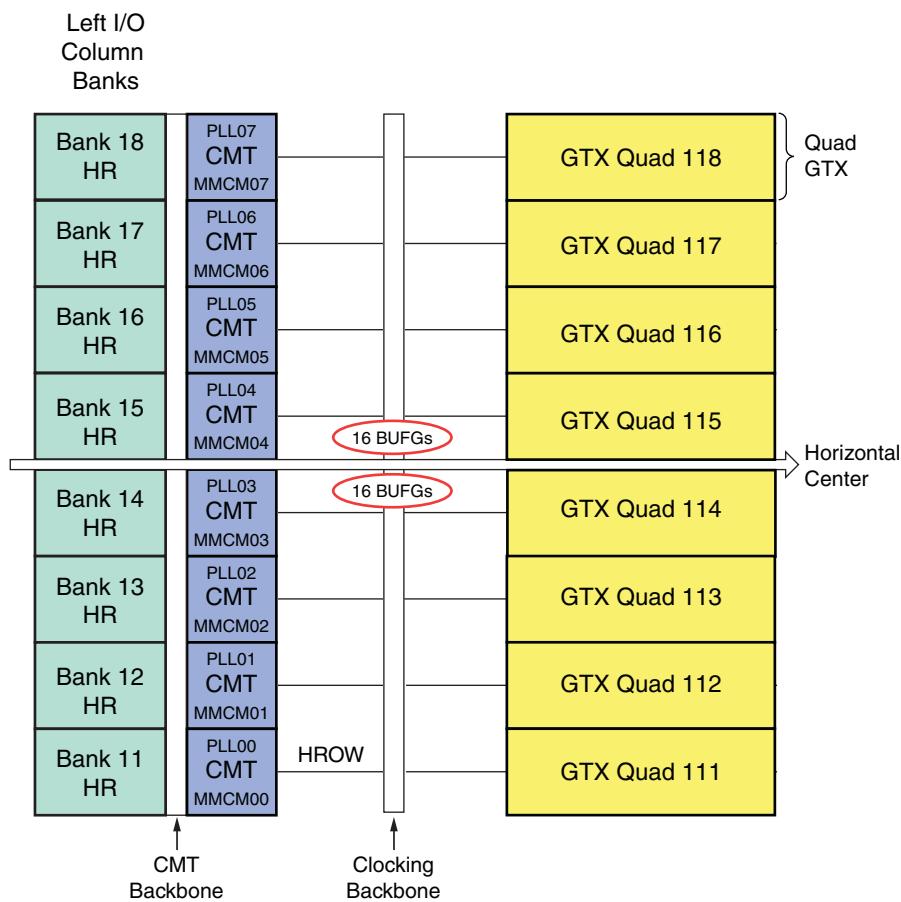
Figure 1-12 shows the I/O and transceiver banks for the XC7K480T.

FFG901 and FFV901 Packages

- HR I/O bank 18 is not fully bonded out.
- GTX Quad 118 is not bonded out.

FFG1156 and FFV1156 Packages

- All HR I/O banks and the GTX Quads are fully bonded out in this package.



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Figure 1-12: XC7K480T Banks

XC7V585T and XQ7V585T Banks

Figure 1-13 shows the I/O and transceiver banks for the XC7V585T and XQ7V585T.

FFG1157 and RF1157 Packages

- All HR I/O banks (11, 12, and 13) are not bonded out.
- HP I/O banks 31, 32, and 33 are not bonded out.
- GTX Quads 111, 112, 113, and 119 are not bonded out.

FFG1761 and RF1761 Packages

- HR I/O bank 11 is not bonded out.
- All HP I/O banks and the GTX Quads are fully bonded out in these packages.

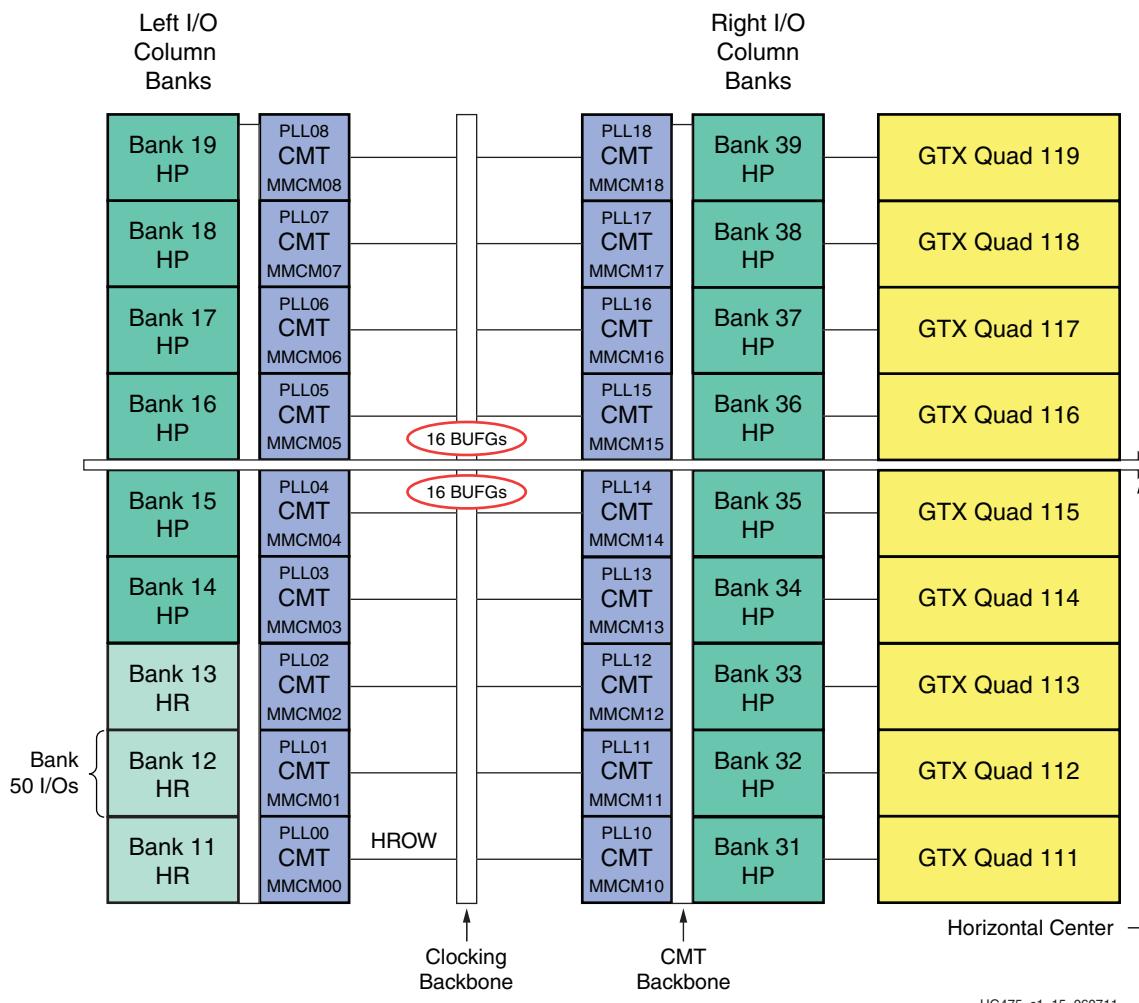


Figure 1-13: XC7V585T and XQ7V585T Banks

XC7V2000T Banks

Figure 1-14 shows the I/O and transceiver banks for the XC7V2000T.

FHG1761 Package

- HP I/O banks 11, 20, 21, 22, 40, 41, and 42 are not bonded out.
- GTX Quads 120, 121, and 122 are not bonded out.

FLG1925 Package

- All HP I/O banks are fully bonded out in this package.
- GTX Quads 111, 116, 117, 118, 119, 120, 121, and 122 are not bonded out.

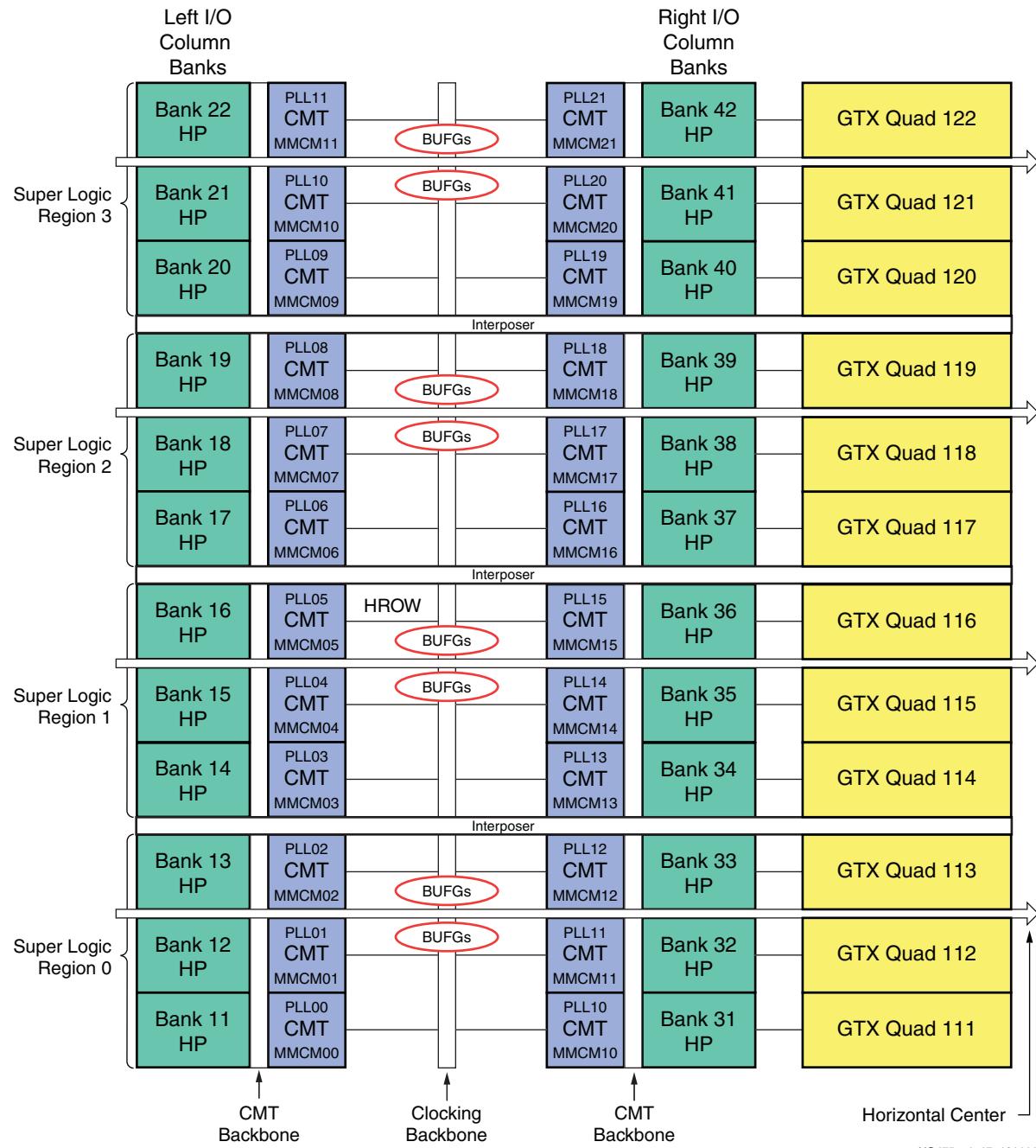


Figure 1-14: XC7V2000T Banks

XC7VX330T and XQ7VX330T Banks

Figure 1-15 shows the I/O and transceiver banks for the XC7VX330T and XQ7VX330T.

FFG1157, FFV1157, and RF1157 Packages

- HR I/O bank 13 is not bonded out.
- HP I/O bank 33 is not bonded out.
- GTH Quads 113 and 119 are not bonded out.

FFG1761, FFV1761, and RF1761 Packages

All HR and HP I/O banks and the GTH Quads are fully bonded out in these packages.

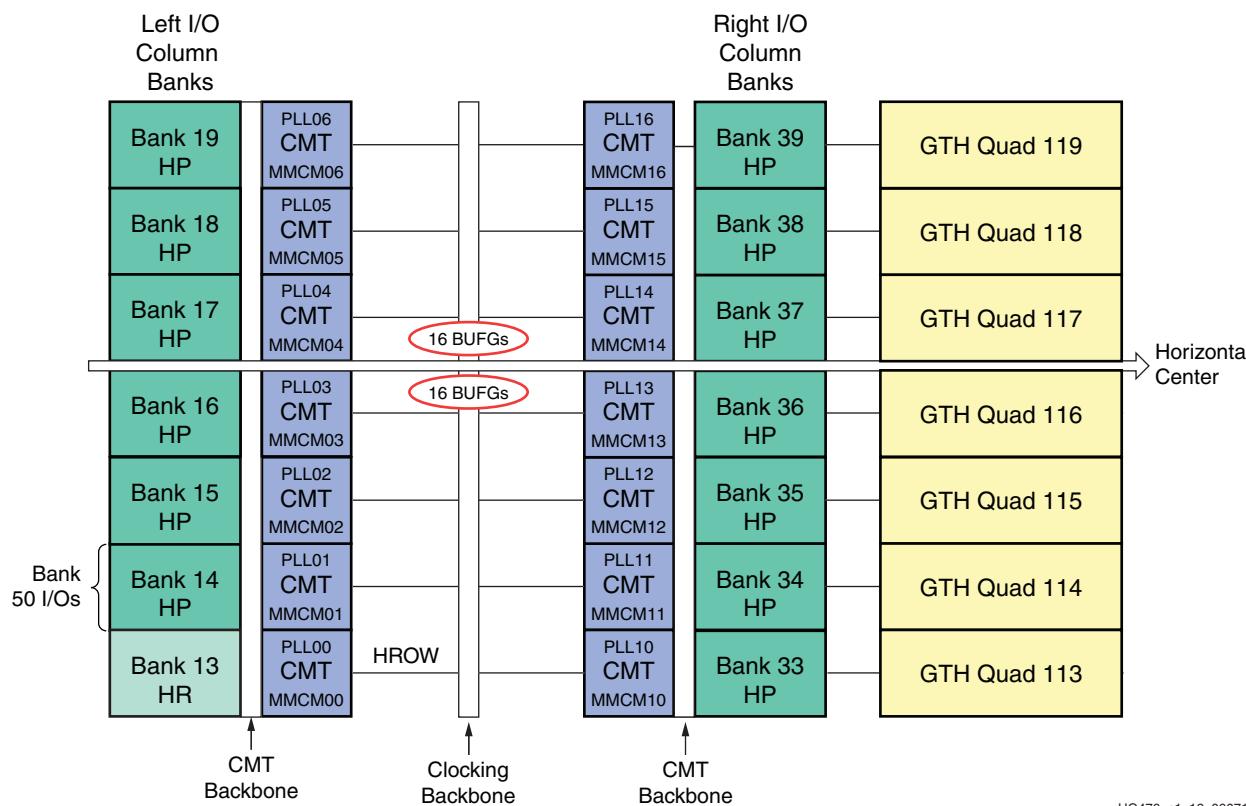


Figure 1-15: XC7VX330T and XQ7VX330T Banks

XC7VX415T Banks

Figure 1-16 shows the I/O and transceiver banks for the XC7VX415T.

FFG1157 and FFV1157 Packages

- All HP I/O banks are fully bonded out.
- GTH Quads 119, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1158 and FFV1158 Packages

- HP I/O banks 18, 19, 37, 38, and 39 are not bonded out.
- GTH Quads are fully bonded out in this package.

FFG1927 and FFV1927 Packages

All HP I/O banks and the GTH Quads are fully bonded out in this package.

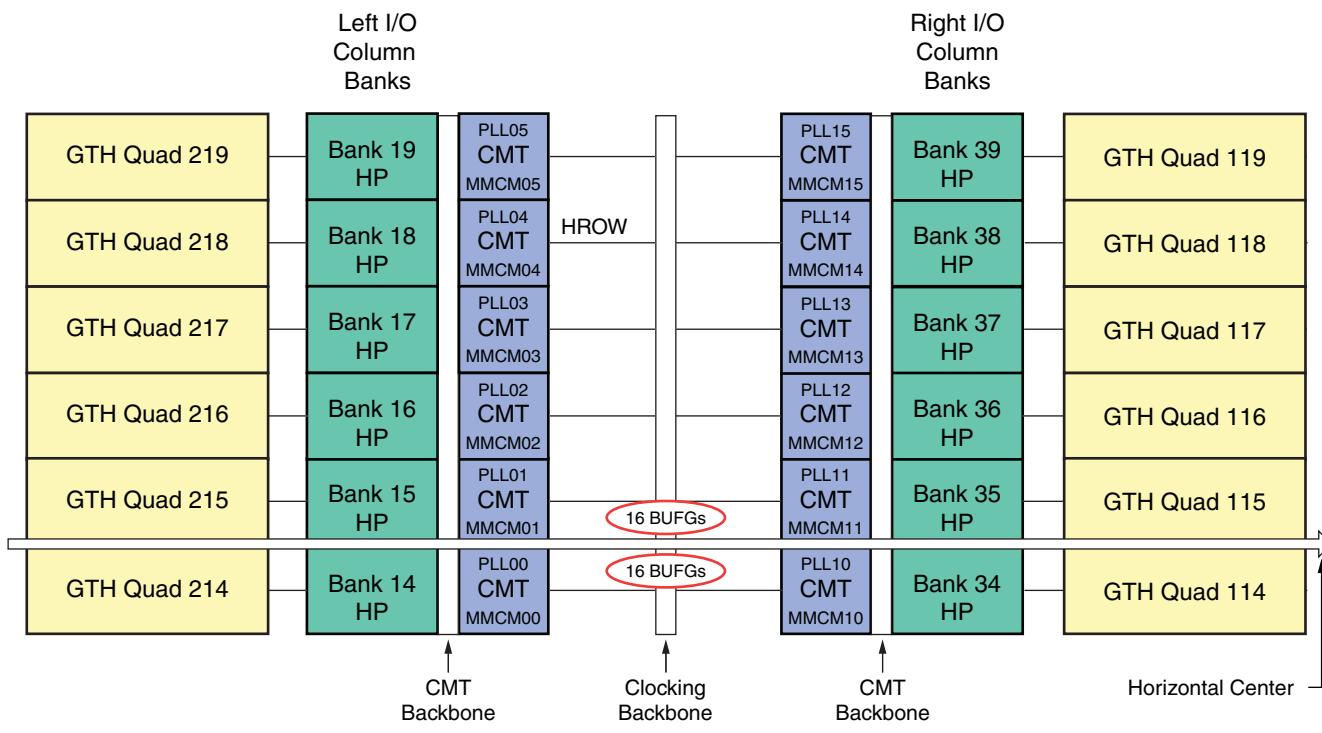


Figure 1-16: XC7VX415T Banks

XC7VX485T and XQ7VX485T Banks

Figure 1-17 shows the I/O and transceiver banks for the XC7VX485T and XQ7VX485T.

FFG1157 Package

- HP I/O banks 13 and 33 are not bonded out.
- GTX Quads 113, 119, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1158 and RF1158 Packages

- HP I/O banks 13, 18, 19, 33, 37, 38, and 39 are not bonded out.
- GTX Quads 113 and 213 are not bonded out.

FFG1761 and RF1761 Packages

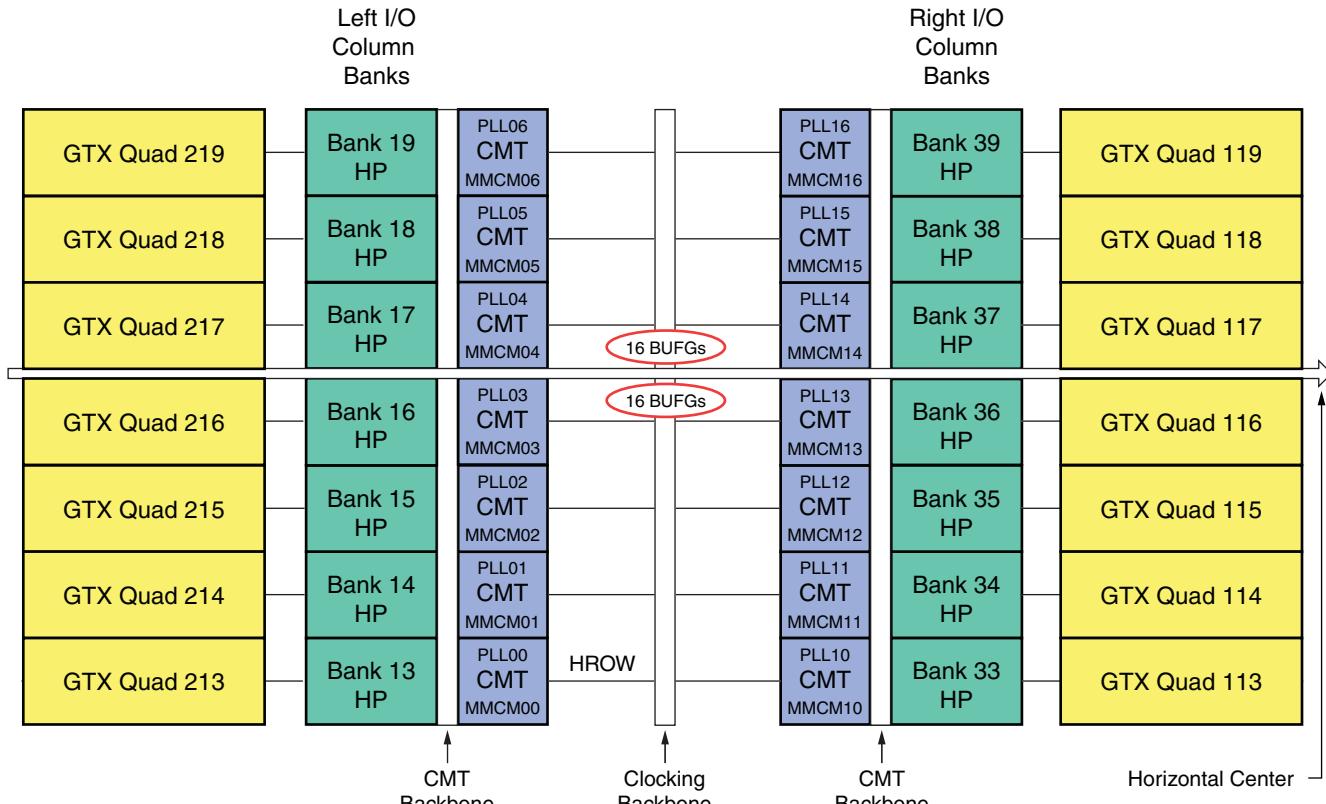
- All HP I/O banks are fully bonded out in these packages.
- GTX Quads 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1927 Package

- HP I/O banks 13 and 33 are not bonded out.
- All the GTX Quads are fully bonded out in this package.

FFG1930 and RF1930 Packages

- All HP I/O banks are fully bonded out in these packages.
- GTX Quads 119, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.



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Figure 1-17: XC7VX485T and XQ7VX485T Banks

XC7VX550T Banks

Figure 1-18 shows the I/O and transceiver banks for the XC7VX550T.

FFG1158 Package

- HP I/O banks 10, 11, 12, 13, 18, 19, 30, 31, 32, 33, 37, 38, and 39 are not bonded out.
- GTH Quads 110, 111, 112, 113, 210, 211, 212, and 213 are not bonded out.

FFG1927 Package

- HP I/O banks 10, 11, 12, 13, 30, 31, 32, and 33 are not bonded out.
- All GTH Quads are fully bonded out in this package.



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Figure 1-18: XC7VX550T Banks

XC7VX690T and XQ7VX690T Banks

Figure 1-19 shows the I/O and transceiver banks for the XC7VX690T and XQ7VX690T.

FFG1157 and RF1157 Packages

- HP I/O banks 10, 11, 12, 13, 30, 31, 32, and 33 are not bonded out.
- GTH Quads 110, 111, 112, 113, 119, 210, 211, 212, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1158 and RF1158 Packages

- HP I/O banks 10, 11, 12, 13, 18, 19, 30, 31, 32, 33, 37, 38, and 39 are not bonded out.
- GTH Quads 110, 111, 112, 113, 210, 211, 212, and 213 are not bonded out.

FFG1761 and RF1761 Packages

- HP I/O banks 10, 11, and 30 are not bonded out.
- GTH Quads 110, 210, 211, 212, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1926 Package

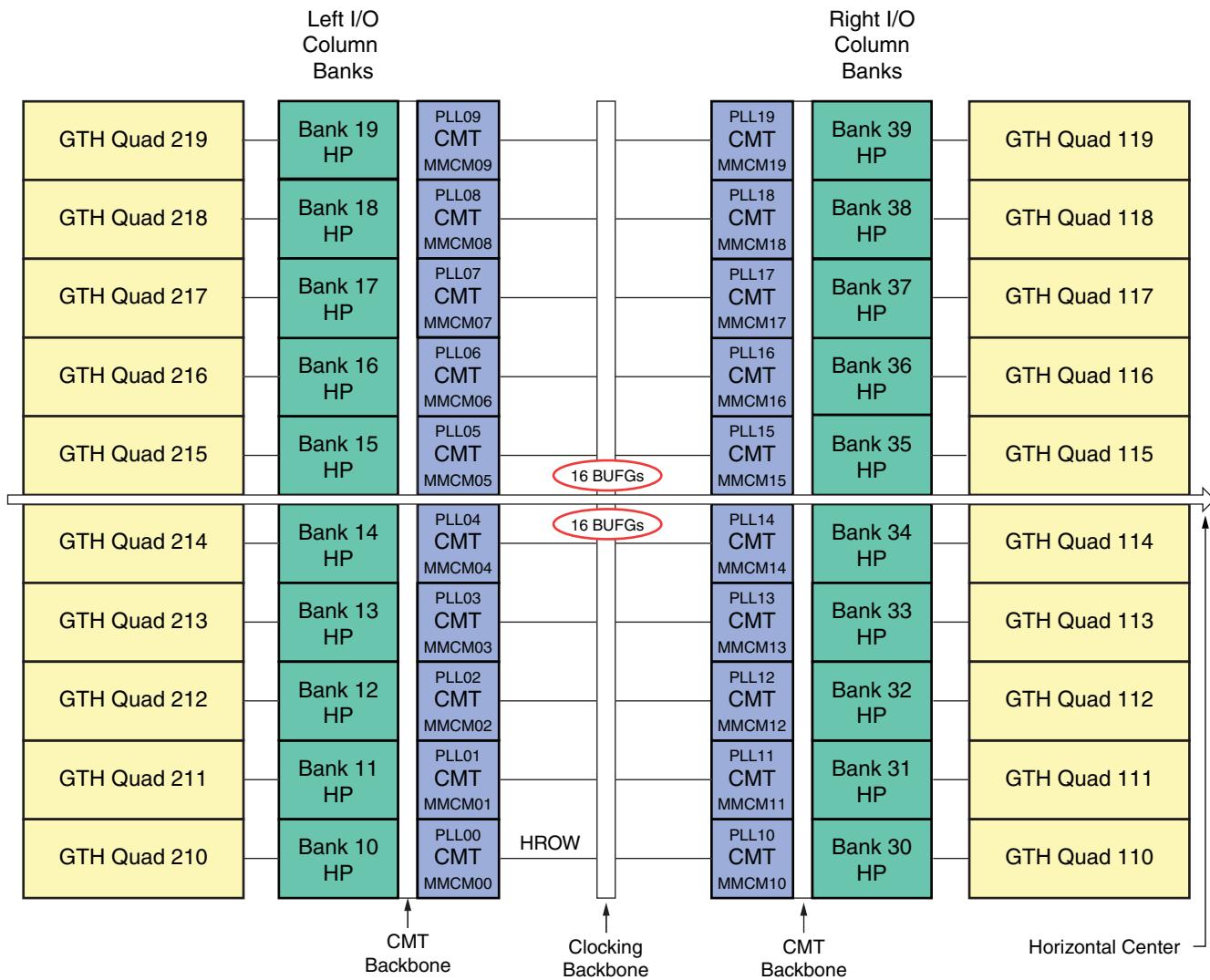
- HP I/O bank 17 is partially bonded out.
- HP I/O banks 18, 19, 37, 38, and 39 are not bonded out.
- GTH Quads 110, 119, 210, and 219 are not bonded out.

FFG1927 Package

- HP I/O banks 10, 11, 12, 13, 30, 31, 32, and 33 are not bonded out.
- All GTH Quads are fully bonded out in this package.

FFG1930 and RF1930 Packages

- All HP I/O banks are fully bonded out in these packages.
- GTH Quads 110, 111, 112, 119, 210, 211, 212, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.



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Figure 1-19: XC7VX690T and XQ7VX690T Banks

XC7VX980T and XQ7VX980T Banks

Figure 1-20 shows the I/O and transceiver banks for the XC7VX980T and XQ7VX980T.

FFG1926 Package

- HP I/O bank 17 is partially bonded out.
- HP I/O banks 18, 37, and 38 are not bonded out.
- GTH Quads 110 and 210 are not bonded out.

FFG1928 Package

- HP I/O bank 16 is partially bonded out.
- HP I/O banks 10, 11, 12, 17, 18, 30, 31, and 32 are not bonded out.
- All GTH Quads are fully bonded out in this package.

FFG1930 and RF1930 Packages

- All HP I/O banks are fully bonded out in these packages.
- GTH Quads 110, 111, 112, 210, 211, 212, 213, 214, 215, 216, 217, and 218 are not bonded out.

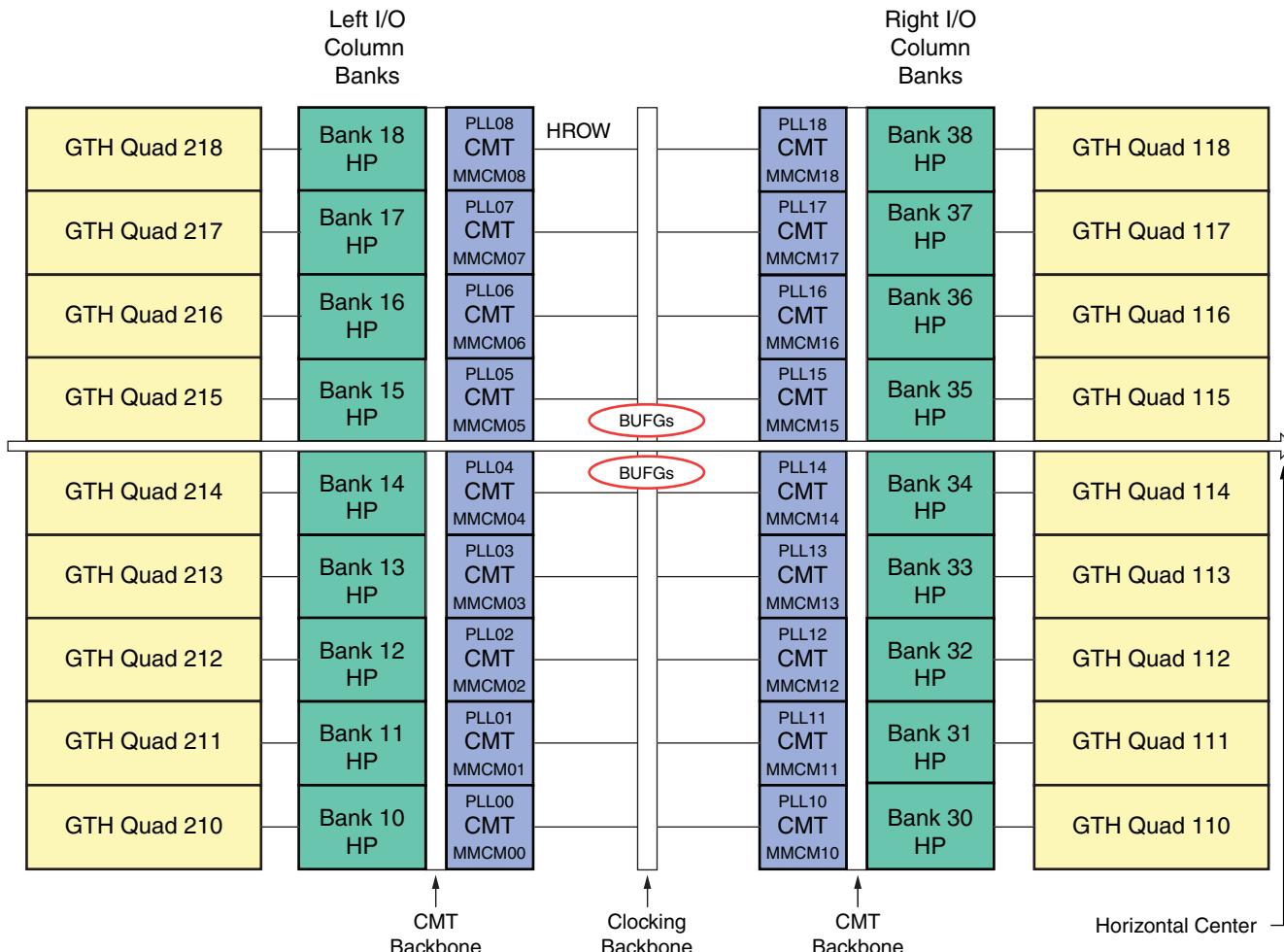


Figure 1-20: XC7VX980T and XQ7VX980T Banks

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XC7VX1140T Banks

Figure 1-21 shows the I/O and transceiver banks for the XC7VX1140T.

FLG1926 Package

- HP I/O bank 17 is partially bonded out.
- HP I/O banks 18, 19, 20, 21, 37, 38, 39, 40, and 41 are not bonded out.
- GTH Quads 110, 119, 120, 121, 210, 219, 220, and 221 are not bonded out.

FLG1928 Package

- HP I/O bank 16 is partially bonded out.
- HP I/O banks 10, 11, 12, 17, 18, 19, 20, 21, 30, 31, 32, 39, 40, and 41 are not bonded out.
- All GTH Quads are fully bonded out in this package.

FLG1930 Package

- HP I/O banks 40 and 41 are not bonded out.
- GTH Quads 110, 111, 112, 119, 120, 121, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, and 221 are not bonded out.

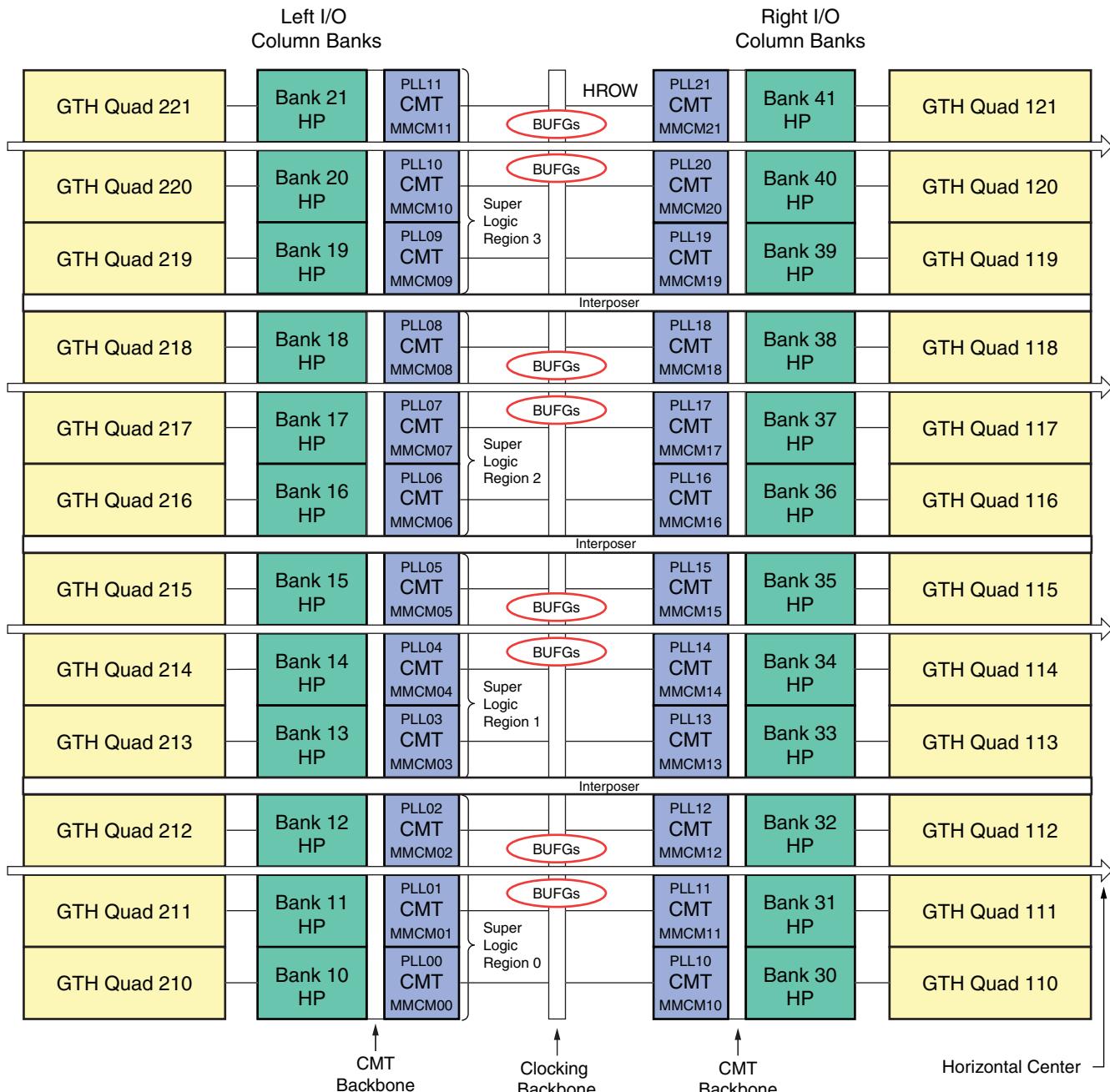


Figure 1-21: XC7VX1140T Banks

7 Series FPGAs Package Files

About ASCII Package Files

The ASCII files for each package include a comma-separated-values (CSV) version and a text version optimized for a browser or text editor. Each of the files consists of the following:

- Device/Package name (*FPGA Family—Device—Package*), date and time of creation
- Eight columns containing data for each pin:
 - Pin—Pin location on the package.
 - Pin Name—The name of the assigned pin.
 - Memory Byte Group—Memory byte group between 0 and 3. For more information on the memory byte group, see [UG586, 7 Series FPGAs Memory Interface Solutions User Guide](#).
 - Bank—Bank number.
 - V_{CCAUX} Group—Number corresponding to the V_{CCAUX_IO} power supply for the given pin. V_{CCAUX} is shown for packages with only one V_{CCAUX} group.
 - Super Logic Region—Number corresponding to the super logic region (SLR) in the devices implemented with stacked silicon interconnect (SSI) technology.
 - I/O Type—CONFIG, HR, HP, or GT (GTP, GTX, GTH) depending on the I/O type. For more information on the I/O type, see [UG471, 7 Series FPGAs SelectIO Resources User Guide](#).
 - No-Connect—This list of devices is used for migration between devices that have the same package size and are not connected at that specific pin.
- Total number of pins in the package.
- The package file links for the ruggedized packages have the same pinouts as the equivalent BGA packages.
 - RS pinouts use the SBG/SBV files (Artix®-7 devices)
 - RB pinouts use the FBG/FBV files (Artix-7 devices)
 - RF pinouts use the FFG/FFV files (Kintex®-7 and Virtex®-7 devices)

ASCII Pinout Files

This chapter includes the pinout information tables for the following device/packages. For brevity, all the package selections are not listed in the link ZIP file names. For more information on available device and package choices, consult the device/package ordering information tables in [DS180, 7 Series FPGAs Overview](#) or the [7 Series Product Selection Guide](#). The XA devices are further outlined in [DS197, XA Artix®-7 FPGAs Overview](#). The XQ devices are outlined in [DS185, Defense-Grade 7 Series FPGAs Overview](#).

Note: All package files are ASCII files in TXT and CSV file format.

To download all available Artix-7 FPGAs package/device/pinout files click here:

www.xilinx.com/support/package-pinout-files/artix-7-pkgs.html

Table 2-1: Artix-7 FPGAs Package/Device Pinout Files

Device	CPG 236	CS CSG 324	CS CSG 325	FTG 256	SBG SBV 484	FG FGG 484	FGG 676	FBG FBV 484	FBG FBV 676	FFG FFV 1156	RB 484	RS 484	RB 676
XC7A15T	CPG236	CSG324	CSG325	FTG256		FGG484							
XC7A35T	CPG236	CSG324	CSG325	FTG256		FGG484							
XC7A50T	CPG236	CSG324	CSG325	FTG256		FGG484							
XC7A75T		CSG324		FTG256		FGG484	FGG676						
XC7A100T		CSG324		FTG256		FGG484	FGG676						
XC7A200T					SBG484			FBG484	FBG676	FFG1156			
XA7A15T	CPG236	CSG324	CSG325										
XA7A35T	CPG236	CSG324	CSG325										
XA7A50T	CPG236	CSG324	CSG325										
XA7A75T		CSG324				FGG484							
XA7A100T		CSG324				FGG484							
XQ7A50T			CS325			FG484							
XQ7A100T		CS324				FG484							
XQ7A200T											RB484	RS484	RB676

To download all available Kintex®-7 FPGAs package/device/pinout files click here:

www.xilinx.com/support/package-pinout-files/kintex-7-pkgs.html

Note: Only the available files listed in [Table 2-2](#) are linked and consolidated in the above ZIP file.

Table 2-2: Kintex-7 FPGAs Package/Device Pinout Files

Device	FB484 FBG484	FB676 FBG676	FB900 FBG900	FF676 FFG676	FF900 FFG900	FF901 FFG901	FF1156 FFG1156	RF676	RF900
XC7K70T	FBG484	FBG676							
XC7K160T	FBG484	FBG676		FFG676					
XC7K325T		FBG676	FBG900	FFG676	FFG900				
XC7K355T						FF901 / FFG901			
XC7K410T		FBG676	FBG900	FFG676	FFG900				
XC7K420T						FFG901	FFG1156		
XC7K480T						FFG901	FFG1156		
XQ7K325T								RF676	RF900
XQ7K410T								RF676	RF900

To download all available Virtex®-7 FPGAs package/device/pinout files click here:

www.xilinx.com/support/package-pinout-files/virtex-7-pkgs.html

Note: Only the available files listed in Table 2-3 and Table 2-4 are linked and consolidated in the above ZIP file.

Table 2-3: Virtex-7 T FPGAs Package/Device Pinout Files

Device	FF1157/FFG1157	FF1761/FFG1761	FL1925/FLG1925	FH1761/FHG1761	RF1157	RF1761
XC7V585T	FFG1157	FFG1761				
XC7V2000T			FLG1925	FHHG1761		
XQ7V585T					RF1157	RF1761

Table 2-4: Virtex-7 XT FPGAs Package/Device Pinout Files

Device	FF1157 FFG1157 FFV1157 RF1157	FF1158 FFG1158 FFV1158 RF1158	FF1761 FFG1761 FFV1761 RF1761	FF1926 FFG1926	FF1927 FFG1927 FFV1927	FF1928 FFG1928	FF1930 FFG1930 RF1930	FL1926 FLG1926	FL1928 FLG1928	FL1930 FLG1930
XC7VX330T	FFG1157		FFG1761							
XC7VX415T	FFG1157	FFG1158			FFG1927					
XC7VX485T	FFG1157	FFG1158	FFG1761		FFG1927		FFG1930			
XC7VX550T		FFG1158			FFG1927					
XC7VX690T	FFG1157	FFG1158	FFG1761	FFG1926	FFG1927		FFG1930			
XC7VX980T				FFG1926		FFG1928	FFG1930			
XC7VX1140T								FLG1926	FLG1928	FLG1930
XQ7VX330T	RF1157		RF1761							
XQ7VX485T			RF1761				RF1930			
XQ7VX690T	RF1157	RF1158	RF1761				RF1930			
XQ7VX980T							RF1930			

Device Diagrams

Summary

This chapter provides pinout, high-performance and high-range I/O bank, memory groupings, and power and ground placement diagrams for each 7 series FPGA package/device combination.

- [Artix-7 FPGAs Device Diagrams, page 62](#)
- [Kintex-7 FPGAs Device Diagrams, page 93](#)
- [Virtex-7 FPGAs Device Diagrams, page 126](#)

The figures provide a top-view perspective.

The symbols for the multi-function I/O pins are represented by only one of the available pin functions; with precedence (by functionality) in this order:

- ADV_B, FCS_B, FOE_B, MOSI, FWE_B, DOUT_CS0_B, CSI_B, PUDC_B, or RDWR_B
- RS0–RS1
- AD0P, AD0N–AD15P, AD15N
- EMCCLK
- VRN, VRP, or VREF
- D00–D31
- A00–A28
- DQS, MRCC, or SRCC

For example, a pin description such as IO_L8P_SRCC_12 is represented with a SRCC symbol, a pin description such as IO_L19N_T3_A09_D25_VREF_14 is represented with a VREF symbol, and a pin description such as IO_L21N_T3_DQS_A06_D22_14 is represented with a D0–D31 symbol.

Note: For brevity, the prefixes for Xilinx commercial (XC) devices are used when the defense-grade (XQ) or the automotive (XA) could also be available. See the [7 Series Data Sheets](#) for ordering options.

Artix-7 FPGAs Device Diagrams

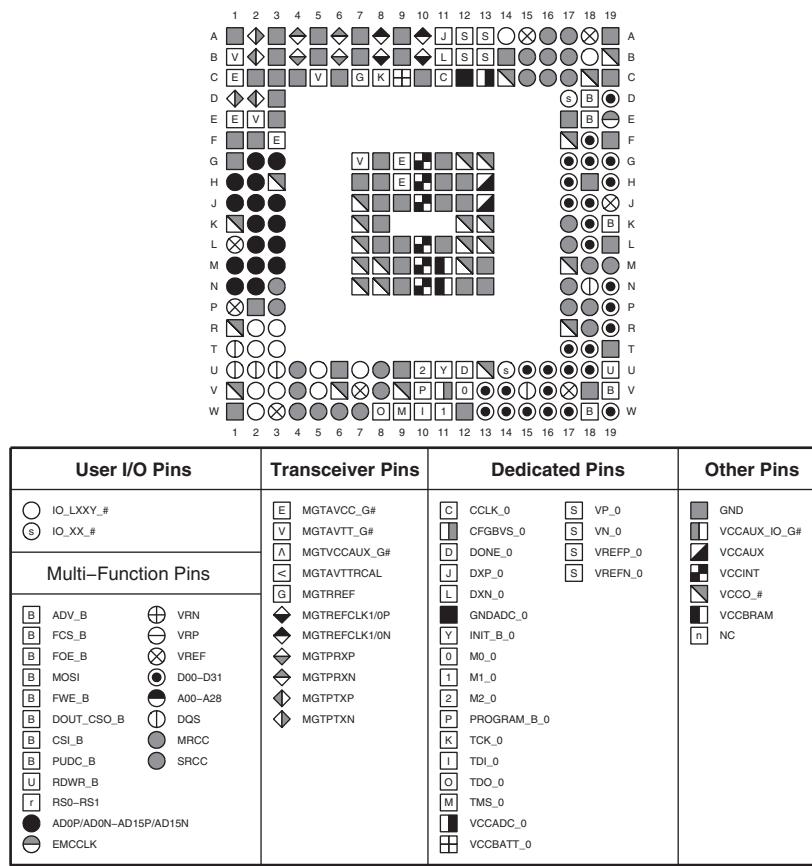
Table 3-1: Artix®-7 FPGAs Device Diagrams Cross-Reference⁽¹⁾

Device	CP236 CPG236	CS324 CSG324	CS325 CSG325	FT256 FTG256	SB484 SBG484 SBV484 RS484	FG484 FGG484	FG676 FGG676	FB484 FBG484 FBV484 RB484	FB676 FBG676 FBV676 RB676	FF1156 FFG1156 FFV1156
XC7A15T	page 62	page 65	page 67	page 69		page 71				
XC7A35T	page 62	page 65	page 67	page 69		page 71				
XC7A50T	page 62	page 65	page 67	page 69		page 71				
XC7A75T		page 65		page 69		page 74	page 77			
XC7A100T		page 65		page 69		page 74	page 77			
XC7A200T					page 80			page 83	page 86	page 89

Notes:

1. FGG676, FBG676, FBV676, and FGG484, FBG484, FBV484 packages are pin compatible.

CP236 and CPG236 Packages—XC7A15T, XC7A35T, and XC7A50T



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Figure 3-1: CP236 and CPG236 Packages—XC7A15T, XC7A35T, and XC7A50T Pinout Diagram

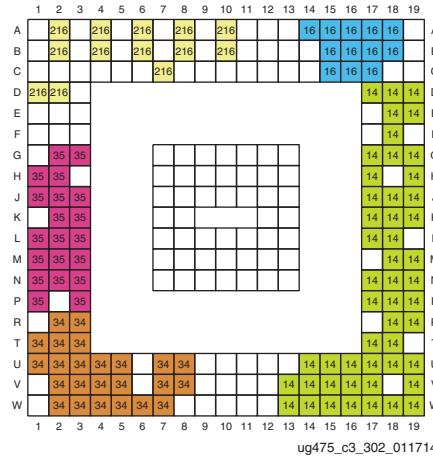


Figure 3-2: CP236 and CPG236 Packages—XC7A15T, XC7A35T, and XC7A50T I/O Banks

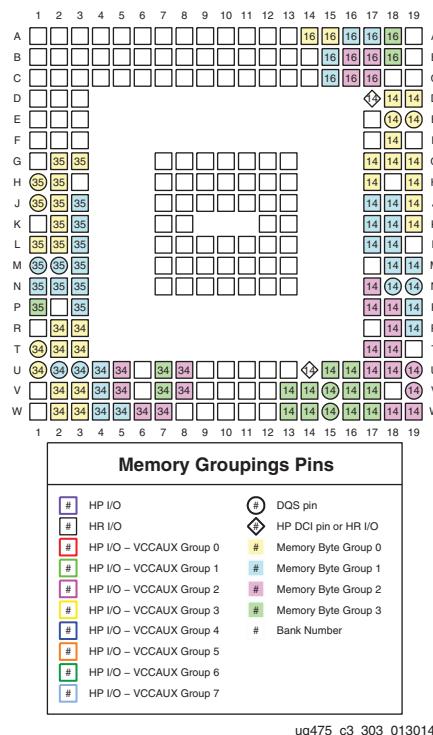
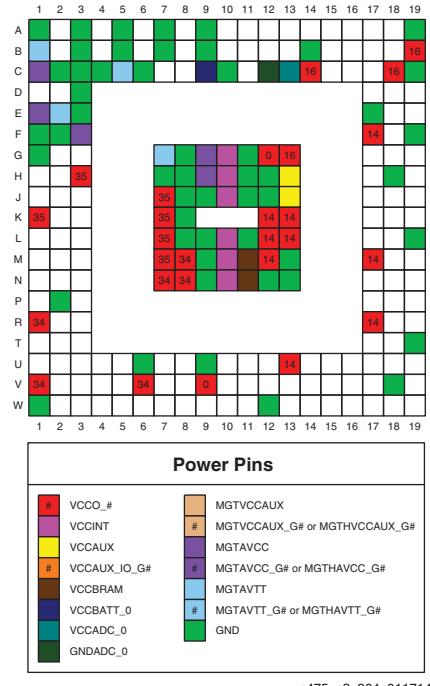


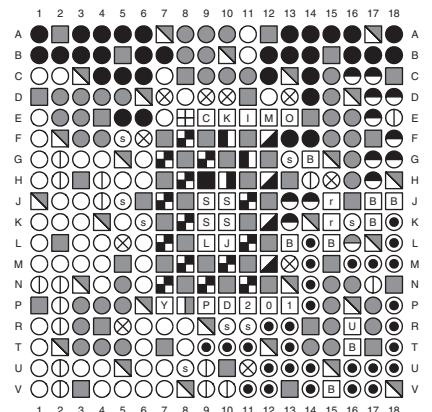
Figure 3-3: CP236 and CPG236 Packages—XC7A15T, XC7A35T, and XC7A50T Memory Groupings



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Figure 3-4: CP236 and CPG236 Packages—XC7A15T, XC7A35T, and XC7A50T Power and GND Placement

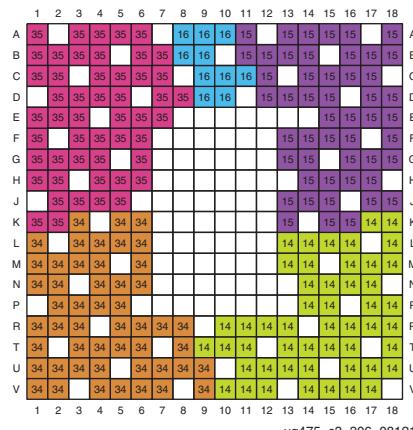
CS324 and CSG324 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T



User I/O Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	C CCLK_0	GND
○ IO_XX_#	S VP_0	VCCAUX
	S CFGBVS_0	VCCINT
	D DONE_0	VCCO_#
	J DXP_0	VCCBRAM
	L DXN_0	NC
B ADV_B	Y GNDADC_0	
B FCS_B	INIT_B_0	
B FOE_B	0 M0_0	
B MOSI	1 M1_0	
B FWE_B	2 M2_0	
B DOUT_CSO_B	P PROGRAM_B_0	
B CSL_B	K TCK_0	
B PUDC_B	I TDI_0	
U RDWR_B	O TDO_0	
r RS0-RS1	M TMS_0	
● AD0P/AD0N-AD15P/AD15N	Q VCCADC_0	
● EMCCLK	■ VCCBATT_0	

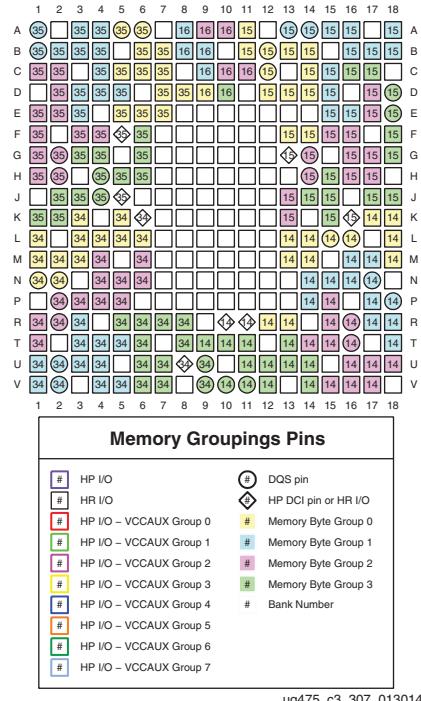
ug475_c3_305_090711

Figure 3-5: CS324 and CSG324 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T Pinout Diagram



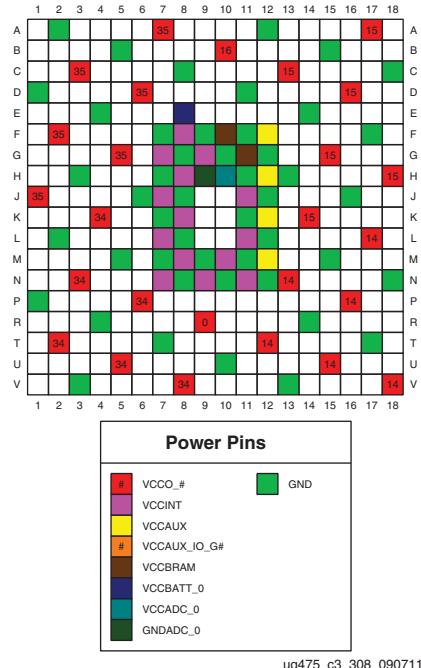
ug475_c3_306_081211

Figure 3-6: CS324 and CSG324 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T I/O Banks



ug475_c3_307_013014

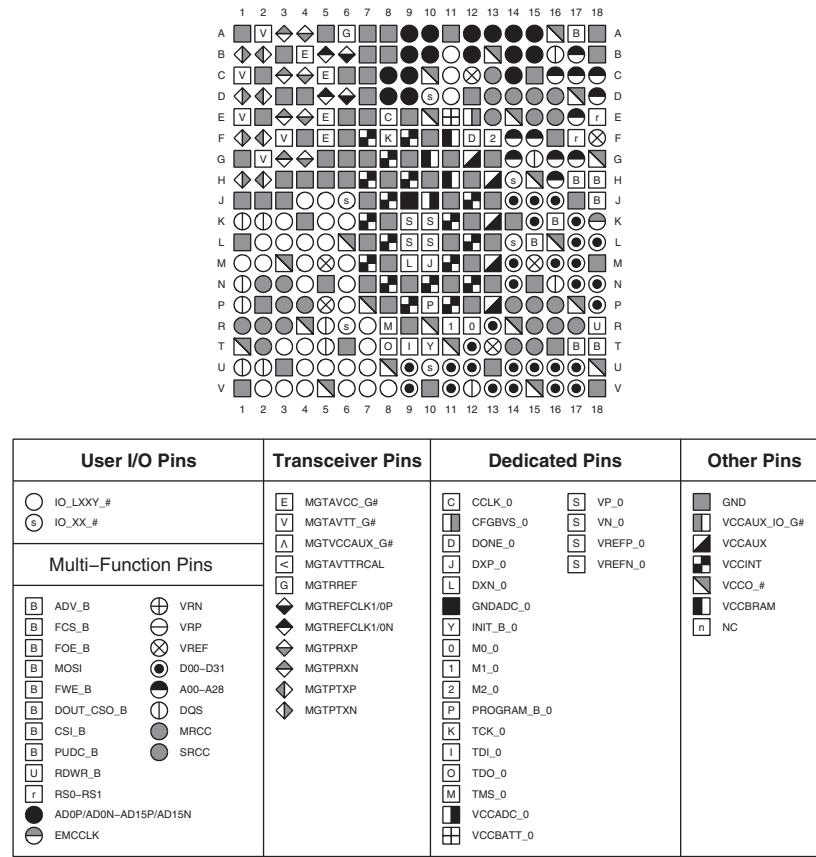
Figure 3-7: CS324 and CSG324 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T Memory Groupings



ug475_c3_308_090711

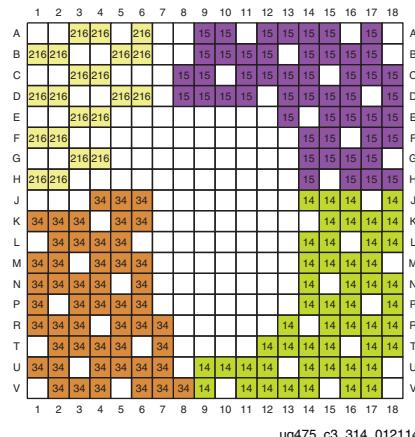
Figure 3-8: CS324 and CSG324 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T Power and GND Placement

CS325 and CSG325 Packages—XC7A15T, XC7A35T, and XC7A50T



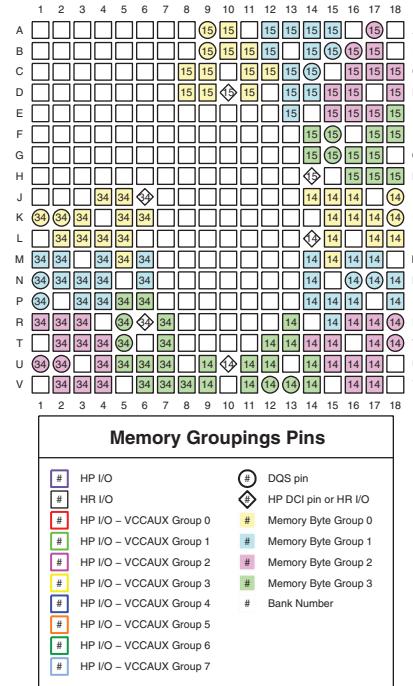
ug475_c3_313_012114

Figure 3-9: CS325 and CSG325 Packages—XC7A15T, XC7A35T, and XC7A50T Pinout Diagram



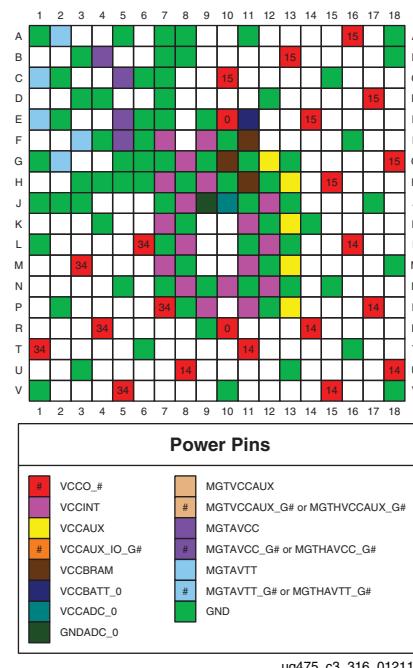
ug475_c3_314_012114

Figure 3-10: CS325 and CSG325 Packages—XC7A15T, XC7A35T, and XC7A50T I/O Banks



ug475_c3_315_013014

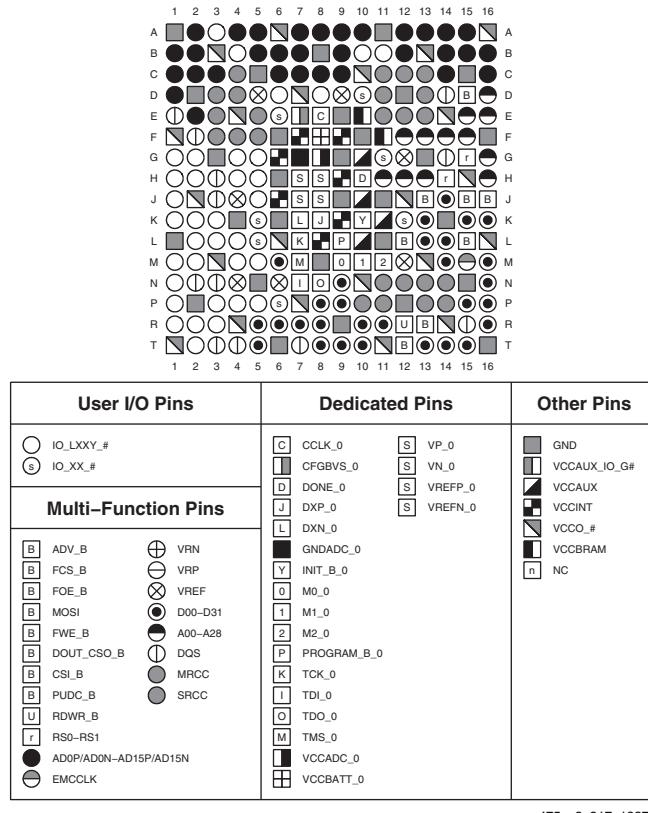
Figure 3-11: CS325 and CSG325 Packages—XC7A15T, XC7A35T, and XC7A50T Memory Groupings



ug475_c3_316_012114

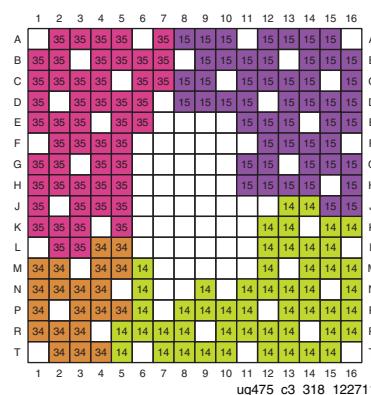
Figure 3-12: CS325 and CSG325 Packages—XC7A15T, XC7A35T, and XC7A50T Power and GND Placement

FT256 and FTG256 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T



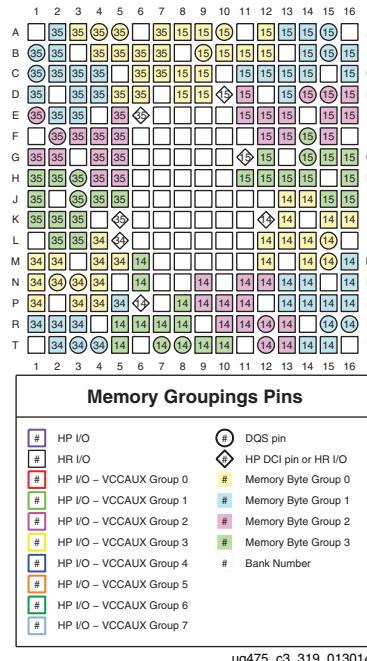
ug475_c3_317_122711

Figure 3-13: FT256 and FTG256 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T Pinout Diagram



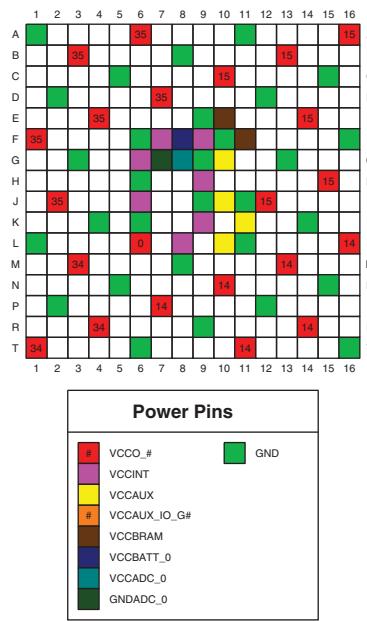
ug475_c3_318_122711

Figure 3-14: FT256 and FTG256 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T I/O Banks



ug475_c3_319_013014

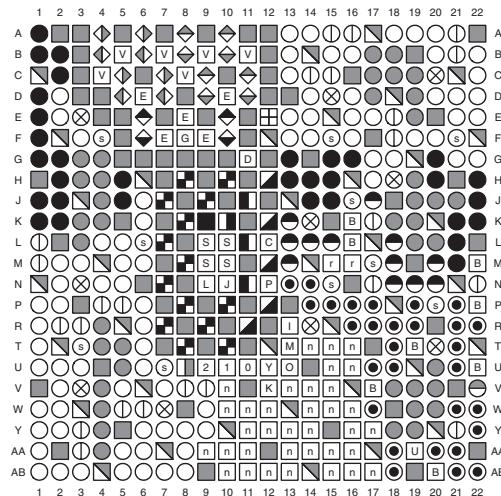
Figure 3-15: FT256 and FTG256 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T Memory Groupings



ug475_c3_320_122711

Figure 3-16: FT256 and FTG256 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T Power and GND Placement

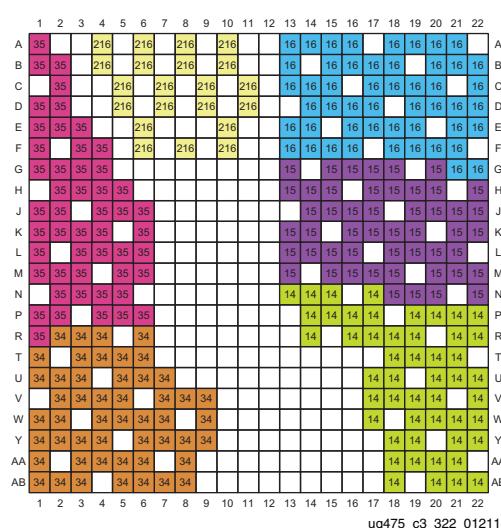
FG484 and FGG484 Packages—XC7A15T, XC7A35T, and XC7A50T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_# ○ S IO_XX_#	[E] MGTAVCC_G# [V] MGTAVTT_G# [A] MGTVCXAUX_G# [K] MGTAVTRCAL [G] MGTRREF ◆ MGTREFCLK1/0P ◆ MGTREFCLK1/0N ◆ MGTPRXN ◆ MGPTXP ◆ MGPTXN	[C] CCLK_0 [I] CFGBVS_0 [D] DONE_0 [J] DXP_0 [L] DXN_0 [Y] GNDADC_0 [O] INIT_B_0 [0] MO_0 [1] M1_0 [2] M2_0 [P] PROGRAM_B_0 [K] TCK_0 [I] TDI_0 [O] TDO_0 [M] TMS_0 [S] VP_0 [S] VN_0 [S] VREFP_0 [S] VREFN_0	[GND] [VCCAUX_IO_G#] [VCCAUX] [VCCINT] [VCCO_#] [VCCBRAM] [NC]
Multi-Function Pins			
[B] ADV_B [B] FCS_B [B] FOE_B [B] MOSI [B] FWE_B [B] DOUT_CSO_B [B] CSI_B [B] PUDC_B [U] RDWR_B [r] RS0-RS1 ● AD0P/AD0N-AD15P/AD15N ○ EMCCLK	⊕ VRN ○ VRP ⊗ VREF ○ D00-D31 ○ A00-A28 ○ DOS ○ MRCC ○ SRCC		

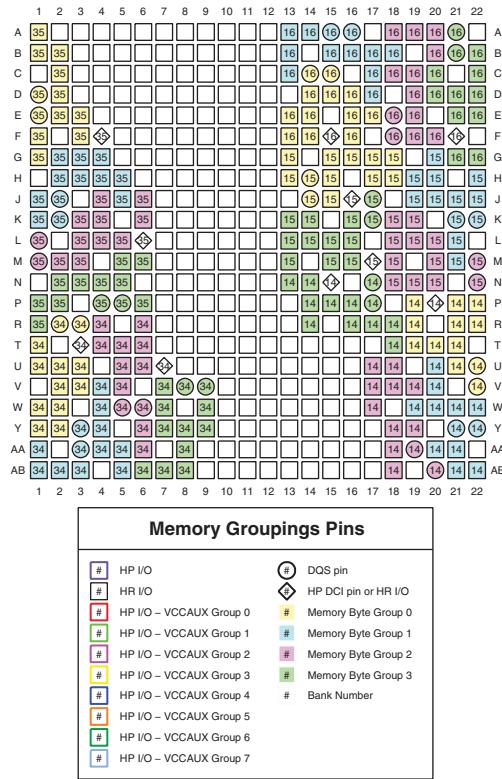
ug475_c3_321_012114

Figure 3-17: FG484 and FGG484 Packages—XC7A15T, XC7A35T, and XC7A50T Pinout Diagram



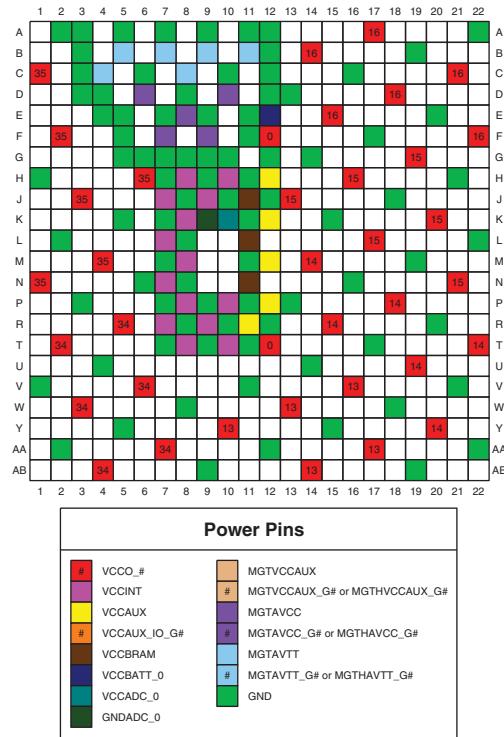
ug475_c3_322_012114

Figure 3-18: FG484 and FGG484 Packages—XC7A15T, XC7A35T, and XC7A50T I/O Banks



ug475_c3_323_013014

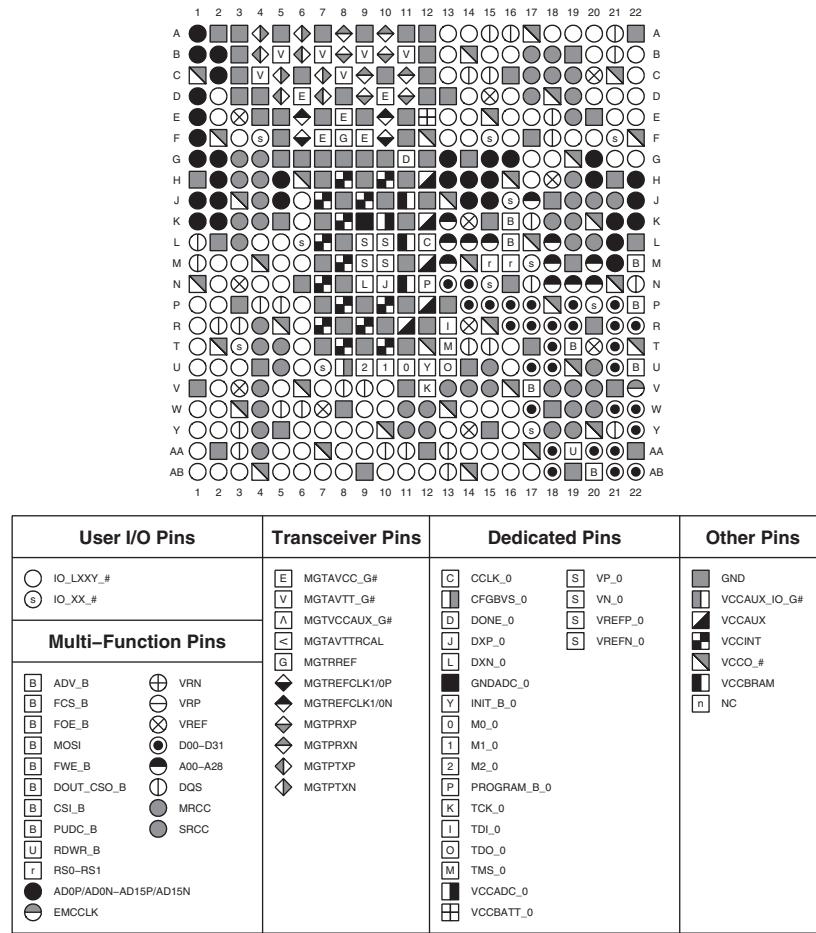
Figure 3-19: FG484 and FGG484 Packages—XC7A15T, XC7A35T, and XC7A50T Memory Groupings



ug475_c3_324_012114

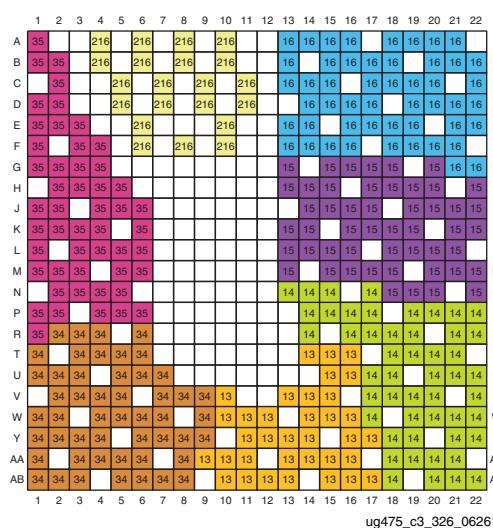
Figure 3-20: FG484 and FGG484 Packages—XC7A15T, XC7A35T, and XC7A50T Power and GND Placement

FG484 and FGG484 Packages—XC7A75T and XC7A100T



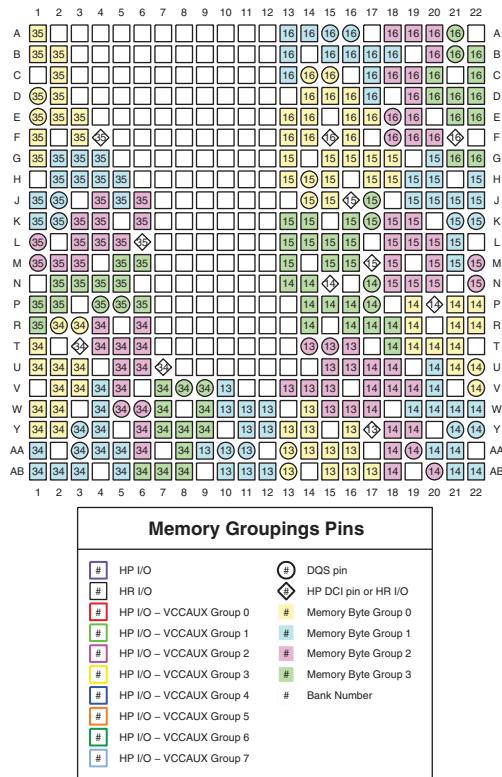
ug475_c3_325_122811

Figure 3-21: FG484 and FGG484 Packages—XC7A75T and XC7A100T Pinout Diagram



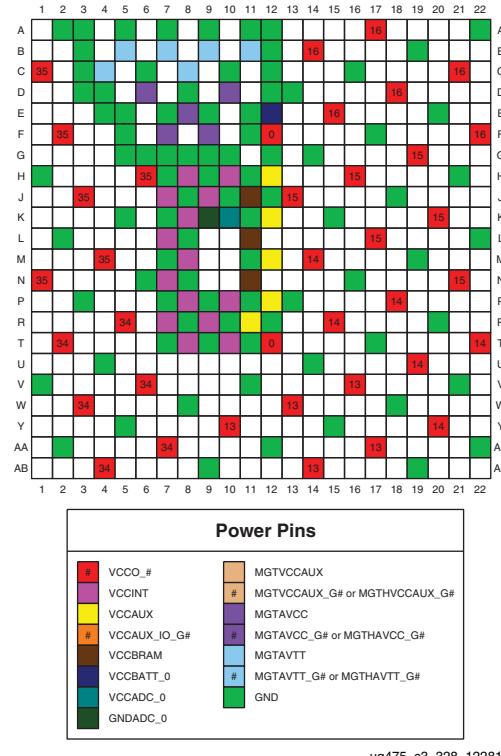
ug475_c3_326_062612

Figure 3-22: FG484 and FGG484 Packages—XC7A75T and XC7A100T I/O Banks



ug475_c3_327_013014

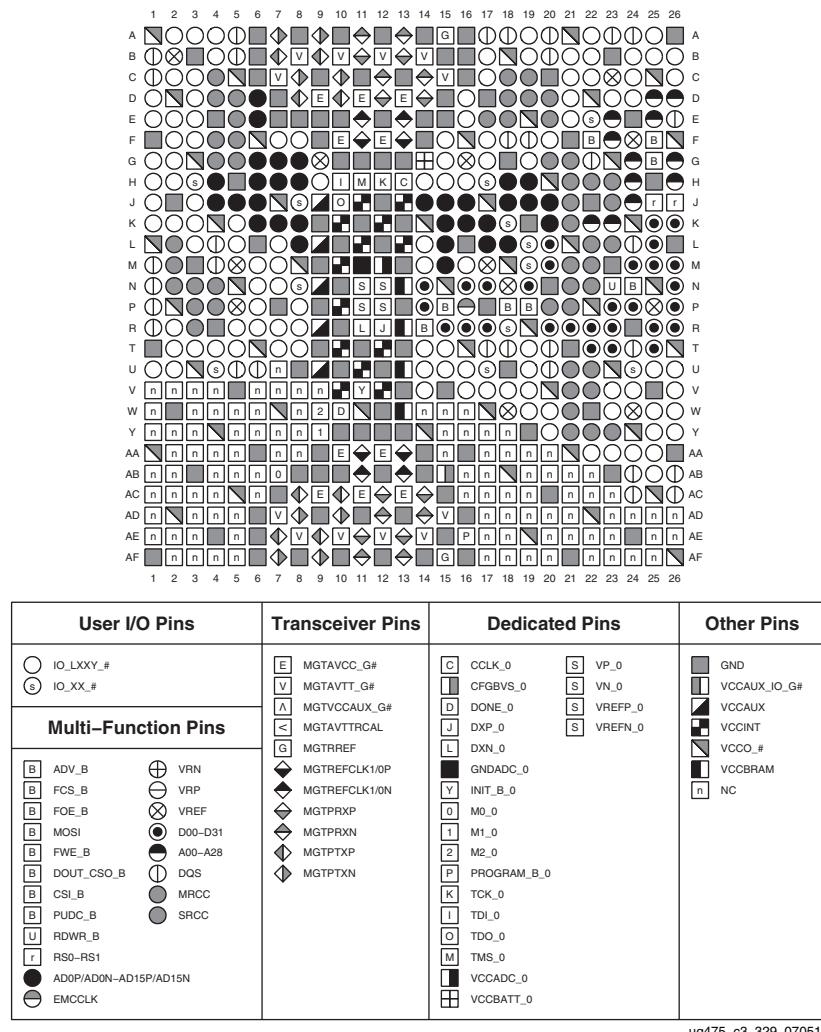
Figure 3-23: FG484 and FGG484 Packages—XC7A75T and XC7A100T Memory Groupings



ug475_c3_328_122811

Figure 3-24: FG484 and FGG484 Packages—XC7A75T and XC7A100T Power and GND Placement

FG676 and FGG676 Packages—XC7A75T and XC7A100T



ug475_c3_329_070512

Figure 3-25: FG676 and FGG676 Packages—XC7A75T and XC7A100T Pinout Diagram

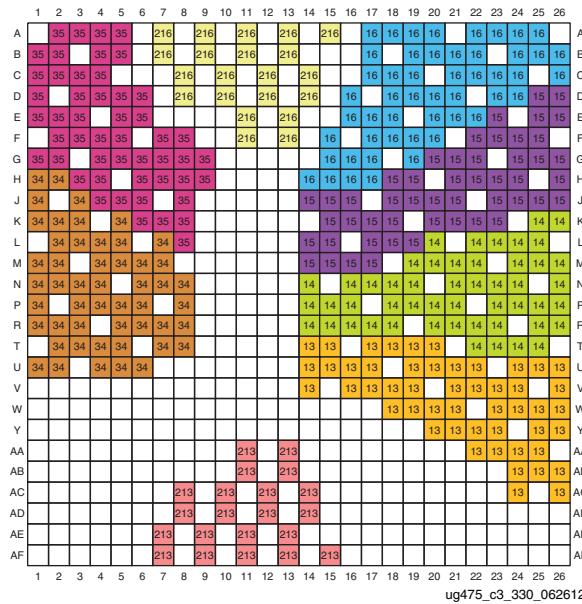


Figure 3-26: FG676 and FGG676 Packages—XC7A75T and XC7A100T I/O Banks

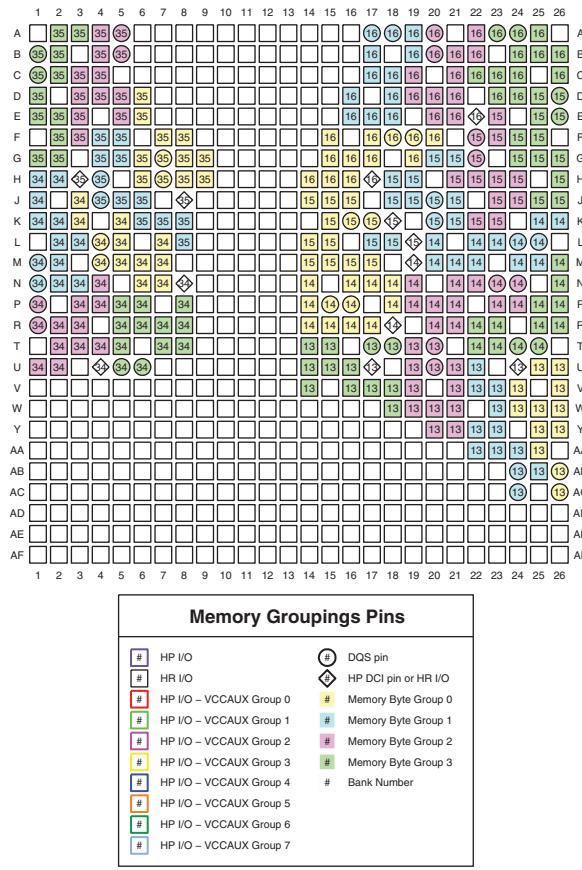


Figure 3-27: FG676 and FGG676 Packages—XC7A75T and XC7A100T Memory Groupings

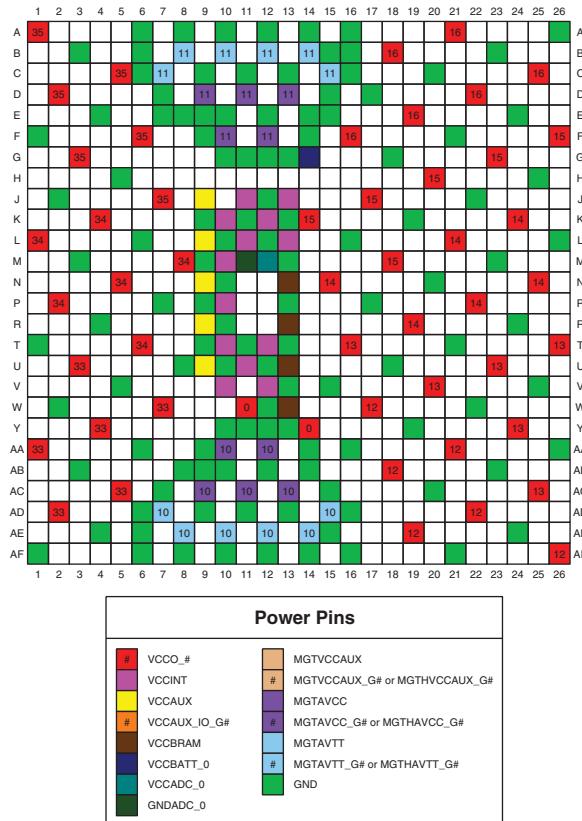


Figure 3-28: FG676 and FGG676 Packages—XC7A75T and XC7A100T Power and GND Placement

SB484, SBG484, SBV484, and RS484 Packages—XC7A200T

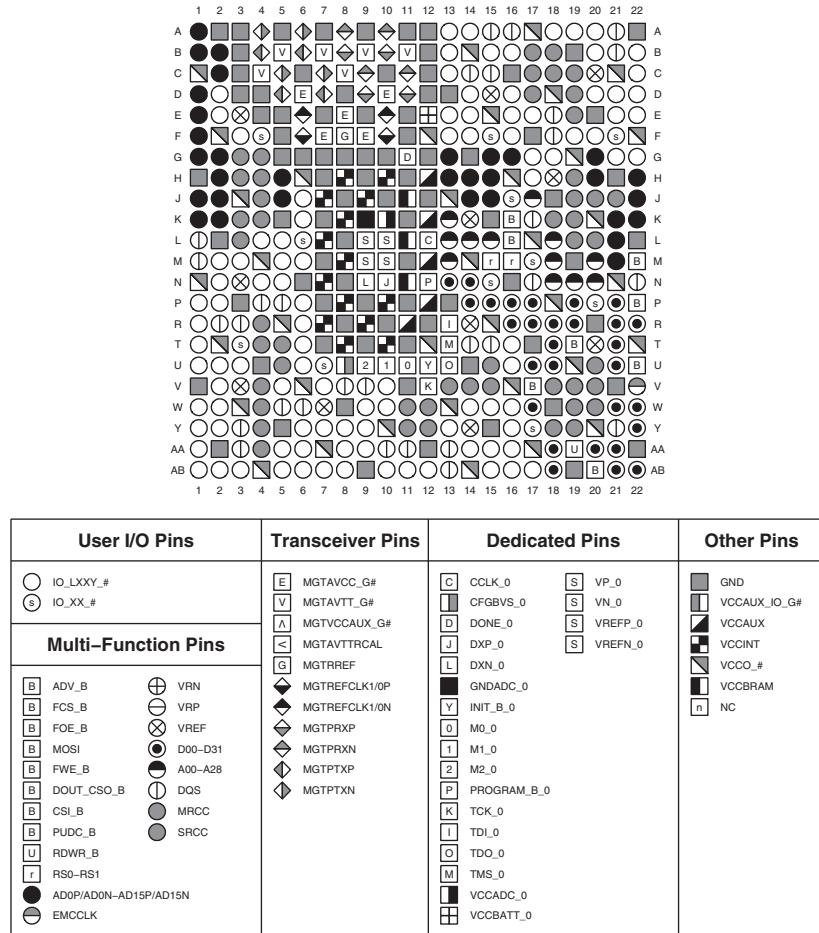


Figure 3-29: SB484, SBG484, SBV484, and RS484 Packages—XC7A200T Pinout Diagram

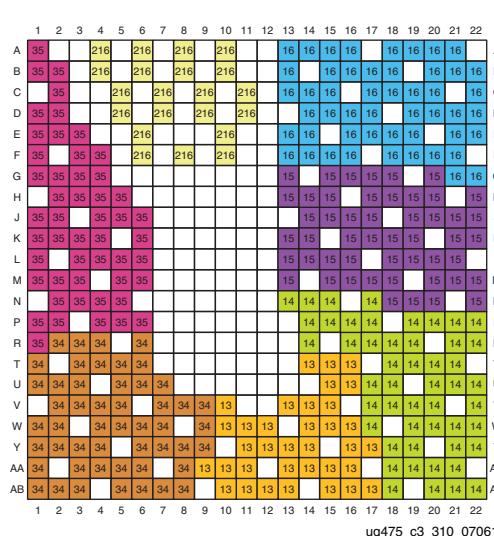
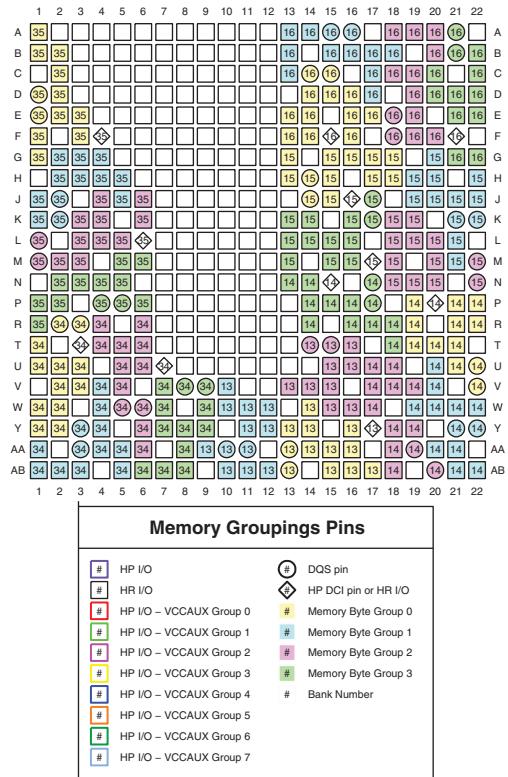
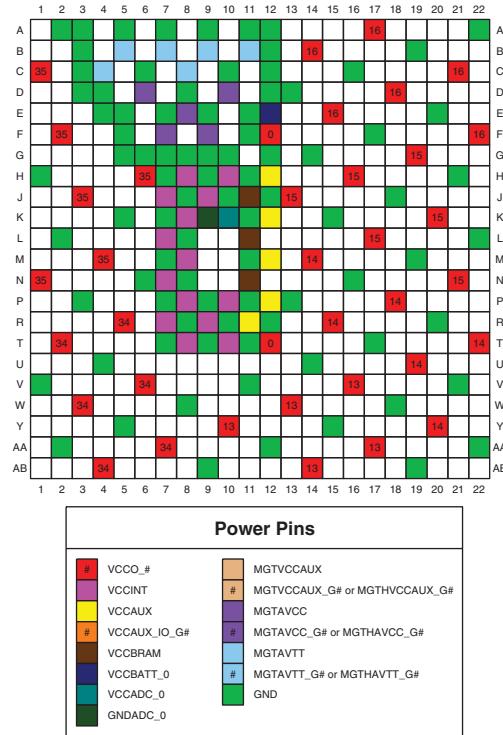


Figure 3-30: SB484, SBG484, SBV484, and RS484 Packages—XC7A200T I/O Banks



ug475_c3_311_013014

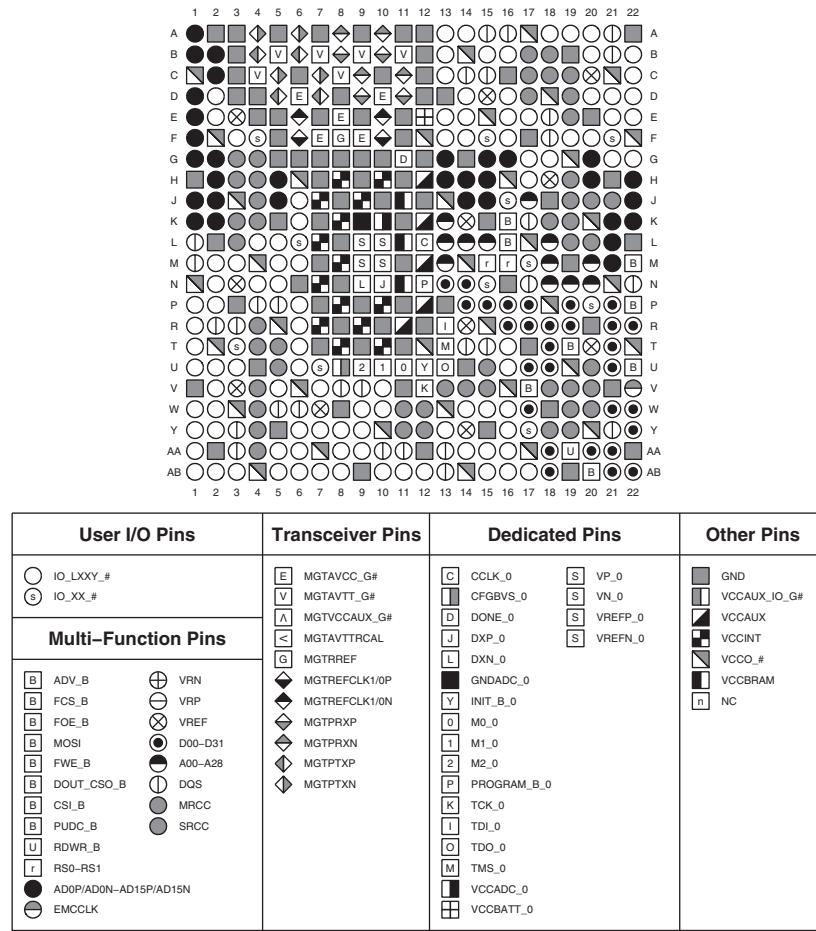
Figure 3-31: SB484, SBG484, SBV484, and RS484 Packages—XC7A200T Memory Groupings



ug475_c3_312_070612

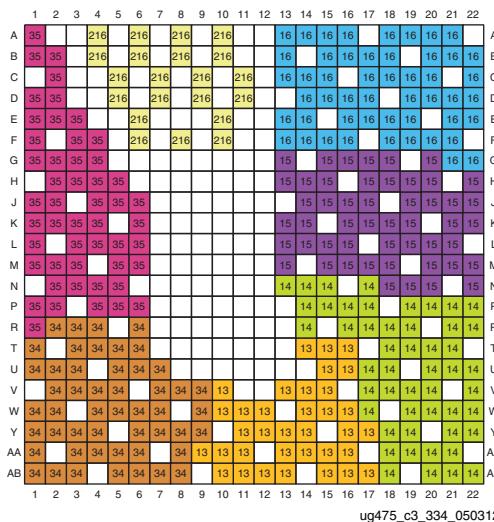
Figure 3-32: SB484, SBG484, SBV484, and RS484 Packages—XC7A200T Power and GND Placement

FB484, FBG484, FBV484, and RB484 Packages—XC7A200T



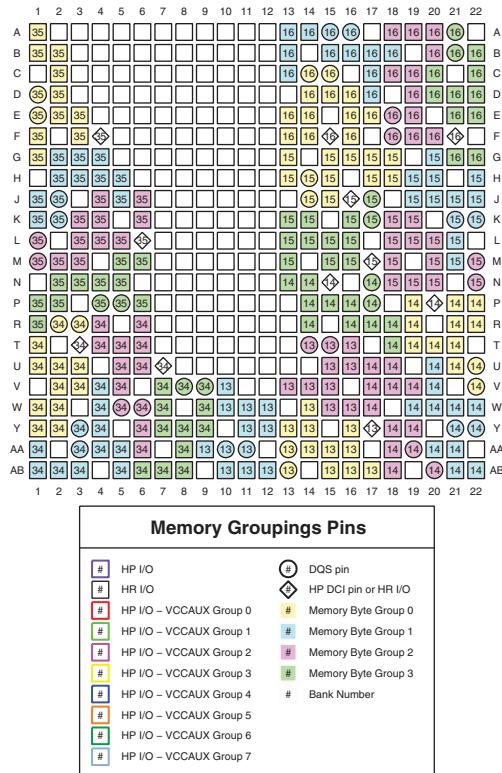
ug475_c3_333_122811

Figure 3-33: FB484, FBG484, FBV484, and RB484 Packages—XC7A200T Pinout Diagram



ug475_c3_334_050312

Figure 3-34: FB484, FBG484, FBV484, and RB484 Packages—XC7A200T I/O Banks



ug475_c3_335_013014

Figure 3-35: FB484, FBG484, FBV484, and RB484 Packages—XC7A200T Memory Groupings

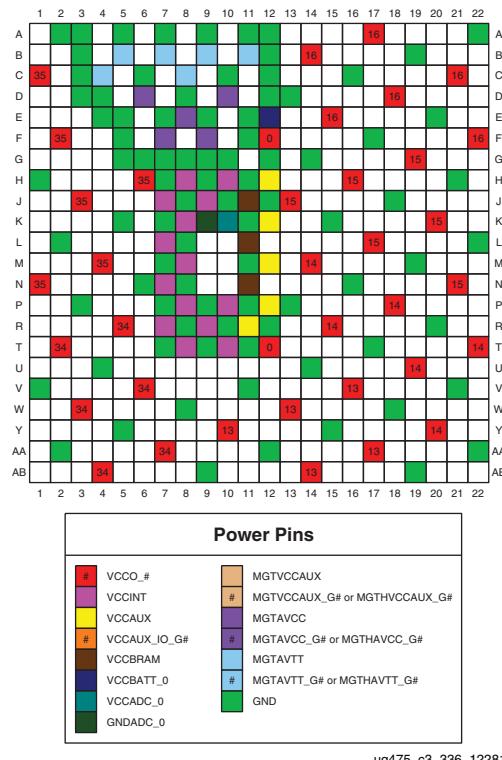
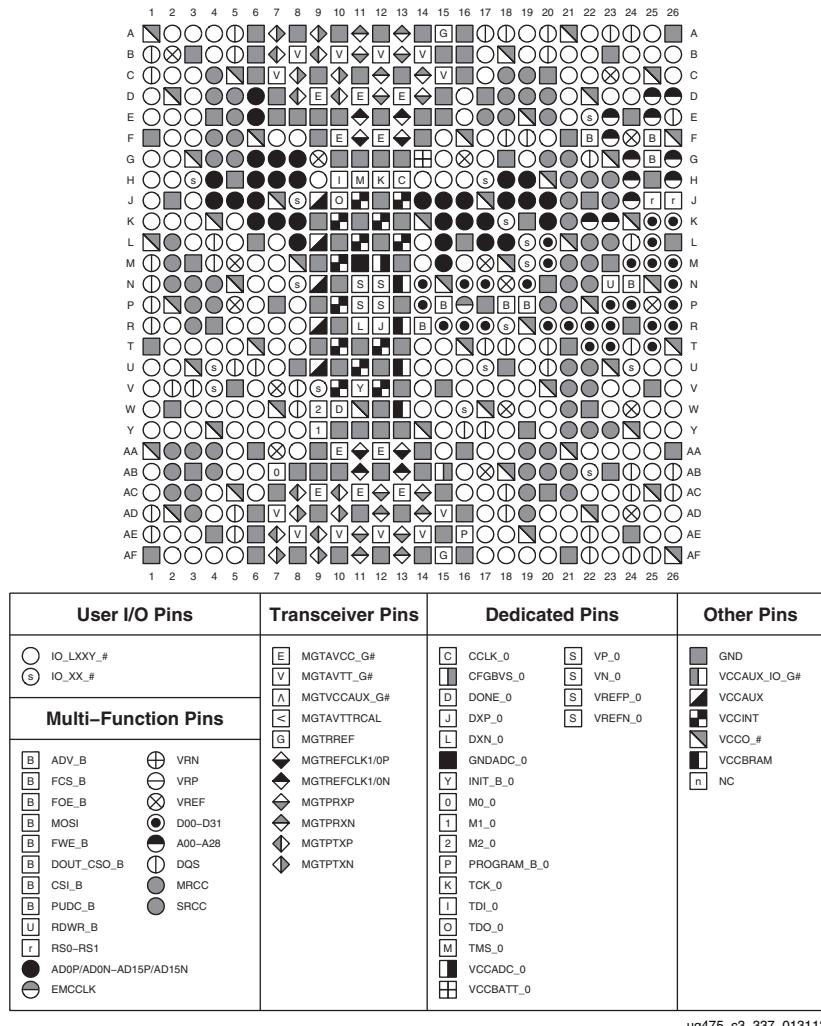


Figure 3-36: FB484, FBG484, FBV484, and RB484 Packages—XC7A200T Power and GND Placement

FB676, FBG676, FBV676, and RB676 Packages—XC7A200T



ug475_c3_337_013113

Figure 3-37: FB676, FBG676, FBV676, and RB676 Packages—XC7A200T Pinout Diagram

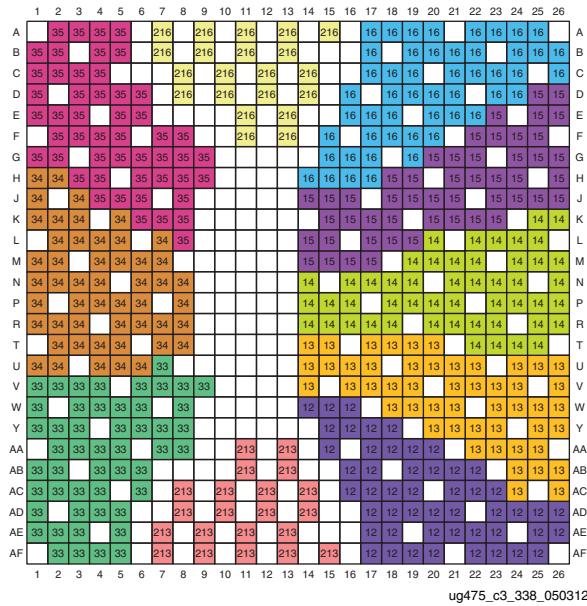


Figure 3-38: FB676, FBG676, FBV676, and RB676 Packages—XC7A200T I/O Banks

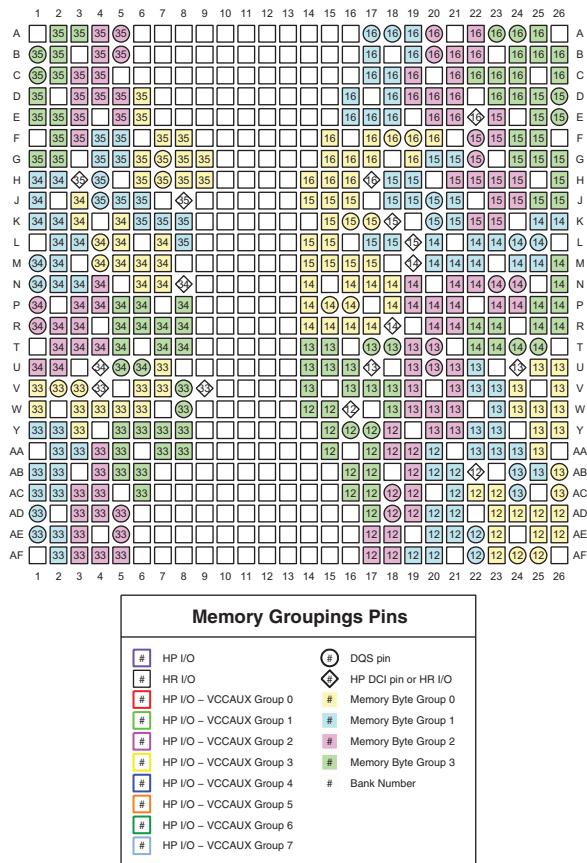
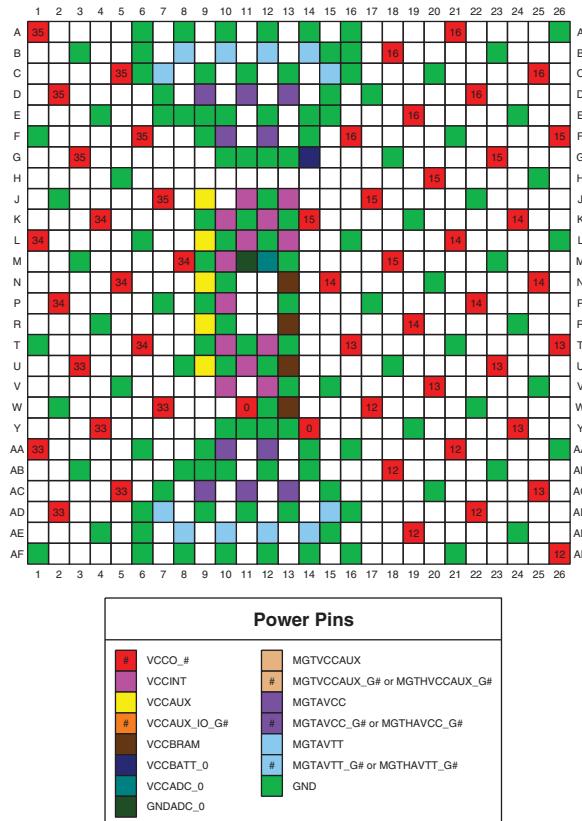


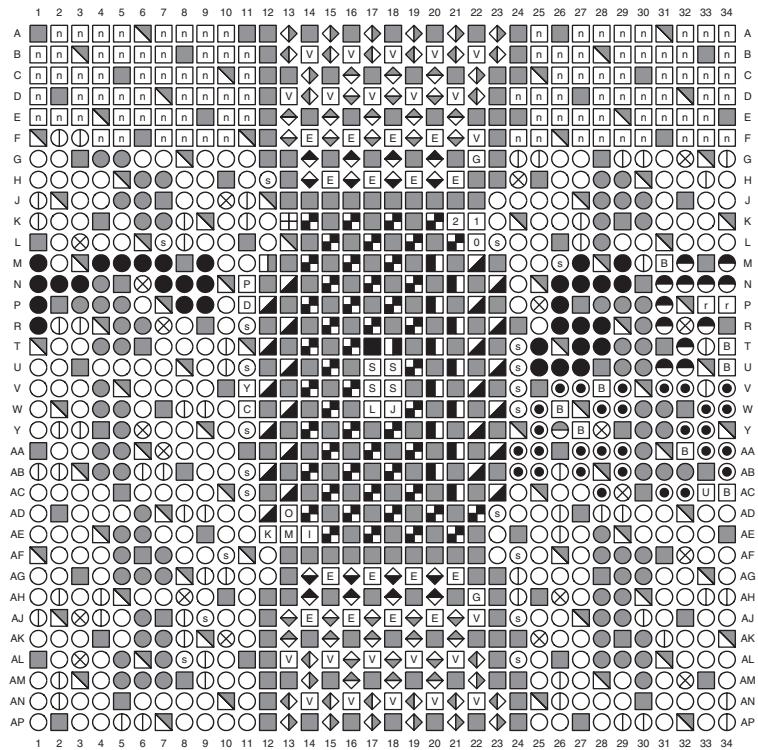
Figure 3-39: FB676, FBG676, FBV676, and RB676 Packages—XC7A200T Memory Groupings



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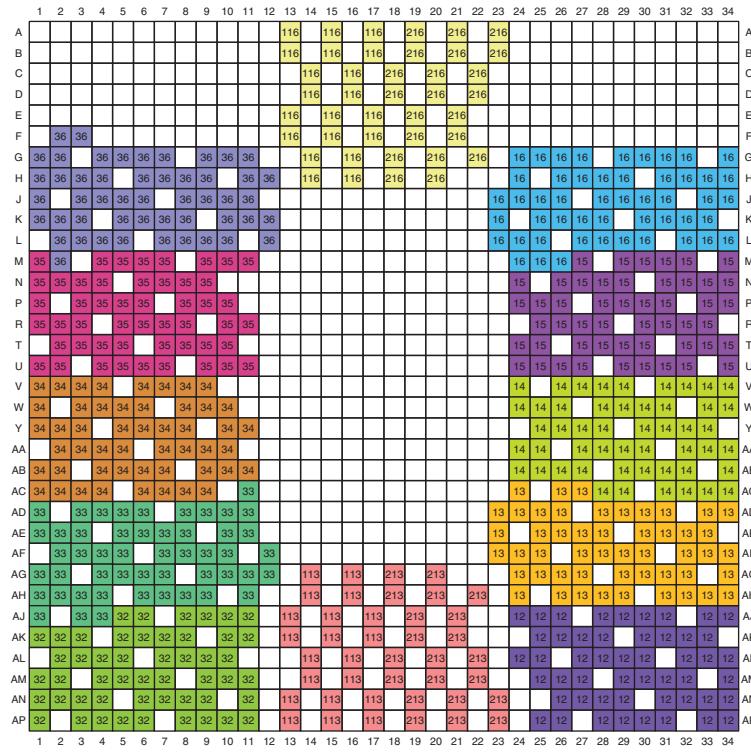
Figure 3-40: FB676, FBG676, FBV676, and RB676 Packages—XC7A200T Power and GND Placement

FF1156, FFG1156, and FFV1156 Packages—XC7A200T



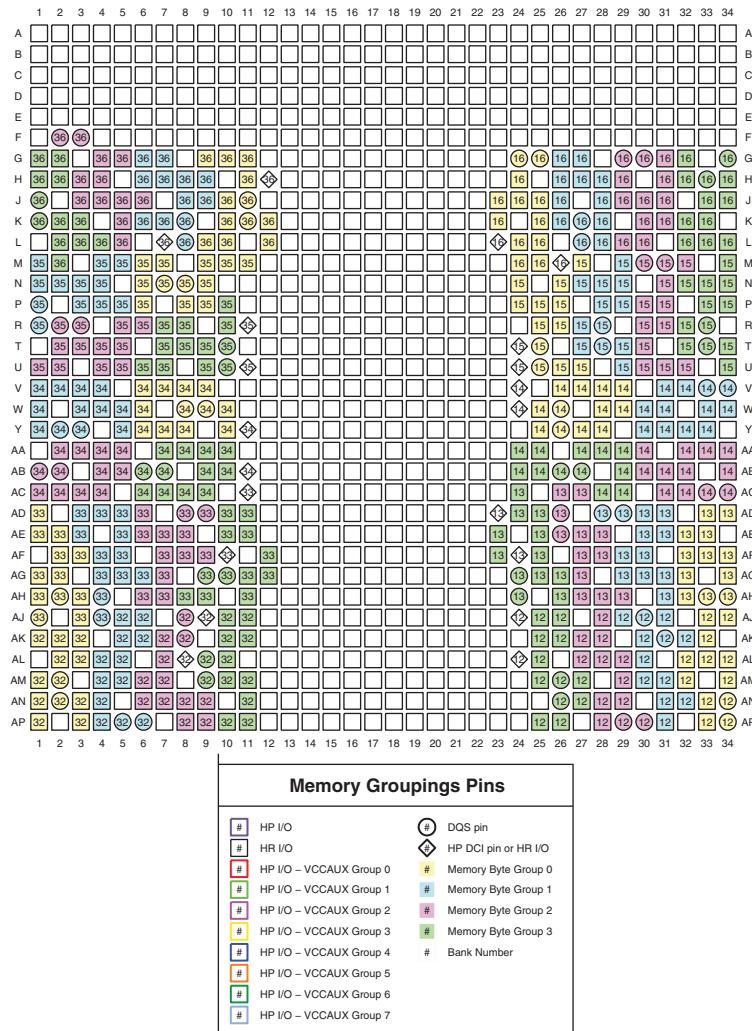
User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
<ul style="list-style-type: none"> (○) IO_LXXY_# (\\$) IO_XX_# <p>Multi-Function Pins</p> <ul style="list-style-type: none"> [B] ADV_B (⊕) VRN [B] FCS_B (⊖) VRP [B] FOE_B (⊗) VREF [B] MOSI (●) D00-D31 [B] FWE_B (●) A00-A28 [B] DOUT_CSQ_B (○) DQS [B] CSI_B (●) MRCC [B] PUDC_B (●) SRCC [U] RDWR_B [r] RS0-RS1 (●) AD0P/AD0N-AD15P/AD15N (●) EMCCLK 	<ul style="list-style-type: none"> [E] MGTAVCC_G# [V] MGTAVTT_G# [A] MGTVCCAUX_G# [L] MGTAVTRCAL [G] MGTRREF [◆] MGTRREFCLK1/0P [◆] MGTRREFCLK1/0N [◆] MGTPRXP [◆] MGTPRXN [◆] MGTPTXP [◆] MGPTXN 	<ul style="list-style-type: none"> [C] CCLK_0 [S] VP_0 [C] CFGBVS_0 [S] VN_0 [D] DONE_0 [S] VREFP_0 [J] DXP_0 [S] VREFN_0 [L] DXN_0 [■] GNDADC_0 [Y] INIT_B_0 [0] M0_0 [1] M1_0 [2] M2_0 [P] PROGRAM_B_0 [K] TCK_0 [I] TDl_0 [O] TDO_0 [M] TMS_0 [■] VCCADC_0 [H] VCCBATT_0 	<ul style="list-style-type: none"> [■] GND [■] VCCAUX_IO_G# [■] VCCAUX [■] VCCINT [■] VCCO_# [■] VCCBRAM [n] NC
			ug475_c3_341_122811

Figure 3-41: FF1156, FFG1156, and FFV1156 Packages—XC7A200T Pinout Diagram



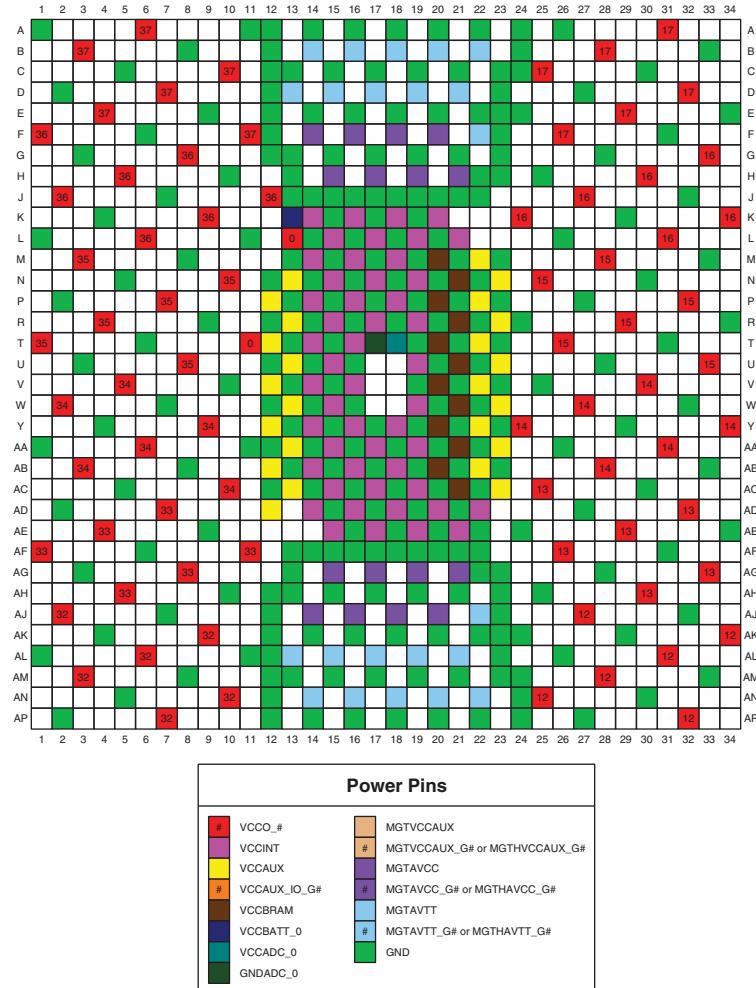
ug475_c3_342_050312

Figure 3-42: FF1156, FFG1156, and FFV1156 Packages—XC7A200T I/O Banks



ug475_c3_343_013014

Figure 3-43: FF1156, FFG1156, and FFV1156 Packages—XC7A200T Memory Groupings



ug475_c3_344_122811

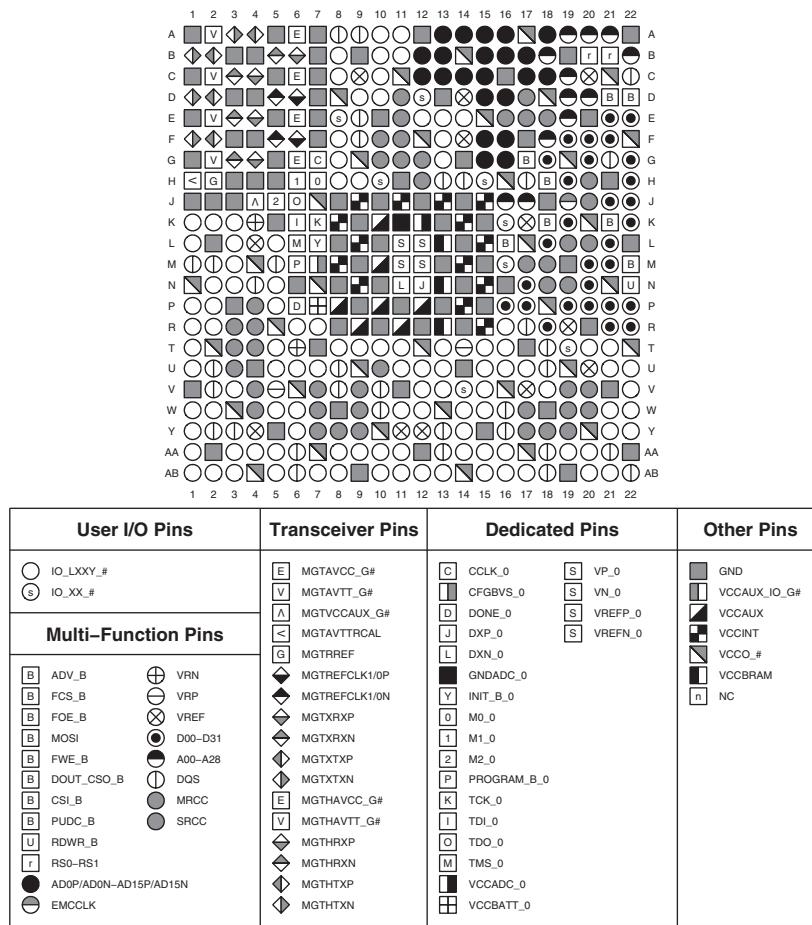
Figure 3-44: FF1156, FFG1156, and FFV1156 Packages—XC7A200T Power and GND Placement

Kintex-7 FPGAs Device Diagrams

Table 3-2: Kintex®-7 FPGAs Device Diagrams Cross-Reference

Device	FB484 FBG484 FBV484	FB676 FBG676 FBV676	FB900 FBG900 FBV900	FF676 FFG676 FFV676 RF676	FF900 FFG900 FFV900 RF900	FF901 FFG901 FFV901	FF1156 FFG1156 FFV1156
XC7K70T	page 93	page 96					
XC7K160T	page 93	page 99		page 106			
XC7K325T		page 99	page 102	page 106	page 110		
XC7K355T						page 114	
XC7K410T		page 99	page 102	page 106	page 110		
XC7K420T						page 118	page 122
XC7K480T						page 118	page 122

FB484, FBG484, and FBV484 Packages—XC7K70T and XC7K160T



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Figure 3-45: FB484, FBG484, and FBV484 Packages—XC7K70T and XC7K160T Pinout Diagram

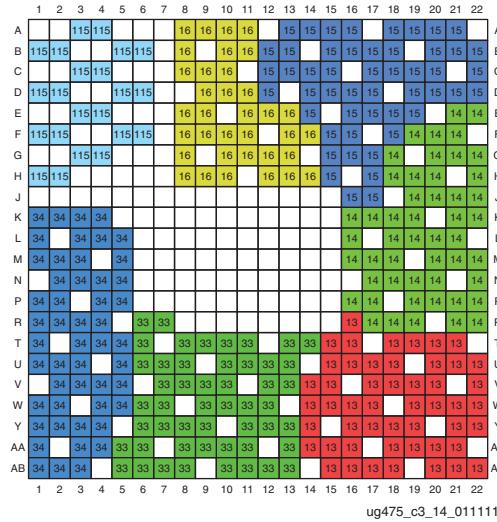


Figure 3-46: FB484, FBG484, and FBV484 Packages—XC7K70T and XC7K160T I/O Banks

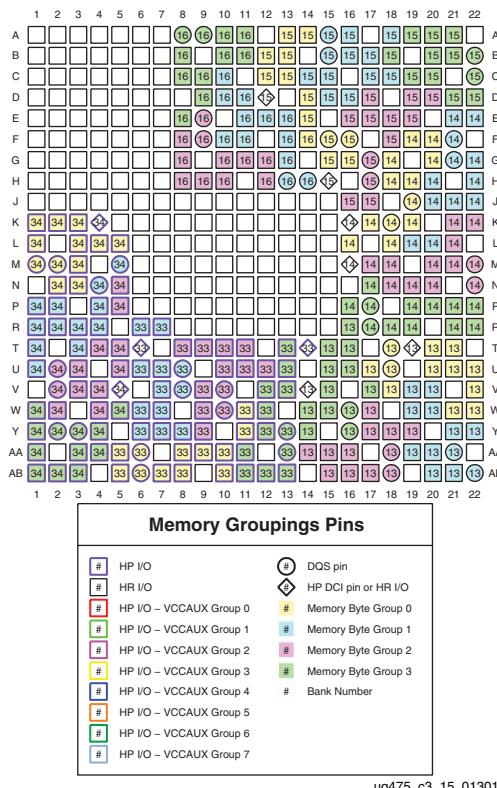
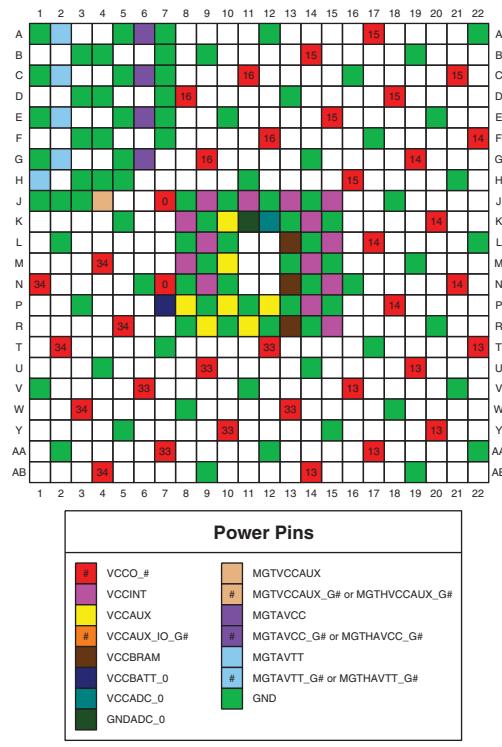


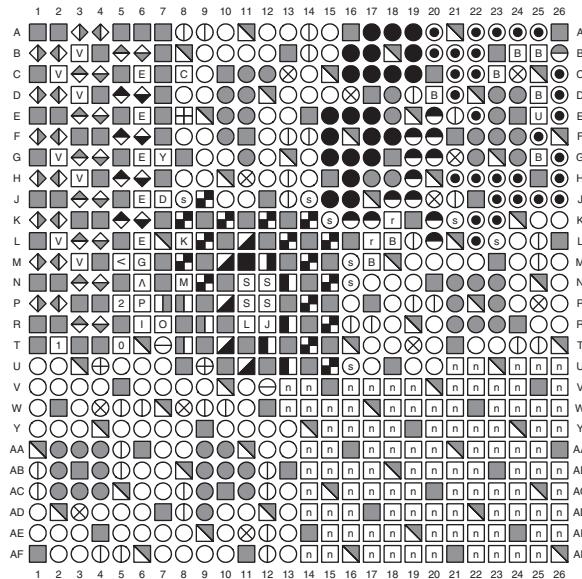
Figure 3-47: FB484, FBG484, and FBV484 Packages—XC7K70T and XC7K160T Memory Groupings



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Figure 3-48: FB484, FBG484, and FBV484 Packages—XC7K70T and XC7K160T Power and GND Placement

FB676, FBG676, and FBV676 Packages—XC7K70T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
<ul style="list-style-type: none"> ○ IO_LXXY_# (S) IO_XX_# 	<ul style="list-style-type: none"> [E] MGTAVCC_G# [V] MGTAVTT_G# [A] MGTVCCAUX_G# [L] MGTAVTTRCAL [G] MGTREF [D] MGTREFCLK1/0P [H] MGTREFCLK1/0N [F] MGTXRXP [I] MGTXRN [B] MGTXTP [J] MGTXTN [E] MGTHAVCC_G# [V] MGTHAVTT_G# [F] MGTHRXP [I] MGTHRN [D] MGTHTP [H] MGHTXN 	<ul style="list-style-type: none"> [C] CCLK_0 [V] CFGBVS_0 [D] DONE_0 [J] DXP_0 [L] DXN_0 [Y] GNDADC_0 [0] INIT_B_0 [1] M0_0 [2] M1_0 [3] M2_0 [P] PROGRAM_B_0 [K] TCK_0 [I] TDI_0 [O] TDO_0 [M] TMS_0 [T] VCCADC_0 [U] VCCBATT_0 	<ul style="list-style-type: none"> [■] GND [■] VCCAUX_IO_G# [■] VCCAUX [■] VCCINT [■] VCCO_# [■] VCCBRAM [n] NC
Multi-Function Pins <ul style="list-style-type: none"> [B] ADV_B [B] FCS_B [B] FOE_B [B] MOSI [B] FWE_B [B] DOUT_CS0_B [B] CSI_B [B] PUDC_B [U] RDWR_B [r] RS0-RS1 [●] AD0P/AD0N-AD15P/AD15N [○] EMCCLK 			

ug475_c3_05_090511

Figure 3-49: FB676, FBG676, and FBV676 Packages—XC7K70T Pinout Diagram

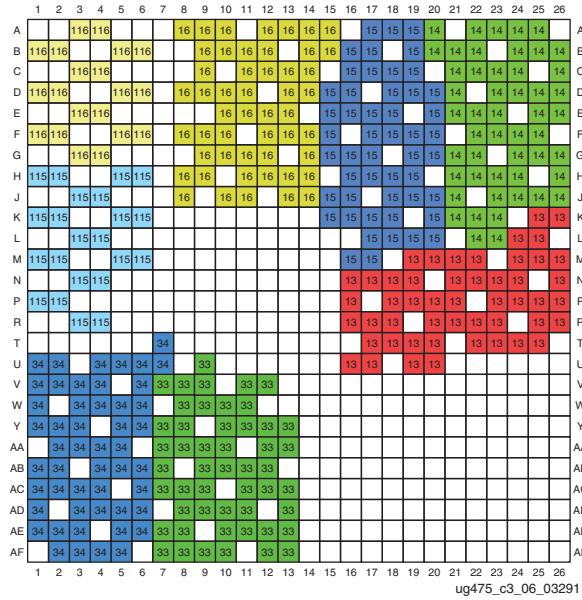


Figure 3-50: FB676, FBG676, and FBV676 Packages—XC7K70T I/O Banks

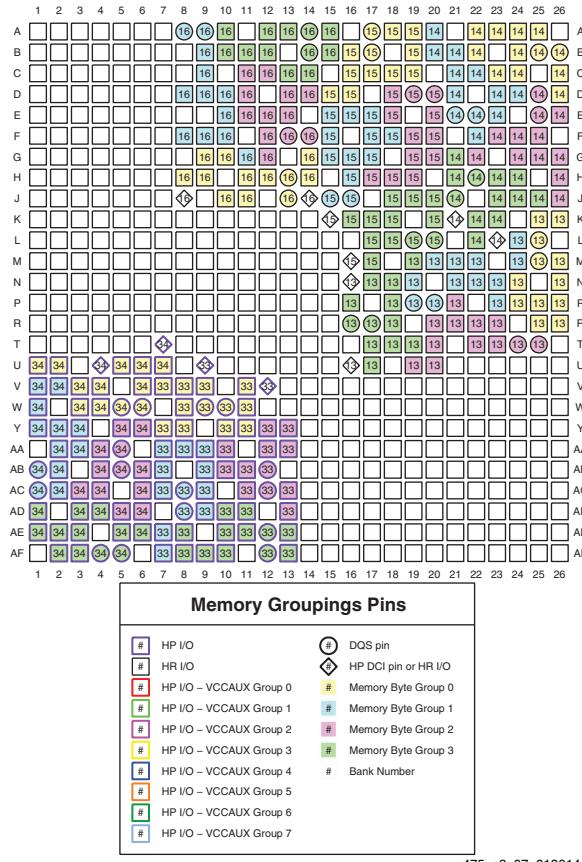


Figure 3-51: FB676, FBG676, and FBV676 Packages—XC7K70T Memory Groupings

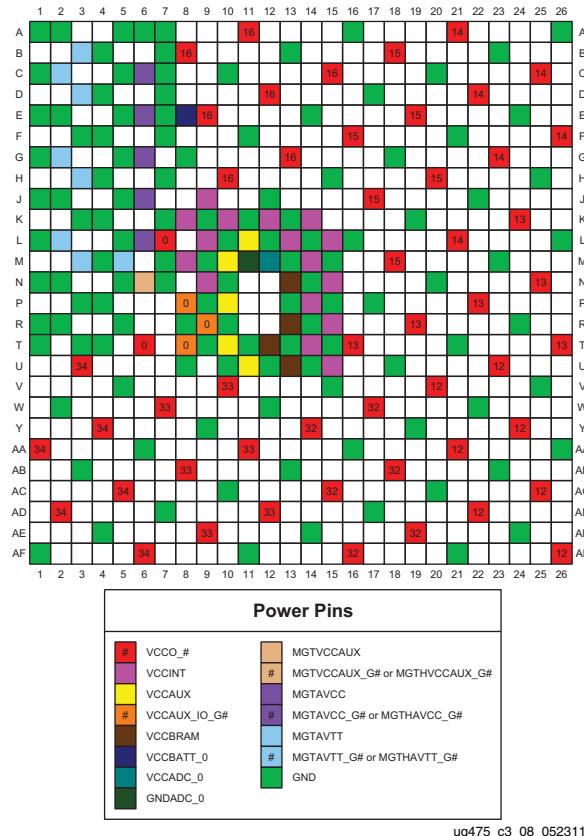
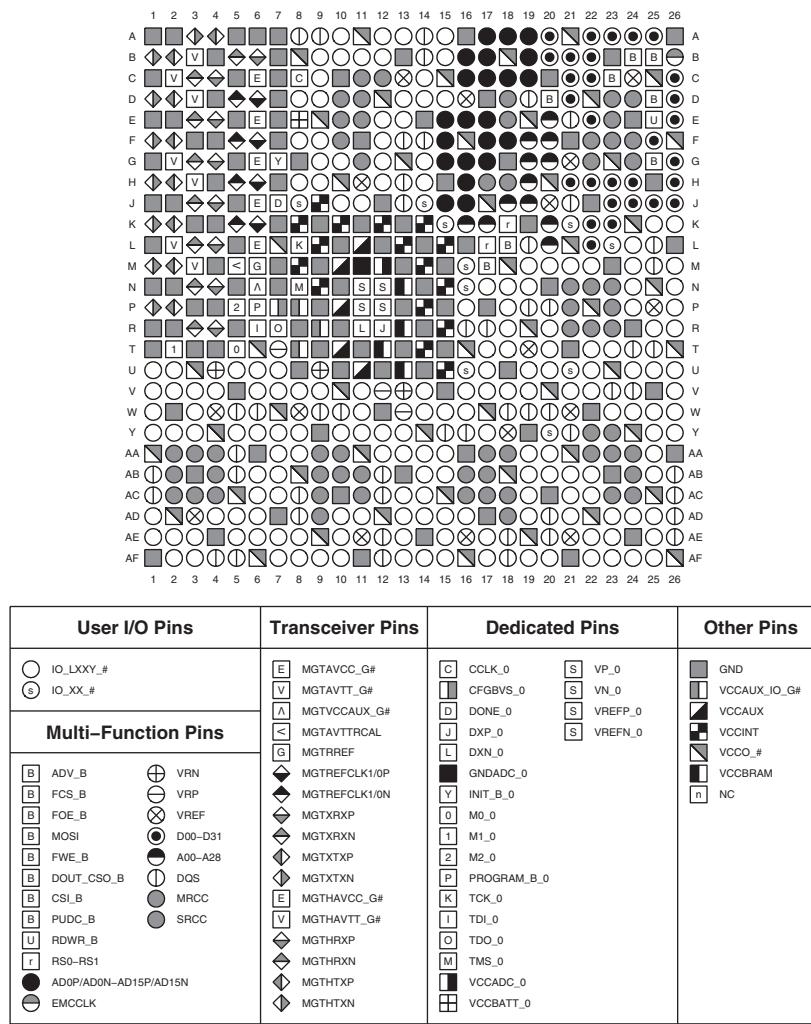


Figure 3-52: FB676, FBG676, and FBV676 Packages—XC7K70T Power and GND Placement

FB676, FBG676, and FBV676 Packages—XC7K160T, XC7K325T, and XC7K410T



ug475_c3_21_090511

Figure 3-53: FB676, FBG676, and FBV676 Packages—XC7K160T, XC7K325T, and XC7K410T Pinout Diagram

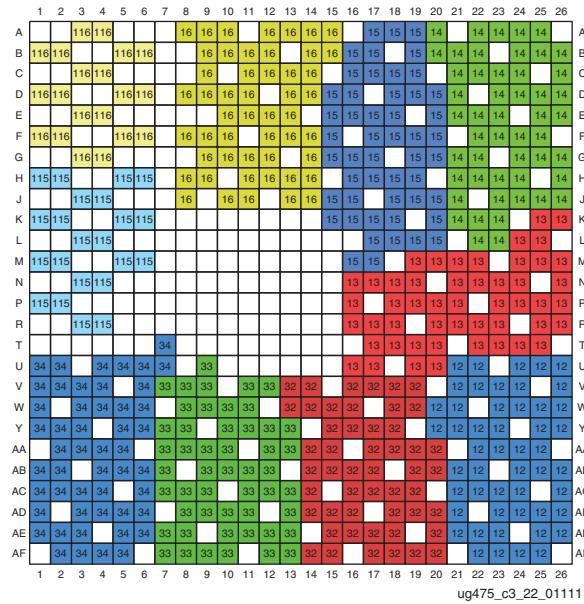


Figure 3-54: FB676, FBG676, and FBV676 Packages—XC7K160T, XC7K325T, and XC7K410T I/O Banks

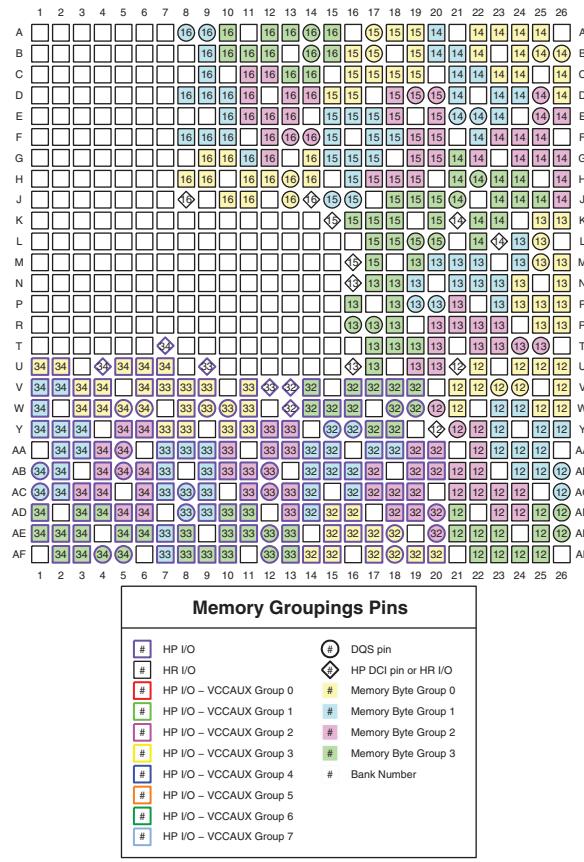


Figure 3-55: FB676, FBG676, and FBV676 Packages—XC7K160T, XC7K325T, and XC7K410T Memory Groupings

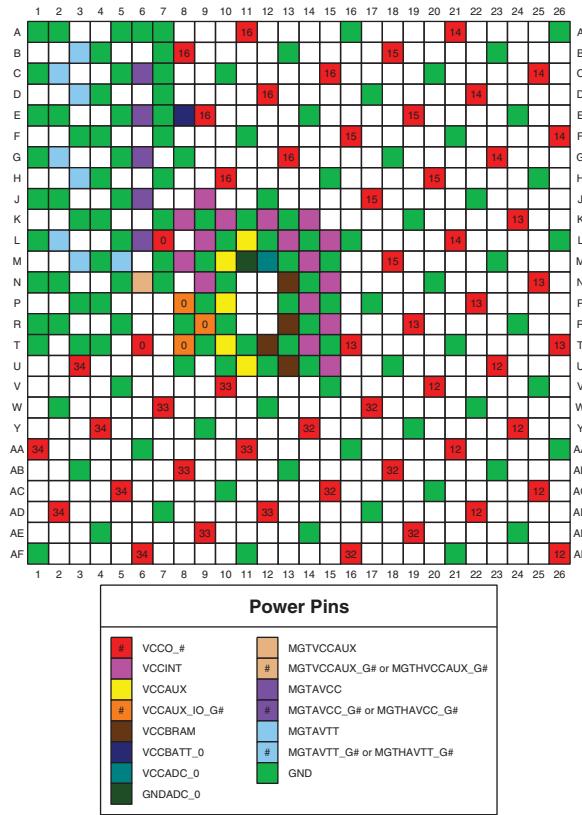
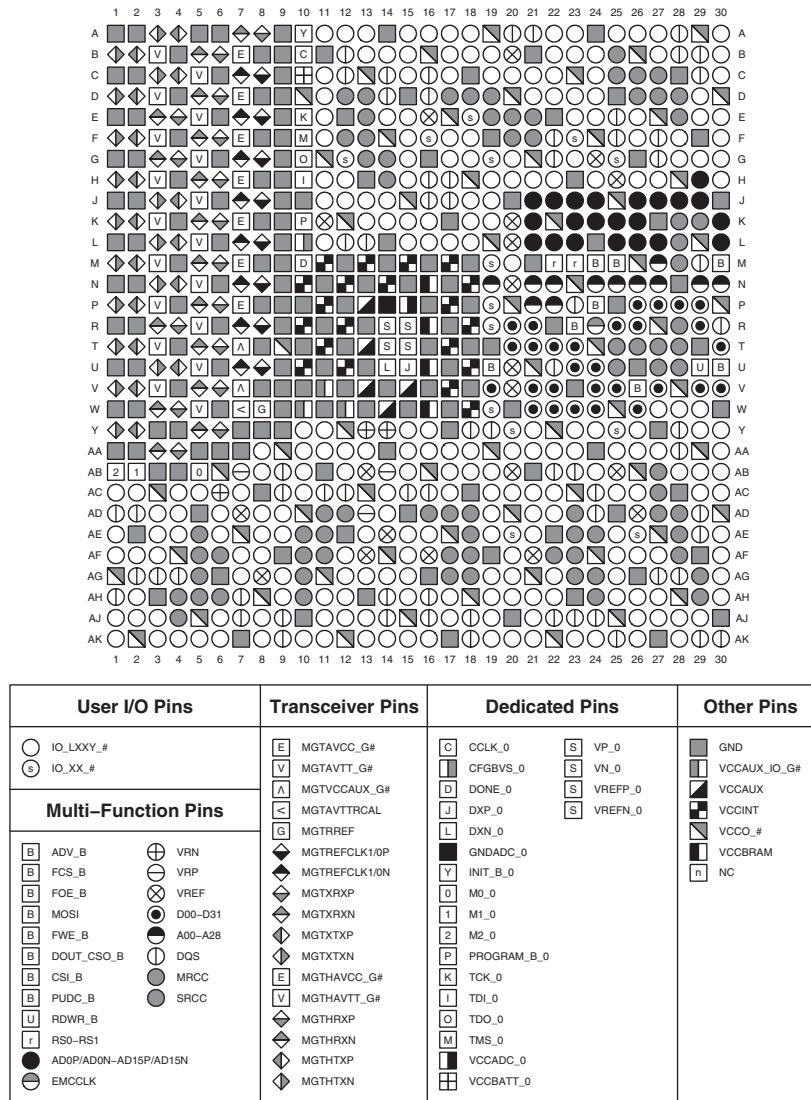


Figure 3-56: FB676, FBG676, and FBV676 Packages—XC7K160T, XC7K325T, and XC7K410T Power and GND Placement

FB900, FBG900, and FBV900 Packages—XC7K325T and XC7K410T



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Figure 3-57: FB900, FBG900, and FBV900 Packages—XC7K325T and XC7K410T Pinout Diagram

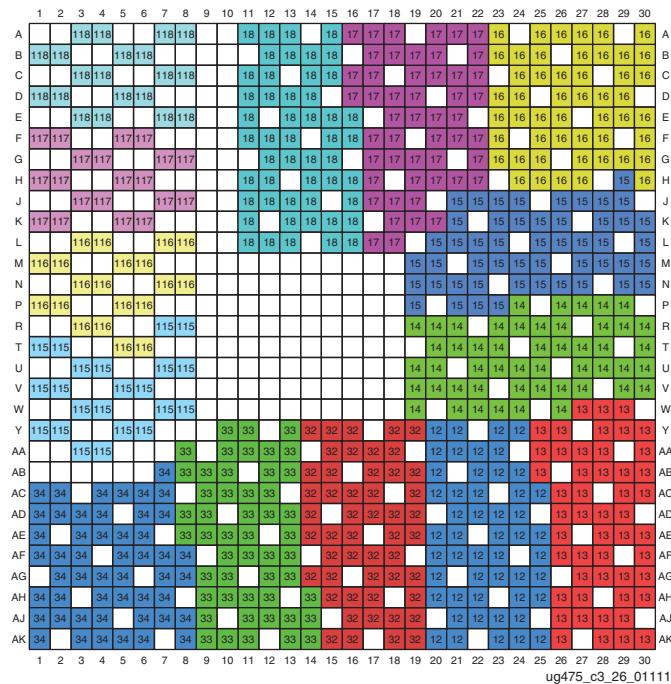
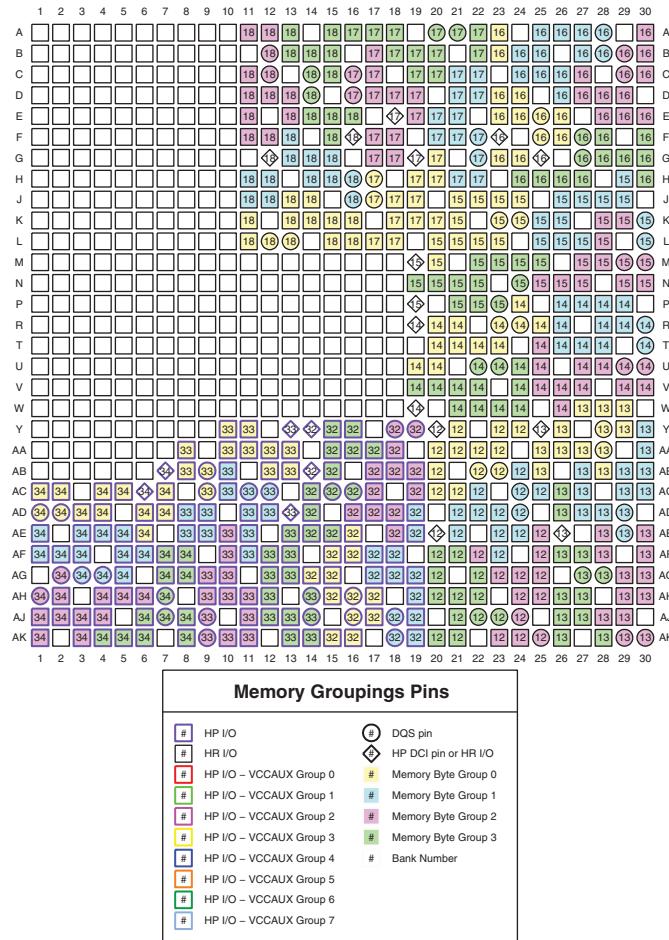
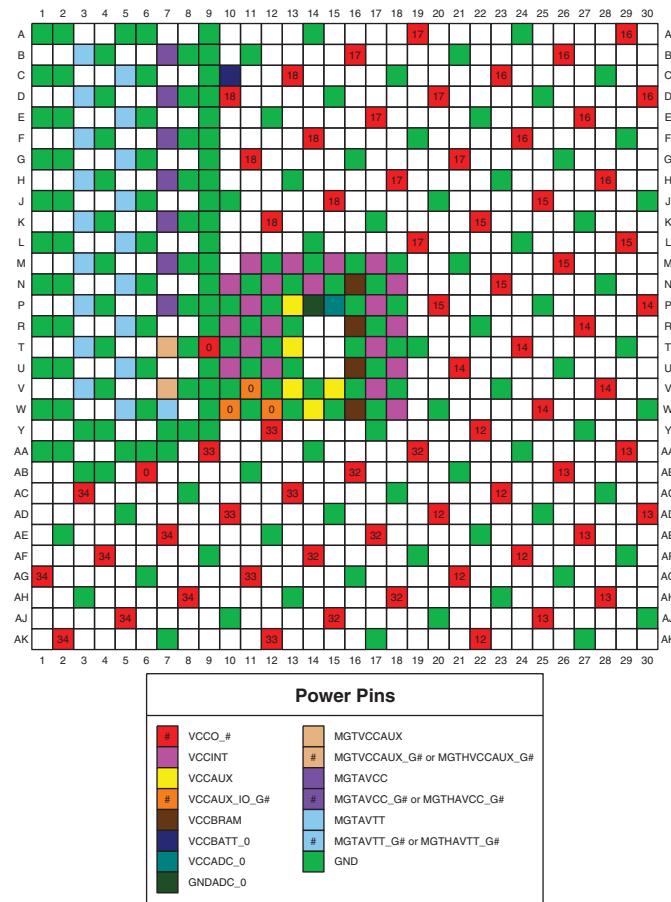


Figure 3-58: FB900, FBG900, and FBV900 Packages—XC7K325T and XC7K410T I/O Banks



ug475_c3_27_013014

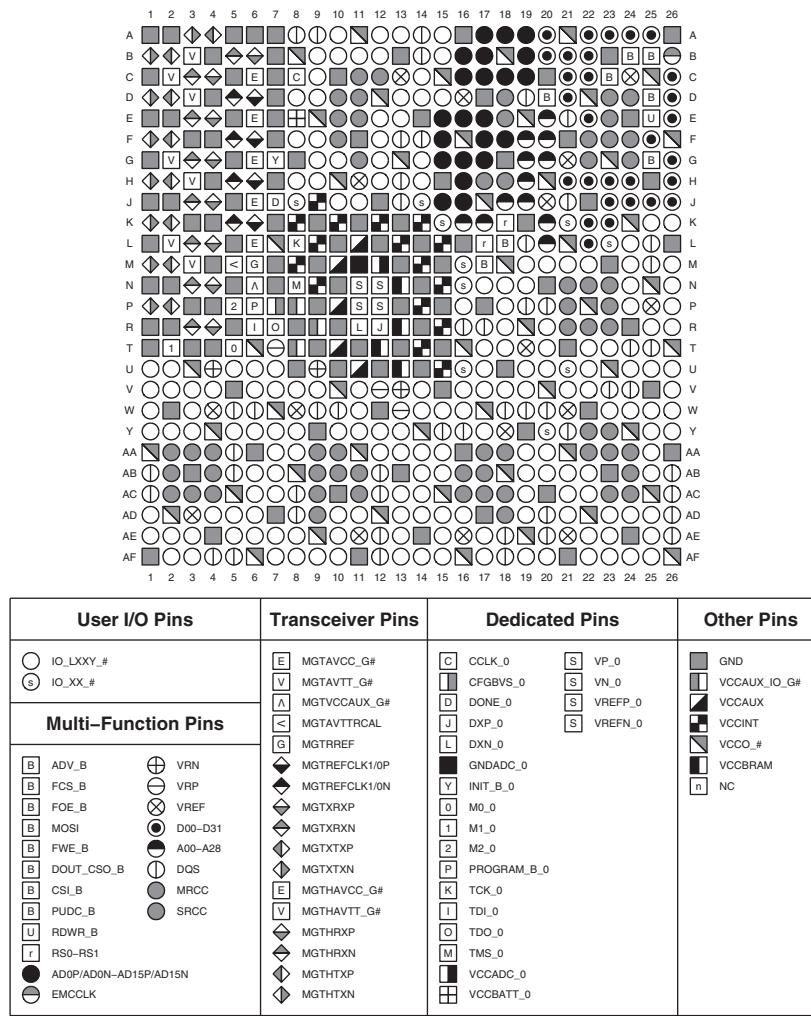
Figure 3-59: FB900, FBG900, and FBV900 Packages—XC7K325T and XC7K410T Memory Groupings



ug475_c3_28_052311

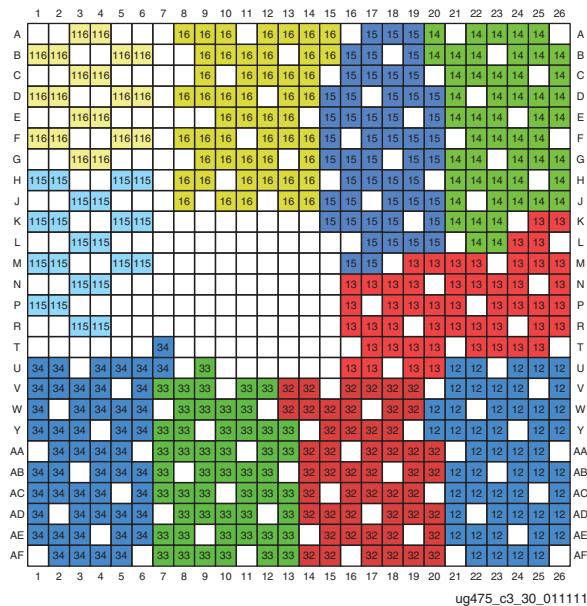
Figure 3-60: FB900, FBG900, and FBV900 Packages—XC7K325T and XC7K410T Power and GND Placement

FF676, FFG676, FFV676, and RF676 Packages—XC7K160T, XC7K325T, and XC7K410T



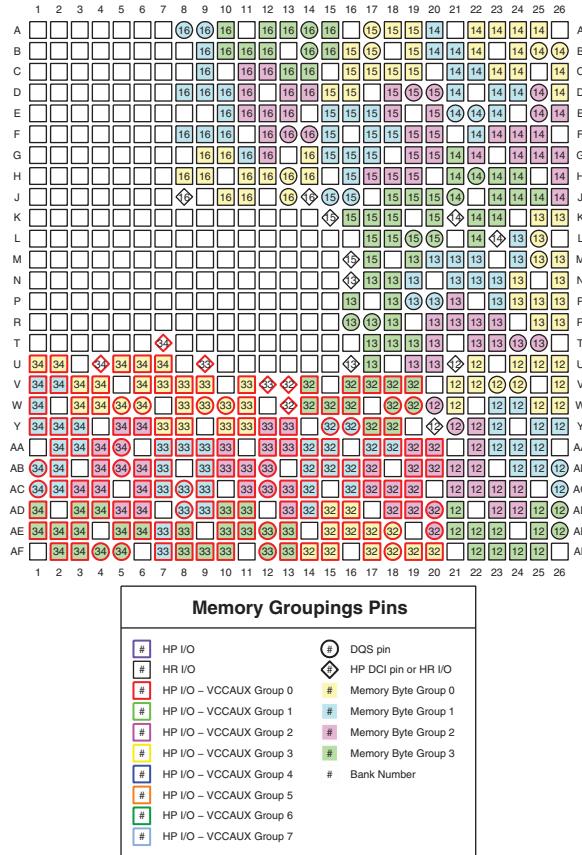
ug475_c3_29_090511

Figure 3-61: FF676, FFG676, FFV676, and RF676 Packages—XC7K160T, XC7K325T, and XC7K410T Pinout Diagram



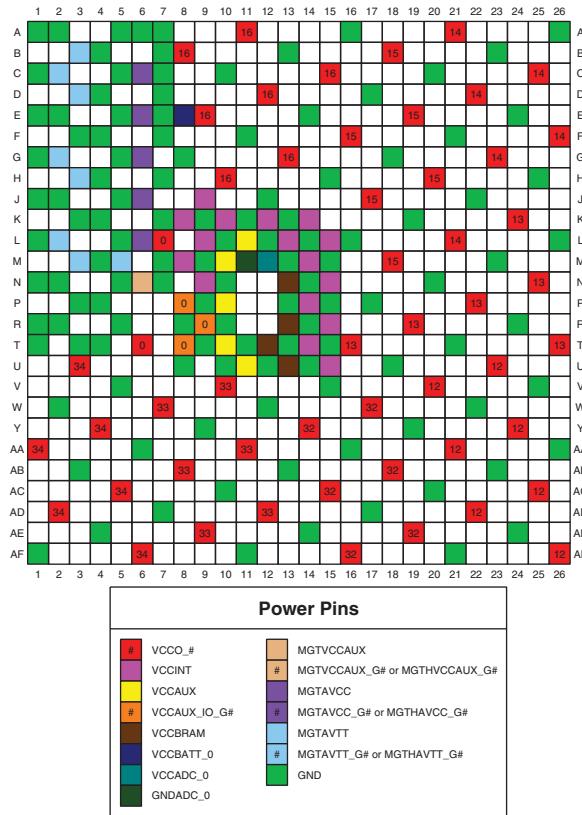
ug475_c3_30_011111

Figure 3-62: FF676, FFG676, FFV676, and RF676 Packages—XC7K160T, XC7K325T, and XC7K410T I/O Banks



ug475_c3_31_013014

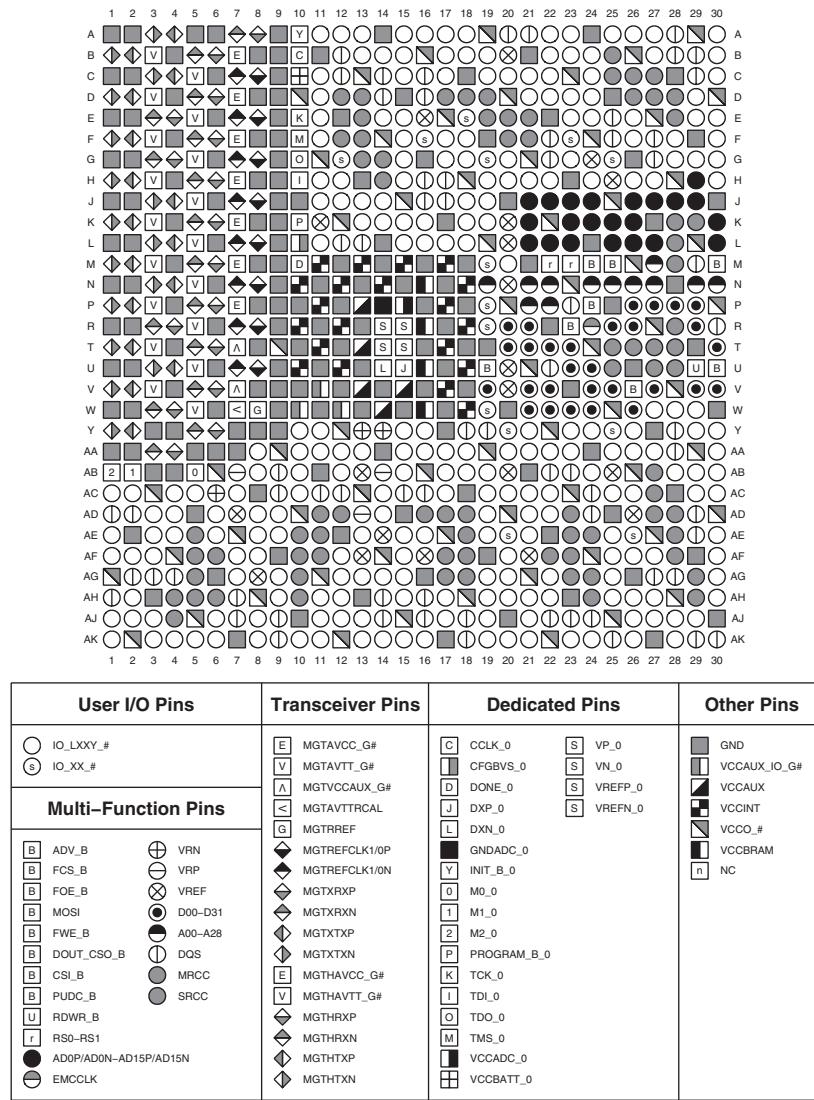
Figure 3-63: FF676, FFG676, FFV676, and RF676 Packages—XC7K160T, XC7K325T, and XC7K410T Memory Groupings



ug475_c3_32_052311

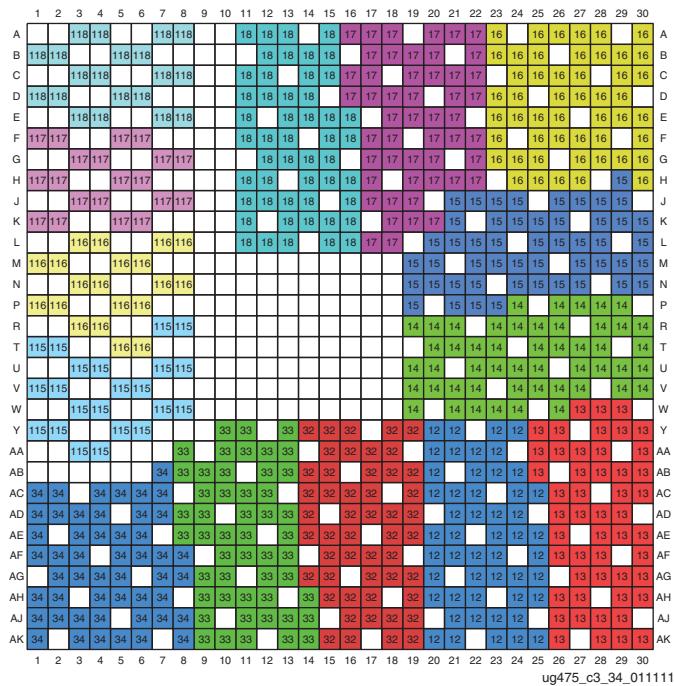
Figure 3-64: FF676, FFG676, FFV676, and RF676 Packages—XC7K160T, XC7K325T, and XC7K410T Power and GND Placement

FF900, FFG900, FFV900, and RF900 Packages—XC7K325T and XC7K410T



ug475_c3_33_090511

Figure 3-65: FF900, FFG900, FFV900, and RF900 Packages—XC7K325T and XC7K410T Pinout Diagram



ug475_c3_34_011111

Figure 3-66: FF900, FFG900, FFV900, and RF900 Packages—XC7K325T and XC7K410T I/O Banks

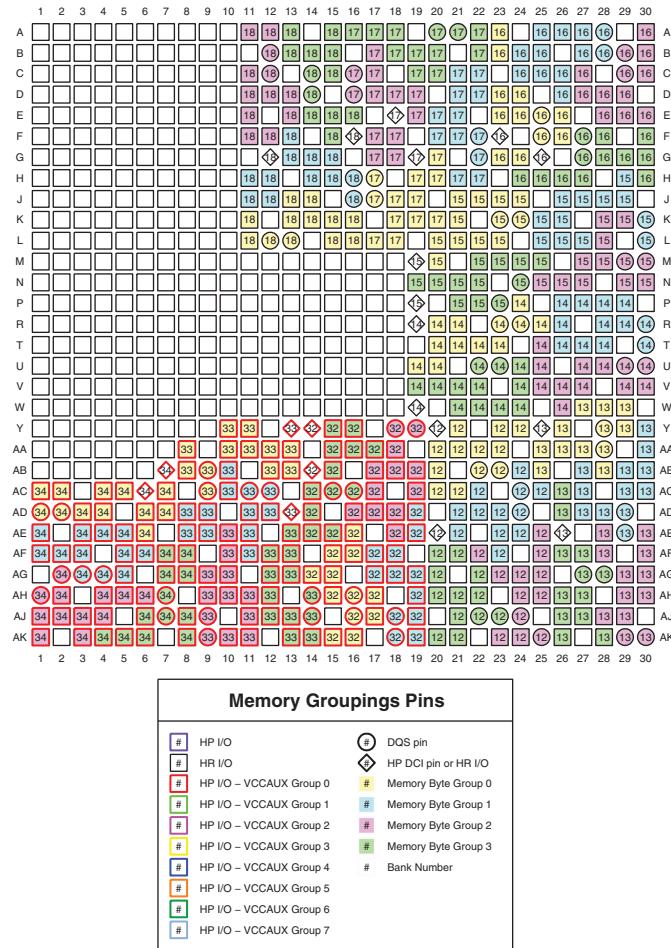
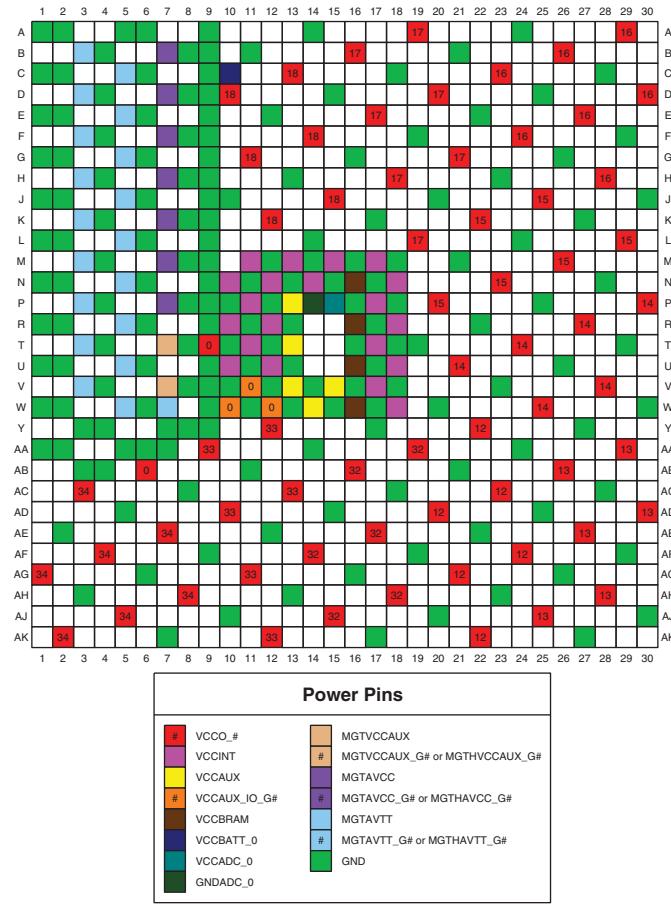


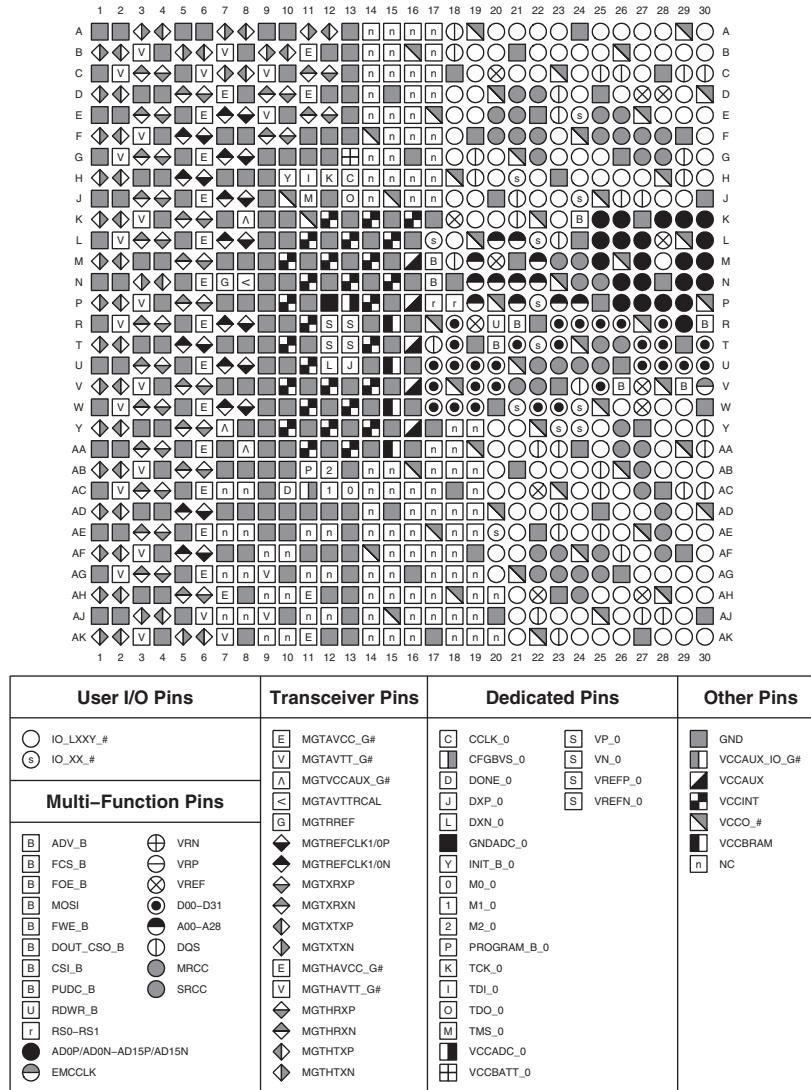
Figure 3-67: FF900, FFG900, FFV900, and RF900 Packages—XC7K325T and XC7K410T Memory Groupings



ug475_c3_36_052311

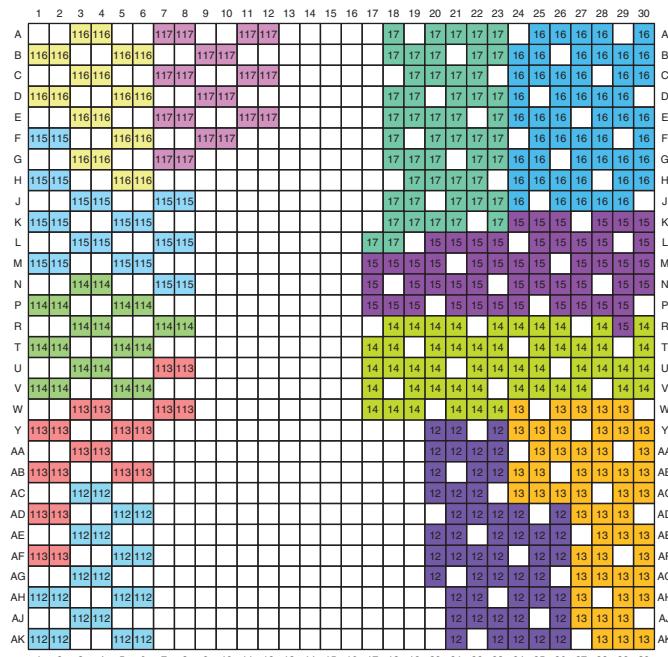
Figure 3-68: FF900, FFG900, FFV900, and RF900 Packages—XC7K325T and XC7K410T Power and GND Placement

FF901, FFG901, and FFV901 Packages—XC7K355T



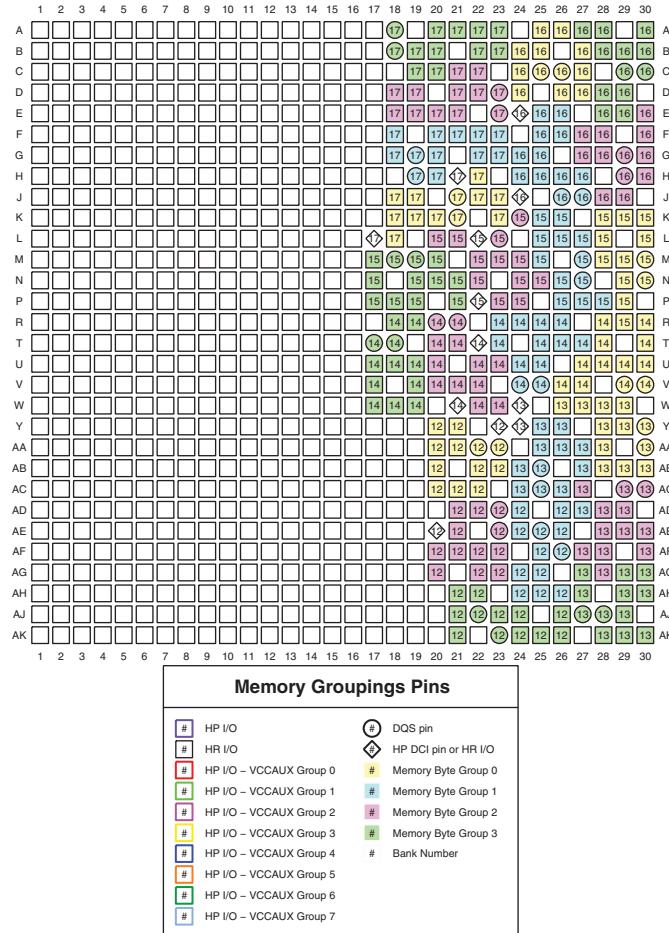
ug475_c3_37_090511

Figure 3-69: FF901, FFG901, and FFV901 Packages—XC7K355T Pinout Diagram



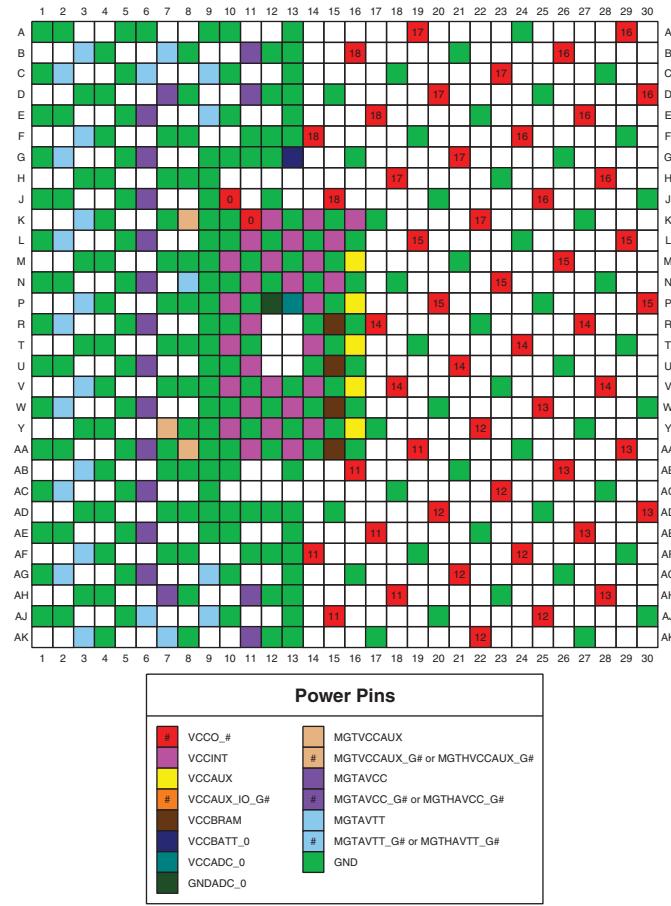
ug475_c3_38_052311

Figure 3-70: FF901, FFG901, and FFV901 Packages—XC7K355T I/O Banks



ug475_c3_39_013014

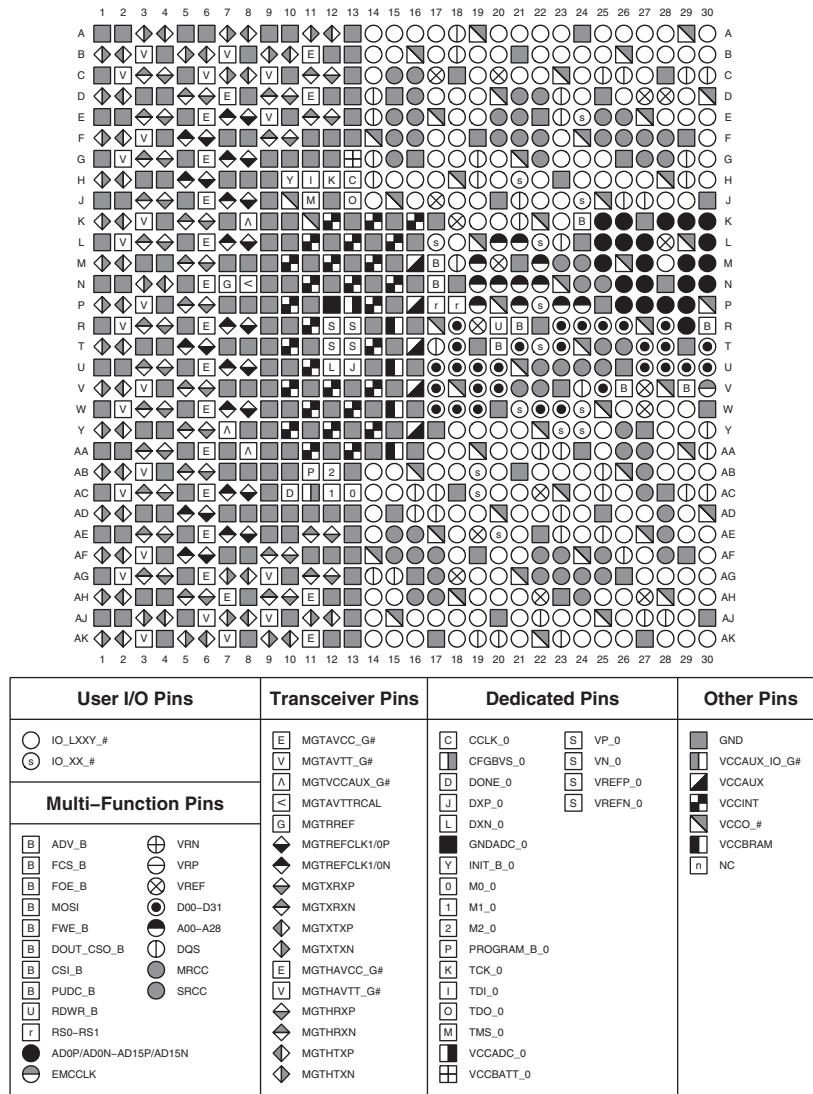
Figure 3-71: FF901, FFG901, and FFV901 Packages—XC7K355T Memory Groupings



ug475_c3_40_052311

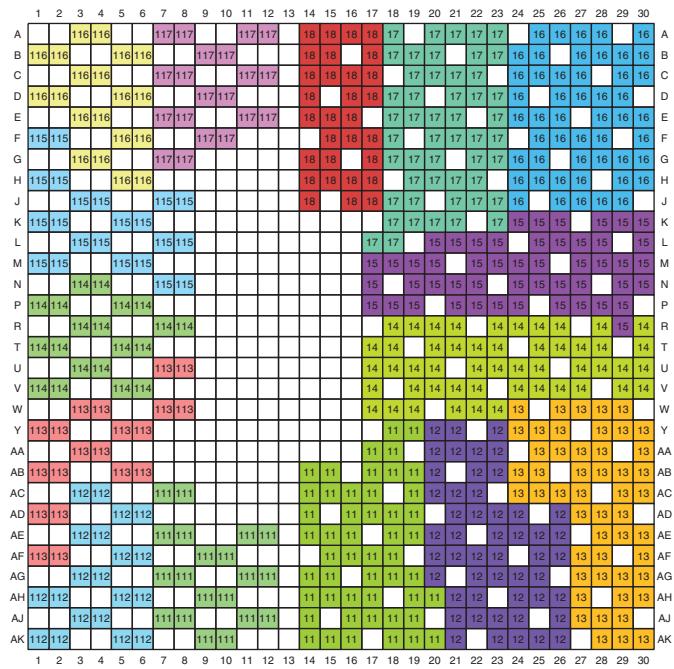
Figure 3-72: FF901, FFG901, and FFV901 Packages—XC7K355T Power and GND Placement

FF901, FFG901, and FFV901 Packages—XC7K420T and XC7K480T



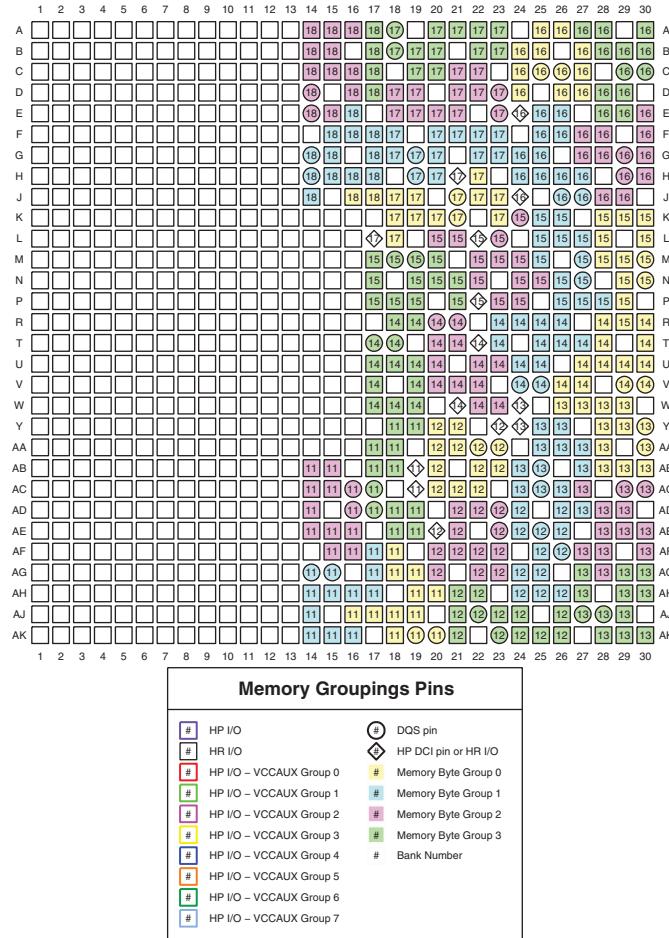
ug475_c3_45_090511

Figure 3-73: FF901, FFG901, and FFV901 Packages—XC7K420T and XC7K480T Pinout Diagram



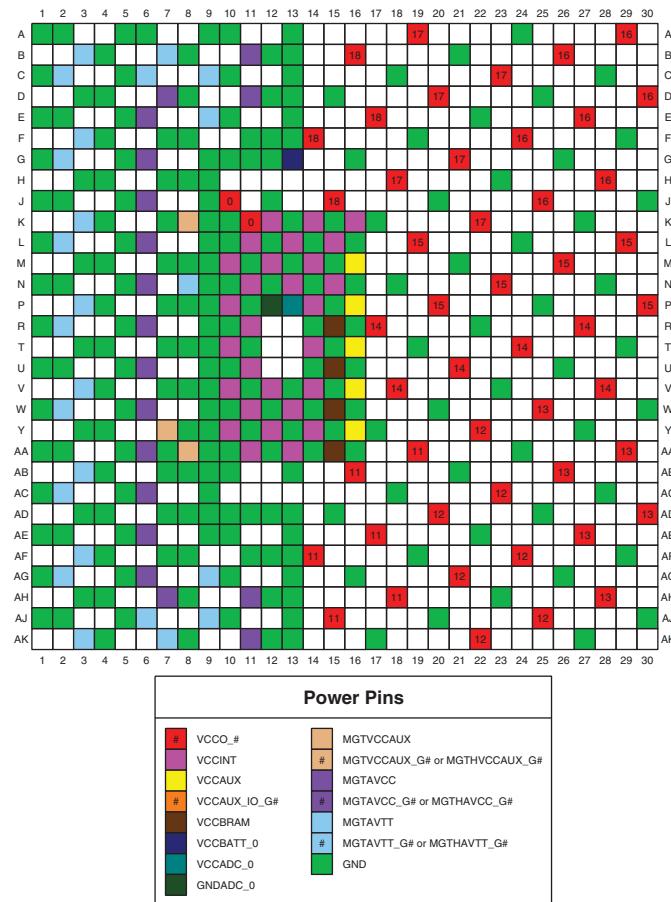
ug475_c3_46_052311

Figure 3-74: FF901, FFG901, and FFV901 Packages—XC7K420T and XC7K480T I/O Banks



ug475_c3_47_013014

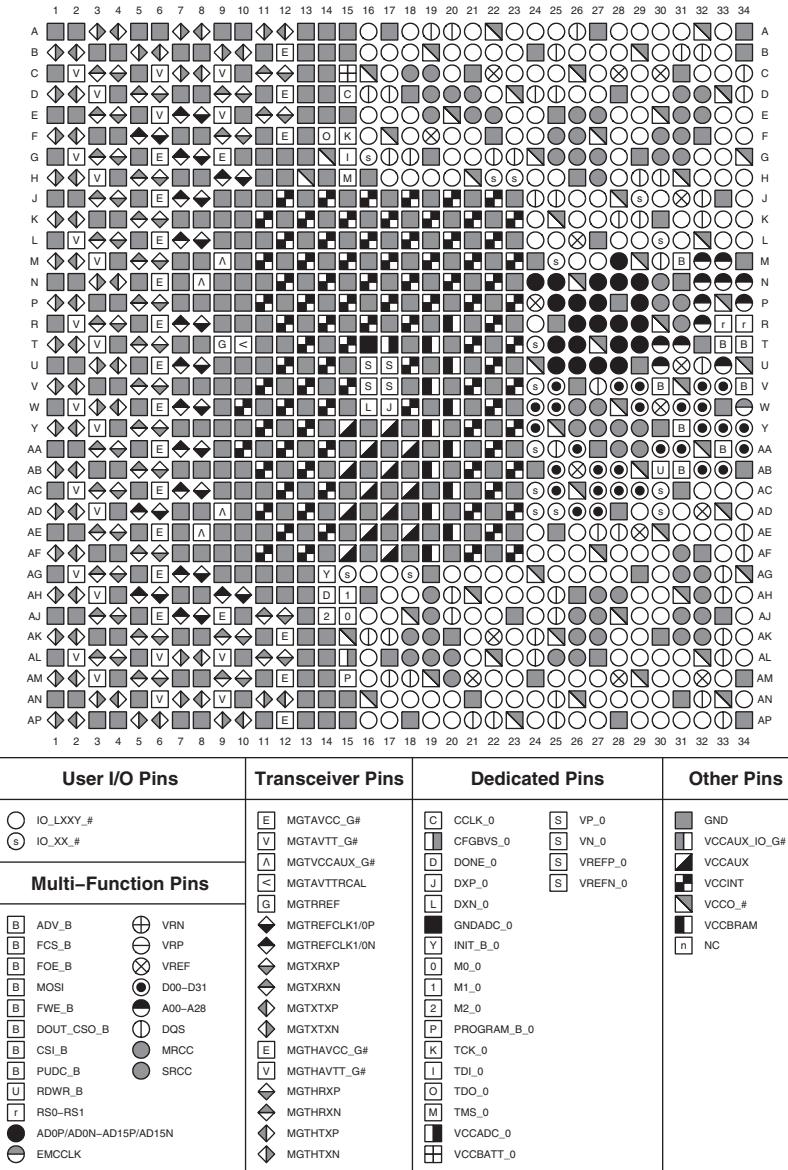
Figure 3-75: FF901, FFG901, and FFV901 Packages—XC7K420T and XC7K480T Memory Groupings



ug475_c3_48_052311

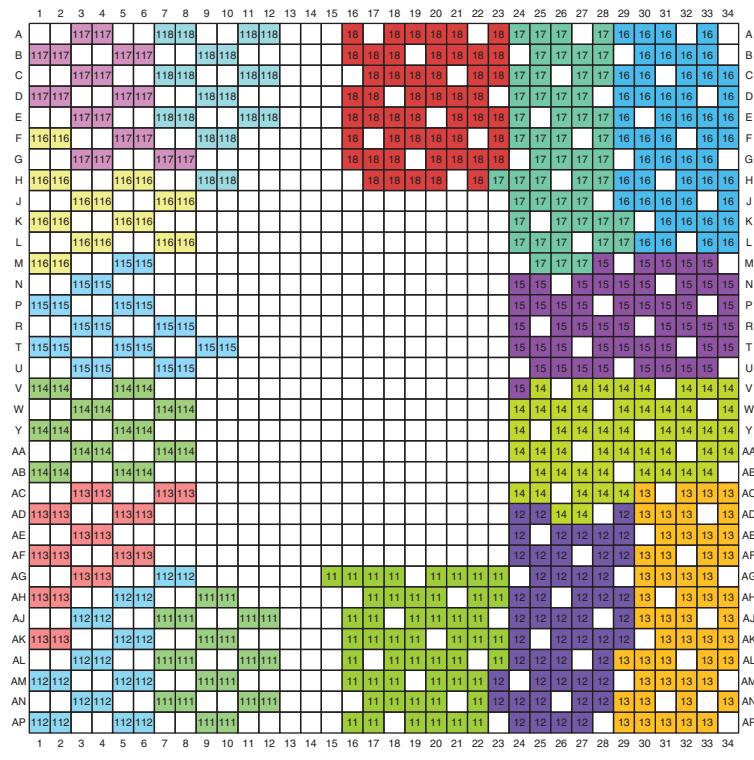
Figure 3-76: FF901, FFG901, and FFV901 Packages—XC7K420T and XC7K480T Power and GND Placement

FF1156, FFG1156, and FFV1156 Packages—XC7K420T and XC7K480T



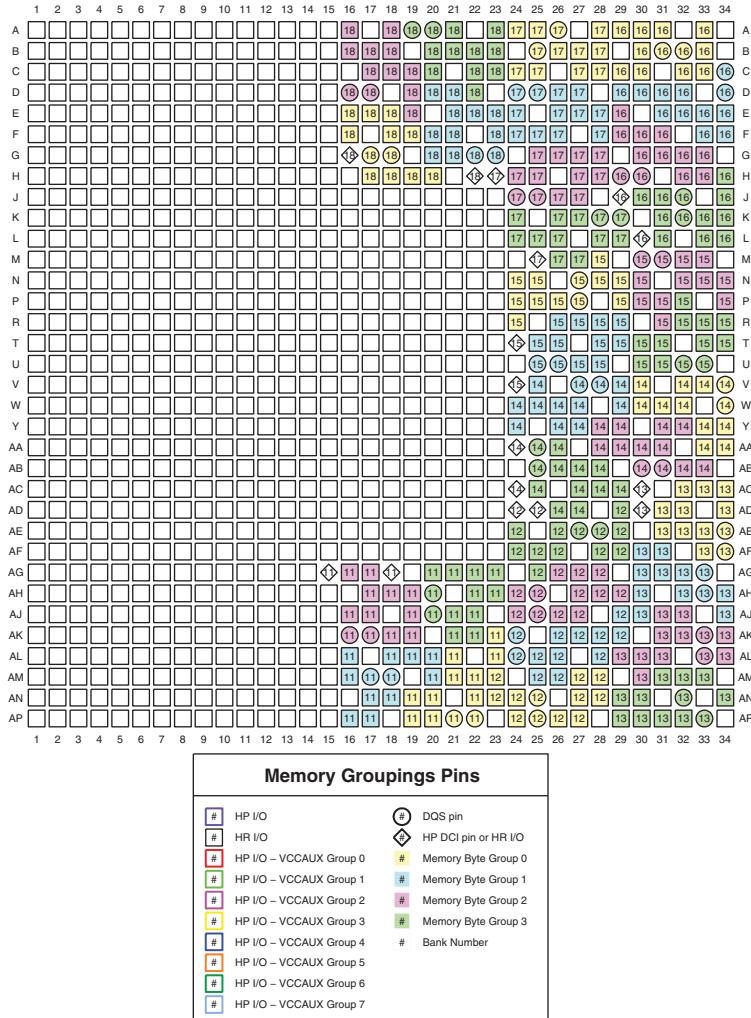
ug475_c3_53_090511

Figure 3-77: FF1156, FFG1156, and FFV1156 Packages—XC7K420T and XC7K480T Pinout Diagram



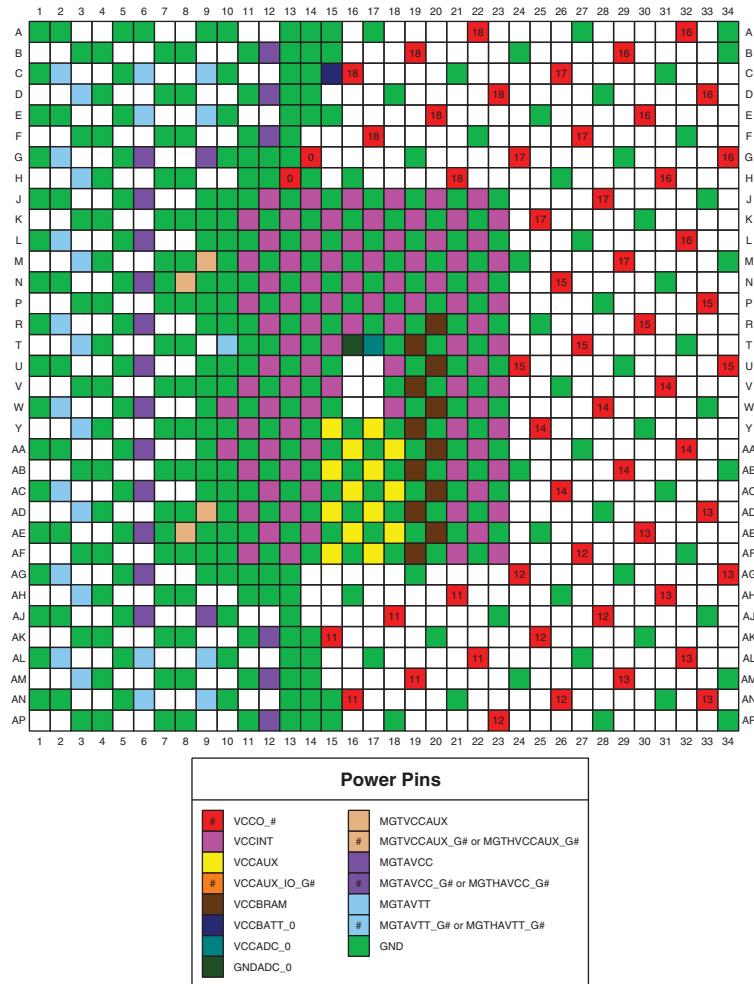
ug475_c3_54_052311

Figure 3-78: FF1156, FFG1156, and FFV1156 Packages—XC7K420T and XC7K480T I/O Banks



ug475_c3_55_013014

Figure 3-79: FF1156, FFG1156, and FFV1156 Packages—XC7K420T and XC7K480T Memory Groupings



ug475_c3_56_052311

Figure 3-80: FF1156, FFG1156, and FFV1156 Packages—XC7K420T and XC7K480T Power and GND Placement

Virtex-7 FPGAs Device Diagrams

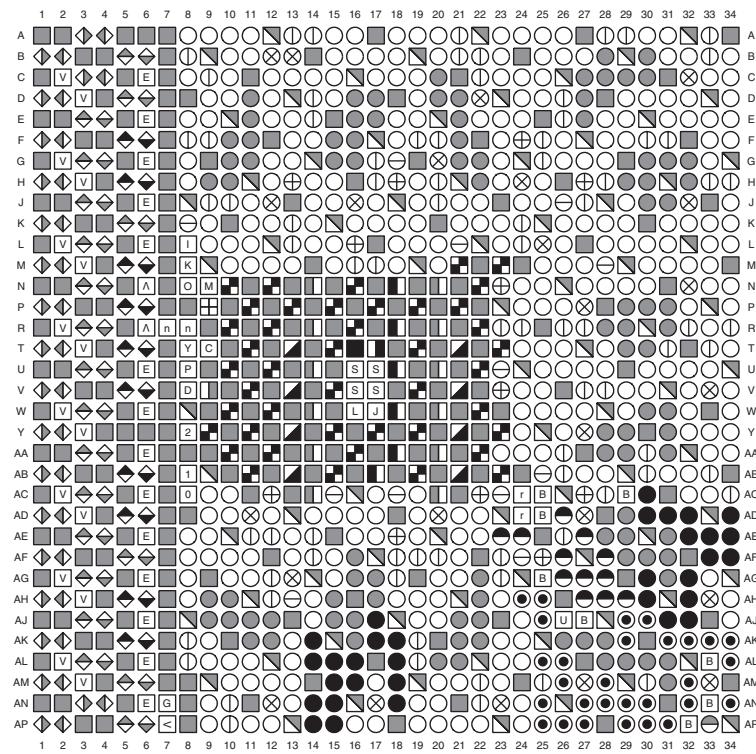
Table 3-3: Virtex®-7 T FPGAs Device Diagrams Cross Reference

Device	FF1157 FFG1157 RF1157	FF1761 FFG1761 RF1761	FL1925 FLG1925	FH1761 FHG1761
XC7V585T	page 127	page 131		
XC7V2000T			page 135	page 139

Table 3-4: Virtex-7 XT FPGAs Device Diagrams Cross Reference

Device	FF1157 FFG1157 FFV1157 RF1157	FF1158 FFG1158 FFV1158 RF1158	FF1761 FFG1761 FFV1761 RF1761	FF1926 FFG1926	FF1927 FFG1927 FFV1927	FF1928 FFG1928	FF1930 FFG1930 RF1930	FL1926 FLG1926	FL1928 FLG1928	FL1930 FLG1930
XC7VX330T	page 143		page 147							
XC7VX415T	page 143	page 151			page 155					
XC7VX485T	page 159	page 163	page 167		page 171		page 175			
XC7VX550T		page 151			page 187					
XC7VX690T	page 143	page 151	page 179	page 183	page 187		page 191			
XC7VX980T				page 183		page 195	page 199			
XC7VX1140T								page 203	page 207	page 211

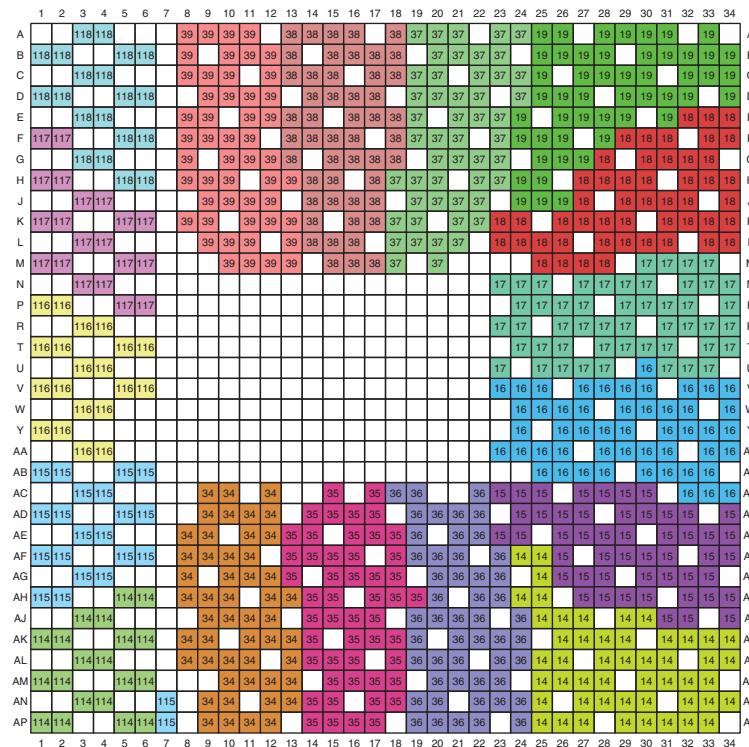
FF1157, FFG1157, and RF1157 Packages—XC7V585T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins		
<input type="circle"/> IO_LXXY_# <input style="border: 1px solid black; border-radius: 50%; padding: 2px 4px;" type="circle"/> IO_XX_#	Multi-Function Pins B ADV_B <input type="circle"/> VRN B FCS_B <input type="circle"/> VRP B FOE_B <input type="circle"/> VREF B MOSI <input type="circle"/> D00-D31 B FWE_B <input type="circle"/> A00-A28 B DOUT_CS0_B <input type="circle"/> DQS B CSI_B <input type="circle"/> MRCC B PUDC_B <input type="circle"/> SRCC U RDWR_B R RS0-RS1 ● AD0P/AD0N-AD15P/AD15N ○ EMCCLK	E MGTAVCC_G# V MGTAVTT_G# A MGTVAUXCAU_G# C MGTAVTRCAL G MGTRREF ◆ MGTREFCLK1/0P ◆ MGTREFCLK1/0N ◆ MGTTRXP ◆ MGTTRXN ◆ MGTXTXP ◆ MGTXTXN E MGTHAVCC_G# V MGTHAVTT_G# ◆ MGTHTRXP ◆ MGTHRXN ◆ MGTHTXP ◆ MGHTHDXN	C CCLK_0 V CFGBVS_0 A DONE_0 P DXP_0 L DXN_0 S GND S VN_0 S VREFF_0 S VREFN_0	S VP_0 S VN_0 S VREFF_0 S VREFN_0	GND VCCAUX_IO_G# VCCAUX VCCINT VCCO_# VCCBRAM NC
		C CCLK_0 V CFGBVS_0 A DONE_0 P DXP_0 L DXN_0 S GND S VN_0 S VREFF_0 S VREFN_0			
		S VP_0 S VN_0 S VREFF_0 S VREFN_0			

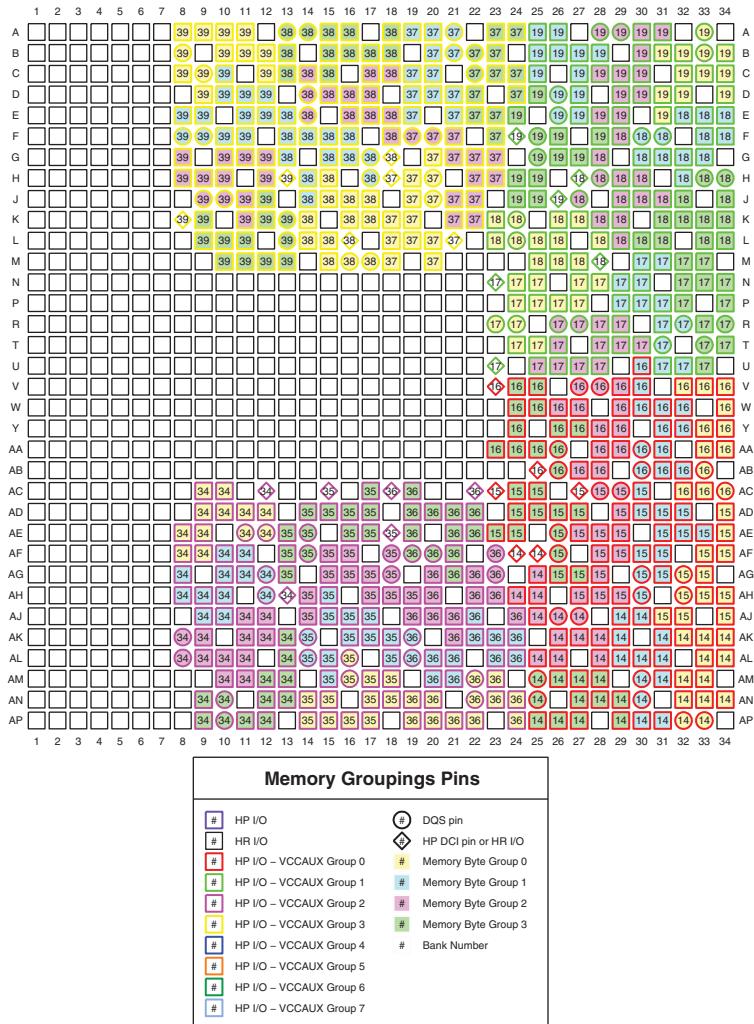
ug475_c3_085_122811

Figure 3-81: FF1157, FFG1157, and RF1157 Packages—XC7V585T Pinout Diagram



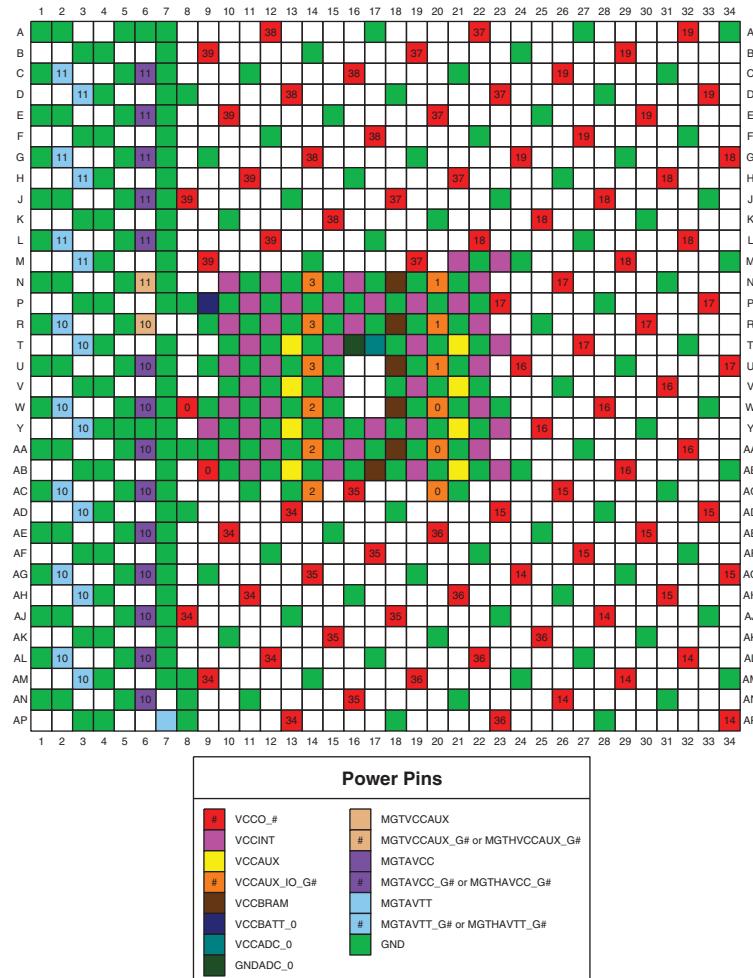
ug475_c3_086_122811

Figure 3-82: FF1157, FFG1157, and RF1157 Packages—XC7V585T I/O Banks



ug475_c3_087_013014

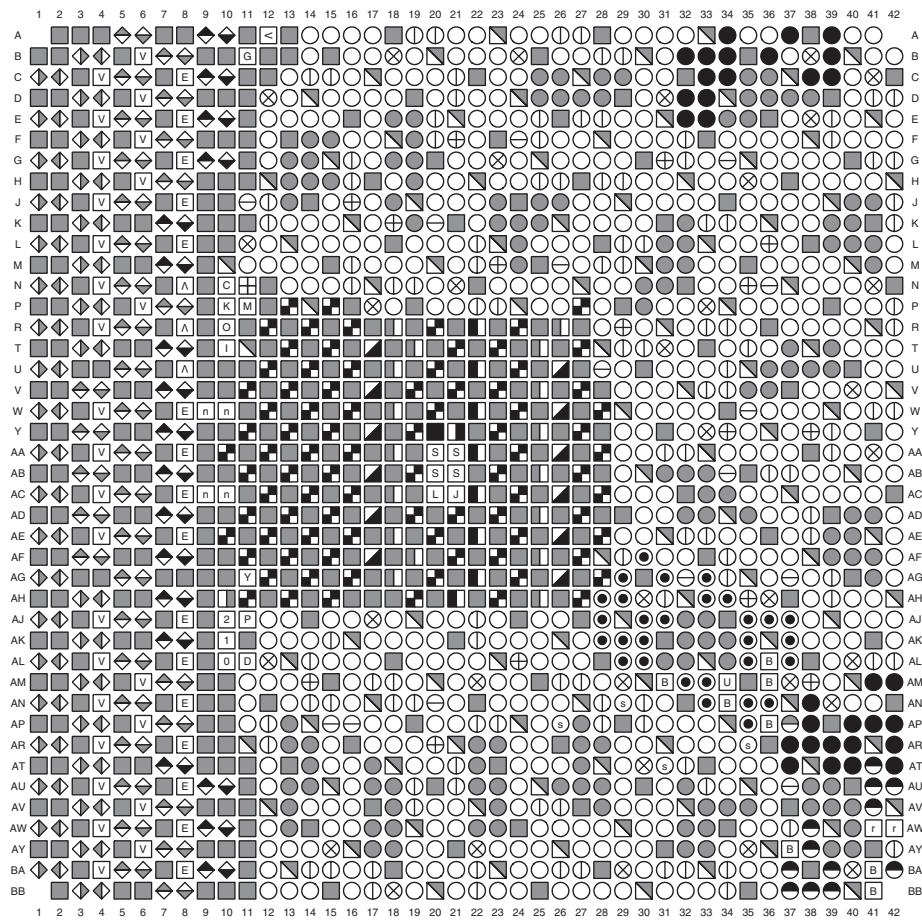
Figure 3-83: FF1157, FFG1157, and RF1157 Packages—XC7V585T Memory Groupings



ug475_c3_088_122811

Figure 3-84: FF1157, FFG1157, and RF1157 Packages—XC7V585T Power and GND Placement

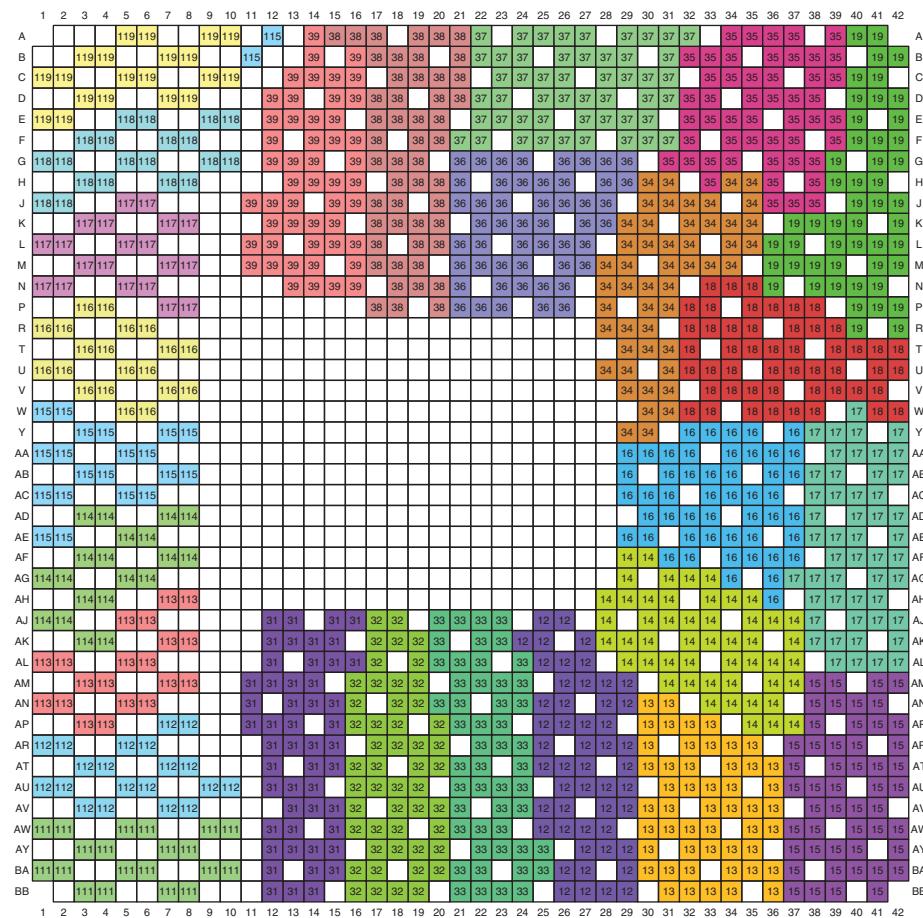
FF1761, FFG1761, and RF1761 Packages—XC7V585T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	[E] MGTAVCC_G#	[C] CCLK_0	■ GND
(S) IO_XX_#	[V] MGTAVTT_G#	[S] VP_0	□ VCCAUX_IO_G#
	[A] MGTVCAXX_G#	[D] CFGBVS_0	■ VCCAUX
	[<] MGTAVTRCAL	[D] DONE_0	□ VCCINT
	[S] MGTTRREF	[J] DXP_0	■ VCCO_#
		[L] DXN_0	□ VCCBRAM
		[■] GNDADC_0	[n] NC
		[Y] INIT_B_0	
		[0] MO_0	
		[1] M1_0	
		[2] M2_0	
		[P] PROGRAM_B_0	
		[K] TCK_0	
		[I] TDl_0	
		[O] TDO_0	
		[M] TMS_0	
		[■] VCCADC_0	
		[□] VCCBATT_0	

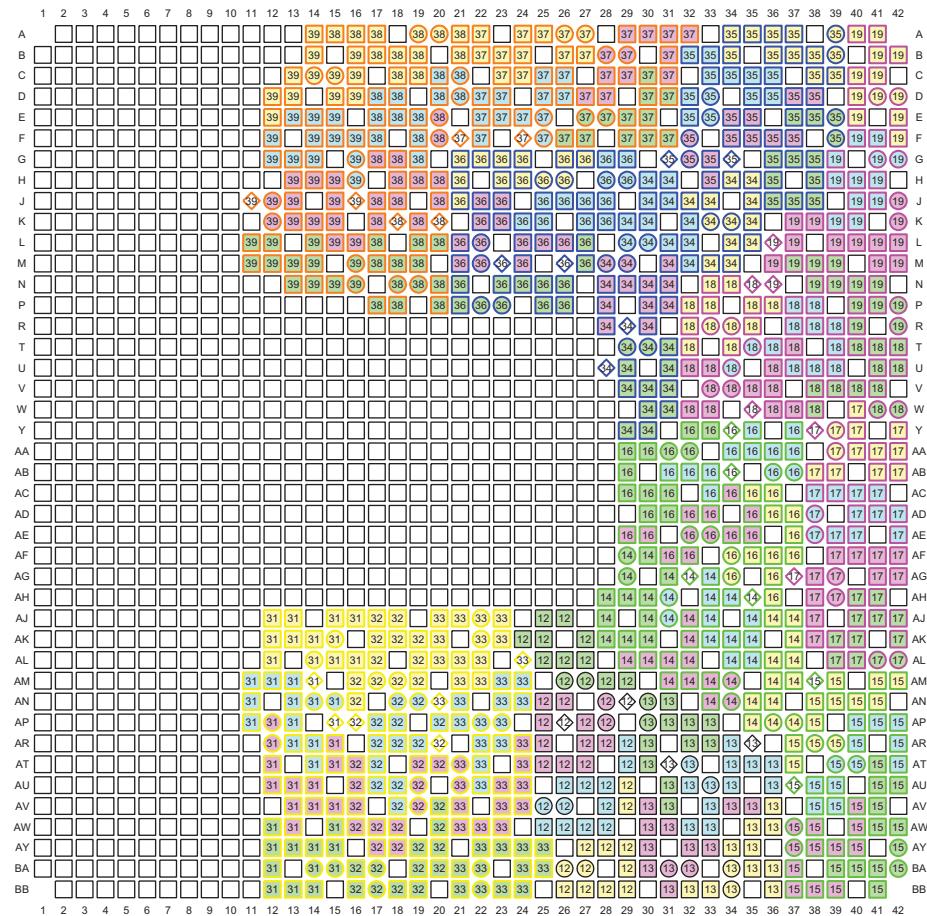
ug475_c3_089_070512

Figure 3-85: FF1761, FFG1761, and RF1761 Packages—XC7V585T Pinout Diagram



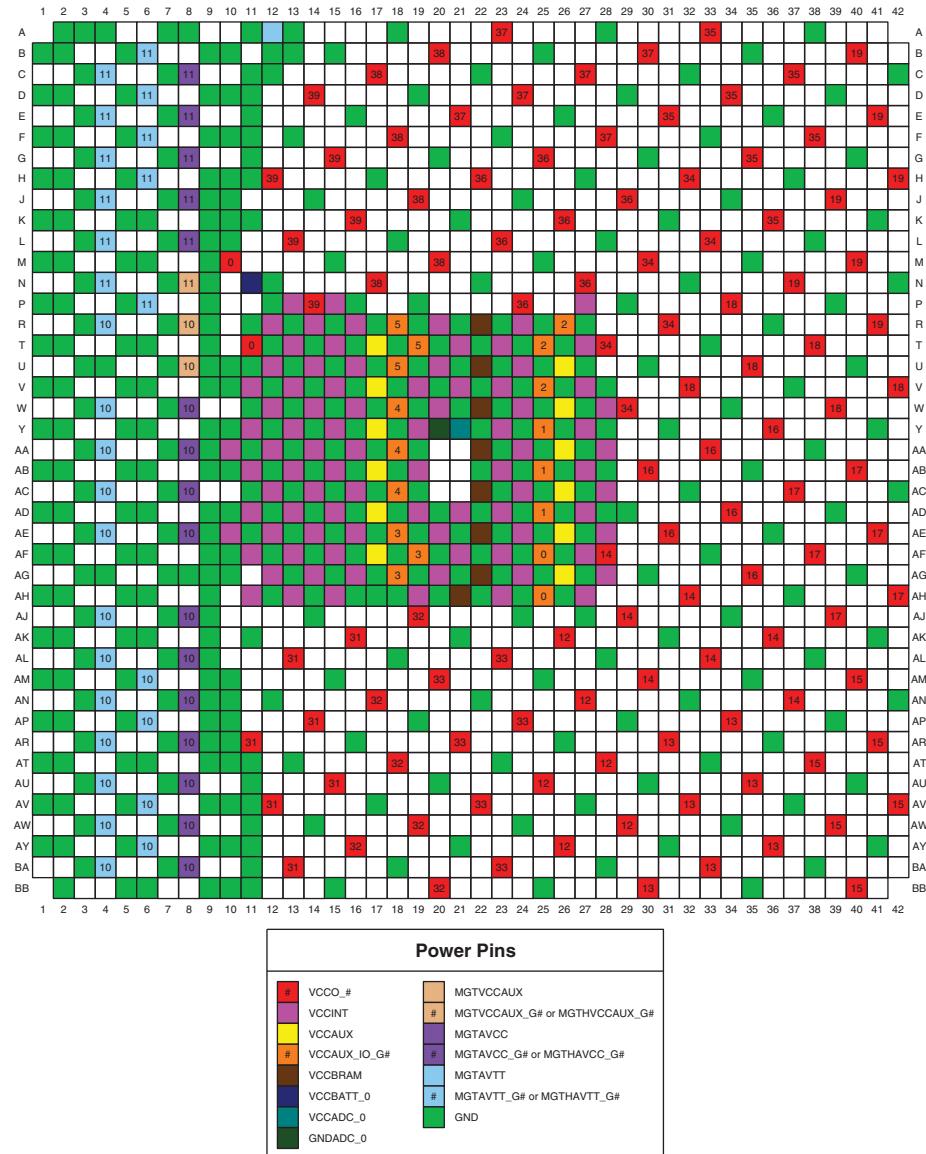
ug475_c3_090_122811

Figure 3-86: FF1761, FFG1761, and RF1761 Packages—XC7V585T I/O Banks



ug475_c3_091_013014

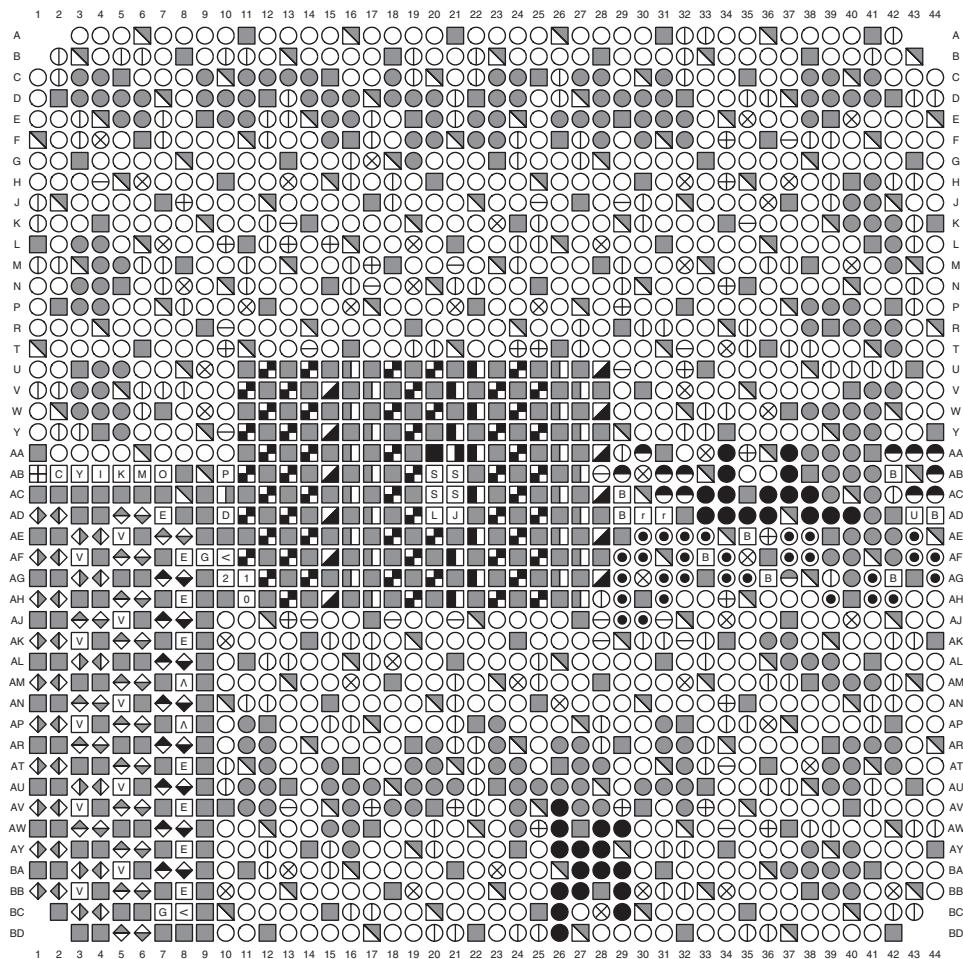
Figure 3-87: FF1761, FFG1761, and RF1761 Packages—XC7V585T Memory Groupings



ug475_c3_092_070512

Figure 3-88: FF1761, FFG1761, and RF1761 Packages—XC7V585T Power and GND Placement

FL1925 and FLG1925 Packages—XC7V2000T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins	
○ IO_LXXY_# ○ IO_XX_#				
Multi-Function Pins				
B ADV_B B FCS_B B FOE_B B MOSI B FWE_B B DOUT_CS0_B B CSL_B B PUDC_B U RDWR_B r RS0-RS1 ● ADOP/ADON-AD15P/AD15N ○ EMCCLK	⊕ VRN ○ VRP ⊗ VREF ● D00-D31 ● A00-A28 ○ DQS ● MRCC ● SRCC	E MGTAVCC_G# V MGTVTT_G# A MGTVCCAUX_G# L MGTAVTRCAL G MGTRREF △ MGTRCLK1/0P ◆ MGTRCLK1/0N △ MGTXXP ◆ MGTXRXN △ MGTXXP ◆ MGTXTN E MGTHAVCC_G# V MGTHAVTT_G# △ MGTHRXP ◆ MGTHRXXN △ MGHTXP ◆ MGHTXN	C CCLK_0 I CFGBVS_0 A MGTVCCAUX_G# D DONE_0 J DXP_0 L DXN_0 Y INIT_B_0 O M0_0 1 M1_0 2 M2_0 P PROGRAM_B_0 K TCK_0 I TDI_0 O TDO_0 M TMS_0 ■ VCCADC H VCCBATT_0	GND VCCAUX_IO_G# VCCAUX VCCINT VCCO_# VCCBRAM n NC

ug475_c3_097_101413

Figure 3-89: FL1925 and FLG1925 Packages—XC7V2000T Pinout Diagram

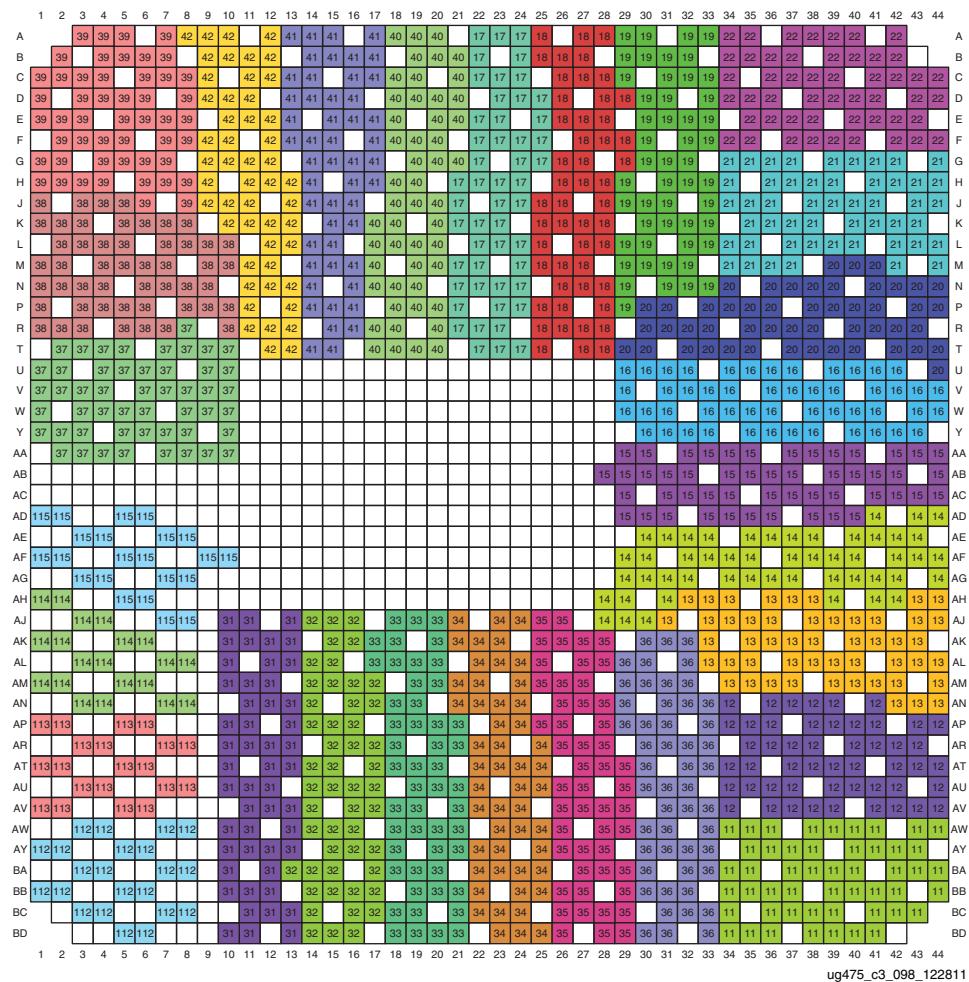


Figure 3-90: FL1925 and FLG1925 Packages—XC7V2000T I/O Banks

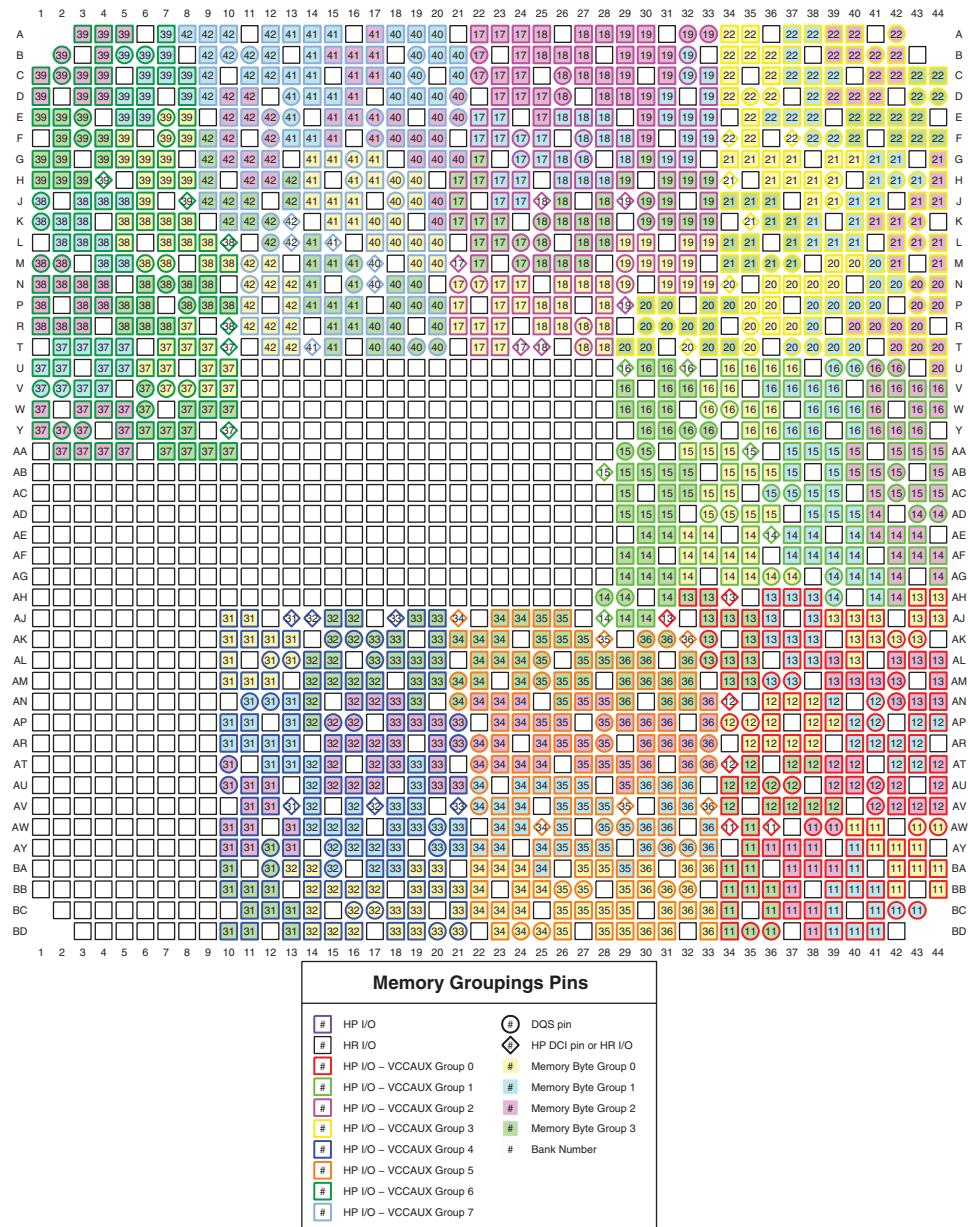
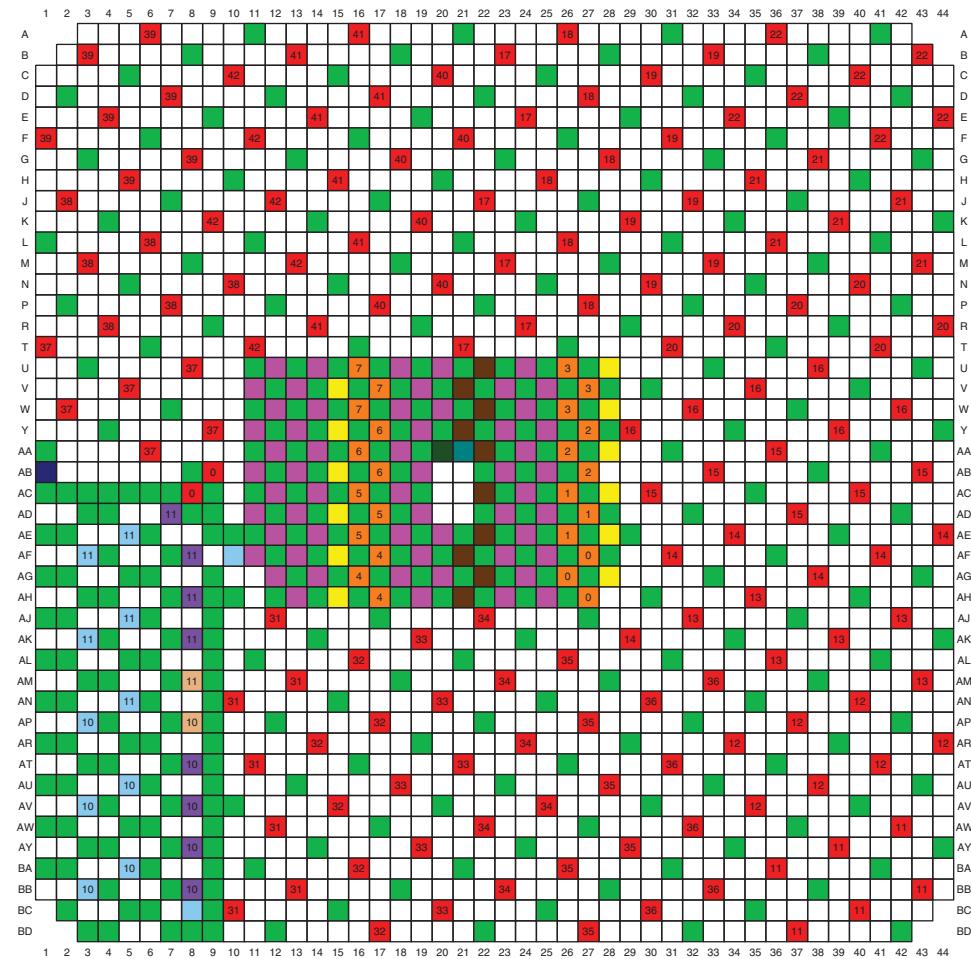


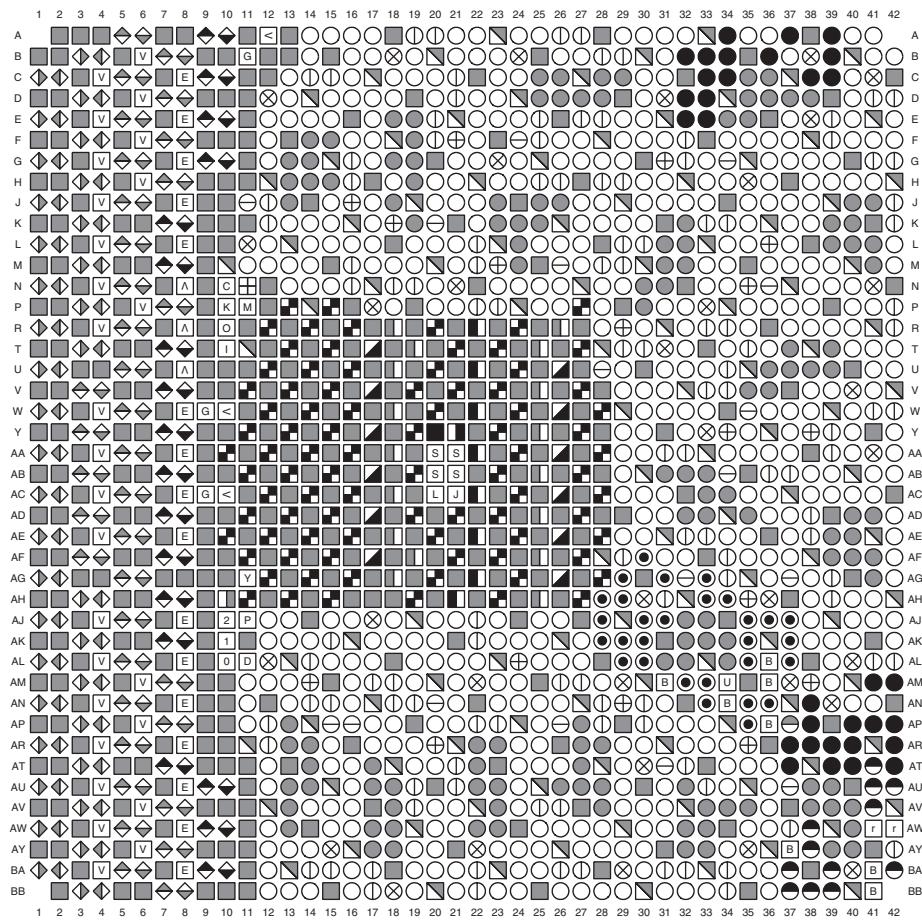
Figure 3-91: FL1925 and FLG1925 Packages—XC7V2000T Memory Groupings



ug475_c3_100_101413

Figure 3-92: FL1925 and FLG1925 Packages—XC7V2000T Power and GND Placement

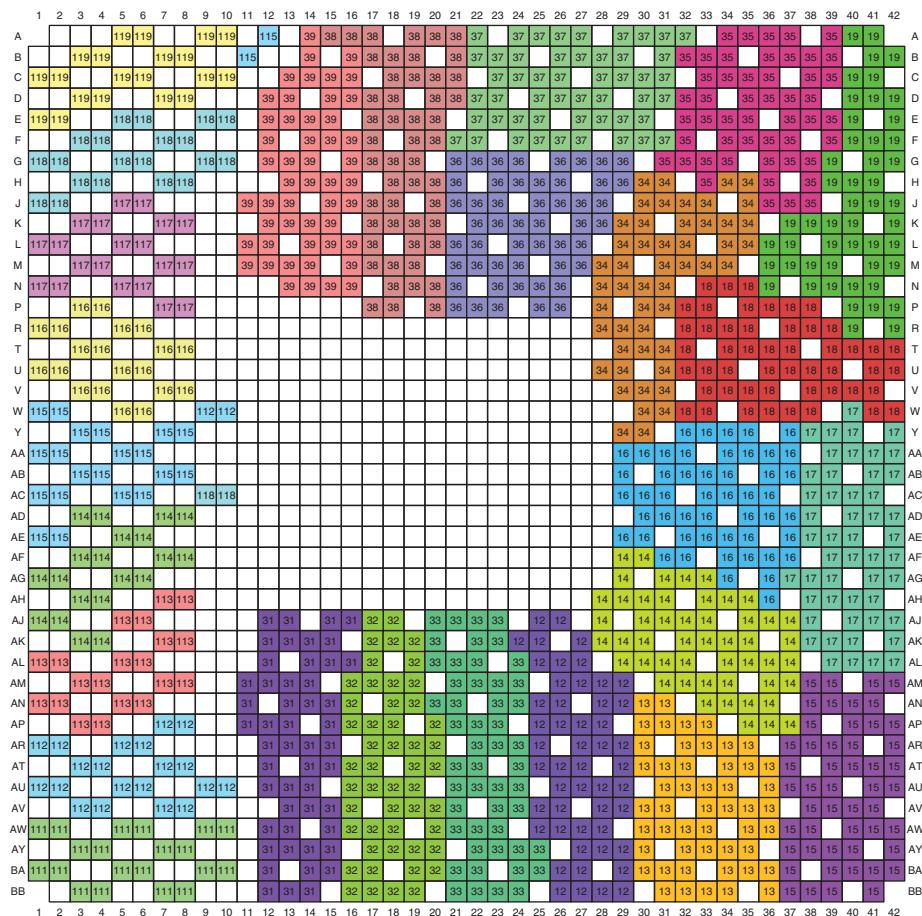
FH1761 and FHG1761 Packages—XC7V2000T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_# ○ IO_XX_#	[E] MGTAVCC_G# [V] MGTAVTT_G# [A] MGTVCAXX_G# [L] MGTAVTRCAL [G] MGTRREF	[C] CCLK_0 [I] CFGBVS_0 [D] DONE_0 [J] DXP_0 [L] DXN_0 [Y] MGTRREFCLK1/0P [D] MGTRREFCLK1/0N [M] MGTXRXP [F] MGTXRXN [E] MGTXTXP [V] MGTXTXN [W] MGTHAVCC_G# [U] MGTHAVTT_G# [R] MGTHRXP [S] MGTHRXN [T] MGHTXP [B] MGHTXN	[S] VP_0 [S] VN_0 [S] VREFP_0 [S] VREFN_0 [GNDADC] [INIT_B_0] [M0_0] [M1_0] [M2_0] [PROGRAM_B_0] [TCK_0] [TDI_0] [TDO_0] [TMS_0] [VCCADC] [VCCBATT_0]
Multi-Function Pins			GND VCCAUX_IO_G# VCCAUX VCCINT VCCO # VCCBRAM NC
B ADV_B B FCS_B B FOE_B B MOSI B FWE_B B DOUT_CSO_B B CSI_B B PUDC_B U RDWR_B F RSO-RS1 ● ADOP/ADON-AD15P/AD15N ○ EMCCLK	⊕ VRN ○ VRP ⊗ VREF ● D00-D31 ● A00-A28 ○ DQS ○ MRCC ● SRCC		

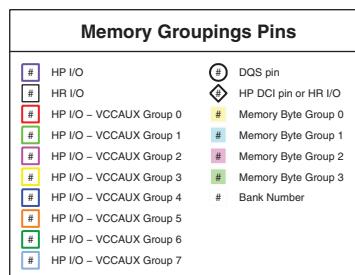
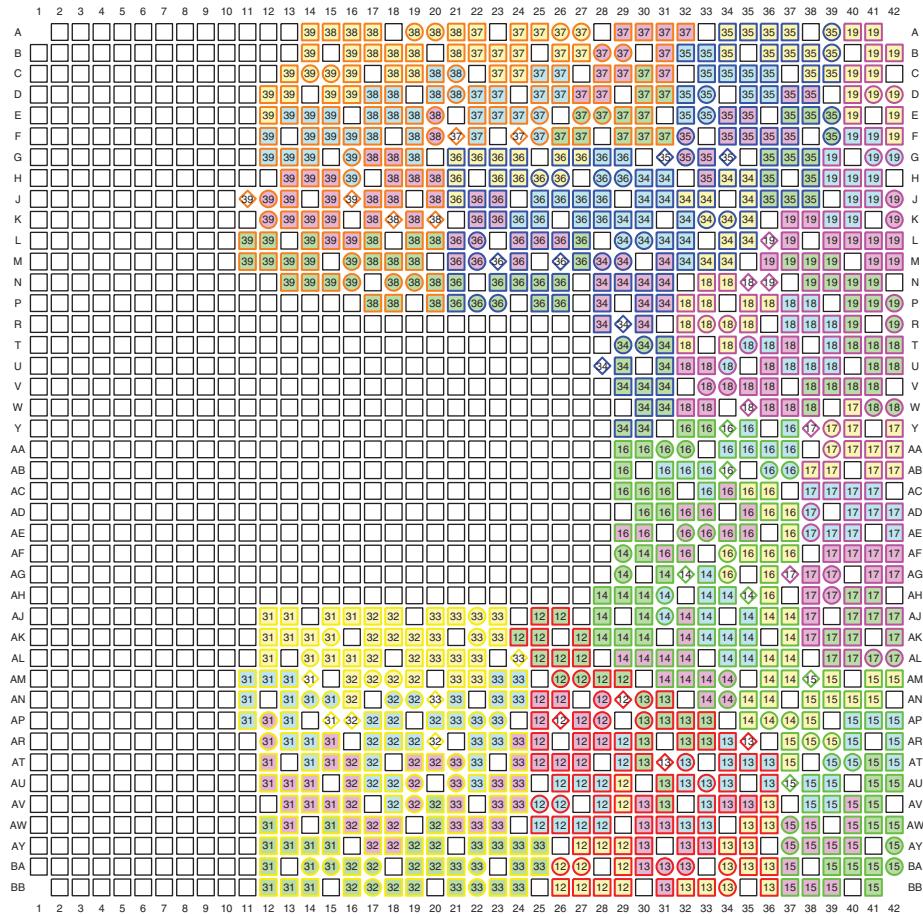
ug475_c3_101_101413

Figure 3-93: FH1761 and FHG1761 Packages—XC7V2000T Pinout Diagram



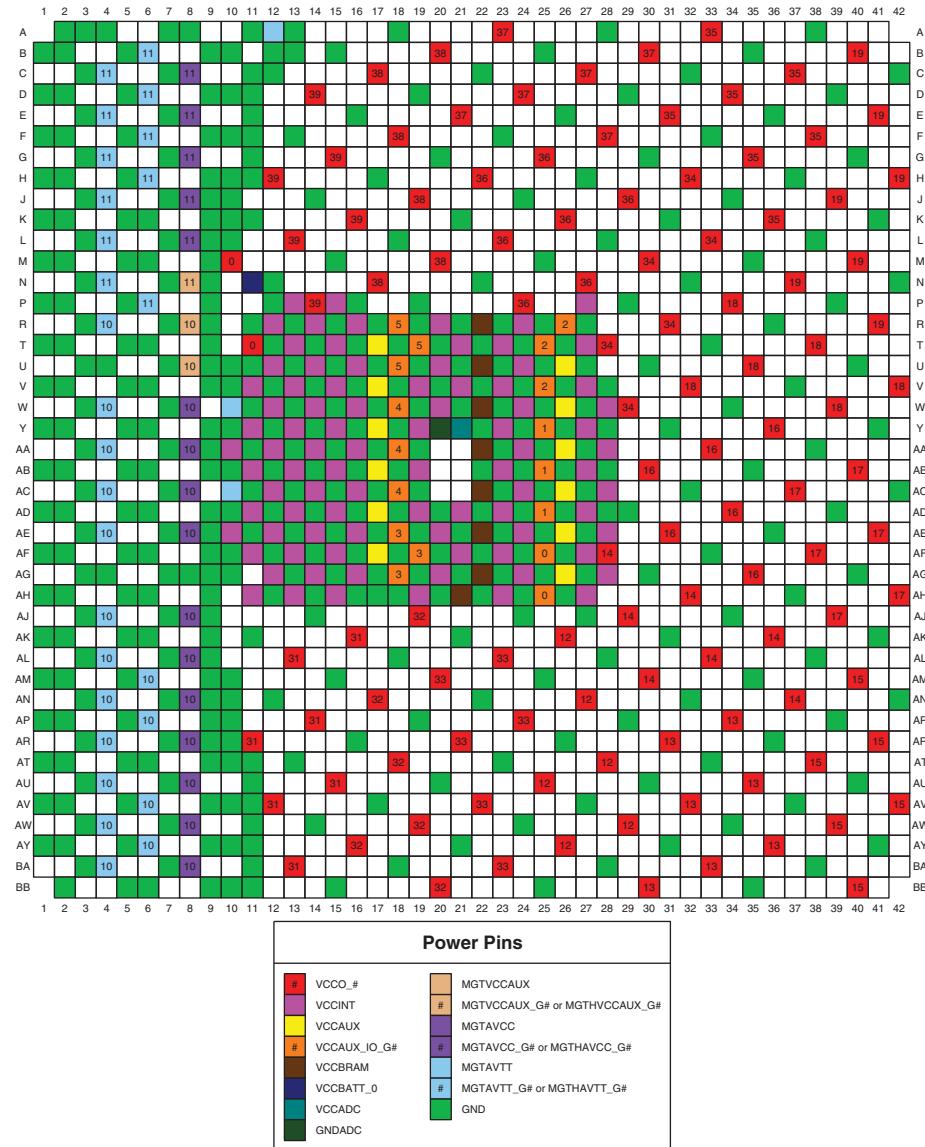
ug475_c3_205_052311

Figure 3-94: FH1761 and FHG1761 Packages—XC7V2000T I/O Banks



ug475_c3_103_013014

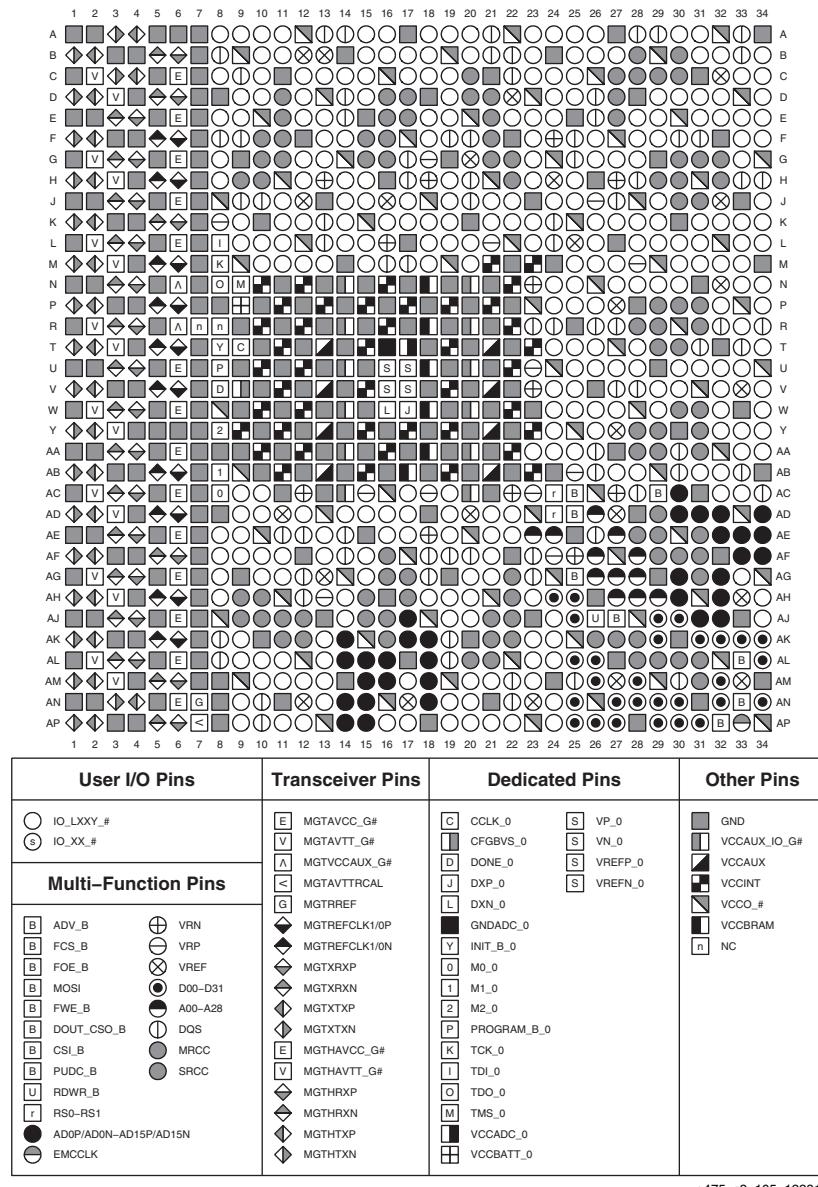
Figure 3-95: FH1761 and FHG1761 Packages—XC7V2000T Memory Groupings



ug475_c3_104_101413

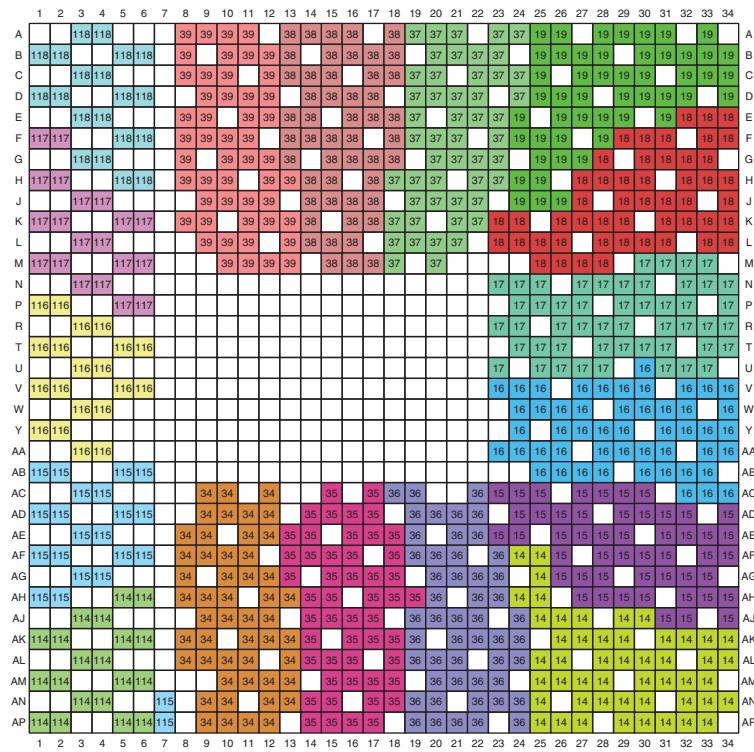
Figure 3-96: FH1761 and FHG1761 Packages—XC7V2000T Power and GND Placement

FF1157, FFG1157, FFV1157, and RF1157 Packages—XC7VX330T, XC7VX415T, and XC7VX690T



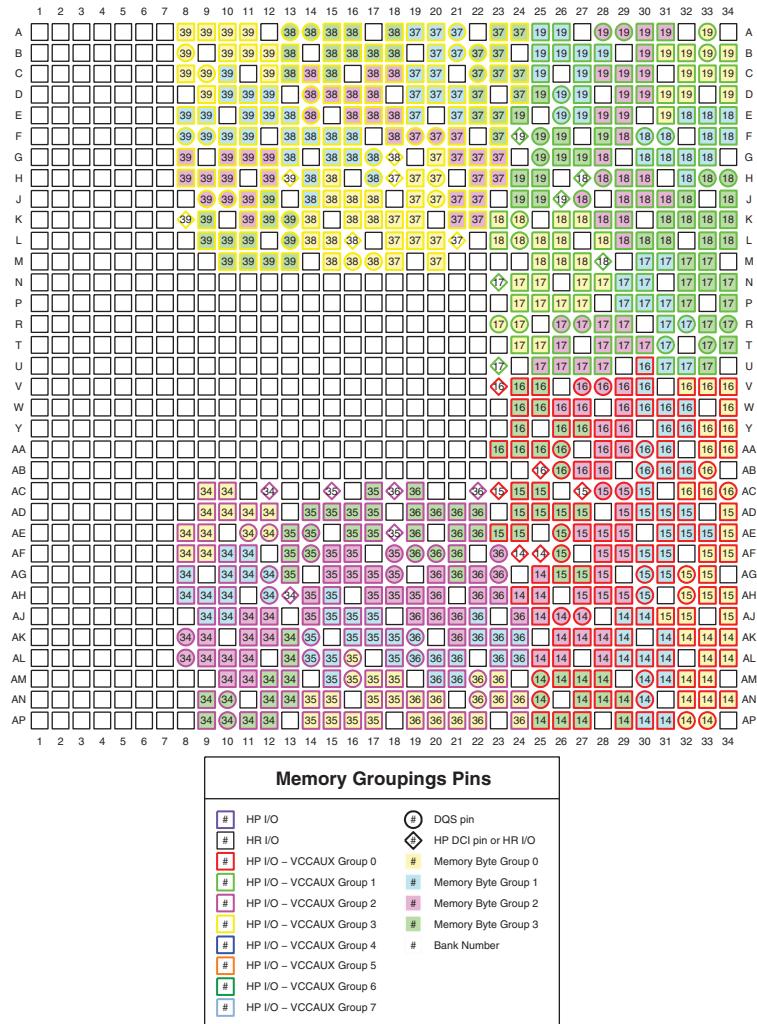
ug475_c3_105_122811

Figure 3-97: FF1157, FFG1157, FFV1157, and RF1157 Packages—XC7VX330T, XC7VX415T, and XC7VX690T Pinout Diagram



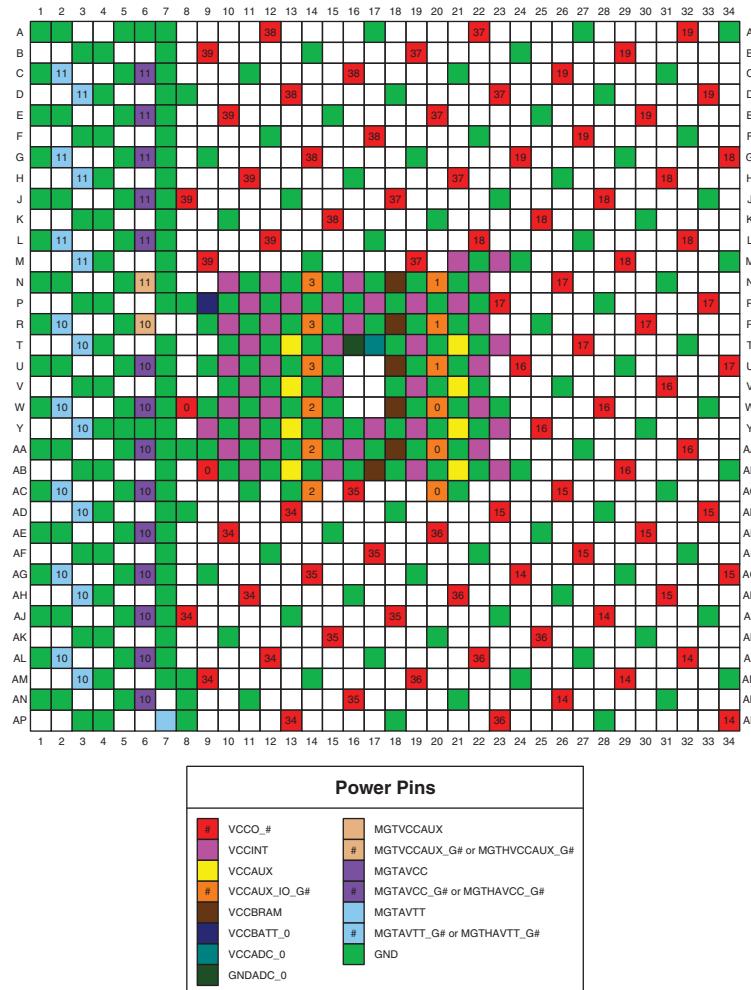
ug475_c3_106_122811

Figure 3-98: FF1157, FFG1157, FFV1157, and RF1157 Packages—XC7VX330T, XC7VX415T, and XC7VX690T I/O Banks



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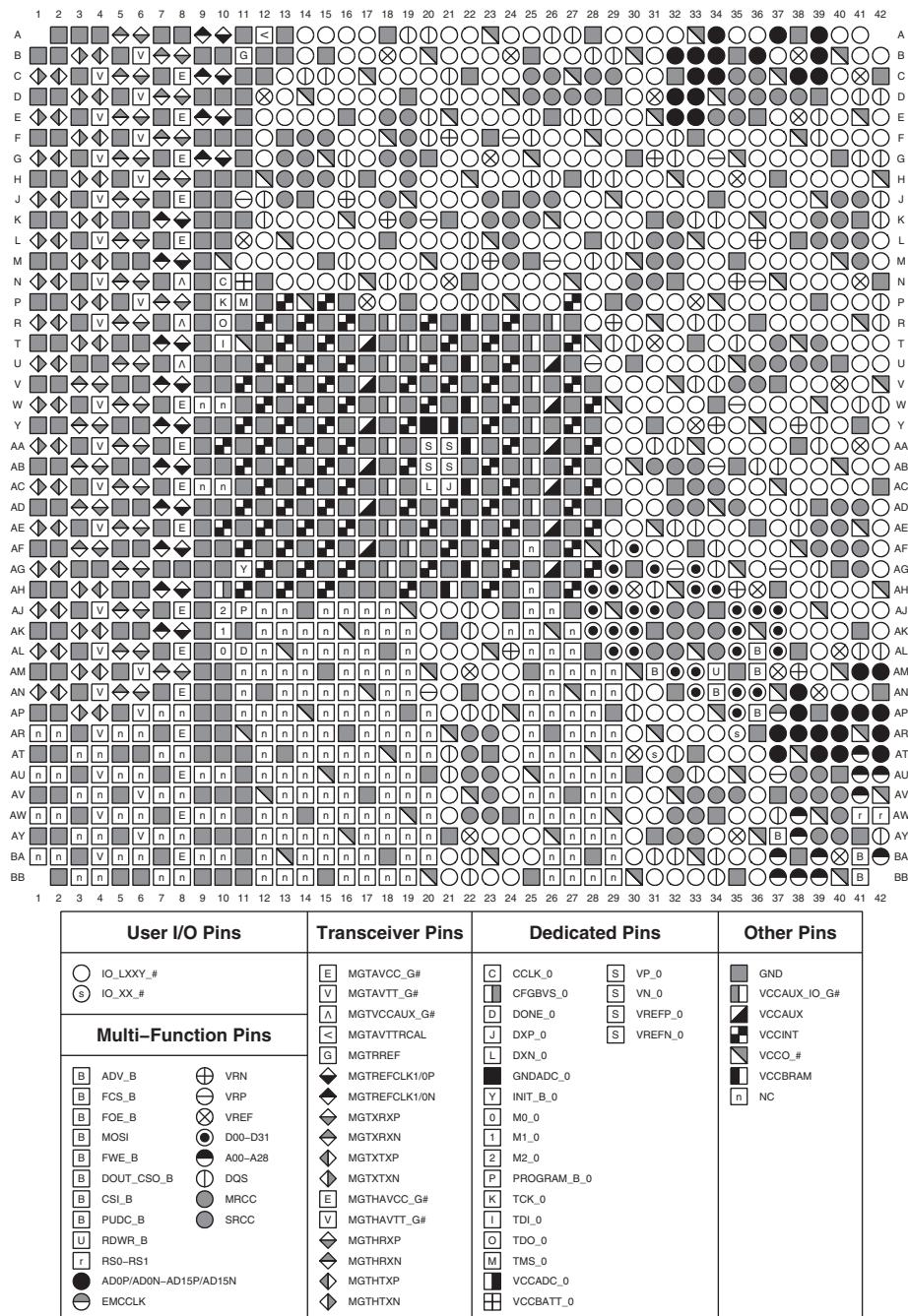
Figure 3-99: FF1157, FFG1157, FFV1157, and RF1157 Packages—XC7VX330T, XC7VX415T, and XC7VX690T Memory Groupings



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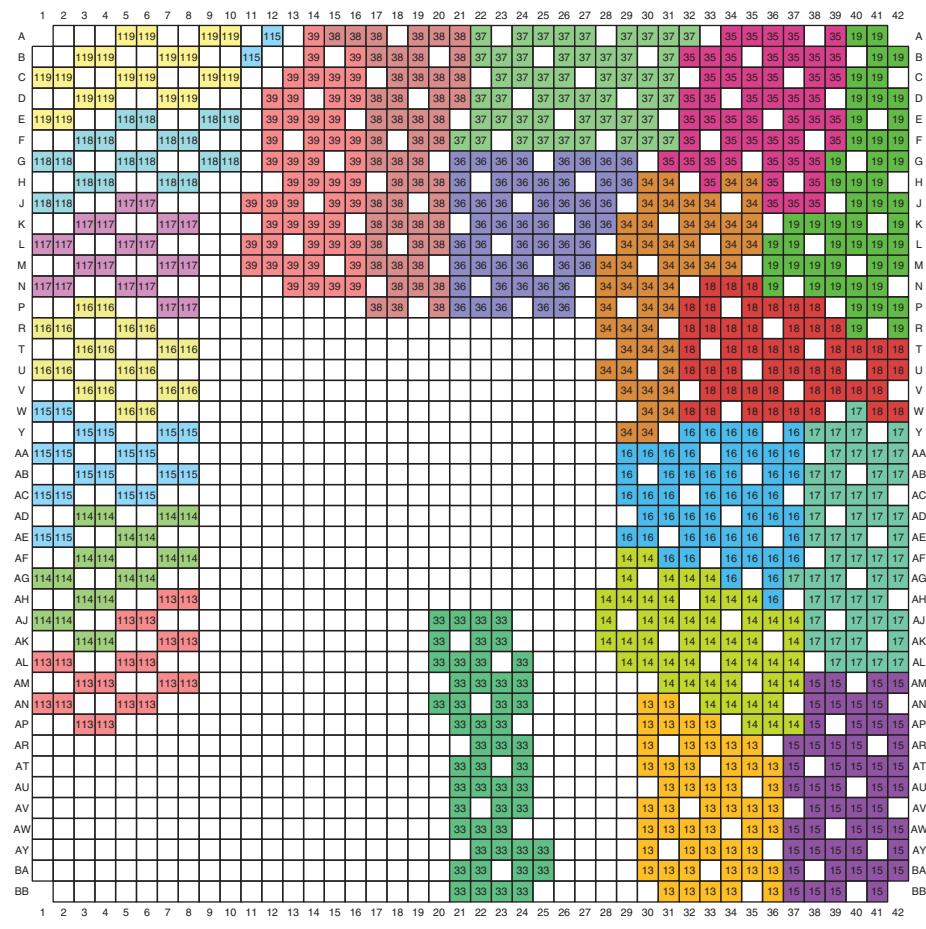
Figure 3-100: FF1157, FFG1157, FFV1157, and RF1157 Packages—XC7VX330T, XC7VX415T, and XC7VX690T Power and GND Placement

FF1761, FFG1761, FFV1761, and RF1761 Packages—XC7VX330T



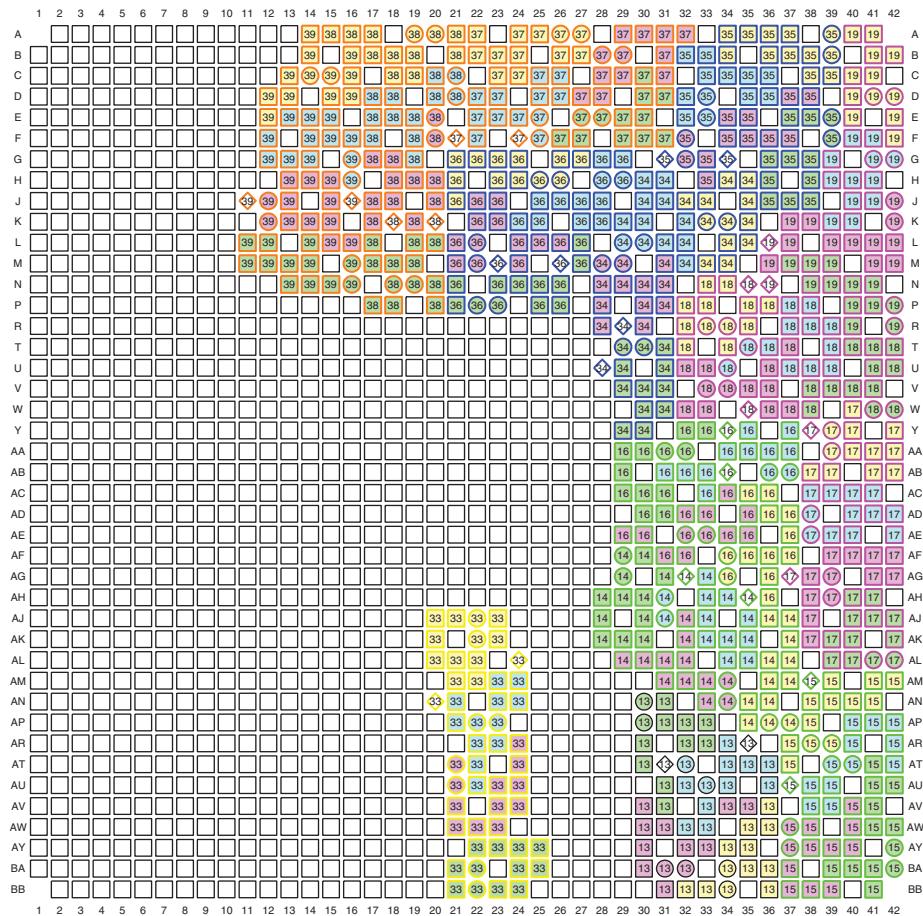
ug475_c3_109_122811

Figure 3-101: FF1761, FFG1761, FFV1761, and RF1761 Packages—XC7VX330T Pinout Diagram



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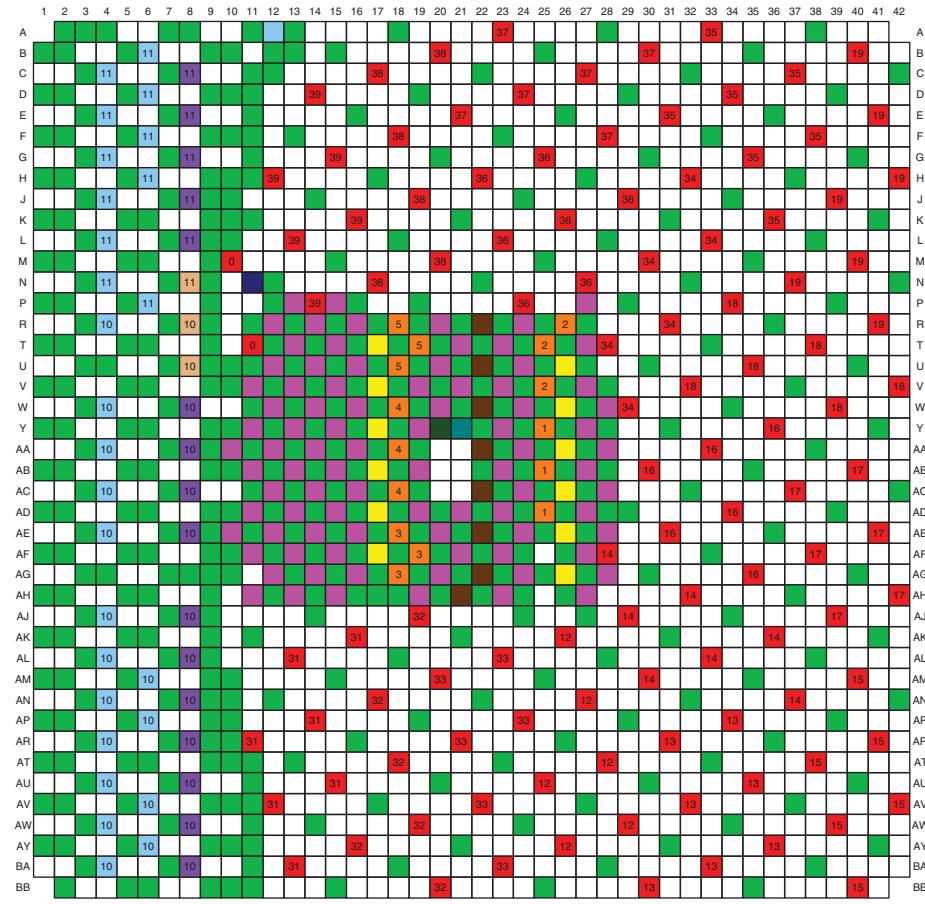
Figure 3-102: FF1761, FFG1761, FFV1761, and RF1761 Packages—XC7VX330T I/O Banks



Memory Groupings Pins	
# HP I/O	# DQS pin
# HR I/O	# HP DCI pin or HR I/O
# HP I/O - VCCAUX Group 0	# Memory Byte Group 0
# HP I/O - VCCAUX Group 1	# Memory Byte Group 1
# HP I/O - VCCAUX Group 2	# Memory Byte Group 2
# HP I/O - VCCAUX Group 3	# Memory Byte Group 3
# HP I/O - VCCAUX Group 4	# Bank Number
# HP I/O - VCCAUX Group 5	
# HP I/O - VCCAUX Group 6	
# HP I/O - VCCAUX Group 7	

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Figure 3-103: FF1761, FFG1761, FFV1761, and RF1761 Packages—XC7VX330T Memory Groupings

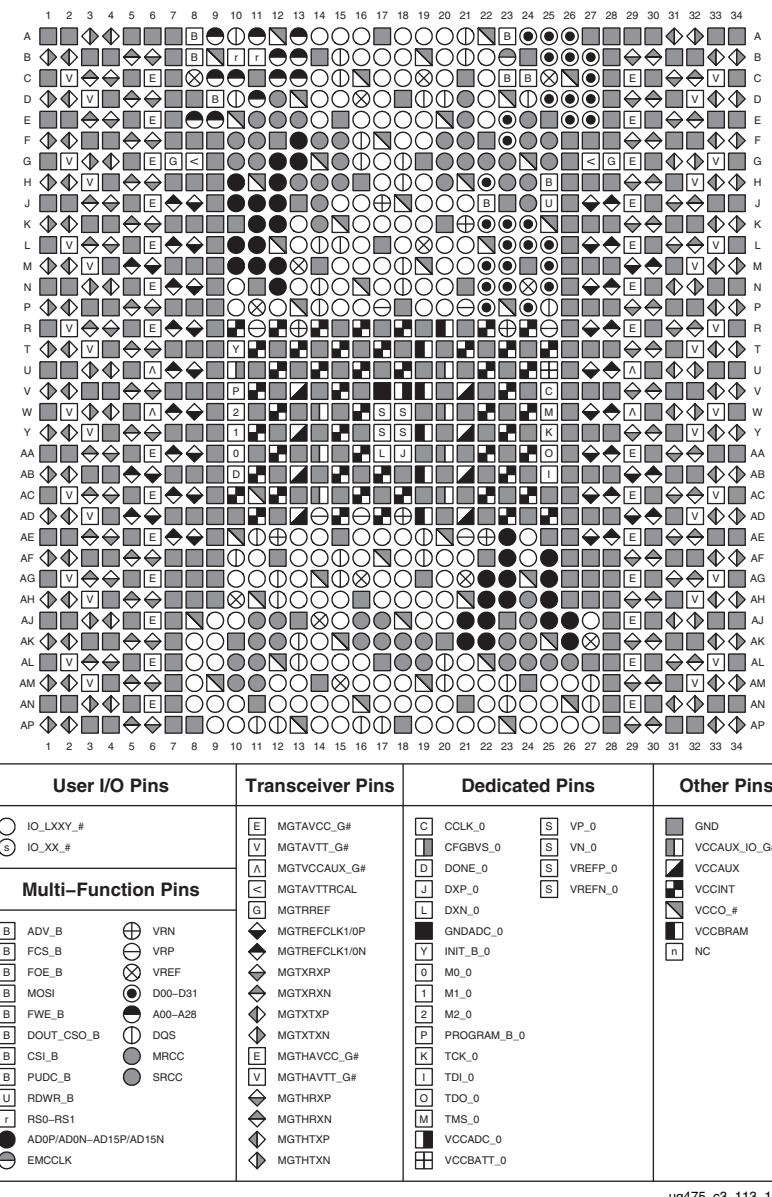


Power Pins	
#	VCCO_#
#	VCCINT
Yellow	VCCAUX
Orange	VCCAUX_IO_G#
Blue	VCCBRAM
Teal	VCCBATT_0
Cyan	VCCADC_0
Dark Green	GNDADC_0
Light Orange	MGTVCVCAUX
Light Purple	MGTVCVCAUX_G# or MGTHVCCAU_X_G#
Purple	MGTAVCC
Light Blue	MGTAVCC_G# or MGTHAVCC_G#
Light Teal	MGTAVTT
Light Cyan	MGTAVTT_G# or MGTHAVTT_G#
Dark Green	GND

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Figure 3-104: FF1761, FFG1761, FFV1761, and RF1761 Packages—XC7VX330T Power and GND Placement

FF1158, FFG1158, FFV1158, and RF1158 Packages—XC7VX415T, XC7VX550T, and XC7VX690T



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Figure 3-105: FF1158, FFG1158, FFV1158, and RF1158 Packages—XC7VX415T, XC7VX550T, and XC7VX690T Pinout Diagram

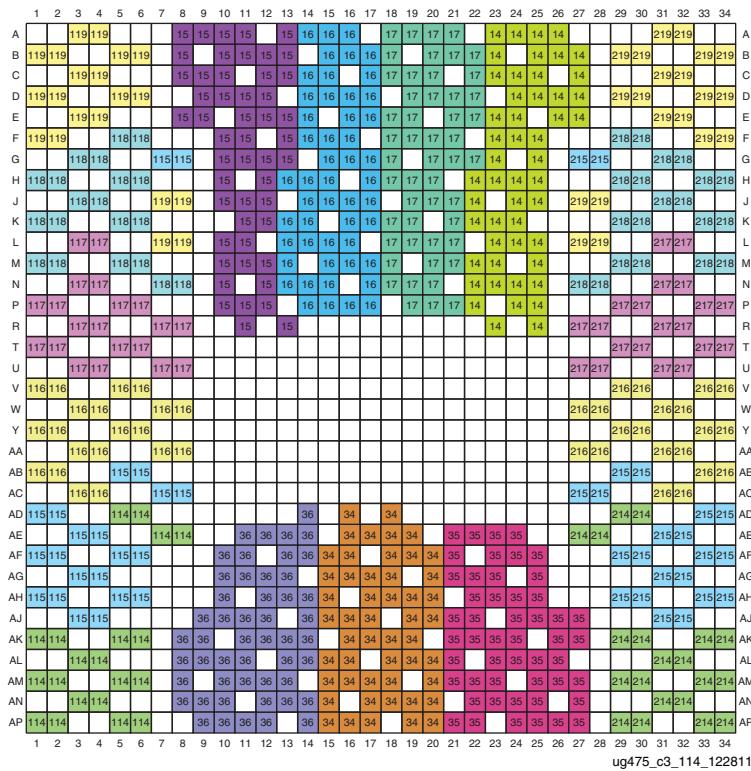
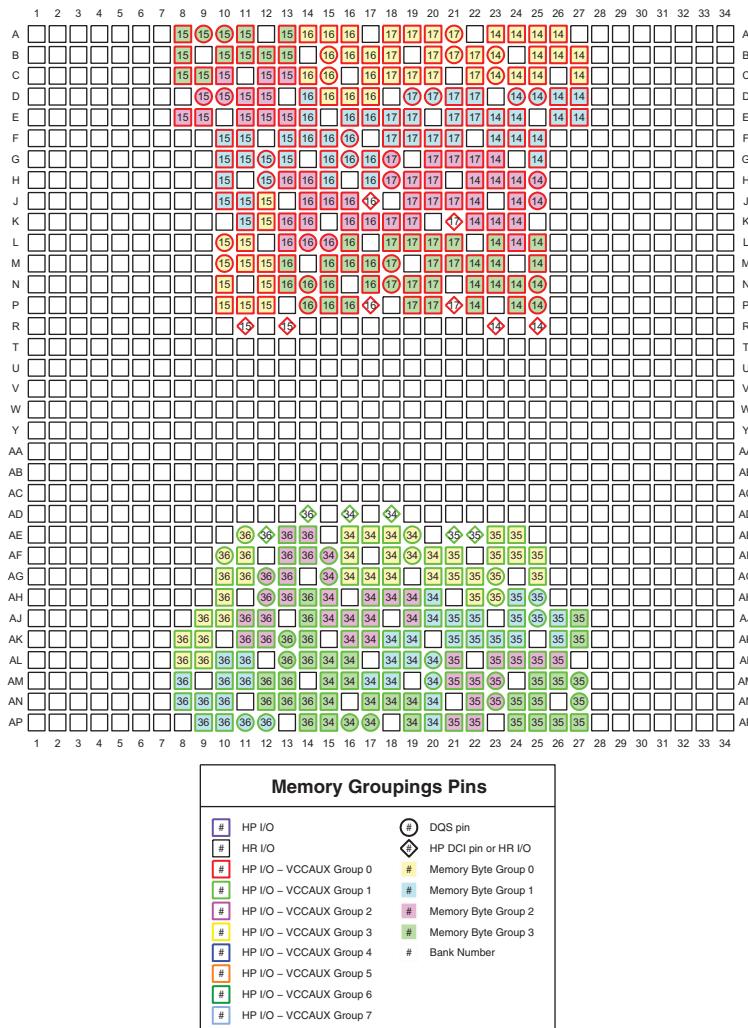
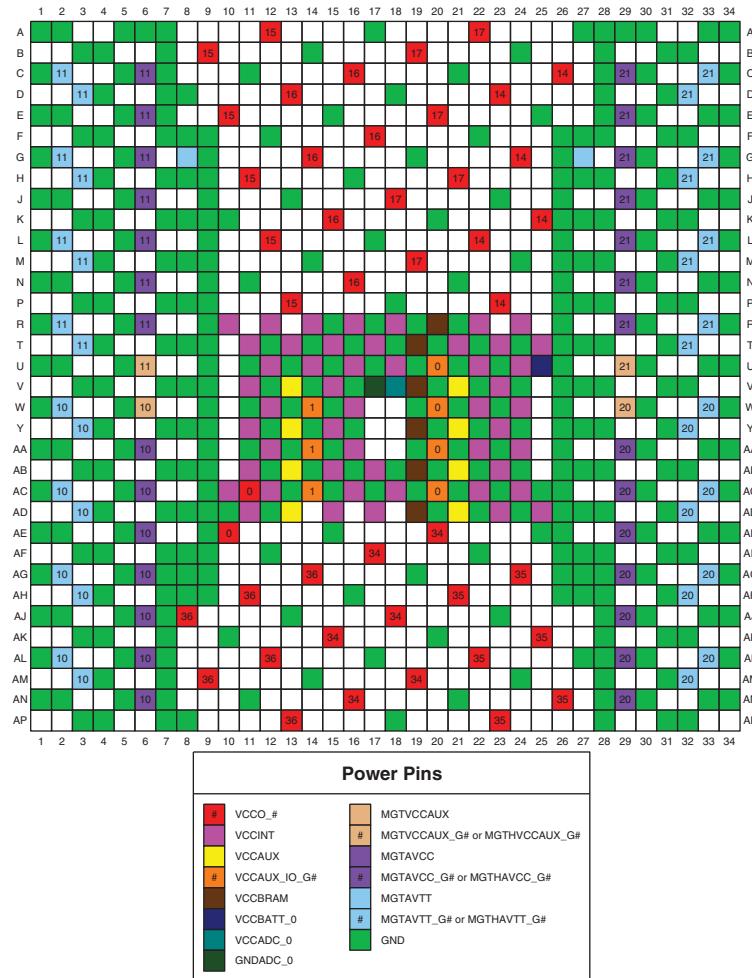


Figure 3-106: FF1158, FFG1158, FFV1158, and RF1158 Packages—XC7VX415T, XC7VX550T, and XC7VX690T I/O Banks



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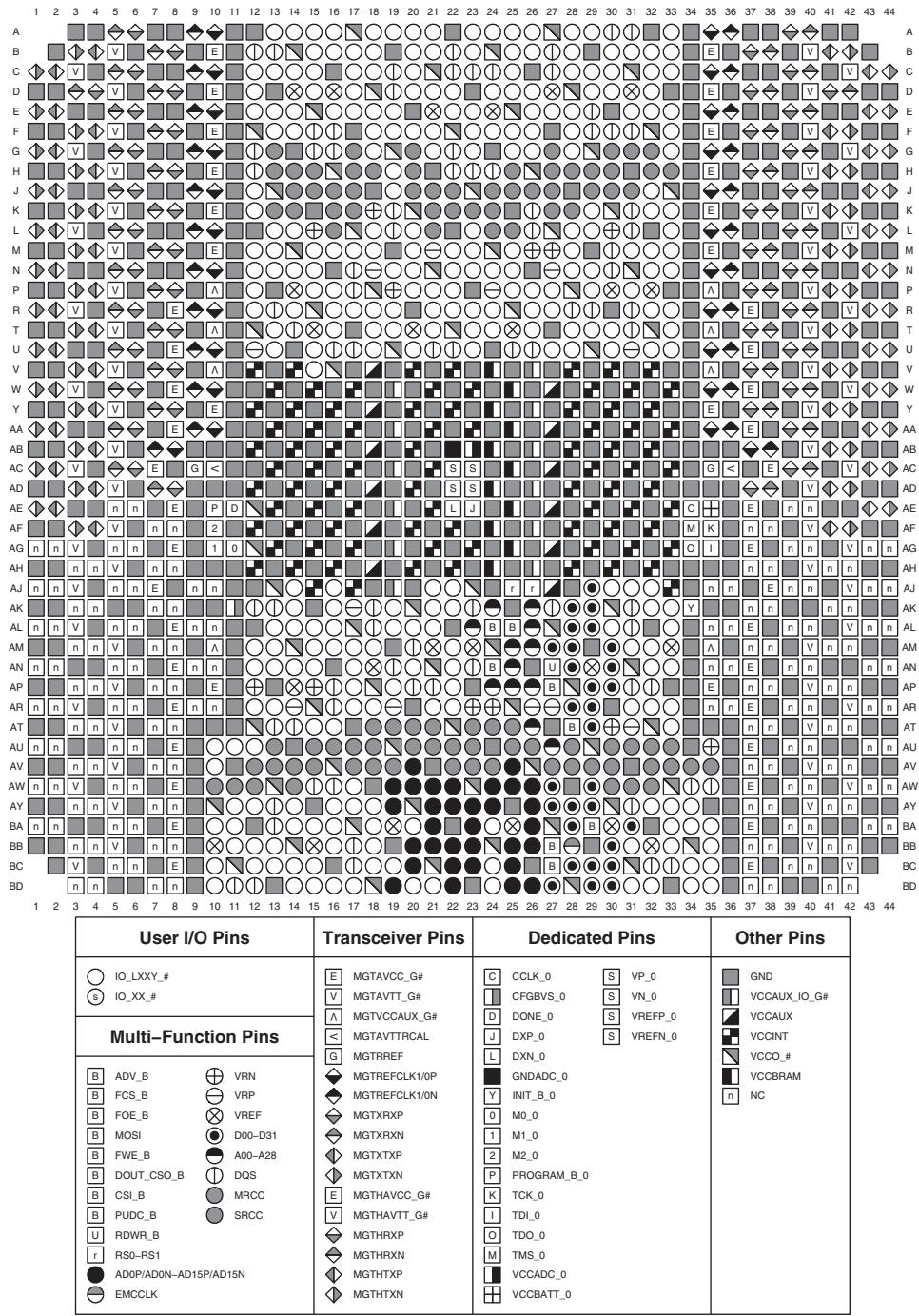
Figure 3-107: FF1158, FFG1158, FFV1158, and RF1158 Packages—XC7VX415T, XC7VX550T, and XC7VX690T Memory Groupings



ug475_c3_116_122811

Figure 3-108: FF1158, FFG1158, FFV1158, and RF1158 Packages—XC7VX415T, XC7VX550T, and XC7VX690T Power and GND Placement

FF1927, FFG1927, and FFV1927 Packages—XC7VX415T



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Figure 3-109: FF1927, FFG1927, and FFV1927 Packages—XC7VX415T Pinout Diagram

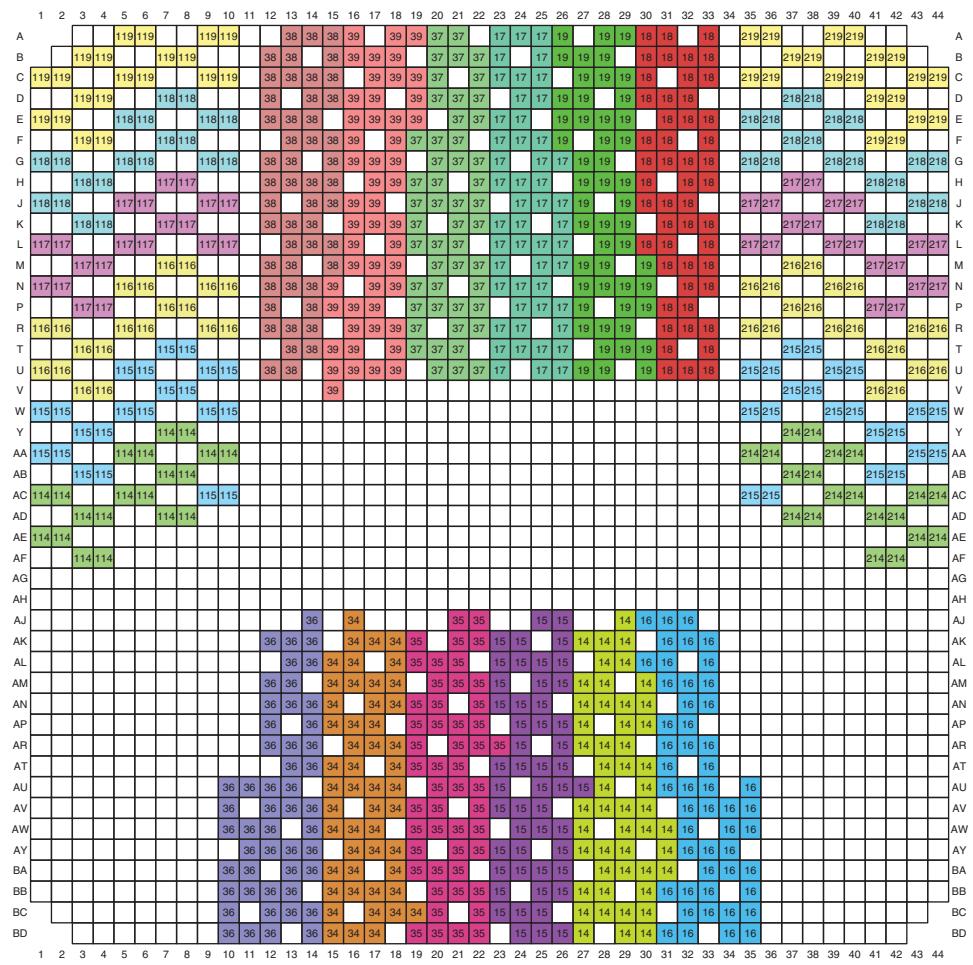
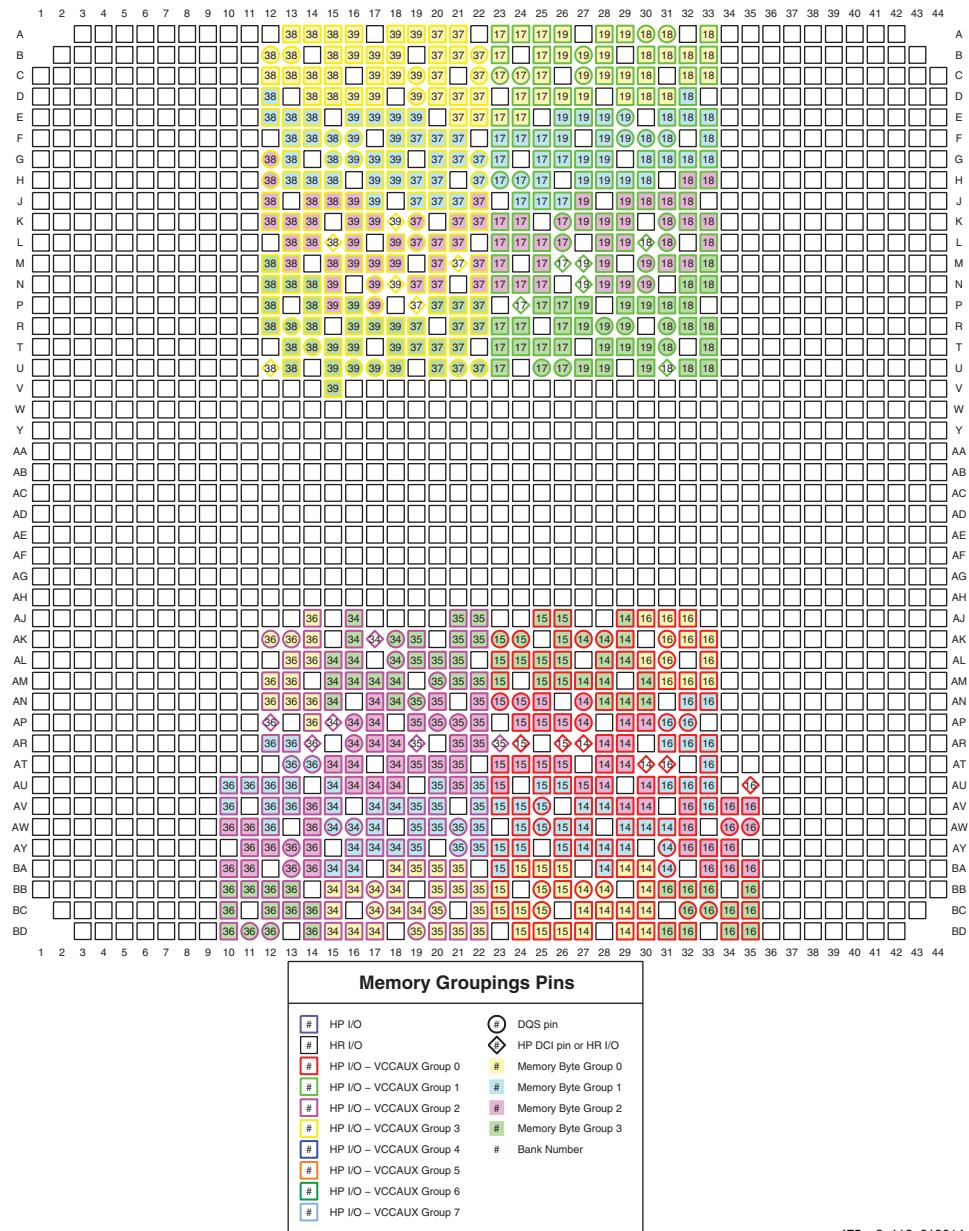
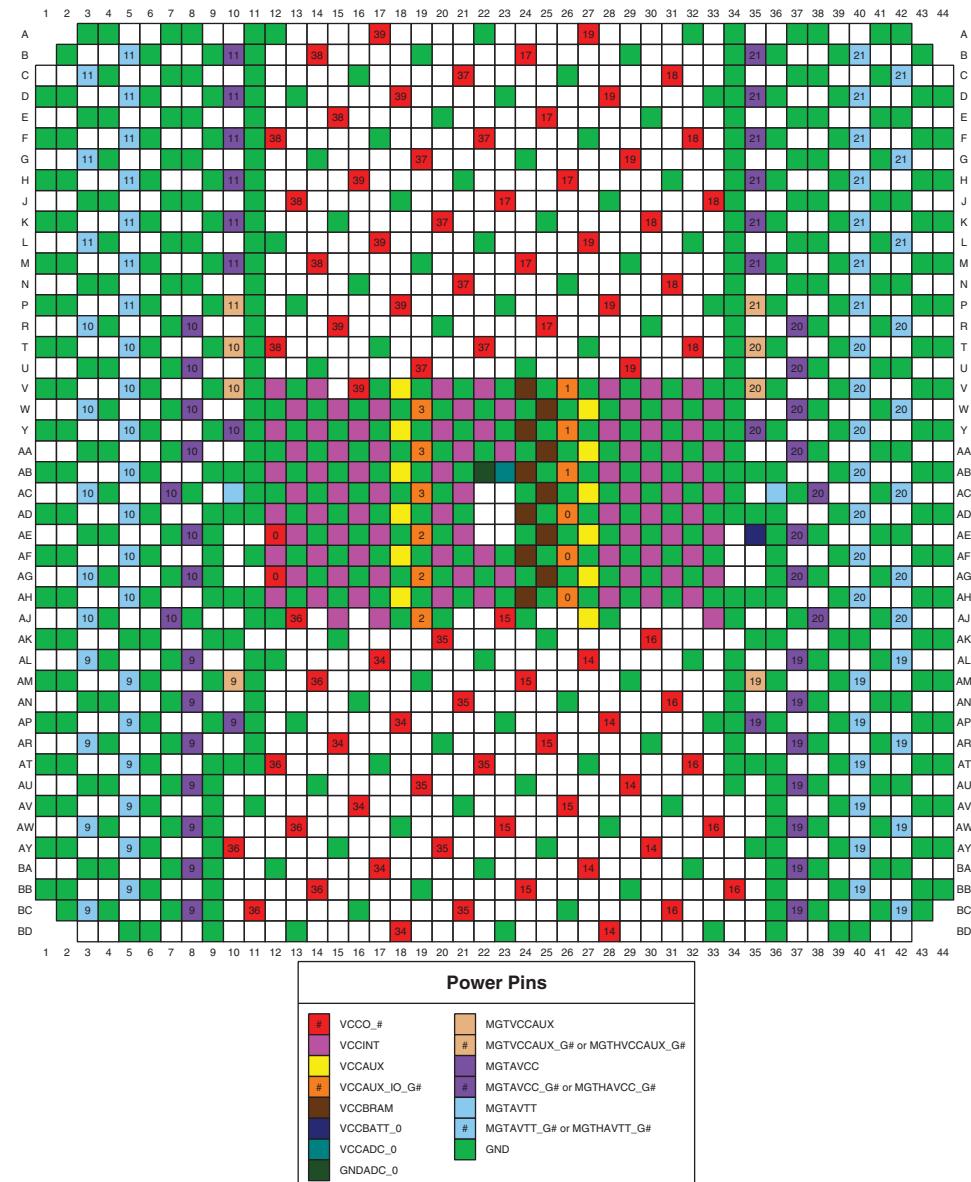


Figure 2-110: EE1007, EEC1007, and EEV1007 Packages – XQZVX41ET I/O Banks



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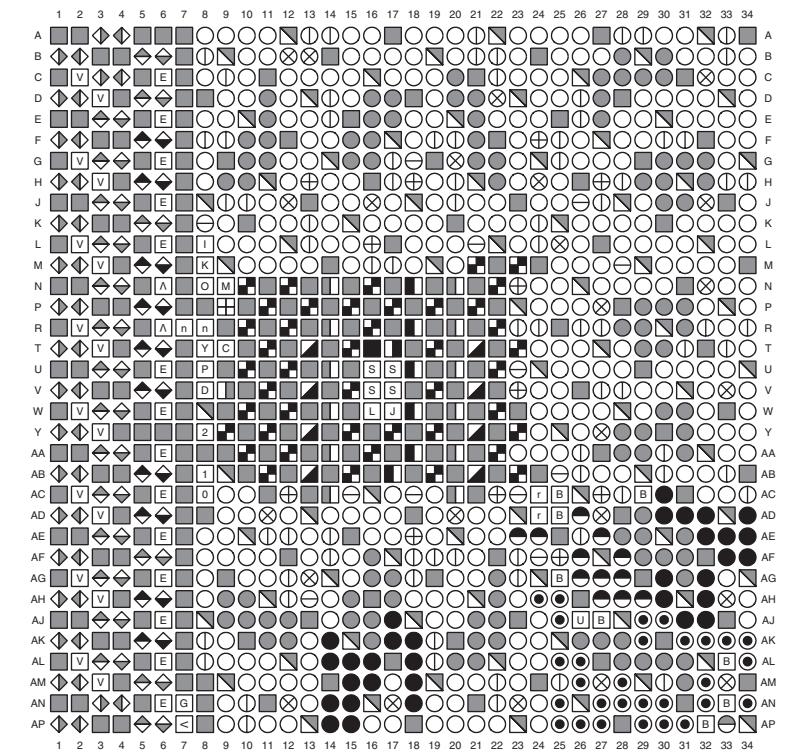
Figure 3-111: FF1927, FFG1927, and FFV1927 Packages—XC7VX415T Memory Groupings



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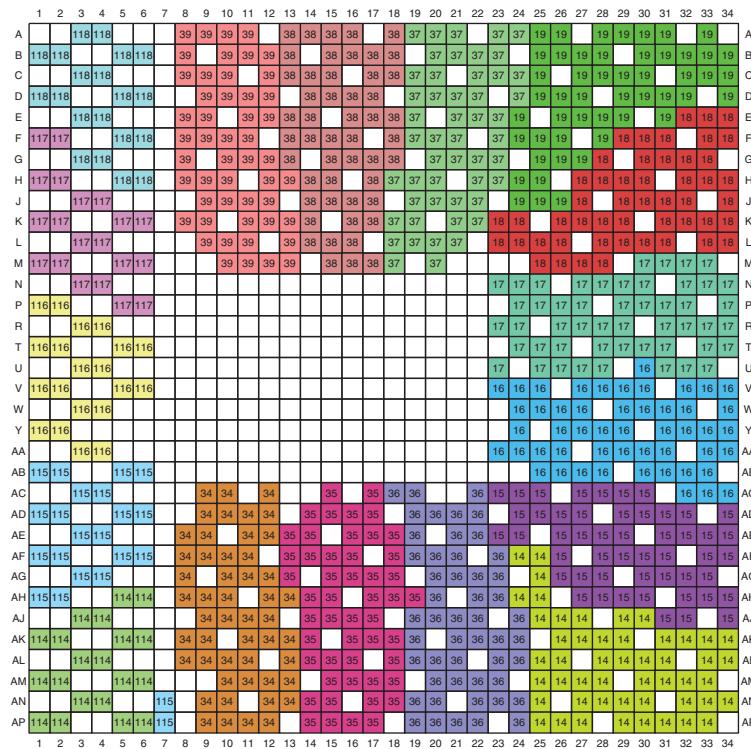
Figure 3-112: FF1927, FFG1927, and FFV1927 Packages—XC7VX415T Power and GND Placement

FF1157 and FFG1157 Packages—XC7VX485T



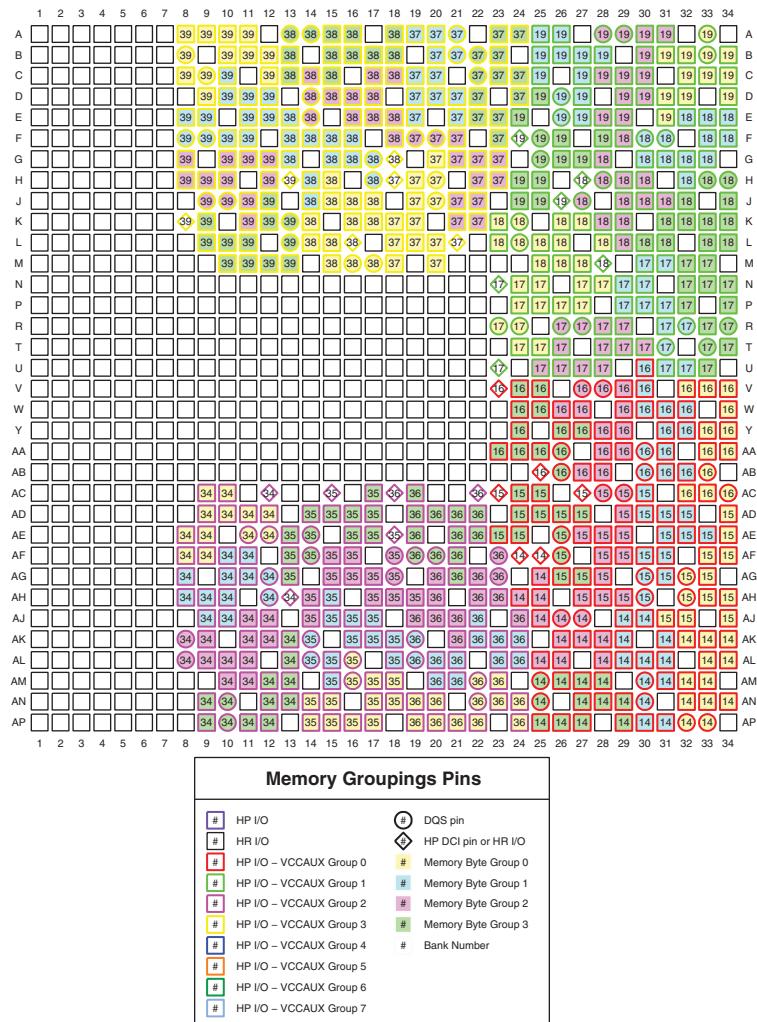
ug475_c3_100_090511

Figure 3-113: FF1157 and FFG1157 Packages—XC7VX485T Pinout Diagram



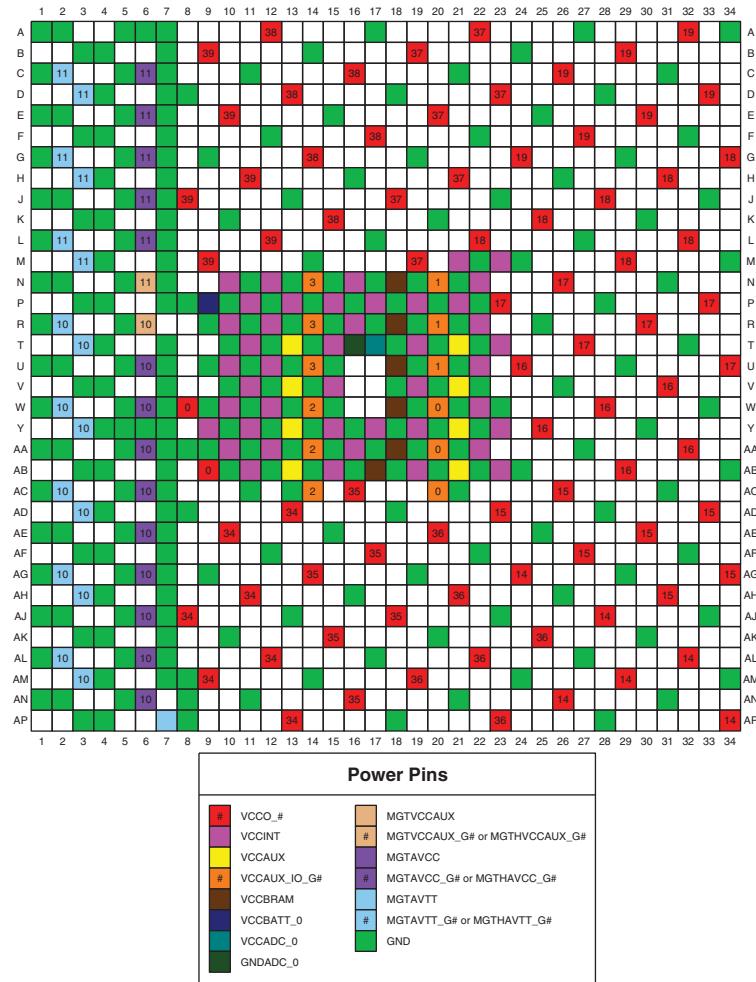
ug475_c3_101_052311

Figure 3-114: FF1157 and FFG1157 Packages—XC7VX485T I/O Banks



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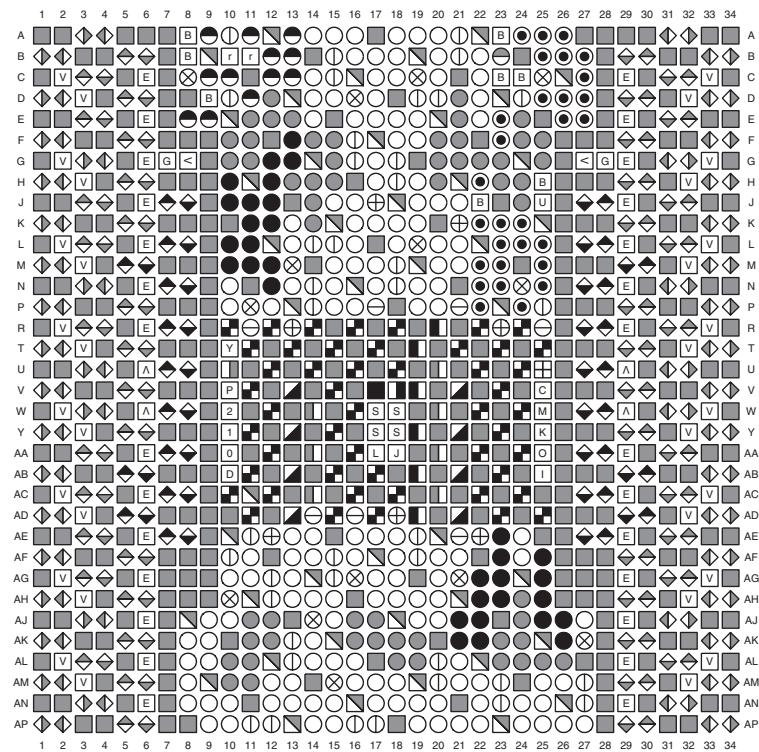
Figure 3-115: FF1157 and FFG1157 Packages—XC7VX485T Memory Groupings



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Figure 3-116: FF1157 and FFG1157 Packages—XC7VX485T Power and GND Placement

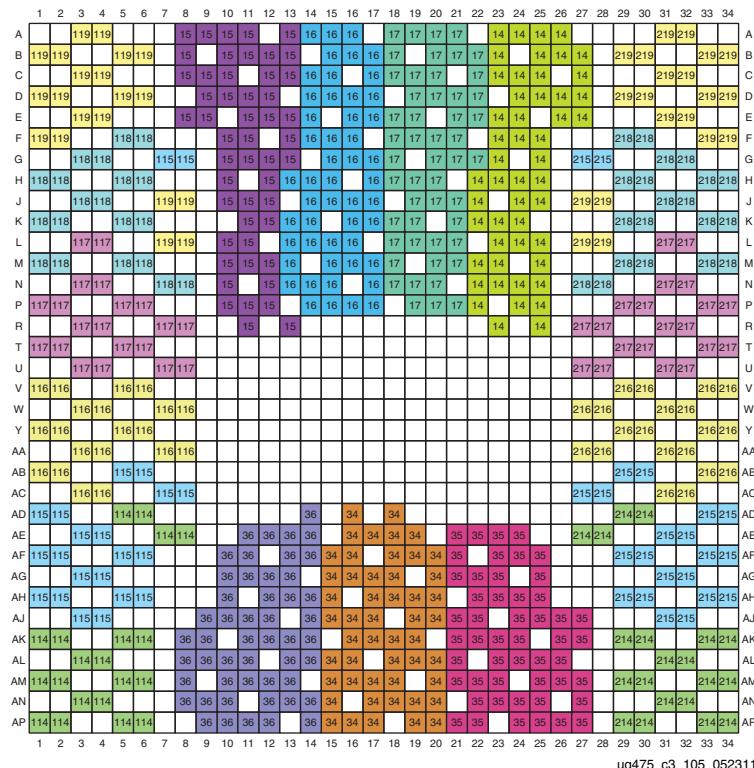
FF1158 and FFG1158 Packages—XC7VX485T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
<input type="circle"/> IO_LXXY_# <input type="square"/> IO_XX_#	<input type="square"/> MGTAVCC_G# <input type="square"/> MGTAVTT_G# <input type="square"/> MGTVCCAUX_G# <input type="square"/> MGTAVITRICAL <input type="square"/> MGTRREF <input type="square"/> MGTRREFCLK1/IOP <input type="square"/> MGTRREFCLK1/0N <input type="square"/> MGTXRP <input type="square"/> MGTXRN <input type="square"/> MGTXXP <input type="square"/> MGTXTN <input type="square"/> MGTHAVCC_G# <input type="square"/> MGTHAVTT_G# <input type="square"/> MGTHRXP <input type="square"/> MGTHRXN <input type="square"/> MGTHTXP <input type="square"/> MGHTHTXN	<input type="square"/> C CCLK_0 <input type="square"/> D CFGBVS_0 <input type="square"/> E DONE_0 <input type="square"/> J DXP_0 <input type="square"/> L DXN_0 <input type="square"/> Y GNDADC_0 <input type="square"/> 0 M0_0 <input type="square"/> 1 M1_0 <input type="square"/> 2 M2_0 <input type="square"/> P PROGRAM_B_0 <input type="square"/> K TCK_0 <input type="square"/> I TD1_0 <input type="square"/> O TDO_0 <input type="square"/> M TMS_0 <input type="square"/> S VP_0 <input type="square"/> S VN_0 <input type="square"/> S VREFP_0 <input type="square"/> S VREFN_0	<input type="square"/> GND <input type="square"/> VCCAUX_IO_G# <input type="square"/> VCCAUX <input type="square"/> VCCINT <input type="square"/> VCCO_# <input type="square"/> VCCBRAM <input type="square"/> NC
Multi-Function Pins <input type="square"/> ADV_B <input type="square"/> FCS_B <input type="square"/> FOE_B <input type="square"/> MOSI <input type="square"/> FWE_B <input type="square"/> DOUT_CS0_B <input type="square"/> CSI_B <input type="square"/> PUOC_B <input type="square"/> RDWR_B <input type="square"/> RS0-RS1 <input type="circle"/> ADOP/AD0N-AD15P/AD15N <input type="circle"/> EMCCLK	<input type="square"/> VRN <input type="square"/> VRP <input type="square"/> VREF <input type="circle"/> D00-D31 <input type="circle"/> A00-A28 <input type="square"/> DQS <input type="square"/> MRCC <input type="square"/> SRCC	<input type="square"/> C CCLK_0 <input type="square"/> D CFGBVS_0 <input type="square"/> E DONE_0 <input type="square"/> J DXP_0 <input type="square"/> L DXN_0 <input type="square"/> Y GNDADC_0 <input type="square"/> 0 M0_0 <input type="square"/> 1 M1_0 <input type="square"/> 2 M2_0 <input type="square"/> P PROGRAM_B_0 <input type="square"/> K TCK_0 <input type="square"/> I TD1_0 <input type="square"/> O TDO_0 <input type="square"/> M TMS_0 <input type="square"/> S VP_0 <input type="square"/> S VN_0 <input type="square"/> S VREFP_0 <input type="square"/> S VREFN_0	<input type="square"/> GND <input type="square"/> VCCAUX_IO_G# <input type="square"/> VCCAUX <input type="square"/> VCCINT <input type="square"/> VCCO_# <input type="square"/> VCCBRAM <input type="square"/> NC

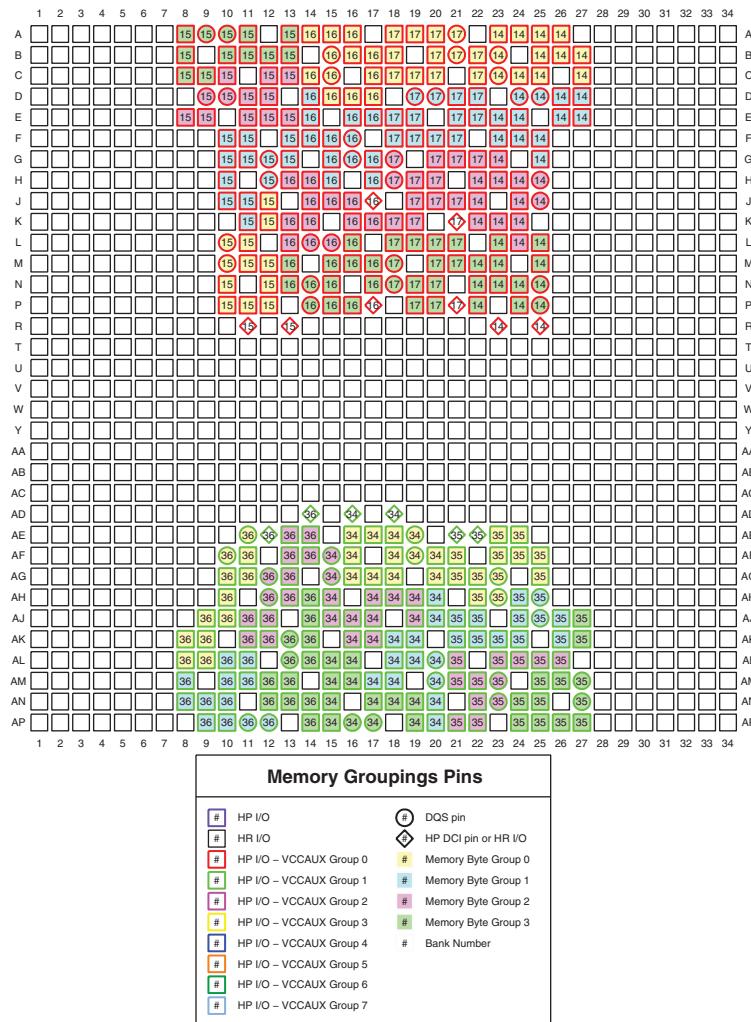
ug475_c3_104_090511

Figure 3-117: FF1158 and FFG1158 Packages—XC7VX485T Pinout Diagram



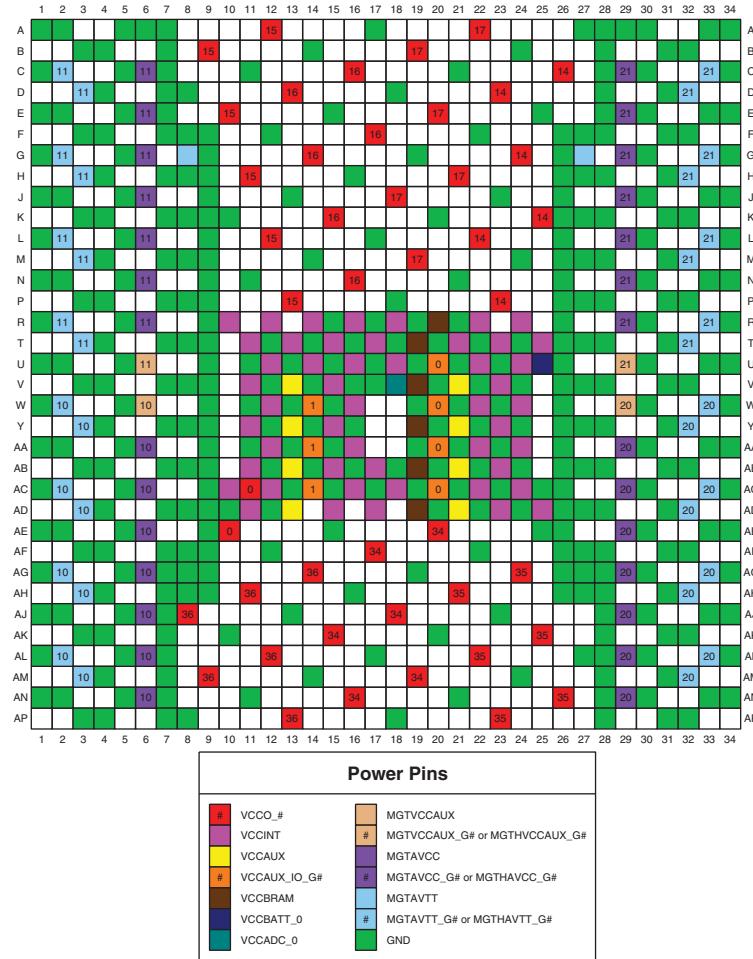
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Figure 3-118: FF1158 and FFG1158 Packages—XC7VX485T I/O Banks



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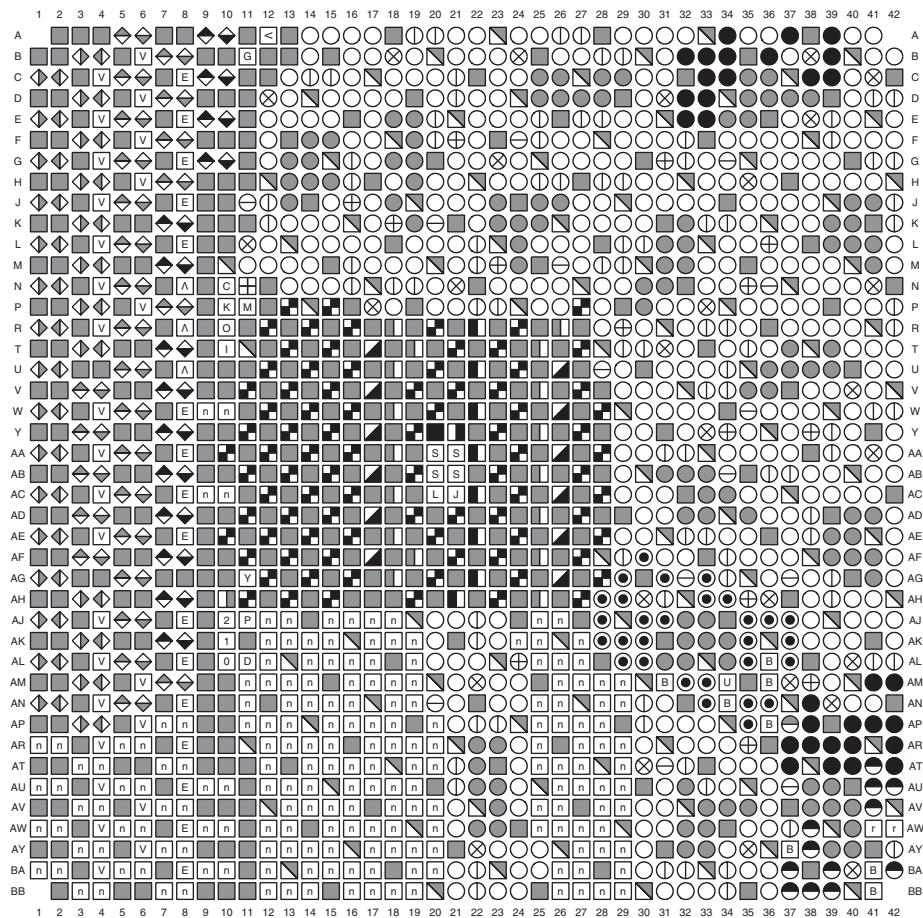
Figure 3-119: FF1158 and FFG1158 Packages—XC7VX485T Memory Groupings



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Figure 3-120: FF1158 and FFG1158 Packages—XC7VX485T Power and GND Placement

FF1761, FFG1761, and RF1761 Packages—XC7VX485T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_# ○ IO_XX_#	[E] MGTAVCC_G# [V] MGTAVTT_G# [A] MGTVCXAUX_G# [D] MGTAVTRCAL [G] MGTRREF	[C] CCLK_0 [I] CFGBVS_0 [D] DONE_0 [J] DXP_0 [L] DXN_0	[S] VP_0 [S] VN_0 [S] VREFP_0 [S] VREFN_0 [S] GNDADC_0 [Y] INIT_B_0 [O] M0_0 [I] M1_0 [Z] M2_0 [P] PROGRAM_B_0 [K] TCK_0 [I] TD1_0 [O] TDO_0 [M] TMS_0 [V] VCCADC_0 [H] VCCBATT_0
Multi-Function Pins			
B ADV_B B FCS_B B FOE_B B MOSI B FWE_B B DOUT_CS0_B B CSL_B B PUDC_B U RDWR_B f RSO-RS1 ● ADOP/ADON-AD15P/AD15N ○ EMCCLK	⊕ VRN ○ VRP ○ VREF ● D00-D31 ● A00-A28 ○ DQS ○ MRCC ○ SRCC	◆ MGTREFCLK1/0P ◆ MGTREFCLK1/0N ◆ MGTXXP ◆ MGTXRXN ◆ MGTXXP ◆ MGTXRN ◆ MGTHAVCC_G# ◆ MGTHAVTT_G# ◆ MGTHRXP ◆ MGTHRXN ◆ MGTHXP ◆ MGTHTXN	■ GND □ VCCAUX_IO_G# ▨ VCCAUX ▨ VCCINT ▨ VCCO_# ▨ VCCBRAM n NC

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Figure 3-121: FF1761, FFG1761, and RF1761 Packages—XC7VX485T Pinout Diagram

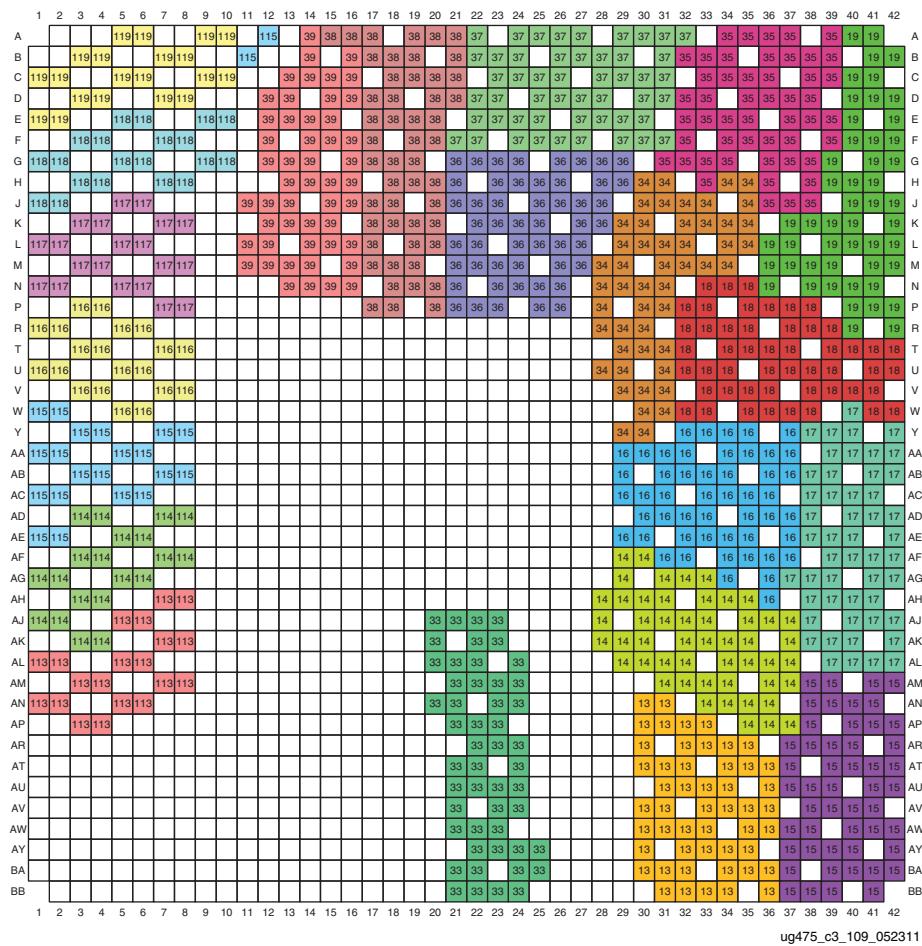
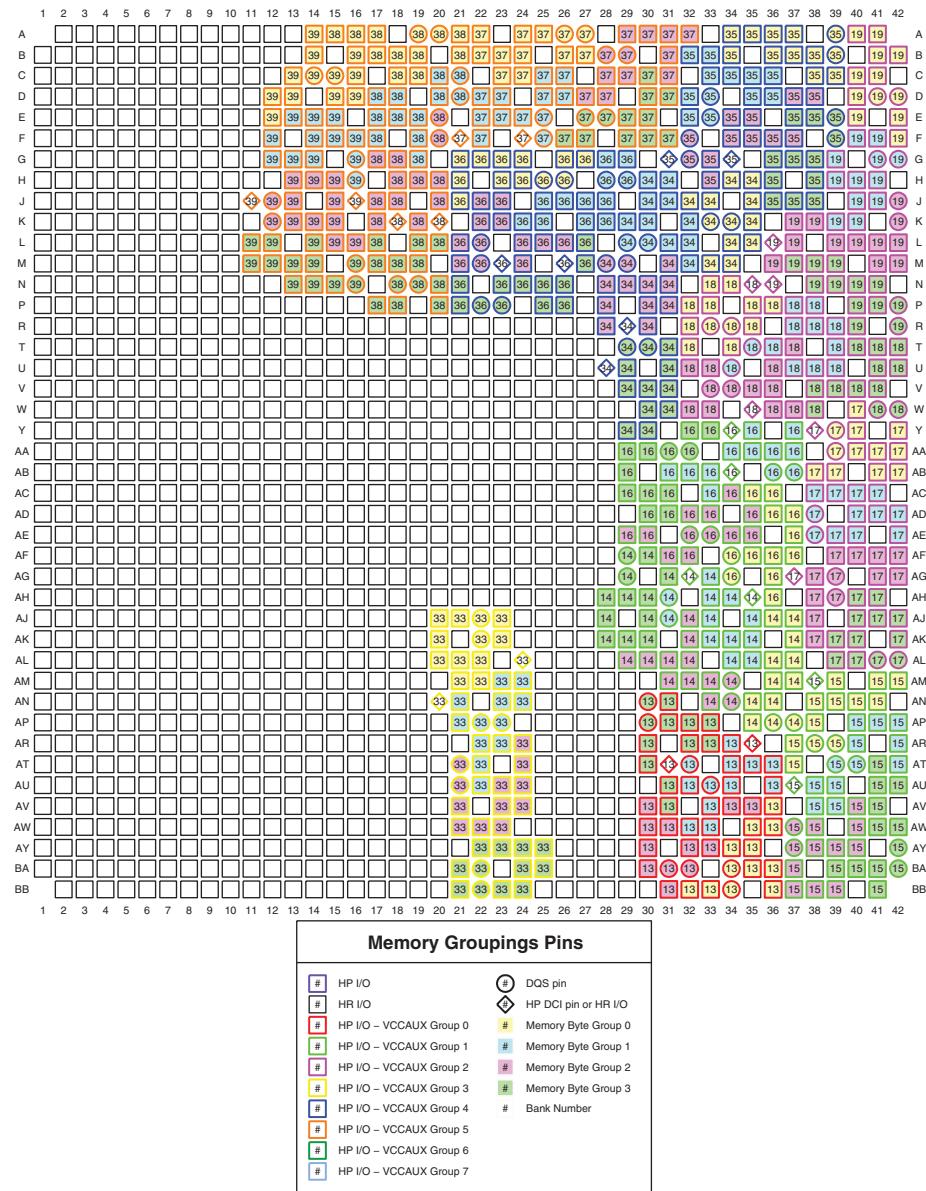
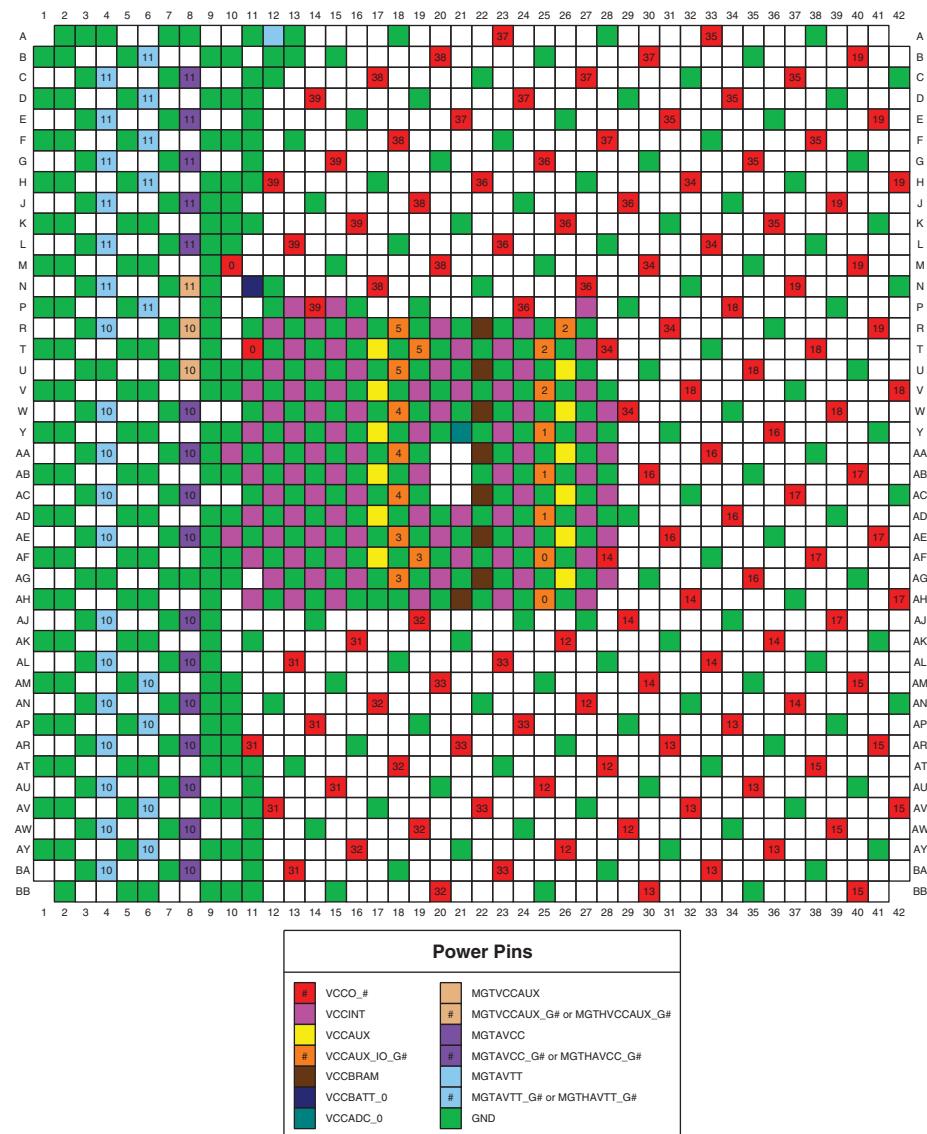


Figure 3-122: FF1761, FFG1761, and RF1761 Packages—XC7VX485T I/O Banks



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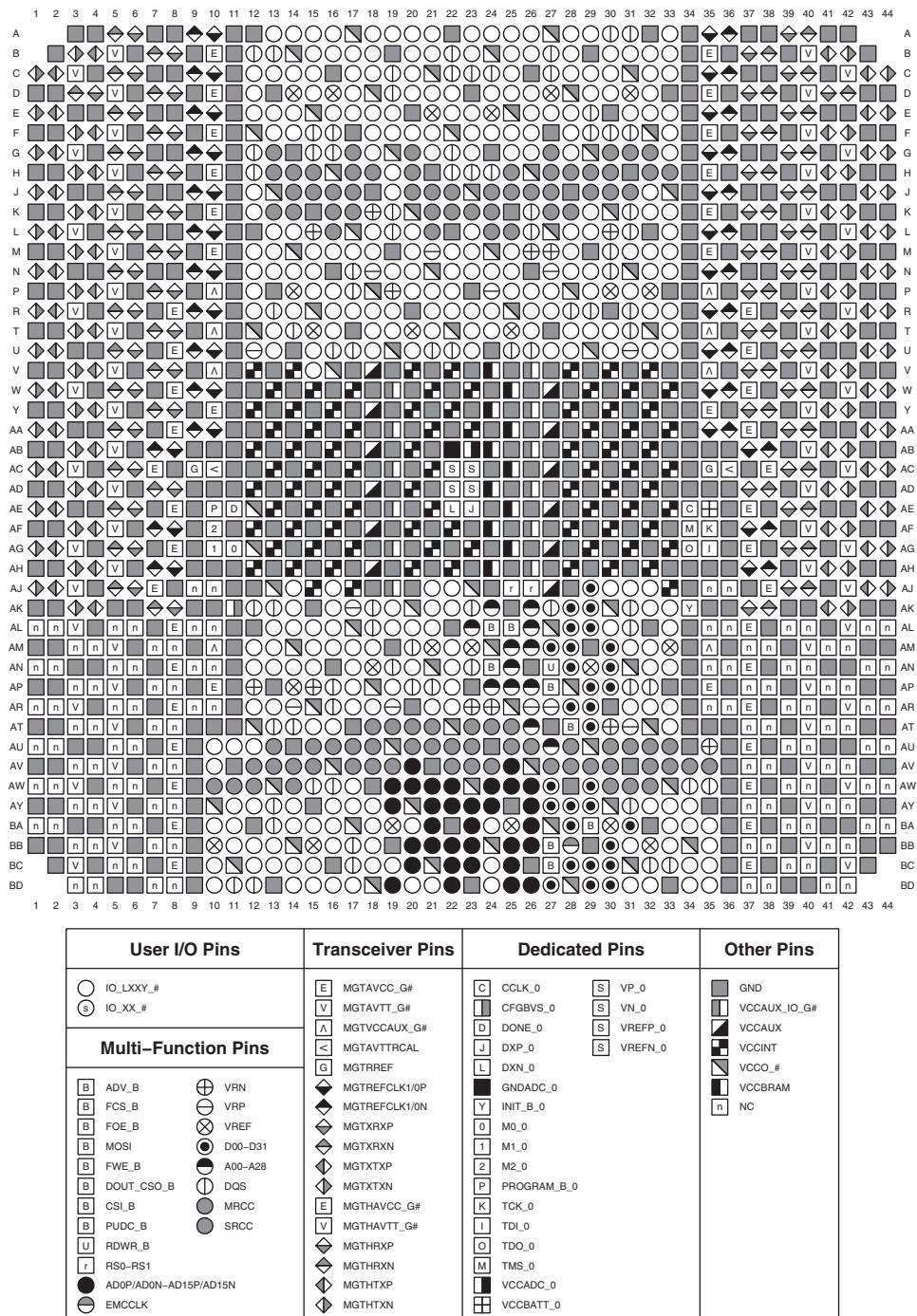
Figure 3-123: FF1761, FFG1761, and RF1761 Packages—XC7VX485T Memory Groupings



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Figure 3-124: FF1761, FFG1761, and RF1761 Packages—XC7VX485T Power and GND Placement

FF1927 and FFG1927 Packages—XC7VX485T



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Figure 3-125: FF1927 and FFG1927 Packages—XC7VX485T Pinout Diagram

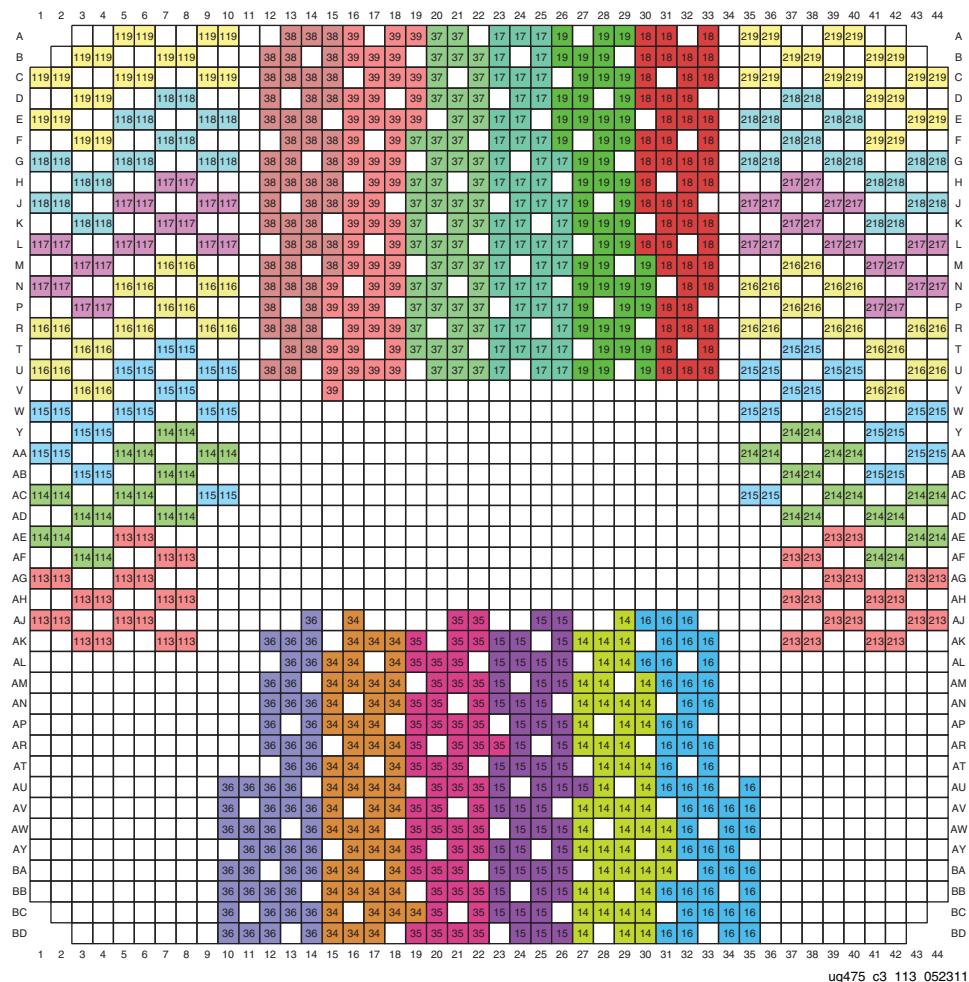
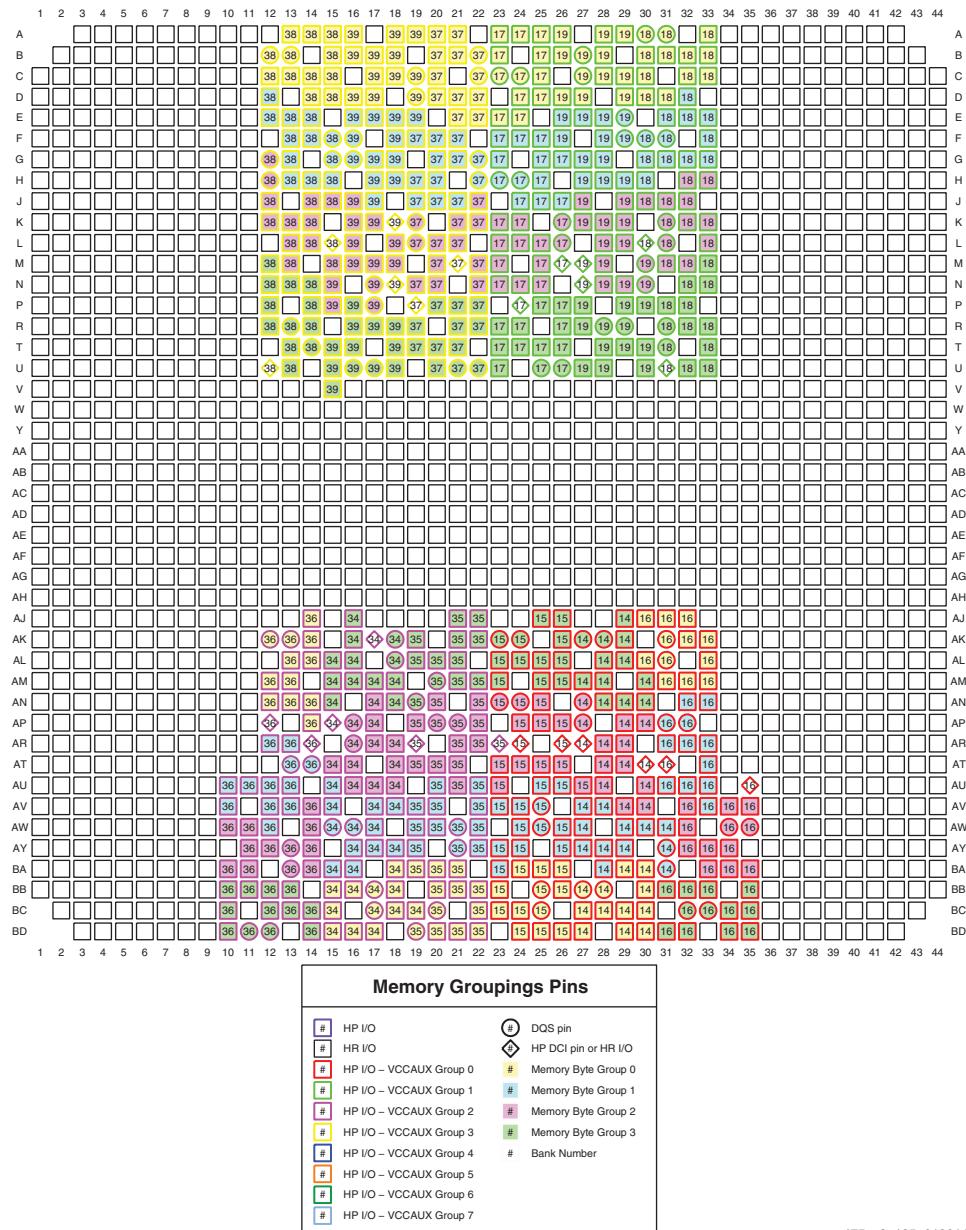
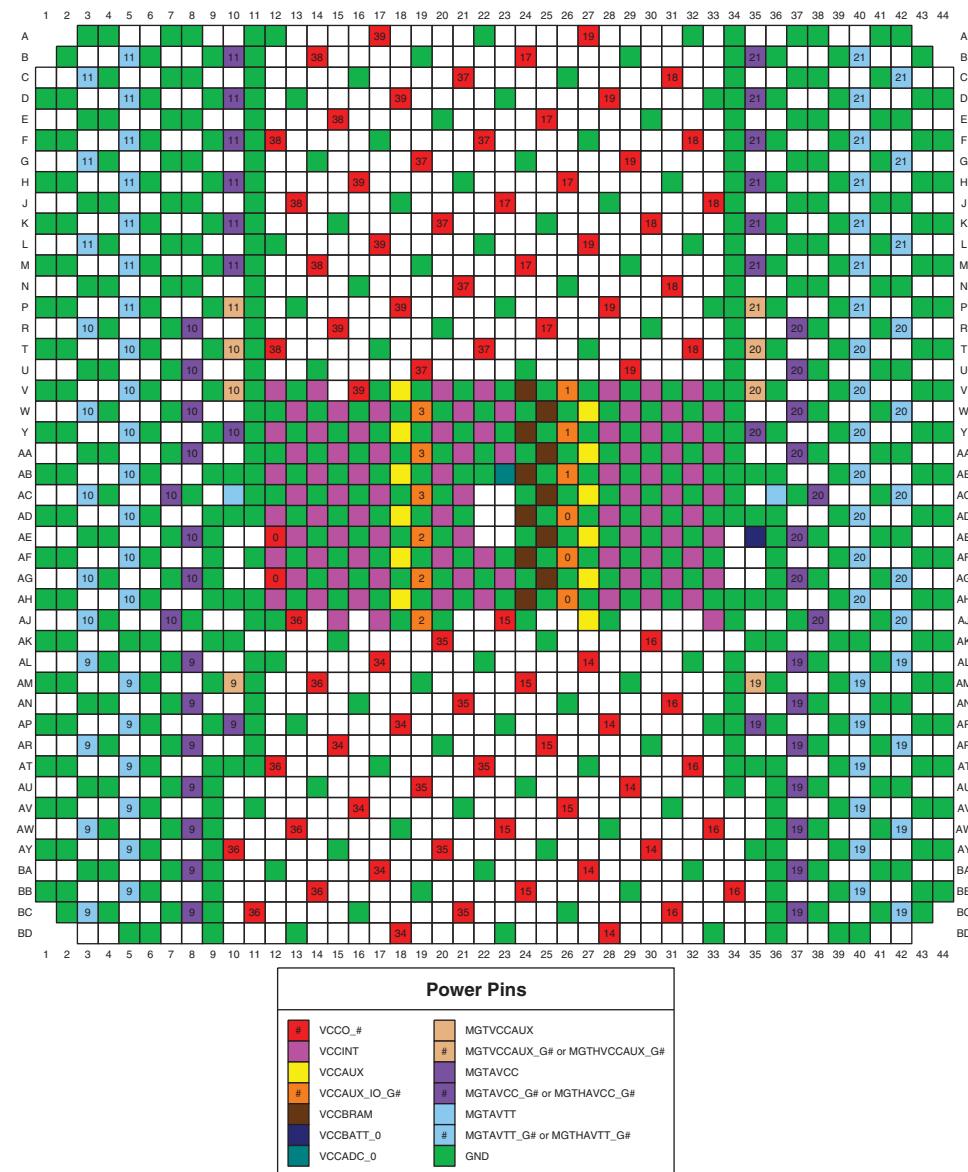


Figure 3-126: FF1927 and FFG1927 Packages—XC7VX485T I/O Banks



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Figure 3-127: FF1927 and FFG1927 Packages—XC7VX485T Memory Groupings



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Figure 3-128: FF1927 and FFG1927 Packages—XC7VX485T Power and GND Placement

FF1930, FFG1930, and RF1930 Packages—XC7VX485T

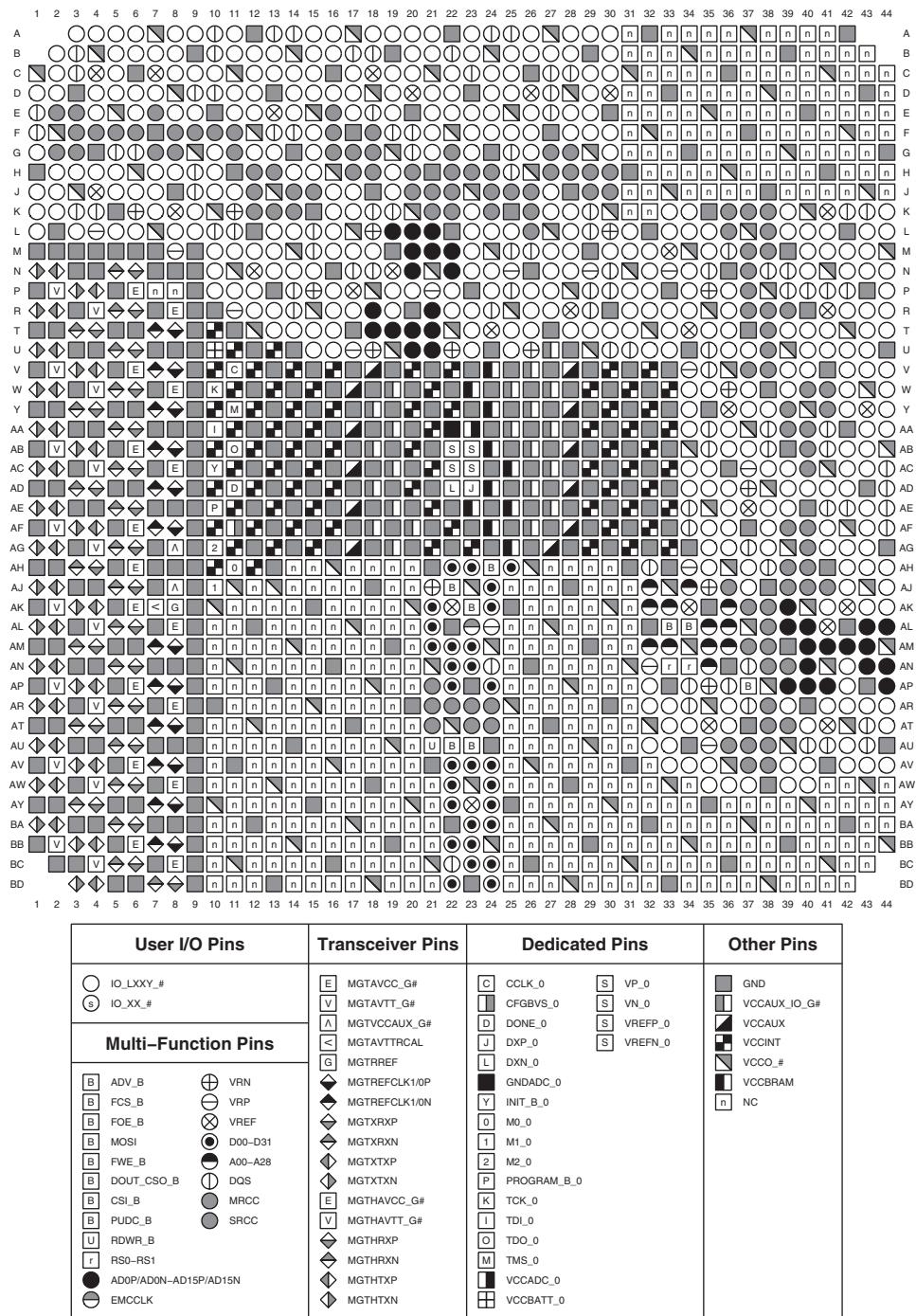


Figure 3-129: FF1930, FFG1930, and RF1930 Packages—XC7VX485T Pinout Diagram

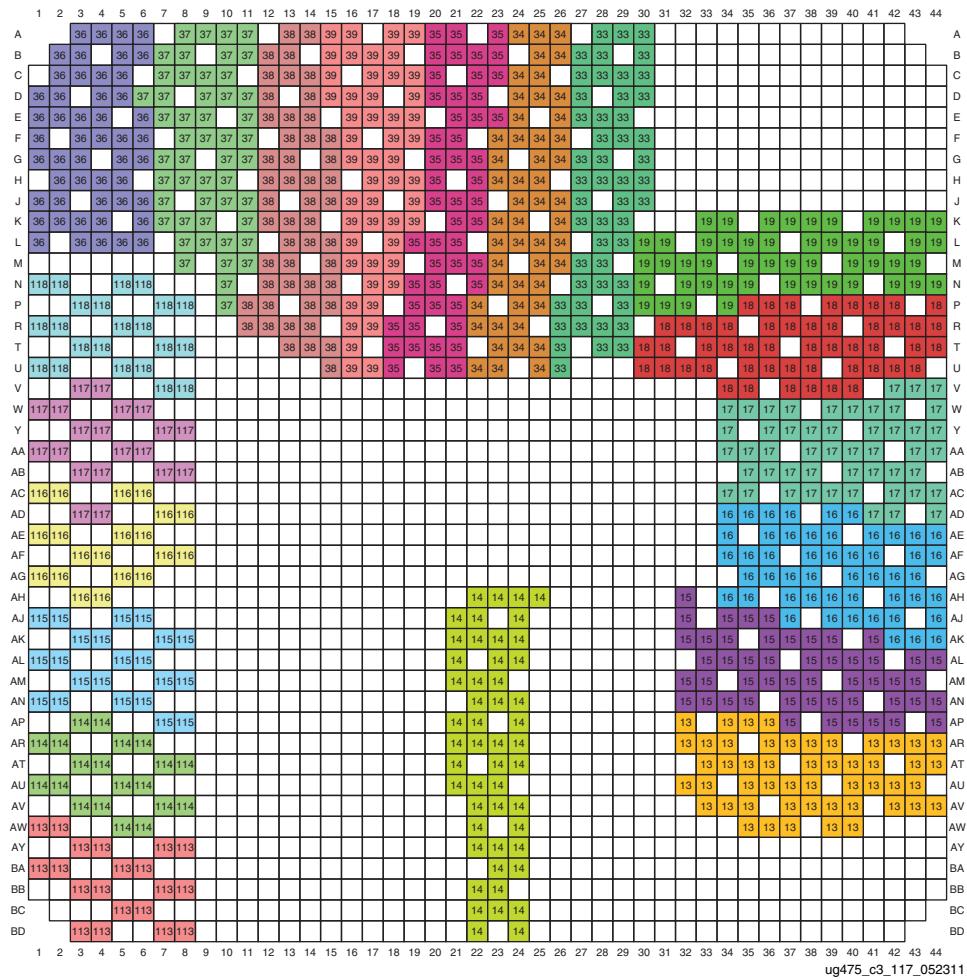
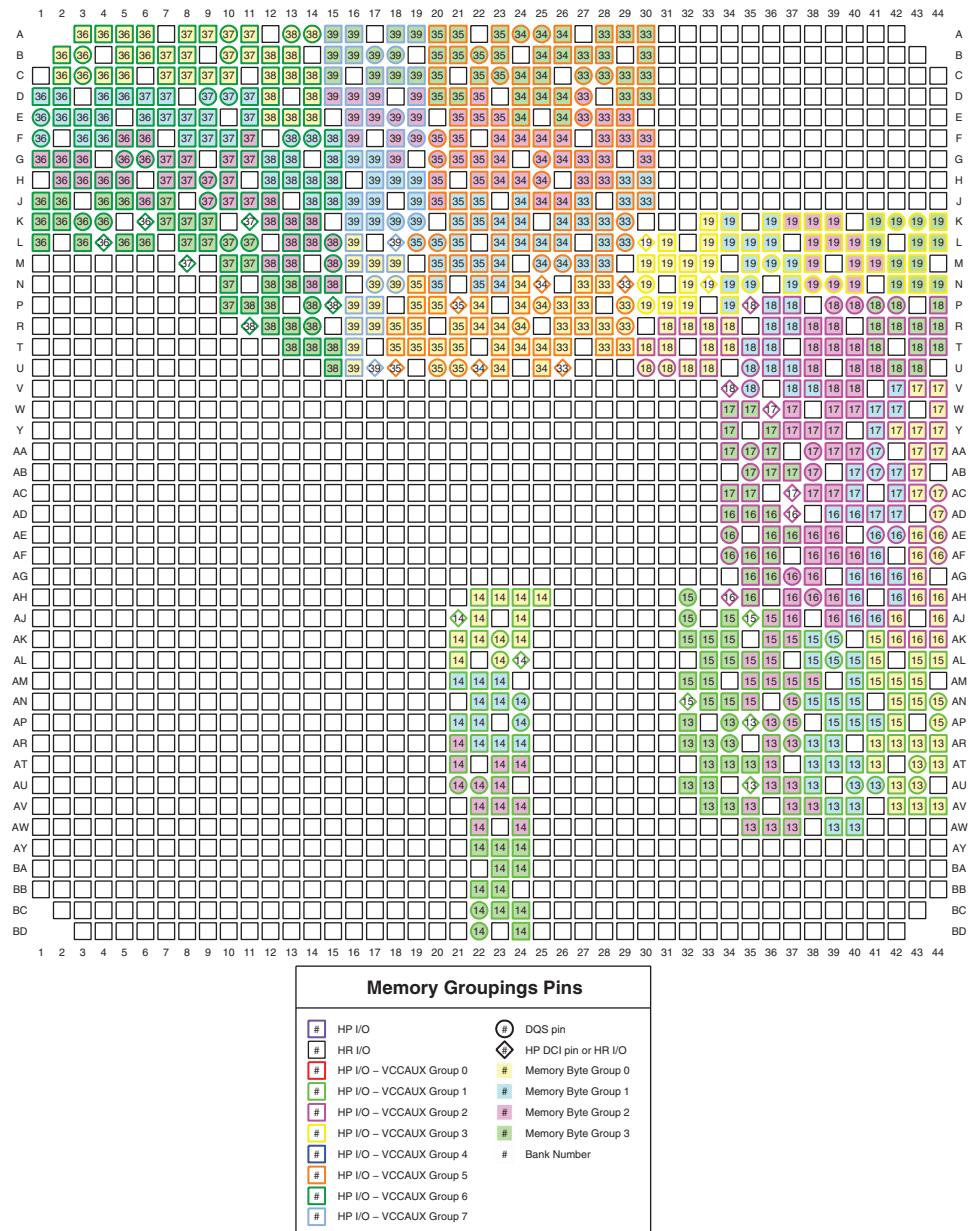
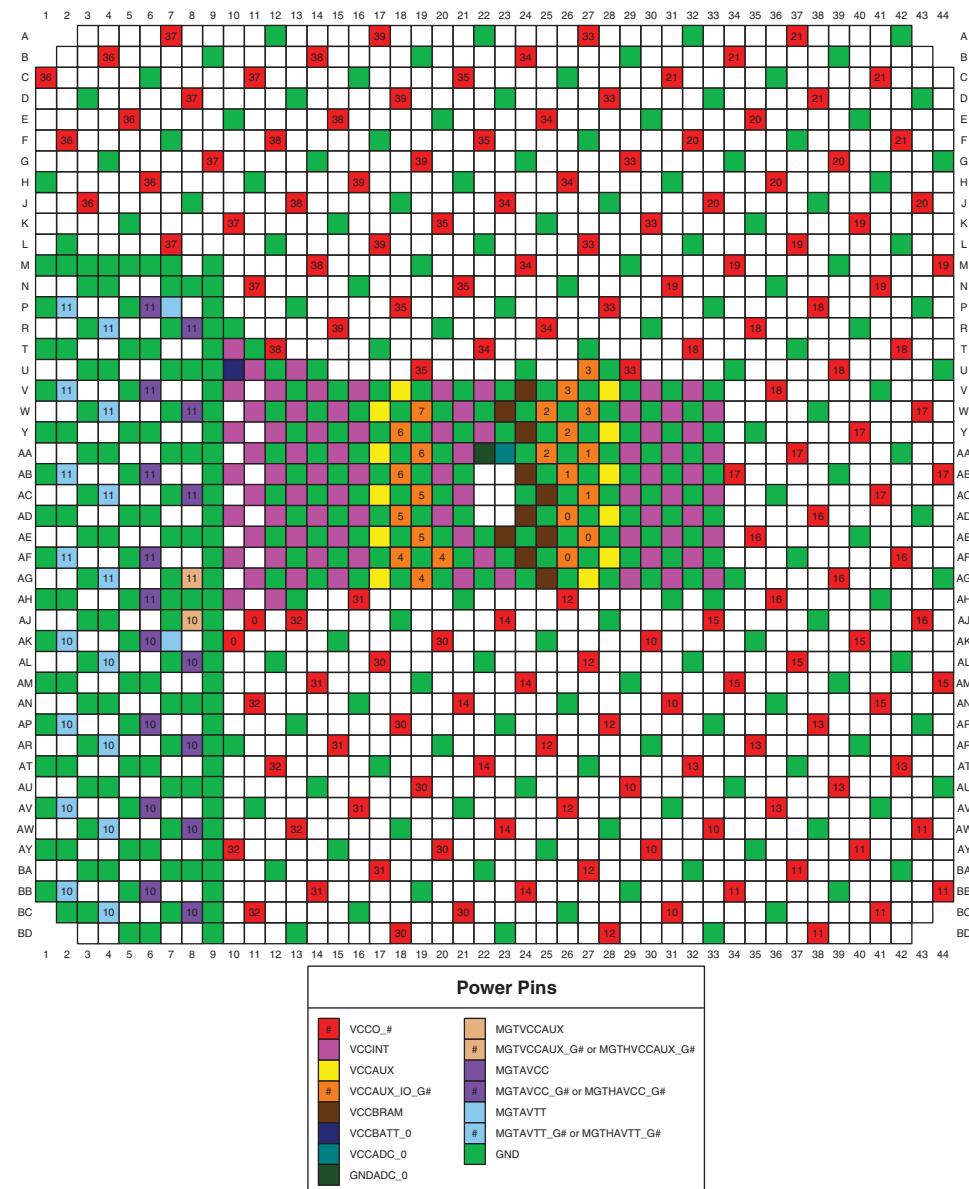


Figure 3-130: FF1930, FFG1930, and RF1930 Packages—XC7VX485T I/O Banks



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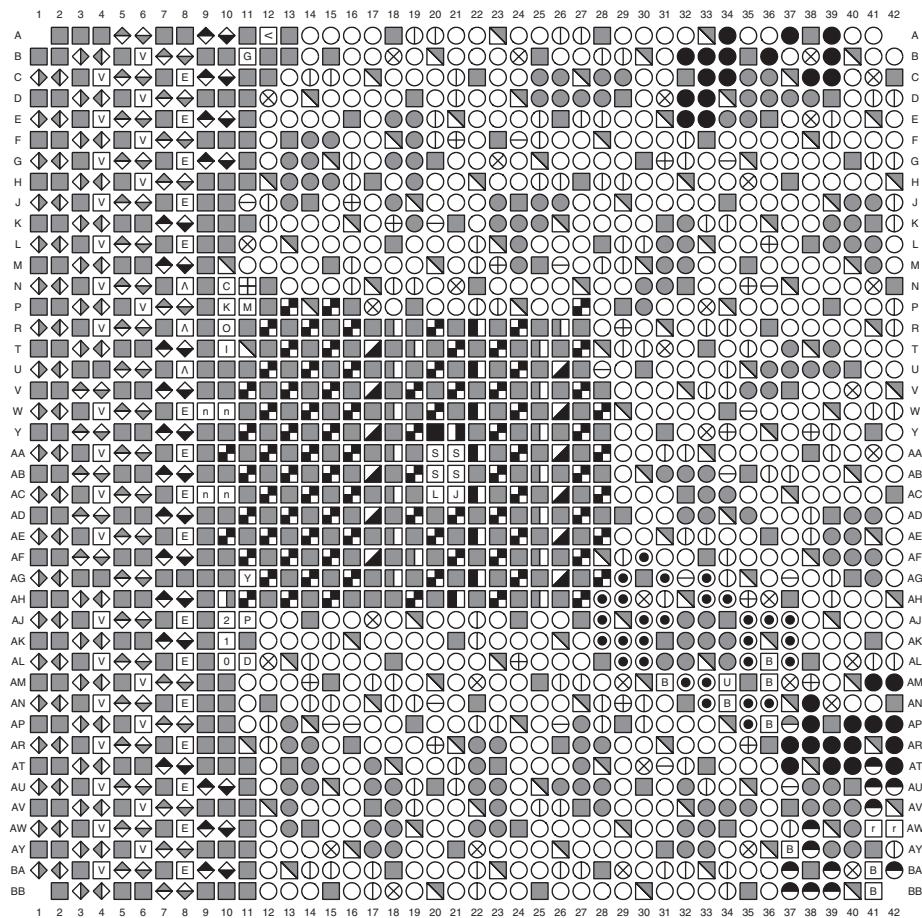
Figure 3-131: FF1930, FFG1930, and RF1930 Packages—XC7VX485T Memory Groupings



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Figure 3-132: FF1930, FFG1930, and RF1930 Packages—XC7VX485T Power and GND Placement

FF1761, FFG1761, and RF1761 Packages—XC7VX690T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_# ⊖ IO_XX_#	E MGTAVCC_G# V MGTAVTT_G# A MGTVCCAUX_G# < MGTAVTRCAL G MGTRREF	C CCLK_0 CFGBVS_0 D DONE_0 J DXP_0 L DXN_0 Y GNDADC_0 INIT_B_0 0 M0_0 1 M1_0 2 M2_0 P PROGRAM_B_0 K TCK_0 V TDI_0 O TDO_0 M TMS_0 V VCCADC_0 BBATT_0	S VP_0 VN_0 S VREFP_0 S VREFN_0 ■ GND ■ VCCAUX_IO_G# ■ VCCAUX ■ VCCINT ■ VCCO_# ■ VCCBRAM n NC
Multi-Function Pins	B ADV_B B FCS_B B FOE_B B MOSI B FWE_B B DOUT_CSO_B B CSL_B B PUDC_B U RDWR_B r RS0-RS1 ● AD0P/AD0N-AD15P/AD15N ⊖ EMCCLK	⊕ VRN ⊖ VRP ⊗ VREF ● D00-D31 ● A00-A28 ○ DQS ● MRCC ● SRCC	

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Figure 3-133: FF1761, FFG1761, and RF1761 Packages—XC7VX690T Pinout Diagram

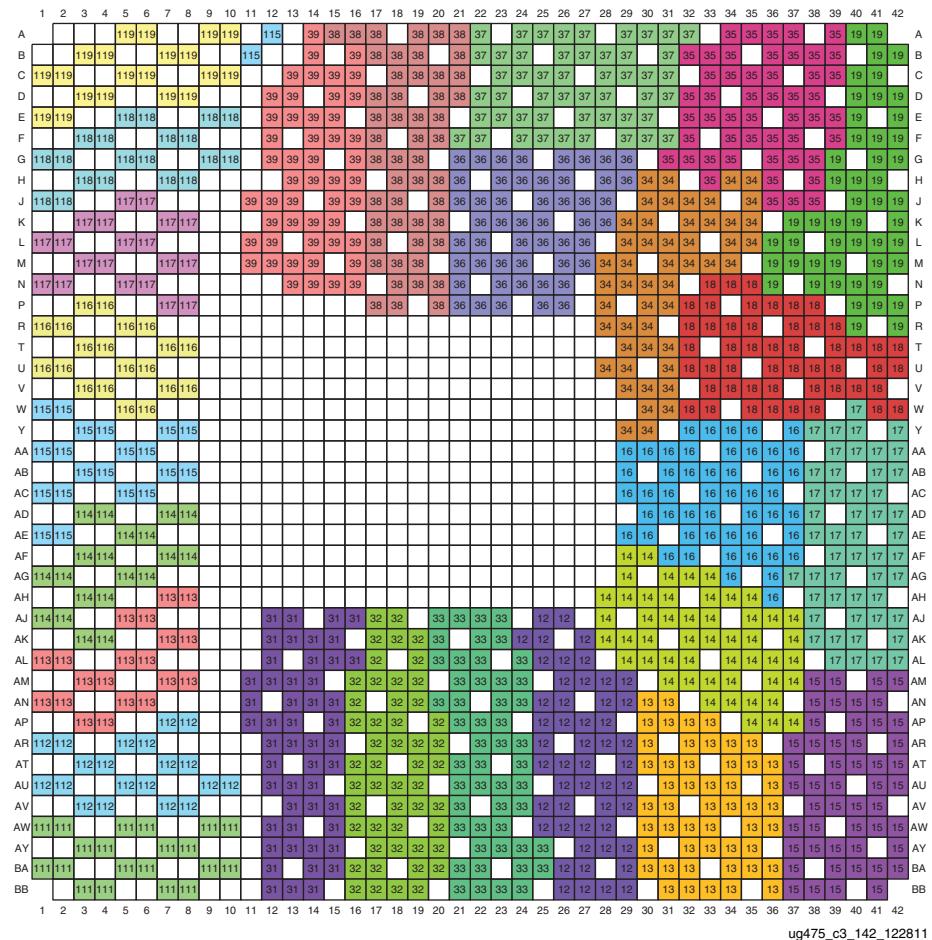
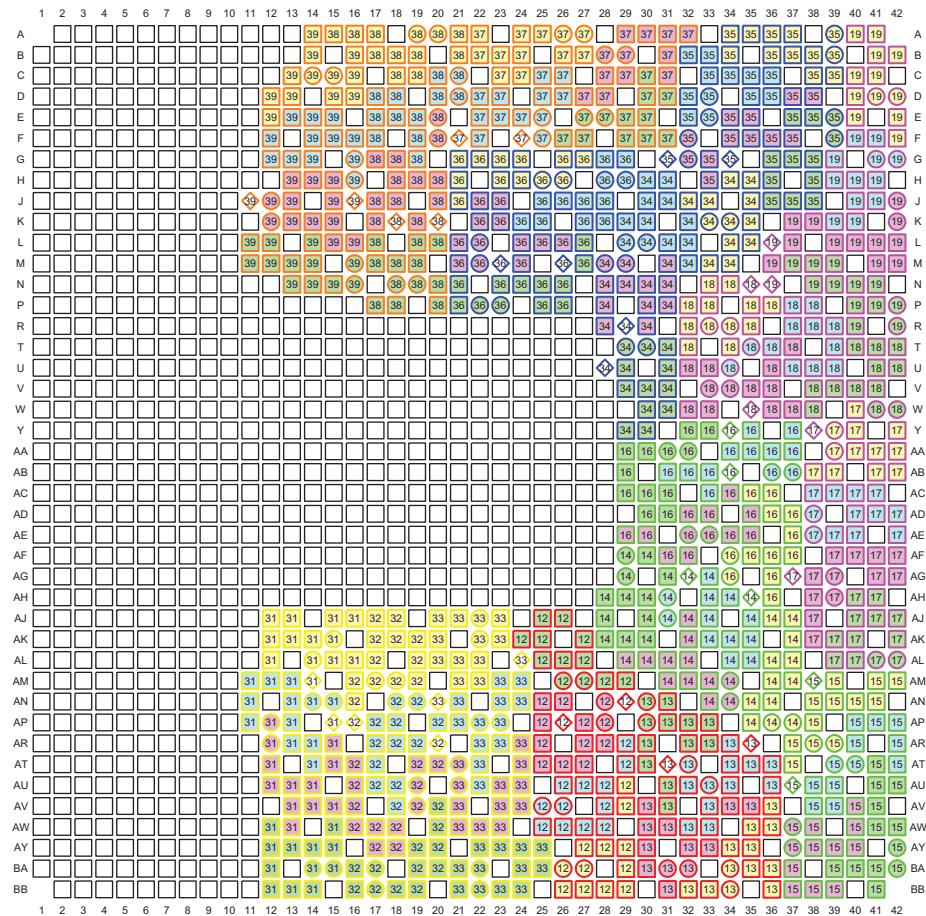
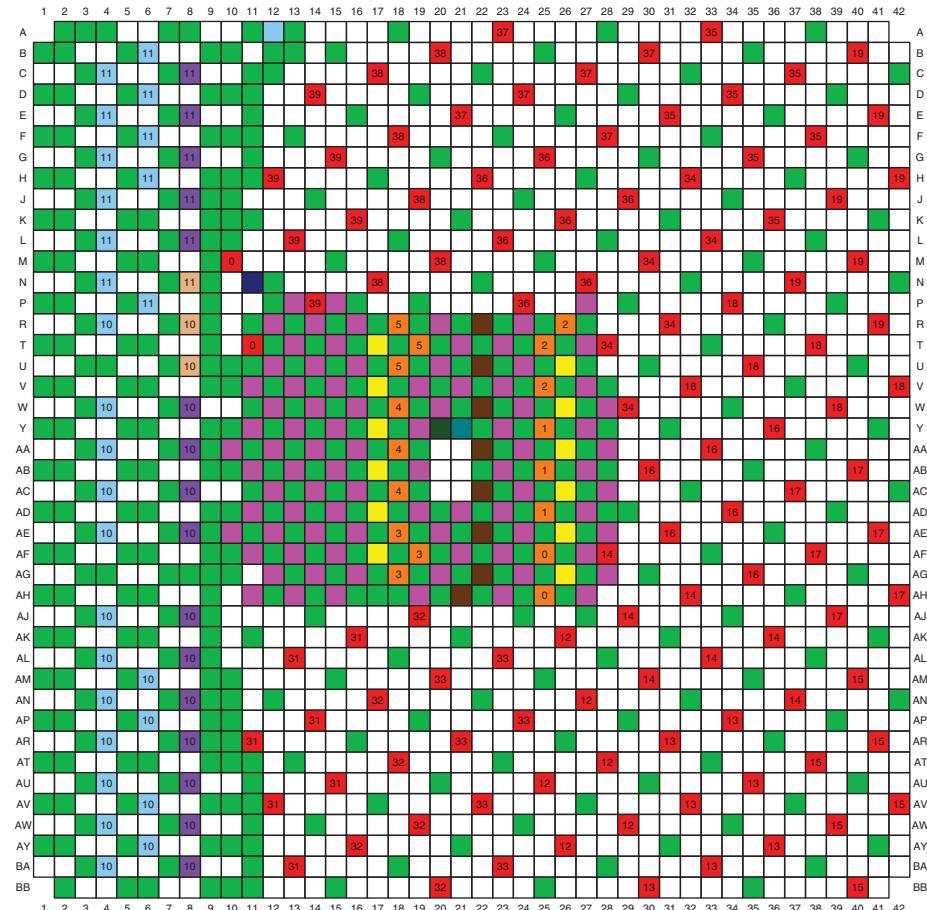


Figure 3-134: FF1761, FFG1761, and RF1761 Packages—XC7VX690T I/O Banks



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Figure 3-135: FF1761, FFG1761, and RF1761 Packages—XC7VX690T Memory Groupings

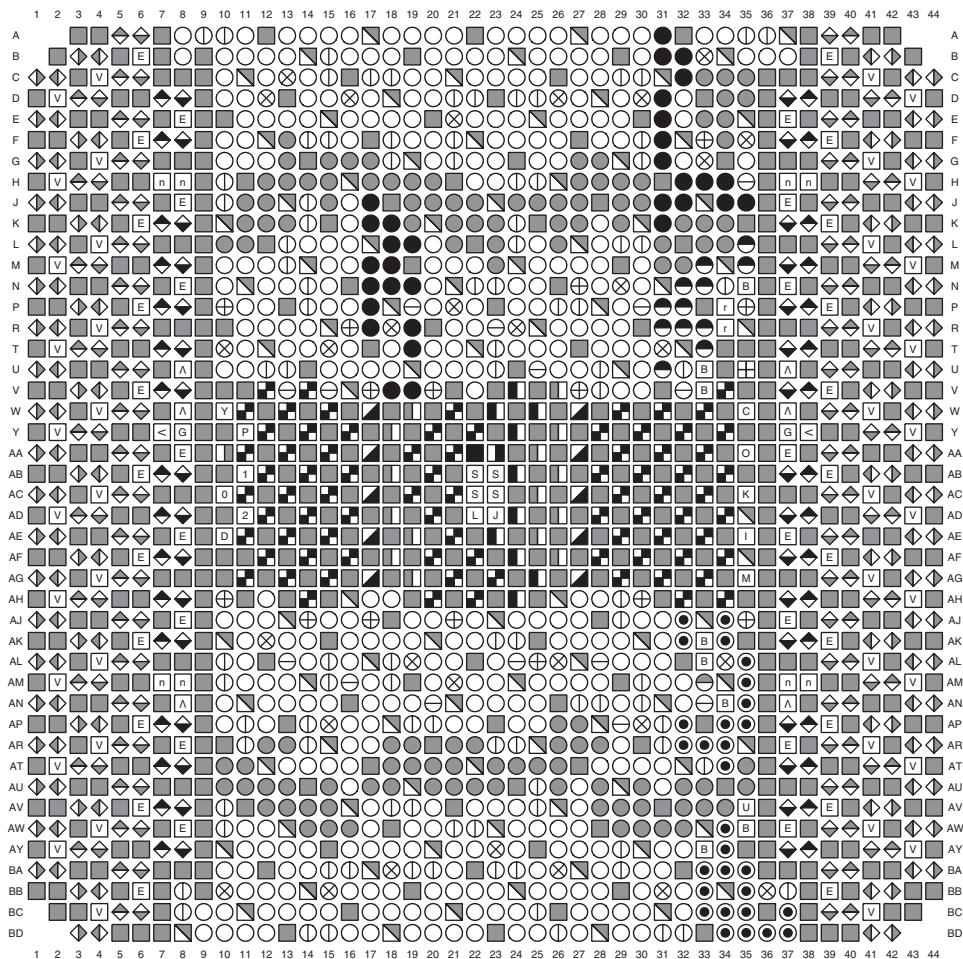


Power Pins	
VCCO_#	MGTVCXAUX
VCCINT	MGTVCXAUX_G# or MGTHVCCAUX_G#
VCCAUX	MGTAVCC
VCCAUX_IO_G#	MGTAVCC_G# or MGTHAVCC_G#
VCCBRAM	MGTAVTT
VCCBATT_0	MGTAVTT_G# or MGTHAVTT_G#
VCCADC_0	GND
GNDADC_0	

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Figure 3-136: FF1761, FFG1761, and RF1761 Packages—XC7VX690T Power and GND Placement

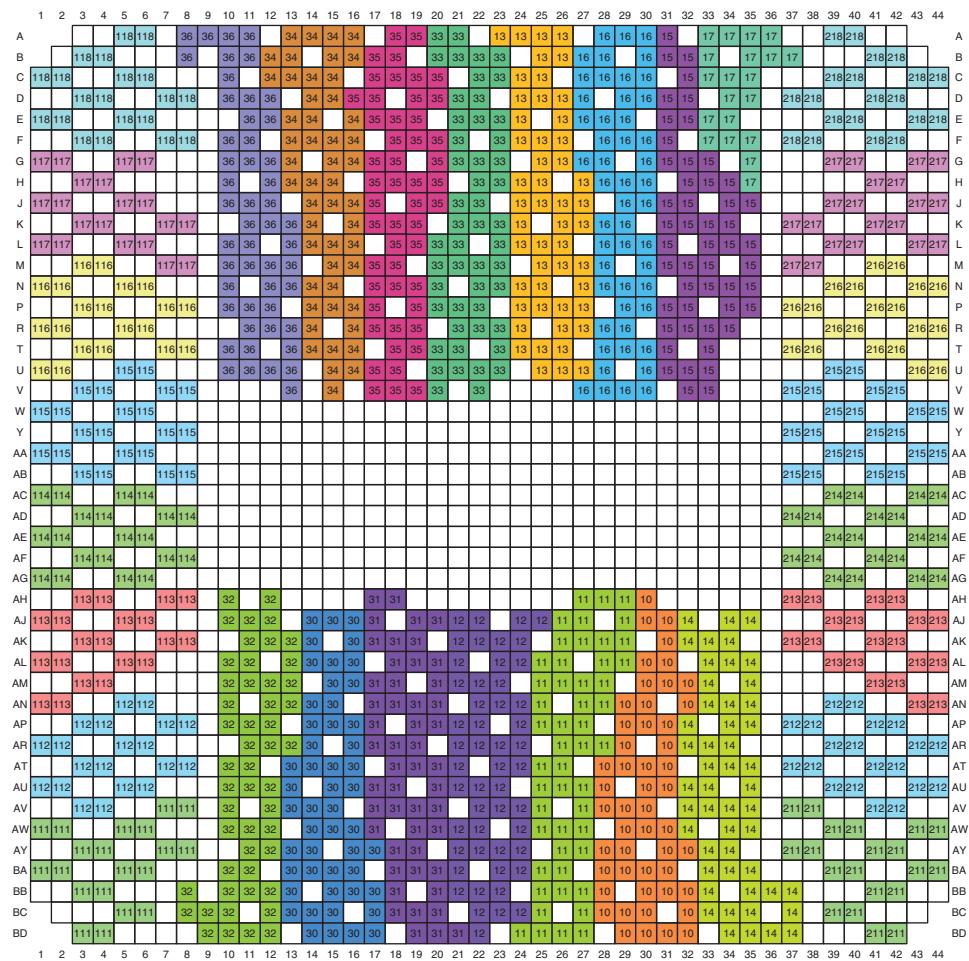
FF1926 and FFG1926 Packages—XC7VX690T and XC7VX980T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_# ⊖ IO_XX_#			■ GND □ VCCAUX_IO_G# ▨ VCCAUX ▨ VCCINT ▨ VCCO_# ▨ VCCBRAM n NC
Multi-Function Pins	■ ADV_B ■ FCS_B ■ FOE_B ■ MOSI ■ FWE_B ■ DOUT_CSO_B ■ CSL_B ■ PUDC_B ■ RDWR_B r RS0-RS1 ● ADOP/AD0N-AD15P/AD15N ⊖ EMCCLK	○ VRN ○ VRP ○ VREF ○ D00-D31 ○ A00-A28 ○ DQS ○ MRCC ○ SRCC ○ MGTHAVCC_G# ○ MGTHAVTT_G# ○ MGTHRXP ○ MGTHRXN ○ MGHTXP ○ MGHTXN	■ CCLKL_0 ■ CFGBVS_0 ■ DONE_0 ■ DXP_0 ■ DXN_0 ■ GNDADC_0 ■ INIT_B_0 ○ M0_0 ○ M1_0 ○ M2_0 ○ PROGRAM_B_0 ■ TCK_0 ■ TDIL_0 ○ TDO_0 ○ TMS_0 ■ VCCADC_0 ■ VCCBATT_0

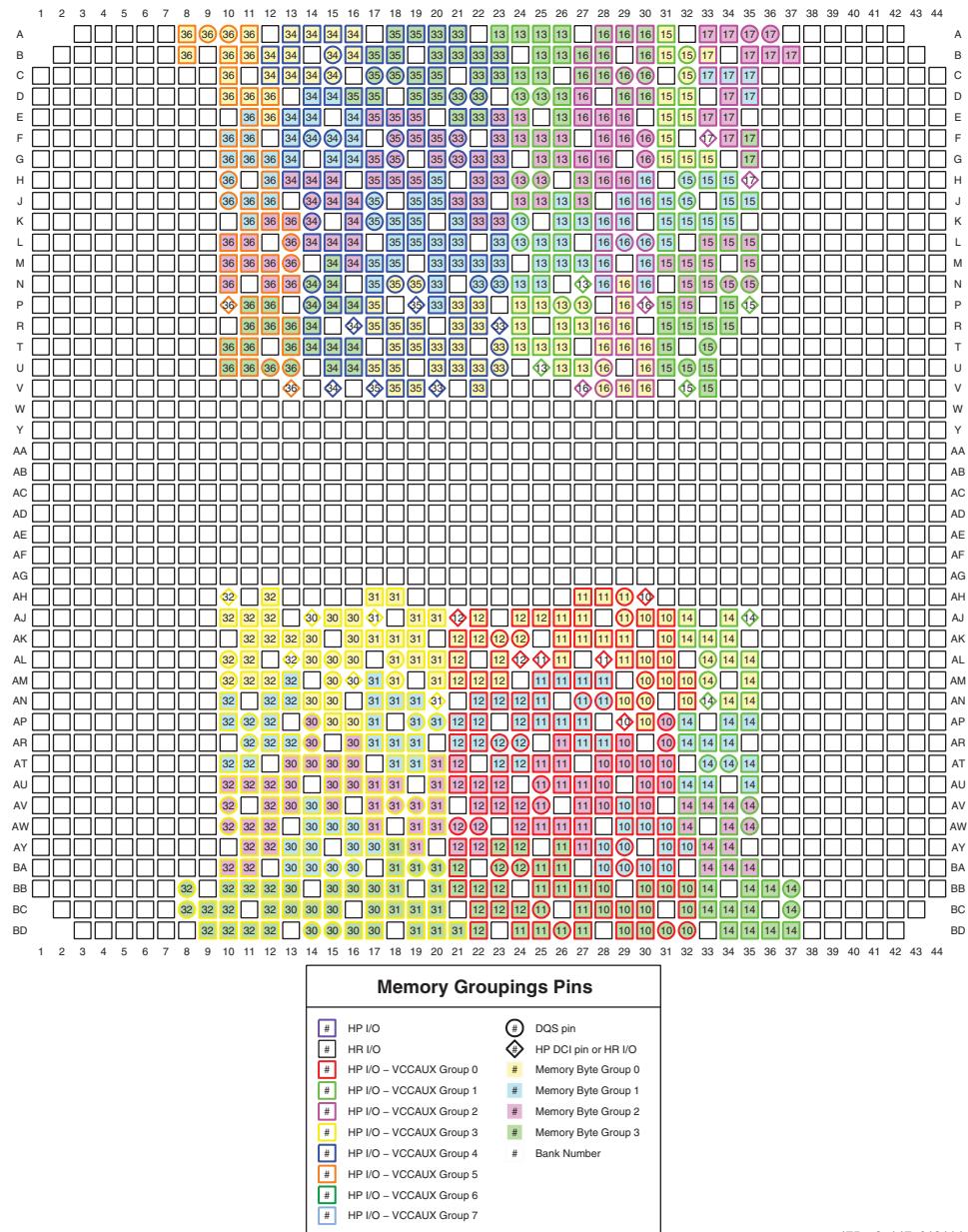
ug475_c3_145_122811

Figure 3-137: FF1926 and FFG1926 Packages—XC7VX690T and XC7VX980T Pinout Diagram



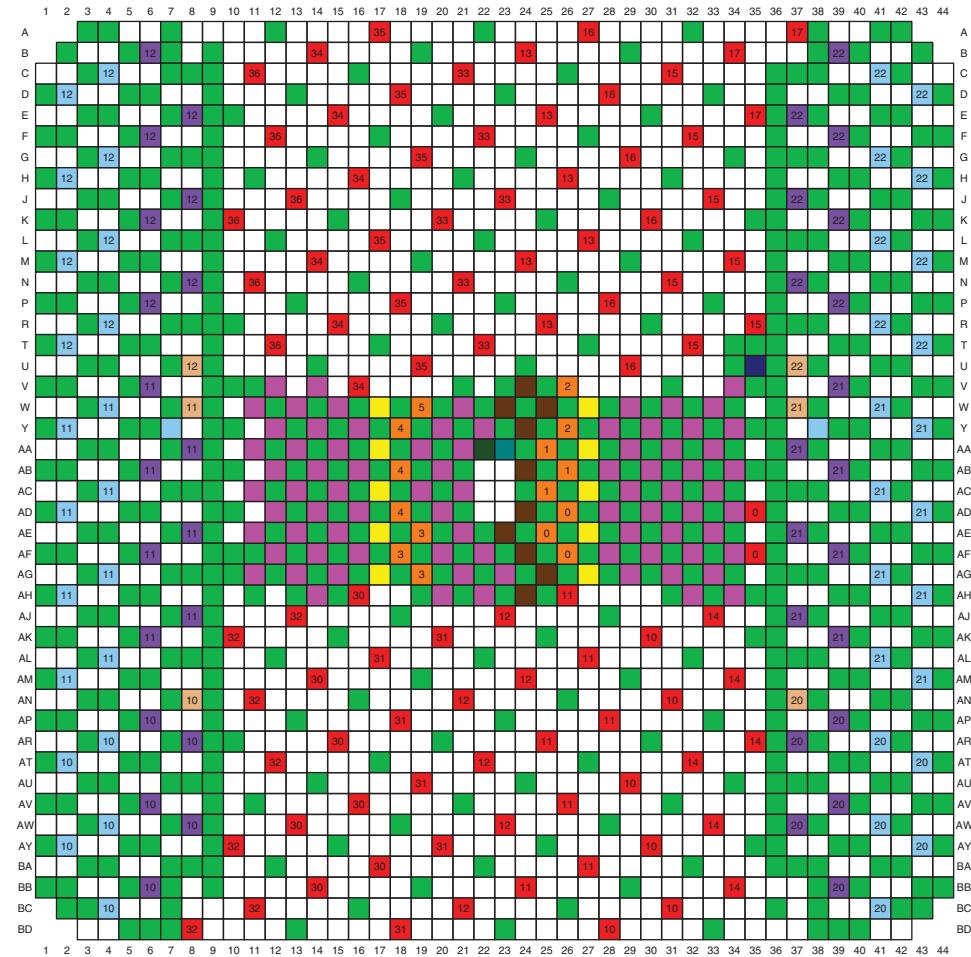
ug475_c3_146_122811

Figure 3-138: FF1926 and FFG1926 Packages—XC7VX690T and XC7VX980T I/O Banks



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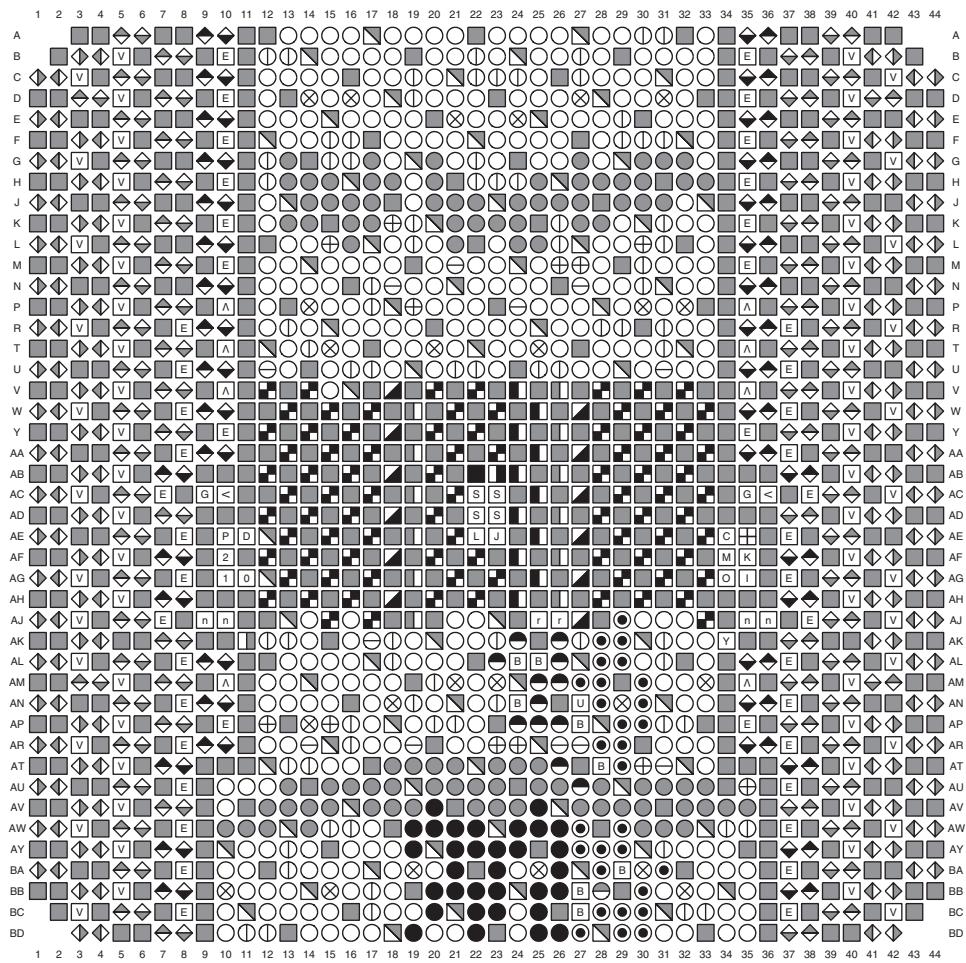
Figure 3-139: FF1926 and FFG1926 Packages—XC7VX690T and XC7VX980T Memory Groupings



ug475_c3_148_122811

Figure 3-140: FF1926 and FFG1926 Packages—XC7VX690T and XC7VX980T Power and GND Placement

FF1927 and FFG1927 Packages—XC7VX550T and XC7VX690T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
<ul style="list-style-type: none"> (○) IO_LXXY_# (○) IO_XX_# 	<ul style="list-style-type: none"> [E] MGTAVCC_G# [V] MGTAVTT_G# [A] MGTVCCAUX_G# [L] MGTAVITRICAL [G] MGTRREF [D] MGTRREFCLK1/IOP [D] MGTRREFCLK1/ON [F] MGTXRXP [F] MGTXRXN [F] MGTXXP [F] MGTXTN [E] MGTHAVCC_G# [V] MGTHAVTT_G# [D] MGTHRXP [D] MGTHRXN [F] MGHTXP [D] MGHTXN 	<ul style="list-style-type: none"> [C] CCLKL_0 [C] CFGBVS_0 [D] DONE_0 [J] DXP_0 [L] DXN_0 [C] GNDADC_0 [Y] INIT_B_0 [O] M0_0 [I] M1_0 [2] M2_0 [P] PROGRAM_B_0 [K] TCK_0 [I] TDI_0 [O] TDO_0 [M] TMS_0 [S] VP_0 [S] VN_0 [S] VREFP_0 [S] VREFN_0 	<ul style="list-style-type: none"> GND VCCAUX_IO_G# VCCAUX VCCINT VCCO_# VCCBRAM NC
Multi-Function Pins <ul style="list-style-type: none"> [B] ADV_B [B] FCS_B [B] FOE_B [B] MOSI [B] FWE_B [B] DOUT_CSO_B [B] CSI_B [B] PUDC_B [U] RDWR_B [I] RS0-RS1 [●] ADOP/AD0N-AD15P/AD15N [○] EMCCLK 			

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Figure 3-141: FF1927 and FFG1927 Packages—XC7VX550T and XC7VX690T Pinout Diagram

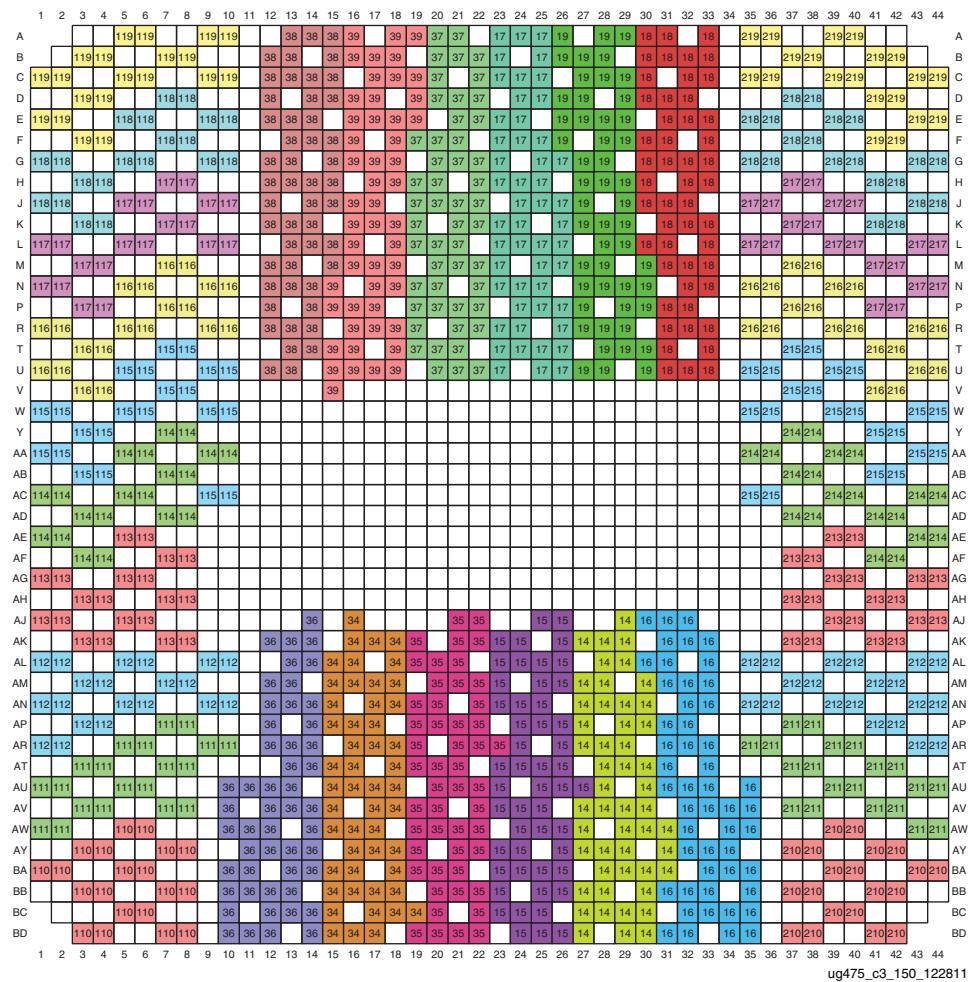
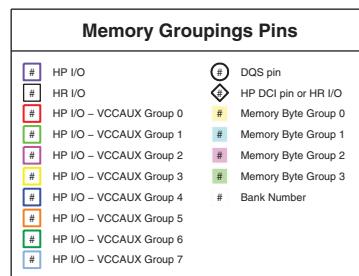
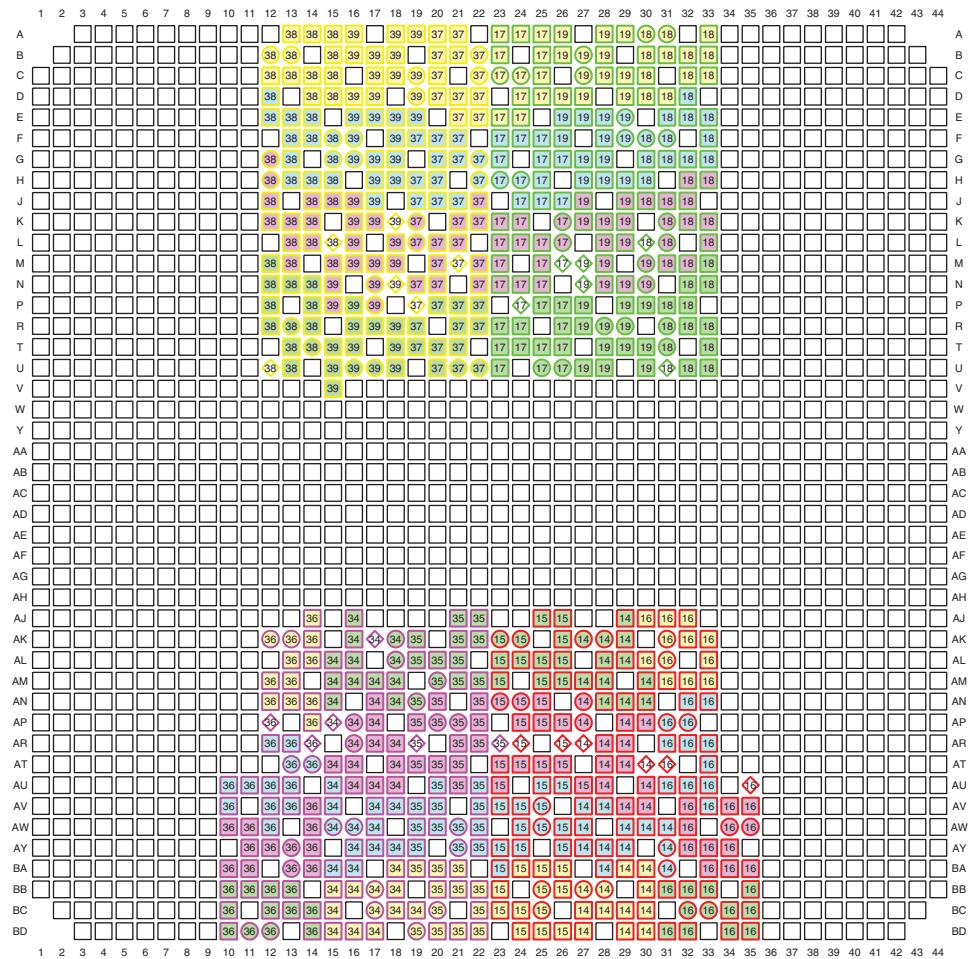
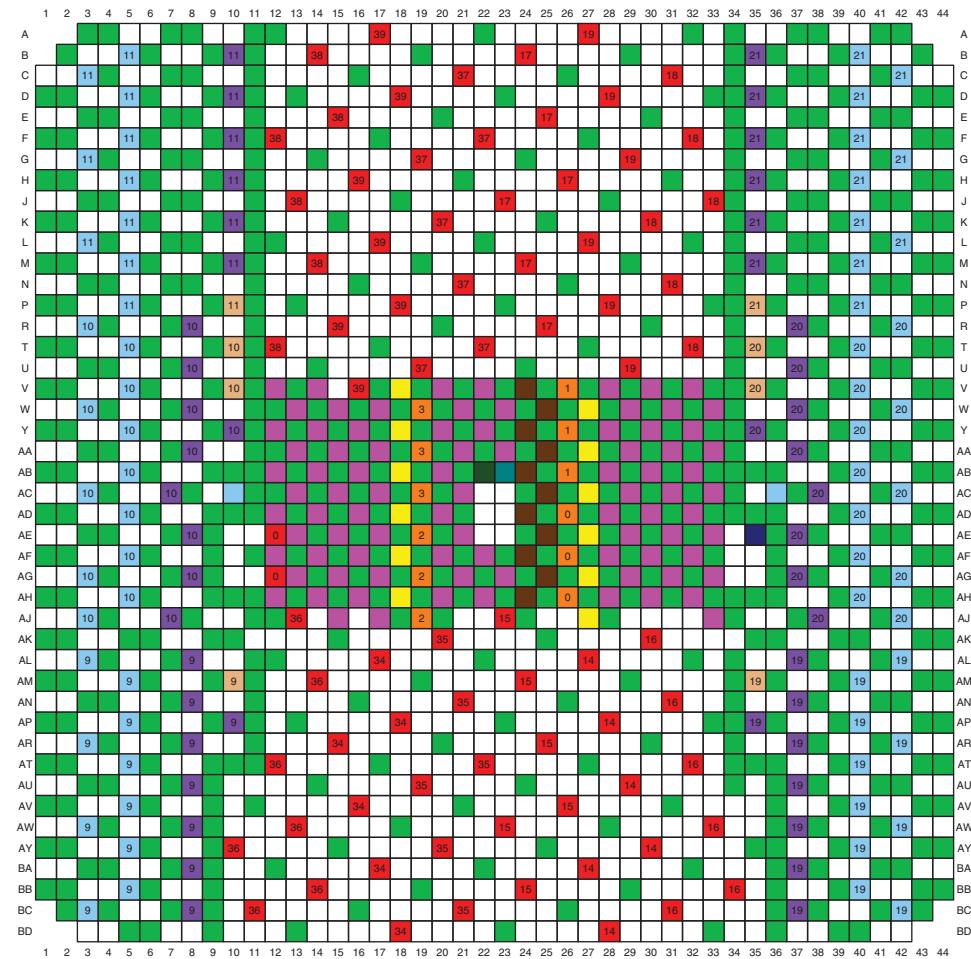


Figure 3-142: FF1927 and FFG1927 Packages—XC7VX550T and XC7VX690T I/O Banks



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Figure 3-143: FF1927 and FFG1927 Packages—XC7VX550T and XC7VX690T Memory Groupings

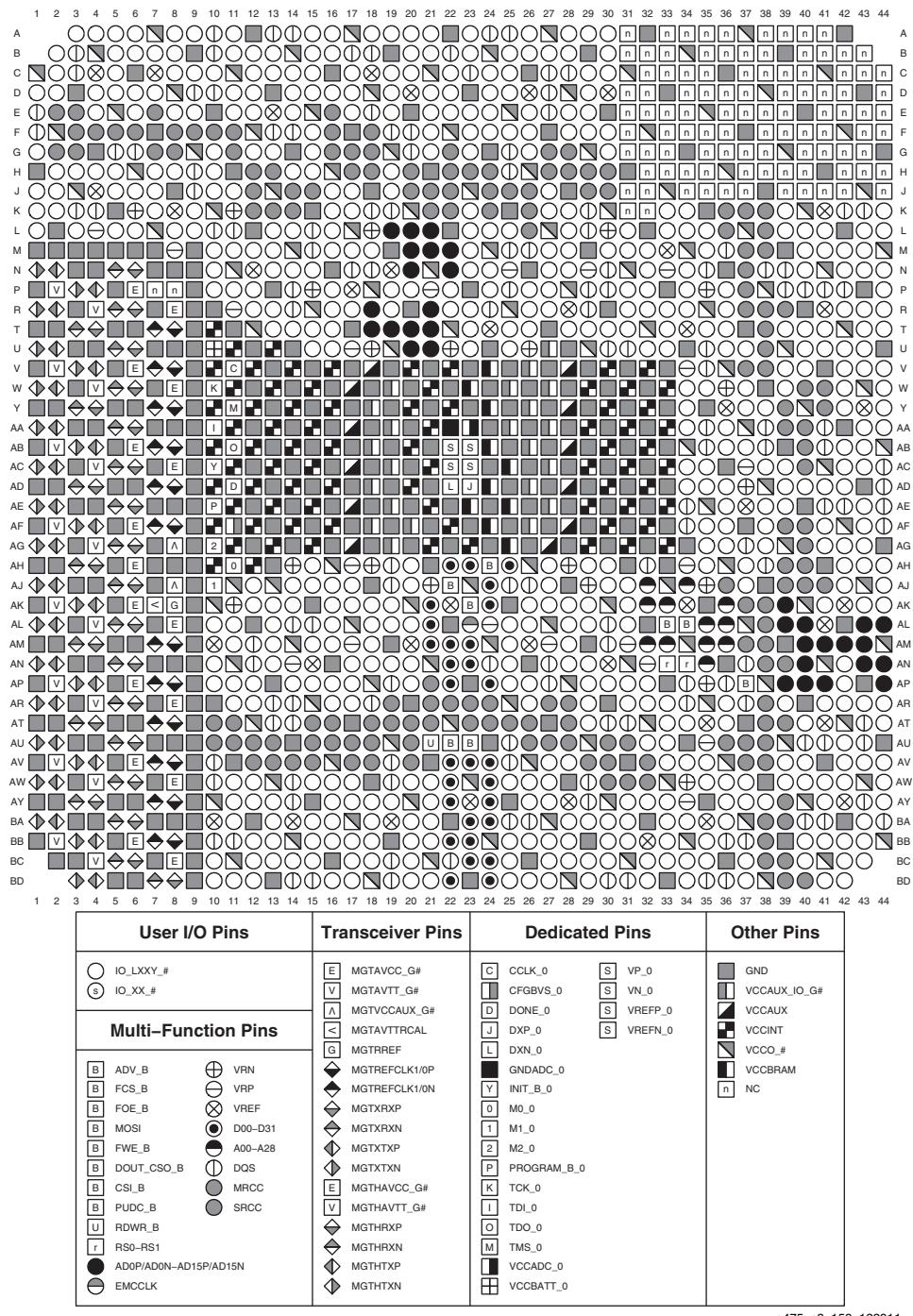


Power Pins	
■	VCCO_#
■	VCCINT
■	VCCAUX
■	VCCAUX_IO_G#
■	VCCBRAM
■	VCCBATT_0
■	VCCADC_0
■	GNDADC_0
■	MGTVCCAUX
■	MGTVCCAUX_G# or MGTHVCCAUX_G#
■	MGTAVCC
■	MGTAVCC_G# or MGTHAVCC_G#
■	MGTVTT
■	MGTAVT
■	MGTAVT_G# or MGTHAVTT_G#
■	GND

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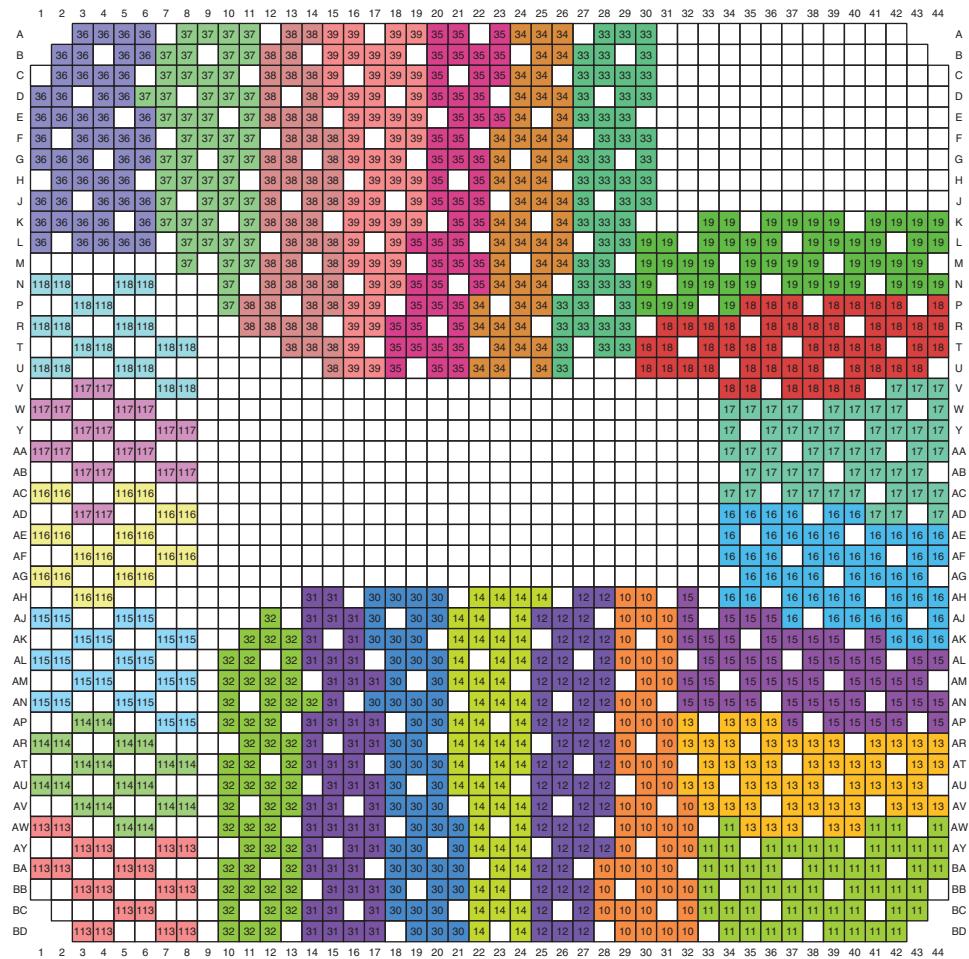
Figure 3-144: FF1927 and FFG1927 Packages—XC7VX550T and XC7VX690T Power and GND Placement

FF1930, FFG1930, and RF1930 Packages—XC7VX690T



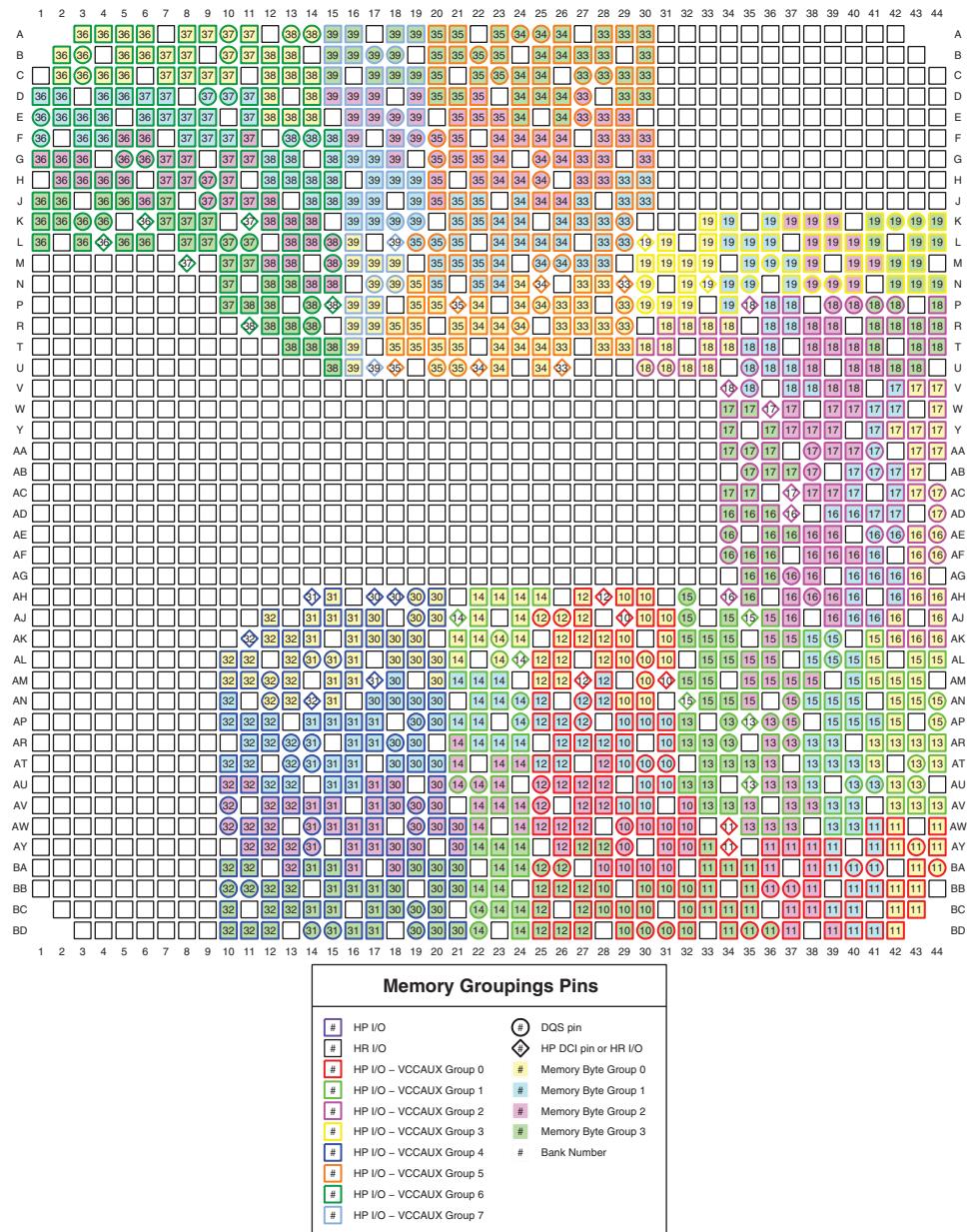
ug475_c3_153_122911

Figure 3-145: FF1930, FFG1930, and RF1930 Packages—XC7VX690T Pinout Diagram



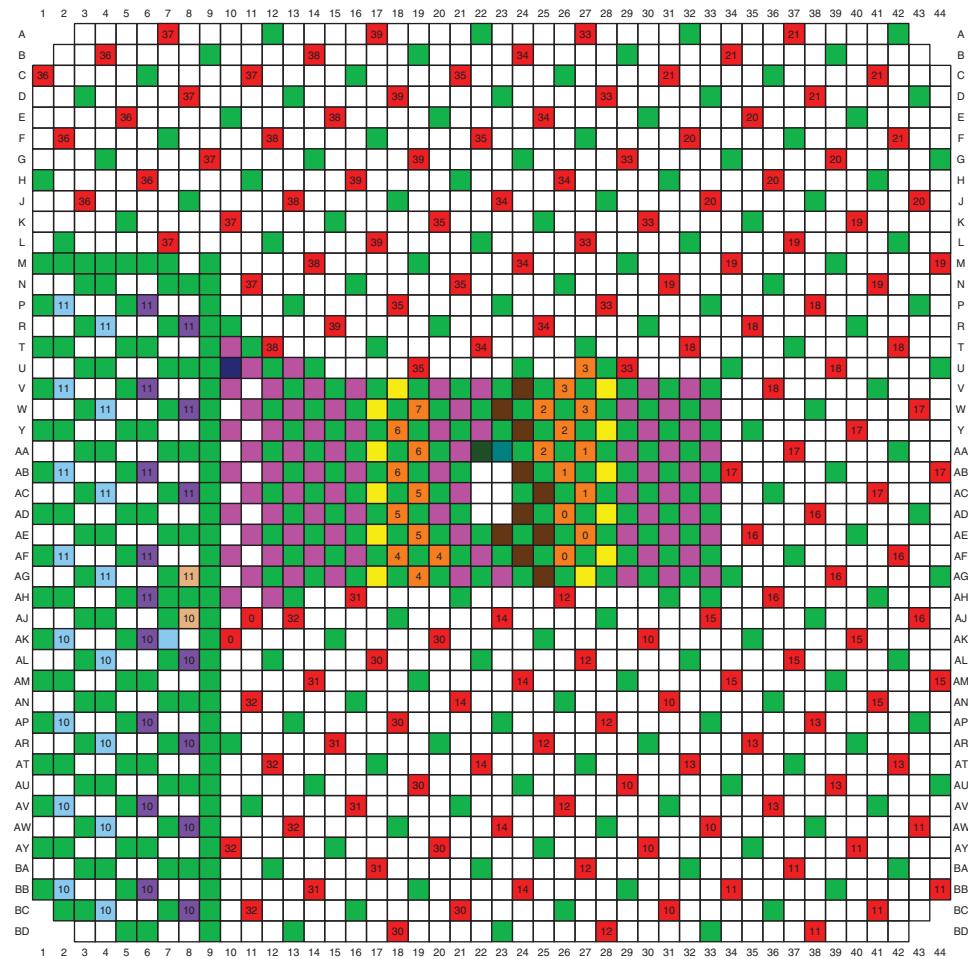
ug475_c3_154_122911

Figure 3-146: FF1930, FFG1930, and RF1930 Packages—XC7VX690T I/O Banks



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Figure 3-147: FF1930, FFG1930, and RF1930 Packages—XC7VX690T Memory Groupings

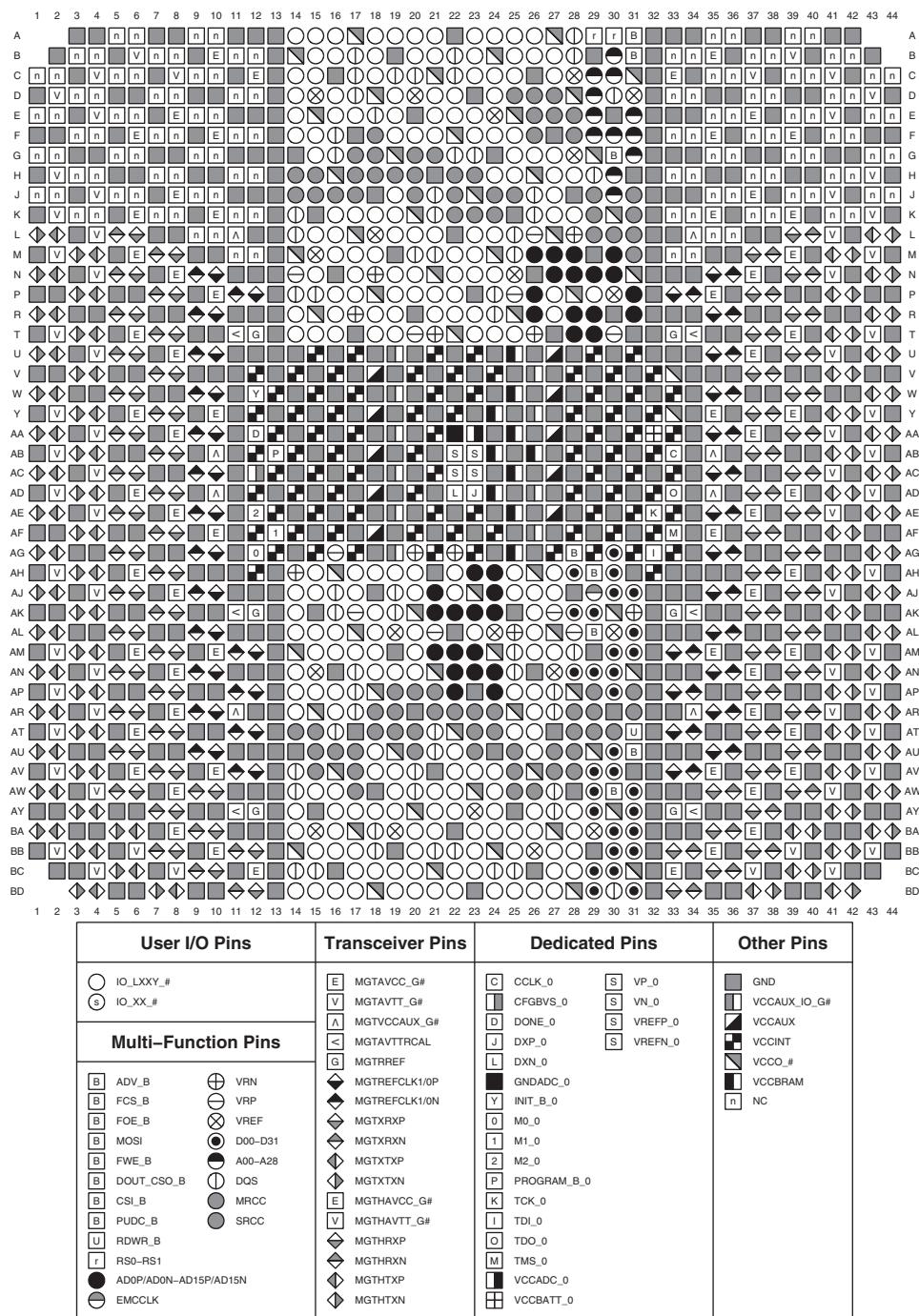


Power Pins	
	VCCO_#
	VCCINT
	VCCAUX
	MGTVCCAUX # MGTVCVAUX_G# or MGTHVCCAUX_G#
	VCCAUX_IO_G#
	VCCBRAM
	VCCBATT_0
	VCCADC_0
	GNDADC_0
	MGTAVCC # MGTAVCC_G# or MGTHAVCC_G#
	MGTAVTT
	MGTAVTT_G# or MGTHAVTT_G#
	GND

ug475_c3_156_122911

Figure 3-148: FF1930, FFG1930, and RF1930 Packages—XC7VX690T Power and GND Placement

FF1928 and FFG1928 Packages—XC7VX980T



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Figure 3-149: FF1928 and FFG1928 Packages—XC7VX980T Pinout Diagram

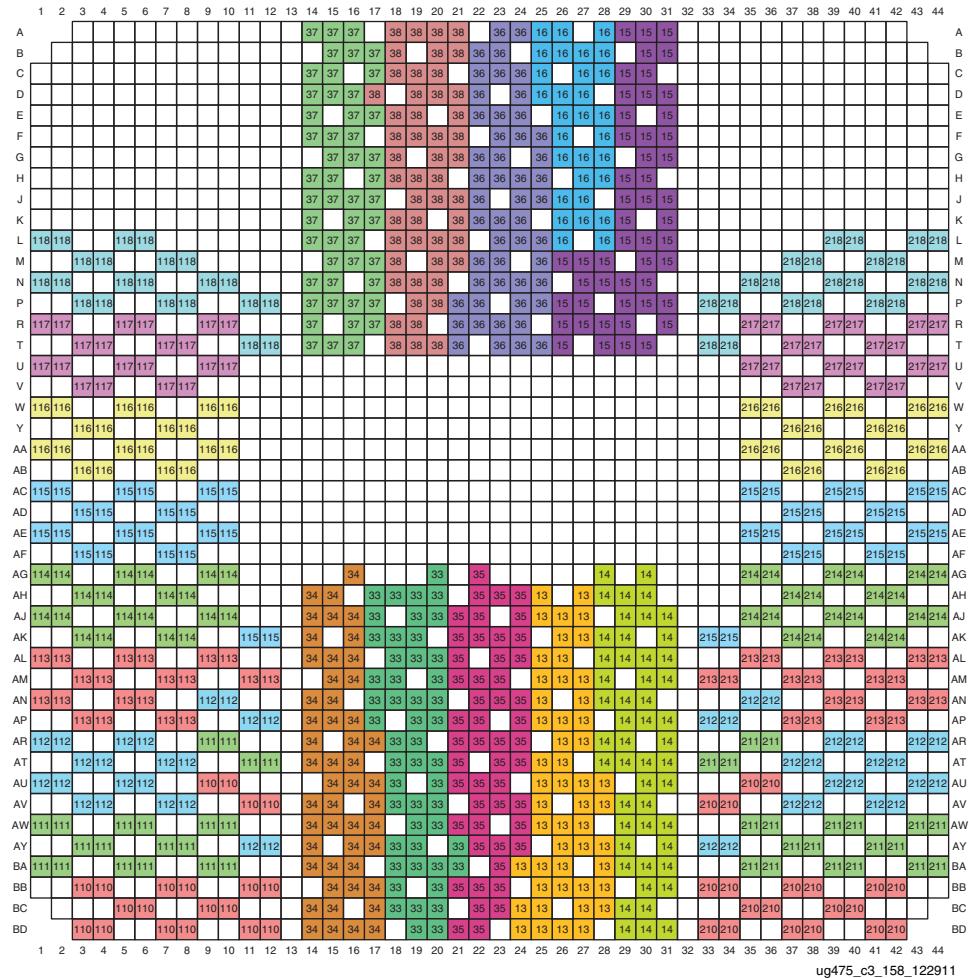
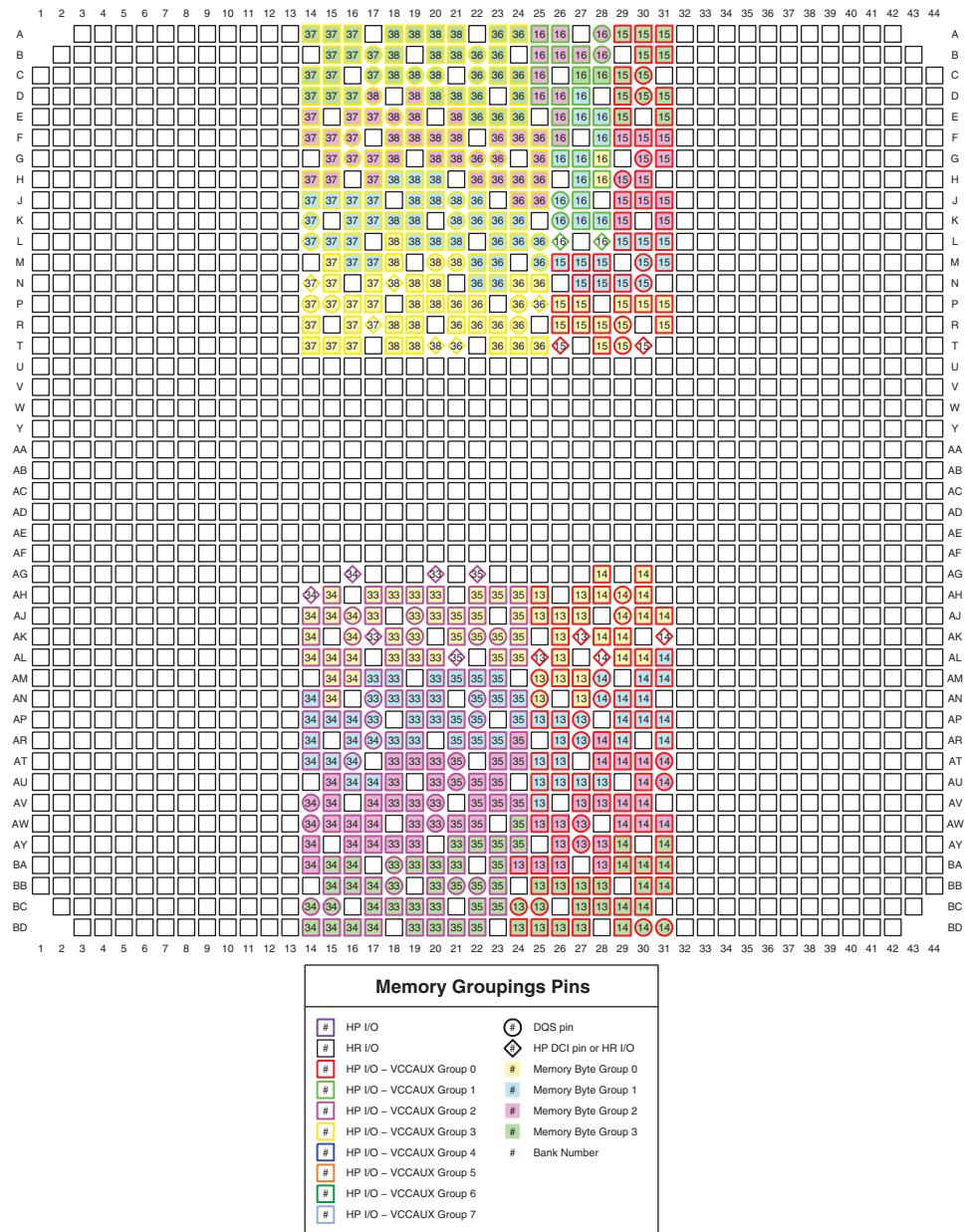
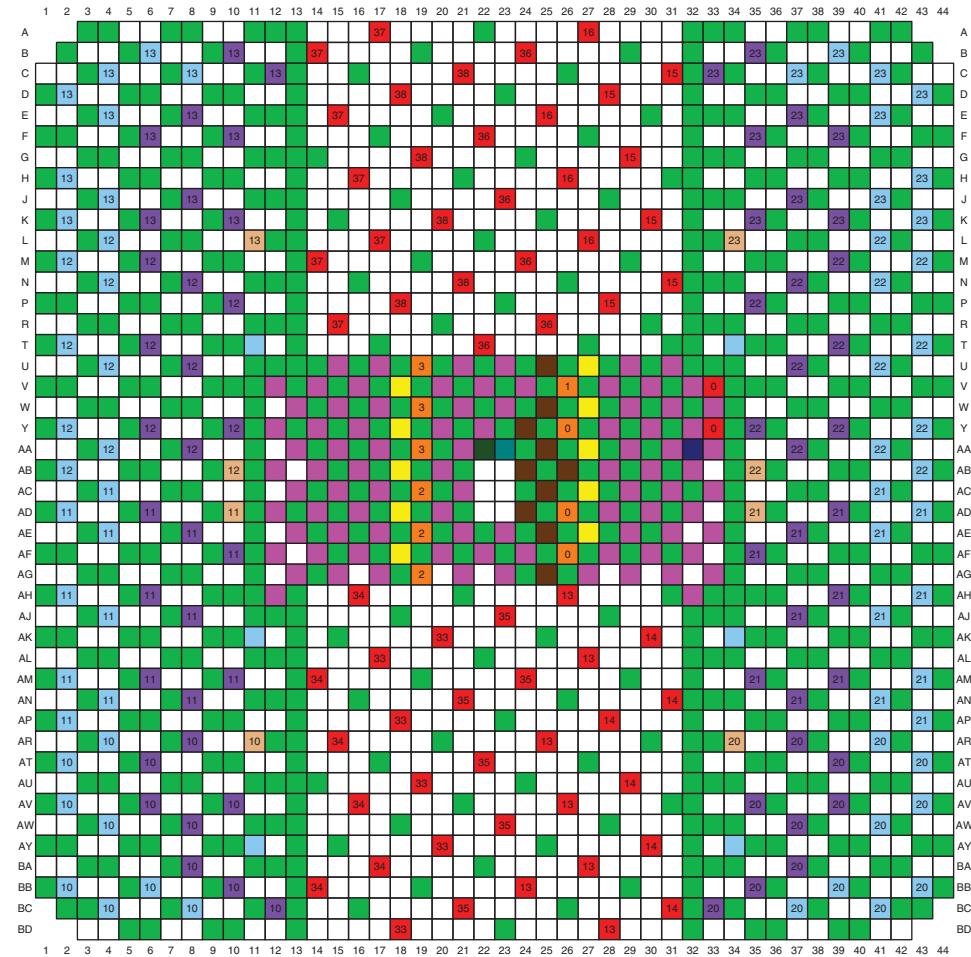


Figure 3-150: FF1928 and FFG1928 Packages—XC7VX980T I/O Banks



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Figure 3-151: FF1928 and FFG1928 Packages—XC7VX980T Memory Groupings



Power Pins	
VCCO_#	MGTVCCAUX
VCCINT	MGTVCCAUX_G# or MGTHVCCAUX_G#
VCCAUX	MGTAVCC
VCCAUX_IO_G#	MGTAVCC_G# or MGTHAVCC_G#
VCCBRAM	MGTAVTT
VCBATT_0	MGTAVTT_G# or MGTHAVTT_G#
VCCADC_0	GND
GNDADC_0	

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Figure 3-152: FF1928 and FFG1928 Packages—XC7VX980T Power and GND Placement

FF1930, FFG1930, and RF1930 Packages—XC7VX980T

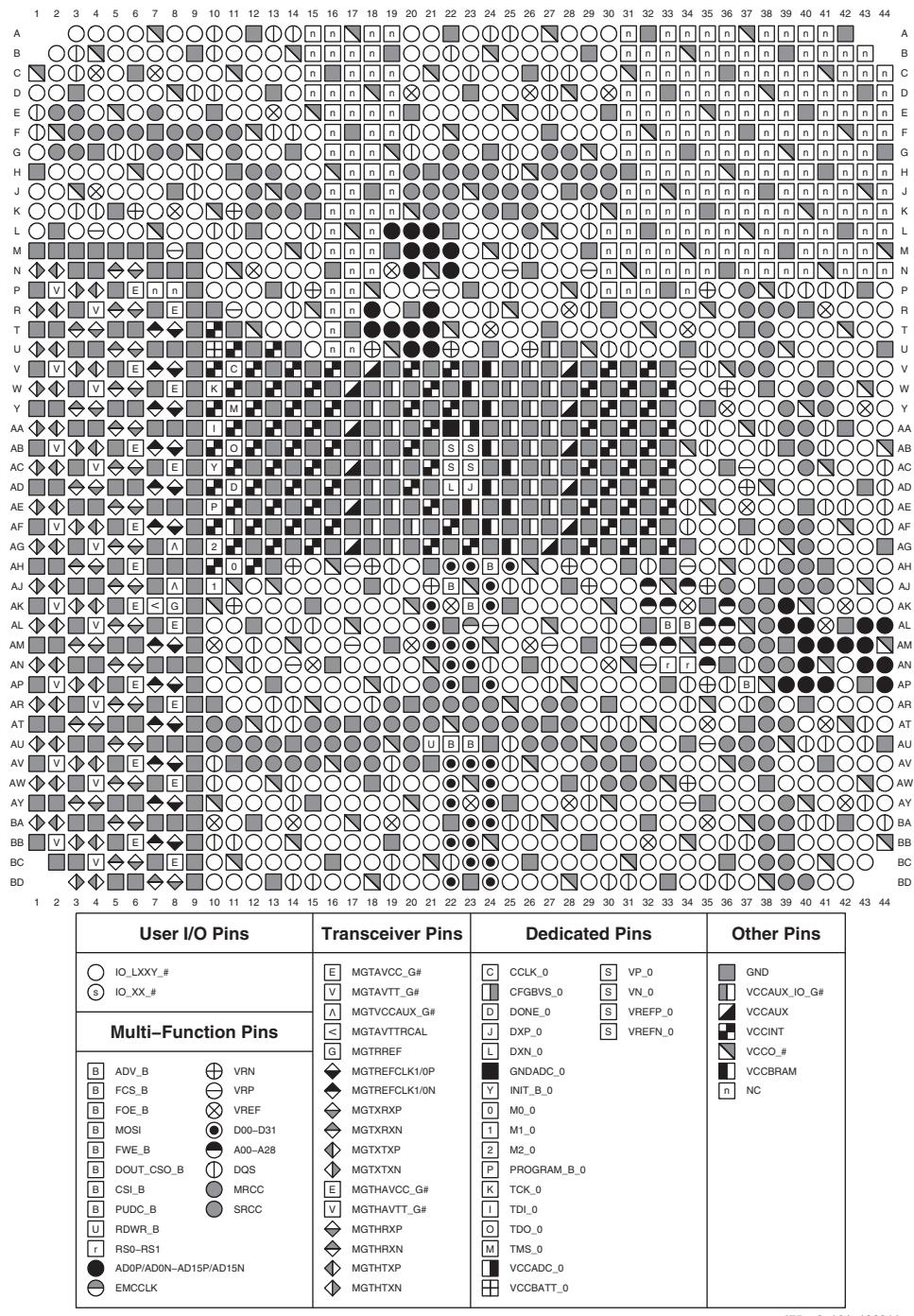
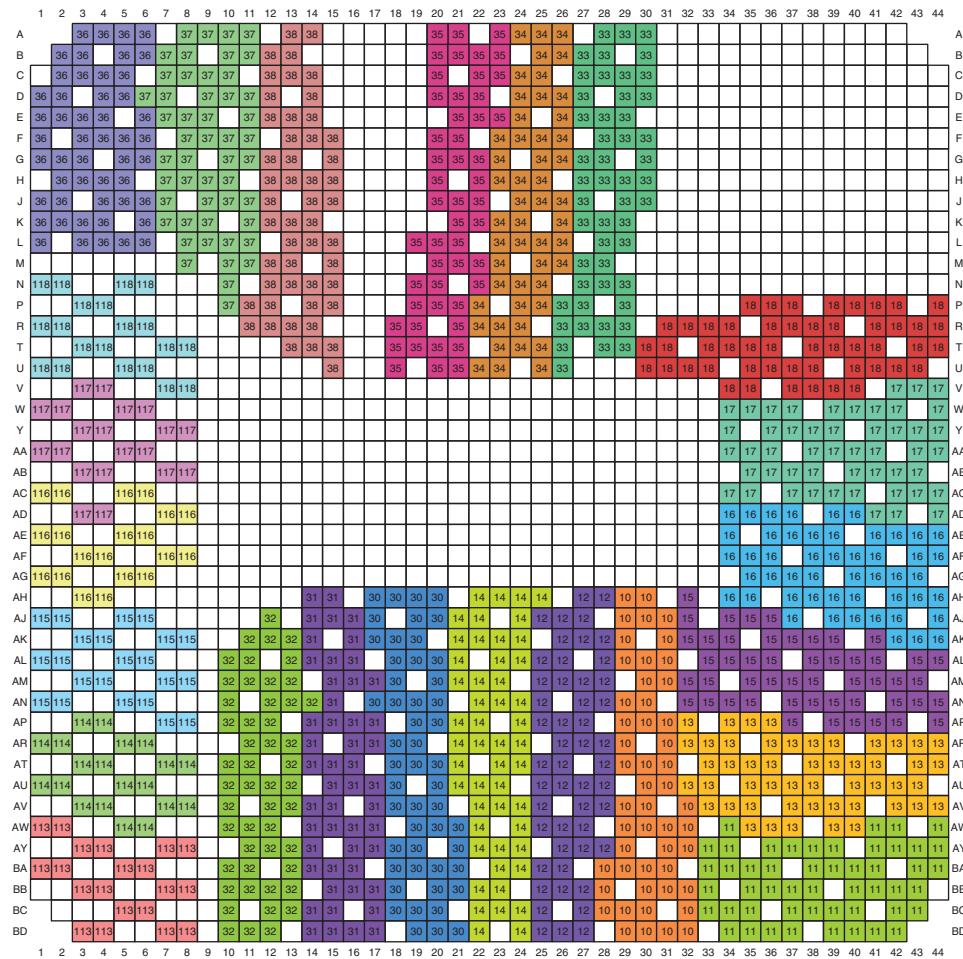


Figure 3-153: FF1930, FFG1930, and RF1930 Packages—XC7VX980T Pinout Diagram



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Figure 3-154: FF1930, FFG1930, and RF1930 Packages—XC7VX980T I/O Banks

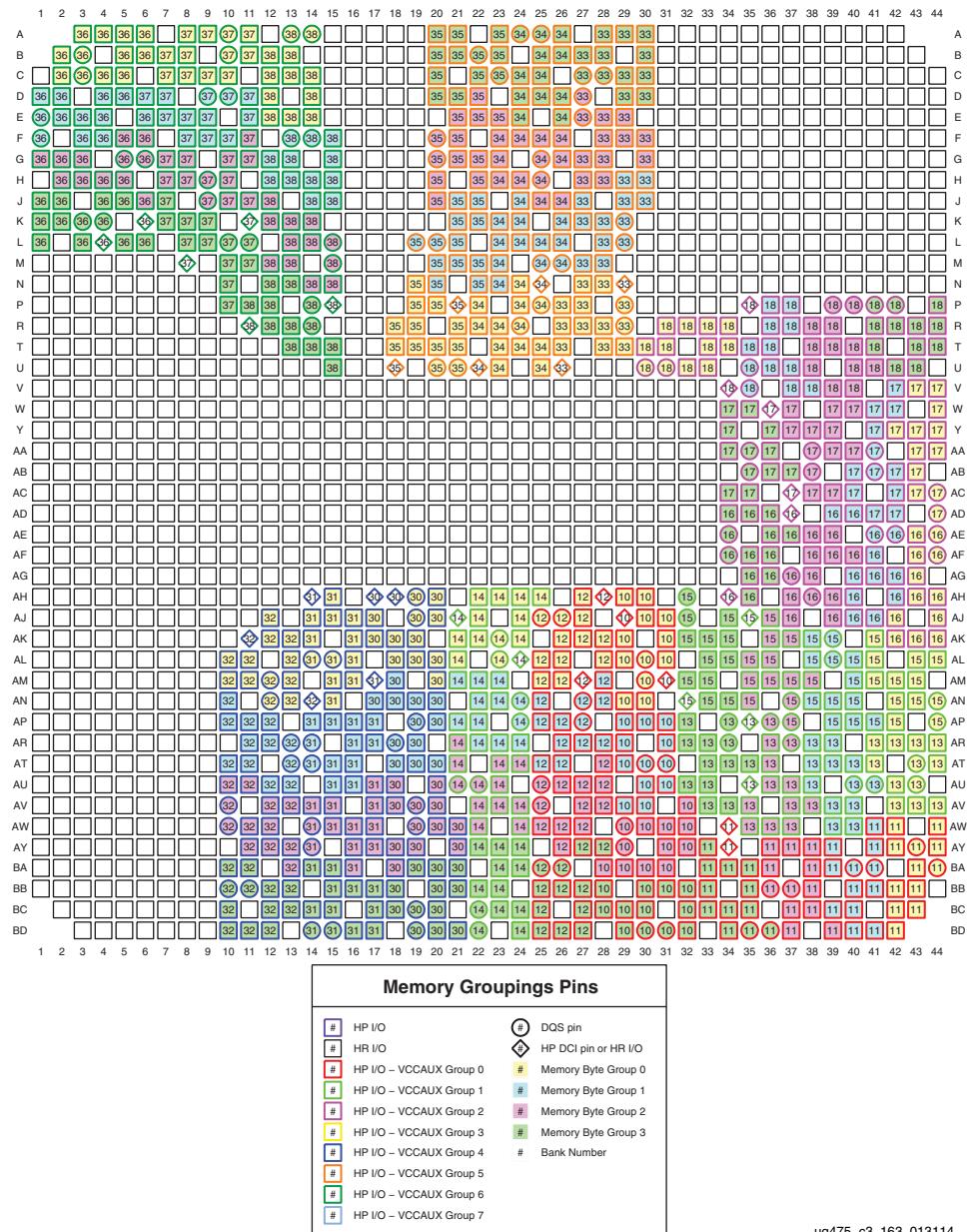
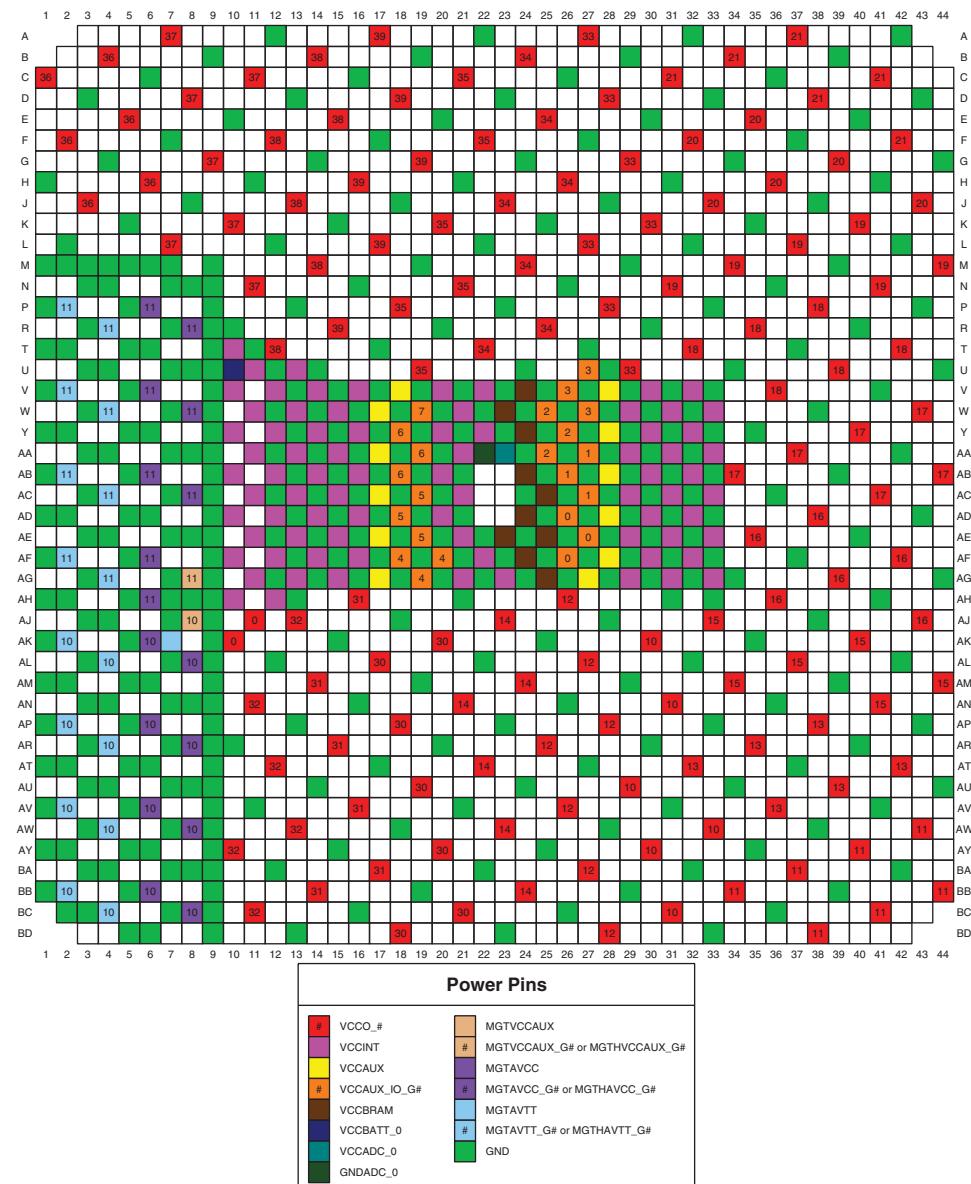


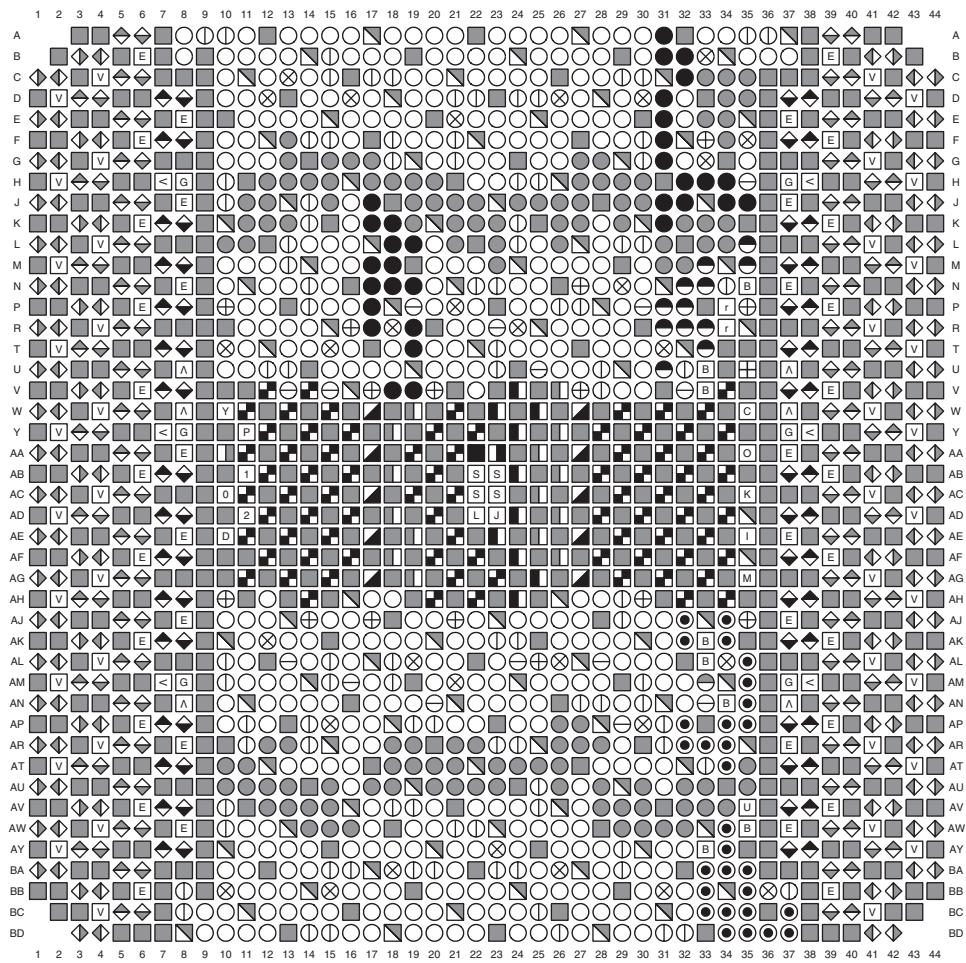
Figure 3-155: FF1930, FFG1930, and RF1930 Packages—XC7VX980T Memory Groupings



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Figure 3-156: FF1930, FFG1930, and RF1930 Packages—XC7VX980T Power and GND Placement

FL1926 and FLG1926 Packages—XC7VX1140T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
<ul style="list-style-type: none"> (○) IO_LXXY_# (○) IO_XX_# 	<ul style="list-style-type: none"> [E] MGTAVCC_G# [V] MGTAVTT_G# [A] MGTVCVAUX_G# [MGTAVITRICAL] [G] MGTRREF [△] MGTRREFCLK1/0P [◆] MGTRREFCLK1/0N [◆] MGTXRXP [◆] MGTXRXN [◆] MGTXTXP [◆] MGTXTXN [E] MGTHAVCC_G# [V] MGTHAVTT_G# [△] MGTHRXP [◆] MGTHRXP [◆] MGTHTXP [◆] MGHTHDXN 	<ul style="list-style-type: none"> [C] CCLK_0 [V] CFGBVS_0 [A] DONE_0 [J] DXP_0 [L] DXN_0 [Y] INIT_B_0 [0] M0_0 [1] M1_0 [2] M2_0 [P] PROGRAM_B_0 [K] TCK_0 [I] TDI_0 [O] TDO_0 [M] TMS_0 [■] VCCADC [+/-] VCCBATT_0 	<ul style="list-style-type: none"> [■] GND [■] VCCAUX_IO_G# [■] VCCAUX [■] VCCINT [■] VCCO_# [■] VCCBRAM [n] NC
<h3>Multi-Function Pins</h3> <ul style="list-style-type: none"> [B] ADV_B [B] FCS_B [B] FOE_B [B] MOSI [B] FWE_B [B] DOUT_CS0_B [B] CSI_B [B] PUDC_B [U] RDWR_B [r] RS0-RS1 [●] ADOP/AD0N-AD15P/AD15N [○] EMCCLK 			

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Figure 3-157: FL1926 and FLG1926 Packages—XC7VX1140T Pinout Diagram

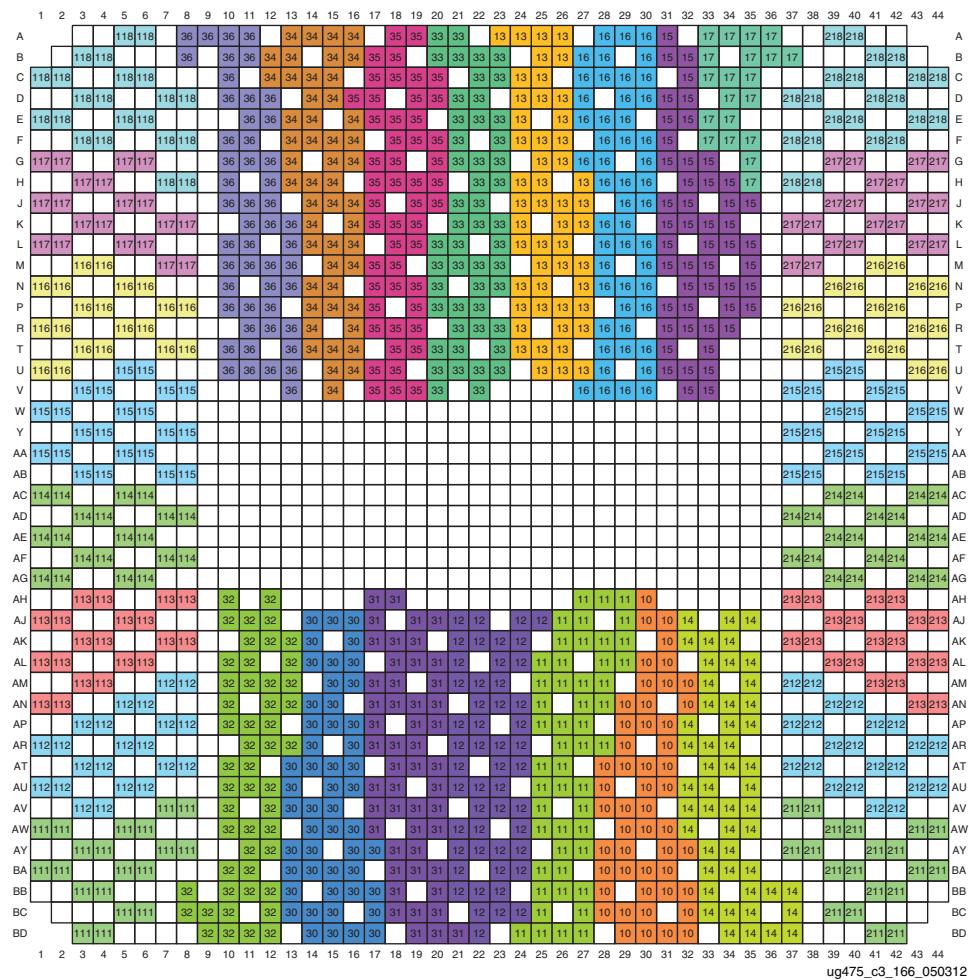
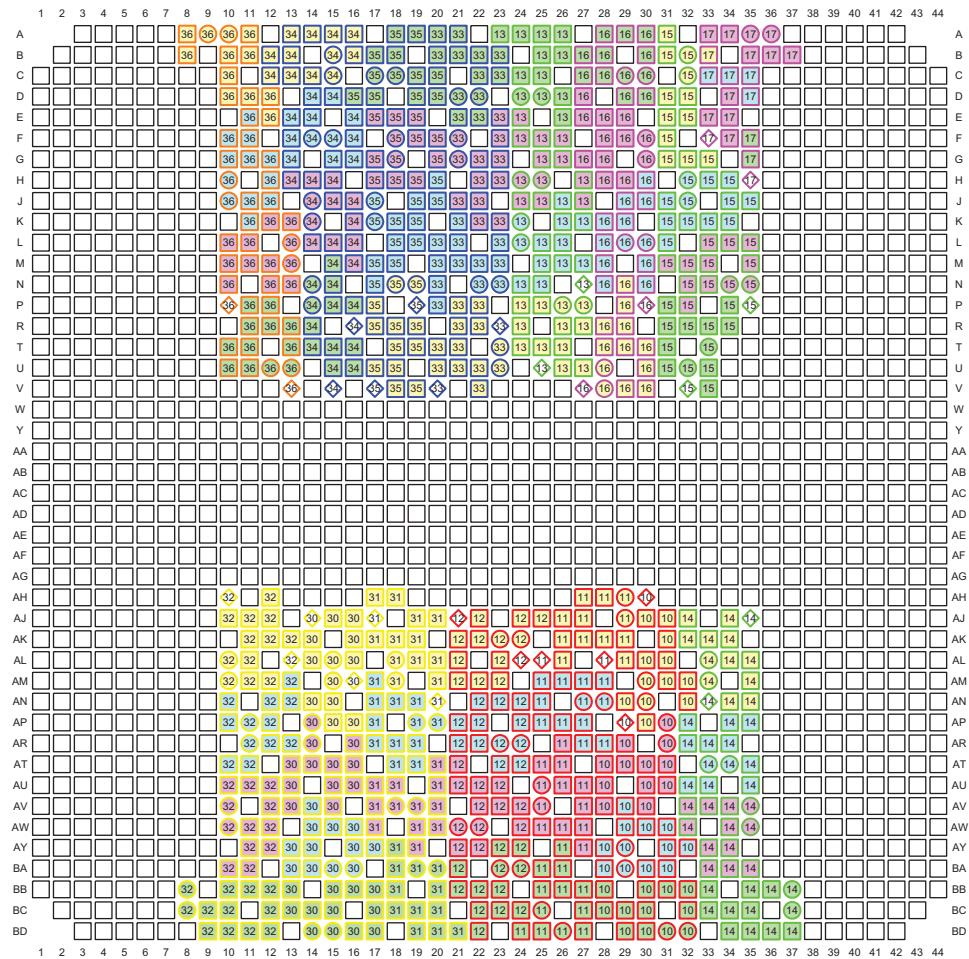


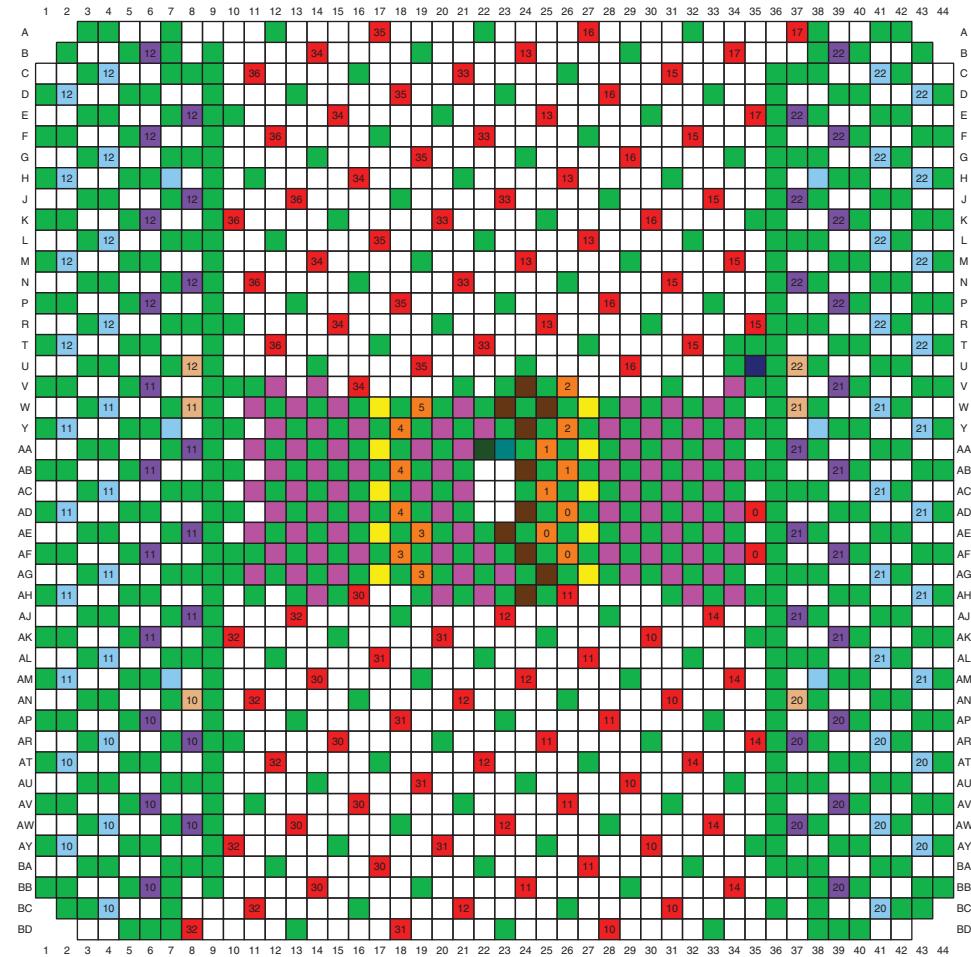
Figure 3-158: FL1926 and FLG1926 Packages—XC7VX1140T I/O Banks



Memory Groupings Pins															
#	HP I/O	#	DQS pin												
#	HR I/O	#	HP DCI pin or HR I/O												
#	HP I/O – VCCAUX Group 0	#	Memory Byte Group 0												
#	HP I/O – VCCAUX Group 1	#	Memory Byte Group 1												
#	HP I/O – VCCAUX Group 2	#	Memory Byte Group 2												
#	HP I/O – VCCAUX Group 3	#	Memory Byte Group 3												
#	HP I/O – VCCAUX Group 4	#	Bank Number												
#	HP I/O – VCCAUX Group 5														
#	HP I/O – VCCAUX Group 6														
#	HP I/O – VCCAUX Group 7														

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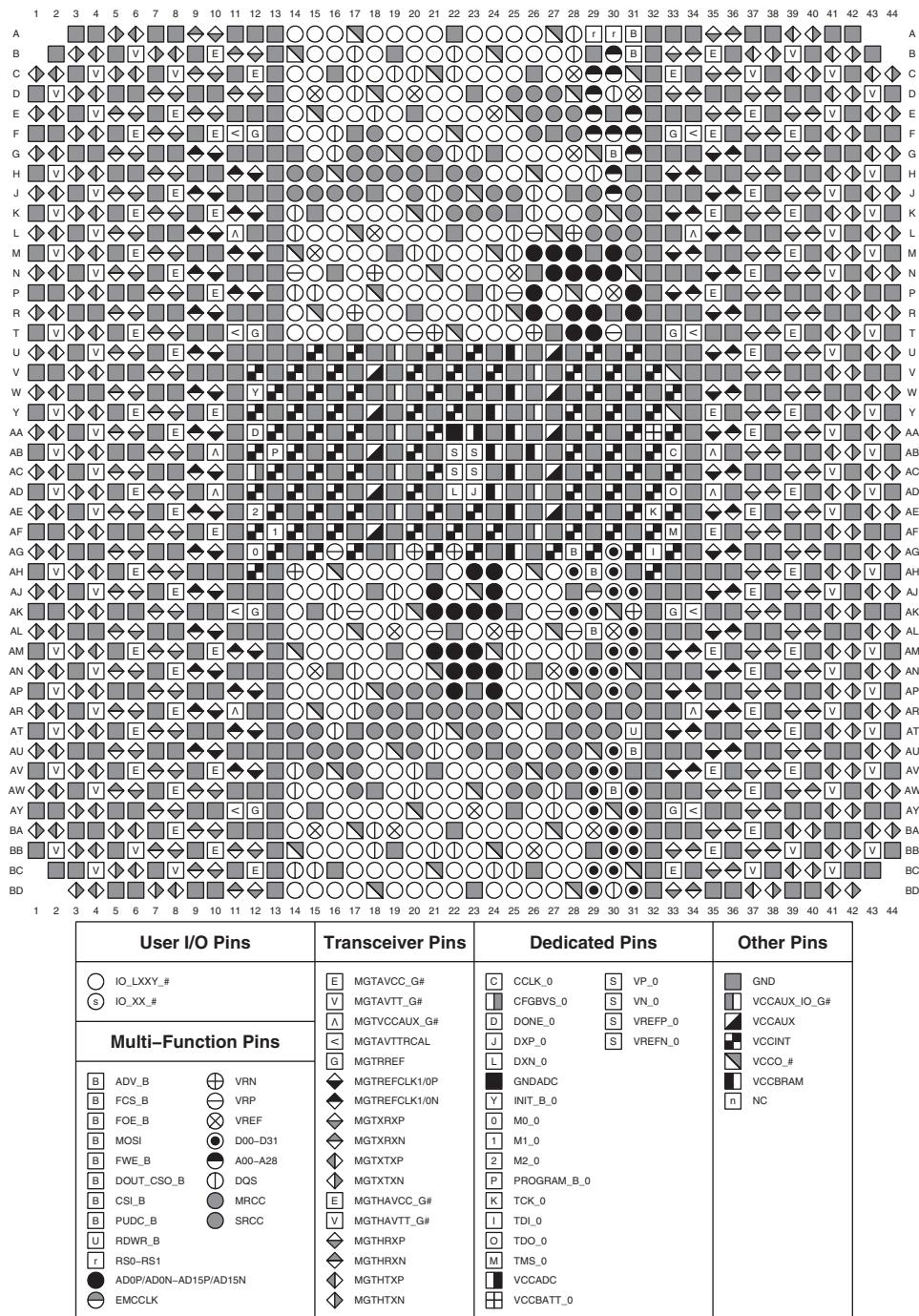
Figure 3-159: FL1926 and FLG1926 Packages—XC7VX1140T Memory Groupings



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Figure 3-160: FL1926 and FLG1926 Packages—XC7VX1140T Power and GND Placement

FL1928 and FLG1928 Packages—XC7VX1140T



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Figure 3-161: FL1928 and FLG1928 Packages—XC7VX1140T Pinout Diagram

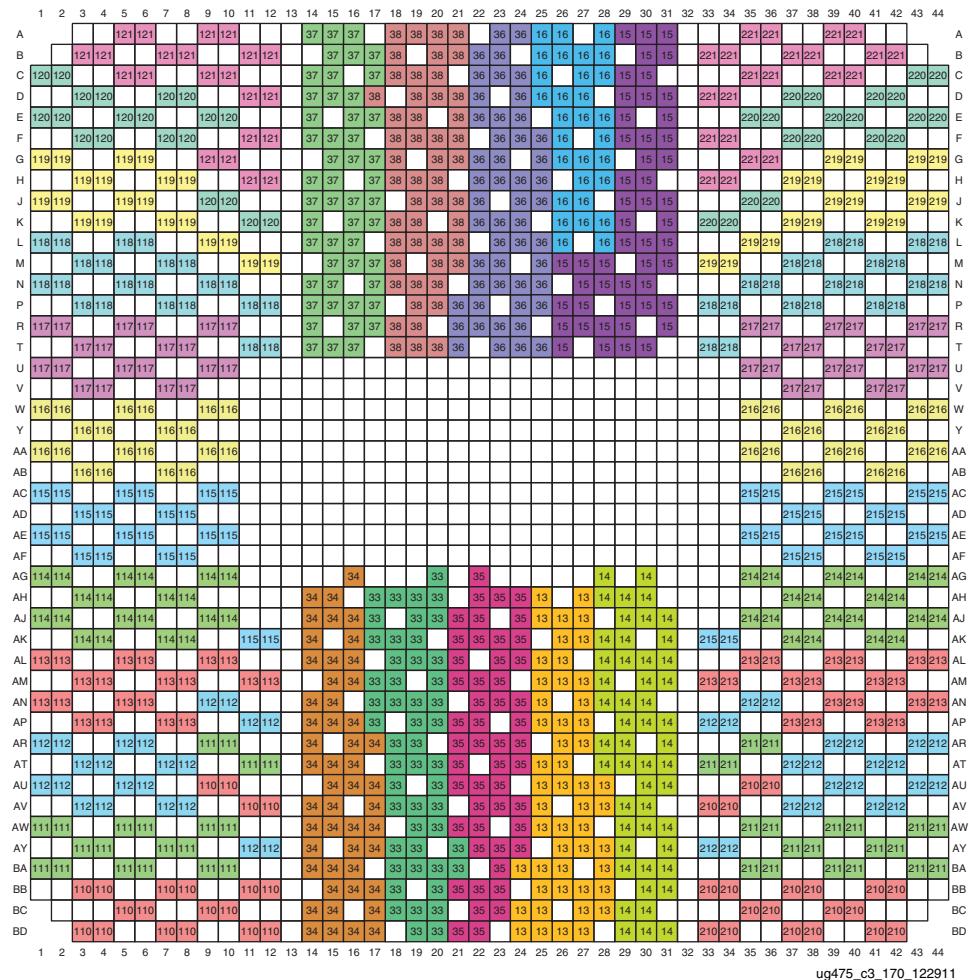
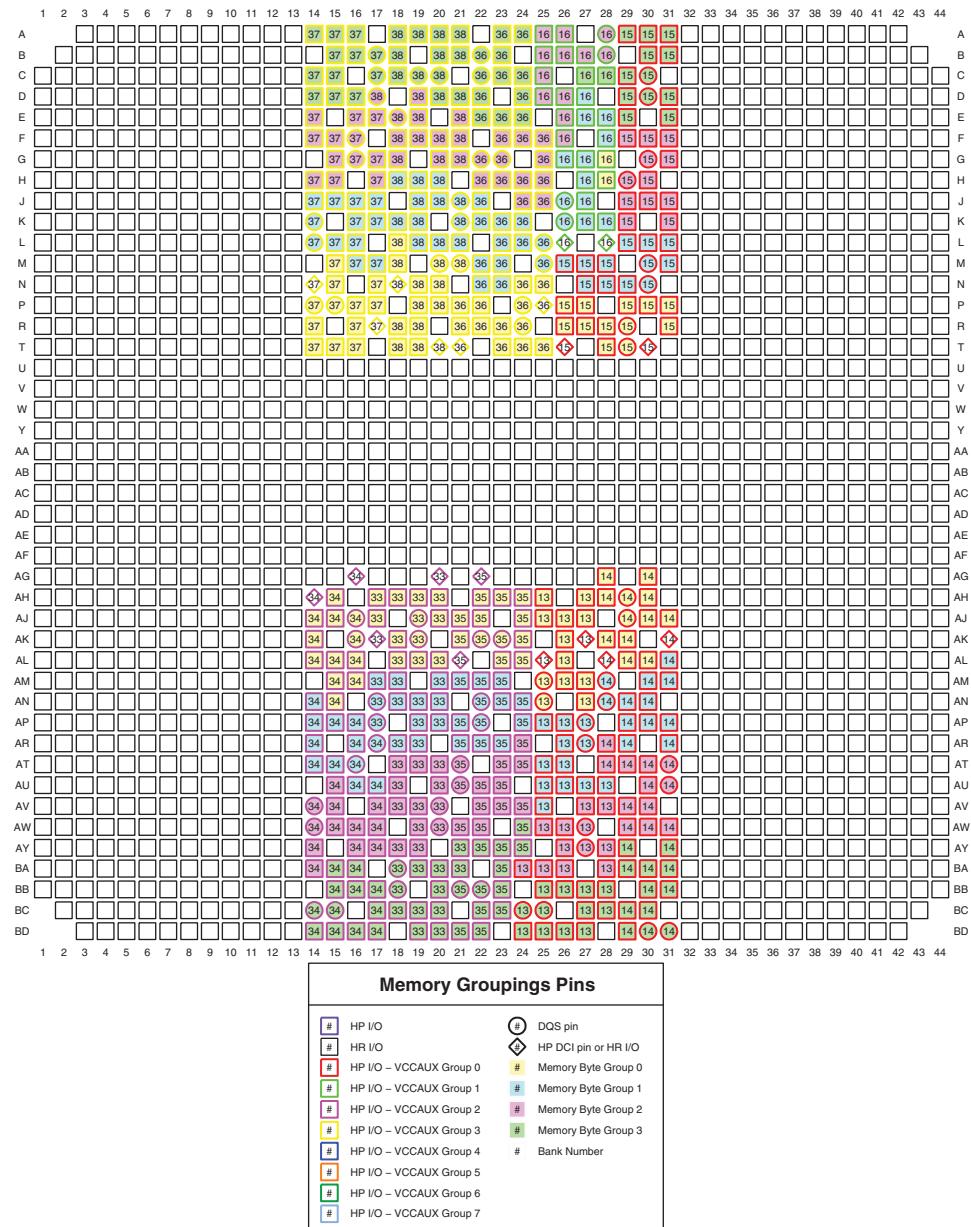
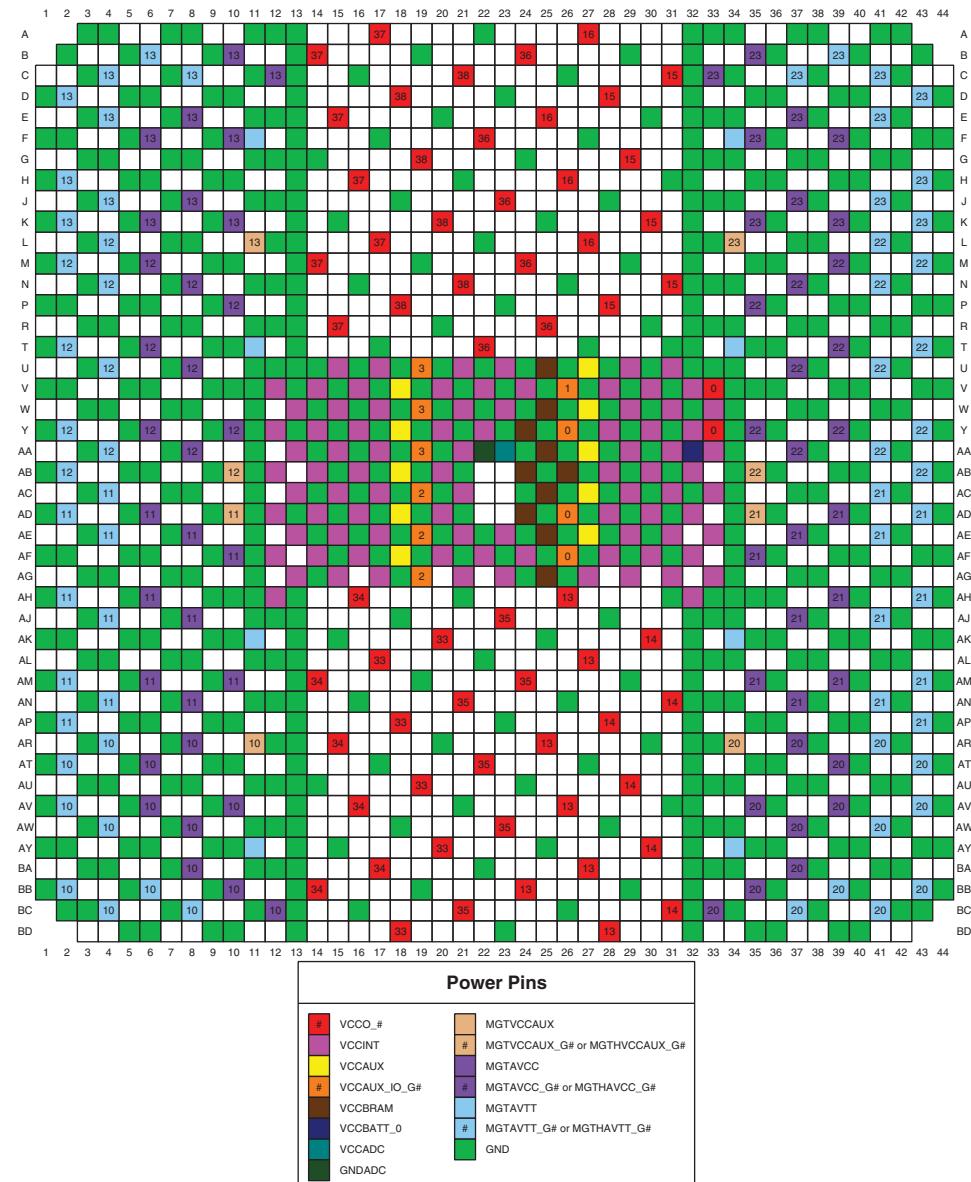


Figure 3-162: FL1928 and FLG1928 Packages—XC7VX1140T I/O Banks



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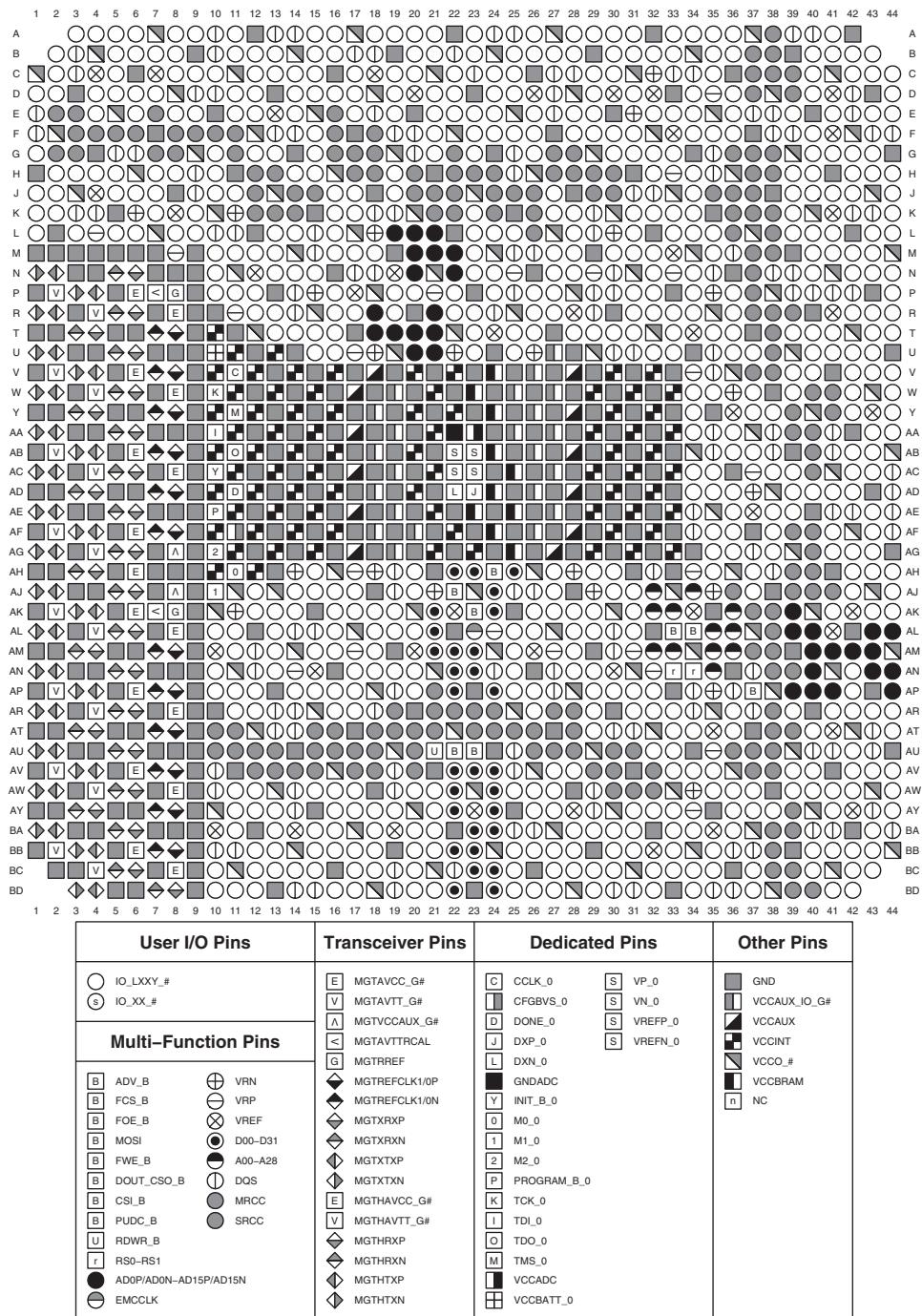
Figure 3-163: FL1928 and FLG1928 Packages—XC7VX1140T Memory Groupings



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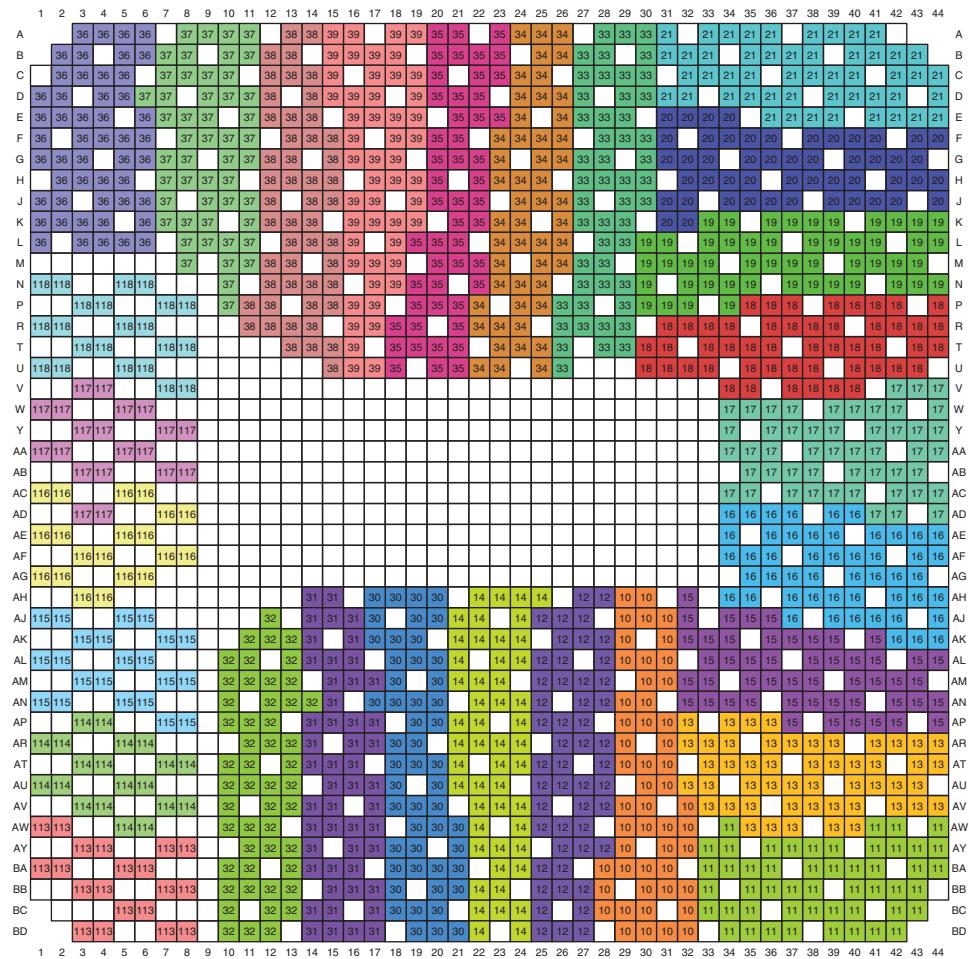
Figure 3-164: FL1928 and FLG1928 Packages—XC7VX1140T Power and GND Placement

FL1930 and FLG1930 Packages—XC7VX1140T



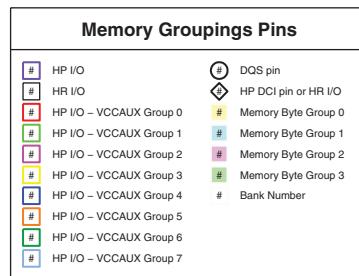
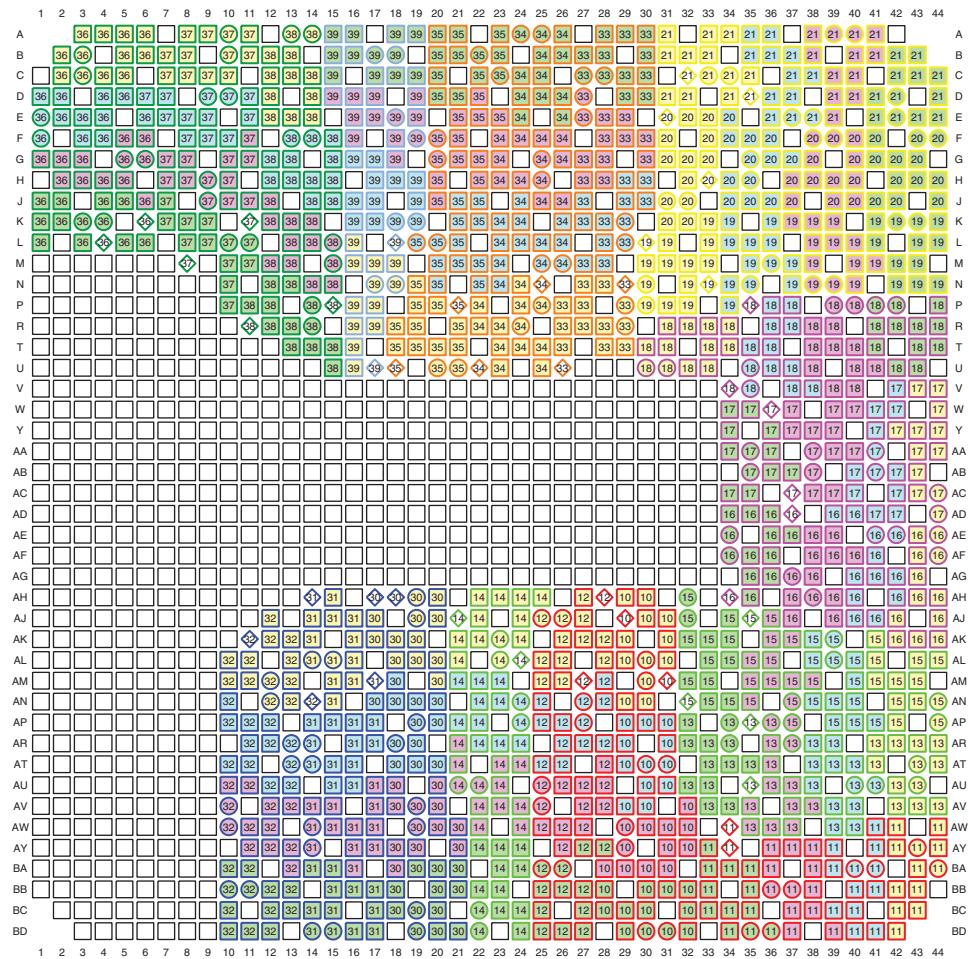
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Figure 3-165: FL1930 and FLG1930 Packages—XC7VX1140T Pinout Diagram



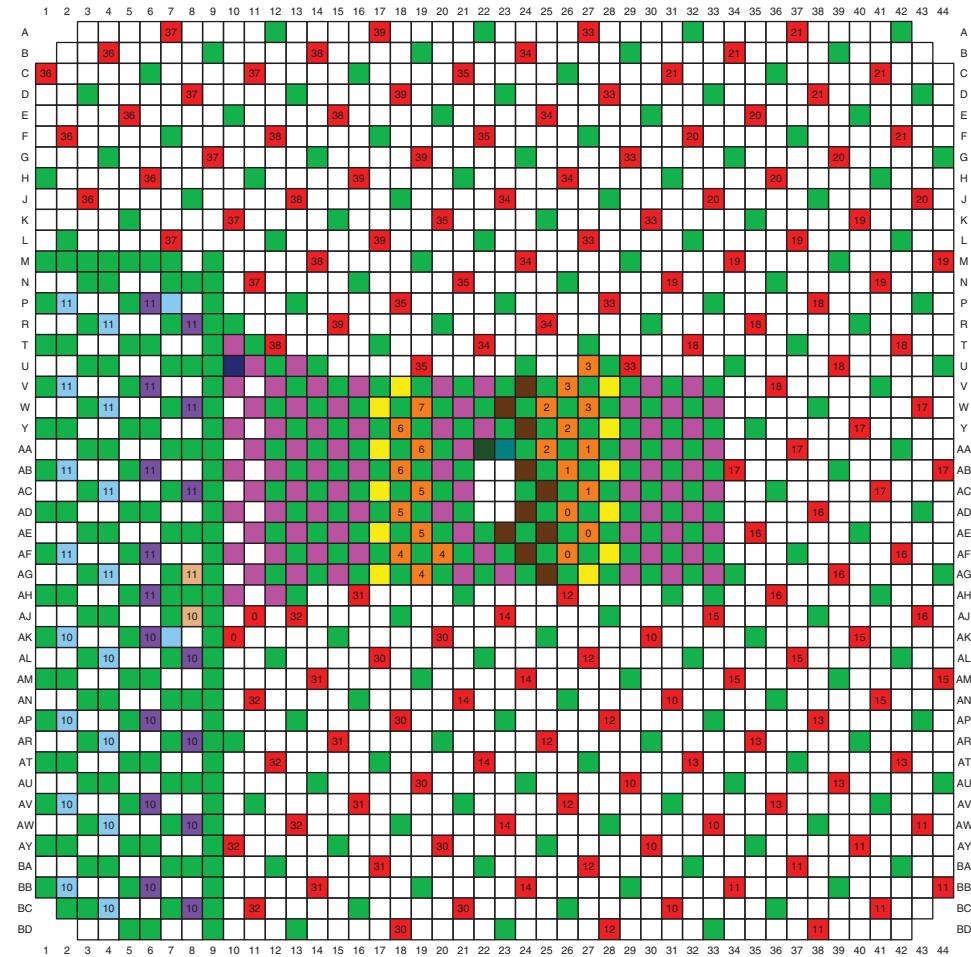
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Figure 3-166: FL1930 and FLG1930 Packages—XC7VX1140T I/O Banks



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Figure 3-167: FL1930 and FLG1930 Packages—XC7VX1140T Memory Groupings



Power Pins	
■	VCCO_#
■	MGTVCCAUX
■	MGTVCCAUX_G# or MGTHVCCAUX_G#
■	MGTAVCC
■	MGTAVCC_G# or MGTHAVCC_G#
■	MGTAVT
■	MGTAVT_G# or MGTHAVTT_G#
■	GND

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Figure 3-168: FL1930 and FLG1930 Packages—XC7VX1140T Power and GND Placement

Mechanical Drawings

Summary

This chapter provides mechanical drawings (package specifications) of the following 7 series FPGA packages.

Artix-7 FPGAs

- CP236 and CPG236 (Artix-7 FPGAs) Wire-Bond Chip-Scale BGA (0.5 mm Pitch),
page 217
- CS/CSG324 and CS/CSG325 (Artix-7 FPGAs) Wire-Bond Chip-Scale BGA (0.8 mm Pitch), page 218
- FT/FTG256 (Artix-7 FPGAs) Wire-Bond Fine-Pitch Thin BGA (1.0 mm Pitch),
page 219
- SB484, SBG484, and SBV484 (Artix-7 FPGAs) Flip-Chip Lidless BGA (0.8 mm Pitch),
page 220
- FB484, FBG484, and FBV484 (Artix-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch),
page 221
 - XC7A200T FB484, FBG484, and FBV484 Die Dimensions, page 222
- FB676, FBG676, and FBV676 (Artix-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch),
page 223
 - XC7A200T FB676, FBG676, and FBV676 Die Dimensions, page 224
- FG484 and FGG484 (Artix-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch),
page 225
- FG676 and FGG676 (Artix-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch),
page 226
- FF1156, FFG1156, and FFV1156 (Artix-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch),
page 227
- RB484 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA (1.0 mm Pitch), page 228
- RS484 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA (0.8 mm Pitch), page 229
- RB676 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA (1.0 mm Pitch), page 230

Kintex-7 FPGAs

- FB484, FBG484, and FBV484 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch), page 231
 - XC7K70T FB484, FBG484, and FBV484 Die Dimensions with Capacitor Locations, page 232
 - XC7K160T FB484, FBG484, and FBV484 Die Dimensions with Capacitor Locations, page 233
- FB676, FBG676, and FBV676 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch), page 234
 - XC7K70T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations, page 235
 - XC7K160T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations, page 236
 - XC7K325T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations, page 237
 - XC7K410T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations, page 238
- FB900, FBG900, and FBV900 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch), page 239
 - XC7K325T FB900, FBG900, and FBV900 Die Dimensions with Capacitor Locations, page 240
 - XC7K410T FB900, FBG900, and FBV900 Die Dimensions with Capacitor Locations, page 241
- FF676, FFG676, and FFV676 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 242
- FF900, FFG900, FFV900, FF901, FFG901, and FFV901 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 243
- FF1156, FFG1156, and FFV1156 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 244
- RF676 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 245
- RF900 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 246

Virtex-7 FPGAs

- FF1157, FFG1157, FFV1157, FF1158, FFG1158, and FFV1158 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 247
- FF1761 and FFG1761 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 248
- FFV1761 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 249
- FH1761 and FHG1761 (Virtex-7 T FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 250
- FF1926, FFG1926, FF1927, FFG1927, FFV1927, FF1928, FFG1928, FF1930, and FFG1930 (Virtex-7 XT FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 251
- FL1925, FLG1925, FL1926, FLG1926, FL1928, FLG1928, and FL1930, FLG1930 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 252
- RF1157 and RF1158 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch), page 253
- RF1761 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch), page 254
- RF1930 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch), page 255

CP236 and CPG236 (Artix-7 FPGAs) Wire-Bond Chip-Scale BGA (0.5 mm Pitch)

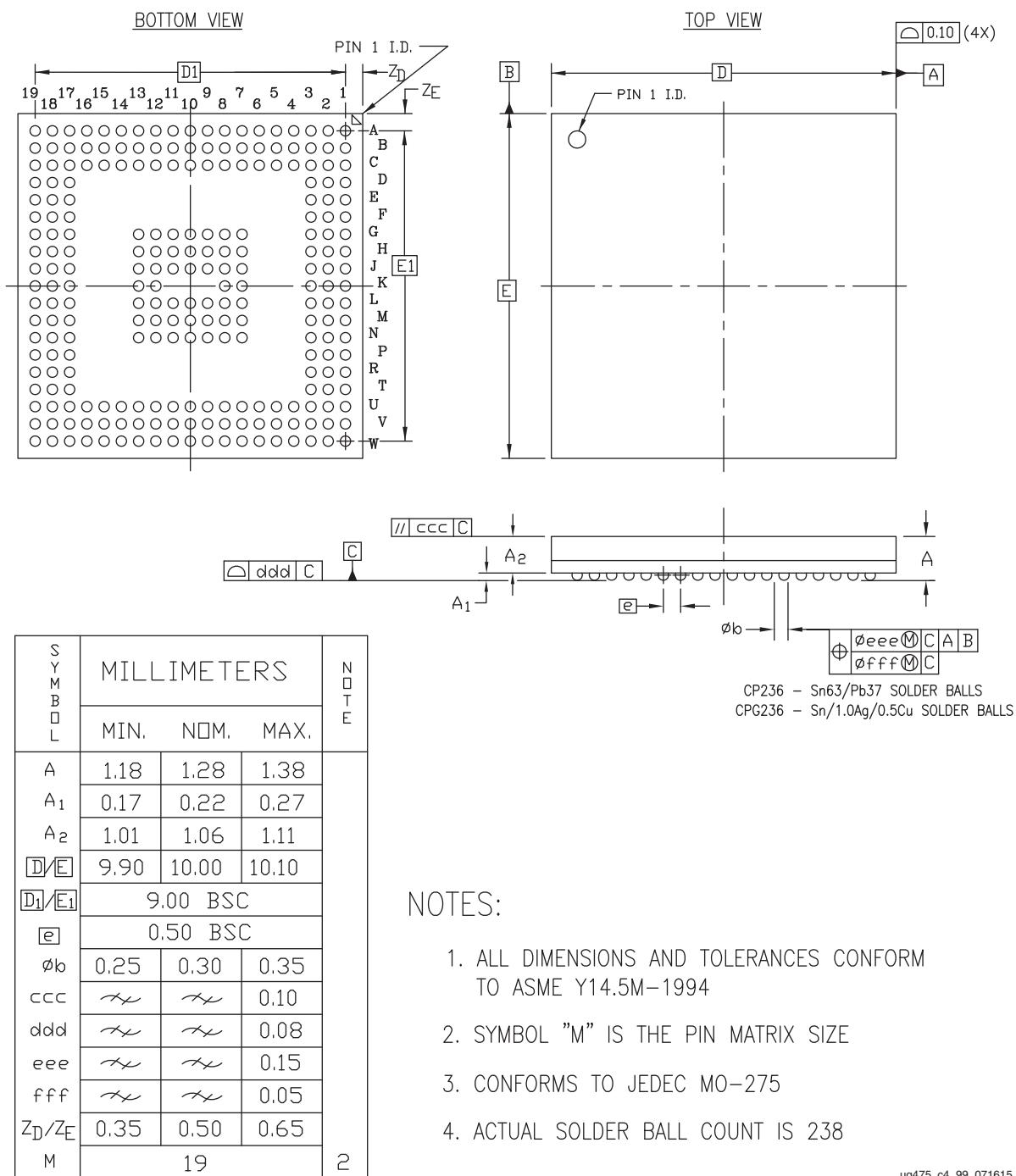
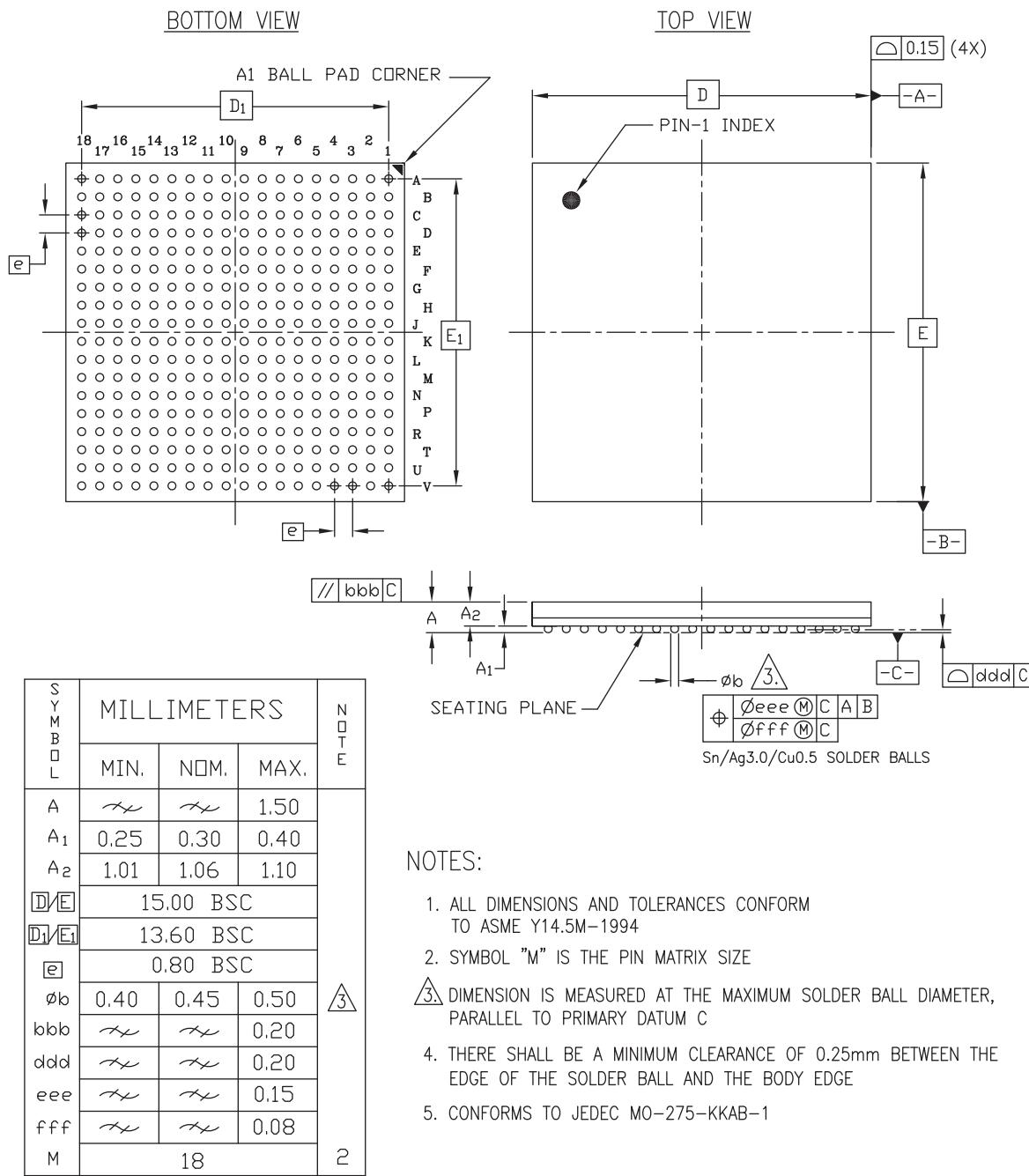


Figure 4-1: CP236 and CPG236 Wire-Bond Chip-Scale BGA Package Specifications for Artix®-7 FPGAs

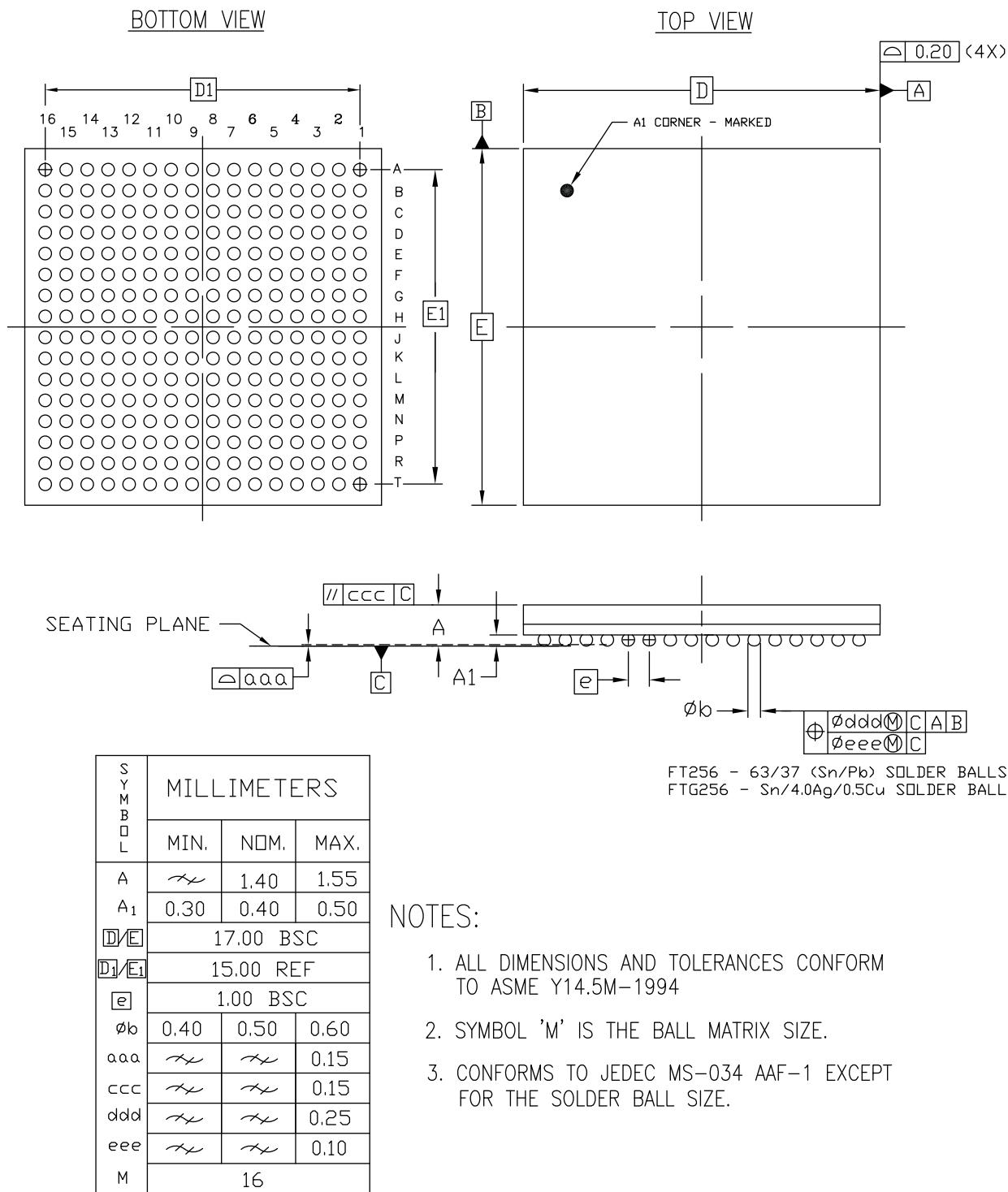
CS/CSG324 and CS/CSG325 (Artix-7 FPGAs) Wire-Bond Chip-Scale BGA (0.8 mm Pitch)



ug475_c4_100_013014

Figure 4-2: CS/CSG324 and CS/CSG325 Wire-Bond Chip-Scale BGA Package Specifications for Artix-7 FPGAs

FT/FTG256 (Artix-7 FPGAs) Wire-Bond Fine-Pitch Thin BGA (1.0 mm Pitch)



ug475_c4_101_070912

Figure 4-3: FT/FTG256 Wire-Bond Fine-Pitch Thin BGA Package Specifications for Artix-7 FPGAs

SB484, SBG484, and SBV484 (Artix-7 FPGAs) Flip-Chip Lidless BGA (0.8 mm Pitch)

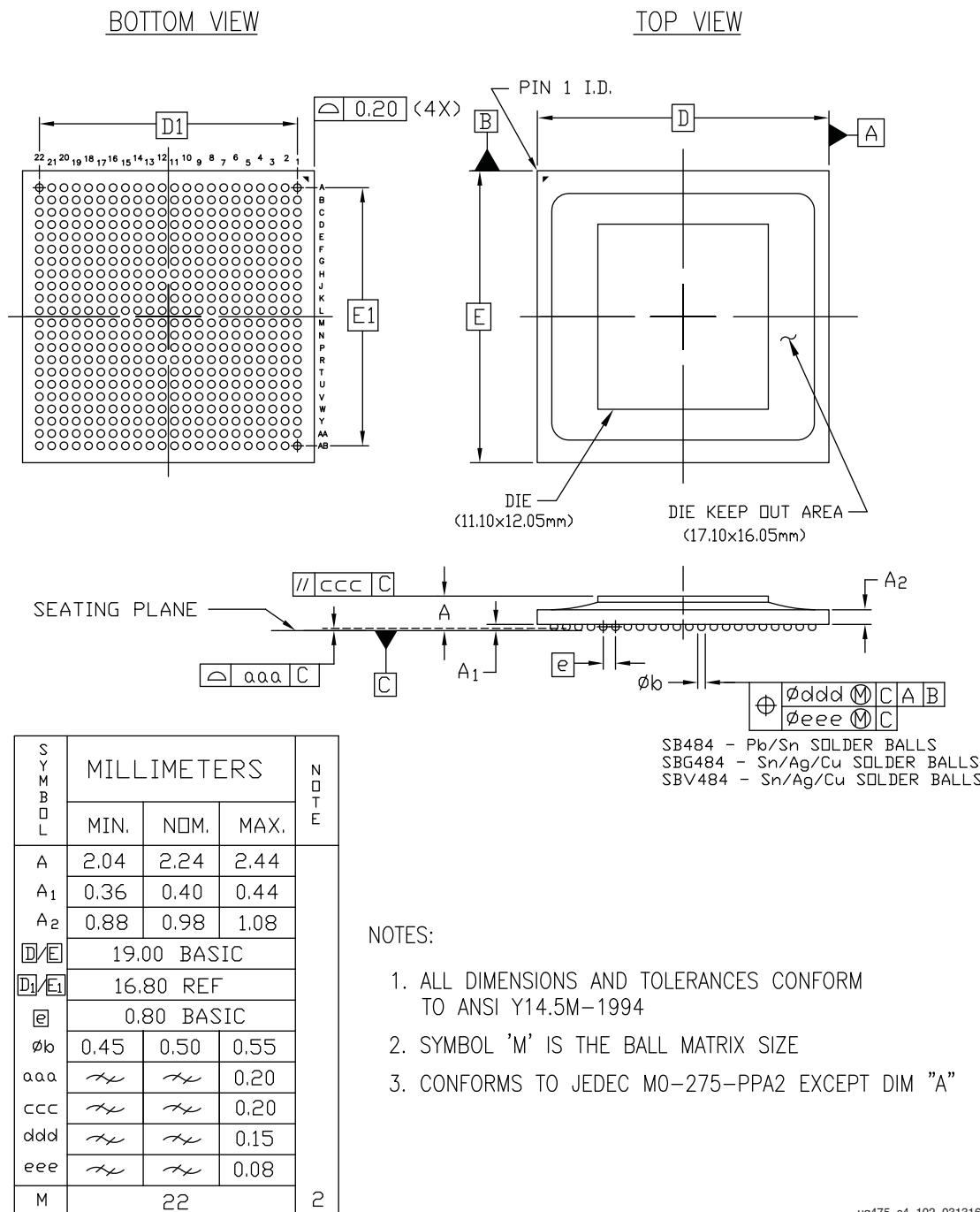
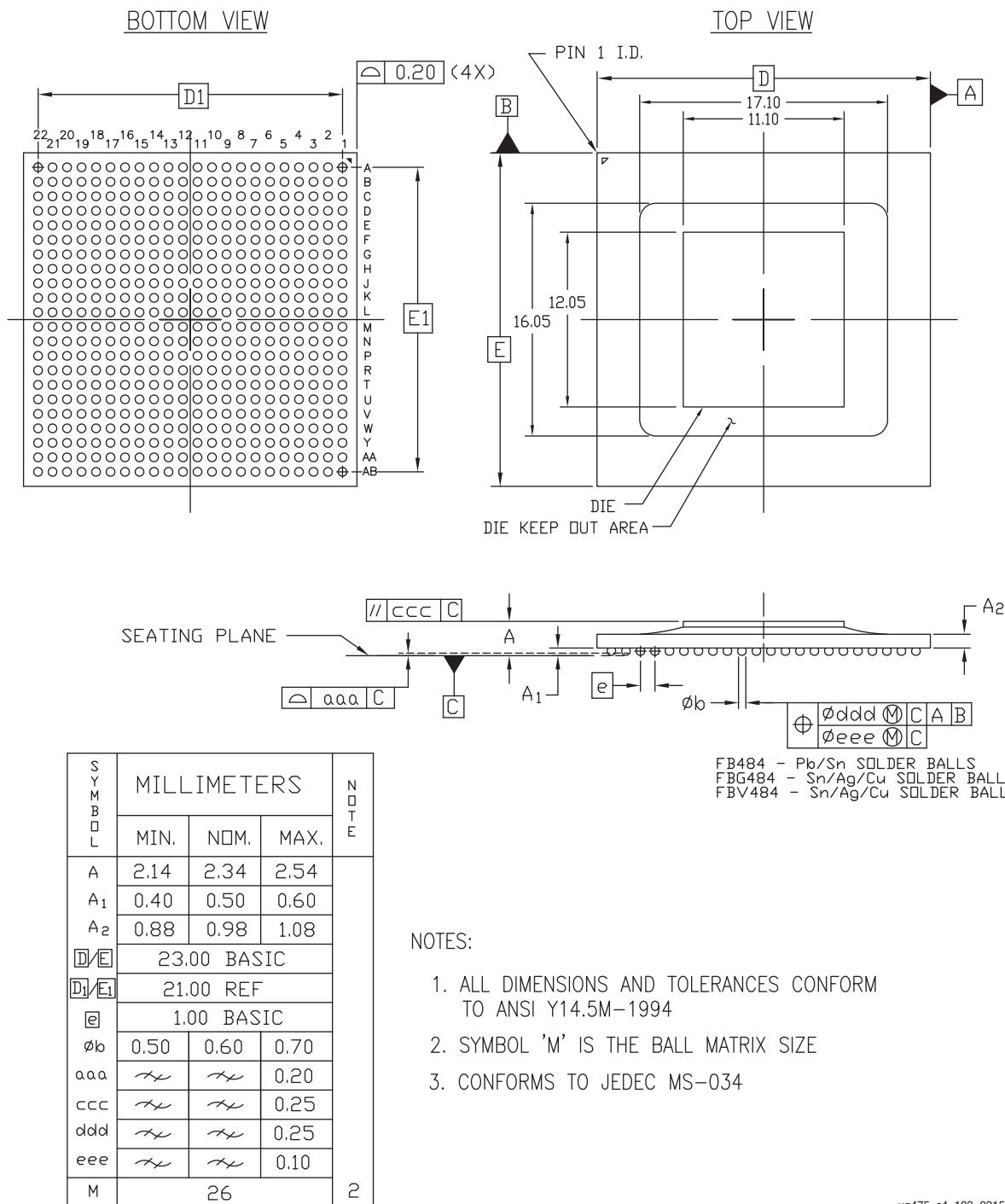


Figure 4-4: SB484, SBG484, and SBV484 Flip-Chip Lidless BGA Package Specifications for Artix-7 FPGAs

FB484, FBG484, and FBV484 (Artix-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch)



ug475_c4_103_031516

Figure 4-5: FB484, FBG484, and FBV484 Flip-Chip Lidless BGA Package Specifications for Artix-7 FPGAs

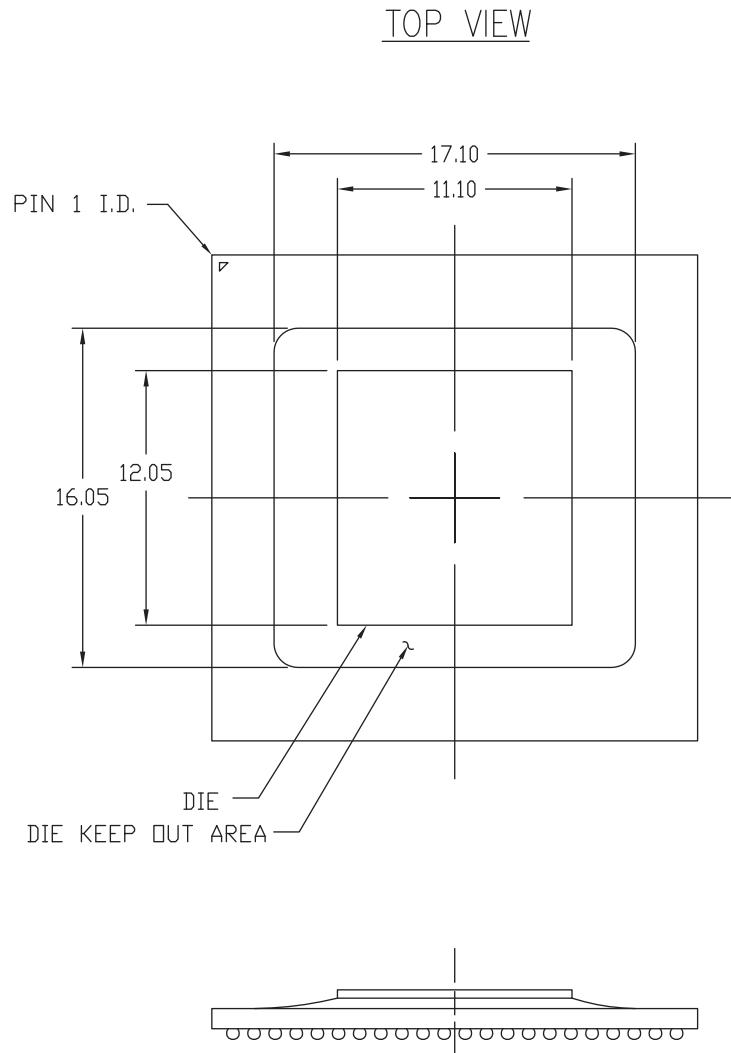


Figure 4-6: XC7A200T FB484, FBG484, and FBV484 Die Dimensions

FB676, FBG676, and FBV676 (Artix-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch)

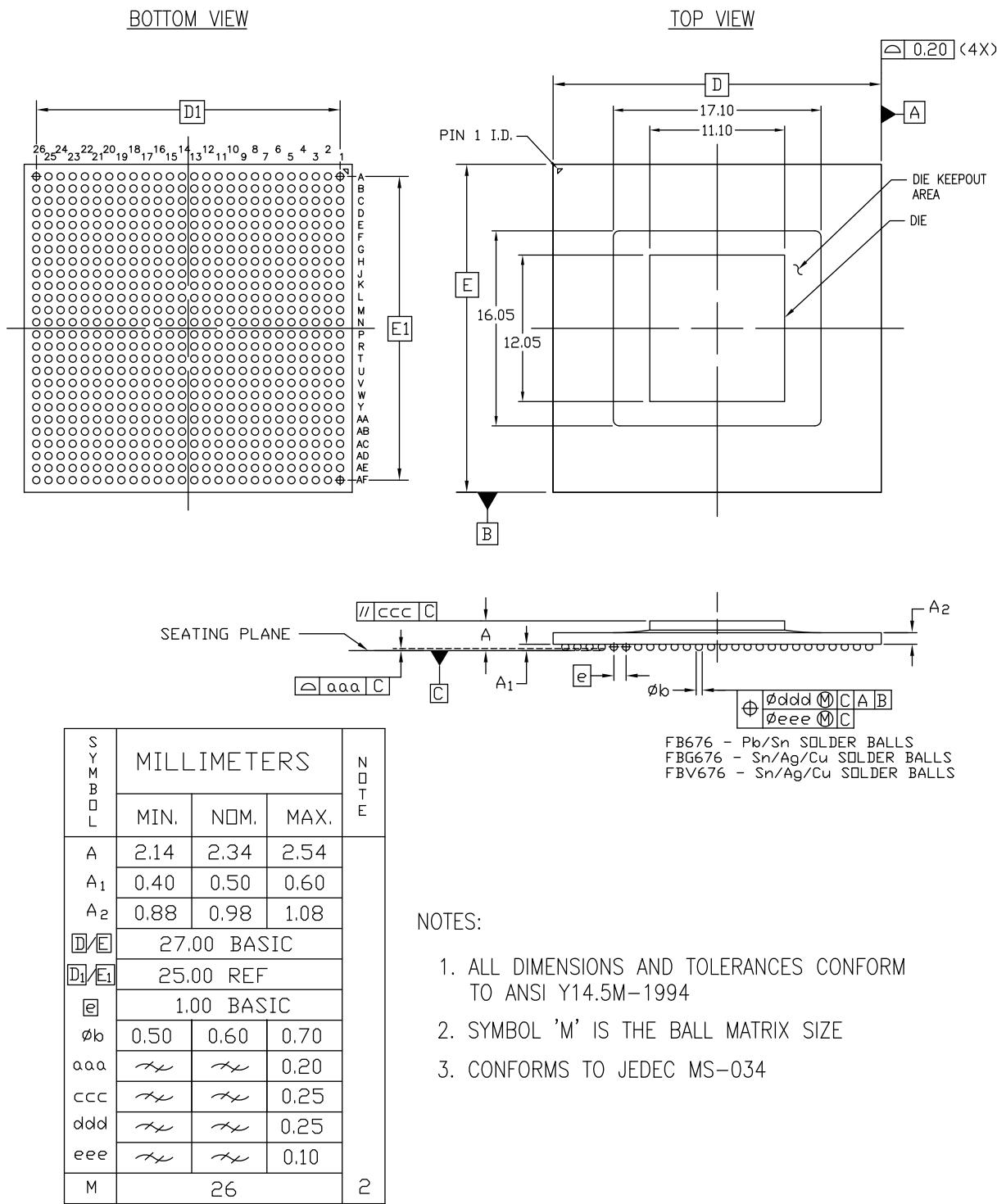
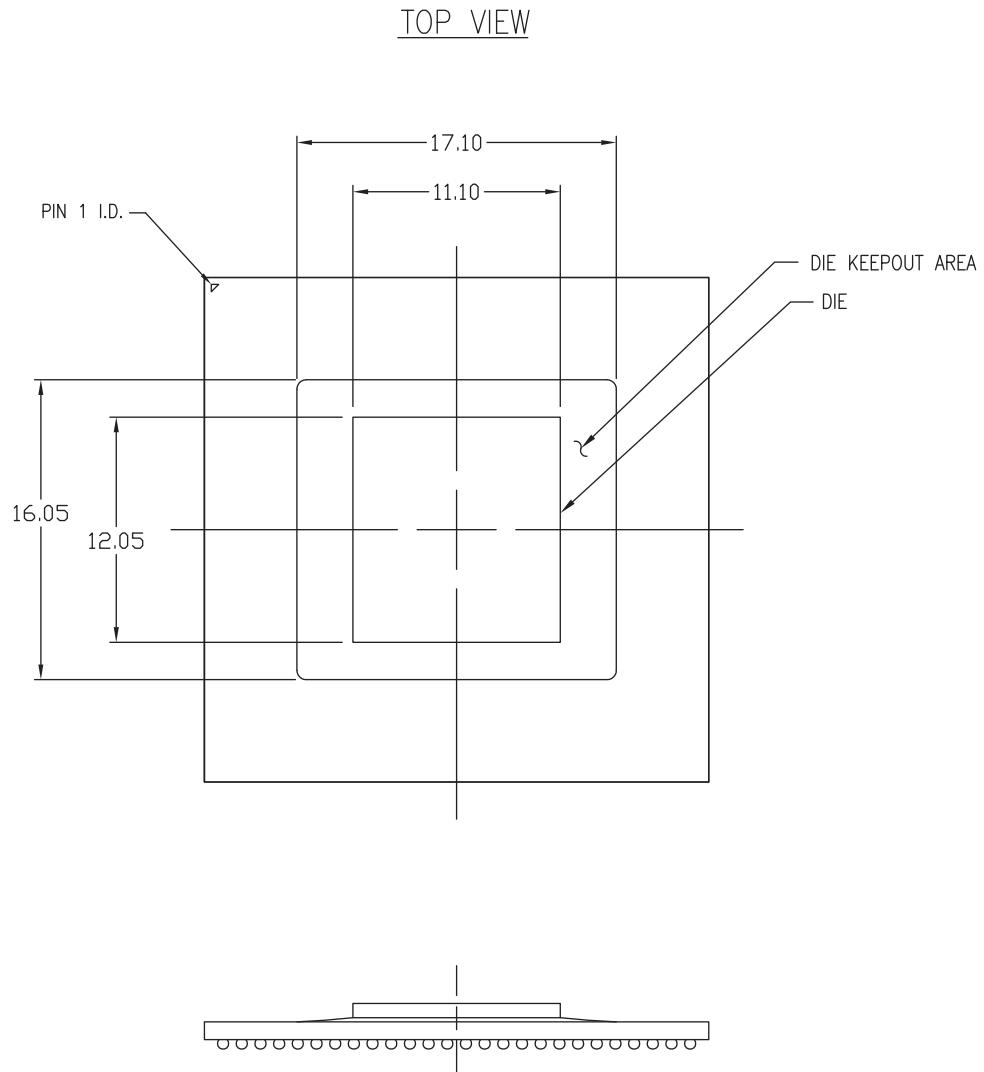


Figure 4-7: FB676, FBG676, and FBV676 Flip-Chip Lidless BGA Package Specifications for Artix-7 FPGAs

ug475_c4_106_031316



ug475_c4_107_070912

Figure 4-8: XC7A200T FB676, FBG676, and FBV676 Die Dimensions

FG484 and FGG484 (Artix-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch)

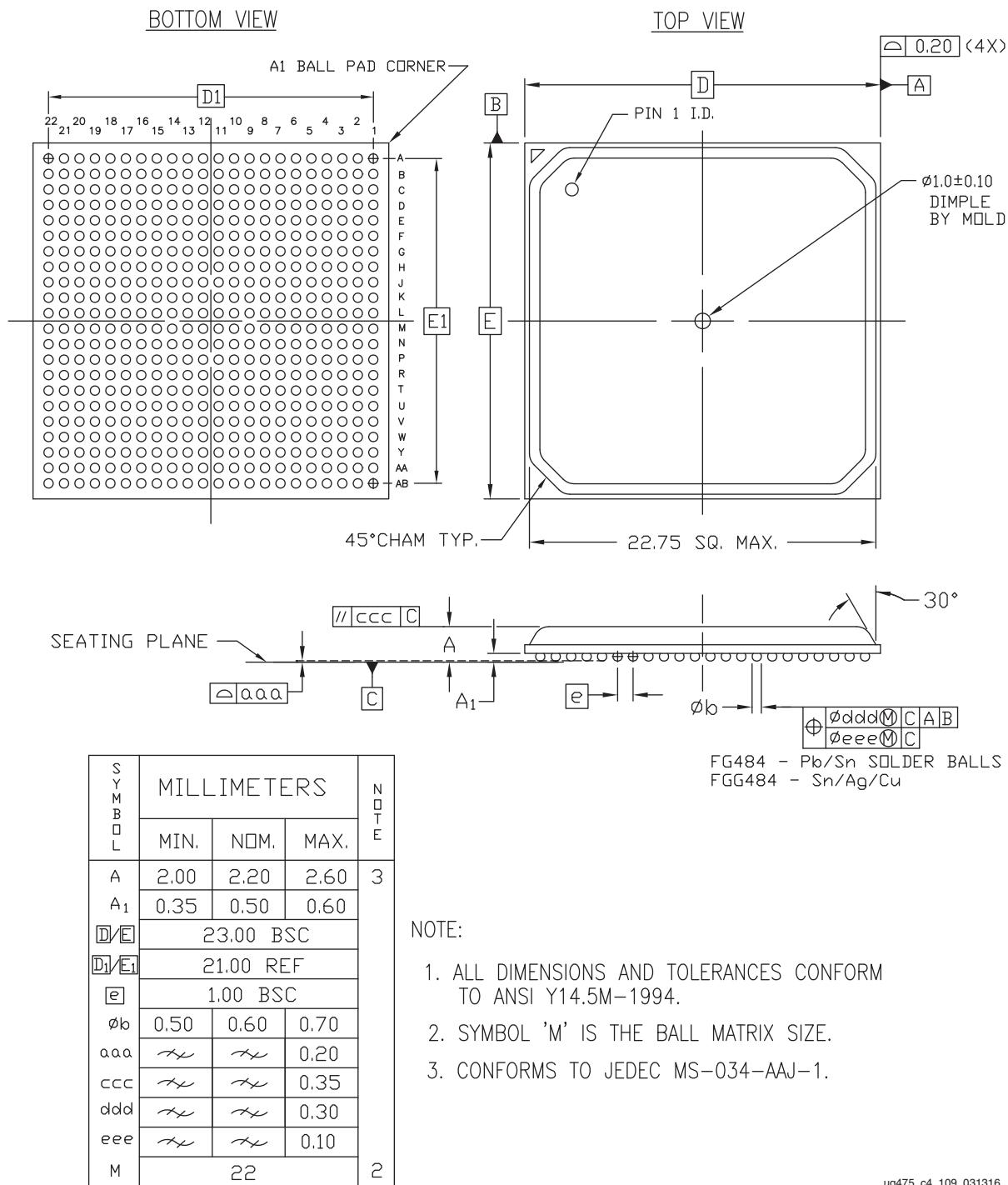


Figure 4-9: FG484 and FGG484 Wire-bond Fine-Pitch BGA Package Specification for Artix-7 FPGAs

FG676 and FGG676 (Artix-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch)

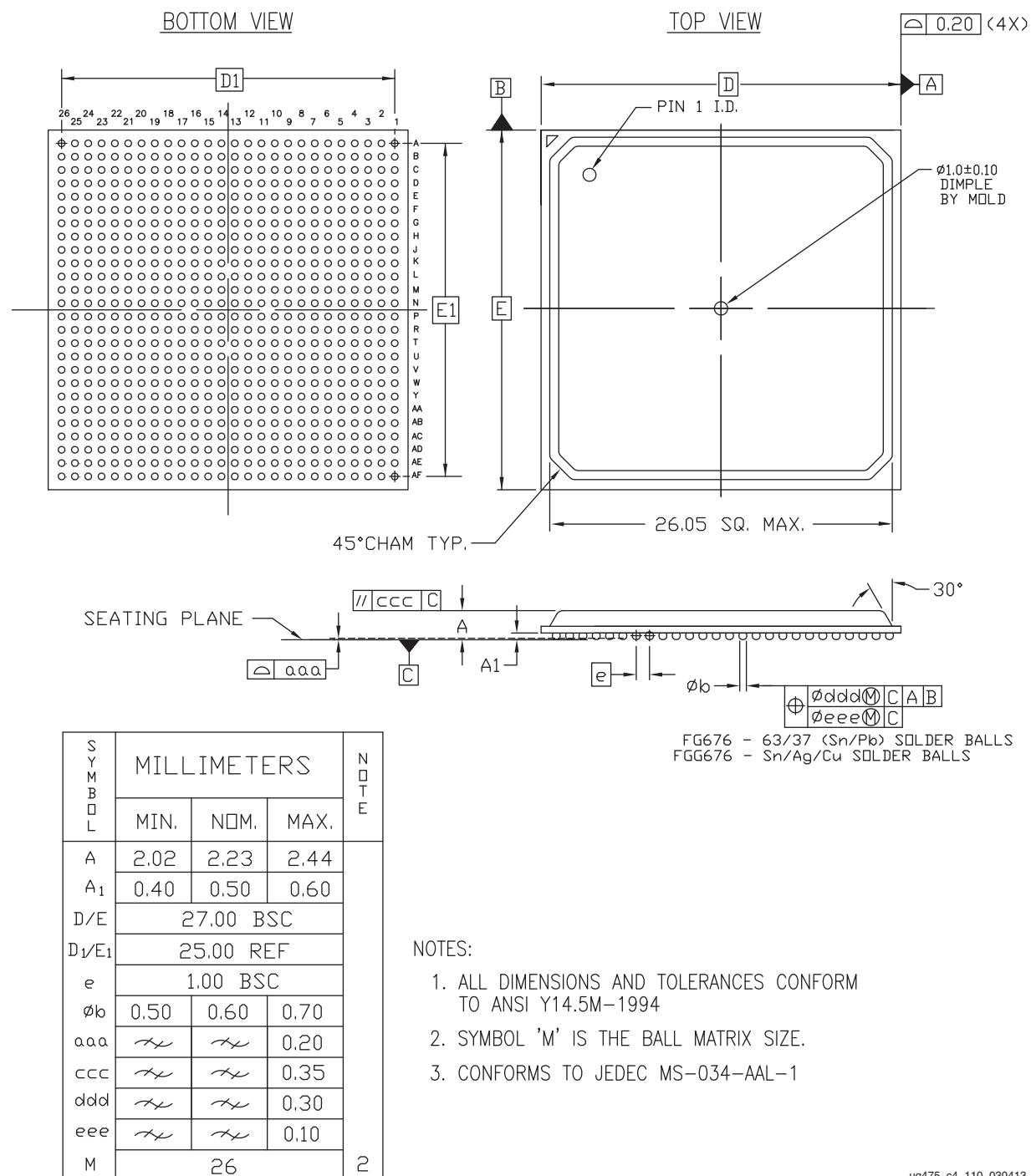


Figure 4-10: FG676 and FGG676 Wire-bond Fine-Pitch BGA Package Specification for Artix-7 FPGAs

FF1156, FFG1156, and FFV1156 (Artix-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)

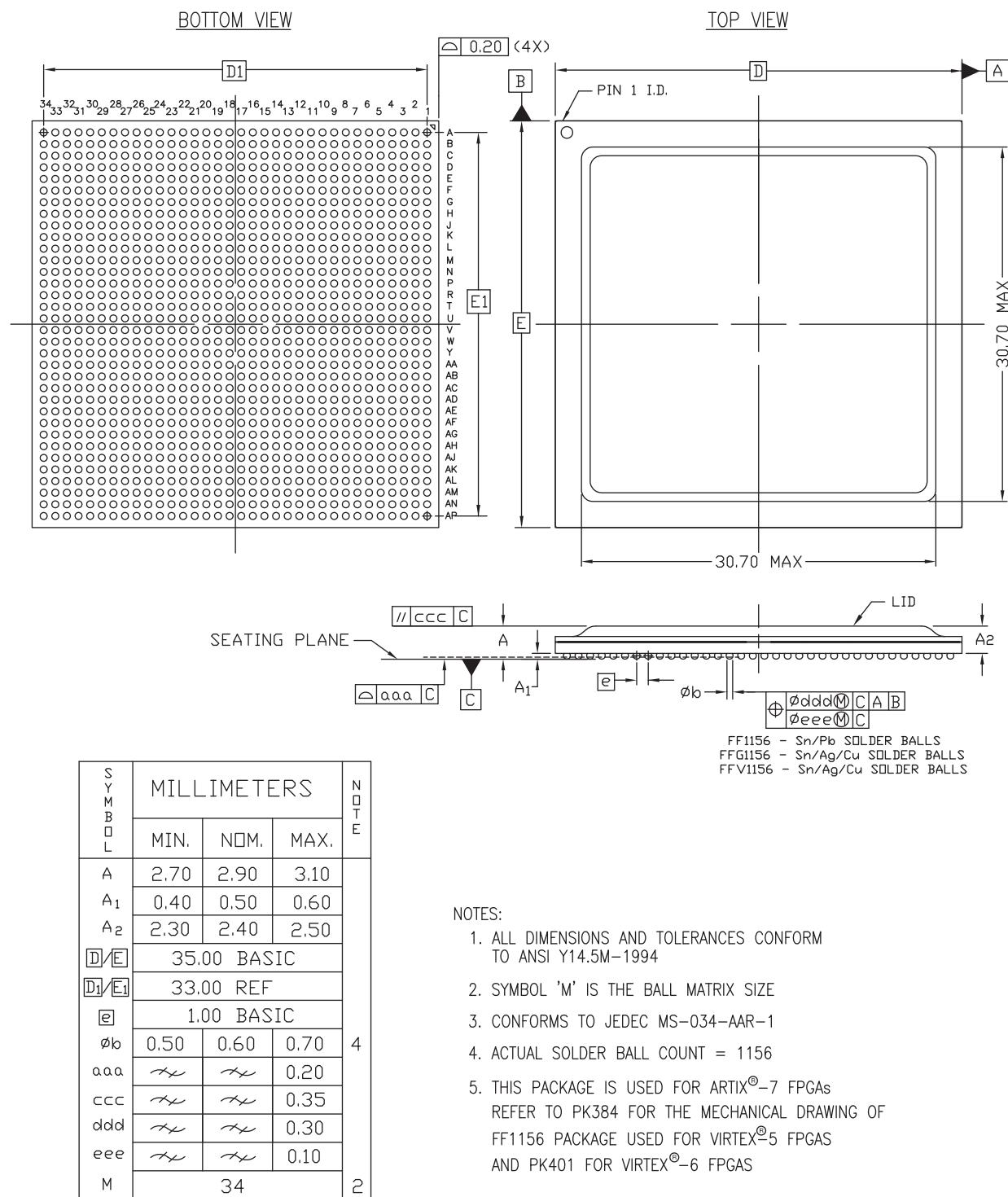


Figure 4-11: FF1156, FFG1156, and FFV1156 Flip-Chip BGA Package Specification for Artix-7 FPGAs

RB484 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA (1.0 mm Pitch)

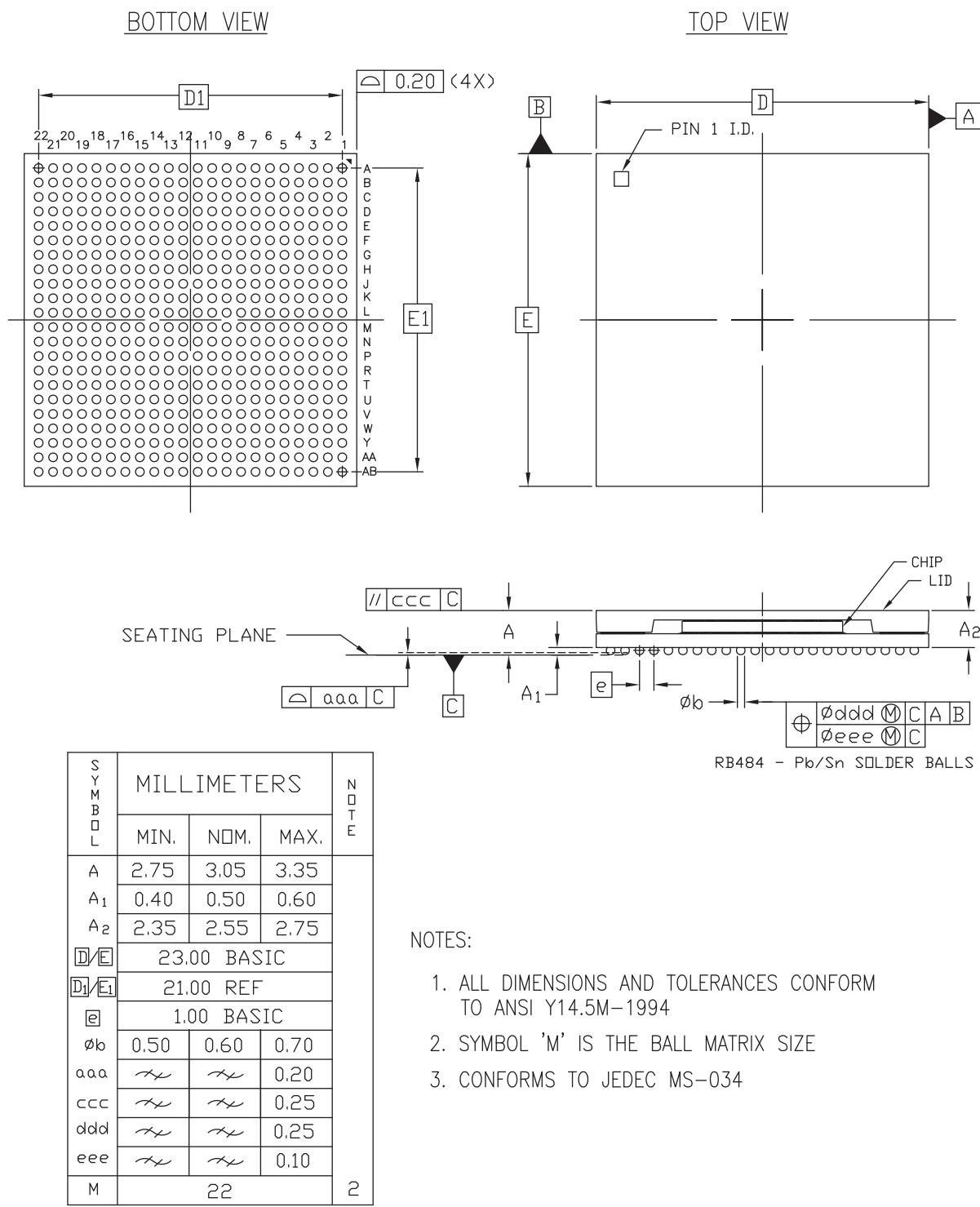


Figure 4-12: RB484 Ruggedized Flip-Chip BGA Package Specifications for Artix-7 FPGAs

RS484 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA (0.8 mm Pitch)

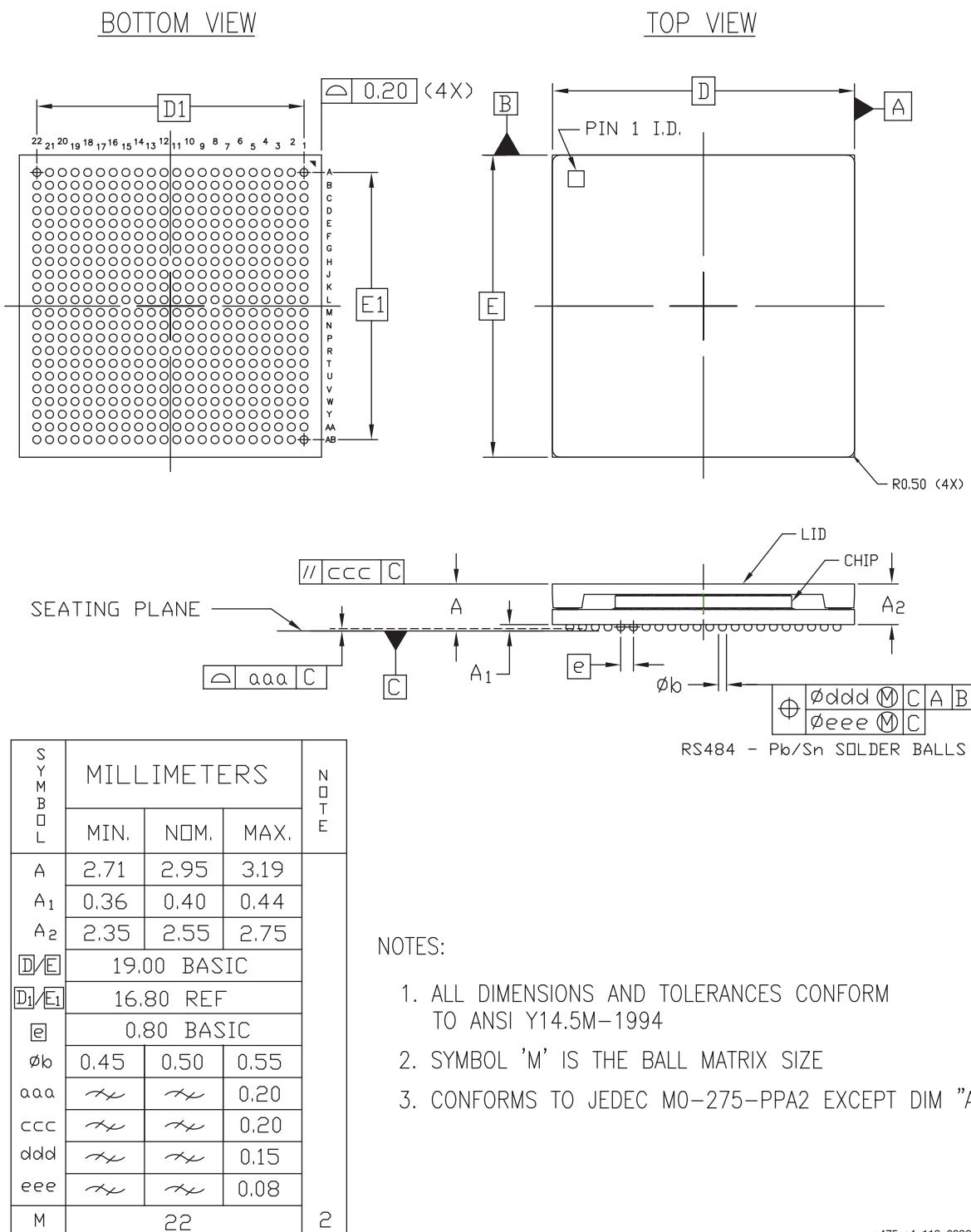


Figure 4-13: RS484 Ruggedized Flip-Chip BGA Package Specifications for Artix-7 FPGAs

RB676 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA (1.0 mm Pitch)

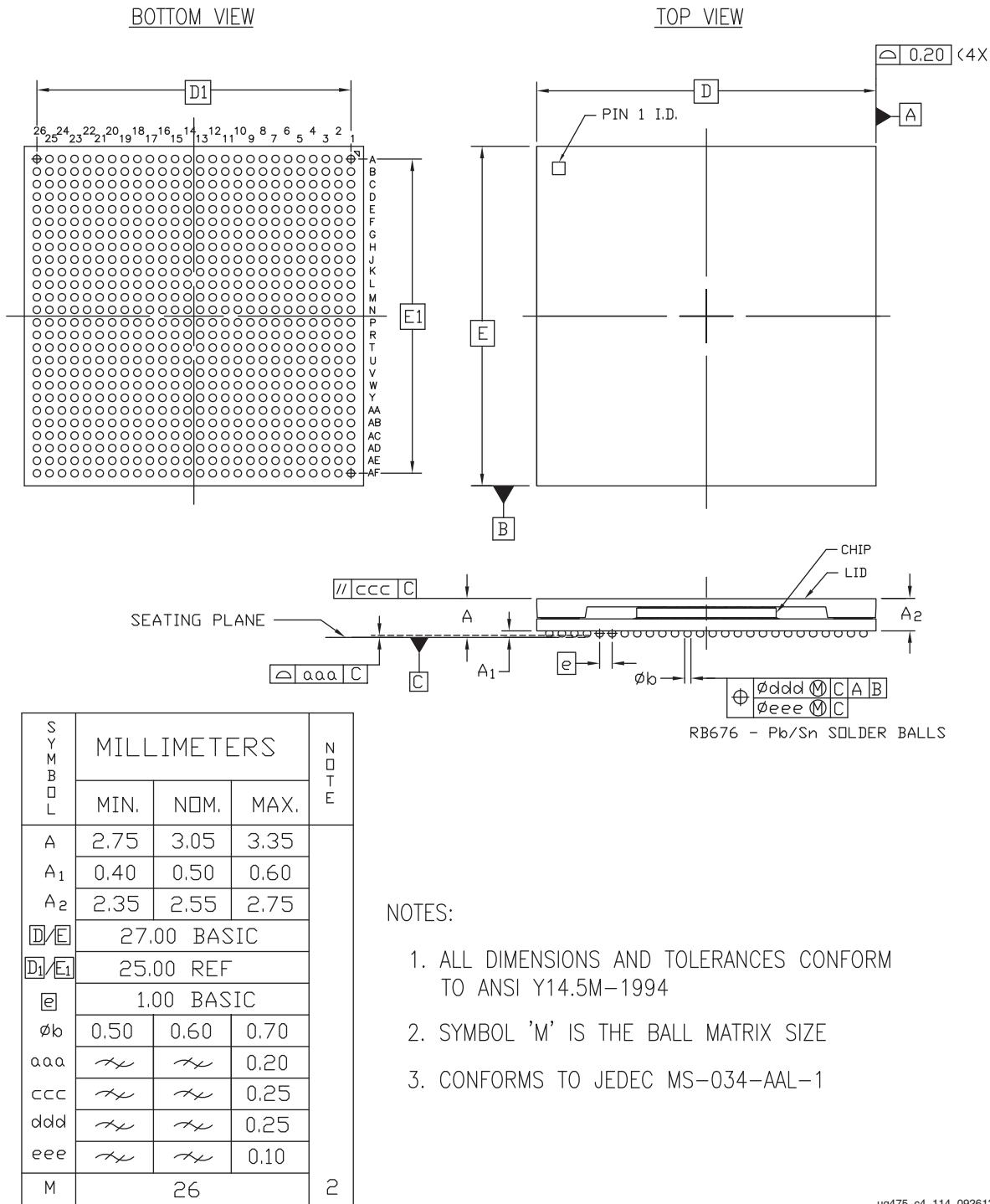
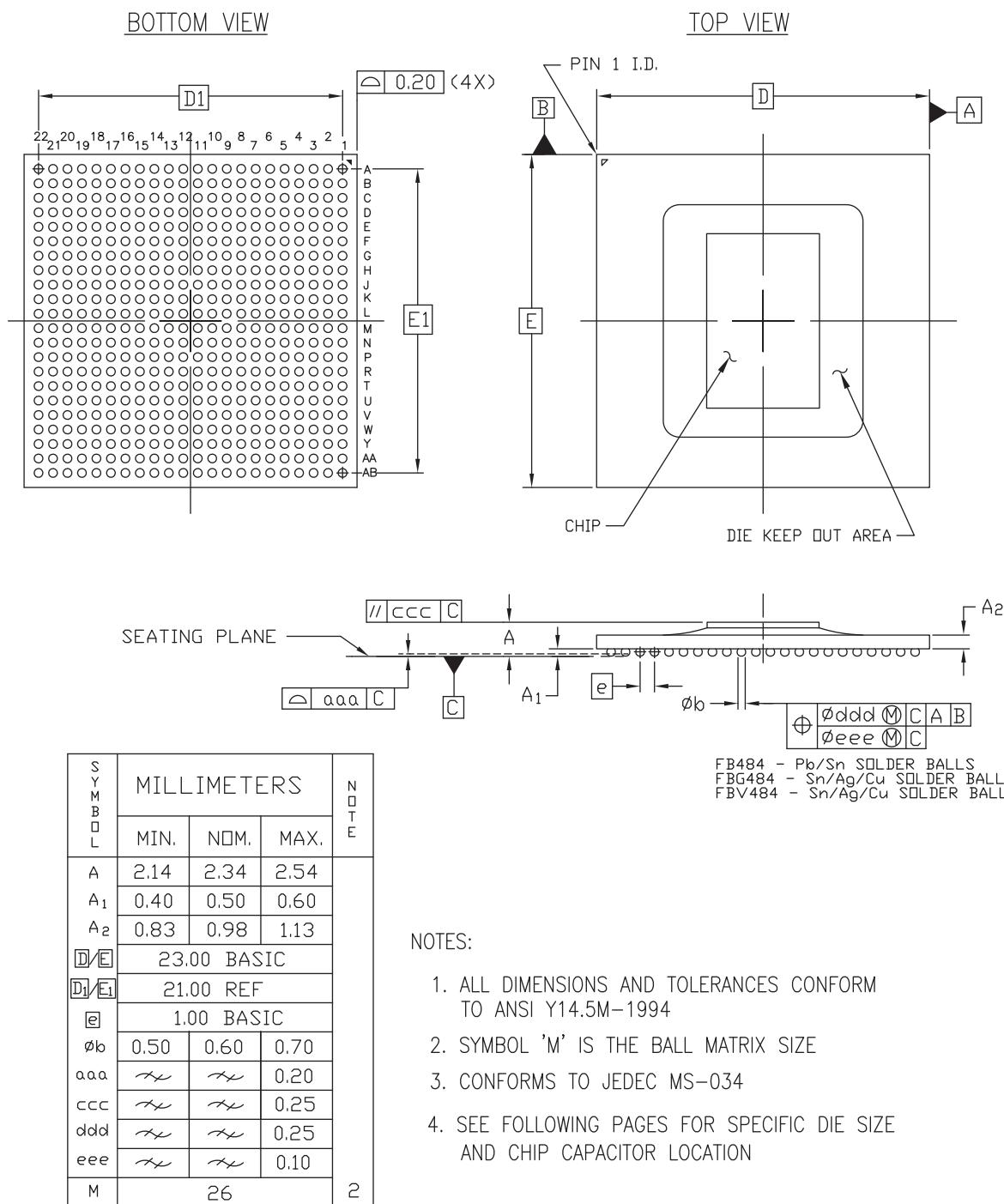


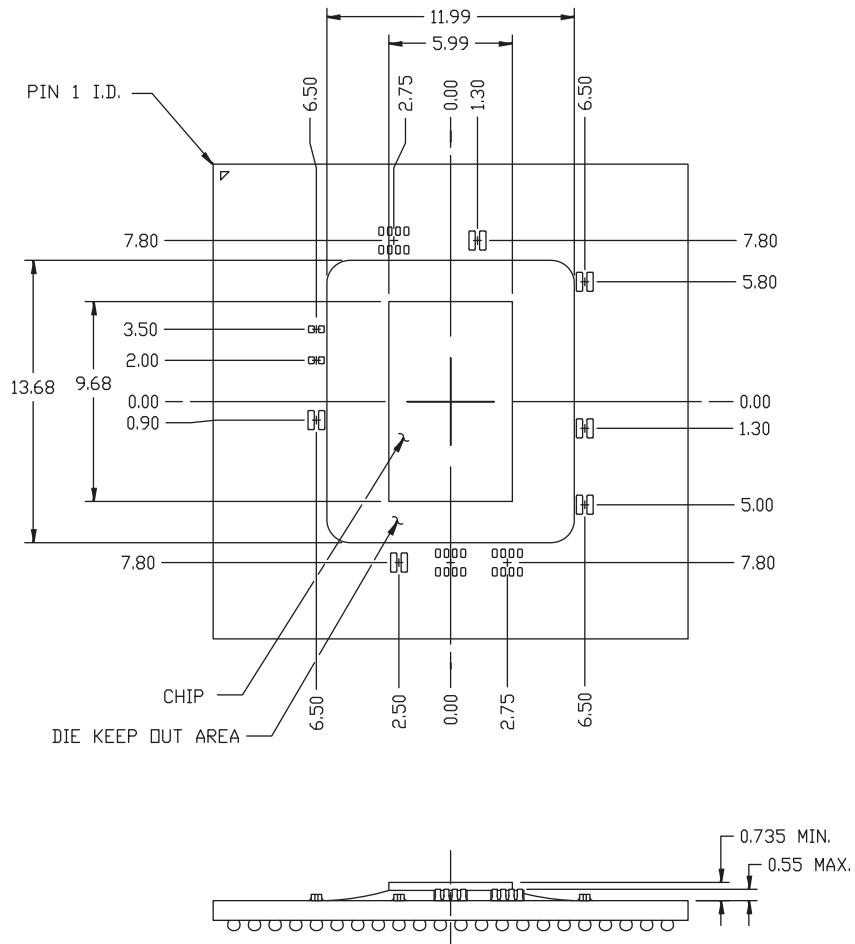
Figure 4-14: RB676 Ruggedized Flip-Chip BGA Package Specifications for Artix-7 FPGAs

FB484, FBG484, and FBV484 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch)



ug475_c4_01_031516

Figure 4-15: FB484, FBG484, and FBV484 Flip-Chip Lidless BGA Package Specifications for Kintex®-7 FPGAs



ug475_c4_20_013113

Figure 4-16: XC7K70T FB484, FBG484, and FBV484 Die Dimensions with Capacitor Locations

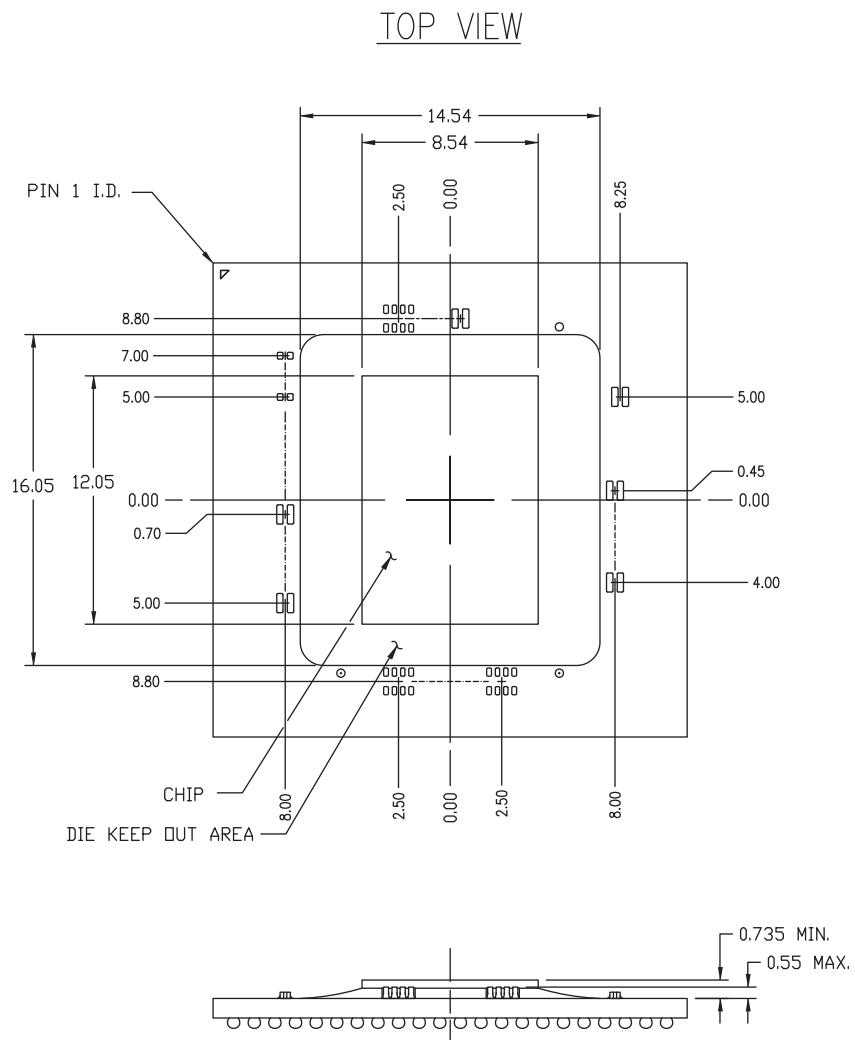


Figure 4-17: XC7K160T FB484, FBG484, and FBV484 Die Dimensions with Capacitor Locations

FB676, FBG676, and FBV676 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch)

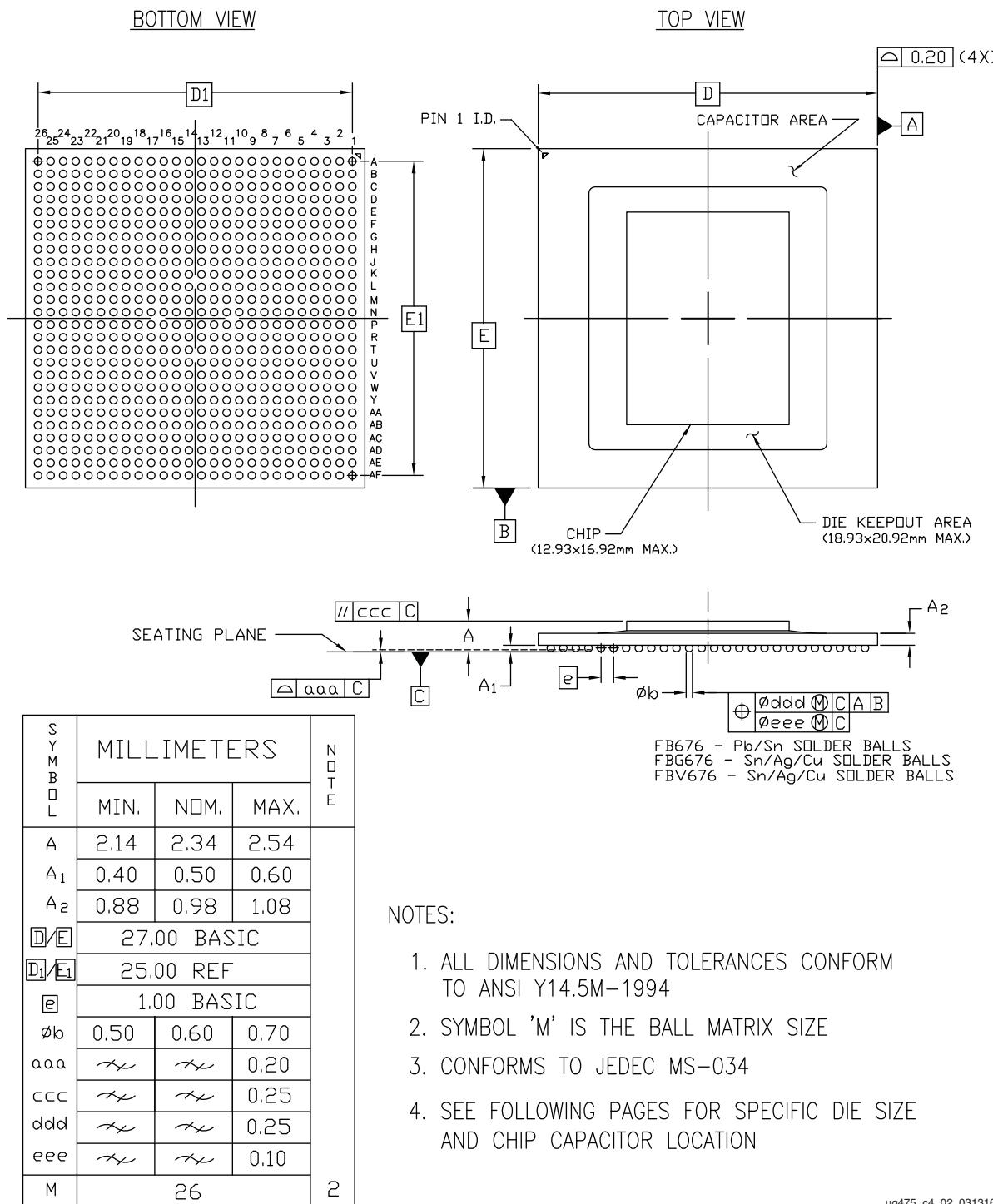
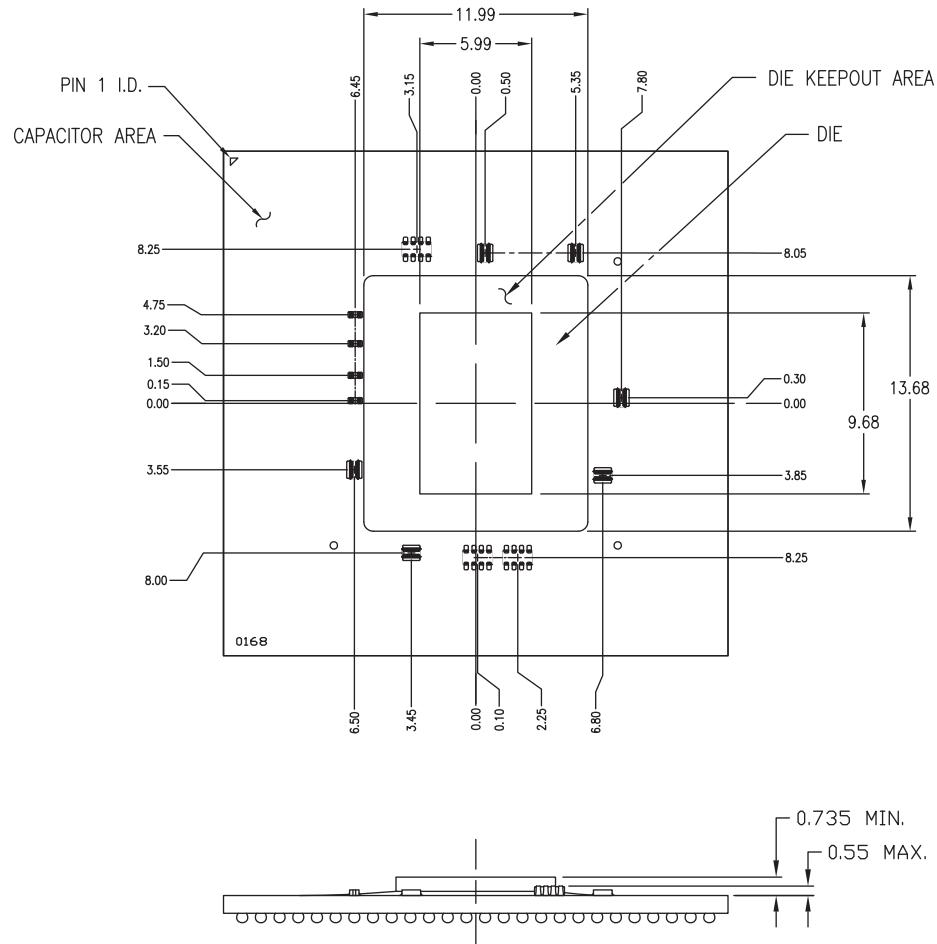


Figure 4-18: FB676, FBG676, and FBV676 Flip-Chip Lidless BGA Package Specifications for Kintex-7 FPGAs



ug475_c4_203_091712

Figure 4-19: XC7K70T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations

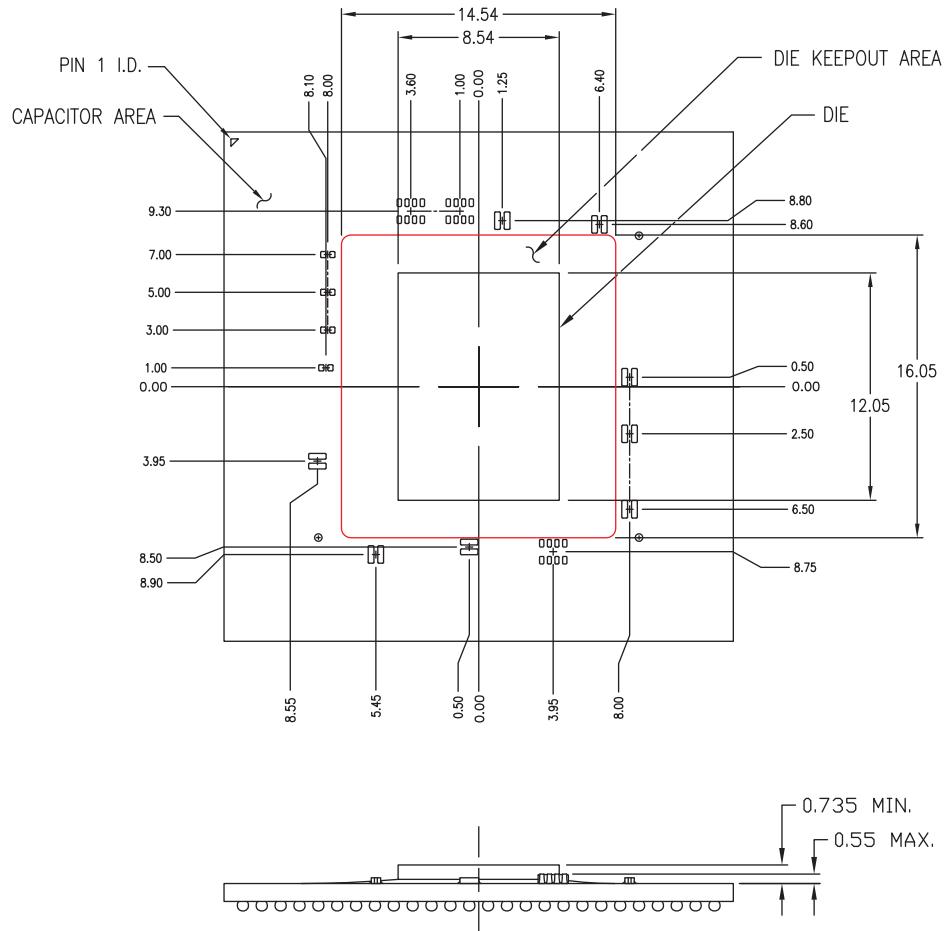


Figure 4-20: XC7K160T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations

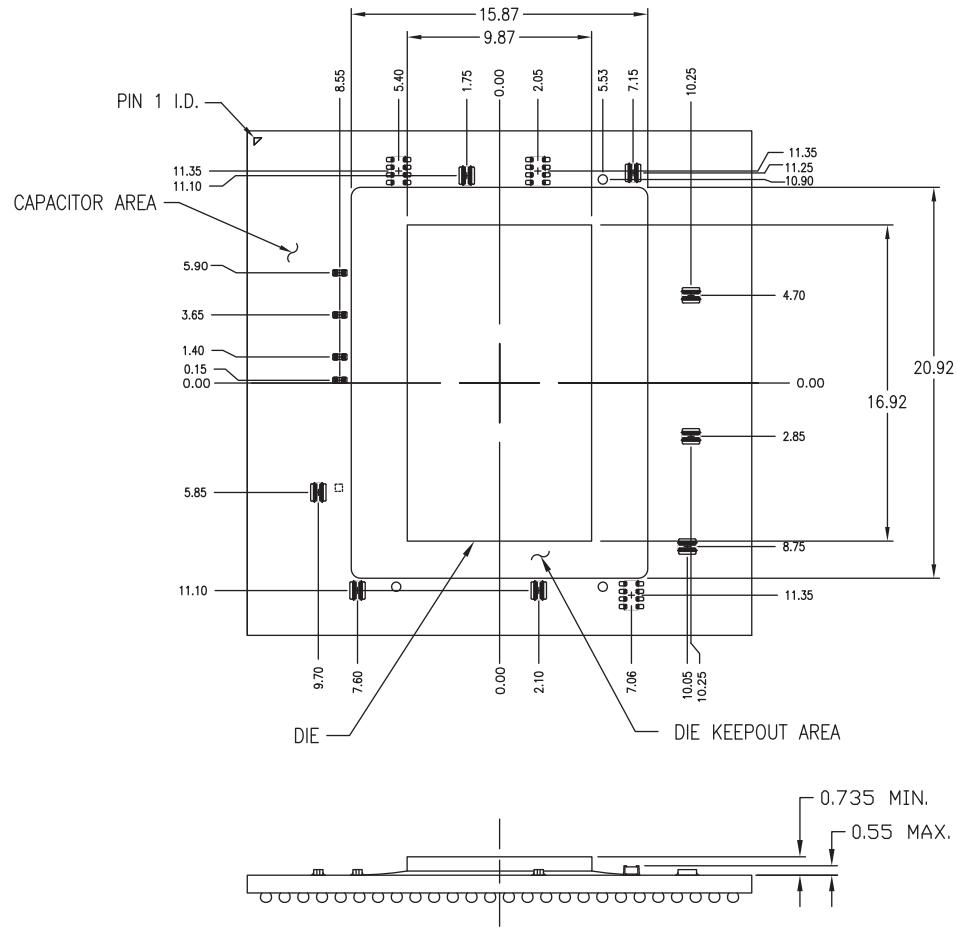


Figure 4-21: XC7K325T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations

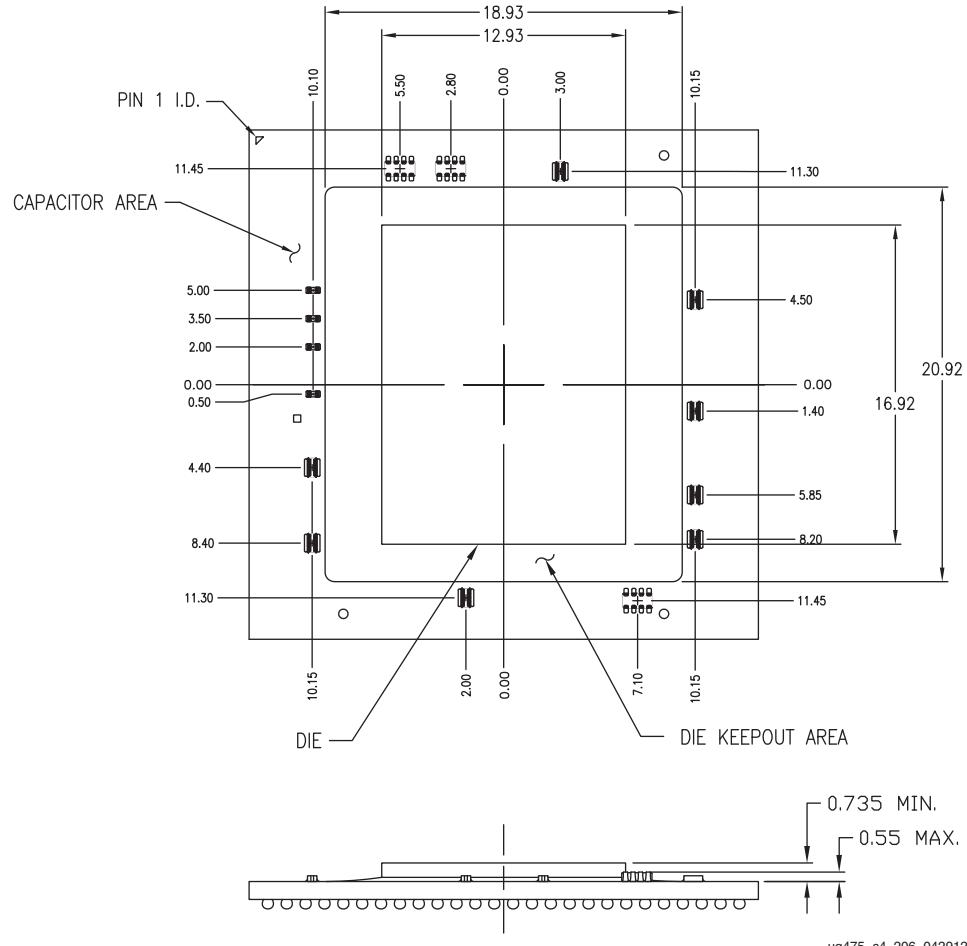


Figure 4-22: XC7K410T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations

FB900, FBG900, and FBV900 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch)

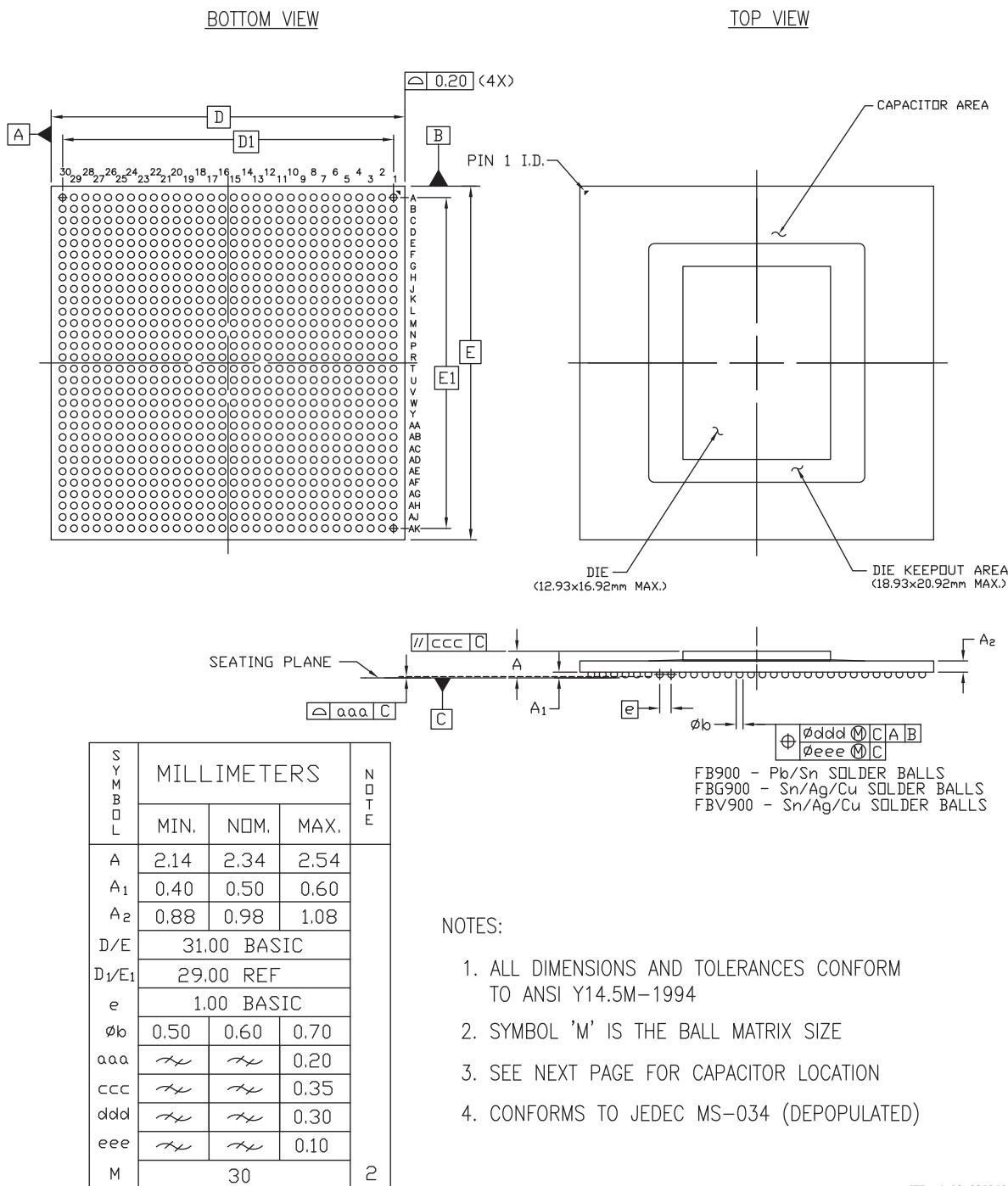


Figure 4-23: FB900, FBG900, and FBV900 Flip-Chip Lidless BGA Package Specifications for Kintex-7 FPGAs

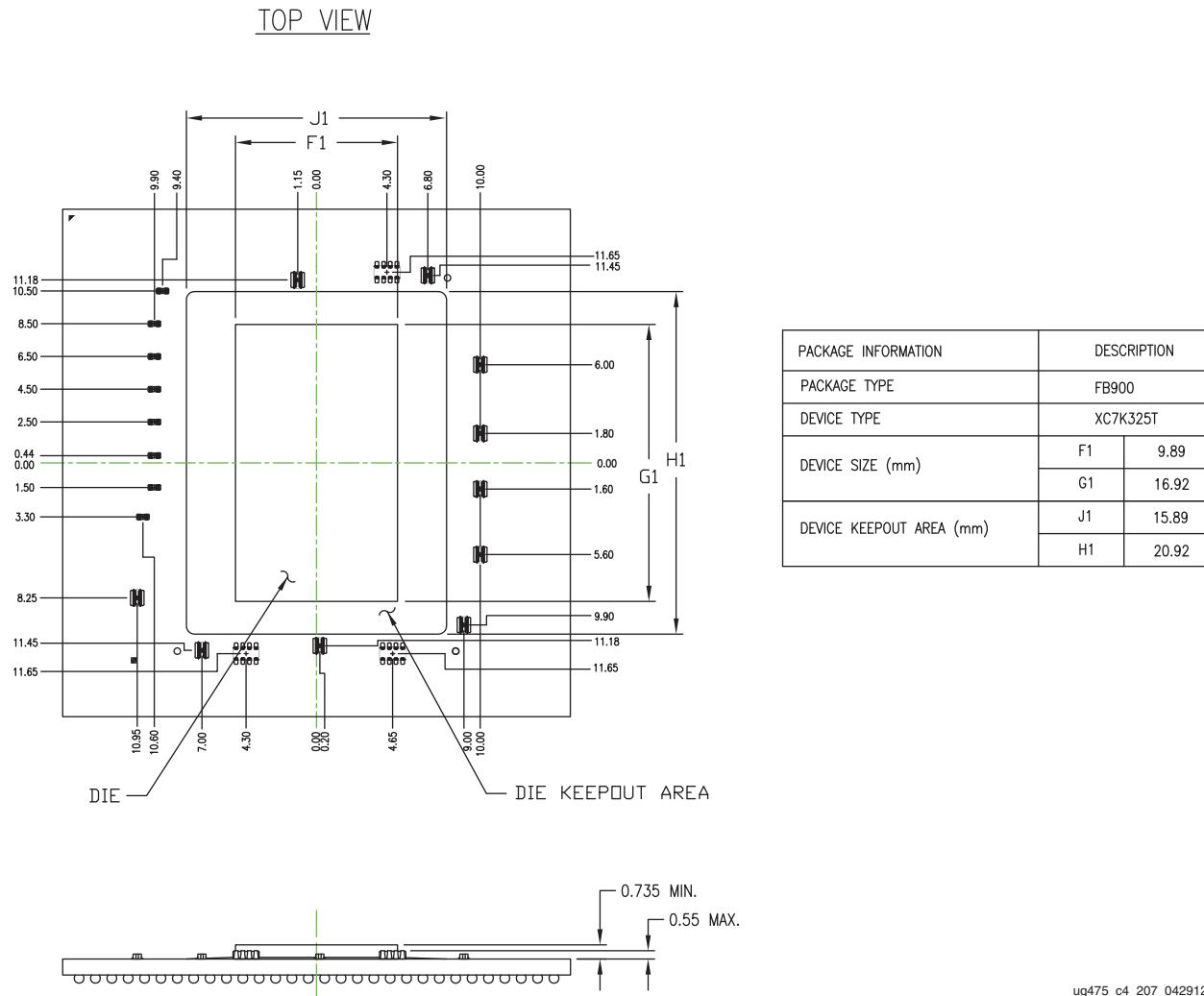
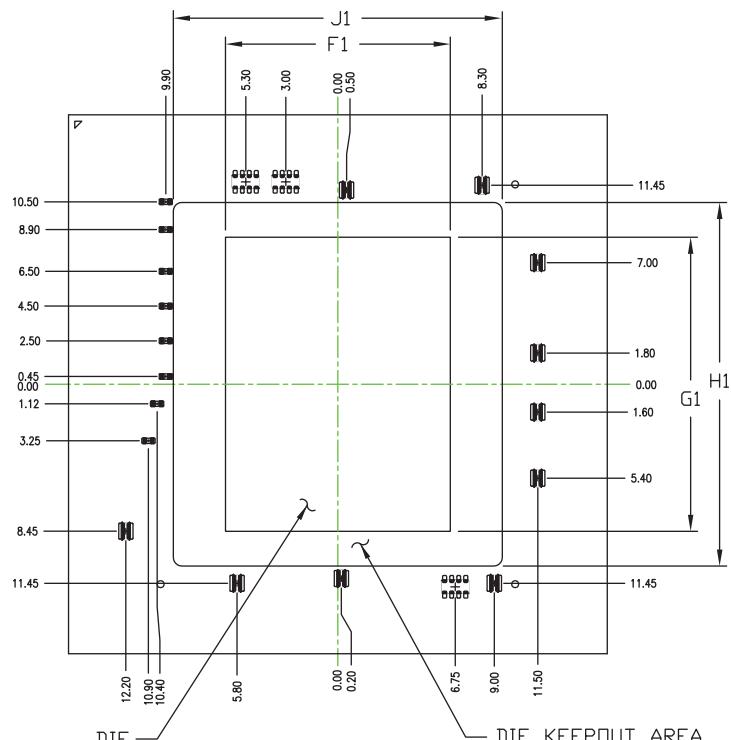


Figure 4-24: XC7K325T FB900, FBG900, and FBV900 Die Dimensions with Capacitor Locations

TOP VIEW



PACKAGE INFORMATION	DESCRIPTION	
PACKAGE TYPE	FB900	
DEVICE TYPE	XC7K410T	
DEVICE SIZE (mm)	F1	12.93
	G1	16.92
DEVICE KEEPOUT AREA (mm)	J1	18.93
	H1	20.92

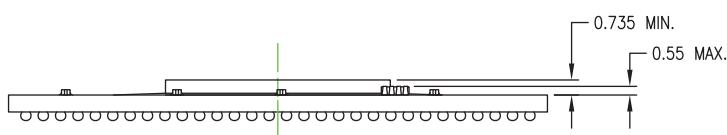


Figure 4-25: XC7K410T FB900, FBG900, and FBV900 Die Dimensions with Capacitor Locations

FF676, FFG676, and FFV676 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)

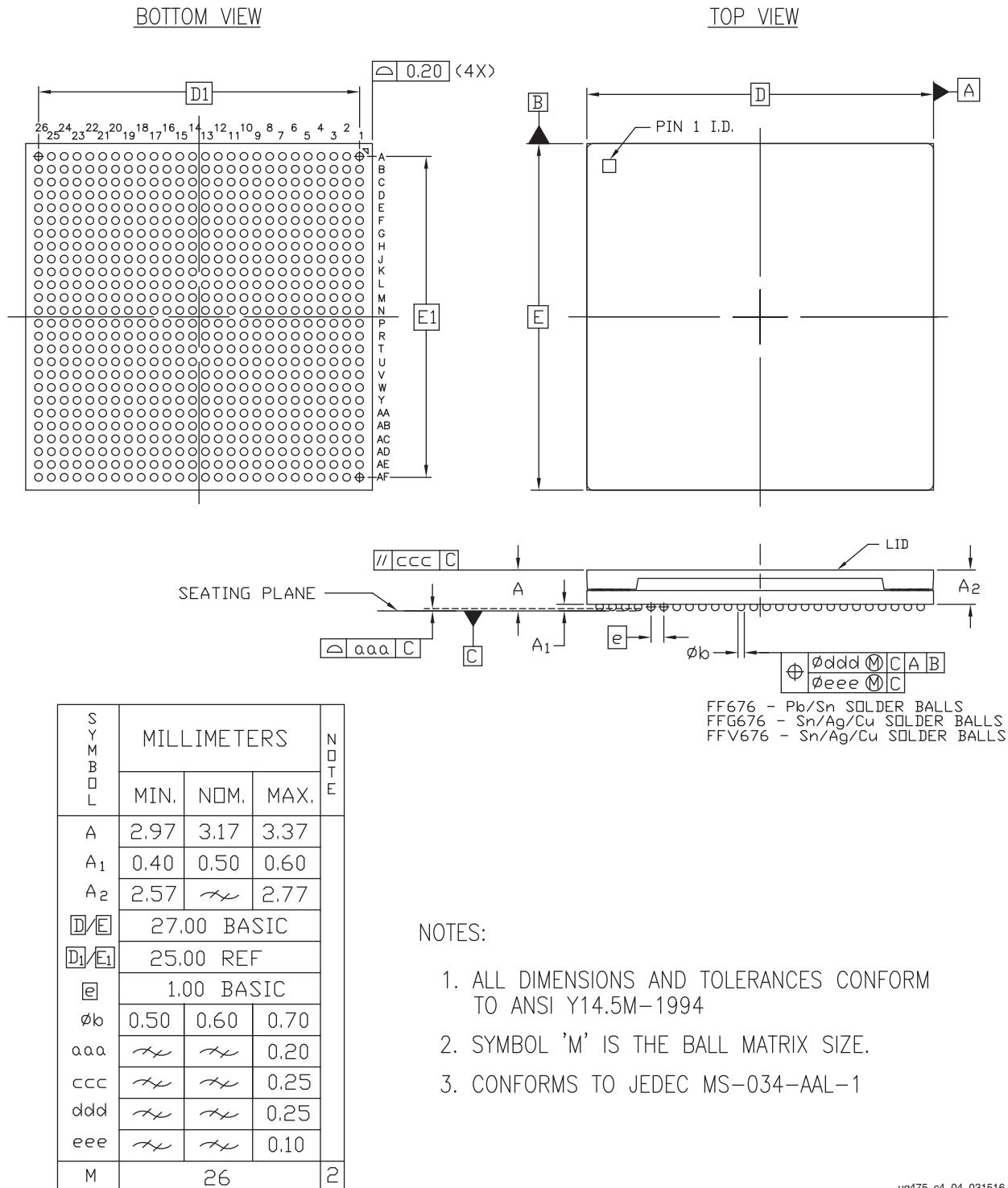
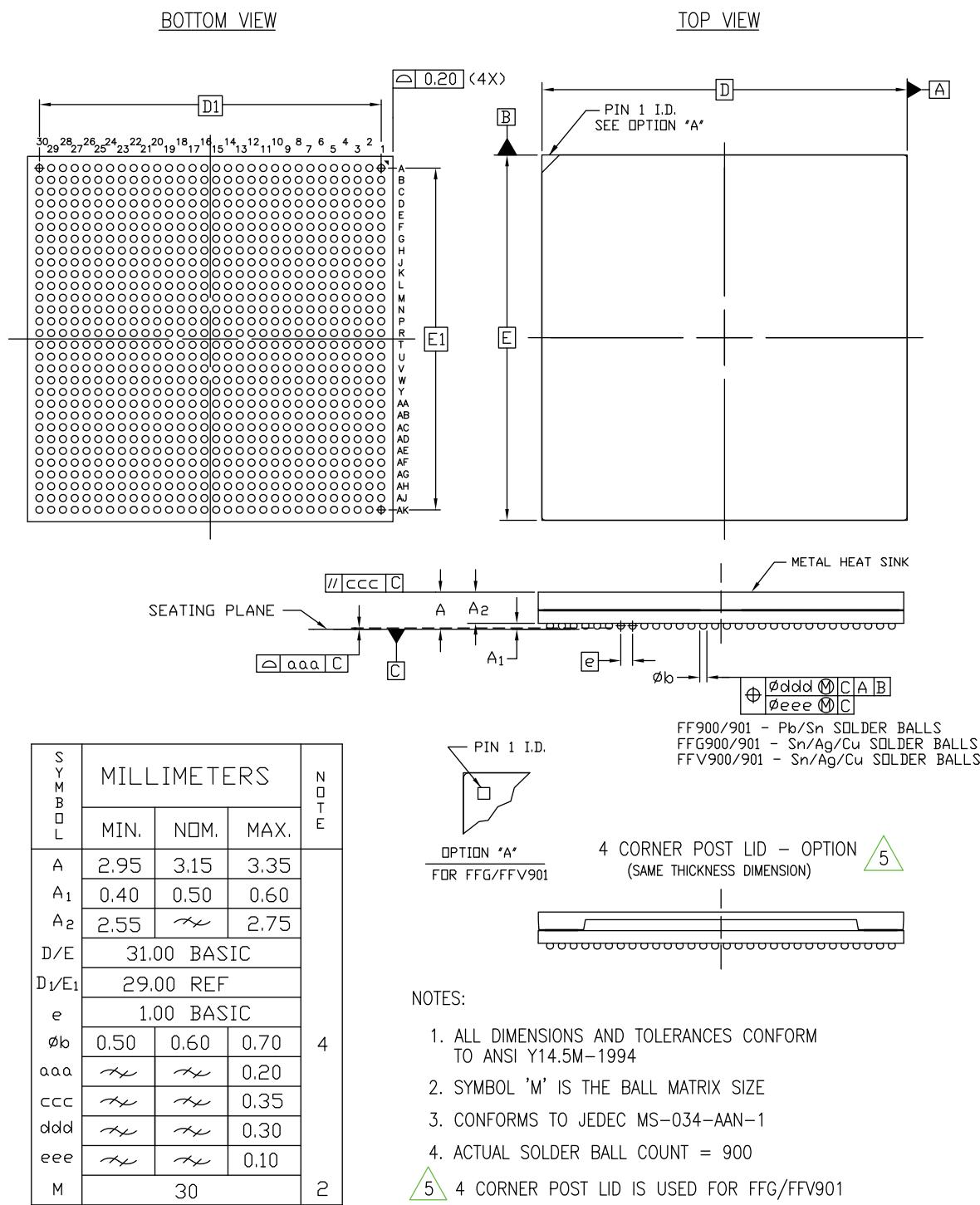


Figure 4-26: FF676, FFG676, and FFV676 Flip-Chip BGA Package Specifications for Kintex-7 FPGAs

FF900, FFG900, FFV900, FF901, FFG901, and FFV901 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)



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Figure 4-27: FF900, FFG900, FFV900, FF901, FFG901, and FFV901 Flip-Chip BGA Package Specifications for Kintex-7 FPGAs

FF1156, FFG1156, and FFV1156 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)

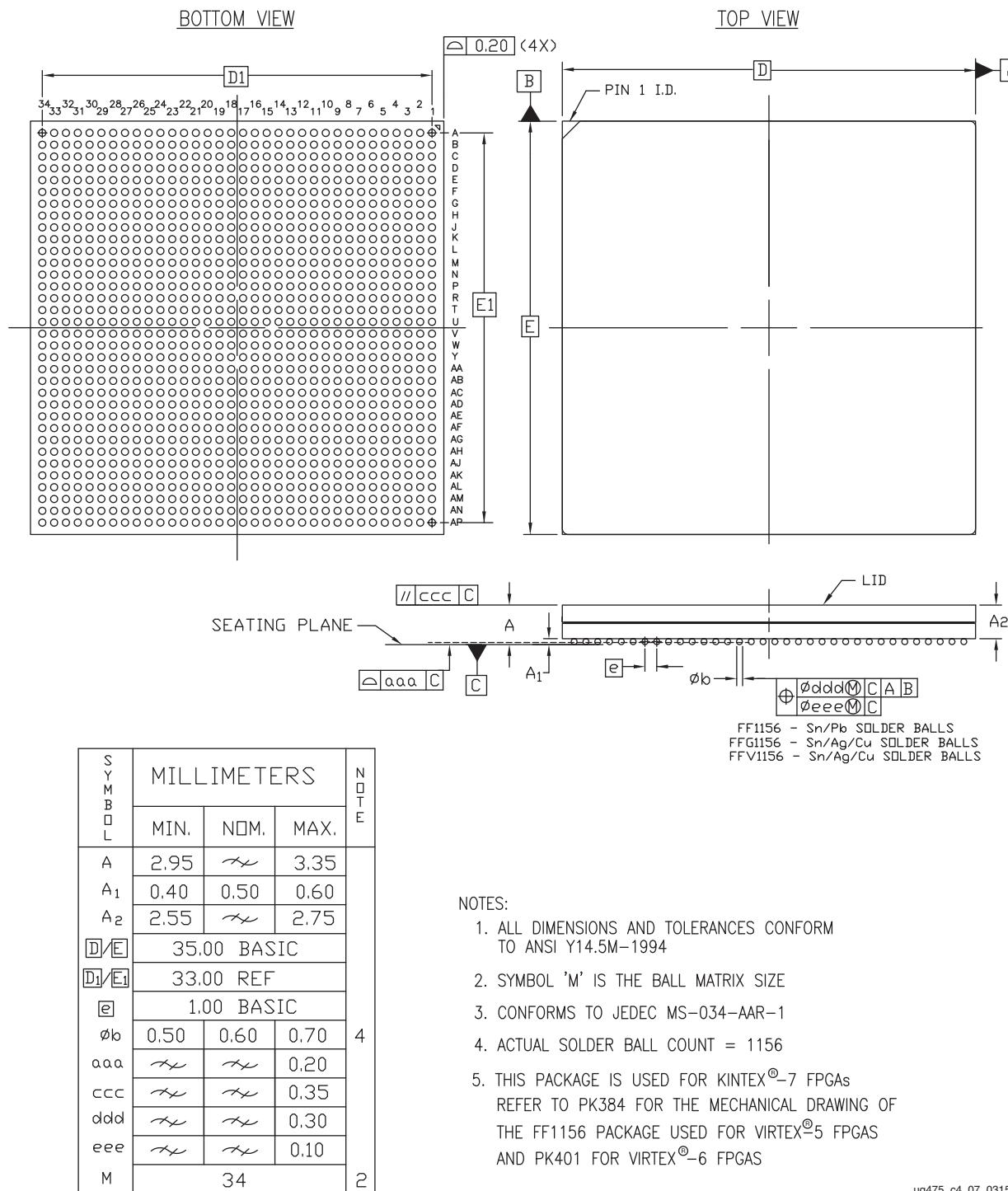
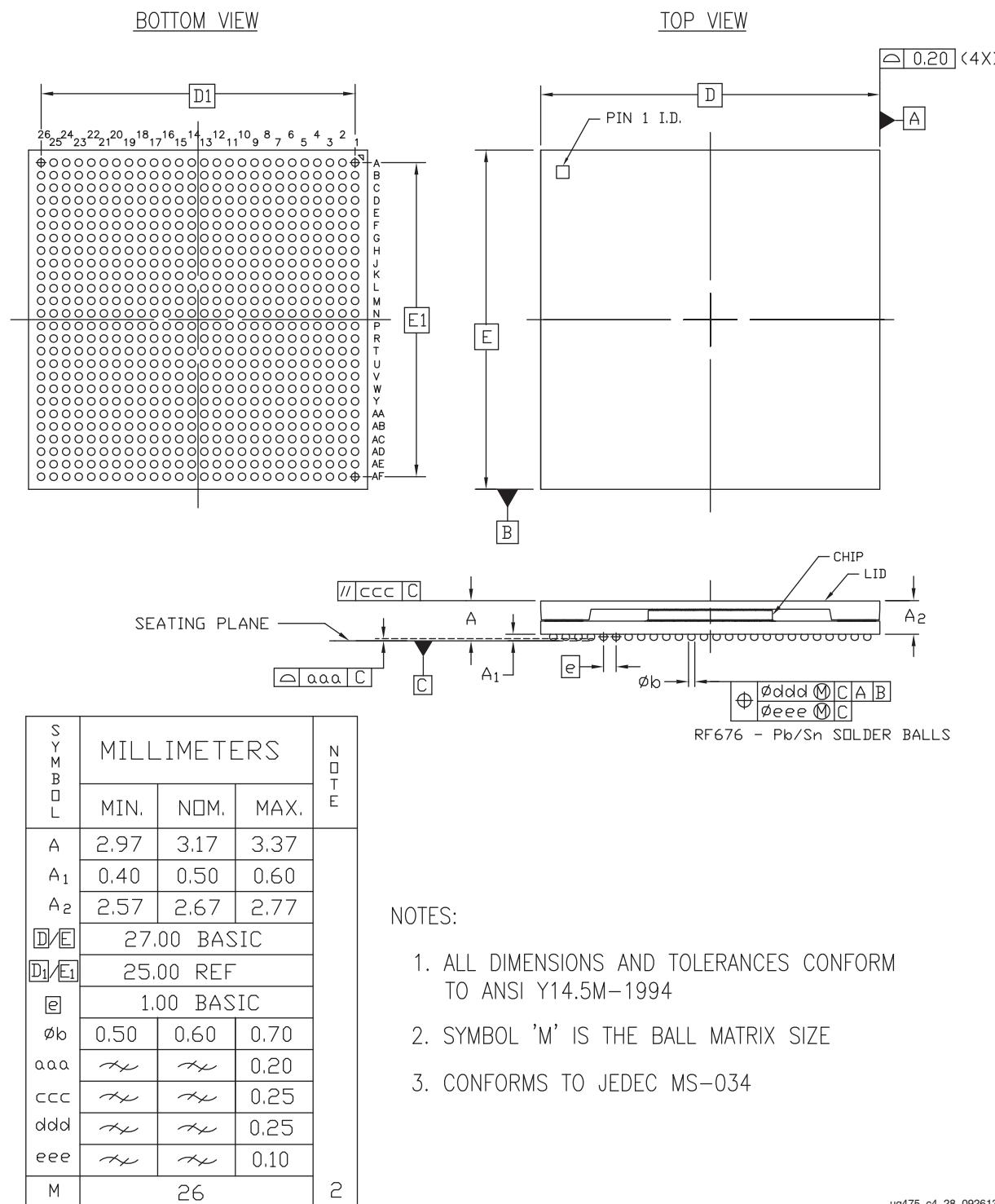


Figure 4-28: FF1156, FFG1156, and FFV1156 Flip-Chip BGA Package Specification for Kintex-7 FPGAs

RF676 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)



ug475_c4_28_092613

Figure 4-29: RF676 Flip-Chip BGA Package Specifications for Kintex-7 FPGAs

RF900 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)

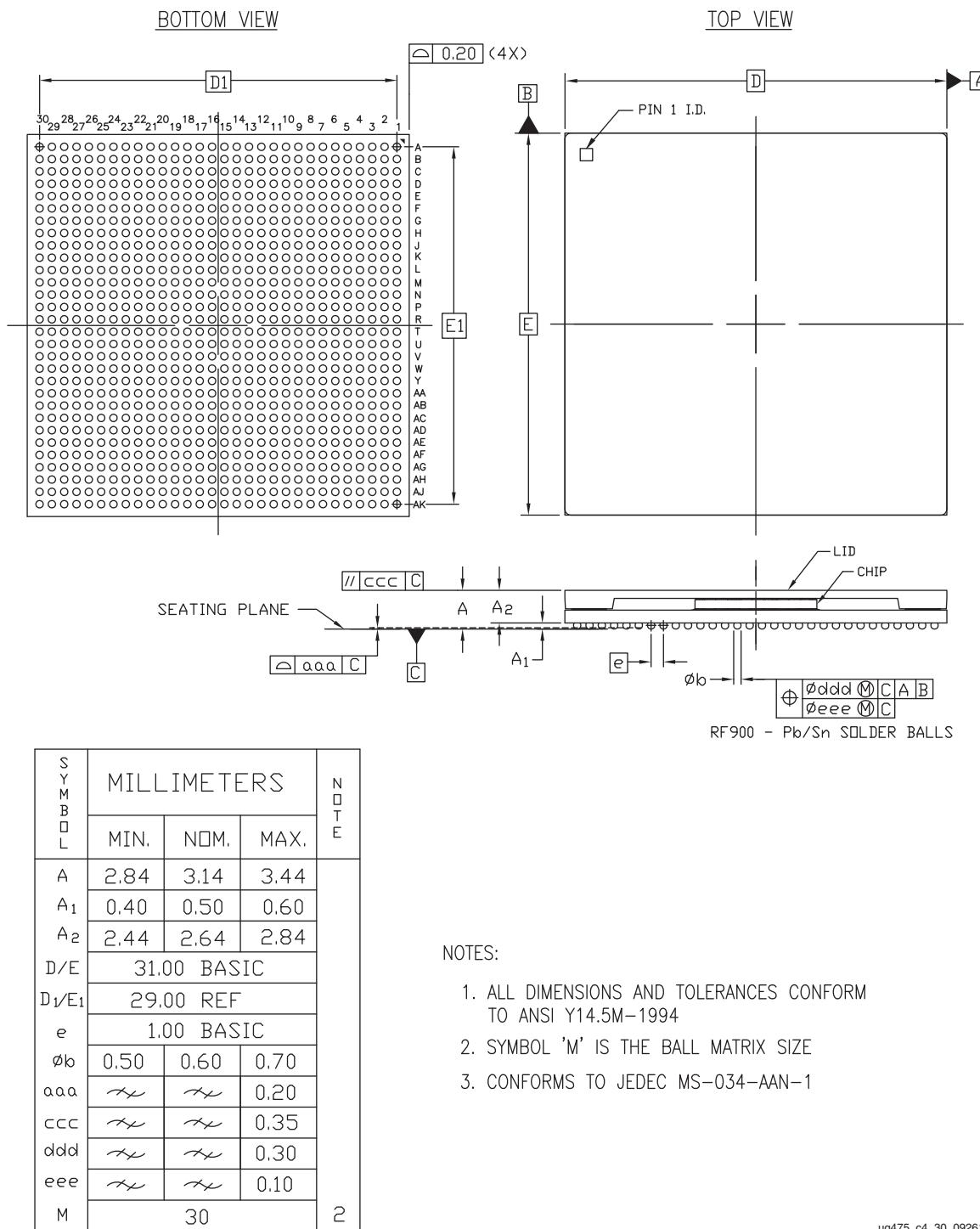
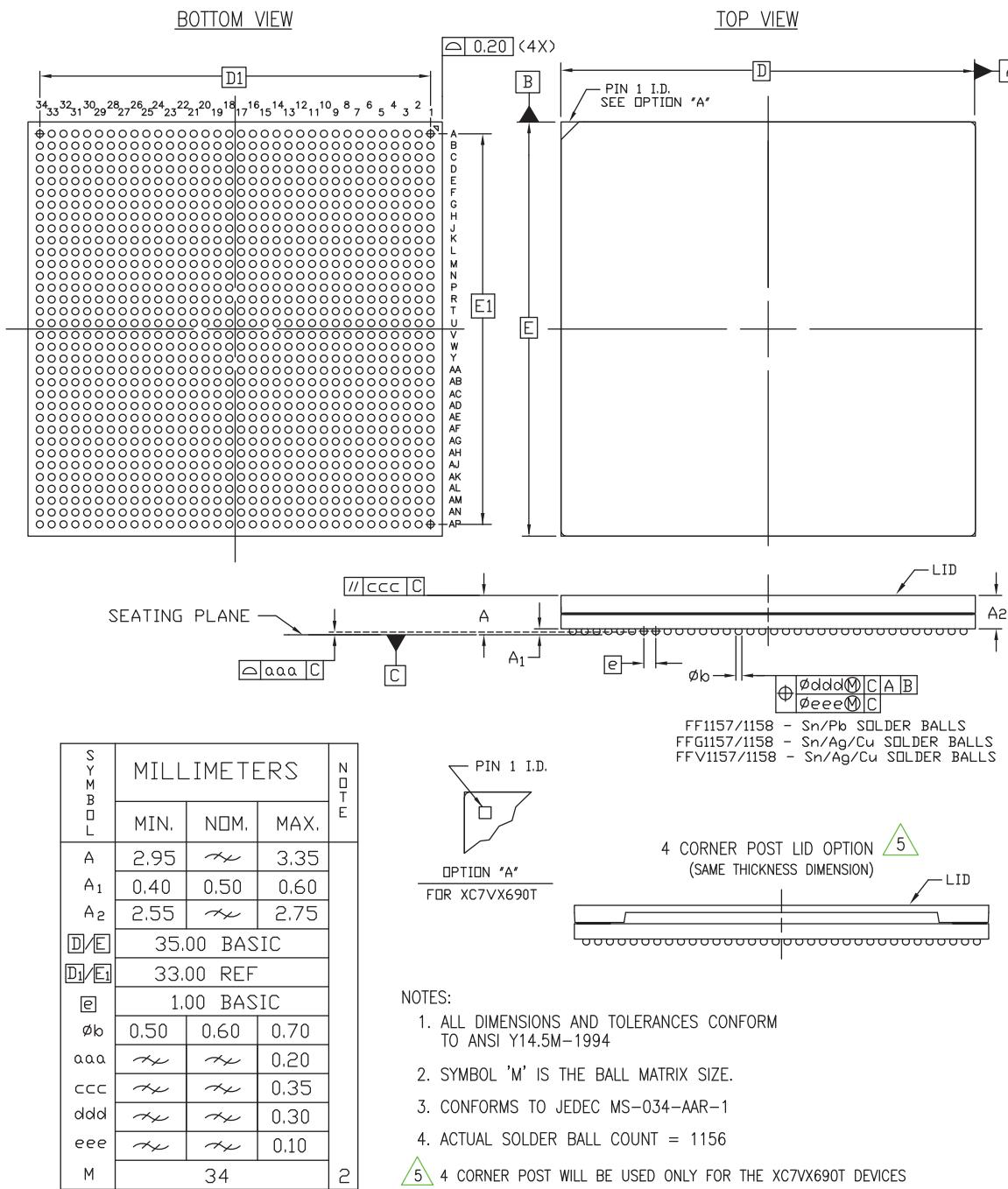


Figure 4-30: RF900 Flip-Chip BGA Package Specifications for Kintex-7 FPGAs

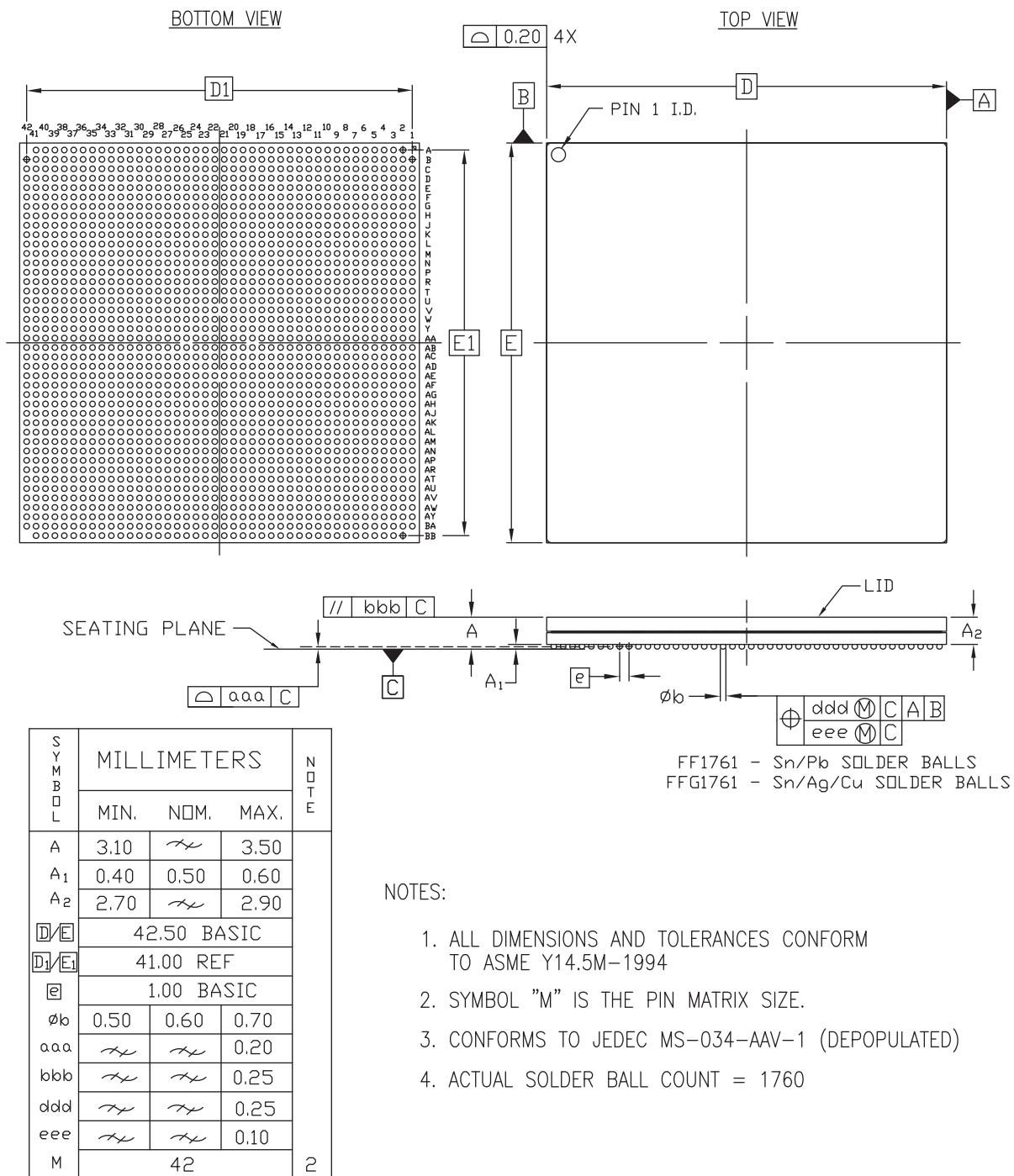
FF1157, FFG1157, FFV1157, FF1158, FFG1158, and FFV1158 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)



ug475_c4_08_031316

Figure 4-31: FF1157, FFG1157, FFV1157, FF1158, FFG1158, and FFV1158 Flip-Chip BGA Package Specification for Virtex®-7 FPGAs

FF1761 and FFG1761 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)



ug475_c4_09_091411

Figure 4-32: FF1761 and FFG1761 Flip-Chip BGA Package Specification for Virtex-7 FPGAs

FFV1761 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)

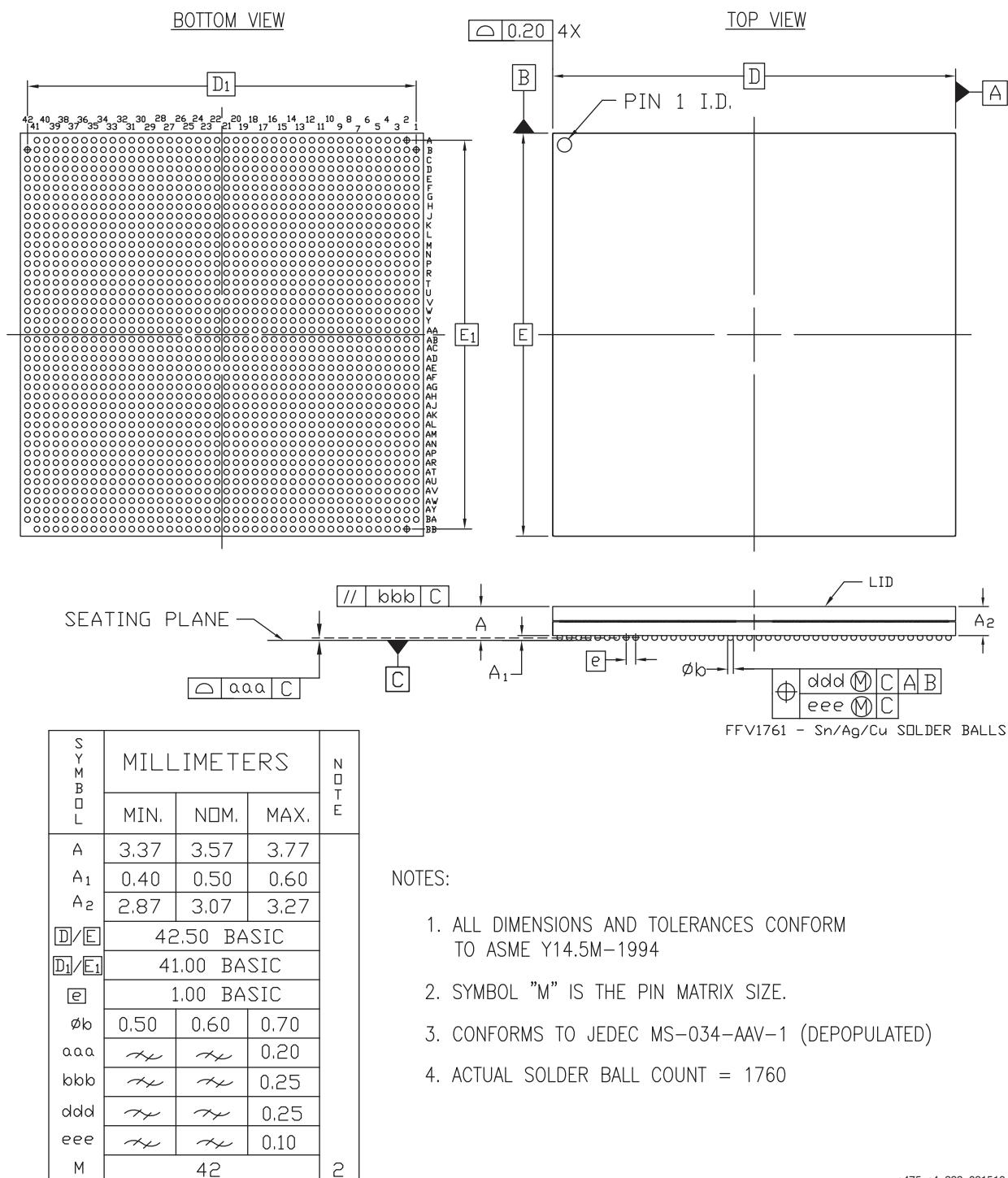
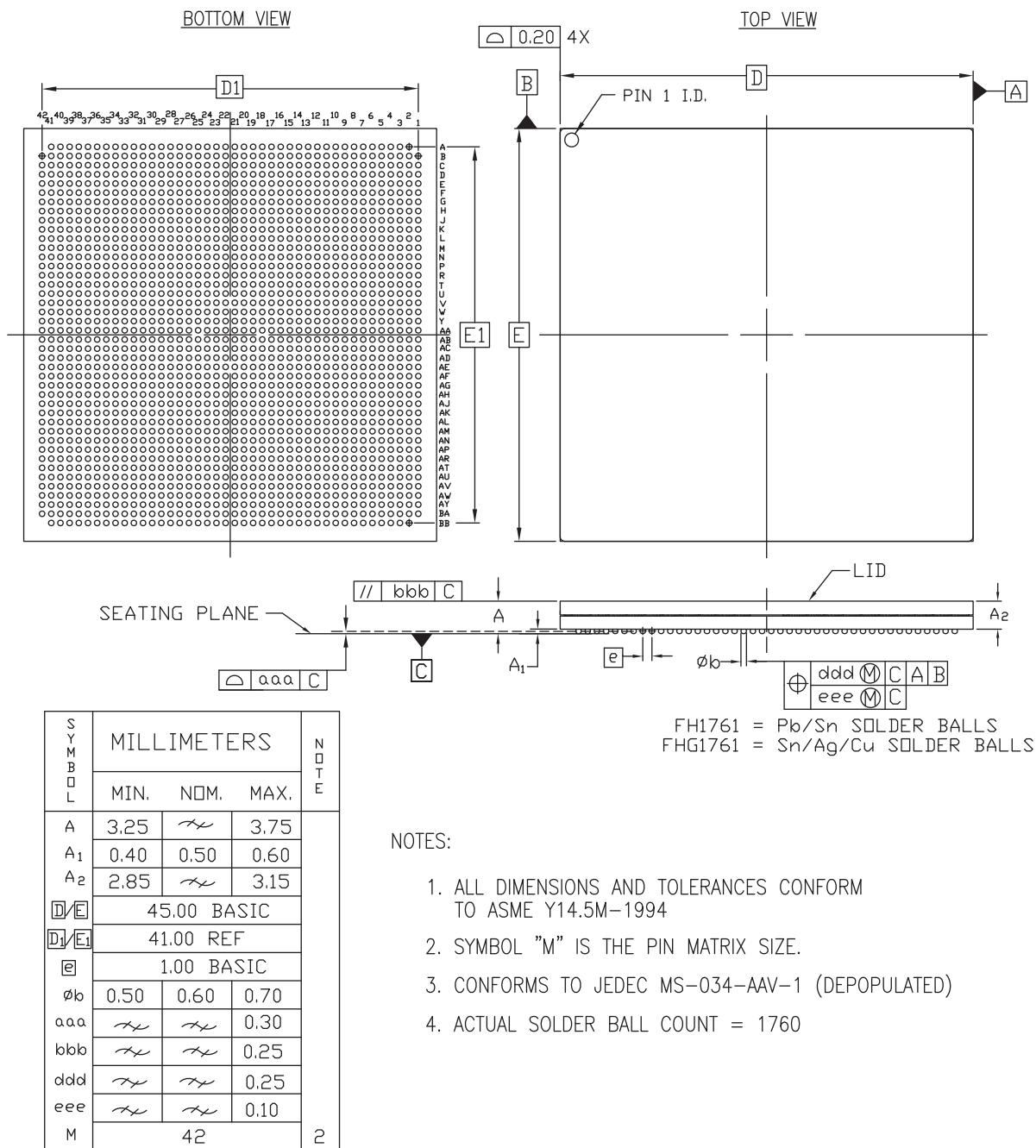


Figure 4-33: FFV1761 Flip-Chip BGA Package Specification for Virtex-7 FPGAs

FH1761 and FHG1761 (Virtex-7 T FPGAs) Flip-Chip BGA (1.0 mm Pitch)



ug475_c4_10_092412

Figure 4-34: FH1761 and FHG1761 Flip-Chip BGA Package Specification for Virtex-7 T FPGAs

FF1926, FFG1926, FF1927, FFG1927, FFV1927, FF1928, FFG1928, FF1930, and FFG1930 (Virtex-7 XT FPGAs) Flip-Chip BGA (1.0 mm Pitch)

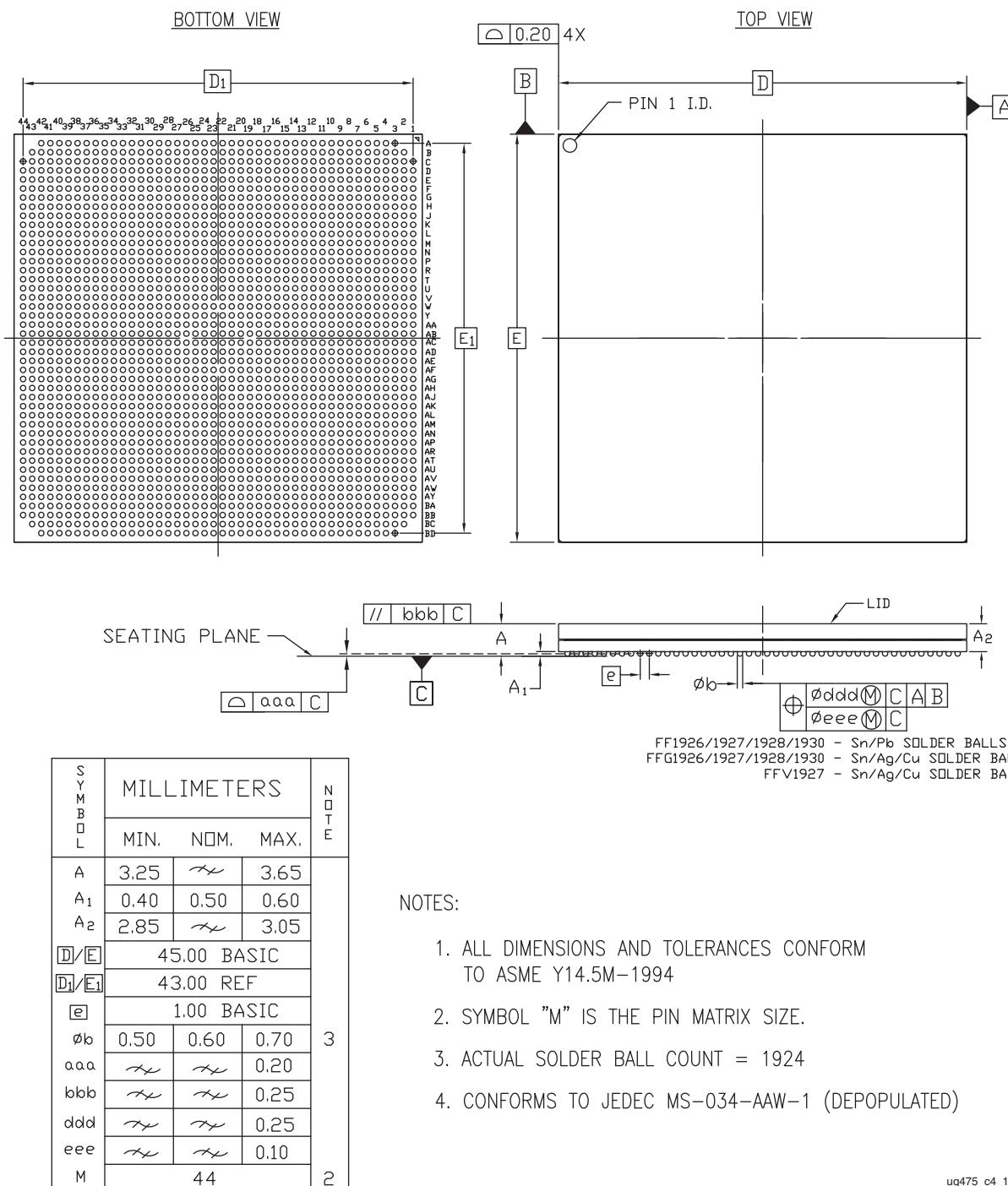


Figure 4-35: FF1926, FFG1926, FF1927, FFG1927, FFV1927, FF1928, FFG1928, FF1930, and FFG1930
Flip-Chip BGA Package Specification for Virtex-7 XT FPGAs

FL1925, FLG1925, FL1926, FLG1926, FL1928, FLG1928, and FL1930, FLG1930 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)

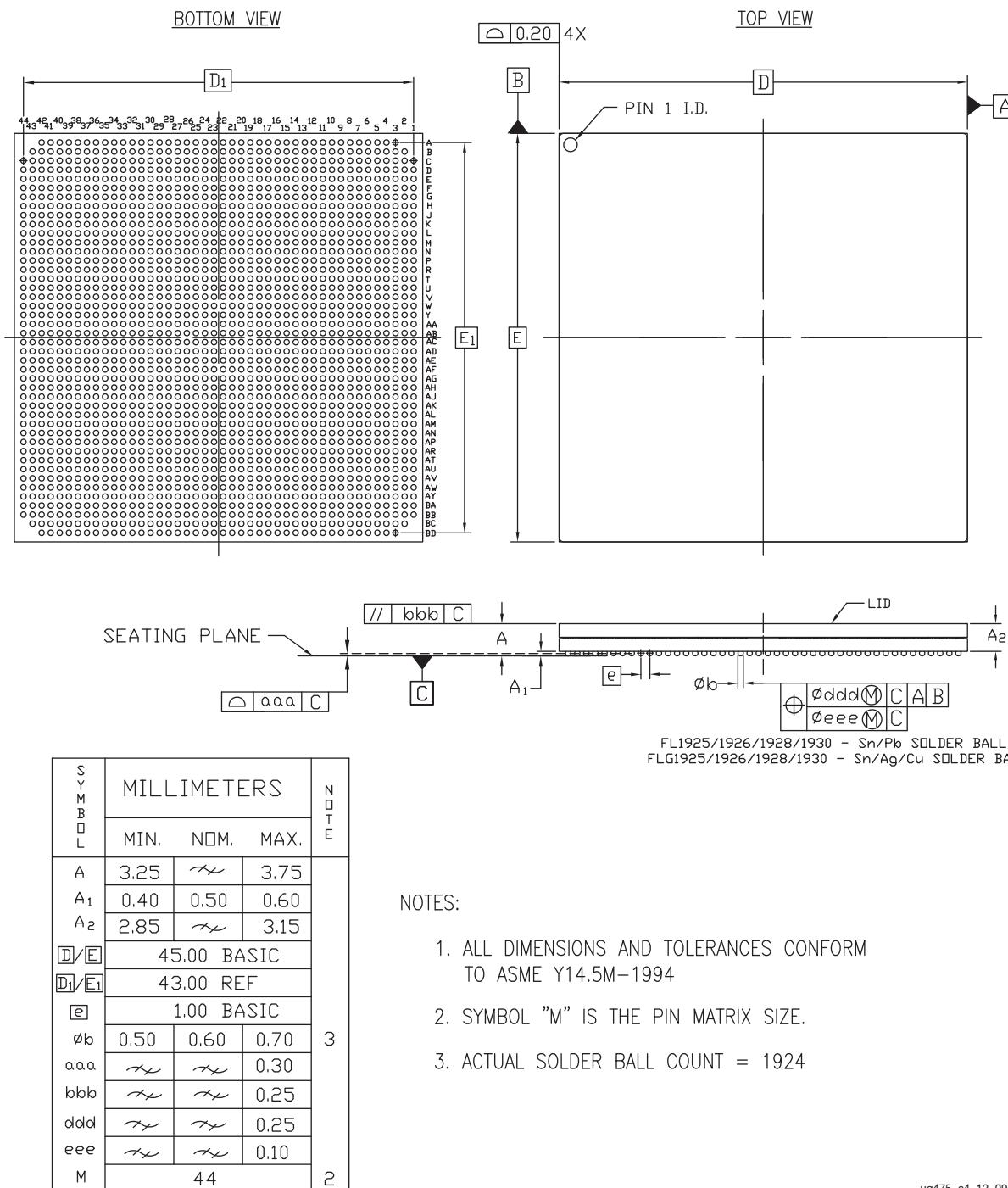


Figure 4-36: FL1925, FLG1925, FL1926, FLG1926, FL1928, FLG1928, and FL1930, FLG1930 Flip-Chip BGA Package Specification for Virtex-7 FPGAs

ug475_c4_12_091712

RF1157 and RF1158 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch)

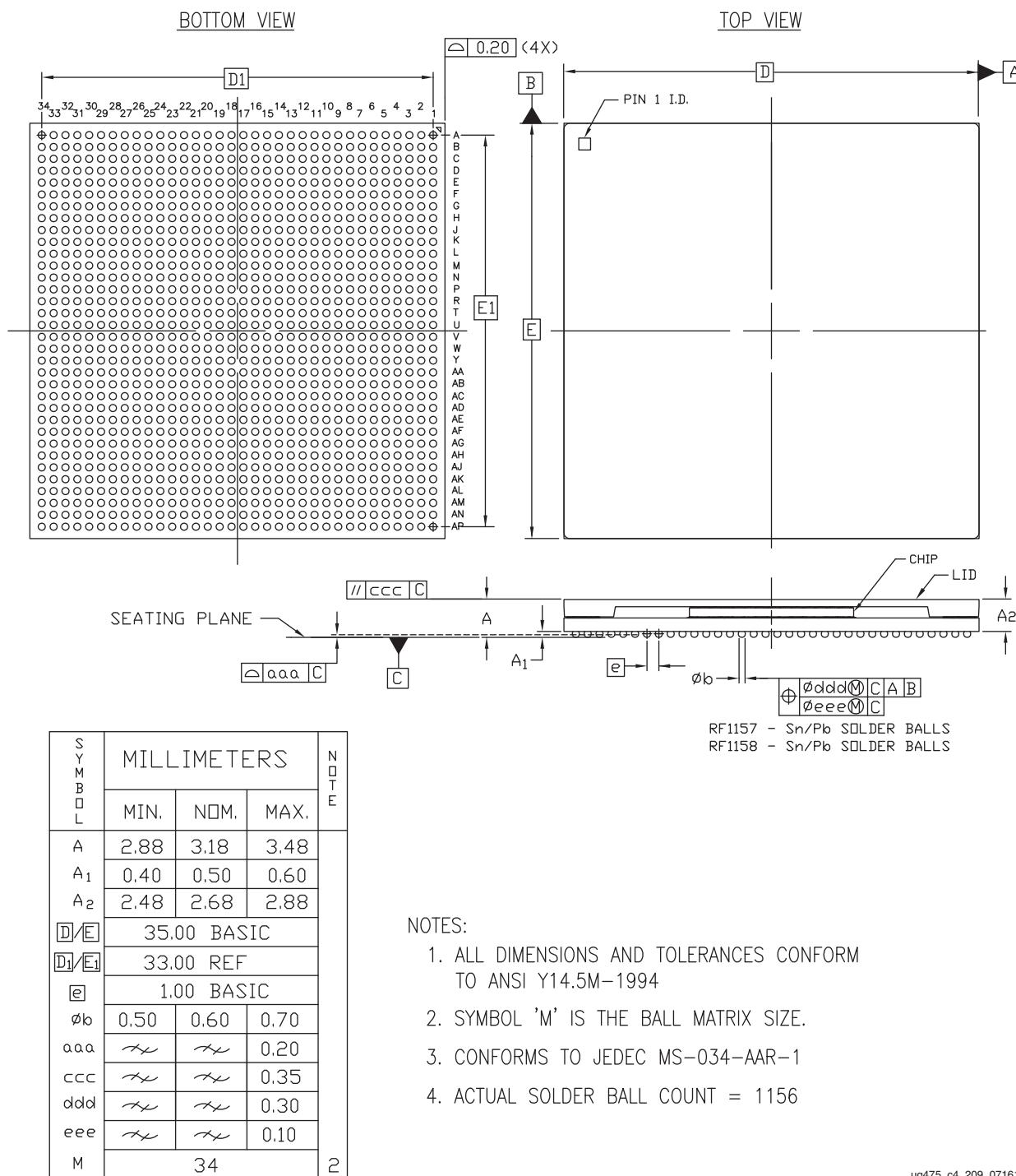


Figure 4-37: RF1157 and RF1158 Flip-Chip BGA Package Specifications for Virtex-7 FPGAs

RF1761 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch)

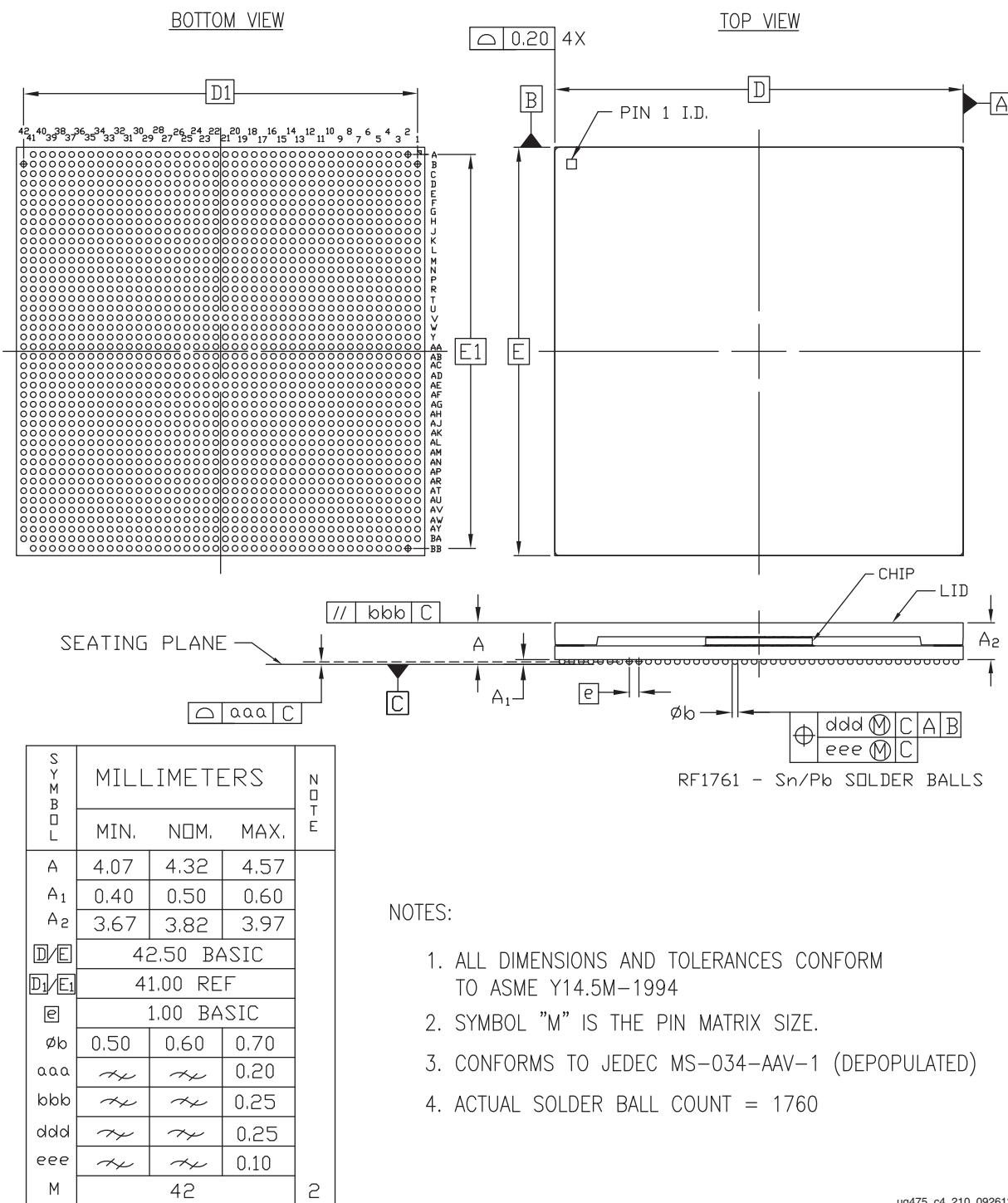
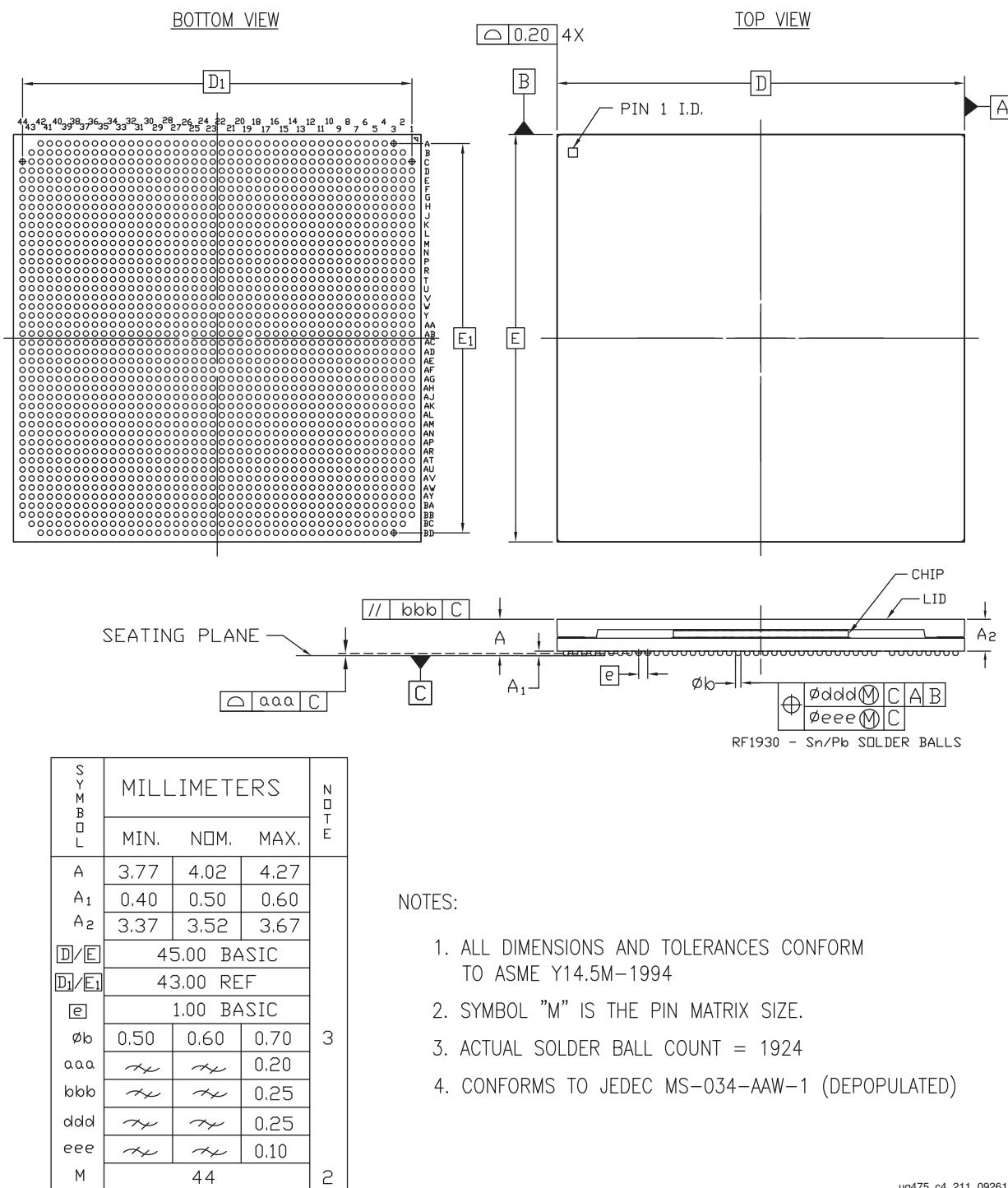


Figure 4-38: RF1761 Flip-Chip BGA Package Specifications for Virtex-7 FPGAs

RF1930 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch)



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Figure 4-39: RF1930 Flip-Chip BGA Package Specifications for Virtex-7 FPGAs

Thermal Specifications

Summary

This chapter provides thermal data associated with 7 series FPGAs packages. The following topics are discussed:

- [Introduction](#)
- [Support for Compact Thermal Models \(CTM\)](#)
- [Thermal Management Strategy](#)
- [Thermal Interface Material](#)
- [Heat Sink Removal Procedure](#)
- [Soldering Guidelines](#)
- [References](#)

Introduction

7 series FPGAs are offered exclusively in thermally efficient flip-chip BGA packages. These 0.5 mm, 0.8 mm, and 1.0 mm flip-chip packages range in pin-count from the smaller 10 x 10 mm CPG236 to the 45 x 45 mm FFG1930. This suite of packages is used to address the various power requirements of the 7 series devices. All 7 series devices are implemented in the 28 nm process technology.

Unlike features in an ASIC or a microprocessor, the combination of FPGA features used in a user application are not known to the component supplier. Therefore, it remains a challenge for Xilinx to predict the power requirements of a given FPGA when it leaves the factory. Accurate estimates are obtained when the board design takes shape. For this purpose, Xilinx offers and supports a suite of integrated device power analysis tools to help users quickly and accurately estimate their design power requirements. 7 series devices are supported similarly to previous FPGA products. The uncertainty of design power requirements makes it difficult to apply canned thermal solutions to fit all users. Therefore, Xilinx devices do not come with preset thermal solutions. The user's operating conditions dictate the appropriate solution.

[Table 5-1](#) shows the thermal resistance data for 7 series devices (grouped in the packages offered). The data includes junction-to-ambient in still air, junction-to-case, and junction-to-board data based on standard JEDEC four-layer measurements.

Note: The data in [Table 5-1](#) is for device/package comparison purposes only. Do not apply directly to your system design. Attempts to recreate this data are only valid using the transient 2-phase measurement techniques outlined in JESD51-14.

- Thermal data is available on the Xilinx website at:
www.xilinx.com/cgi-bin/thermal/thermal.pl

Table 5-1: Thermal Resistance Data—All Devices

Package	Package Body Size	Devices	θ_{JB} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	$\theta_{JA-Effective}$ (°C/W) ⁽¹⁾		
						@250 LFM	@500 LFM	@750 LFM
Artix®-7 FPGAs								
CP/CPG236	10 x 10	XC7A15T	7.9	24.8	5.29	20.3	18.9	18.0
CP/CPG236	10 x 10	XC7A35T	7.9	24.8	5.29	20.3	18.9	18.0
CP/CPG236	10 x 10	XC7A50T	7.9	24.8	5.29	20.3	18.9	18.0
CS/CSG324	15 x 15	XC7A15T	6.9	19.6	4.03	15.4	14.3	13.6
CS/CSG324	15 x 15	XC7A35T	6.9	19.6	4.03	15.4	14.3	13.6
CS/CSG324	15 x 15	XC7A50T	6.9	19.6	4.03	15.4	14.3	13.6
CS/CSG324	15 x 15	XC7A75T	5.7	18.2	3.25	14.1	13.0	12.3
CS/CSG324	15 x 15	XC7A100T	5.7	18.2	3.25	14.1	13.0	12.3
CS/CSG324	15 x 15	XQ7A100T	5.7	18.2	3.25	14.1	13.0	12.3
CS/CSG325	15 x 15	XC7A15T	6.9	19.6	4.05	15.4	14.3	13.6
CS/CSG325	15 x 15	XC7A35T	6.9	19.6	4.05	15.4	14.3	13.6
CS/CSG325	15 x 15	XC7A50T	6.9	19.6	4.05	15.4	14.3	13.6
CS/CSG325	15 x 15	XQ7A50T	6.9	19.6	4.05	15.4	14.3	13.6
FT/FTG256	17 x 17	XC7A15T	8.4	19.8	4.24	15.6	14.4	13.7
FT/FTG256	17 x 17	XC7A35T	8.4	19.8	4.24	15.6	14.4	13.7
FT/FTG256	17 x 17	XC7A50T	8.4	19.8	4.24	15.6	14.4	13.7
FT/FTG256	17 x 17	XC7A75T	6.9	18.2	3.34	14.1	12.9	12.2
FT/FTG256	17 x 17	XC7A100T	6.9	18.2	3.34	14.1	12.9	12.2
SB/SBG/SBV484	19 x 19	XC7A200T	5.0	14.8	0.08	10.9	9.8	9.2
RS484	19 x 19	XQ7A200T	4.7	14.2	0.33	9.9	8.7	8.0
FB/FBG/FBV484	23 x 23	XC7A200T	4.8	13.9	0.08	9.9	8.9	8.3
FG/FGG484	23 x 23	XC7A15T	8.7	17.7	4.89	13.6	12.6	12.1
FG/FGG484	23 x 23	XC7A35T	8.7	17.7	4.89	13.6	12.6	12.1
FG/FGG484	23 x 23	XC7A50T	8.7	17.7	4.89	13.6	12.6	12.1
FG/FGG484	23 x 23	XQ7A50T	9.1	18.1	5.42	14.1	13.0	12.5
FG/FGG484	23 x 23	XC7A75T	6.8	15.8	3.85	12.1	11.0	10.4
FG/FGG484	23 x 23	XC7A100T	6.8	15.8	3.85	12.1	11.0	10.4
FG/FGG484	23 x 23	XQ7A100T	6.8	15.8	3.85	12.1	11.0	10.4
RB484	23 x 23	XQ7A200T	4.0	12.5	0.26	8.3	7.2	6.7
FB/FBG/FBV676	27 x 27	XC7A200T	4.7	13.0	0.08	9.2	8.2	7.7
FG/FGG676	27 x 27	XC7A75T	6.8	15.0	3.71	11.2	10.2	9.7

Table 5-1: Thermal Resistance Data—All Devices (Cont'd)

Package	Package Body Size	Devices	θ_{JB}	θ_{JA}	θ_{JC}	$\theta_{JA\text{-Effective}} \text{ (}^{\circ}\text{C/W)}^{(1)}$		
			($^{\circ}\text{C/W}$)	($^{\circ}\text{C/W}$)	($^{\circ}\text{C/W}$)	@250 LFM	@500 LFM	@750 LFM
FG/FGG676	27 x 27	XC7A100T	6.8	15.0	3.71	11.2	10.2	9.7
RB676	27 x 27	XQ7A200T	3.7	11.4	0.33	7.3	6.2	5.6
FF/FFG/FFV1156	35 x 35	XC7A200T	2.6	9.3	0.32	6.1	5.2	4.7
Kintex®-7 FPGAs								
FB/FBG/FBV484	23 x 23	XC7K70T	6.8	16.4	0.13	11.7	10.7	10.1
		XC7K160T	5.3	14.6	0.10	10.5	9.5	8.9
FB/FBG/FBV676	27 x 27	XC7K70T	6.7	15.7	0.13	11.8	10.8	10.2
		XC7K160T	5.2	14.0	0.10	9.8	8.8	8.3
		XC7K325T	4.2	12.9	0.06	8.9	8.0	7.5
		XC7K410T	3.7	12.2	0.05	8.6	7.6	7.1
FF/FFG/FFV676	27 x 27	XC7K160T	4.0	11.7	0.41	7.5	6.4	5.8
		XC7K325T	3.5	11.1	0.26	7.3	6.3	5.8
		XC7K410T	3.3	10.9	0.20	7.0	6.0	5.5
RF676	27 x 27	XQ7K325T	3.5	11.1	0.26	7.3	6.3	5.8
		XQ7K410T	3.3	10.9	0.20	7.0	6.0	5.5
FB/FBG/FBV900	31 x 31	XC7K325T	4.3	12.0	0.06	8.9	7.9	7.3
		XC7K410T	3.7	11.4	0.05	8.3	7.3	6.7
FF/FFG/FFV900	31 x 31	XC7K325T	2.8	9.7	0.26	6.2	5.4	5.0
		XC7K410T	2.6	9.5	0.19	6.0	5.2	4.9
RF900	31 x 31	XQ7K325T	3.3	10.0	0.26	6.4	5.4	4.9
		XQ7K410T	3.0	9.8	0.20	6.3	5.4	4.9
FF/FFG/FFV901	31 x 31	XC7K355T	3.2	10.0	0.23	6.3	5.3	4.8
		XC7K420T	2.9	9.6	0.17	6.2	5.3	4.8
		XC7K480T	2.9	9.6	0.17	6.2	5.3	4.8
FF/FFG/FFV1156	35 x 35	XC7K420T	2.4	8.7	0.17	5.7	4.7	4.3
		XC7K480T	2.4	8.7	0.17	5.7	4.7	4.3
Virtex®-7 T FPGAs								
FF/FFG1157	35 x 35	XC7V585T	2.3	8.7	0.14	5.6	4.8	4.3
RF1157	35 x 35	XQ7V585T	2.7	8.9	0.15	5.8	4.8	4.3
FF/FFG1761	42.5 x 42.5	XC7V585T	2.1	7.6	0.11	4.9	4.1	3.7
RF1761	42.5 x 42.5	XQ7V585T	2.4	7.8	0.11	4.9	4.0	3.5
FH/FHG1761	45 x 45	XC7V2000T	2.0	7.0	0.05	4.3	3.5	3.1

Table 5-1: Thermal Resistance Data—All Devices (Cont'd)

Package	Package Body Size	Devices	θ_{JB}	θ_{JA}	θ_{JC}	$\theta_{JA-Effective}$ (°C/W) ⁽¹⁾		
			(°C/W)	(°C/W)	(°C/W)	@250 LFM	@500 LFM	@750 LFM
FL/FLG1925	45 x 45	XC7V2000T	1.7	6.9	0.06	4.2	3.4	3.0
Virtex-7 XT FPGAs								
FF/FFG/FFV1157	35 x 35	XC7VX330T	2.5	8.9	0.19	5.8	4.9	4.5
		XC7VX415T	2.3	8.8	0.16	5.7	4.8	4.4
		XC7VX485T	2.3	8.7	0.13	5.6	4.7	4.3
		XC7VX690T	2.3	8.7	0.09	5.5	4.6	4.1
RF1157	35 x 35	XQ7VX330T	2.9	9.3	0.19	6.0	5.0	4.4
		XQ7VX690T	2.3	8.7	0.09	5.3	4.4	3.9
FF/FFG/FFV1158	35 x 35	XC7VX415T	2.3	8.8	0.16	5.7	4.8	4.4
		XC7VX485T	2.3	8.7	0.13	5.6	4.7	4.3
		XC7VX550T	2.3	8.7	0.09	5.5	4.6	4.1
		XC7VX690T	2.3	8.7	0.09	5.5	4.6	4.1
RF1158	35 x 35	XQ7VX690T	2.3	8.7	0.09	5.3	4.4	3.9
FF/FFG/FFV1761	42.5 x 42.5	XC7VX330T	2.3	7.8	0.19	5.1	4.3	3.9
		XC7VX485T	2.1	7.6	0.13	4.9	4.1	3.6
		XC7VX690T	1.9	7.5	0.09	4.7	3.9	3.5
RF1761	42.5 x 42.5	XQ7VX485T	2.3	7.7	0.14	4.8	3.9	3.4
		XQ7VX330T	2.7	8.0	0.20	5.0	4.1	3.6
		XQ7VX690T	2.1	7.5	0.09	4.7	3.8	3.3
FF/FFG1926	45 x 45	XC7VX690T	1.9	7.1	0.09	4.5	3.7	3.3
		XC7VX980T	1.8	7.1	0.09	4.4	3.6	3.2
FF/FFG/FFV1927	45 x 45	XC7VX415T	2.1	7.4	0.16	4.7	3.9	3.5
		XC7VX485T	2.0	7.3	0.13	4.6	3.8	3.4
		XC7VX550T	1.8	7.1	0.09	4.4	3.6	3.2
		XC7VX690T	1.8	7.1	0.09	4.4	3.6	3.2
FF/FFG1928	45 x 45	XC7VX980T	1.8	7.1	0.09	4.4	3.6	3.2
FF/FFG1930	45 x 45	XC7VX485T	2.0	7.3	0.13	4.8	3.9	3.5
		XC7VX690T	1.9	7.1	0.09	4.5	3.7	3.3
		XC7VX980T	1.8	7.1	0.09	4.4	3.6	3.2
RF1930	45 x 45	XQ7VX485T	2.4	7.5	0.14	4.8	3.9	3.5
		XQ7VX690T	2.2	7.3	0.10	4.5	3.6	3.1
		XQ7VX980T	2.1	7.3	0.09	4.5	3.6	3.1

Table 5-1: Thermal Resistance Data—All Devices (Cont'd)

Package	Package Body Size	Devices	θ_{JB}	θ_{JA}	θ_{JC}	$\theta_{JA\text{-Effective}} \text{ (}^{\circ}\text{C/W}\text{)}^{(1)}$		
			(°C/W)	(°C/W)	(°C/W)	@250 LFM	@500 LFM	@750 LFM
FL/FLG1926	45 x 45	XC7VX1140T	1.7	6.9	0.06	4.2	3.4	3.0
FL/FLG1928	45 x 45	XC7VX1140T	1.7	6.9	0.06	4.2	3.4	3.0
FL/FLG1930	45 x 45	XC7VX1140T	1.7	6.9	0.06	4.2	3.4	3.0

Notes:

1. All $\theta_{JA\text{-Effective}}$ values assume no heat sink and include thermal dissipation through a standard JEDEC four-layer board. The Xilinx power estimation tools (PPE, Vivado® Power Analysis, and Xilinx Power Estimator), which require detailed board dimensions and layer counts, are useful for deriving more precise $\theta_{JA\text{-Effective}}$ values.

Support for Compact Thermal Models (CTM)

Table 5-1 provides the traditional thermal resistance data for 7 series devices. These resistances are measured using a prescribed JEDEC standard that might not necessarily reflect the user's actual board conditions and environment. The quoted θ_{JA} and θ_{JC} numbers are environmentally dependent, and JEDEC has traditionally recommended that these be used with that awareness. For more accurate junction temperature prediction, these might not be enough, and a system-level thermal simulation might be required. Though Xilinx continues to support these figure of merit data, for 7 series FPGAs, boundary conditions independent compact thermal models (BCI-CTM) are also available to assist users in their thermal simulations.

Two-resistor as well as eight to ten-resistor network models are offered for all 7 series devices. These compact models seek to capture the thermal behavior of the packages more accurately at predetermined critical points (junction, case, top, leads, and so on) with the reduced set of nodes as illustrated in Figure 5-1.

Unlike a full 3D model, these are computationally efficient and work well in an integrated system simulation environment. Delphi CTM models are available for download on the Xilinx website (under the Device Model tab) at:

www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/device-models.html

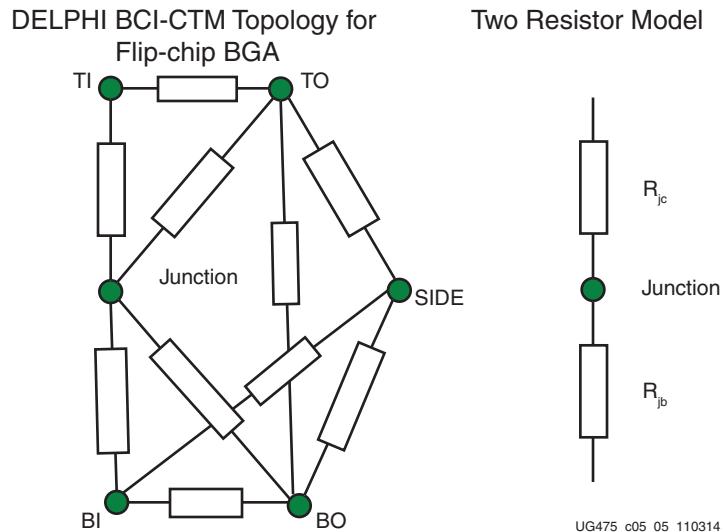


Figure 5-1: Thermal Model Topologies

Note: Xilinx recommends use of the Delphi thermal model during thermal modeling of a package. The Delphi thermal model includes consideration of the thermal interface material parameters and the manufacture variation on the thermal solution. Examples of manufacture variations include the tolerance in airflow from a fan, the tolerance on performance of the heat pipe and vapor chamber, and the manufacture variation of the attachment of fins to the heat-sink base and the flatness of the surface.

Thermal Management Strategy

As described in this section, Xilinx relies on a multi-pronged approach with regards to the heat-dissipating potential of 7 series devices.

Cavity-Up Plastic BGA Packages

BGA is a plastic package technology that utilizes area array solder balls at the bottom of the package to make electrical contact with the circuit board in the users system. The area array format of solder balls reduces package size considerably when compared to leaded products. It also results in improved electrical performance as well as having higher manufacturing yields. The substrate is made of a multi-layer BT (bismaleimide triazene) epoxy-based material. Power and GND pins are grouped together and signal pins are assigned to the perimeter for ease of routing on the board. The package is offered in a die-up format and contains a wire-bond device covered with a mold compound. As shown in the cross section of [Figure 5-2](#), the BGA package contains a wire-bond die on a single-core printed circuit board with an overmold.

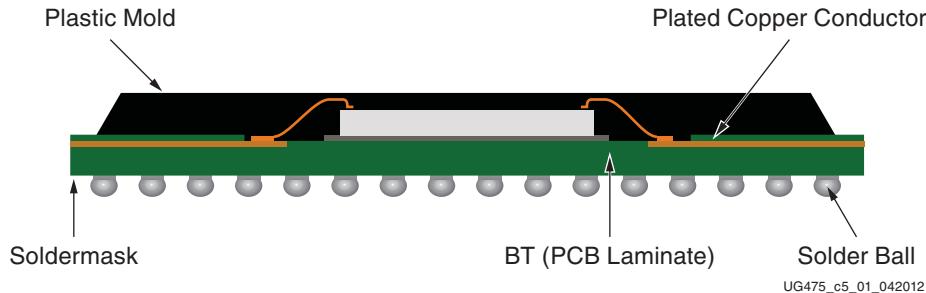


Figure 5-2: Cavity-Up Ball Grid Array Package

The key features/advantages of cavity-up BGA packages are:

- Low profile and small footprint
- Enhanced thermal performance
- Excellent board-level reliability

Wire-Bond Packages

Wire-bond packages meet the demands required by miniaturization while offering improved performance. Applications for wire-bond packages are targeted to portable and consumer products where board space is of utmost importance, miniaturization is a key requirement, and power consumption/dissipation must be low. By employing 7 series FPGA wire-bond packages, system designers can dramatically reduce board area requirements. Xilinx wire-bond packages are rigid BT-based substrates (see [Figure 5-3](#)).

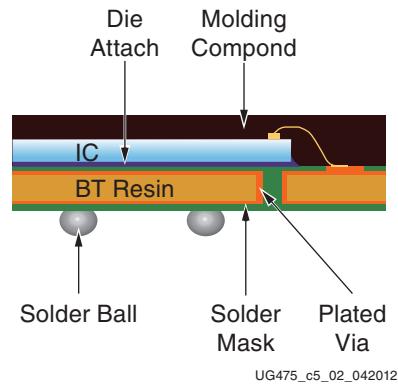


Figure 5-3: Rigid BT-Based Substrate Wire-Bond Packages

The key features/advantages of wire-bond packages are:

- An extremely small form factor which significantly reduces board area requirements for portable and wireless designs and PC add-in card applications.
- Lower inductance and lower capacitance
- The absence of thin, fragile leads found on other small package types
- A very thin, light-weight package

Flip-Chip Packages

For larger 7 series devices, Xilinx offers the flip-chip BGA packages, which present a low thermal path. These packages incorporate a heat spreader with additional thermal interface material (TIM), as shown in [Figure 5-4](#).

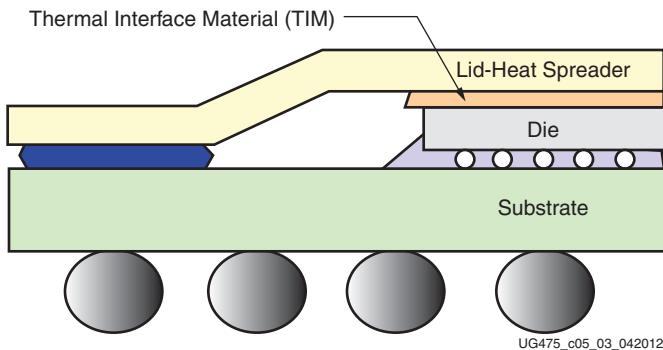


Figure 5-4: Heat Spreader with Thermal Interface Material

Materials with better thermal conductivity and consistent process applications deliver low thermal resistance up to the heat spreader. The junction-to-case thermal resistance (top of heat spreader) of all 7 series FPGA packages is typically less than $0.20^{\circ}\text{C}/\text{W}$. These packages deliver a low resistance platform for heat-sink applications.

A parallel effort to ensure optimized package electrical return paths produces the added benefit of enhanced power and ground plane arrangement in the packages. A boost in copper density on the planes improves the overall thermal conductivity through the laminate. In addition, the extra dense and distributed via fields in the package increase the vertical thermal conductivity. These packages offer up to 20% lower θ_{JB} compared to previous flip-chip packages.

System Level Heat Sink Solutions

To complete a comprehensive thermal management strategy, an overall thermal budget that includes custom or OEM heat sink solutions depends on the physical and mechanical constraints of the system. A heat-sink solution, managed by the system-level designer, should be tailored to the design and specific system constraints. This includes understanding the inherent device capabilities for delivering heat to the surface.

Thermal Interface Material

When installing heat sinks for Xilinx FPGAs, a suitable thermal interface material (TIM) must be used. This thermal material significantly aids the transfer of heat from the component to the heat sink. For optimum heat transfer, Xilinx recommends the use of thermal interface materials.

For lidless flip-chip BGAs, the surface of the silicon contacts the heat sink. For lidded flip-chip BGAs, the lid contacts the heat sink. The surface size of the lidless flip-chip BGA and lidded flip-chip BGA are different. Xilinx recommends a different type of thermal material for long-term use with each type of flip-chip BGA package.

Thermal interface material is needed because even the largest heat sink and fan cannot effectively cool an FPGA unless there is good physical contact between the base of the heat sink and the top of the FPGA. The surfaces of both the heat sink and the FPGA silicon are

not absolutely smooth. This surface roughness is observed when examined at a microscopic level. Because surface roughness reduces the effective contact area, attaching a heat sink without a thermal interface material is not sufficient due to inadequate surface contact.

A thermal interface material such as phase-change material, thermal grease, or thermal pads fills these gaps and allows effective transference of heat between the FPGA die and the heat sink.

The selection of the thermal interface (TIM) between the package and the thermal management solution is critical to ensure the lowest thermal contact resistance. Therefore, the following parameters must be considered.

1. The flatness of the lid and the flatness of the contact surface of the thermal solution.
2. The applied pressure of the thermal solution on the package, which must be within the allowable maximum pressure that can be applied on the package.
3. The total thermal contact of the thermal interface material. This value is determined based on the parameters in [step 1](#) and [step 2](#), which are published in the data sheet of the thermal interface supplier.

Types of TIM

There are many type of TIM available for sale. The most commonly used thermal interface materials are listed.

- Thermal grease
- Thermal pads
- Phase change material
- Thermal paste
- Thermal adhesives
- Thermal tape

Guidelines for Thermal Interface Materials

Five factors affect the choice, use, and performance of the interface material used between the processor and the heat sink:

- [Thermal Conductivity of the Material](#)
- [Electrical Conductivity of the Material](#)
- [Spreading Characteristics of the Material](#)
- [Long-Term Stability and Reliability of the Material](#)
- [Ease of Application](#)
- [Applied Pressure from Heat Sink to the Package via Thermal Interface Materials](#)

Thermal Conductivity of the Material

Thermal conductivity is the quantified ability of any material to transfer heat. The thermal conductivity of the interface material has a significant impact on its thermal performance. The higher the thermal conductivity, the more efficient the material is at transferring heat. Materials that have a lower thermal conductivity are less efficient at transferring heat, causing a higher temperature differential to exist across the interface. To overcome this less efficient heat transfer, a better cooling solution (typically, a more costly solution) must be used to achieve the desired heat dissipation.

Electrical Conductivity of the Material

Some metal-based TIM compounds are electrically conductive. Ceramic-based compounds are typically not electrically conductive. Manufacturers produce metal-based compounds with low-electrical conductivity, but some of these materials are not completely electrically inert. Metal-based thermal compounds are not hazardous to the FPGA die itself, but other elements on the FPGA or motherboard can be at risk if they become contaminated by the compound. For this reason, Xilinx does not recommend the use of electrically conductive thermal interface material.

Spreading Characteristics of the Material

The spreading characteristics of the thermal interface material determines its ability, under the pressure of the mounted heat sink, to spread and fill in or eliminate the air gaps between the FPGA and the heat sink. Because air is a very poor thermal conductor, the more completely the interface material fills the gaps, the greater the heat transference.

Long-Term Stability and Reliability of the Material

The long-term stability and reliability of the thermal interface material is described as the ability to provide a sufficient thermal conductance even after an extended time or extensive. Low-quality compounds can harden or leak out over time (the pump-out effect), leading to overheating or premature failure of the FPGA. High-quality compounds provide a stable and reliable thermal interface material throughout the lifetime of the device. Thermal greases with higher viscosities are typically more resistant to pump out effects on lidless devices.

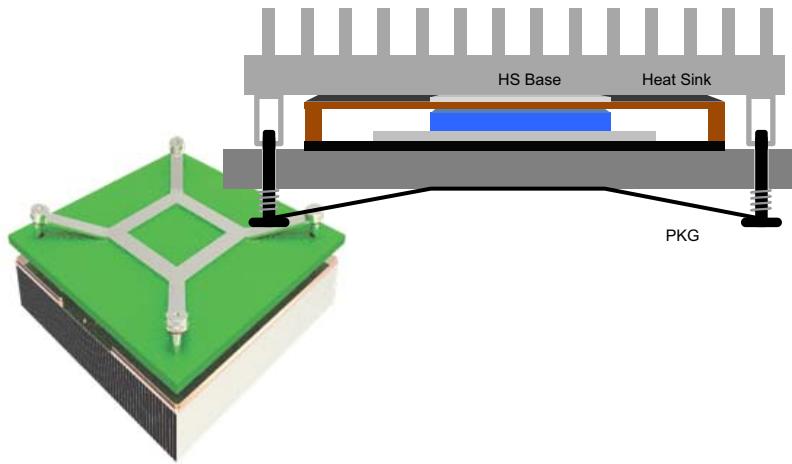
Ease of Application

A spreadable thermal grease requires the surface mount supplier to carefully use the appropriate amount of material. Too much or too little material can cause problems. The thermal pad is a fixed size and is therefore easier to apply in a consistent manner.

Applied Pressure from Heat Sink to the Package via Thermal Interface Materials

Xilinx recommends that the applied pressure on the package be in the range of 20 to 40 PSI for optimum performance of the thermal interface material (TIM) between the package and the heat sink. Thermocouples should not be present between the package and the heat sink, as their presence will degrade the thermal contact and result in incorrect thermal measurements.

Xilinx recommends using dynamic mounting around the four corners of the device package. On the PCB, use a bracket clip as part of the heat sink attachment to provide mechanical package support. See [Figure 5-5](#).



X15431-111115

Figure 5-5: Dynamic Mounting and Bracket Clips on Heat Sink Attachment

Heat Sink Removal Procedure

The heat spreader on the package provides mechanical protection for the die and serves as the primary heat dissipation path. It is attached with an epoxy adhesive to provide the necessary adhesion strength to hold the package together. For an application in which an external heat sink subjects the lid adhesion joint to continuous tension or shear, extra support might be required.

In addition, if the removal of an attached external heat sink subjects the joint to tension, torque, or shear, care should be exercised to ensure that the lid itself does not come off. In such cases, it has been found useful to use a small metal blade or metal wire to break the lid to heat sink joint from the corners and carefully pry the heat sink off. The initial cut should reach far enough so that the blade has leverage to exert upward pressure against the heat sink. Contact the heat sink and heat sink adhesive manufacturer for more specific recommendations on heat sink removal.

Soldering Guidelines

To implement and control the production of surface-mount assemblies, the dynamics of the solder reflow process and how each element of the process is related to the end result must be thoroughly understood.

Note: Xilinx recommends that customers qualify their custom PCB assembly processes using package samples.

The primary phases of the reflow process are:

1. Melting the particles in the solder paste
2. Wetting the surfaces to be joined
3. Solidifying the solder into a strong metallurgical bond

The peak reflow temperature of a plastic surface-mount component (PSMC) body should not be more than 250°C maximum (260°C for dry rework only) for Pb-free packages (220°C for eutectic packages), and is package size dependent. For multiple BGAs in a single board and because of surrounding component differences, Xilinx recommends checking all BGA sites for varying temperatures.

The infrared reflow (IR) process is strongly dependent on equipment and loading. Components might overheat due to lack of thermal constraints. Unbalanced loading can lead to significant temperature variation on the board. These guidelines are intended to assist users in avoiding damage to the components; the actual profile should be determined by those using these guidelines. For complete information on package moisture / reflow classification and package reflow conditions, refer to the Joint IPC/JEDEC Standard J-STD-020C.

Sn/Pb Reflow Soldering

Figure 5-6 shows typical conditions for solder reflow processing of Sn/Pb soldering using IR/convection. Both IR and convection furnaces are used for BGA assembly. The moisture sensitivity of PSMCs must be verified prior to surface-mount flow.

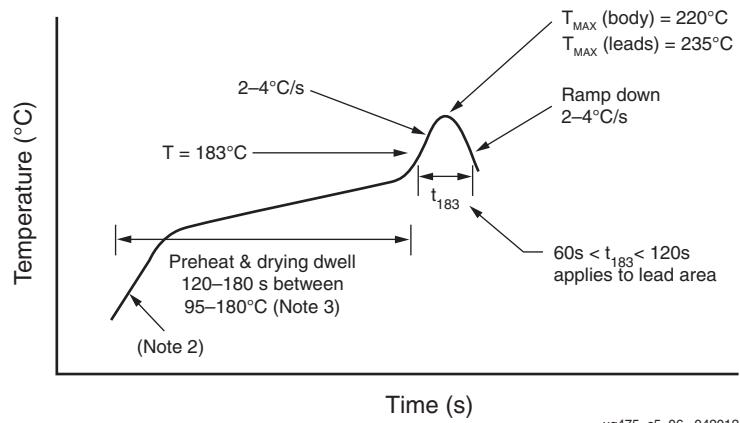


Figure 5-6: Typical Conditions for IR Reflow Soldering of Sn/Pb Solder

Notes for Figure 5-6:

1. Maximum temperature range = 220°C (body). Minimum temperature range before 205°C (leads/balls).

2. Preheat drying transition rate 2–4°C/s
3. Preheat dwell 95–180°C for 120–180 seconds
4. IR reflow must be performed on dry packages

Pb-Free Reflow Soldering

Xilinx uses SnAgCu solder balls for BGA packages. In addition, suitable material are qualified for the higher reflow temperatures (250°C maximum, 260°C for dry rework only) required by Pb-free soldering processes.

Xilinx does not recommend soldering SnAgCu BGA packages with SnPb solder paste using a Sn/Pb soldering process. Traditional Sn/Pb soldering processes have a peak reflow temperature of 220°C. At this temperature range, the SnAgCu BGA solder balls do not properly melt and wet to the soldering surfaces. As a result, reliability and assembly yields can be compromised.

The optimal profile must take into account the solder paste/flux used, the size of the board, the density of the components on the board, and the mix between large components and smaller, lighter components. Profiles should be established for all new board designs using thermocouples at multiple locations on the component. In addition, if there is a mixture of devices on the board, then the profile should be checked at various locations on the board. Ensure that the minimum reflow temperature is reached to reflow the larger components and at the same time, the temperature does not exceed the threshold temperature that might damage the smaller, heat sensitive components.

[Table 5-2](#) and [Figure 5-7](#) provide guidelines for profiling Pb-free solder reflow.

In general, a gradual, linear ramp into a spike has been shown by various sources to be the optimal reflow profile for Pb-free solders ([Figure 5-7](#)). SAC305 alloy reaches full liquidus temperature at 235°C. When profiling, identify the possible locations of the coldest solder joints and ensure that those solder joints reach a minimum peak temperature of 235°C for at least 10 seconds. It might not be necessary to ramp to peak temperatures of 260°C and above. Reflowing at high peak temperatures of 260°C and above can damage the heat sensitive components and cause the board to warp. Users should reference the latest IPC/JEDEC J-STD-020 standard for the allowable peak temperature on the component body. The allowable peak temperature on the component body is dependent on the size of the component. Refer to [Table 5-2](#) for peak package reflow body temperature information. In any case, use a reflow profile with the lowest peak temperature possible.

Table 5-2: Pb-Free Reflow Soldering Guidelines

Profile Feature	Convection, IR/Convection
Ramp-up rate	2°C/s maximum
Preheat temperature 150°–200°C	60–120 seconds
Temperature maintained above 217°C	60–150 seconds (60–90 seconds typical)
Time within 5°C of actual peak temperature	30 seconds maximum
Peak temperature (lead/ball)	235°C minimum, 245°C typical (depends on solder paste, board size, components mixture)
Peak temperature (body)	245°C–250°C, package body size dependent (reference Table 5-3)
Ramp-down rate	2°C/s maximum
Time 25°C to peak temperature	3.5 minutes minimum, 5.0 minutes typical, 8 minutes maximum

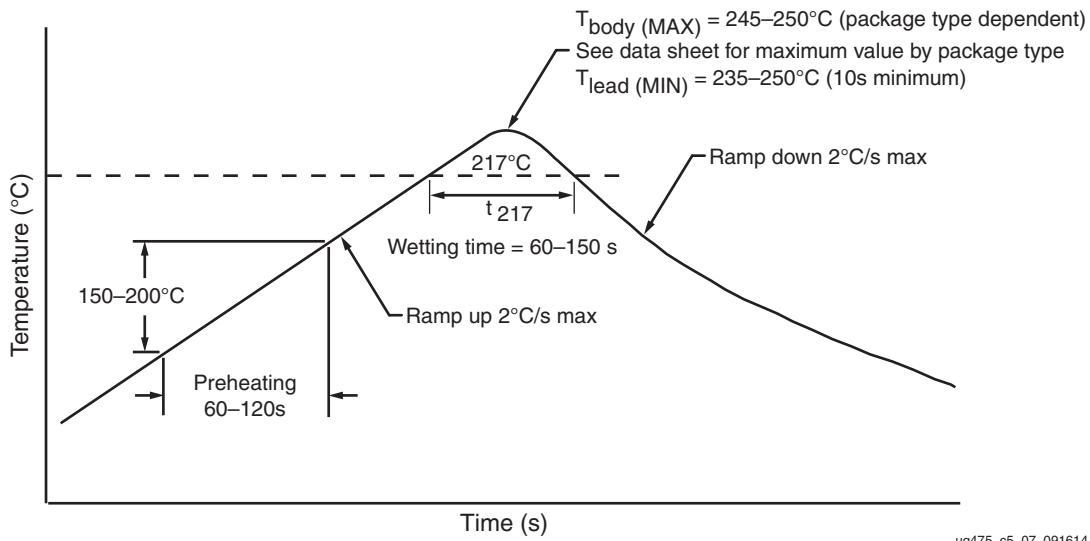


Figure 5-7: Typical Conditions for Pb-Free Reflow Soldering

**Table 5-3: Peak Package Reflow Body Temperature for Xilinx Pb-Free Packages
(Based on J-STD-020 Standard)**

Package	Peak Package Reflow Body Temperature	JEDEC Moisture Sensitivity Level (MSL)
BGA		
FLG1925 FLG1926 FLG1928 FLG1930 FHG1761	250°C	4
SBG484/SBV484 FBG484/FBV484 FBG676/FBV676 FBG900/FBV900 FFG676/FFV676 FFG900/FFV900 FFG901/FFV901 FFG1156/FFV1156 FFG1157/FFV1157 FFG1158/FFV1158 FFG1761/FFV1761 FFG1926 FFG1927/FFV1927 FFG1928 FFG1930	250°C	4
RF676 RF900 RF1157 RF1158 RF1761 RF1930	225°C	4
Wire Bond CSG324 FTG256 FGG484 FGG676	260°C	3

Notes:

- See specific 7 series device data sheets at [Xilinx Documentation](#).

For sophisticated boards with a substantial mix of large and small components, it is critical to minimize the ΔT across the board ($<10^{\circ}\text{C}$) to minimize board warpage and thus, attain higher assembly yields. Minimizing the ΔT is accomplished by using a slower rate in the warm-up and preheating stages. Xilinx recommends a heating rate of less than $1^{\circ}\text{C}/\text{s}$ during the preheating and soaking stages, in combination with a heating rate of not more than $2^{\circ}\text{C}/\text{s}$ throughout the rest of the profile.

It is also important to minimize the temperature gradient on the component, between top surface and bottom side, especially during the cooling down phase. The key is to optimize cooling while maintaining a minimal temperature differential between the top surface of the package and the solder joint area. The temperature differential between the top surface of the component and the solder balls should be maintained at less than 7°C during the critical region of the cooling phase of the reflow process. This critical region is in the part of the cooling phase where the balls are not completely solidified to the board yet, usually between the 200°C – 217°C range. To efficiently cool the parts, divide the cooling section into multiple zones, with each zone operating at different temperatures.

Post Reflow/Cleaning/Washing

Many PCB assembly subcontractors use a no-clean process in which no post-assembly washing is required. Although a no-clean process is recommended, if cleaning is required, Xilinx recommends a water-soluble paste and a washer using a deionized-water. Baking after the water wash is recommended to prevent fluid accumulation.

Cleaning solutions or solvents are not recommended because some solutions contain chemicals that can compromise the lid adhesive, thermal compound, or components inside the package.

Conformal Coating

Xilinx has no information about the reliability of flip-chip BGA packages on a board after exposure to conformal coating. Any process using conformal coating should be qualified for the specific use case to cover the materials and process steps.

Note: Xilinx does not recommend using Toluene-based conformal coatings because they can weaken the lid adhesive used in Xilinx packages.

References

The following websites contain additional information on heat management and contact information.

- Wakefield: www.wakefield-vette.com
- Aavid: www.aavidthermally.com
- Advanced Thermal Solutions: www.qats.com
- CTS: www.ctscorp.com
- Radian Thermal Products: www.radianheatsinks.com
- Thermo Cool: www.thermocoolcorp.com

Refer to the following websites for interface material sources:

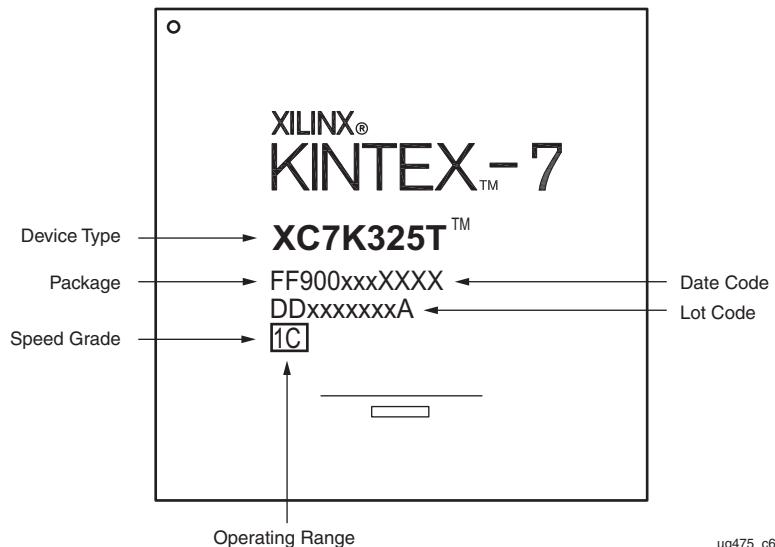
- Henkel: www.henkel.com
- Bergquist Company: www.bergquistcompany.com
- AOS Thermal Compound: www-aosco.com
- Chomerics: www.chomerics.com
- Kester: www.kestercorp.com

Refer to the following websites for CFD tools Xilinx supports with thermal models.

- Mentor: Flotherm: <http://www.mentor.com/products/mechanical/flotherm>
- ANSYS Icepak: www.ansys.com

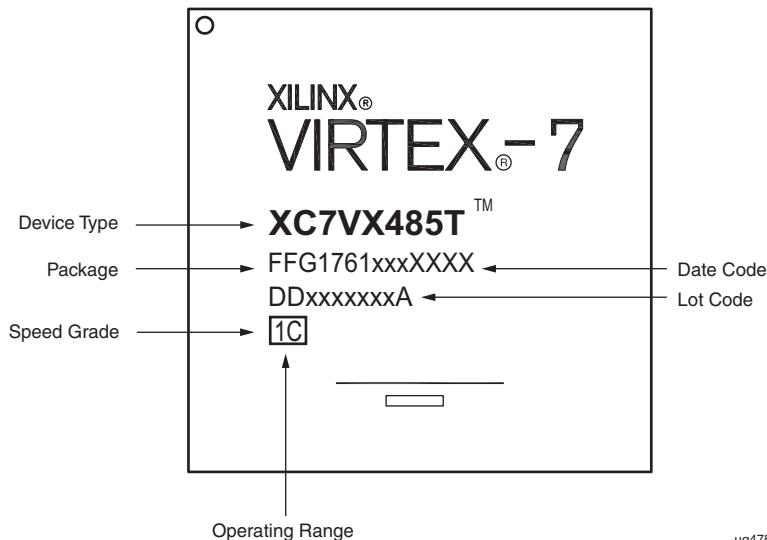
Package Marking

All 7 series devices have package top-markings similar to the examples shown in [Figure 6-1](#), [Figure 6-2](#), and [Figure 6-3](#). The markings are explained in [Table 6-1](#).



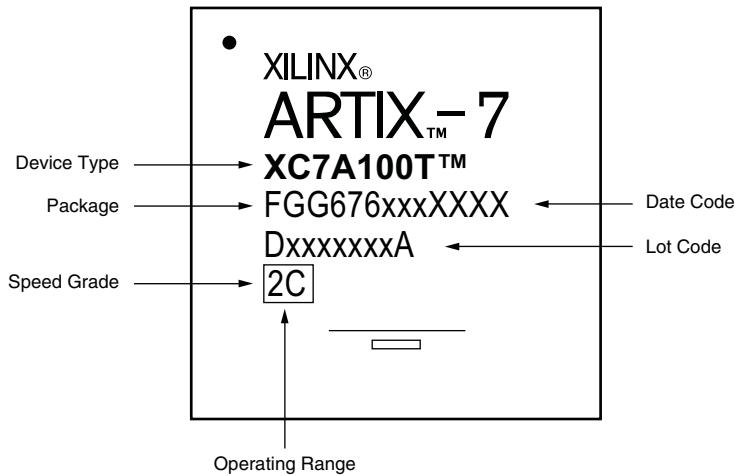
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Figure 6-1: Kintex-7 Device Package Marking



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Figure 6-2: Virtex-7 Device Package Marking



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Figure 6-3: Artix-7 Device Package Marking

Table 6-1: Xilinx Device Marking Definition—Example

Item	Definition
Xilinx Logo	Xilinx logo, Xilinx name with trademark, and trademark-registered status.
Family Brand Logo	Device family name with trademark and trademark-registered status. This line is optional and could appear blank.
1st Line	Device type.
2nd Line	Package code, circuit design revision, the location code for the wafer fab, the geometry code, and date code. A G (or V) in the third letter of a package code indicates a Pb-free RoHS compliant package. For more details on Xilinx Pb-Free and RoHS Compliant Products, see: http://www.xilinx.com/pbfree .

Table 6-1: Xilinx Device Marking Definition—Example (Cont'd)

Item	Definition	
3rd Line	Ten alphanumeric characters for Assembly, Lot, and Step information. The last digit is usually an <i>A</i> or an <i>M</i> if a stepping version does not exist.	
4th Line	<p>Device speed grade and temperature range. When not marked on the package, the product is considered to operate at the commercial (C) temperature range. For more information on the ordering codes, see DS180: 7 Series FPGAs Overview.</p> <p>Other variations for the 4th line:</p>	
	L2E	The L2E indicates a -2LE device. The -2LE speed grade offers reduced maximum power consumption. Artix-7 and Kintex-7 FPGAs are capable of operating at lower core voltage. The E is for the extended temperature operating range. For more information, see the specific device data sheets at: 7 series FPGAs .
	1C xxxx	The xxxx indicates the SCD for the device. An SCD is a special ordering code that is not always marked in the device top mark.
	1C ES	The addition of an ES indicates an Engineering Sample.

Packing and Shipping

Introduction

The 7 series devices are packed in trays (Table 7-1). Trays are used to pack most of Xilinx surface-mount devices since they provide excellent protection from mechanical damage. In addition, they are manufactured using antistatic material to provide limited protection against ESD damage and can withstand a bake temperature of 125°C. The maximum operating temperature is 140°C.

Table 7-1: Standard Device Counts per Tray and Box

Package	Maximum Number of Devices Per Tray	Maximum Number of Units In One Internal Box
CP/CPG236	240	1200
FT/FTG256	90	450
CS/CSG324	126	630
CS/CSG325		
SB/SBG/SBV484	84	420
RS484		
FG/FGG484	60	300
FB/FBG/FBV484		
RB484		
FG/FGG676	40	200
FB/FBG/FBV676		
FF/FFG/FFV676		
RB676		
RF676		
FB/FBG/FBV900	27	135
FF/FFG/FFV900		
FF/FFG/FFV901		
RF900		

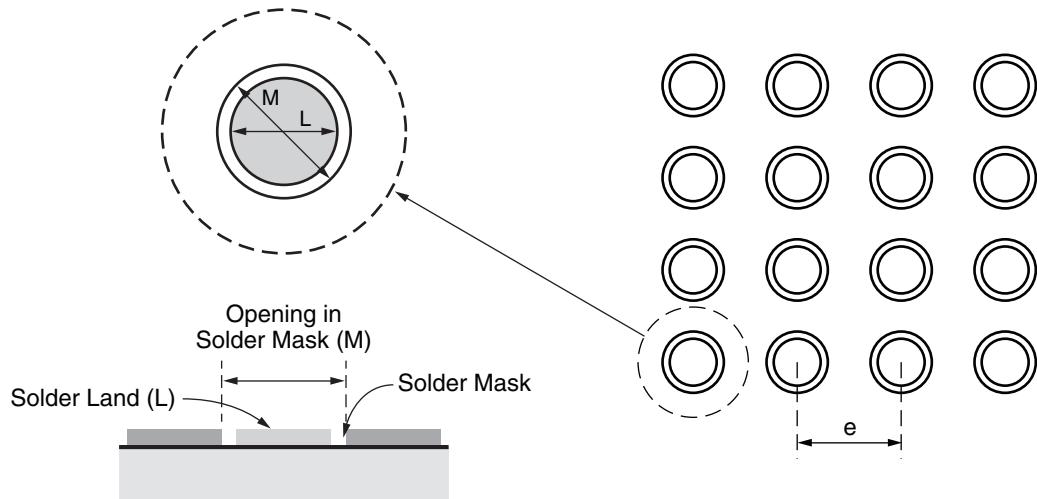
Table 7-1: Standard Device Counts per Tray and Box (Cont'd)

Package	Maximum Number of Devices Per Tray	Maximum Number of Units In One Internal Box
FF/FFG/FFV1156	24	120
FF/FFG/FFV1157		
RF1157		
FF/FFG/FFV1158		
RF1158		
FF/FFG/FFV1761	12	60
RF1761		
FHG1761	12	36
FL/FLG1925	12	36
FF/FFG1926		
FL/FLG1926		
FF/FFG/FFV1927		
FF/FFG1928		
FL/FLG1928		
FF/FFG1930	12	36
FL/FLG1930		
RF1930		

Recommended PCB Design Rules for BGA Packages

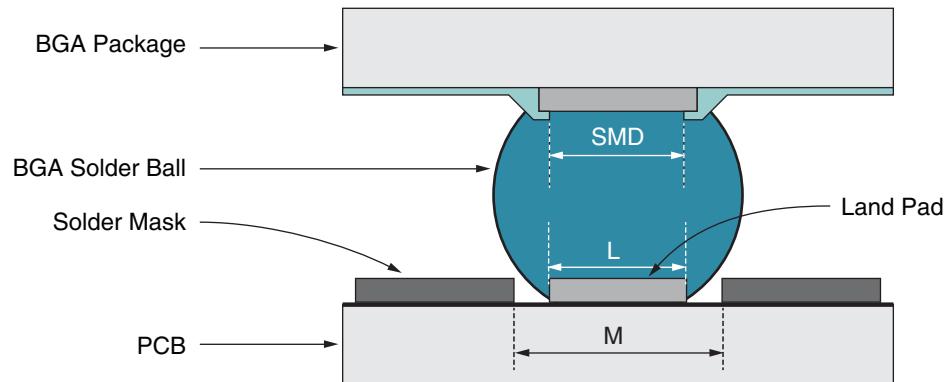
Xilinx provides the diameter of a land pad on the package side. This information is required prior to the start of the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are described in [Figure A-1](#) and summarized in [Table A-1](#) for both 0.8 mm and 1.0 mm pitch packages. For Xilinx BGA packages, non-solder mask defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in [Figure A-1](#). An example of an NSMD PCB pad solder joint is shown in [Figure A-2](#). It is recommended to have the board land pad diameter with a 1:1 ratio to the package solder mask defined (SMD) pad for improved board level reliability.

The space between the NSMD pad and the solder mask as well as the actual signal trace widths and via dimensions depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.



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Figure A-1: Suggested Board Layout of Soldered Pads for BGA Packages



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Figure A-2: Example of an NSMD PCB Pad Solder Joint

Table A-1: BGA Package Design Rules

Packages	0.5 mm Pitch	0.8 mm Pitch	1.0 mm Pitch		
	CPG236	SB/SBG/SBV, CS/CSG	FF/FFG/FFV, FB/FBG/FBV, FH/FHG, FL/FLG, RF/RB/RS	FG/FGG	FT/FTG
Design Rule	Dimensions in mm (mils)				
Package land pad opening (SMD)	0.275 mm (10.8 mils)	0.40 mm (15.7 mils)	0.53 mm (20.9 mils)	0.50 mm (19.7 mils)	0.40 mm (15.7 mils)
Maximum PCB solder land (L) diameter	0.275 mm (10.8 mils)	0.40 mm (15.7 mils)	0.53 mm (20.9 mils)	0.50 mm (19.7 mils)	0.40 mm (15.7 mils)
Opening in PCB solder mask (M) diameter	0.375 mm (14.76 mils)	0.50 mm (19.7 mils)	0.63 mm (24.8 mils)	0.60 mm (23.6 mils)	0.50 mm (19.7 mils)
Solder ball land pitch (e)	0.50 mm (19.7 mils)	0.80 mm (31.5 mils)	1.00 mm (39.4 mils)	1.00 mm (39.4 mils)	1.00 mm (39.4 mils)

Notes:

1. Controlling dimension in mm.

Heat Sink Guidelines for Lidless Flip-Chip Packages

Heat Sink Attachments for Lidless Flip-chip BGA (FB/FBG/FBV)

Heat sinks can be attached to the package in multiple ways. For heat to dissipate effectively, the advantages and disadvantages of each heat sink attachment method must be considered. Factors influencing the selection of the heat sink attachment method include the package type, contact area of the heat source, and the heat sink type.

Silicon and Decoupling Capacitors Height Consideration

When designing heat sink attachments for lidless flip-chip BGA packages, the height of the die above the substrate and also the height of decoupling capacitors must be considered (Figure B-1). This is to prevent electrical shorting between the heat sink (metal) and the decoupling capacitors.

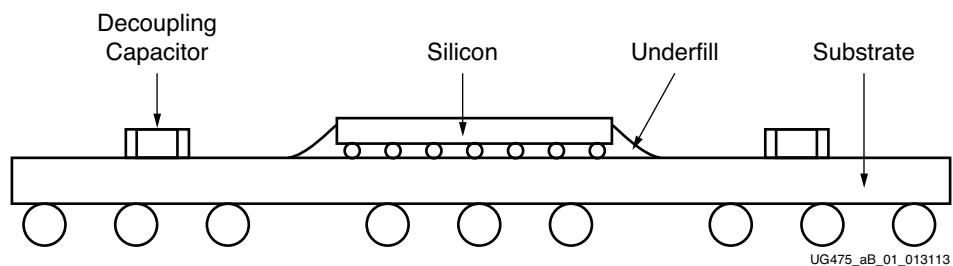


Figure B-1: Cross Section of Lidless Flip-chip BGA

Types of Heat Sink Attachments

There are six main methods for heat sink attachment. Table B-1 lists their advantages and disadvantages.

- Thermal tape
- Thermally conductive adhesive or glue (epoxy)
- Wire form Z-clips
- Plastic clip-ons
- Threaded stand-offs (PEMs) and compression springs
- Push-pins and compression springs

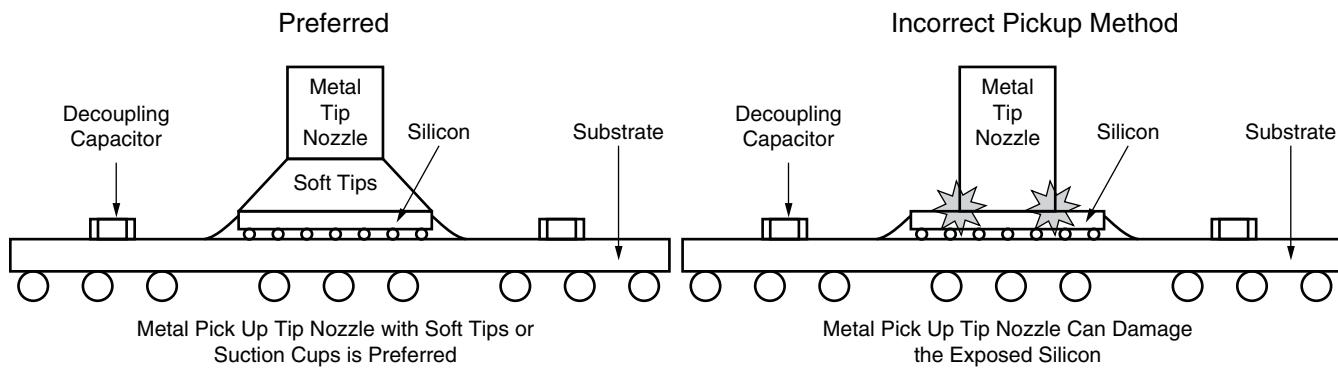
Table B-1: Heat Sink Attachment Methods

Attachment Method	Advantages	Disadvantages
Thermal tape	<ul style="list-style-type: none"> Generally easy to attach and is inexpensive. Lowest cost approach for aluminum heat sink attachment. No additional space required on the PCB. 	<ul style="list-style-type: none"> The surfaces of the heat sink and the chip must be very clean to allow the tape to bond correctly. Because of the small contact area, the tape might not provide sufficient bond strength. Tape is a moderate to low thermal conductor that could affect the thermal performance.
Thermally conductive adhesive or glue	<ul style="list-style-type: none"> Outstanding mechanical adhesion. Fairly inexpensive, costs a little more than tape. No additional space required on the PCB. 	<ul style="list-style-type: none"> Adhesive application process is challenging and it is difficult to control the amount of adhesive to use. Difficult to rework. Because of the small contact area, the adhesive might not provide sufficient bond strength.
Wire form Z-clips	<ul style="list-style-type: none"> It provides a strong and secure mechanical attachment. In environments that require shock and vibration testing, this type of strong mechanical attachment is necessary. Easy to apply and remove. Does not cause the semiconductors to be destroyed (epoxy and occasionally tape can destroy the device). It applies a preload onto the thermal interface material (TIM). Pre-loads actually improve thermal performance. 	<ul style="list-style-type: none"> Requires additional space on the PCB for anchor locations.
Plastic clip-ons	<ul style="list-style-type: none"> Suitable for designs where space on the PCB is limited. Easy to rework by allowing heat sinks to be easily removed and reapplied without damaging the PCB board. Can provide a strong enough mechanical attachment to pass shock and vibration test. 	<ul style="list-style-type: none"> Needs a keep out area around the silicon devices to use the clip. Caution is required when installing or removing clip-ons because localized stress can damage the solder balls or chip substrate.
Threaded stand-offs (PEMs) and compression springs	<ul style="list-style-type: none"> Provides stable attachments to heat source and transfers load to the PCB, backing plate, or chassis. Suitable for high mass heat sinks. Allows for tight control over mounting force and load placed on chip and solder balls. 	<ul style="list-style-type: none"> Holes are required in the PCB taking valuable space that can be used for trace lines. Tends to be expensive, especially since holes need to be drilled or predrilled onto the PCB board to use stand-offs.
Push-pins and compression springs	<ul style="list-style-type: none"> Provides a stable attachment to a heat source and transfers load to the PCB. Allows for tight control over mounting force and load placed on chip and solder balls. 	<ul style="list-style-type: none"> Requires additional space on the PCB for push-pin locations.

Heat Sink Attachment

Component Pick-up Tool Consideration

For pick-and-place machines to place lidless flip-chip BGAs onto PCBs, Xilinx recommends using soft tips or suction cups for the nozzles. This prevents chipping, scratching, or even cracking of the bare die (Figure B-2).



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Figure B-2: Recommended Method For Using Pick-up Tools

Heat Sink Attachment Process Considerations

After the component is placed onto the PCBs, when attaching a heat sink to the lidless package, the factors in Table B-2 must be carefully considered (see Figure B-3).

Table B-2: Heat Sink Attachment Considerations

Consideration(s)	Effect(s)	Recommendation(s)
In heat sink attach process, what factors can cause damage to the expose die and passive capacitors?	<ul style="list-style-type: none"> • Uneven heat sink placement • Uneven TIM thickness • Uneven force applied when placing heat sink placement 	<ul style="list-style-type: none"> • Even heat sink placement • Even TIM thickness • Even force applied when placing heat sink placement
Does the heat sink tilt or tip the post attachment?	Uneven heat sink placement will damage the silicon and can cause field failures.	<ul style="list-style-type: none"> • Careful handling not to contact the heat sink with the post attachment. • Use a fixture to hold the heat sink in place with post attachment until it is glued to the silicon.

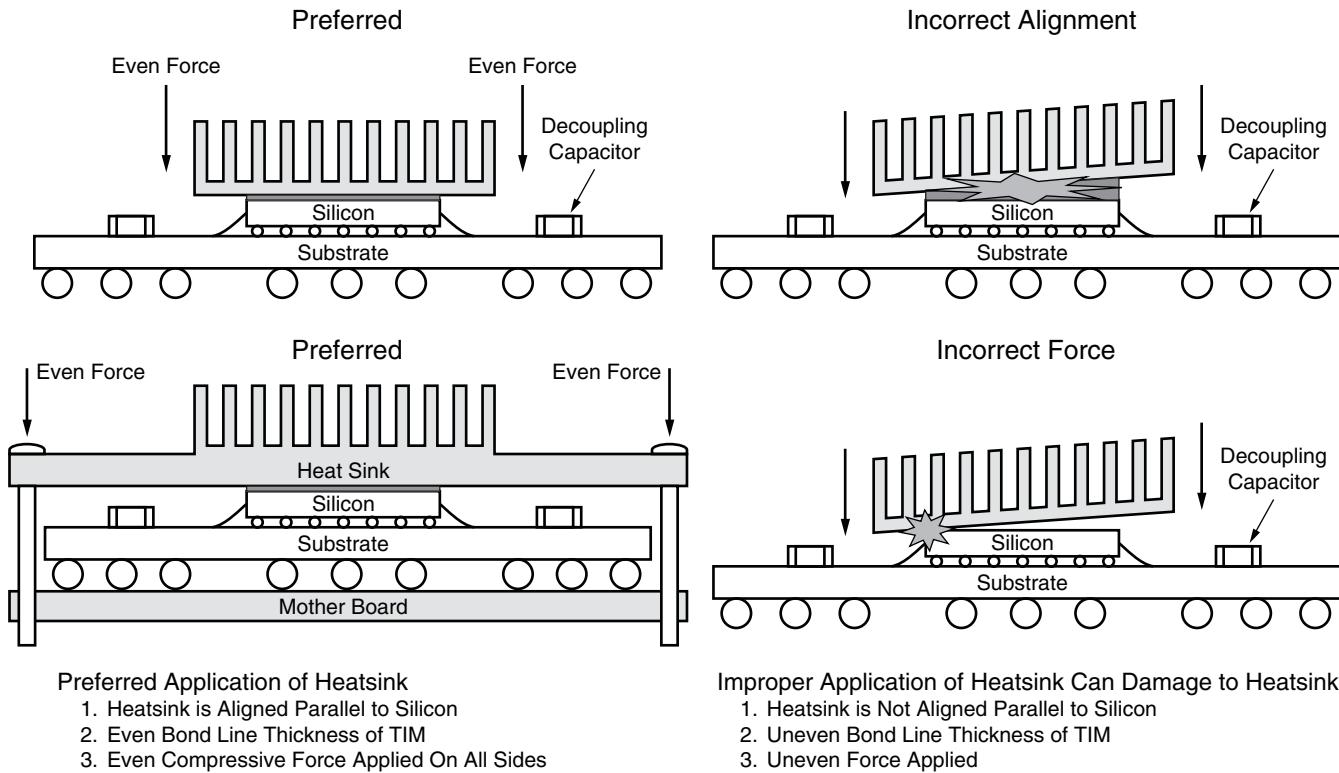


Figure B-3: Recommended Application of Heat Sink

Standard Heat Sink Attach Process with Thermal Conductive Adhesive

Prior to attaching the heat sink, the FPGA needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.
2. Thermoset material (electrically non-conductive) is applied over the backside surface of silicon in a pattern using automated dispensing equipment. Automated dispensers are often used to provide a stable process speed at a relatively low cost. The optimum dispensing pattern needs to be determined by the SMT supplier.

Note: Minimal volume coverage of the backside of the silicon can result in non-optimum heat transfer.

3. The heat sink is placed on the backside of the silicon with a pick and place machine. A uniform pressure is applied over the heat sink to the backside of the silicon. As the heat sink is placed, the adhesive spreads to cover the backside silicon. A force transducer is normally used to measure and limit the placement force.
4. The epoxy is cured with heat at a defined time.

Note: The epoxy curing temperature and time is based on manufacturer's specifications.

Standard Heat Sink Attach Process with Thermal Adhesive Tape

Prior to attaching the heat sink, the FPGA needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.
2. Thermal adhesive tape cut to the size of the heat sink is applied on the underside of the heat sink at a modest angle with the use of a squeegee rubber roller. Apply pressure to help reduce the possibility of air entrapment under the tape during application.
3. The heat sink is placed on the backside of the silicon with a pick and place machine. A uniform pressure is applied over the heat sink to the backside of the silicon. As the heat sink is placed, the thermal adhesive tape is glued to the backside of the silicon. A force transducer is normally used to measure and limit the placement force.
4. A uniform and constant pressure is applied uniformly over the heat sink and held for a defined time.

Note: The thermal adhesive tape hold time is based on manufacturer's specifications.

Push-Pin and Shoulder Screw Heat Sink Attachment Process with Phase Change Material (PCM) Application

Prior to attaching the heat sink, the FPGA needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.
- Note:** The jig or fixture needs to account for the push pin depth of the heat sink.
2. PCM tape, cut to the size of the heat sink, is applied on the underside of the heat sink at a modest angle with the use of a squeegee rubber roller. Apply pressure to help reduce the possibility of air entrapment under the tape during application.
 3. Using the push-pin tool, heat sinks are applied over the packages ensuring a pin locking action with the PCB holes. The compression load from springs applies the appropriate mounting pressure required for proper thermal interface material performance.

Note: Heat sinks must not tilt during installation. This process cannot be automated due to the mechanical locking action which requires manual handling. The PCB drill hole tolerances need to be close enough to eliminate any issues concerning the heat sink attachment.

