Lab Report-8

Entry counter system using Up-Down Counter

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Contents

1 Objective

To design and implement a digital up/down counter that displays the number of people currently in the mess during peak lunch hours.

2 Components Required

- 7-Segment Display (2-digit, Common Anode are used)
- Push Buttons (for simulation purposes if sensors are unavailable)
- Power Supply (5V DC for microcontroller and display)
- Breadboards and Jumper Wires
- Resistors ($1\,\mathrm{k}\Omega, 100\,\Omega$ for display connections)
- 2x 7447 Decoder
- 4x IC 7476(8-JK Flip Flops)
- IC 7432 for OR Gate (as required)
- IC 7408 for AND Gate (as required)
- IC 7404 for inverting gate (as required)
- IC 7486 for XOR gate (combining with not for XNOR)
- IC 7411 for 3-input AND gate (as required)
- IC 7421 for 4-input AND gate (as required)
- IC 7420 for 4-input NAND gate (as required)

3 Circuit network Connections

3.1 Sketch of the Core-counting circuit

This consists of Incrementing/Decrementing circuit, clock-pulse generating circuit, and sub-circuit consisting of T-flipflops which compute binary output of counter.

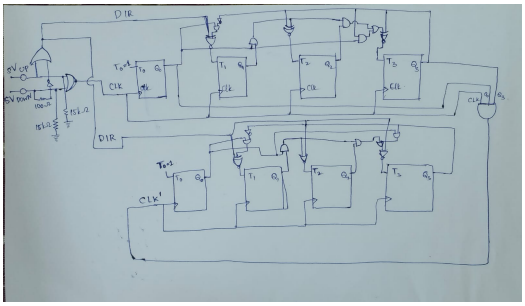


Figure 1: Binary Core-counting circuit

3.2 Incrementing/Decrementing circuit and clock-pulse generating circuit

To navigate the incrementation or decrementation in count, the following circuit is built.

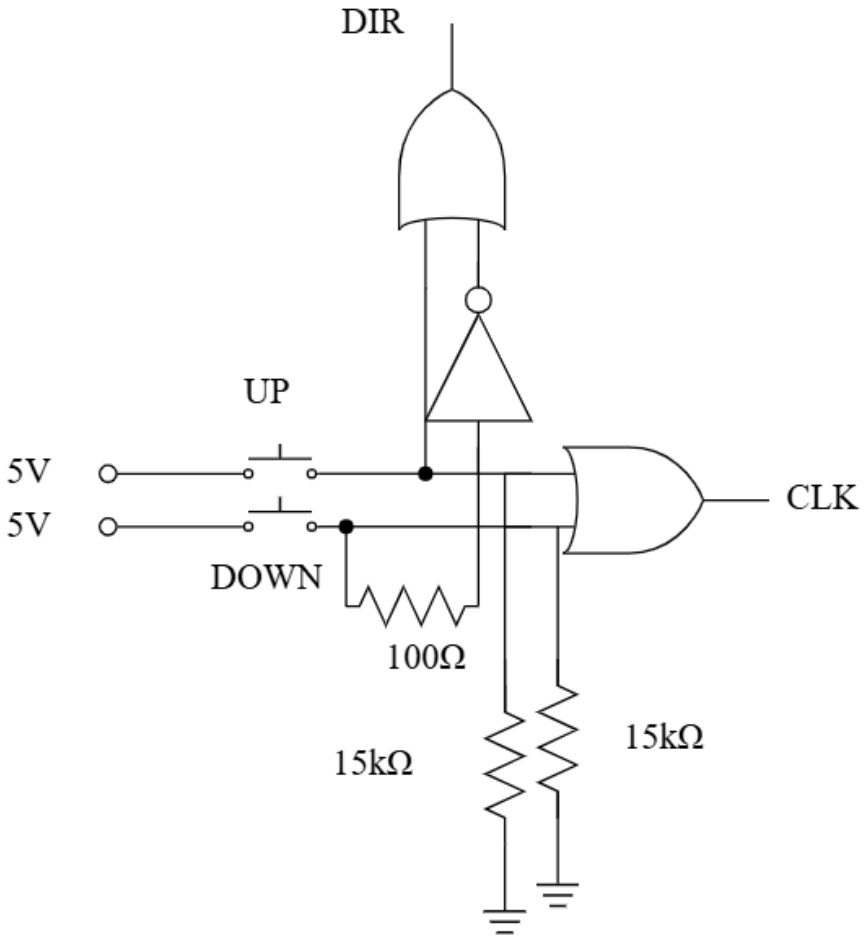


Figure 2: clock-pulse generation circuit

3.3 JK flip-flop connections for units digit

3.3.1 1st IC 7476(for bits Q_0 and Q_1)

Pin	Description
1	Clock for 1st flip-flop
2	$\overline{\text{PRESET}} = 1$ (For 1st flip-flop)
3	$\overline{\text{CLEAR}} = 1$ (For 1st flip-flop)
4	$J_0 = 1$ (should be connected to 5V)
5	Vcc = 5V
6	Clock for 2nd flip-flop
7	$\overline{\text{PRESET}} = 1$ (For 2nd flip-flop)
8	$\overline{\text{CLEAR}} = 1$ (For 2nd flip-flop)
9	$J_1 = Q_0.\overline{Q_3}.DIR + \overline{Q_0.\overline{Q_3}}.\overline{DIR}$
10	$\overline{Q_1}$
11	Q_1
12	$K_1 = Q_0.\overline{Q_3}.DIR + \overline{Q_0.\overline{Q_3}}.\overline{DIR}$
13	Ground (0V)
14	$\overline{Q_0}$
15	Q_0
16	$K_0 = 1$ (should be connected to 5V)

Table 1: Pin Configuration Table

3.3.2 2nd IC 7476(for bits Q_2 and Q_3)

Pin	Description
1	Clock for 3rd flip-flop
2	$\overline{\text{PRESET}} = 1$ (For 3rd flip-flop)
3	$\overline{\text{CLEAR}} = 1$ (For 3rd flip-flop)
4	$J_2 = Q_0.Q_1.DIR + \overline{Q_0.Q_1}.\overline{DIR}$
5	Vcc = 5V
6	Clock for 4th flip-flop
7	$\overline{\text{PRESET}} = 1$ (For 4th flip-flop)
8	$\overline{\text{CLEAR}} = 1$ (For 4th flip-flop)
9	$J_3 = (Q_0.Q_1.Q_2 + Q_0.Q_3).DIR + \overline{(Q_0.Q_1.Q_2 + Q_0.Q_3)}.\overline{DIR}$
10	$\overline{Q_1}$
11	Q_3
12	$K_3 = (Q_0.Q_1.Q_2 + Q_0.Q_3).DIR + \overline{(Q_0.Q_1.Q_2 + Q_0.Q_3)}.\overline{DIR}$
13	Ground (0V)
14	$\overline{Q_2}$
15	Q_2
16	$K_2 = Q_0.Q_1.DIR + \overline{Q_0.Q_1}.\overline{DIR}$

Table 2: Pin Configuration Table

3.4 JK flip-flop connections for tens digit

3.4.1 1st IC 7476(for bits Q_0 and Q_1)

Pin	Description
1	Clock for 1st flip-flop (From $Q_0.Q_3.CLK$)
2	$\overline{\text{PRESET}} = 1$ (For 1st flip-flop)
3	$\overline{\text{CLEAR}} = 1$ (For 1st flip-flop)
4	$J_0 = 1$ (should be connected to 5V)
5	Vcc = 5V
6	Clock for 2nd flip-flop (From $Q_0.Q_3.CLK$)
7	$\overline{\text{PRESET}} = 1$ (For 2nd flip-flop)
8	$\overline{\text{CLEAR}} = 1$ (For 2nd flip-flop)
9	$J_1 = Q_0.\overline{Q_3}.DIR + \overline{Q_0.\overline{Q_3}}.\overline{DIR}$
10	$\overline{Q_1}$
11	Q_1
12	$K_1 = Q_0.\overline{Q_3}.DIR + \overline{Q_0.\overline{Q_3}}.\overline{DIR}$
13	Ground (0V)
14	$\overline{Q_0}$
15	Q_0
16	$K_0 = 1$ (should be connected to 5V)

Table 3: Pin Configuration Table

3.4.2 2nd IC 7476(for bits Q_2 and Q_3)

Pin	Description
1	Clock for 3rd flip-flop (From $Q_0.Q_3.CLK$)
2	$\overline{\text{PRESET}} = 1$ (For 3rd flip-flop)
3	$\overline{\text{CLEAR}} = 1$ (For 3rd flip-flop)
4	$J_2 = Q_0.Q_1.DIR + \overline{Q_0.Q_1}.\overline{DIR}$
5	Vcc = 5V
6	Clock for 4th flip-flop (From $Q_0.Q_3.CLK$)
7	$\overline{\text{PRESET}} = 1$ (For 4th flip-flop)
8	$\overline{\text{CLEAR}} = 1$ (For 4th flip-flop)
9	$J_3 = (Q_0.Q_1.Q_2 + Q_0.Q_3).DIR + \overline{(Q_0.Q_1.Q_2 + Q_0.Q_3)}.\overline{DIR}$
10	$\overline{Q_1}$
11	Q_3
12	$K_3 = (Q_0.Q_1.Q_2 + Q_0.Q_3).DIR + \overline{(Q_0.Q_1.Q_2 + Q_0.Q_3)}.\overline{DIR}$
13	Ground (0V)
14	$\overline{Q_2}$
15	Q_2
16	$K_2 = Q_0.Q_1.DIR + \overline{Q_0.Q_1}.\overline{DIR}$

Table 4: Pin Configuration Table

3.5 Flip Flops to Decoder

Output bit	7447 Pin
Q_0	A
Q_1	B
Q_2	C
Q_3	D

Table 5: Connections from output bits (IC 7476) to 7447 Decoder

- **The output bits Q_0 to Q_3 represent the BCD of a number.**

- **To represet the BCD equivalent of a number on Seven-Segment display, decoder is used.**
- **We use 2 decoders in the entire circuit (one for a digit) to convert BCD to seven segment display.**

3.6 Decoder to seven-segment display

7447 Pin	**Seven-Segment Display Segment**
$\overline{a}$	a
$\overline{b}$	b
$\overline{c}$	c
$\overline{d}$	d
$\overline{e}$	e
$\overline{f}$	f
$\overline{g}$	g

Table 6: Connections from 7447 Decoder to Seven-Segment Display

4 Logic

4.1 Excitation Table for JK Flip-Flop

Q_n	Q_{n+1}	**J**	**K**
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Table 7: Excitation Table for JK Flip-Flop

Table 8: Excitation Table for T Flip-Flop

Present State (Q_n)	**Next State (Q_{n+1})**	**T Input**
0	0	0
0	1	1
1	0	1
1	1	0

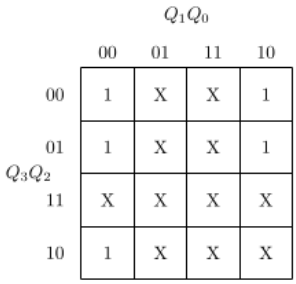
4.2 Excitation Table for T Flip-Flop

4.3 Truth Table for incrementing logic

Q3	**Q2**	**Q1**	**Q0**	**J3**	**K3**	**J2**	**K2**	**J1**	**K1**	**J0**	**K0**	**NS3**	**NS2**	**NS1**	**NS0**
0	0	0	0	0	X	0	X	0	X	1	X	0	0	0	1
0	0	0	1	0	X	0	X	1	X	X	1	0	0	1	0
0	0	1	0	0	X	0	X	X	0	1	X	0	0	1	1
0	0	1	1	0	X	1	X	X	1	X	1	0	1	0	0
0	1	0	0	0	X	X	0	0	X	1	X	0	1	0	1
0	1	0	1	0	X	X	0	1	X	X	1	0	1	1	0
0	1	1	0	0	X	X	0	X	0	1	X	0	1	1	1
0	1	1	1	1	X	X	1	X	1	X	1	1	0	0	0
1	0	0	0	X	0	0	X	0	X	1	X	1	0	0	1
1	0	0	1	X	1	0	X	0	X	X	1	0	0	0	0
1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X

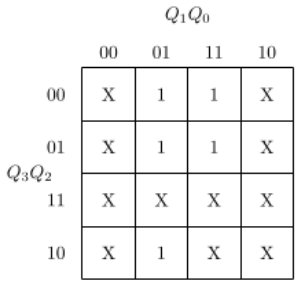
Table 9: Truth Table for Incrementation

4.4 K-maps for J and K of each flip-flop(Incrementation)



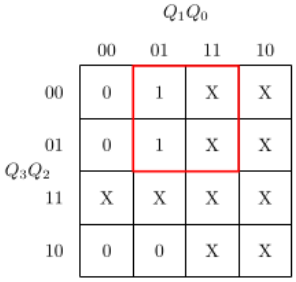
Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	X	X	X	X
10	1	X	X	X

(a) $J_0 = 1$



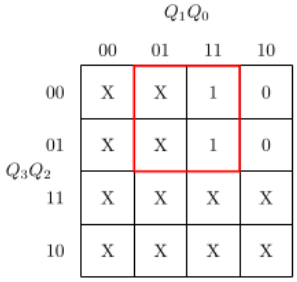
Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	X	X	X
10	X	1	X	X

(b) $K_0 = 1$



Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	1	X	X
01	0	1	X	X
11	X	X	X	X
10	0	0	X	X

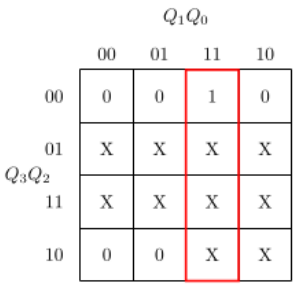
(c) $J_1 = Q_0.\overline{Q_3}$



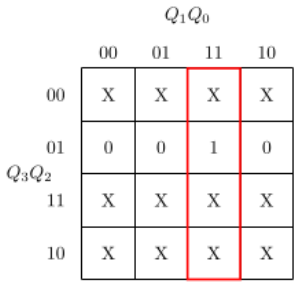
Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	X	1	0
01	X	X	1	0
11	X	X	X	X
10	X	X	X	X

(d) $K_1 = Q_0.\overline{Q_3}$

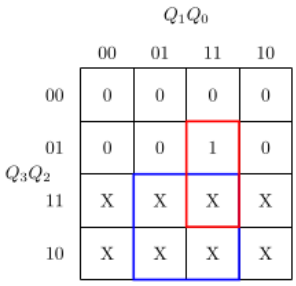
Figure 3: JK values of 1st IC7476



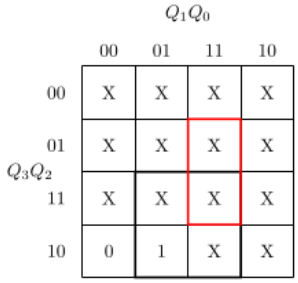
(a) $J_2 = Q_0.Q_1$



(b) $K_2 = Q_0.Q_1$



(c) $J_3 = (Q_0.Q_1.Q_2) + (Q_0.Q_3)$



(d) $K_3 = (Q_0.Q_1.Q_2) + (Q_0.Q_3)$

Figure 4: JK values of 2nd IC7476

4.5 Truth table for Decrementing Logic

Q3	Q2	Q1	Q0	J3	K3	J2	K2	J1	K1	J0	K0	NS3	NS2	NS1	NS0
1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X
1	0	0	1	X	0	0	X	0	X	X	1	1	0	0	0
1	0	0	0	X	1	1	X	1	X	1	X	0	1	1	1
0	1	1	1	0	X	X	0	X	0	X	1	0	1	1	0
0	1	1	0	0	X	X	0	X	1	1	X	0	1	0	1
0	1	0	1	0	X	X	0	0	X	X	1	0	1	0	0
0	1	0	0	0	X	X	1	1	X	1	X	0	0	1	1
0	0	1	1	0	X	0	X	X	0	X	1	0	0	1	0
0	0	1	0	0	X	0	X	X	1	1	X	0	0	0	1
0	0	0	1	0	X	0	X	0	X	X	1	0	0	0	0
0	0	0	0	1	X	0	X	0	X	1	X	1	0	0	1

Table 10: Truth Table for Decrementation

4.6 K-maps for J and K of each flipflop(Decrementation)

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	X	X	X	X
10	1	X	X	X

(a) $J_0 = 1$

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	X	X	X
10	X	1	X	X

(b) $K_0 = 1$

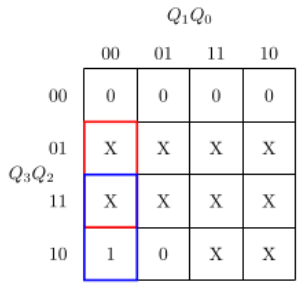
Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	X	X
01	1	0	X	X
11	X	X	X	X
10	1	0	X	X

(c) $J_1 = \overline{Q_0}Q_1 + \overline{Q_0Q_1}(Q_2 + Q_3)$

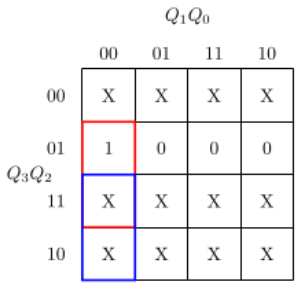
Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	X	0	1
01	X	X	0	1
11	X	X	X	X
10	X	X	X	X

(d) $K_1 = \overline{Q_0}Q_1 + \overline{Q_0Q_1}(Q_2 + Q_3)$

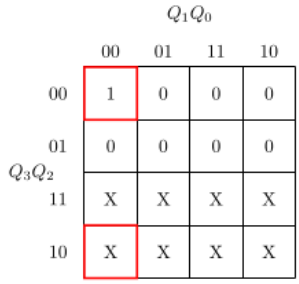
Figure 5: JK values of 3rd IC7476



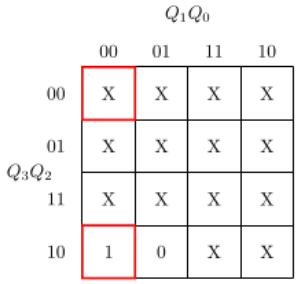
(a) $J_2 = \overline{Q_0Q_1}(Q_3 + Q_2)$



(b) $K_2 = \overline{Q_0Q_1}(Q_3 + Q_2)$



(c) $J_3 = \overline{Q_0Q_1Q_2}$



(d) $K_3 = \overline{Q_0Q_1Q_2}$

Figure 6: JK values of 4th IC7476

5 Working Principle of circuit

5.0.1 Working of DIR

The `DIR` signal acts as a control input to decide the counting direction:

- **DIR = 1 (High)**: The counter increments.
- **DIR = 0 (Low)**: The counter decrements.

5.1 Implementation with Push Buttons

Push buttons play a crucial role in manually controlling the `DIR` signal. The common configurations are:

5.1.1 Two-Button Configuration

Two push buttons can be used:

- **Increment Button (UP)**: When pressed, it sets `DIR` = 1 and triggers a clock pulse. Pressing the UP button generates a pulse that signifies an increment.
- `DIR`=1, The output function is the boolean logic associated with `DIR`, results in enabling $J_1 = K_1 = Q_0.\overline{Q_3}$, and similar will happen for $J_2 = K_2$ and $J_3 = K_3$.
- **Decrement Button (DOWN)**: When pressed, it sets `DIR` = 0 and triggers a clock pulse. Pressing the DOWN button generates a pulse that signifies a decrement.
- `DIR`=0, The the output function is the boolean logic associated with `DIR`, results in enabling $J_1 = K_1 = \overline{Q_0}Q_1 + \overline{Q_0}\overline{Q_1}(Q_2 + Q_3)$, and similar will happen for $J_2 = K_2$ and $J_3 = K_3$.

5.1.2 Single-Button Toggle Configuration

A single push button can toggle the `DIR` state:

- Pressing the button flips `DIR` from 0 to 1 (increment mode) and vice versa.
- A debounce circuit or software debouncing had been setup to ensure a stable transition.

5.1.3 Role of Resistors

- The 100Ω resistor between push button of DOWN and NOT gate acts as a current-limiting resistor to prevent excessive current when the DOWN button is pressed.
- The 15kΩ pull-down resistors ensure the logic state of the gates remains LOW when no buttons are pressed, avoiding floating inputs.

5.2 Working Principle of clock-pulse generation circuit and DIR

5.2.1 Working of clock pulse for units and tens digit

- For the flip flops contributing to units digit, the clock pulse is given directly from clock-pulse generator circuit, so as to increment/decrement the digit.
- For the flip flops contributing to tens digit, the clock signal is given by the **AND** of Q_0,Q_3, and the CLK generated by the clock-pulse generator circuit.

5.2.2 Logic behind the CLOCK of tens digit

- **Incrementing:**When the units digit reaches 9 and the UP button is pushed, the tens digit has to increase by 1. The BCD equivalent of 9 is 1001, which means the **AND** of Q_0,Q_3, and the CLK goes from 1 to 0,causing negative edge trigger and DIR becoming 1 results in incrementation of the tens digit.
- Since the 4-bits of units digit are synchronous, the units digit automatically resets to 0.
- **Decrementing:**When the units digit reach 0 and the DOWN button is pushed, the tens digit has to decrease by 1. The BCD equivalent of 9 is 1001, which means the **AND** of Q_0,Q_3, and the CLK goes from 1 to 0,causing negative edge trigger and DIR becoming 0 results in decrementation of the tens digit.
- Since the 4-bits of units digit are synchronous, the units digit automatically resets to 9.

5.3 T-Flip-flop sub circuit and Decoder and 7-segment setup

5.3.1 T-Flip-flop sub circuit for units digit

- Each flip-flop receives CLOCK from clock-pulse generator circuit.
- Since we are using T-flip-flops, for IC 7476, both J and K are given same logic.

- Each flip flop input requires corresponding logic, it it listed in logic section. The logic is provided using whatever ICs are required.
- The outputs Q_0 to Q_3 for each digit are generated by 4 flip-flops whose manual connections and logic are mentioned above.

5.3.2 T-Flip-flop sub circuit for tens digit

- Each flip-flop receives CLOCK from the **AND** of Q_0, Q_3 and CLK generated from clock-pulse generator circuit.
- Since we are using T-flip-flops, for IC 7476, both J and K are given same logic.
- Each flip flop input requires corresponding logic, it it listed in logic section. The logic is provided using whatever ICs are required.
- The outputs Q_0 to Q_3 for each digit are generated by 4 flip-flops whose manual connections and logic are mentioned above.

5.3.3 Decoder and 7-segment display

- The outputs Q_0 to Q_3 for each digit are generated by 4 flip-flops whose manual connections and logic are mentioned above.
- For each digit, each of Q_0 to Q_3 outputs are sent to IC 7447 decoder and from there, the corresponding number is displayed on seven-segment display.

6 Conclusion

Hence, we can implement a double digit partially synchronous counter using Boolean logic and T-Flip-Flops.