CPE301 – SPRING 2019

Design Assignment 1B

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Primary Github address: https://github.com/eed911/class\_proj.git

Directory: Repository/cpe301/da1b

Submit the following for all Labs:

1. In the document, for each task submit the modified or included code (only) with highlights and justifications of the modifications. Also, include the comments.
2. Use the previously create a Github repository with a random name (no CPE/301, Lastname, Firstname). Place all labs under the root folder ESD301/DA, sub-folder named LABXX, with one document and one video link file for each lab, place modified asm/c files named as LabXX-TYY.asm/c.
3. If multiple asm/c files or other libraries are used, create a folder LabXX-TYY and place these files inside the folder.
4. The folder should have a) Word document (see template), b) source code file(s) and other include files, c) text file with youtube video links (see template).

1. **COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS**

List of Components used

N/A

Block diagram with pins used in the Atmega328P

N/A

1. **INITIAL/MODIFIED/DEVELOPED CODE OF TASK 1/A**

;

; Project1B.asm

;

; Created: 2/23/2019 6:39:21 PM

; Author : Cody Hudson

;

RESET:

; INITIAL PARAMETERS

.EQU STARTADDS = 0X0200

.EQU COUNT = 99

.ORG 0

LDI XL, LOW(STARTADDS) ;INITIALIZES [X] = 0X0200

LDI XH, HIGH(STARTADDS)

LDI YL, LOW(0X400) ;INITIALIZES [Y] = 0X0400

LDI YH, HIGH(0X400)

LDI ZL, LOW(0X600) ;INITIALIZES [Z] = 0X0600

LDI ZH, HIGH(0X600)

; INITILIZING COUNT REGISTERS

LDI R21, COUNT ;R21 = 99

LDI R22, 10 ;R22 = 10 STARTING POINT OF COUNTER

LDI R20, 3 ;R20 = 3

LDI R23, 1

; CLEARING REGISTERS FOR SUMS

CLR R0 ;R0 = 0

CLR R16 ;R16 = 0

CLR R17 ;R17 = 0

CLR R18 ;R18 = 0

CLR R19 ;R19 = 0

START:

; ASSING LOWER AND UPPER ADDRESS BITS TO BE STORED

MOV R1, XL ;R1 = XL

ADD R1, XH ;R1 = XH + XL

MOV R3, R1 ;R3 = R1

ADD R3, R22 ;R3 = 10 + R3

ST X+, R3 ;STORES VALUE OF R3 INTO INCRIMENTED "X" POINTER OF STACK

DIVBYTHREE:

; CHECKING IF DIVISABLE BY 3

CP R1, R20

BRLO DIVBAD ;IF R1 < 3 GOTO DIVBAD

SUB R1, R20 ;R1 - 3

CP R1, R0

BREQ DIVGOOD ;IF R1 = 0 GOTO DIVGOOD

RJMP DIVBYTHREE ;GO BACK TO DIVBYTHREE

DIVGOOD:

; STORING VALUES IN STACK USING "Z" POINTER IF DIVISABLE BY 3 AND SUMMING TOGETHER

SUB R3, R23 ;TANKING IN ACOUNT THTAT R3 IS BING INCRIMENTED IN THE NEXT LINE R3=R3-1

ST Y+, R3 ;STORES VALUE OF R3 INTO INCRIMENTED "Z" POINTER OF STACK

ADD R16, R3 ;R16 = ZH + ZL

ADC R17, R0 ;R17 = CARRY VALUE FROM LINE ABOVE

RJMP DONE ;GO TO DONE

DIVBAD:

; STORING VALUES IN STACK USING "Y" POINTER IF NOT DIVISABLE BY 3 AND SUMMING TOGETHER

SUB R3, R23 ;TANKING IN ACOUNT THTAT R3 IS BING INCRIMENTED IN THE NEXT LINE R3=R3-1

ST Z+, R3 ;STORES VALUE OF R3 INTO INCRIMENTED "Y" POINTER OF STACK

ADD R18, R3 ;R18 = YH + YL

ADC R19, R0 ;R19 = CARRY VALUE FROM LINE ABOVE

RJMP DONE ;GO TO DONE

DONE:

CP R21, R0

SUBI R21, 1 ;R21 = 21 - 1

BRNE START ;IF R21 != 0 GO BACK TO START

FIN:

RJMP FIN ;ENDLES LOOP TO SHOW FINISH

1. **DEVELOPED MODIFIED CODE OF TASK 2/A from TASK 1/A**

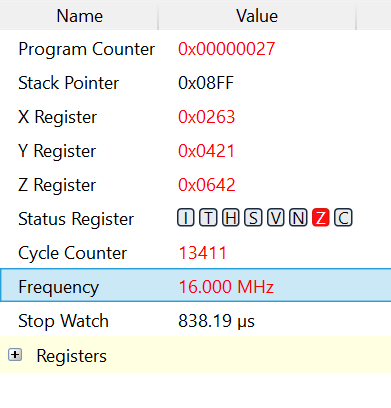
Insert only the modified sections here

1. **SCHEMATICS**

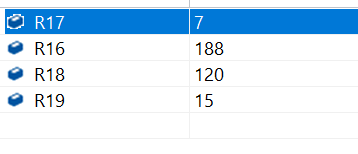
N/A

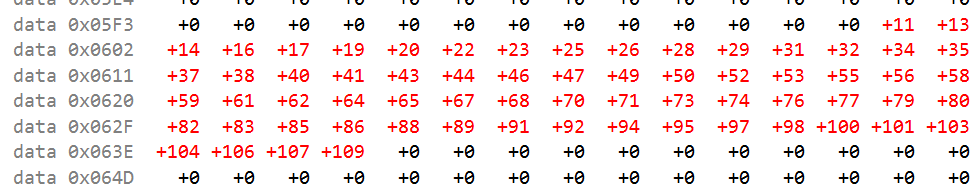
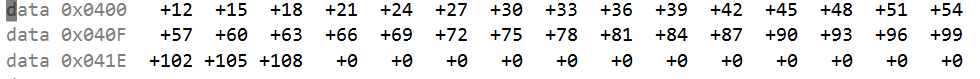
Use fritzing.org

1. **SCREENSHOTS OF EACH TASK OUTPUT (ATMEL STUDIO OUTPUT)**



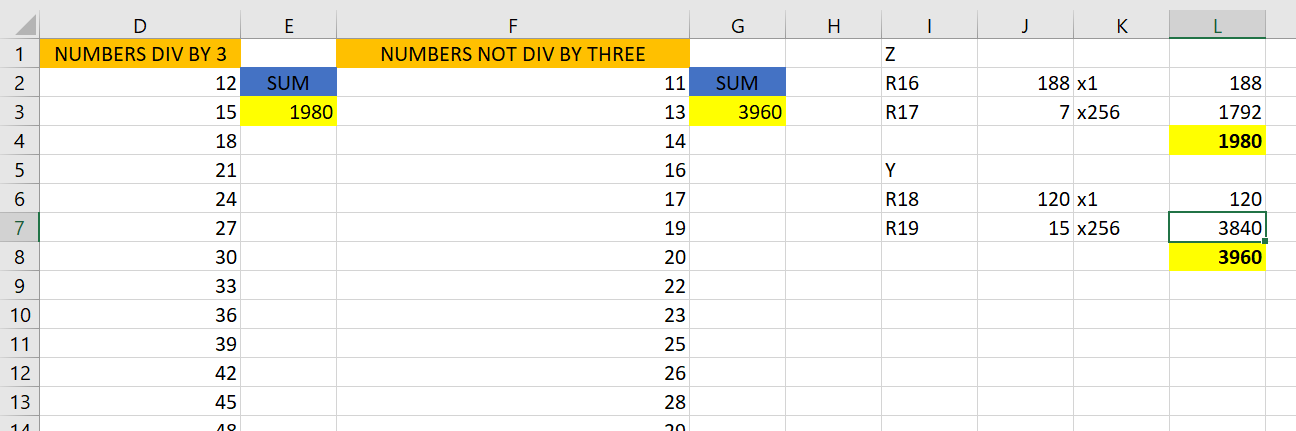
PROCESSOR STATUS: REGISTERS USED:



IRAM VALUES STORED VALUES IN STACK

Verification:

Verification was done using EXCELL for convince.



Note to the right shows the math of how my register values are correct.

1. **SCREENSHOT OF EACH DEMO (BOARD SETUP)**

N/A

1. **VIDEO LINKS OF EACH DEMO**

N/A

1. **GITHUB LINK OF THIS DA**

https://github.com/eed911/class\_proj.git

**Student Academic Misconduct Policy**

<http://studentconduct.unlv.edu/misconduct/policy.html>

“This assignment submission is my own, original work”.

Cody Hudson