CPE301 – SPRING 2019

Design Assignment 2B

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Primary Github address: https://github.com/eed911/class\_proj.git

Directory:

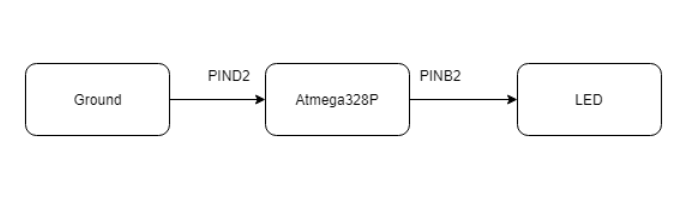
https://github.com/eed911/class\_proj/tree/master/DesignAssignments/DA2B/Project\_2B

1. **COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS**

List of Components used

* ATmega328P Xplained
* Muli Function Shield
  + LED
  + GROUND

Block diagram with pins used in the Atmega328P



1. **INITIAL/MODIFIED/DEVELOPED CODE OF TASK 1/A**

Task 1 Assembly Code:

;

; DA2B\_ASM.asm

;

; Created: 3/8/2019 7:55:29 PM

; Author : Cody Hudson

;

.ORG 0

RJMP START ;JMPS TO START

.ORG 0x02

RJMP EXO\_ISR ;JMPS TO EXTERNAL INTRUPT SUBROUTINE

START:

LDI R16, 0x04 ;LOADS 0b00000100 IN R 16

OUT DDRB, R16 ;SETS DIRECTION AS OUTPUT AT BIT 3

OUT PORTB, R16 ;SETS PULL UP RESISTOR AT PIN 3 OF B

LDI R17, 0x00 ;LOADS 0b00000000 INTO R17

OUT DDRD, R17 ;SETS DIRECTION AS INPUT FOR ALL D

SBI PORTD, 2 ;SETS PULL UP RESISTOR AT PIN 2 OF D

NOP

;Initialize Interrupt

LDI R20, 0x2 ;CONFIGURE INTERRUPT TO OCCUR INT0 FOR FALLING EDGE TRIGGER

STS EICRA, R20 ;LOAD CONFIGURE INTO REGISTER

LDI R20, 1<< INT0 ;ENABLE EXTERNAL INTERRUPT INT0(PD2)

OUT EIMSK, R20 ;LOAD ENABLE INTO REGISTER

SEI ;GLOBAL INTERRUPT ENABLE COMMAND

HERE: JMP HERE

EXO\_ISR:

LDI R21, 0xFB ;LOADS 0b11111011 ONTO R21

OUT PORTB, R21 ;TURNS ON LED

RCALL DELAY\_1S ;RUN THROUGH DELAYS

RCALL DELAY\_100MS

RCALL DELAY\_100MS

RCALL DELAY\_50MS

OUT PORTB, R16 ;TURN OFF LED

RETI

//SAME DELAY SUBROUTINE FROM BEFOR

DELAY\_1S:

RCALL DELAY\_100MS

RCALL DELAY\_100MS

RCALL DELAY\_100MS

RCALL DELAY\_100MS

RCALL DELAY\_100MS

RCALL DELAY\_100MS

RCALL DELAY\_100MS

RCALL DELAY\_100MS

RCALL DELAY\_100MS

RCALL DELAY\_100MS

RET

DELAY\_100MS:

RCALL DELAY\_50MS

RCALL DELAY\_50MS

RET

DELAY\_50MS:

RCALL DELAY\_10MS

RCALL DELAY\_10MS

RCALL DELAY\_10MS

RCALL DELAY\_10MS

RCALL DELAY\_10MS

RET

DELAY\_10MS:

RCALL DELAY\_5MS

RCALL DELAY\_5MS

RET

DELAY\_5MS:

RCALL DELAY\_1MS

RCALL DELAY\_1MS

RCALL DELAY\_1MS

RCALL DELAY\_1MS

RCALL DELAY\_1MS

RET

DELAY\_1MS:

PUSH R16

PUSH R18

LDI R16,255

LDI R18, 6

DELAY\_1A:

DELAY1\_B:

NOP

NOP

NOP

NOP

NOP

NOP

NOP

NOP

DEC R16

BRNE DELAY1\_B

DEC R18

BRNE DELAY1\_B

POP R18

POP R16

RET

Task 2 C code:

/\*

\* DA2B\_C.c

\*

\* Created: 3/8/2019 6:57:05 PM

\* Author : Cody Hudson

\*/

#define *F\_CPU* 16000000UL

#include <avr/io.h>

#include <util/delay.h>

#include <avr/interrupt.h>

int main(void)

{

DDRB |= (1<<DDB2);

PORTB |= (1<<PORTB2);

DDRD &= (0<<DDD2);

PORTD |= (1<<PORTD2);

EICRA = 0x2;

EIMSK = (1<<INT0);

sei ();

while(1);

}

ISR (INT0\_vect)

{

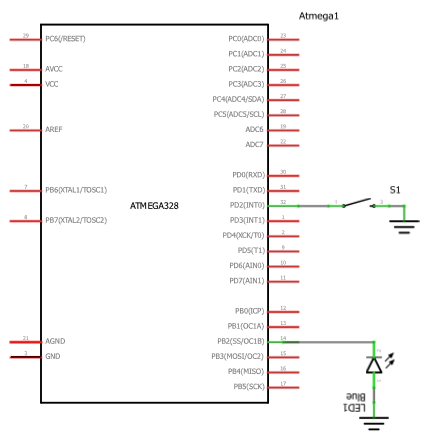
PORTB &= (0<<PORTB2);

*\_delay\_ms*(1250);

PORTB |= (1<<PORTB2);

}

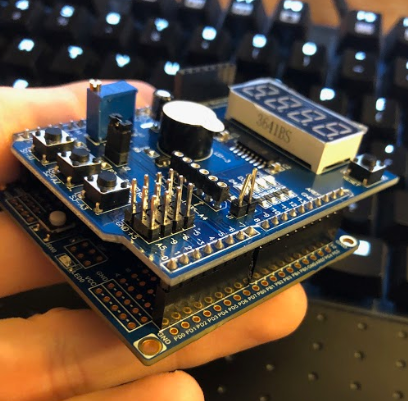
1. **SCHEMATICS**



1. **SCREENSHOTS OF EACH TASK OUTPUT (ATMEL STUDIO OUTPUT)**

N/a all demonstration is done via video on YouTube

1. **SCREENSHOT OF EACH DEMO (BOARD SETUP)**



1. **VIDEO LINKS OF EACH DEMO**

Demo1:

https://youtu.be/O5xUacfzj\_Y

Demo2:

https://youtu.be/84IsuzZ\_lbw

1. **GITHUB LINK OF THIS DA**

https://github.com/eed911/class\_proj.git

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<http://studentconduct.unlv.edu/misconduct/policy.html>

“This assignment submission is my own, original work”.

NAME OF THE STUDENT