COMPUTER HOLOGRAMS

author ; Stephen Barrass

supervisor ; Dr. Chu

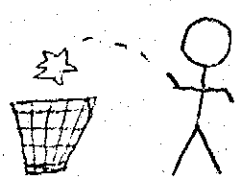
A Hologram is an image formed by manipulating both the phase and magnitude of electromagnetic waves.

This thesis will employ the'detour phase' hologram technique because it is well suited to computer plotter output. The main advantage of computer generated holograms is that the object need not physically exist except as an array of coordinates in the computer memory, as opposed to interferometric methods.

Several of these holograms will be used in an optical data processor as 'matched spatial filters'. This processor is a form of analogue computer which uses the properties of Fourier Transform lenses and the holographic filter to instantaneously output the solution to a convolution integral. This output describes the transmittance of an optical fibre preform and can be used to detect faulty preforms before they are drawn.

anticorrelation

new fandangled camera in physics



DO THE RIGHT THING

TITLE: DATA ACQUISITION ON A RING NETWORK

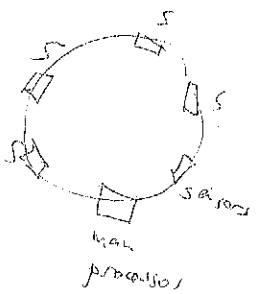
SUPERVISOR: Dr. P.G. McRae

SUBMITTED BY: E.G. Browne

SUMMARY: Sea noise is a parameter which is of great interest in the evaluation of sonar performance. One way of measuring the effect of sea noise is to drop a sensor array over the side of a ship and monitor the sea noise buoy sensors with a central processor. Communication of data between these remote sensors, and a central host, onboard the ship, is the essence of this topic.

For this task a low powered ring network is being developed. The following material then, is an outline of the project and includes:

1. LOCAL AREA NETWORK (LAN) topologies
2. TOKEN PASSING
   a) THE TOKEN RING
   b) FRAME FORMAT
3. DESIGN OF HARDWARE
   a) The master station
   b) The slave station
   c) Self clocking
4. SOFTWARE
5. THE ADLC ALTERNATIVE



Main Reference:

A.S. Tanembaum, "Computer Networks", Prentice Hall, 1982

THESIS SEMINAR

L.I.
H.I. Pager : - keyboard

Topic: 'Remote Control of a Microcomputer'

Speaker: Anthony Craner — Radio link — RS232 300 baud low power/cost bi-directional

NEC
AIM-65
6809
HP85

Supervisor: Proff. A.E. Karbowiak

Date: 24th September, 1985

- ASK before
- 27.290 MHz

The increased use of microprocessors in household appliances, such as ovens, microwaves, dishwashers, allow the possibility of control of these devices by a central personal computer. This thesis looks at the feasibility of having a hand held pager to communicate with the central host computer and thereby control the ancillary devices.

This is a group thesis with my involvement being the construction of the data communications link.

The major factors influencing the design of the communications link were; the unit had to be of low cost, consume low power, for battery operation as a hand held device, and communications had to be bi-directional.

The form of modulation used for transmission of data is frequency shift keying (F.S.K.). The carrier is shifted between two frequencies according to whether the data is a 'mark' or 'space'. The F.S.K. signal is then transmitted by a modified AWA 27 MHz amplitude modulation radio. From the receiving radio the F.S.K. signal is then demodulated to give the serial data.

- Home environment — fading
- other CB interference
- Future Modifications / error checking / storage

PROGRAMMABLE SCANNING OF LASER BEAMS.

(Topic number 23) Scott Domars

Aim:

The aim of this thesis is to scan a laser beam by stepper motors controlled from a 6809 based microprocessor system. By using the microprocessor in this way, accurate control over scan angles and inclinations is possible.

Outline:

Once constructed, the motor control software can be configured for tracking, or television-type scanning of images, or projections. Similarly, by using the scanner to select a particular target a chopped laser beam can be sent to one of a number of recievers; rather like a telephone exchange.

This unit, under the control of suitable software, is both versatile and accurate in a number of communications type applications. It also has the potential for many user applications, by creating customised software, for many other jobs as well.

- 100 steps/rev ; 7½° step
- FROM TTL INTO ... "THE REAL WORLD"
- How that'll be forthcoming
- HeNe 2mW laser
- BD139 reactive

resolution = f(range)

TESTING — parallel control > board
detector
motor rotation

Entered tgts exec.

Topic : A General Purpose Switched Capacitor Filter.
Supervisor : Prof. G. A. RIGBY
Speaker : T. H. GHEE

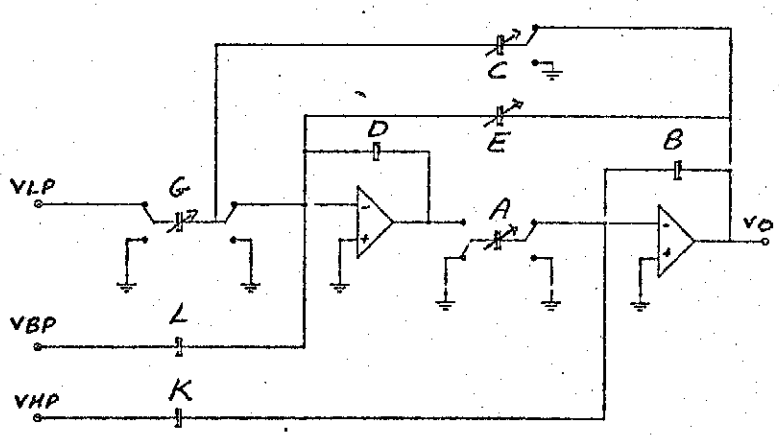
The aim of this thesis is to design and fabricate a programmable general purpose switched capacitor filter. This could be used as a basic cell for use in larger signal processing designs. It is a second order filter with a transfer function of the form :

$$H(s) = \frac{V_o(s)}{V_{in}(s)} = -\frac{K_2 s^2 + K_1 s + K_0}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2}$$

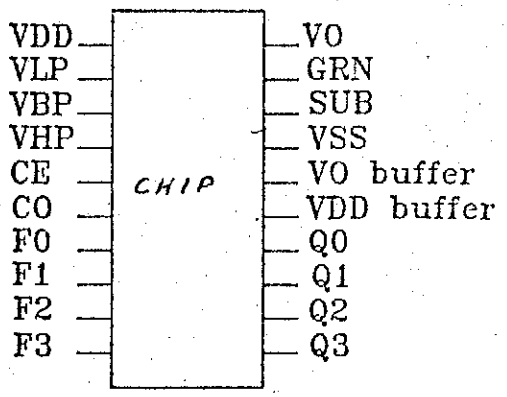
and is generally called a biquad.

The Q and centre frequency response of the filter are controlled by seperate 4-bit digital input which may be hard wired or microprocessor controlled. The clock phases used to operate the switches are to be non- overlapping. The filter type is chosen by hard wire programming the filter input. For optimum performance, all unused inputs should be grounded. The design of this filter is for Q > 1 and is suited for signal frequencies less than 20kHz. For higher frequency operation, the size of the transmission switches as well as the slew rate of the amplifier have to be increased.

The design also incorporate an independently controlled buffer at the output to provide additional current drive for the output signal. The design and layout of the circuit is in metal gate n-well CMOS technology and is fabricated in the Microelectronics laboratory, School of Electrical Engineering, UNSW.



S-C FILTER



Filter type	VLP	VBP	VHP
Lowpass	Vin	Grn	Grn
Bandpass	Grn	Vin	Grn
Highpass	Grn	Grn	Vin
Notch	Vin	Grn	Vin

SELECT TABLE

"DIGITAL IMAGE COMPRESSION AND VIATEL"

Susan Jimenez
27 - 9 - 85

Supervisor: Dr C. Phillips

Aim: To use Image Compression techniques to provide a digital image transmission system, for use on Viatel, that has adequate resolution and display speed.

Design Specifications:

* a resolution of 256 x 256 pixels ~5min @1200band
* transmission of two-tone as well as 16 grey scale or colour images
* display speed of 10 - 20 seconds. (update of screen)

METHODS OF IMAGE COMPRESSION

Image Compression techniques attempt to minimise the amount of information required for transmission and representation of an image, utilizing the redundancy or predictability inherent in picture information.

There are two main categories:

* Exact coding - where the image may be reconstructed from the encoded data, suitable for two-tone images.
* Approximate coding - where some distortion is introduced into the reconstructed image in exchange for high compression, suitable for 16 level images.

a) Exact Coding Methods

i) Runlength Coding

* Instead of transmitting regions or runs of uniform colour pixels the length and colour of the run is encoded and transmitted.
* gives fair compression on two-tone images
* poor compression for 16 levels.

ii) Quadtrees

Hierarchical data structures generated by dividing an image into quadrants and repeatedly subdividing the quadrants into subquadrants until each subquadrant has uniform colour.

* disappointing results for images tested
* published results claim high compression achieved.

b) Approximate Coding Methods

i) Differential Pulse-Code Modulation (DPCM)

A prediction is made of the present sample based on previously transmitted information. The error or difference between the predicted and actual value is the encoded and transmitted . Exact coding methods may then be applied to the error signal to achieve high compression.

ii) Adaptive Predictive Coding

The prediction algorithm is selected according to the contour of the surrounding area. Hence a better prediction is achieved, the picture quality is improved and better compression obtained.

- BOARD LAYOUT
- MEMORY MAP
- FLOWCHARTS
- MENU TABLES

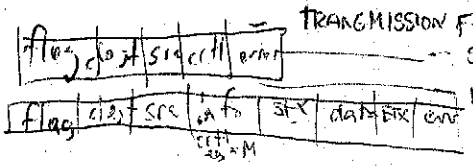
THESIS SUMMARY

24th September , 1985

Topic : REMOTE CONTROL OF MICROCOMPUTERS

Student : BILL M.S. LAM

Supervisor : PROF. A.E. KARBOWIAK



Society today and especially in the future will be strongly influenced by microcomputers and other high technology innovations that would help make our lives easier. The task for this thesis is the design and construction of such an innovation. It will be a remote control device that would communicate with microcomputers from a distance.

For this thesis, the home environment was assumed with the view of a central microcomputer monitoring and controlling most of the appliances.

The main aim of this thesis is to design a remote control device or pager to understand English vocabulary word instructions such as " TURN OVEN ON ". The pager after recognising the item and its function would send the appropriate signal to the host computer by radio wave link with the result that the host microcomputer would turn the oven on. The pager is described as being of high intelligence because it would be capable of sending the same signal if the user happens to type " TURN ON OVEN " or even " TURN STOVE ON " (assuming oven=stove).

In addition, this pager will also function as a typical pocket beeper or pager except that it has the added feature of the user sending back a reply.

The hardwire used for this thesis consists of a 6809 microprocessor with the necessary support chips and power supply. Data is accepted through an alphanumeric keyboard and the display is a Liquid Crystal Display (LCD).

The software mainly consists of a series of subroutines initiated by the use of interrupts.

IMPLEMENTATION OF COMMUNICATION SYSTEMS USING DIGITAL SIGNAL PROCESSING CHIPS

SPEAKER : CHEE KHOON, LEE
SUPERVISOR : DR. R. RADZYNER

The Intel 2920 is a programmable signal processing chip. It has on-chip programme and scratch pad memory, D/A and A/D converters, sample-and-hold circuitry, and a high speed processor. It is thus a stand-alone sampled data system.

The aim of this thesis project is to equ lize the group delay of the S3528 programmable low-pass elliptic filter using the Intel 2920 as an IIR all-pass filter.

If the filter consists of more than one pole-zero pair, the composite group delay can be found by summing the group delay of each pole-zero pair. This is implemented in a Pascal programme which enable the user to specify the parameters of the all-pass filter and then obtain the plot of the group delay against the input signal frequency. The programme also provides a procedure to automatically adjust the parameters of the filter to fit its group delay to a set of data.

Another programme was developed to simulate the operation of the 2920. It reads the 2920 instructions and then carries out each step of the 2920 code on an internally generated input (a sine wave). There are two purposes in writing this programme.

1. To check that the assembler code produces the required output without 'burning' a 2920 chip, which will shorten its life span.
2. If there is an overflow generated by the assembler code, the part of the code which causes this can can be detected. Thus the best overall gain of the filter can be obtained.

Although this thesis project only equ lises the group delay of the S3528 elliptical filter, the developement system can be used to equ lise any other systems given its group delay versus input frequency plot.

JOHN LOCK

HIGH QUALITY DIGITAL AUDIO COMPANDING

BACKGROUND

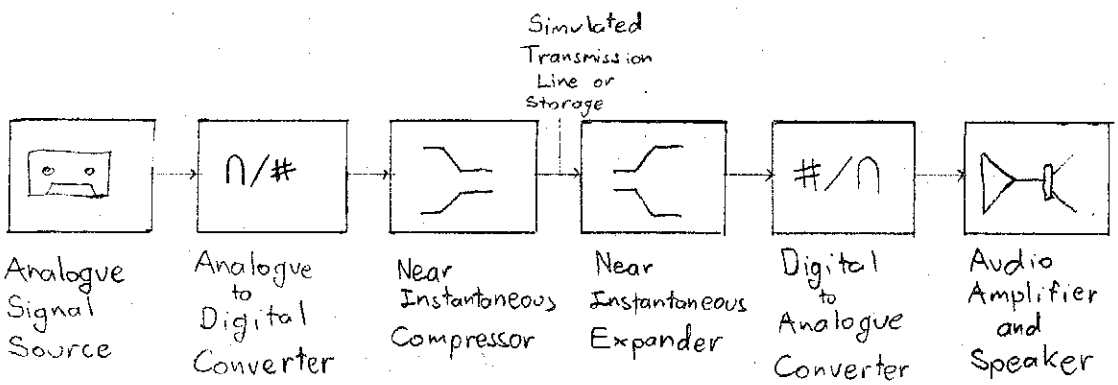
A High quality Digital Audio system requires both a large number of bits per sample and a high sampling rate. When program material of this type is to be transmitted of stored, high bit rates and extensive storage systems are required. The proposed system, originally developed in the United Kingdom, can reduce bandwidth requirements by thirty percent with no audible loss of quality. This bandwidth reduction represents a substantial reduction in costs for both storage and transmission.

TODAY

The operation of the near instantaneous companding system will be explained. Similarities between near instantaneous and instantaneous (mu and A law) companding systems will be drawn.

A demonstration will be given in which a 14 bit digital audio signal will be compressed to 13.03, 12.06, 11.06, 10.09, 9.09 and 8.09bits. The coded signal thus obtained will then be expanded back to its original 14 bit format for digital to analogue conversion. Comparisons will be made with a standard two's compliment system of similar bits per sample.

The system used for this demonstration appears in block form below.



Microprocessor Controlled Data Logging Equipment

At present there are a number of microprocessor chips on the market; all of which are capable of accepting data in one form or another for either storage or program data.

The designer of such a system is sometimes confused as to the correct choice for a specific task. A prime factor in determining the particular microprocessor is available board space, ease of reproduction of the system, power consumption and availability.

For these reasons the 146870502 microcomputer was chosen. It's on board timer, EPROM, various input/output ports, RAM and low power consumption make it very attractive as a stand-alone host for a computer system; to drive anything from a microwave oven to remote control data logging.

The development system used to load the microcomputer is the AM60. The somewhat unconventional method of down-loading the microcomputer will be tested in the next week, where a test program will be loaded. Ultimately a link via UNIX will be incorporated.

Mark Pace (25th September 1985)

? dip available

26Sep85

THESIS SEMINAR

AN INTELLIGENT HARMONISER

Speaker : George Moessis

Supervisor : W.H.Holmes

The aim of this thesis is to design and build a 'black box' which musicians can use to 'create' a harmony, in real time, from a given melody.

The harmony is constructed by sampling the melody at a constant rate whilst reading out the samples at a different rate dependent on the harmony required. This has the same effect as playing a recorded tape at a different speed to that of which it was recorded except that here the melody will not be distorted in time as with a tape.

Since harmony is dependent on key signature and pitch (of each note) a method of key and pitch determination is required.

A Sergeboard microprocessor development system (6809 based) is used with appropriate hardware to perform the following functions.

- ZN448 SUC APRX ADC

f_{sc} 104 kHz (920

I) Control of deglitching circuitry.

2) Key detection.

3) Pitch detection.

4) New note detection.

5) Control of the phase locked loop.

6) To compose harmony.

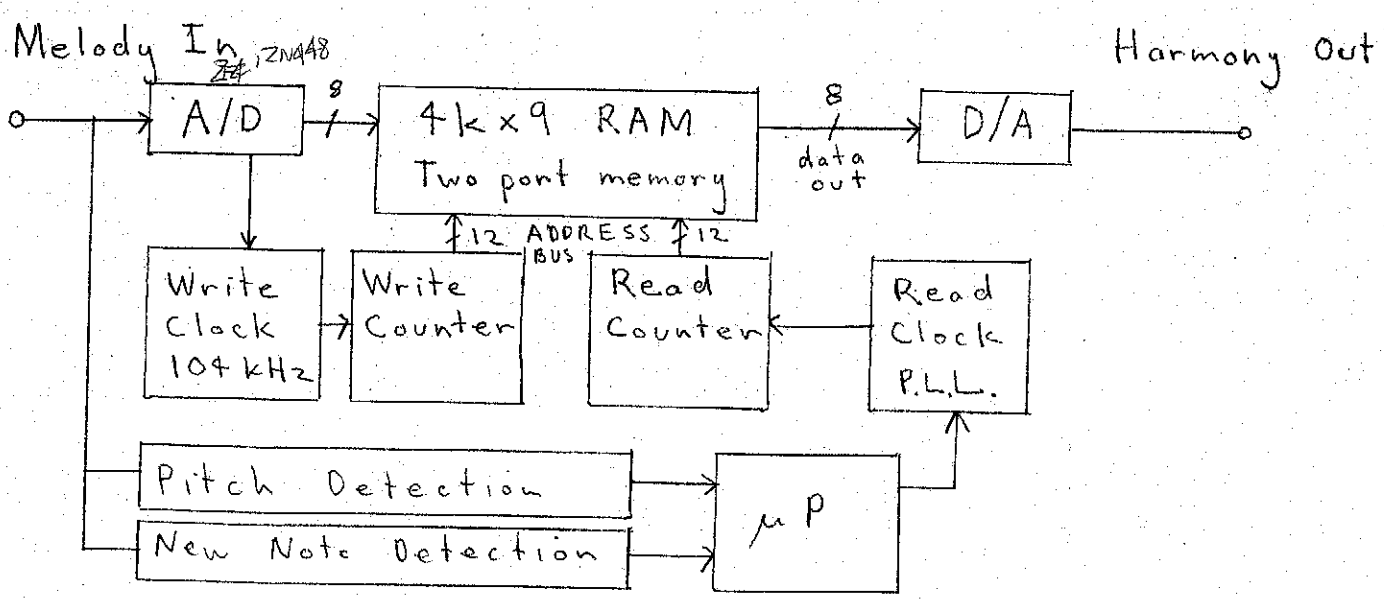


Figure I: Simplified block diagram of harmoniser.

DIRECT CONVERSION RECEIVER

Thesis seminar by Brian Murphy

Supervisor: T.L. HOOPER

Conventional A.M. receivers are of the superheterodyne type which consist of mixing the incoming signal down to an intermediate frequency (I.F.) at which stage the signal is filtered to remove unwanted components, then amplified before being demodulated using an envelope detector. Selectivity of the receiver (i.e. the ability of the receiver to reject unwanted signals) is determined by the filter characteristics of the I.F. stage. However bandpass filters centred at this frequency (455 kHz) with a narrow passband are very difficult to design resulting in some attenuation of the wanted components, and thus poor selectivity.

A direct conversion receiver, on the other hand, mixes the incoming signal directly down to baseband (i.e. a zero I.F.) thus eliminating the need for tuned circuits and the selectivity is provided by lowpass filters in the audio range which are easily designed to have very sharp cut-off characteristics.

A significant problem with this form of receiver is that the local oscillator must exactly match the carrier of the incoming signal. In order for this to be achieved it is necessary to use some form of synchronisation to ensure they are exactly matched.

The aim of this thesis was to design and construct a direct conversion receiver which employed a phase locked loop arrangement to maintain synchronisation with the incoming signal in such a way that the carrier itself is not used. This means that the system will automatically 'lock' on to an incoming signal without the carrier being sent. Thus the receiver will be able to successfully demodulate suppressed carrier signals and so transmitter power may be reduced by not sending the carrier making the system much more efficient.

Application of VLSI Devices

to Radio Communication Networks (DMR project)

A number of VLSI devices have become available in recent years for improving the versatility of mobile radio telephone systems. Important applications of these new devices include:

- simplification of CALLING PROCEDURES,
- making possible DIRECT ACCESS from remote mobiles to data-base management systems,
- realisation of simplified AUTOMATED RELAYING procedures, and
- simplified RECORDING MESSAGES of unattended remote mobiles.

The prime motivation, is the adoption of the VME bus system as their standard for transporting data to and from a "front end" processor. A specific interest of this project is to use the serial bus of this system.

The role of this project is a PILOT investigation for the INTERFACING of a digital signal processor (TMS_320_10) to a general purpose micro_processor controller card (the EUROCARD) designed by the Department of Main Roads.

Having a Texas Instruments development system (the EVM) and the Motorola based micro_processor controller card, is not conducive to straightforward interfacing. This is especially so, when they are incompatible in regards to their speed and differing data line widths. This is one reason why the asynchronous communication link was required.

Before any interfacing can be implemented, each system's input and output connections to the 'outside world', including their availability, timing, have to be ascertained.

The hardware has been built and its testing software written. Also, the protocol, between the EVM and the EUROCARD, has been developed to allow efficient transfer of control and data information. At this stage, each device is able to originate one word (16 bits) of data, but not to interpret it. This is analogous to the simplex (i.e. half duplex) communication protocol.

In the ensuing weeks, more software will be written to complete the full duplex link, thus enabling control of the TMS_320_10 by the EUROCARD.

Bob Smith (23rd September '85)

Implementation of Communication Systems Using Digital Signal Processing Chips

A modem is a device which allows digital information transfer between two or more points via a cable or telephone line. It encodes outgoing data into a modulated analog signal and decodes incoming signals from other modems. They are typically used in networking computer terminals.

A Differential Phase Reversal Keying modulator and coherent demodulator was constructed from two Intel 2920 digital signal processors. The specifications were

1. Simplex channel operation
2. Bit rate of 1200 bits per second

A 2920 simulator was written in Pascal for use on an IBM PC. It was used as a developement tool to debug the modem program.

At this stage both systems have been completed and further modifications are planned to accommodate the demodulation of four phase PRK signals. Such a modem will have an improved bit rate of 2400 bits per second.

Mark Soo
23rd September 1985