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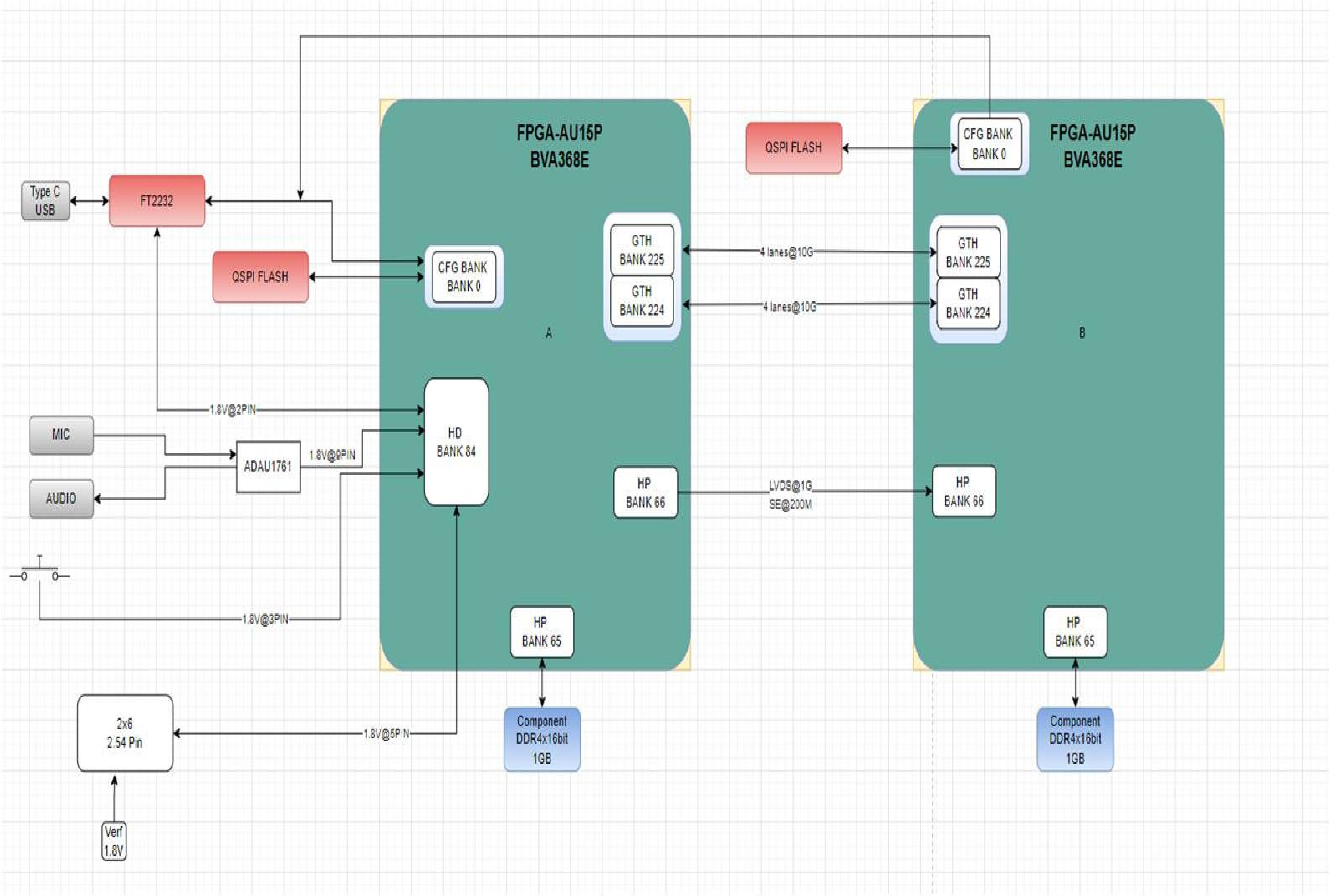
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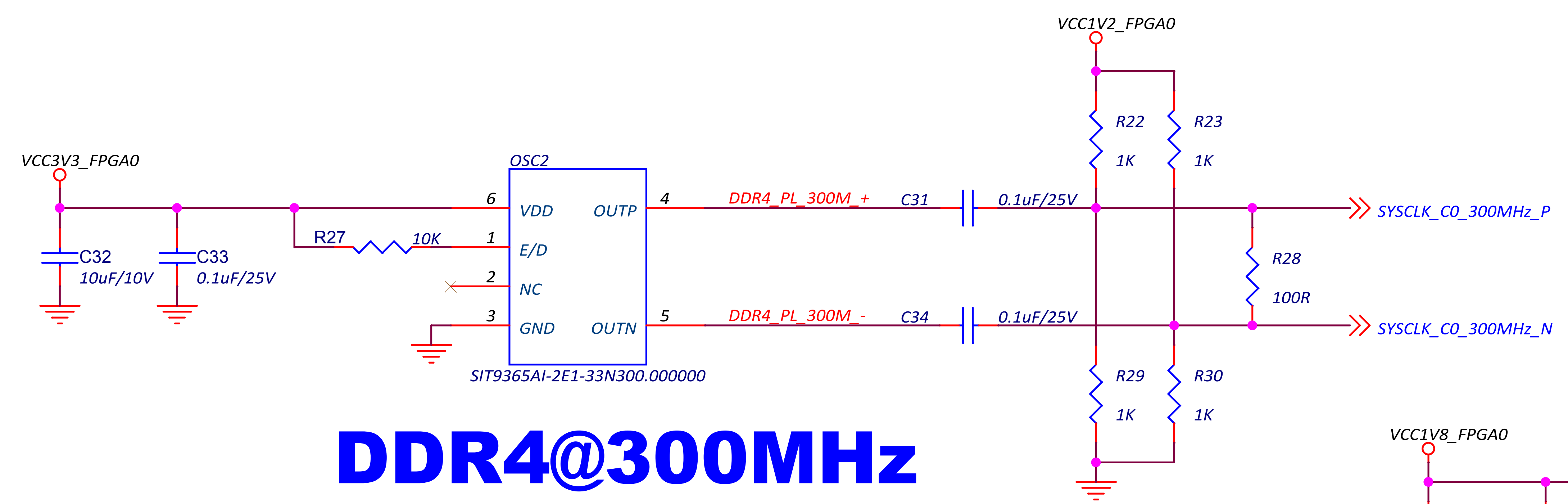
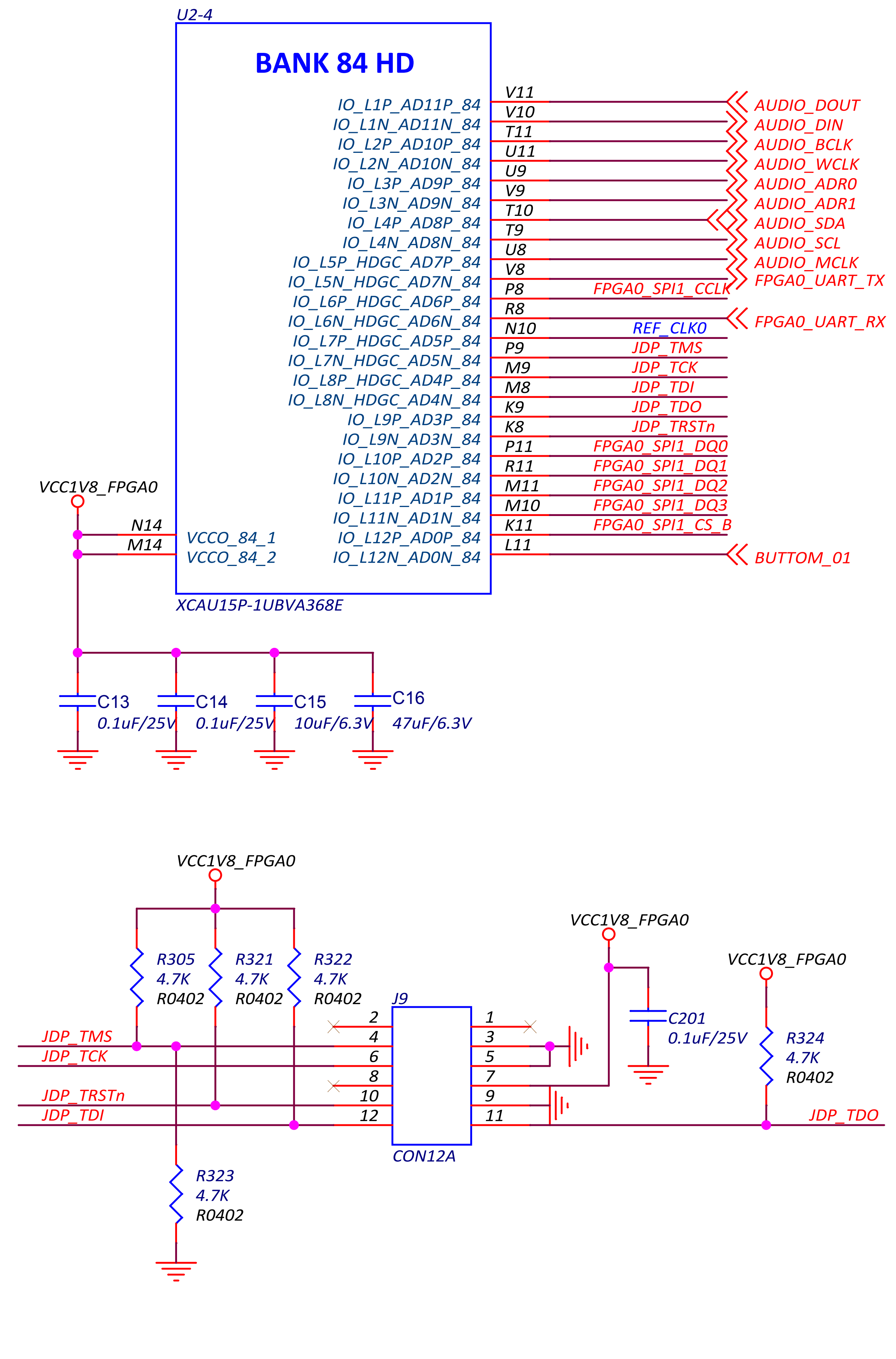
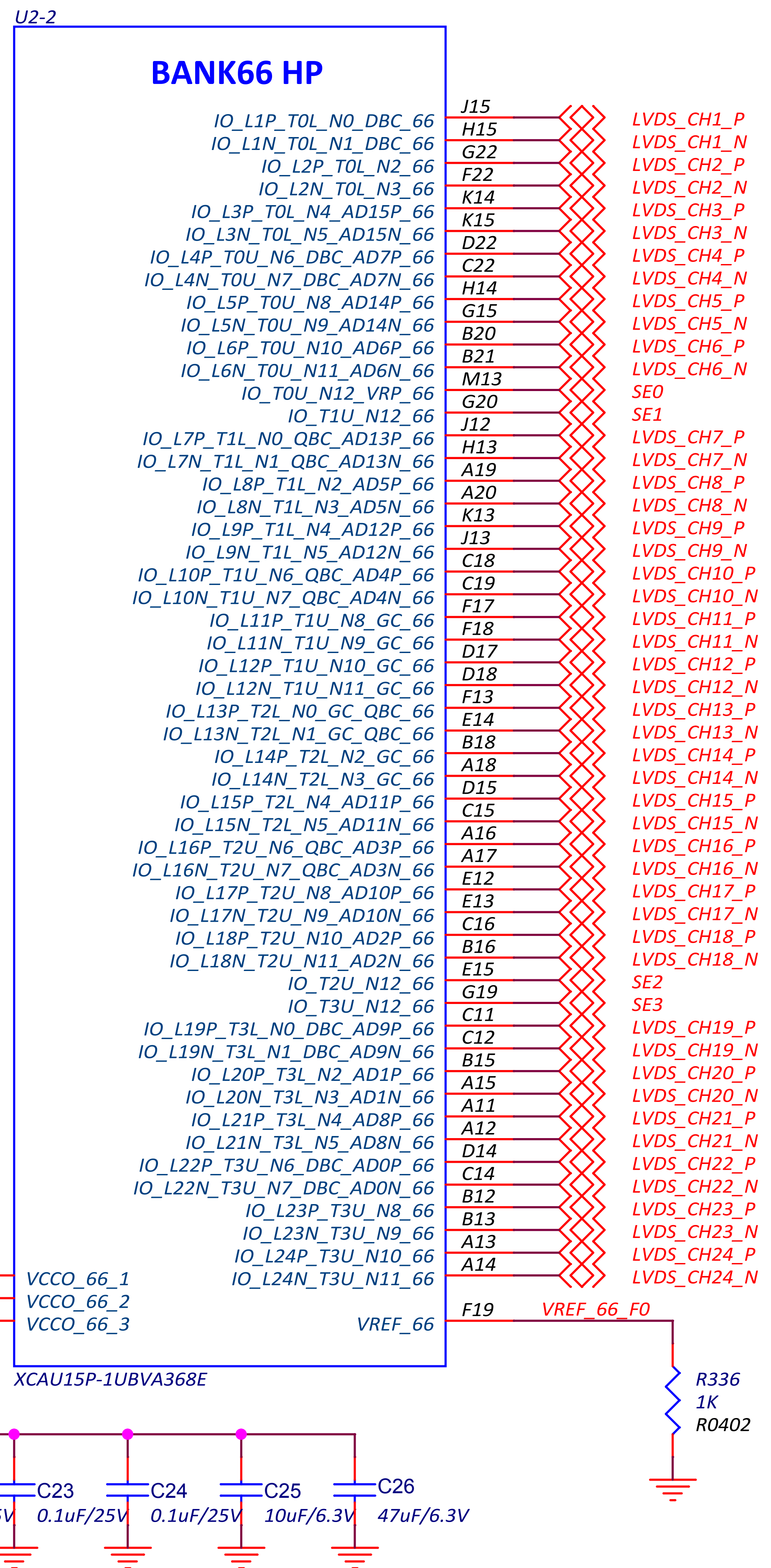
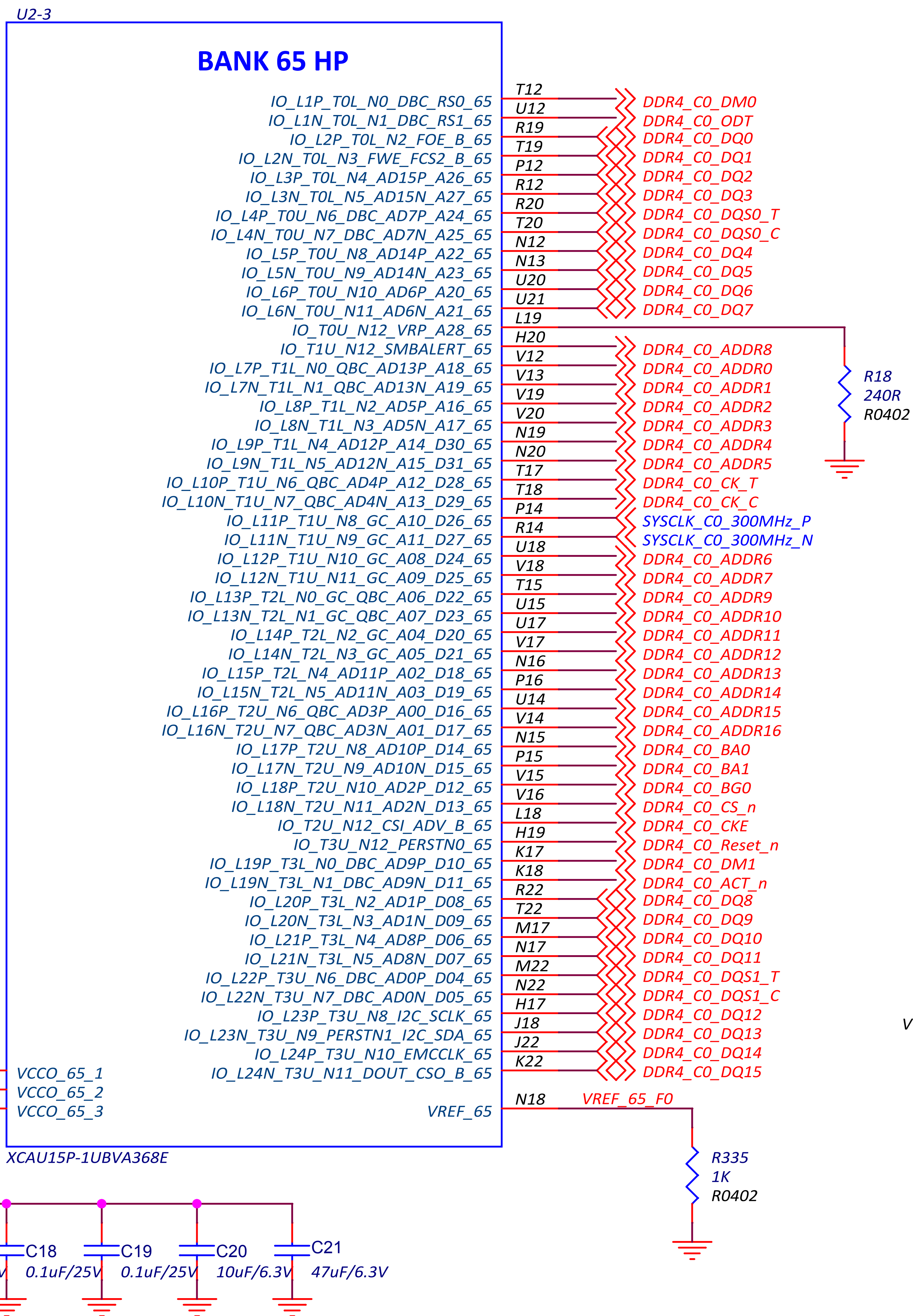
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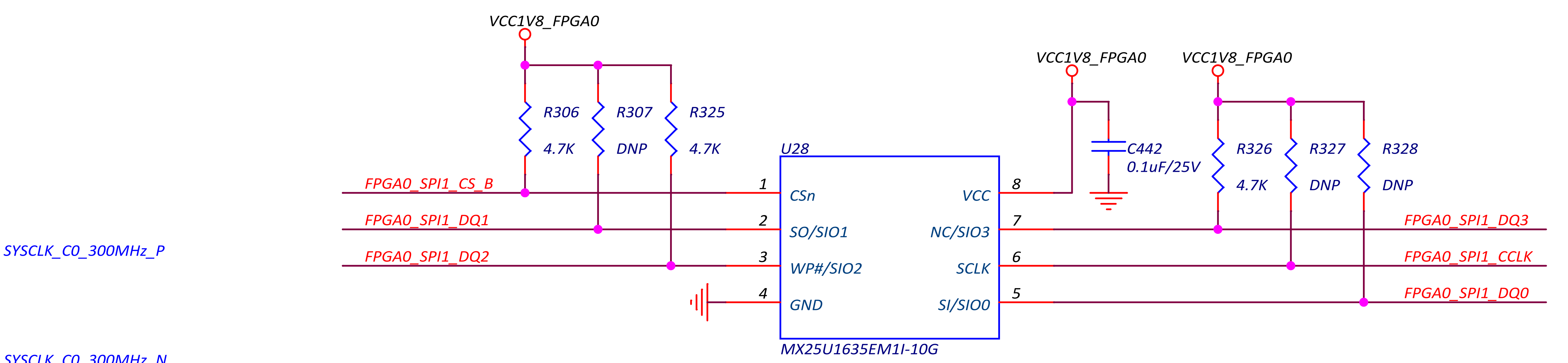
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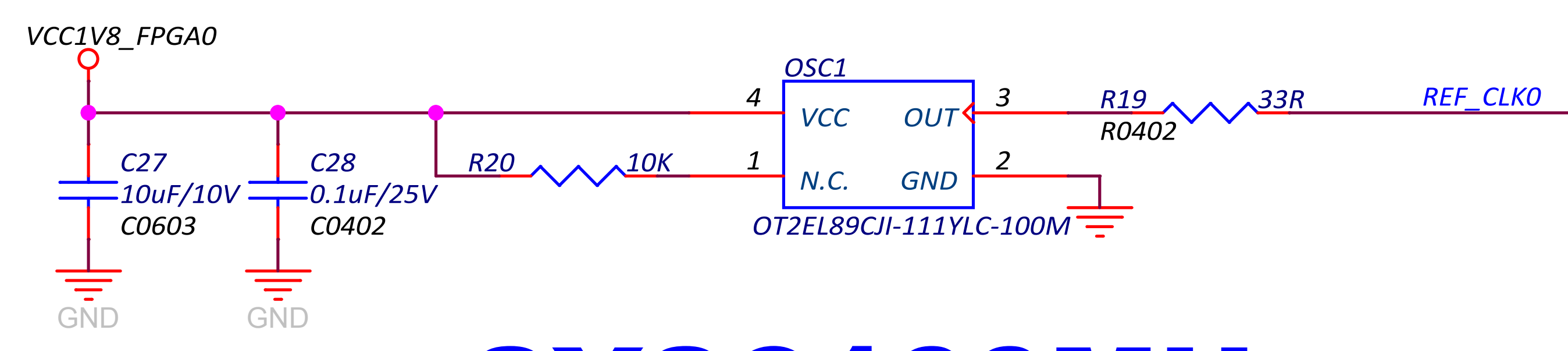




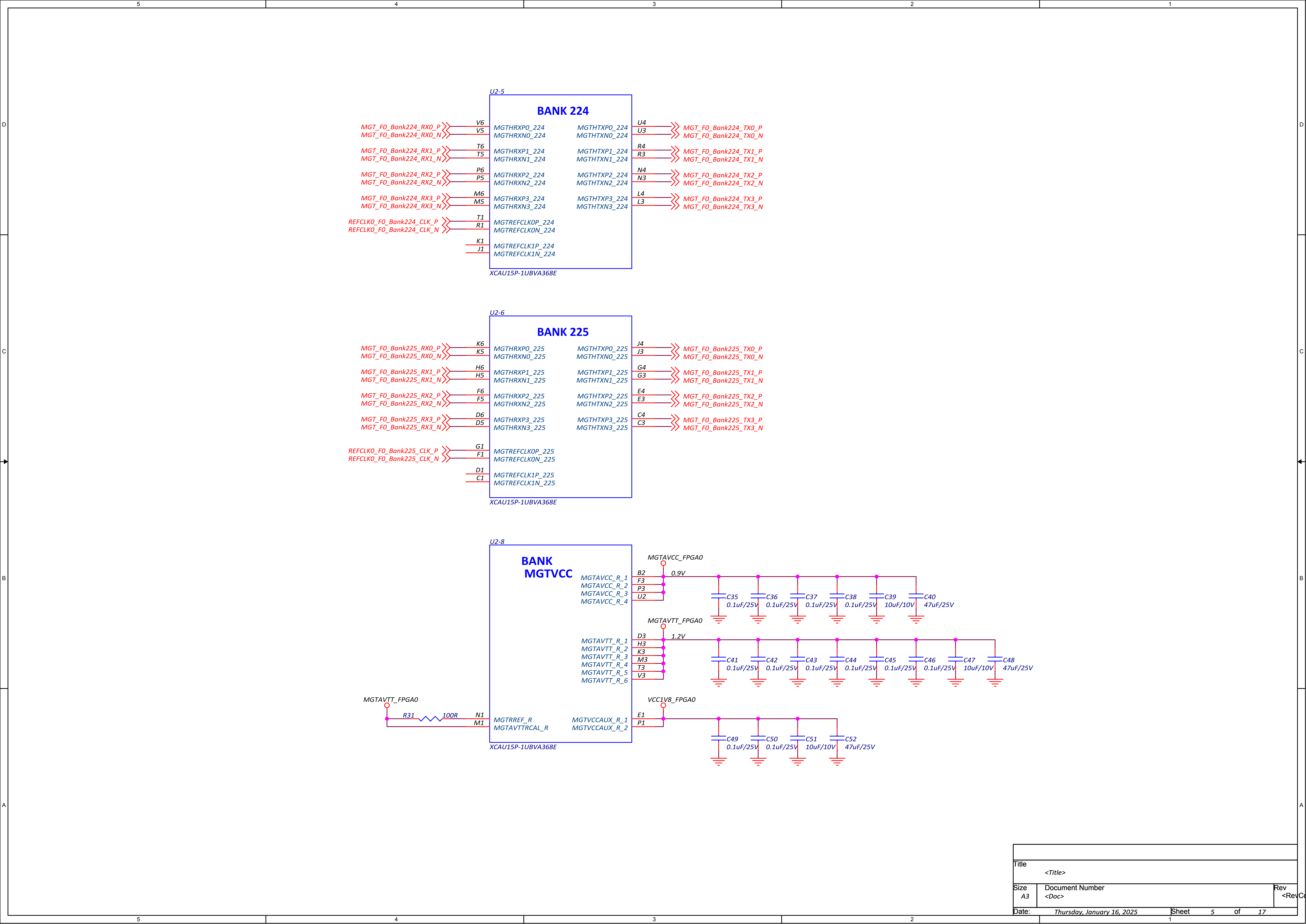
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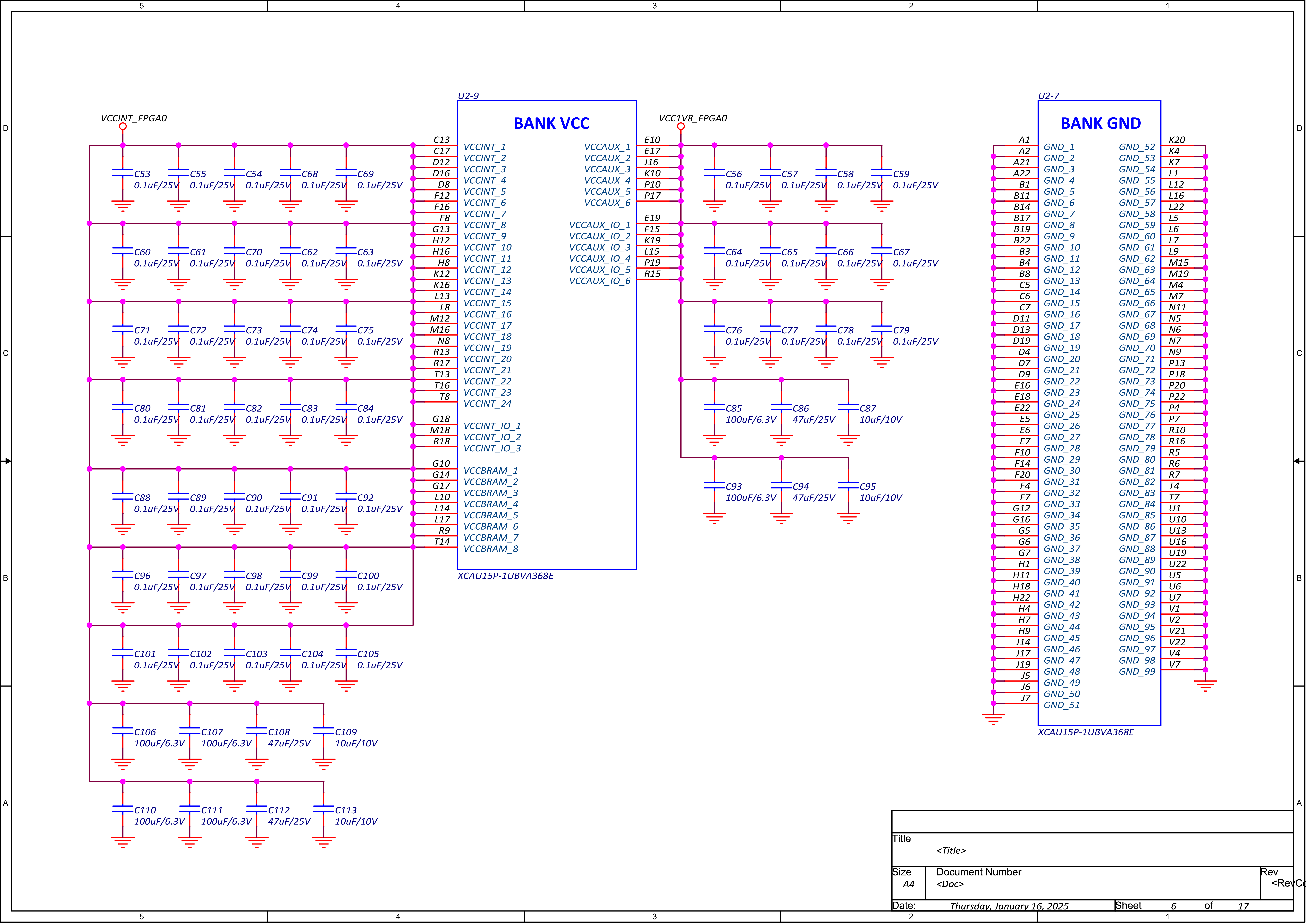


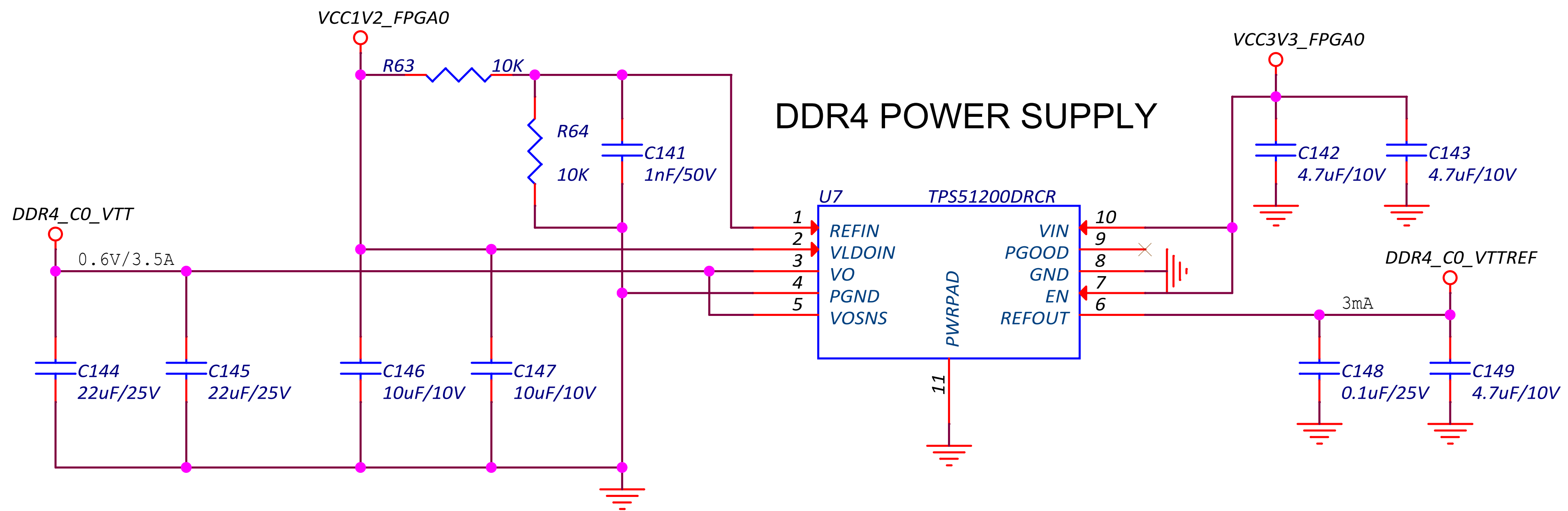
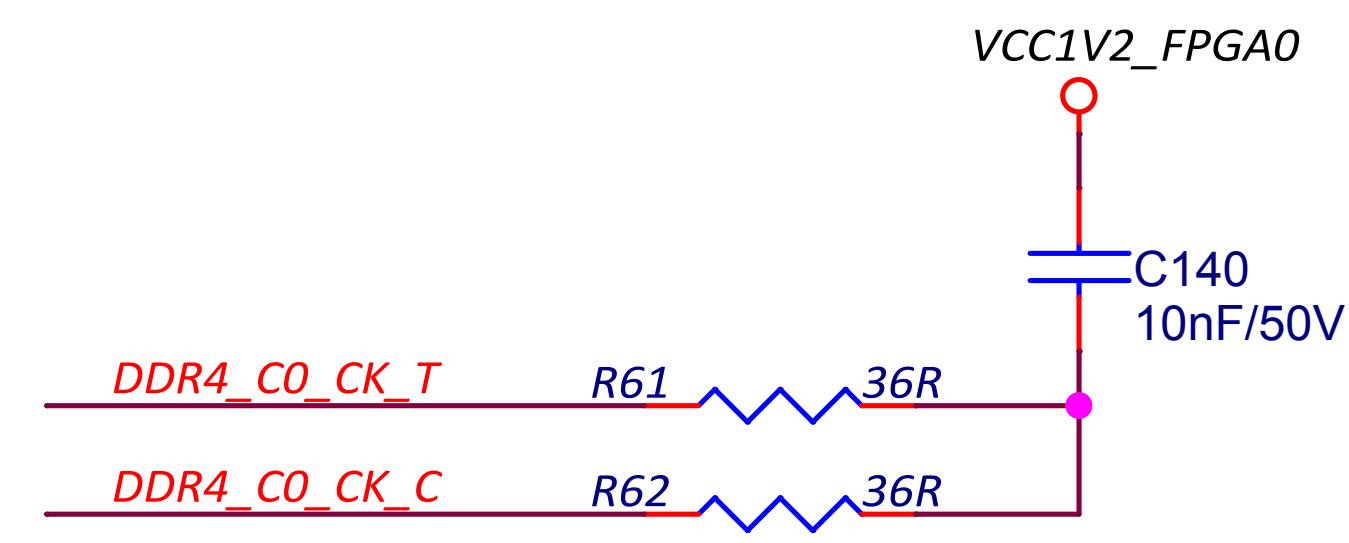
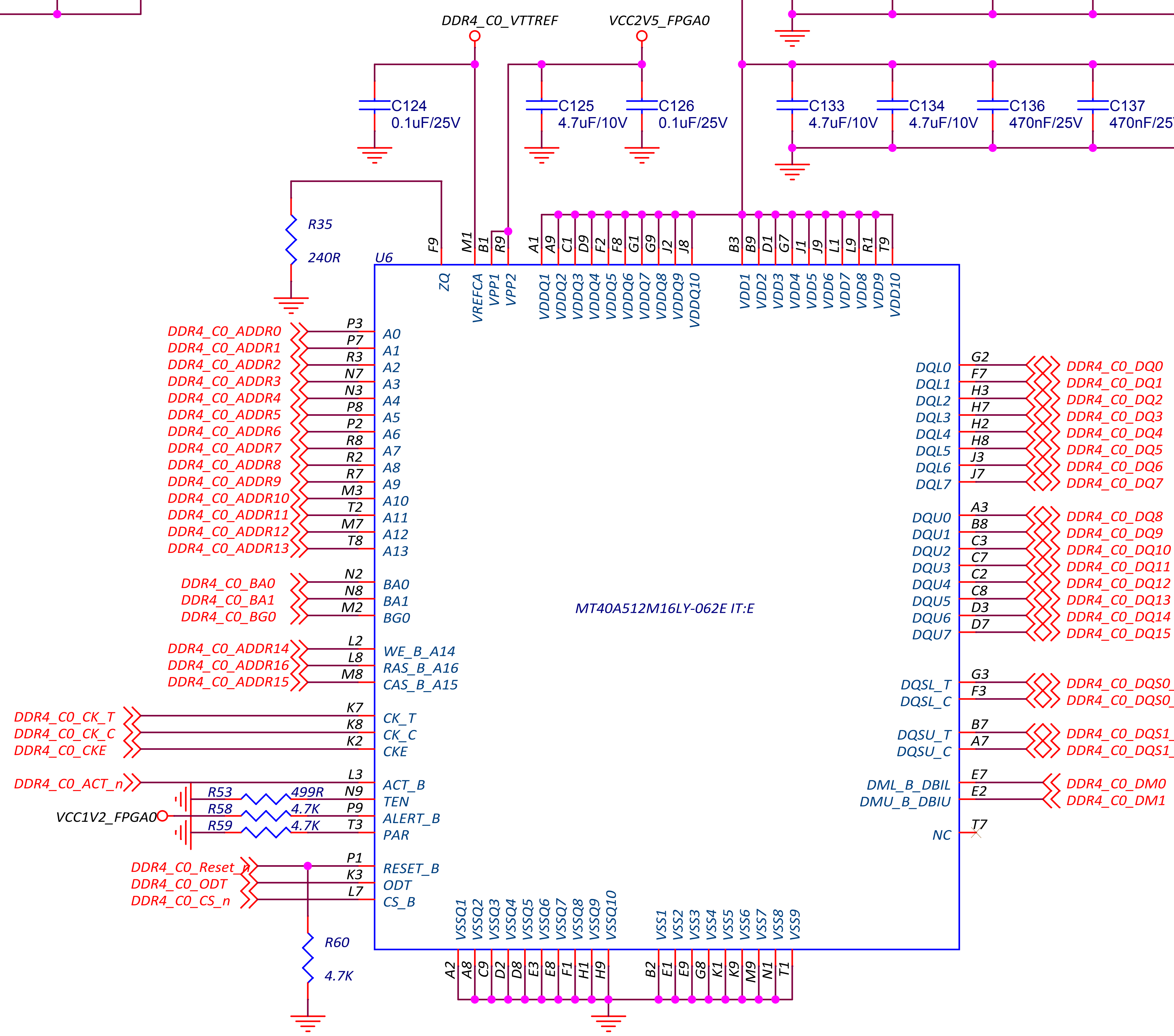
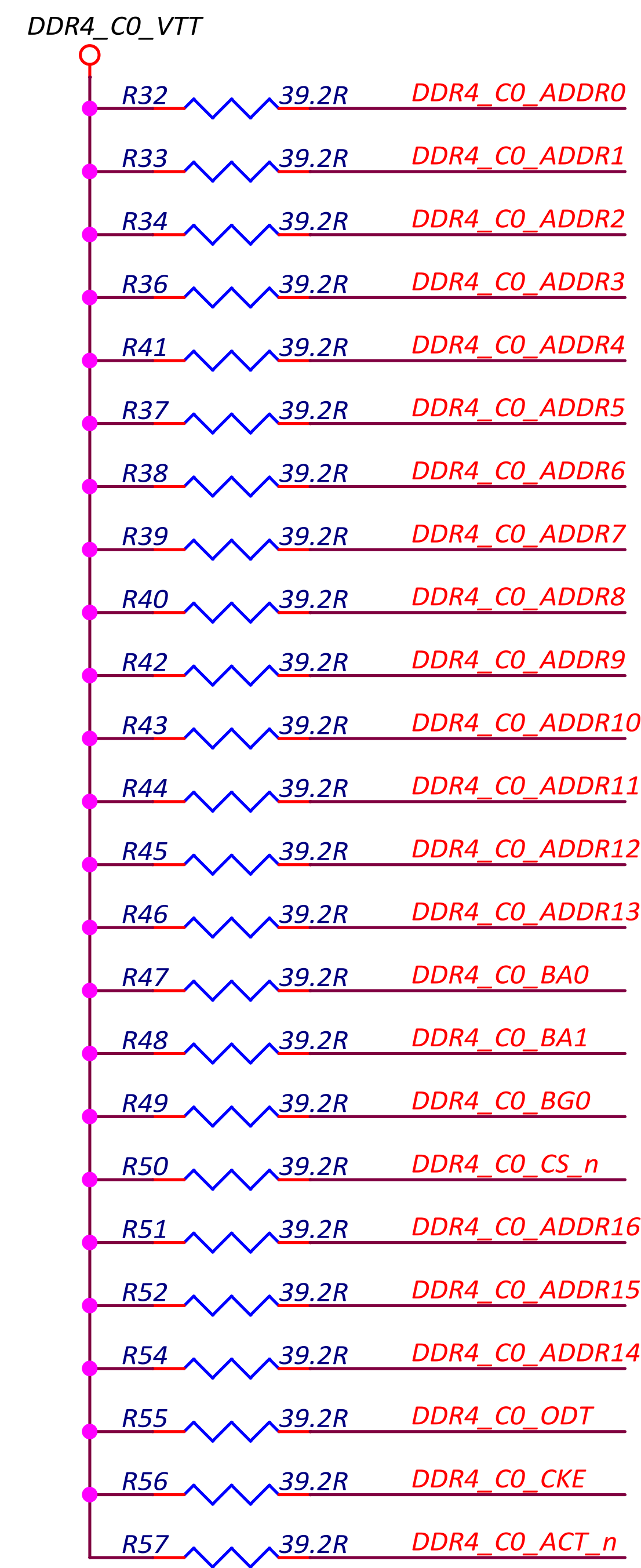
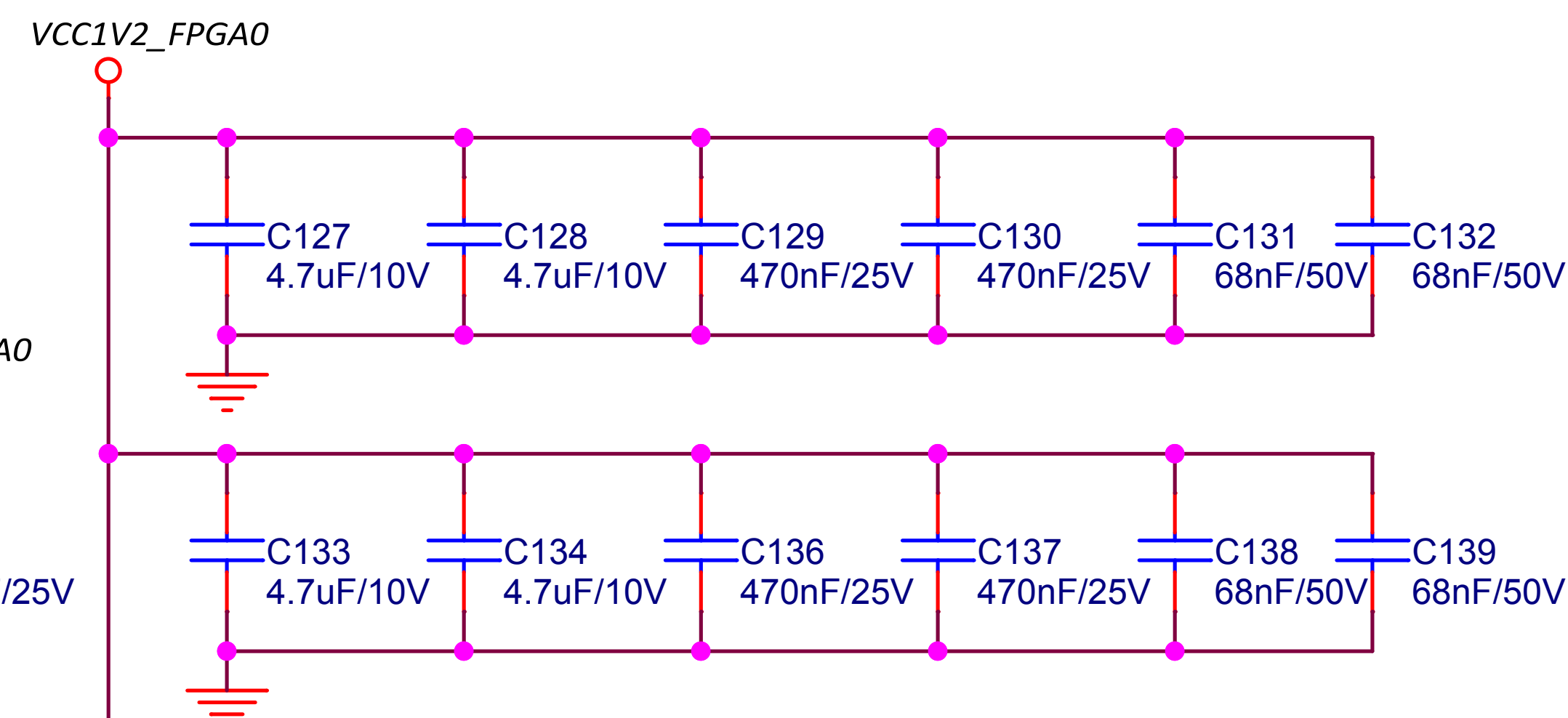
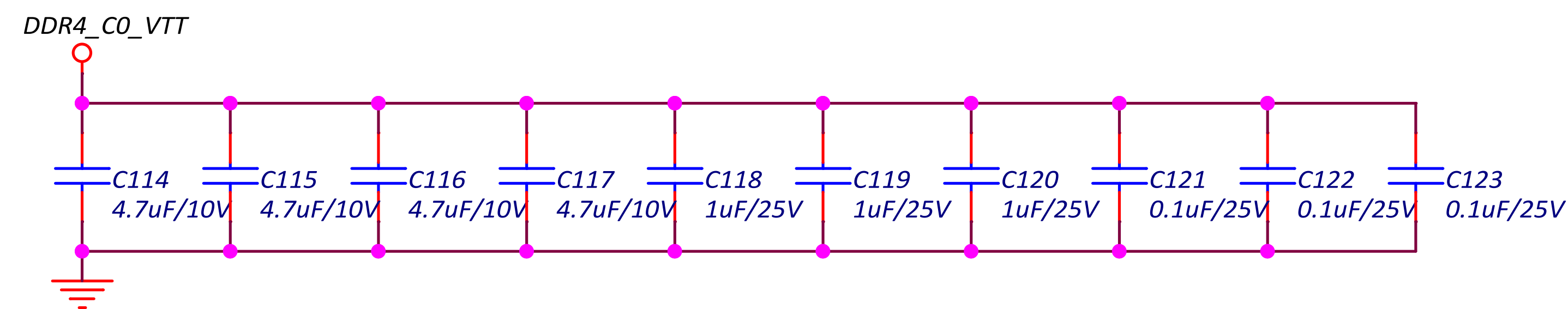
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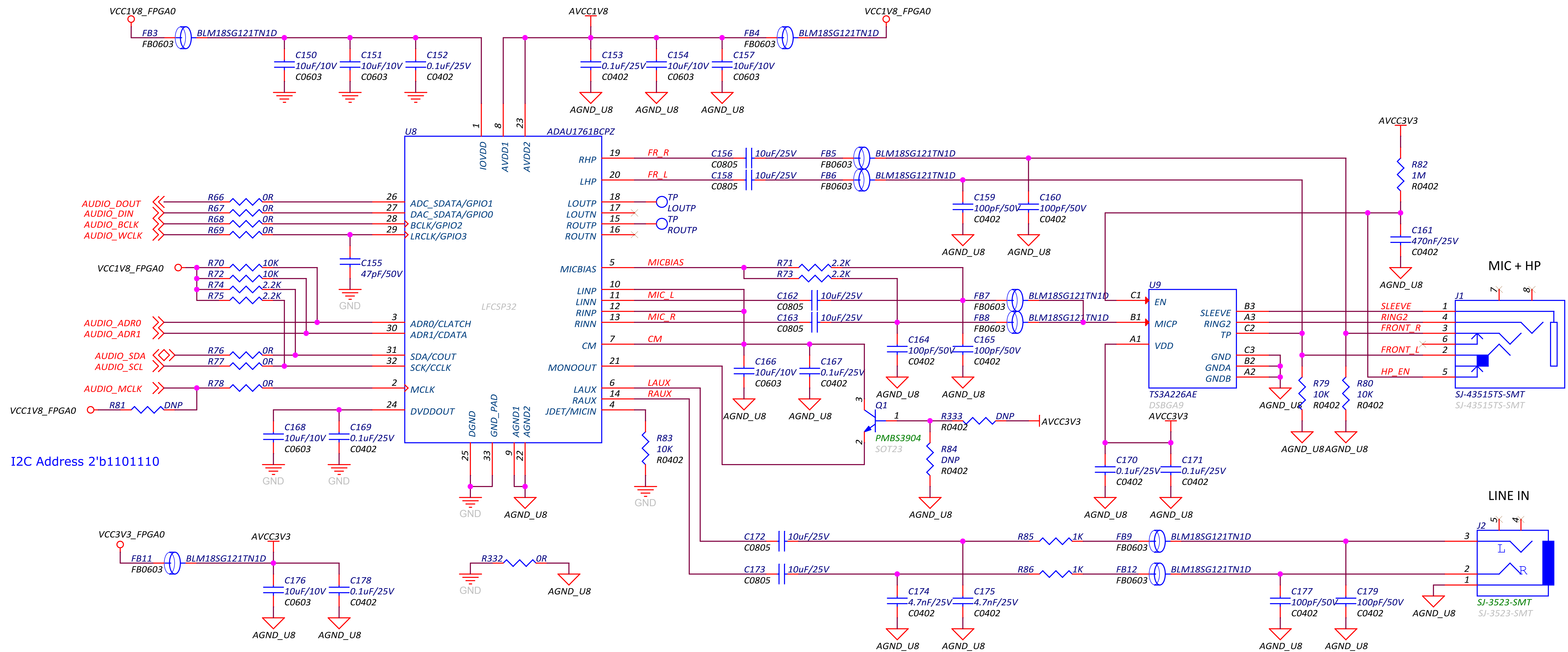
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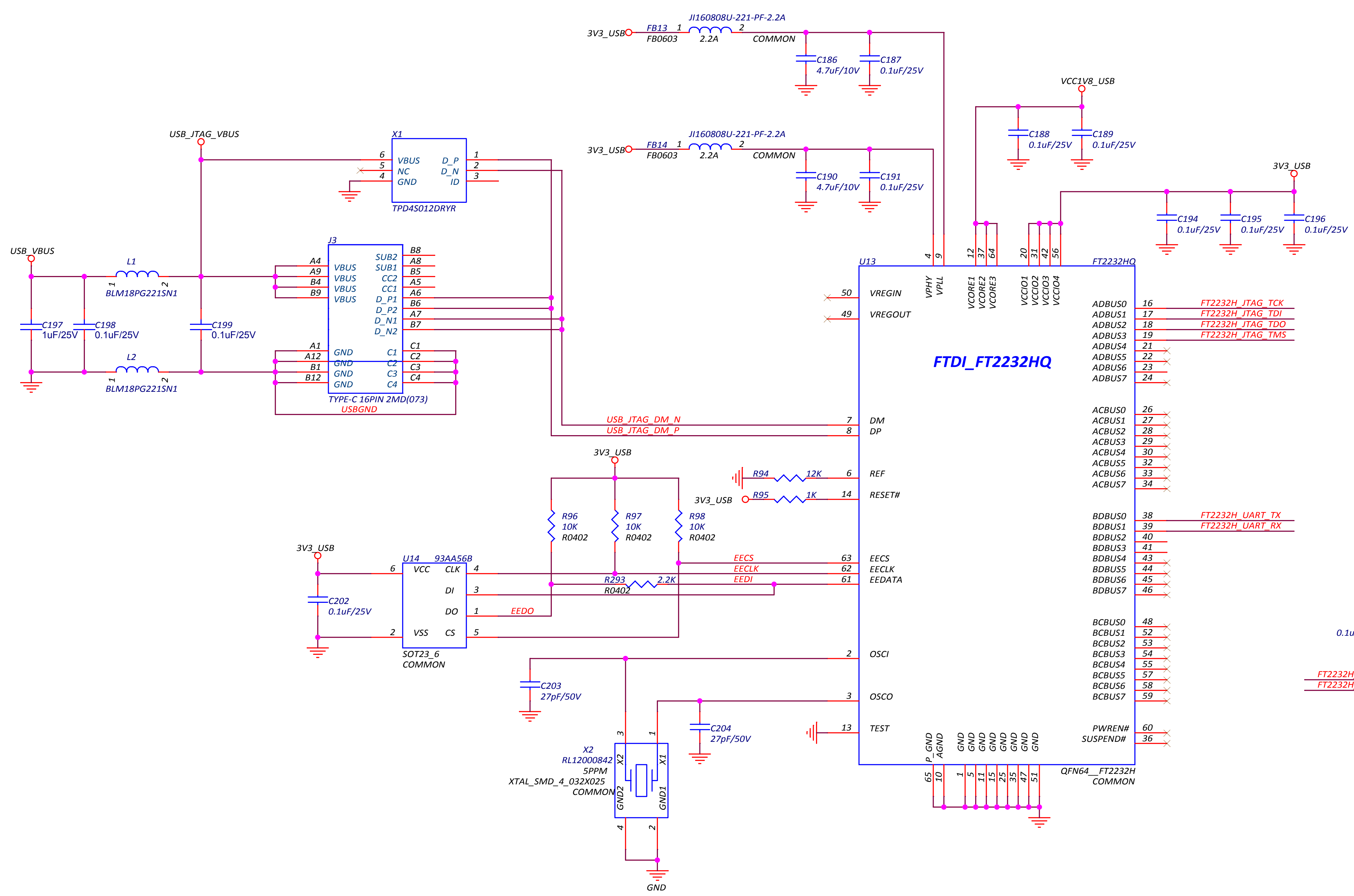
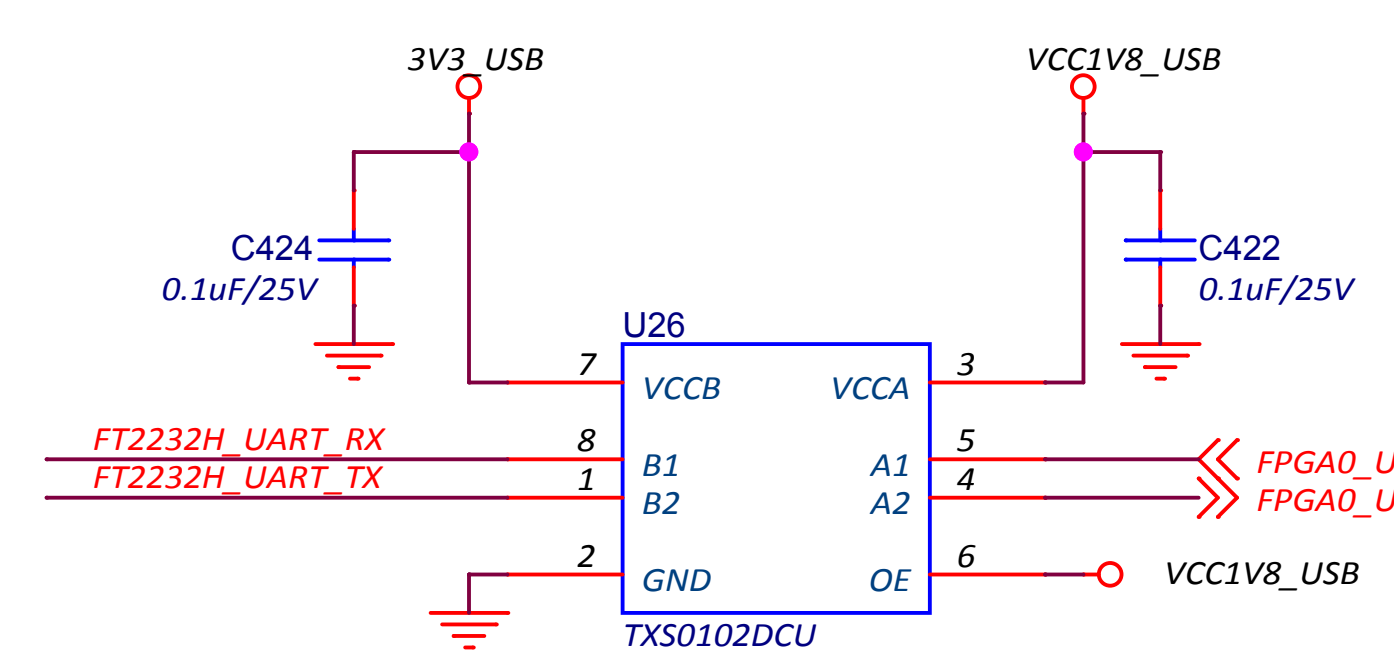
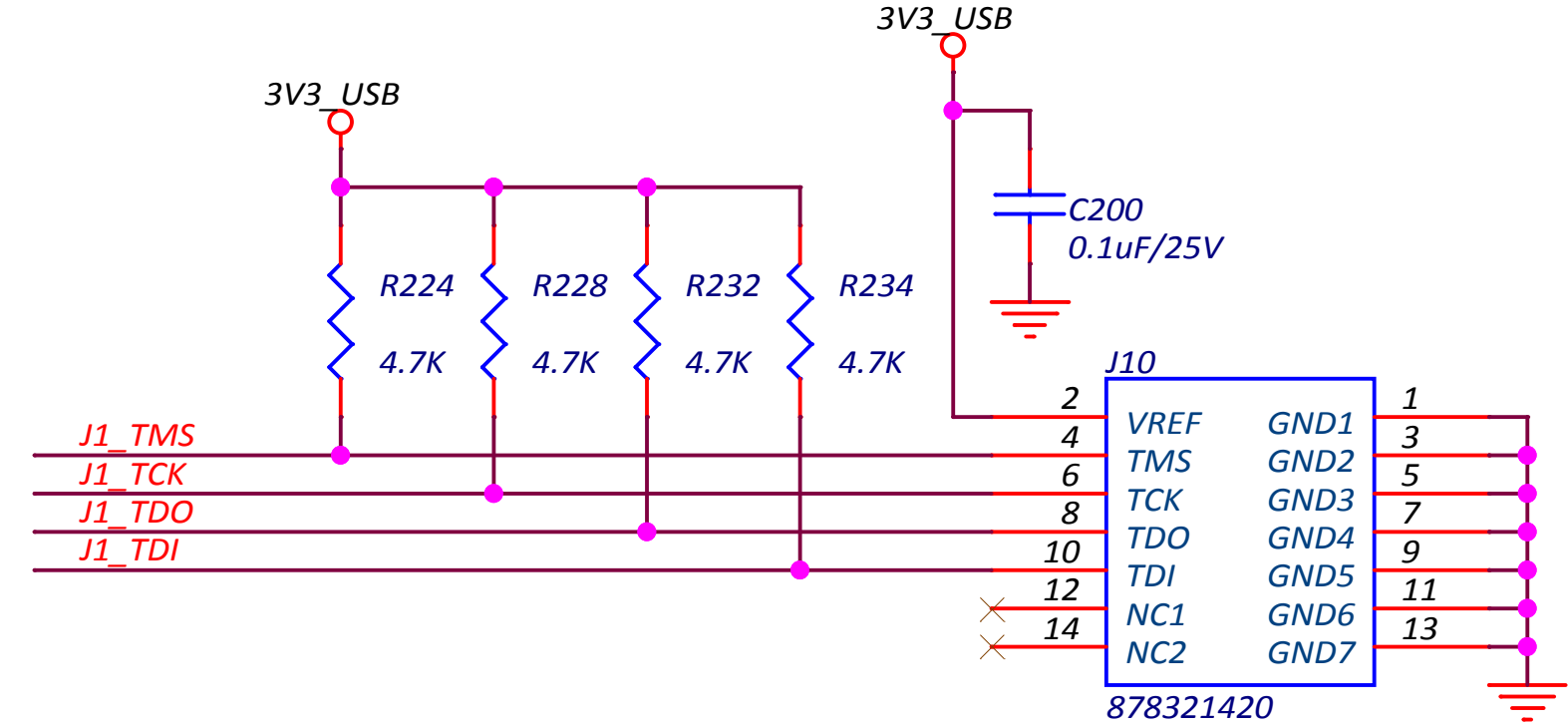
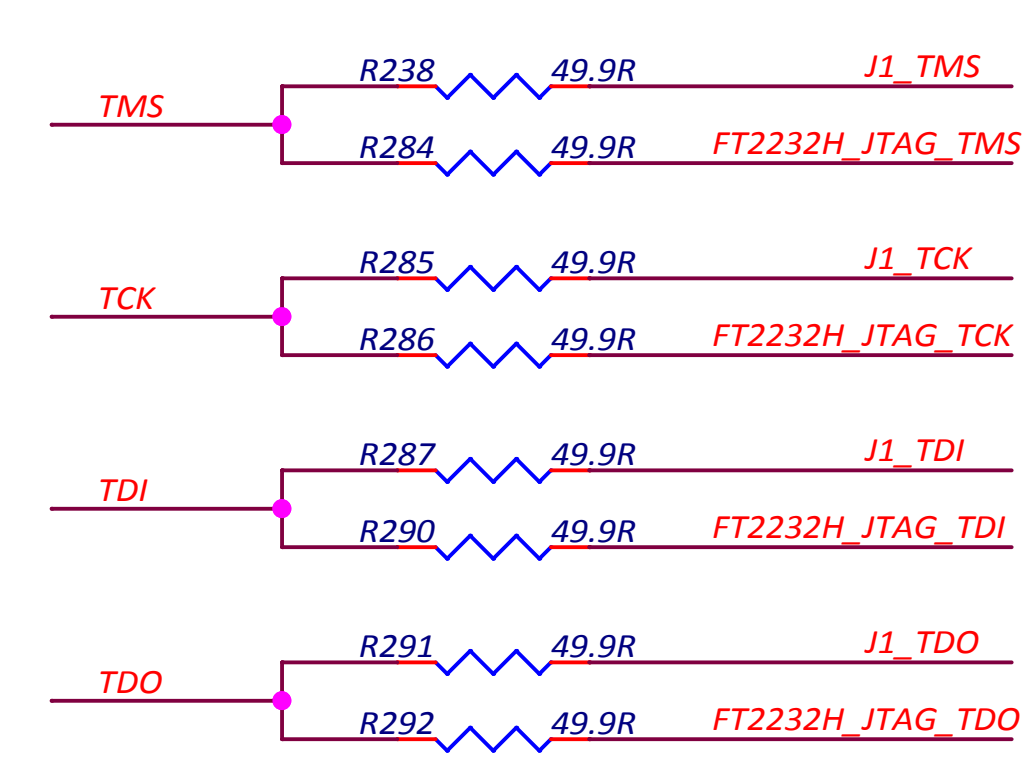
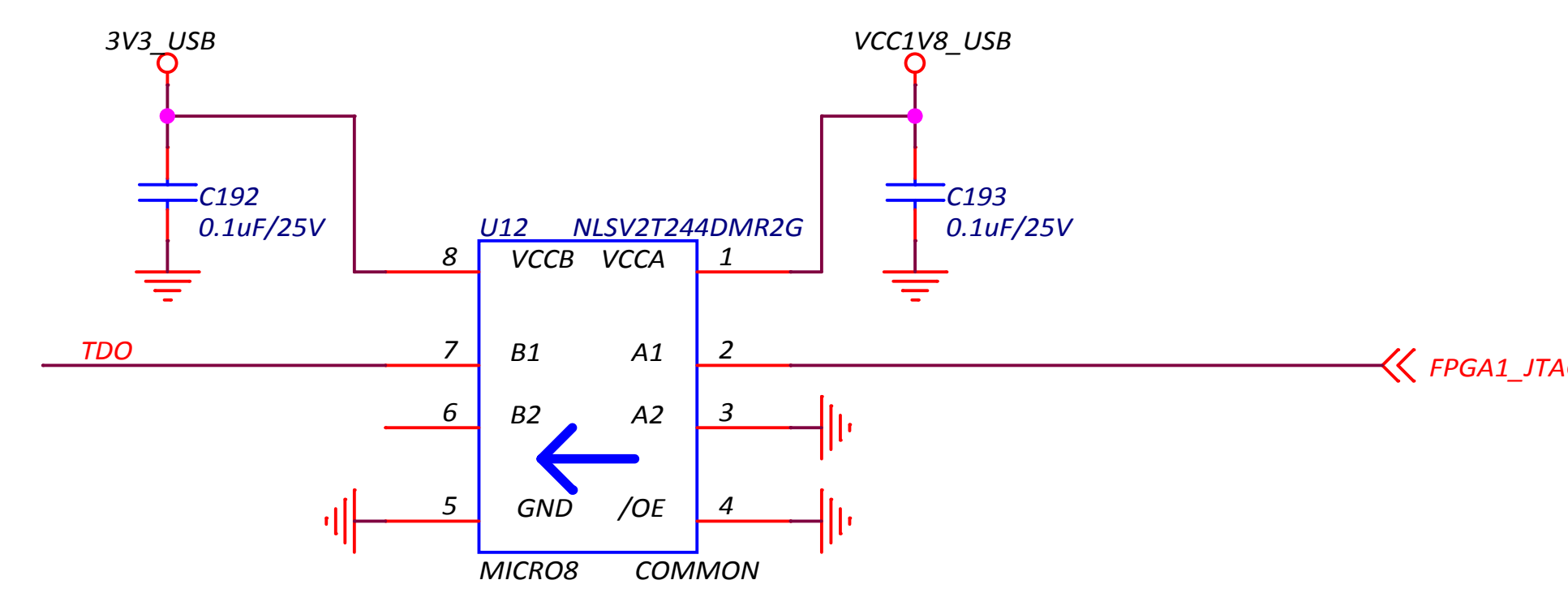
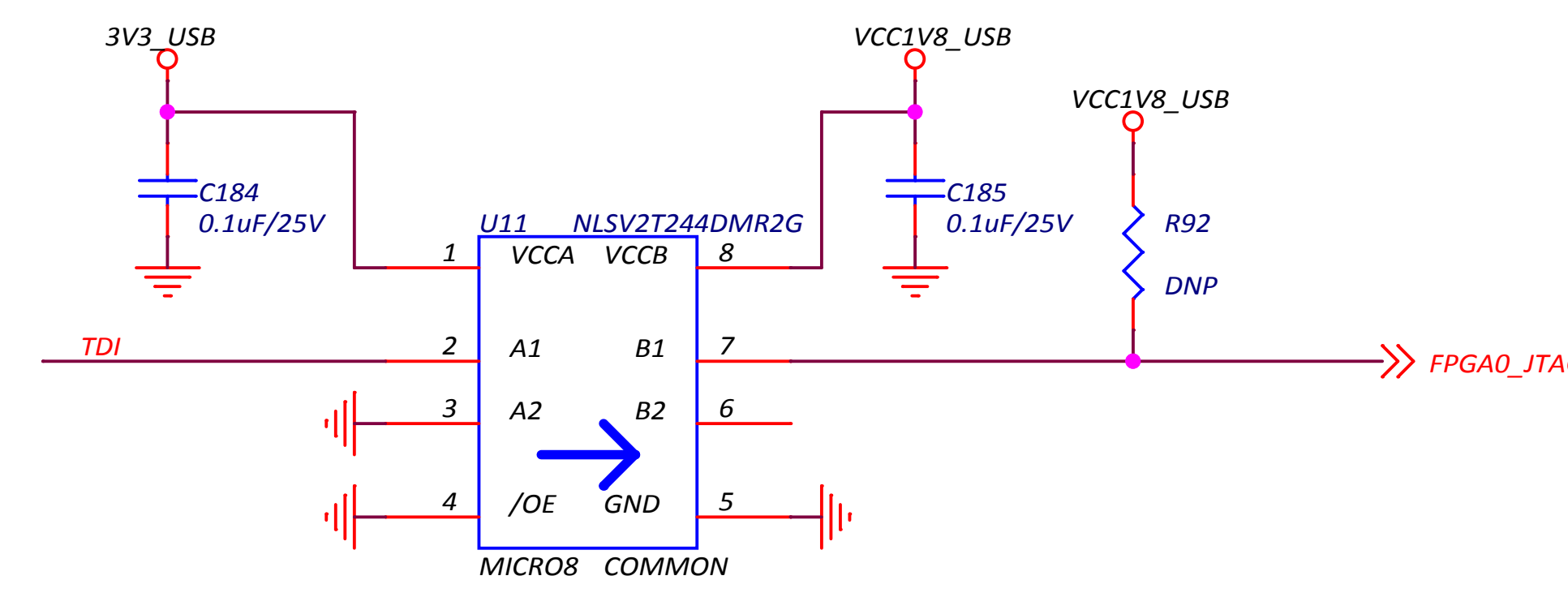
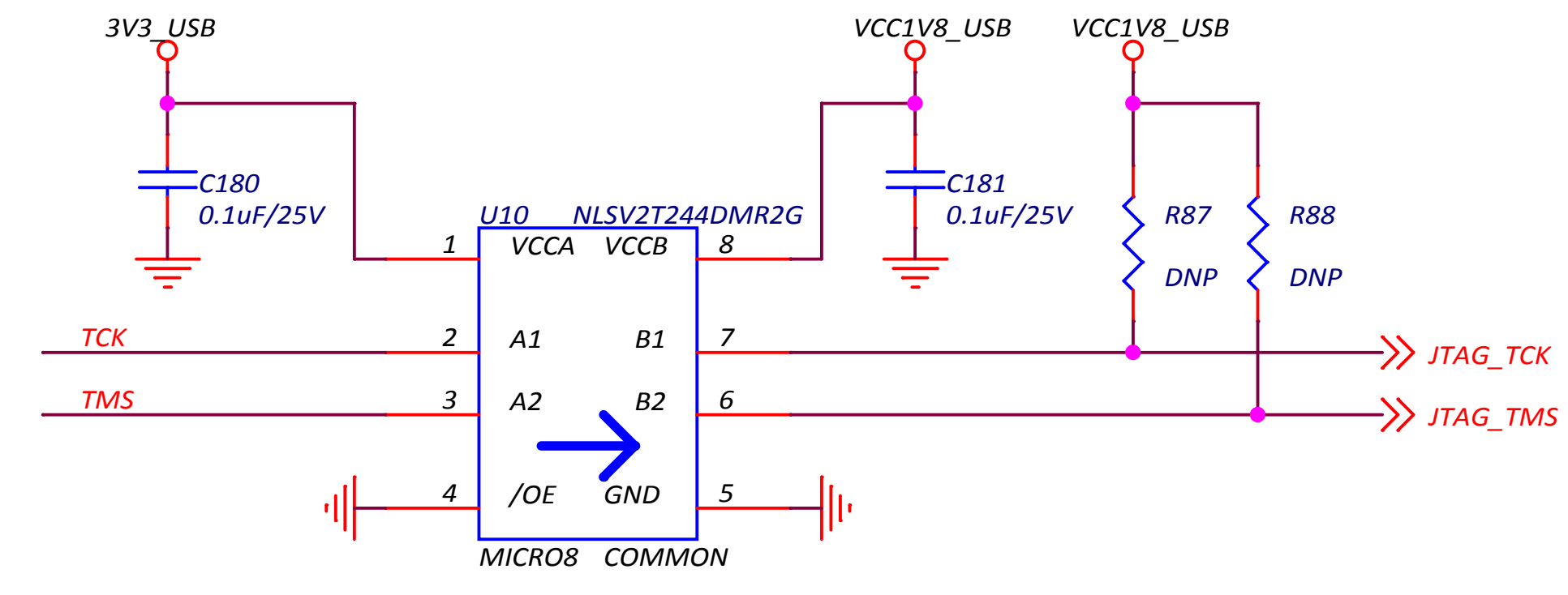
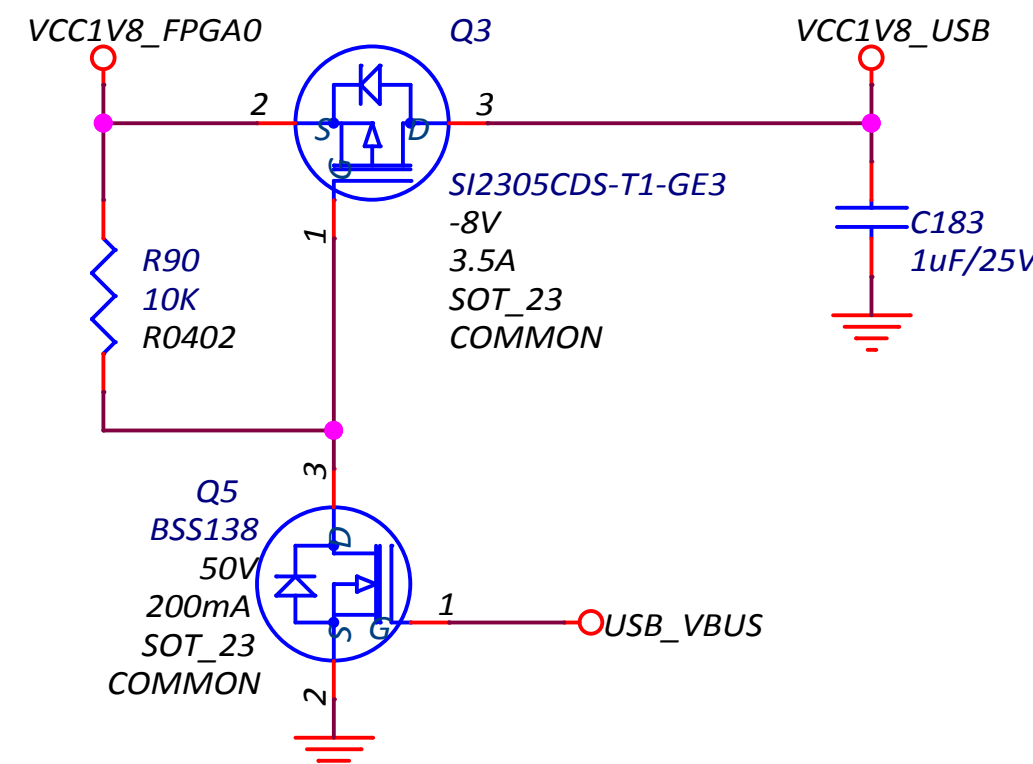
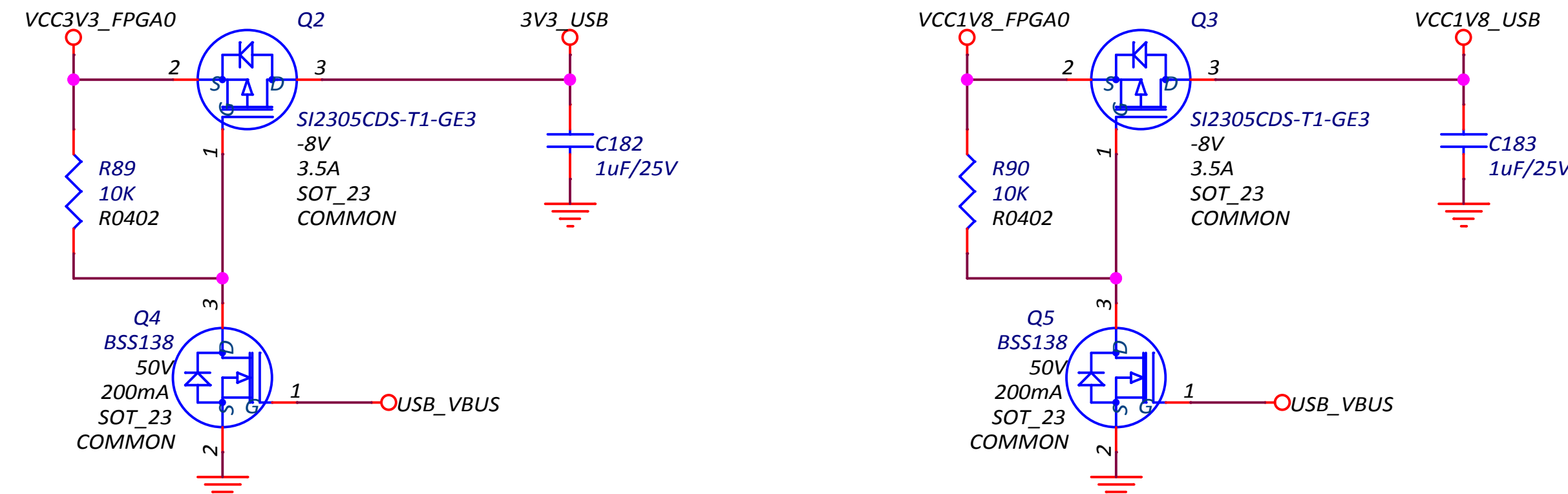




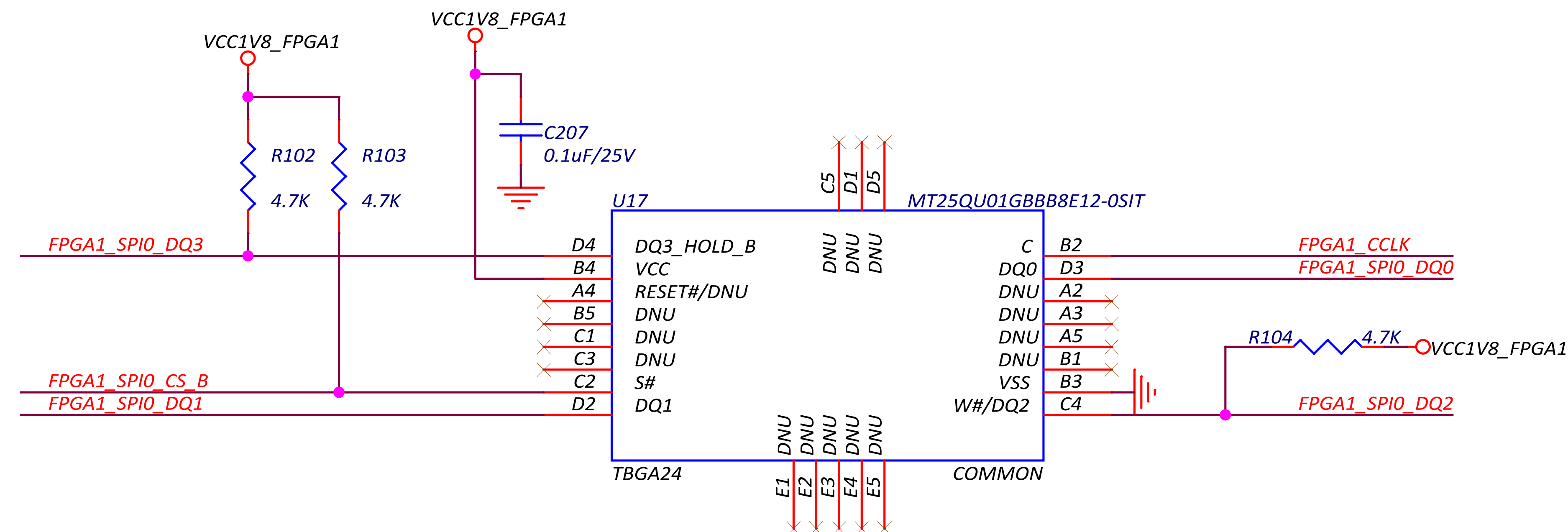
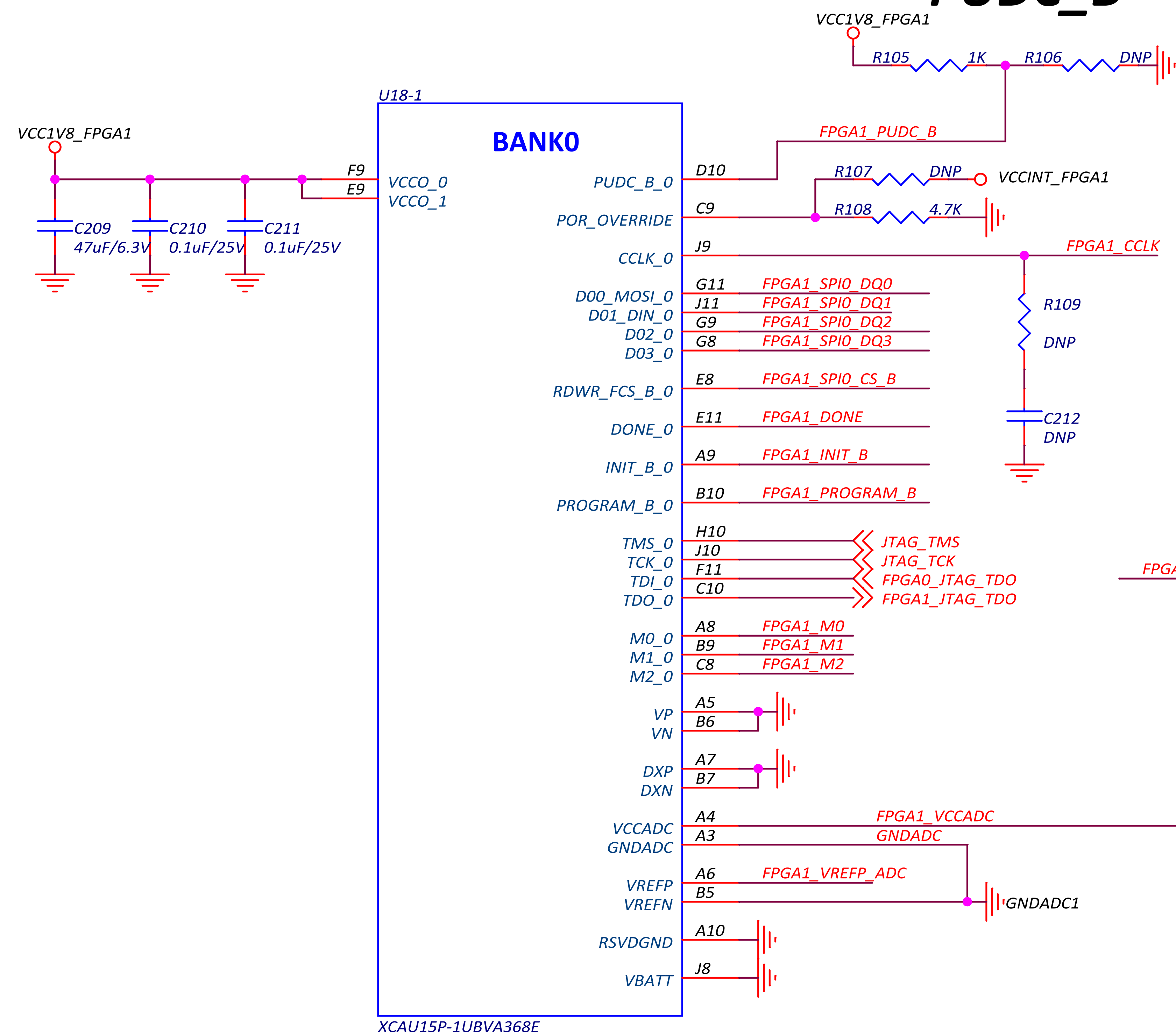


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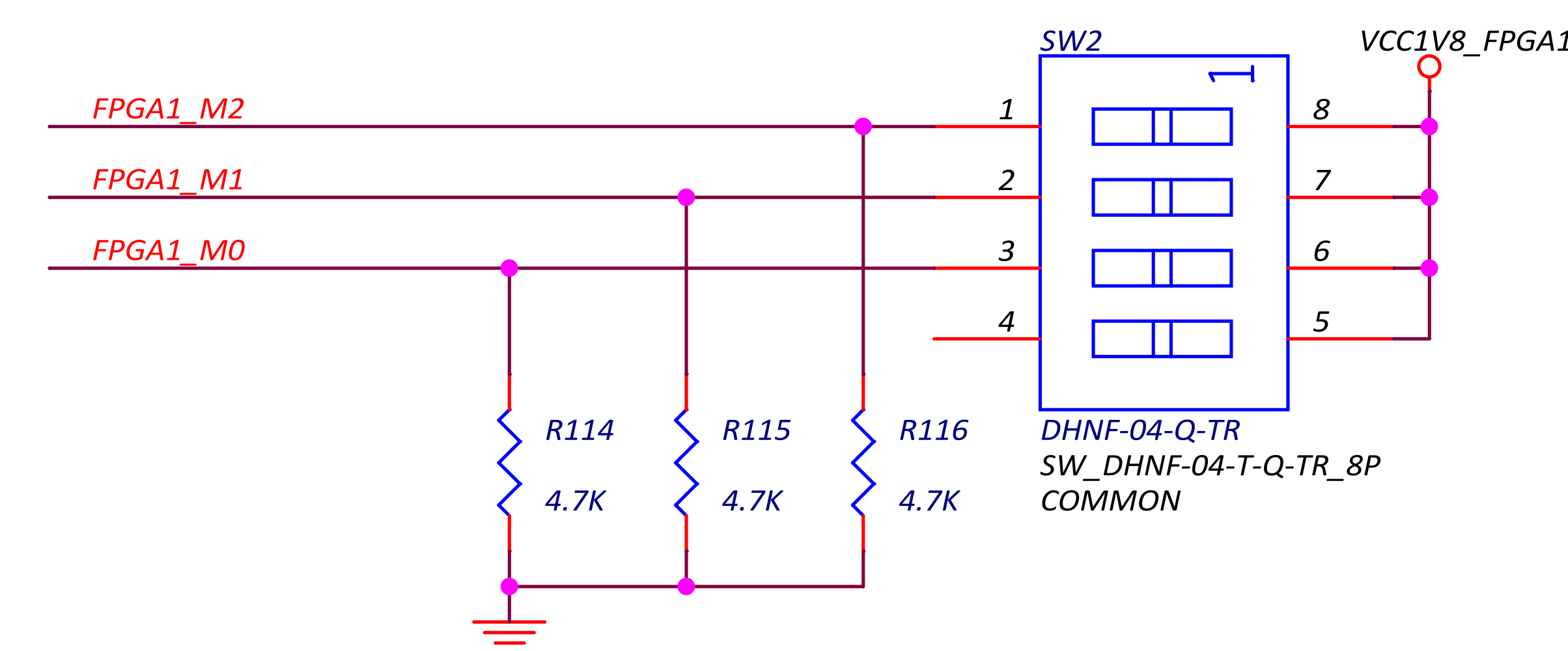
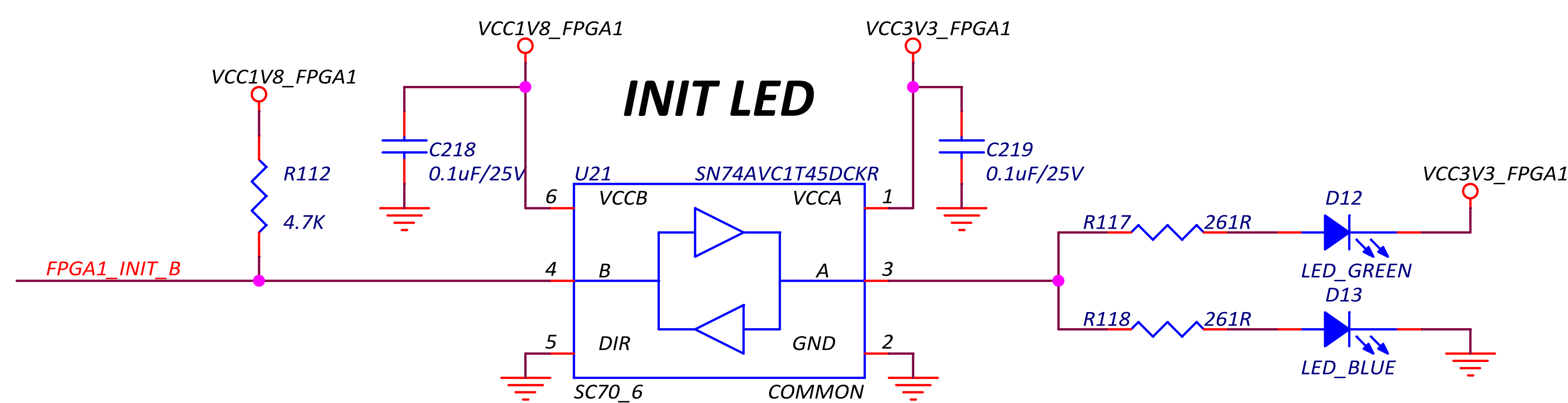
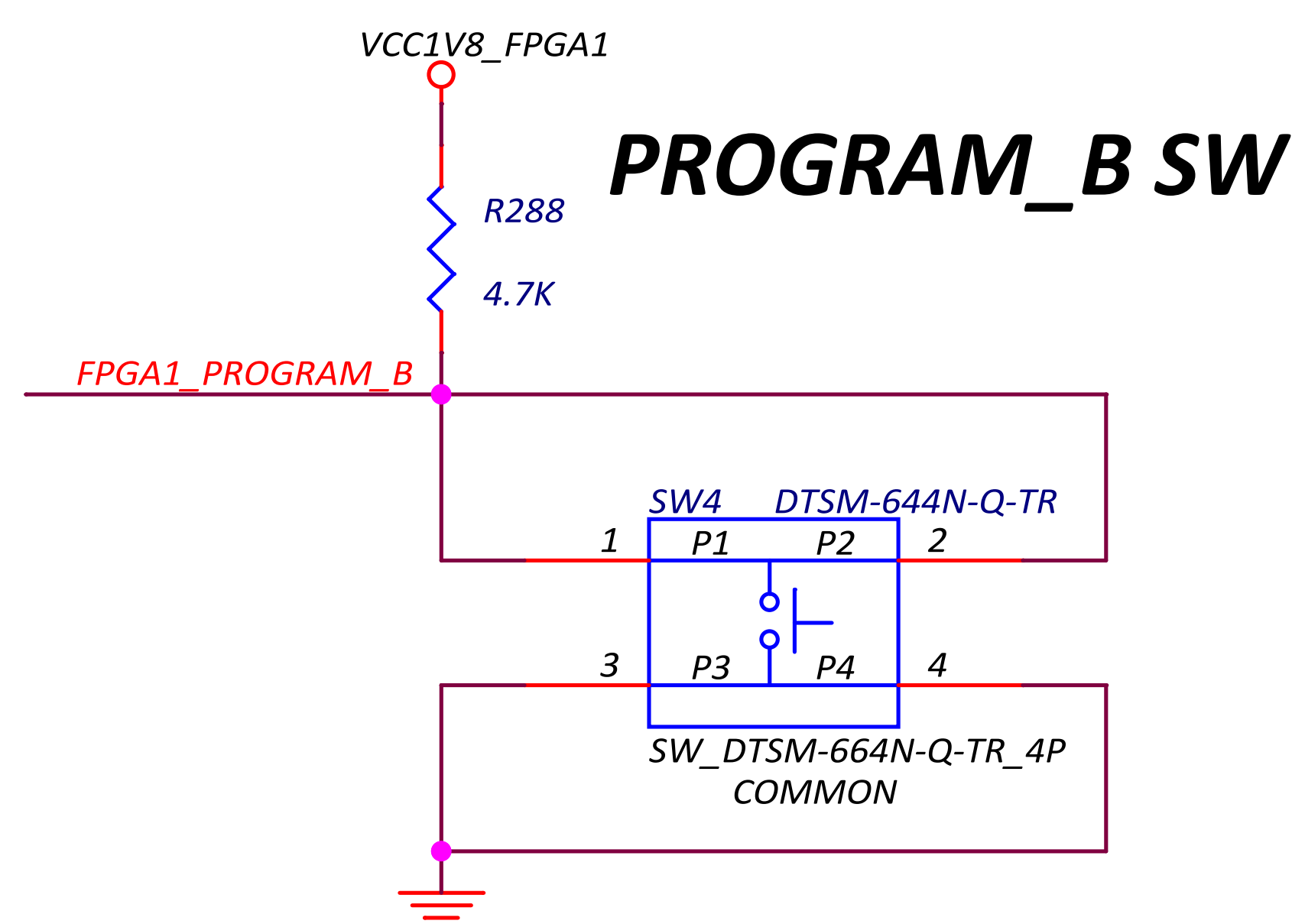
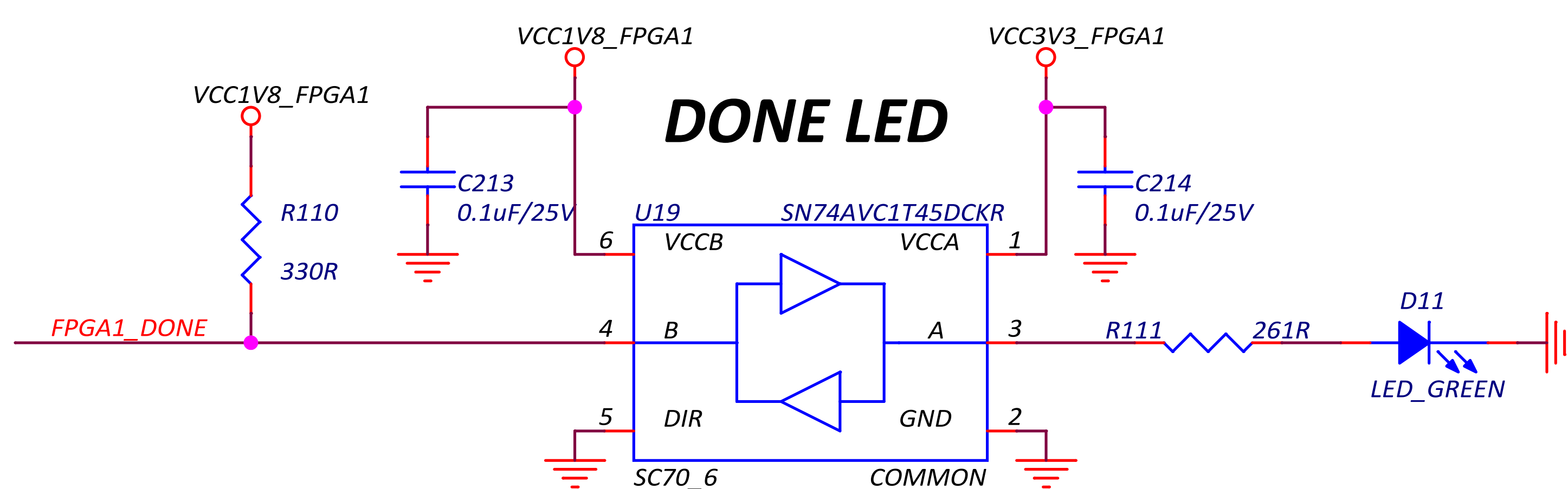


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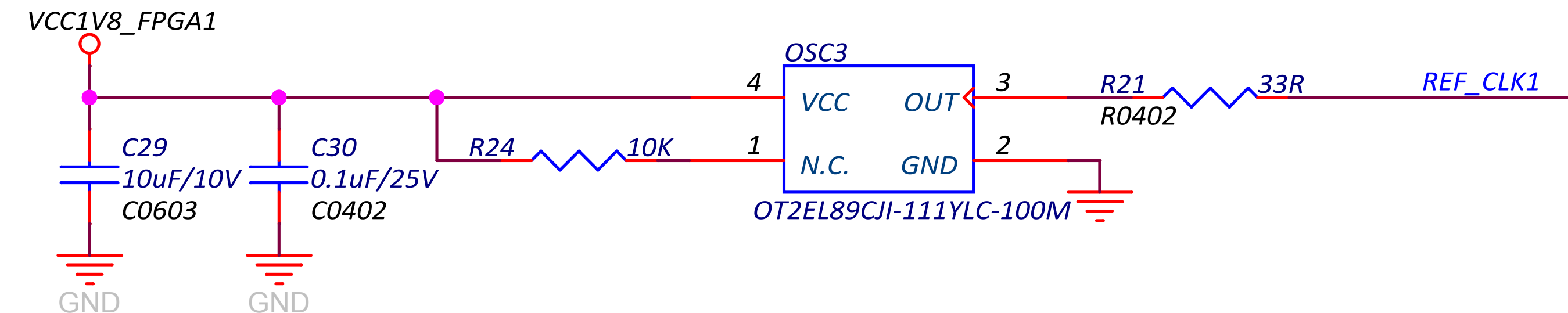
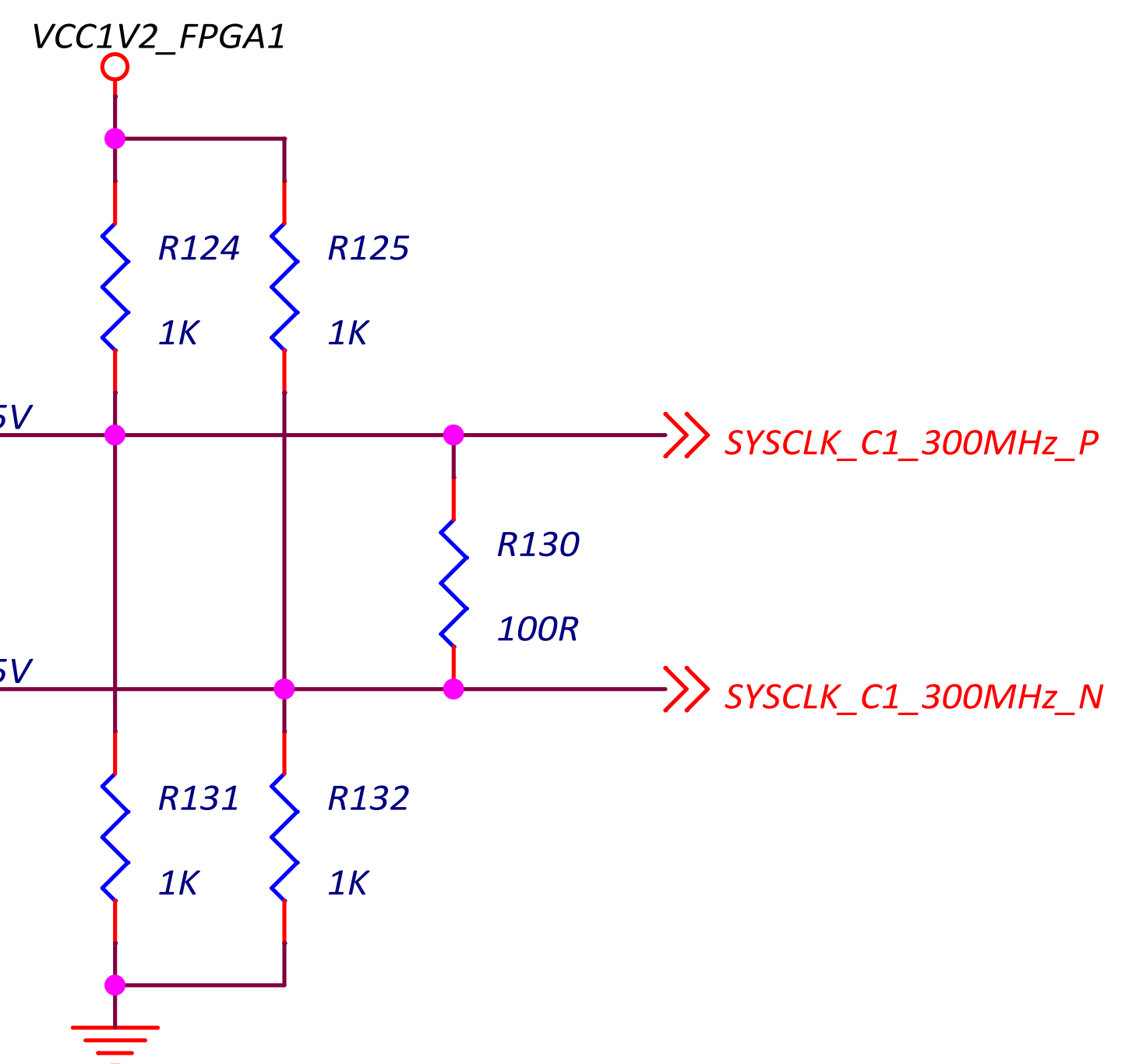
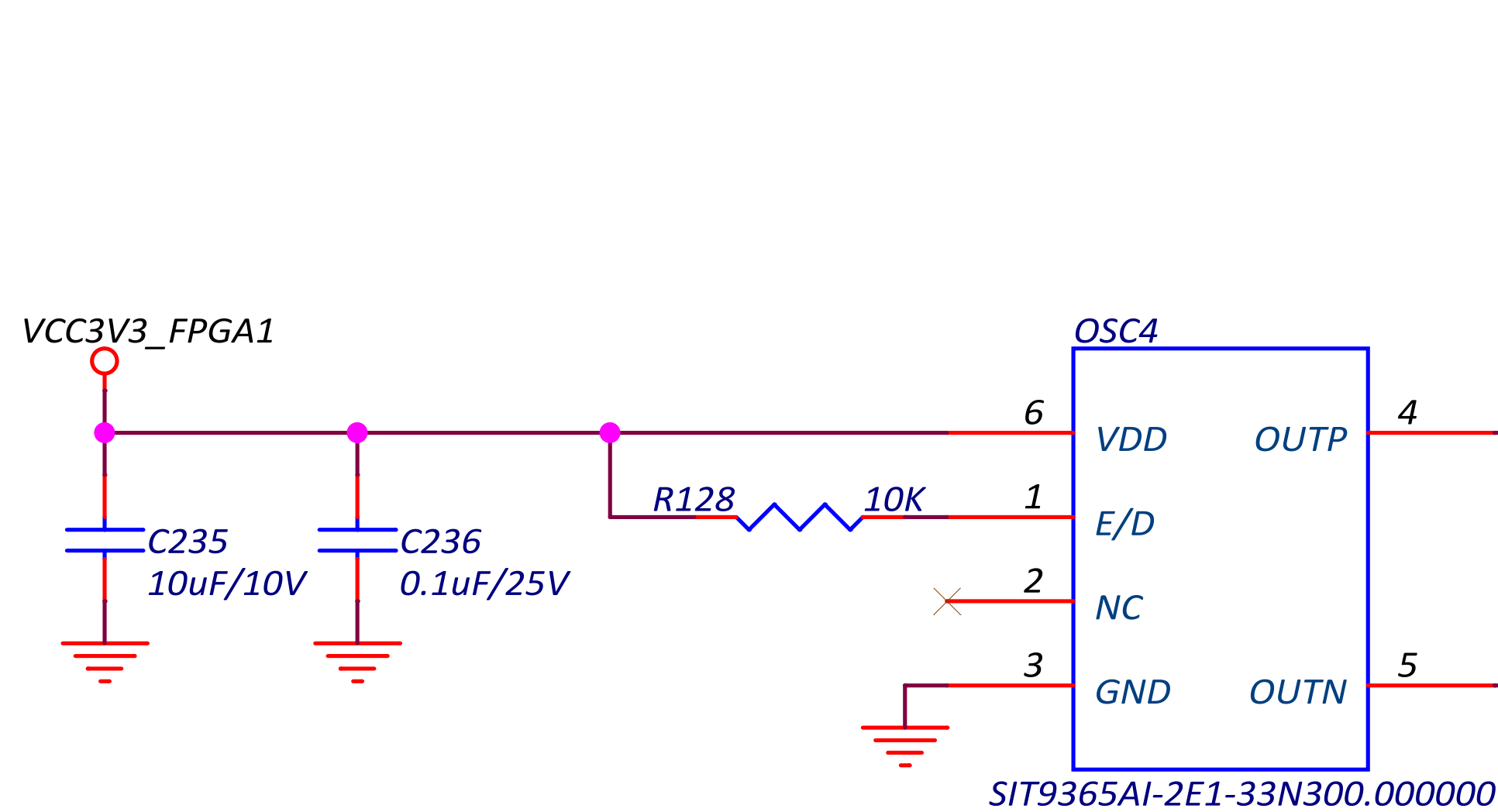
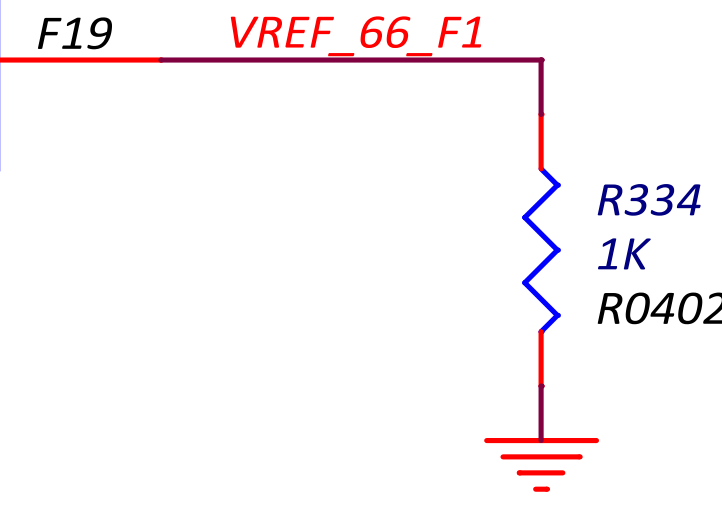
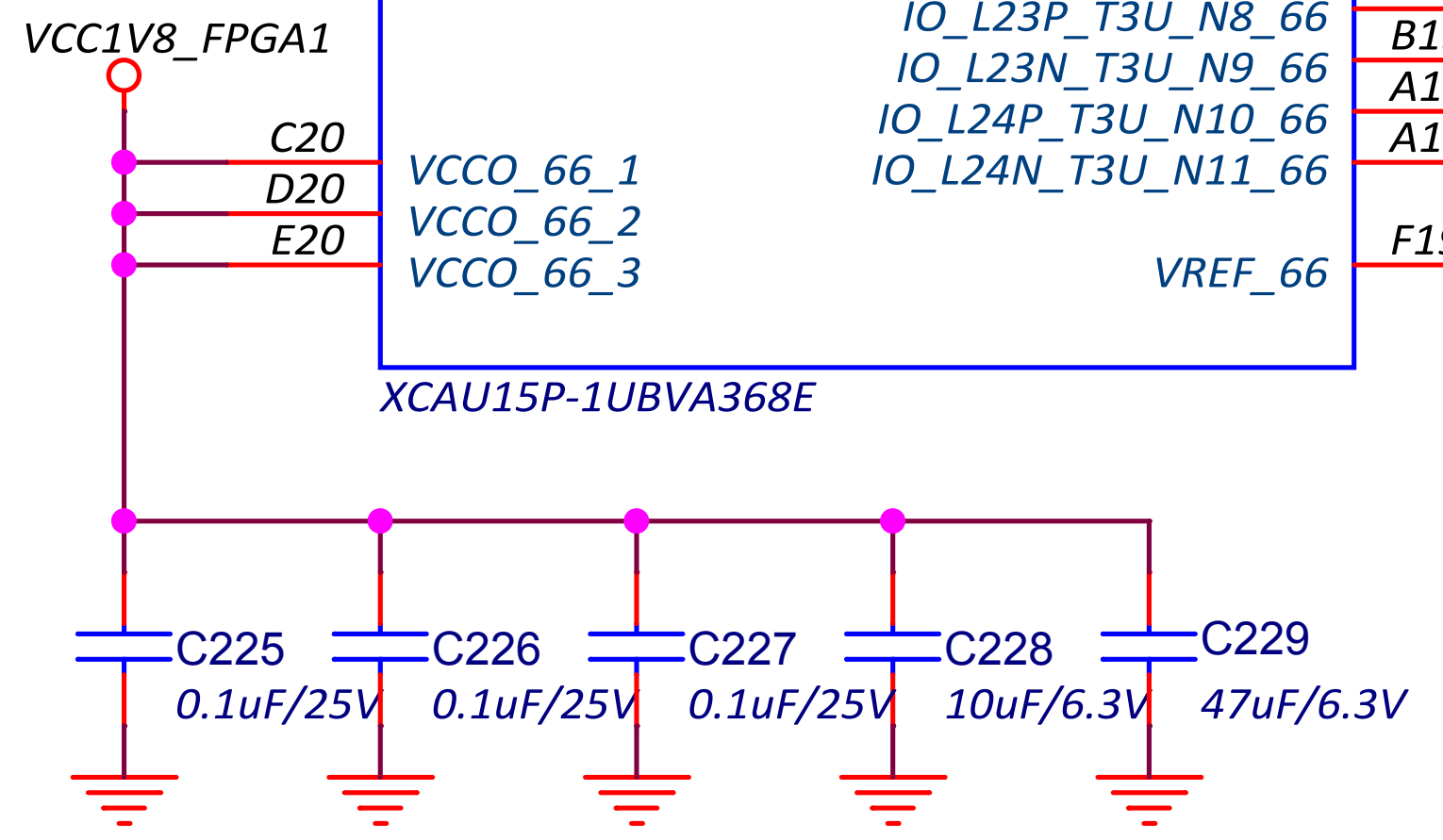
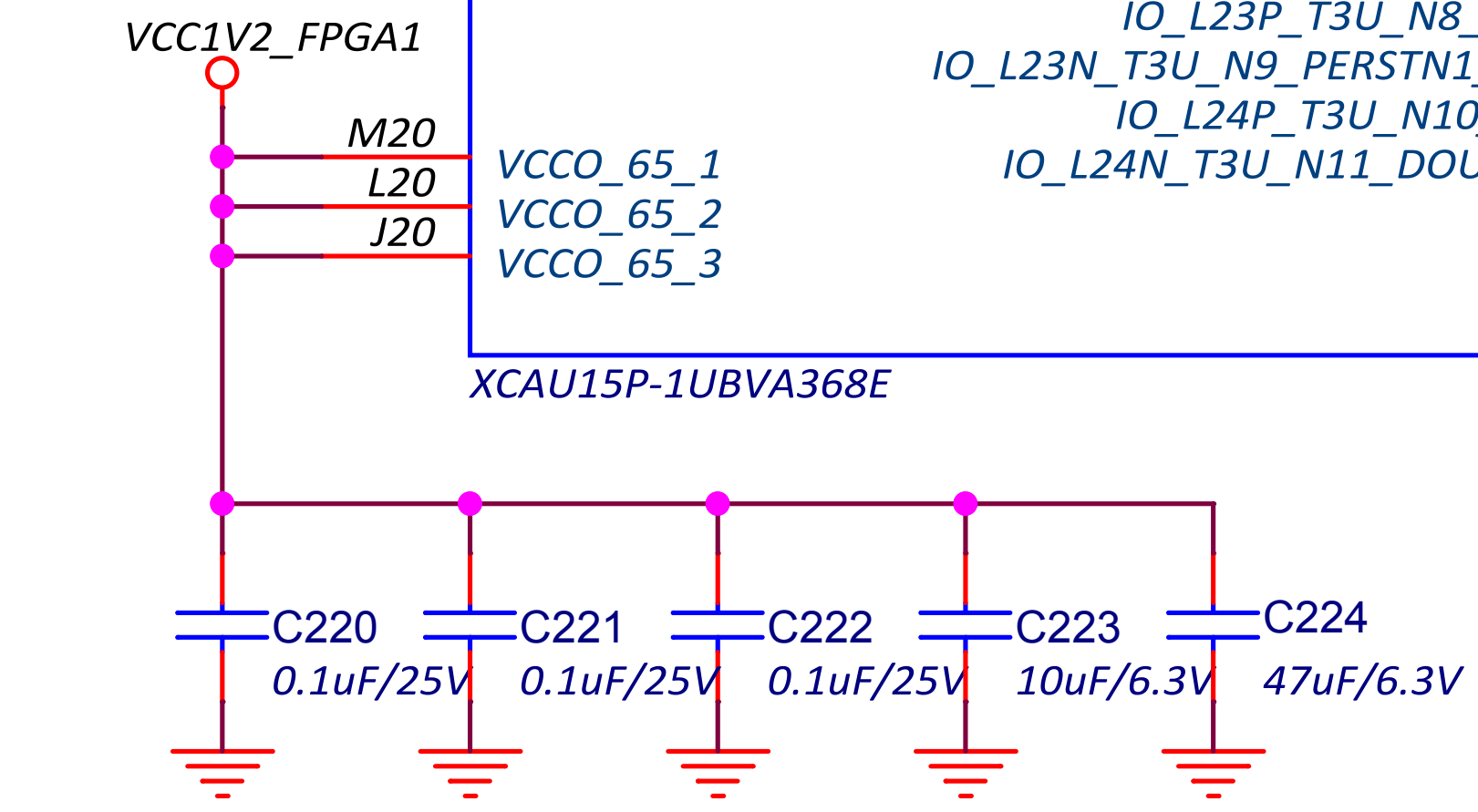
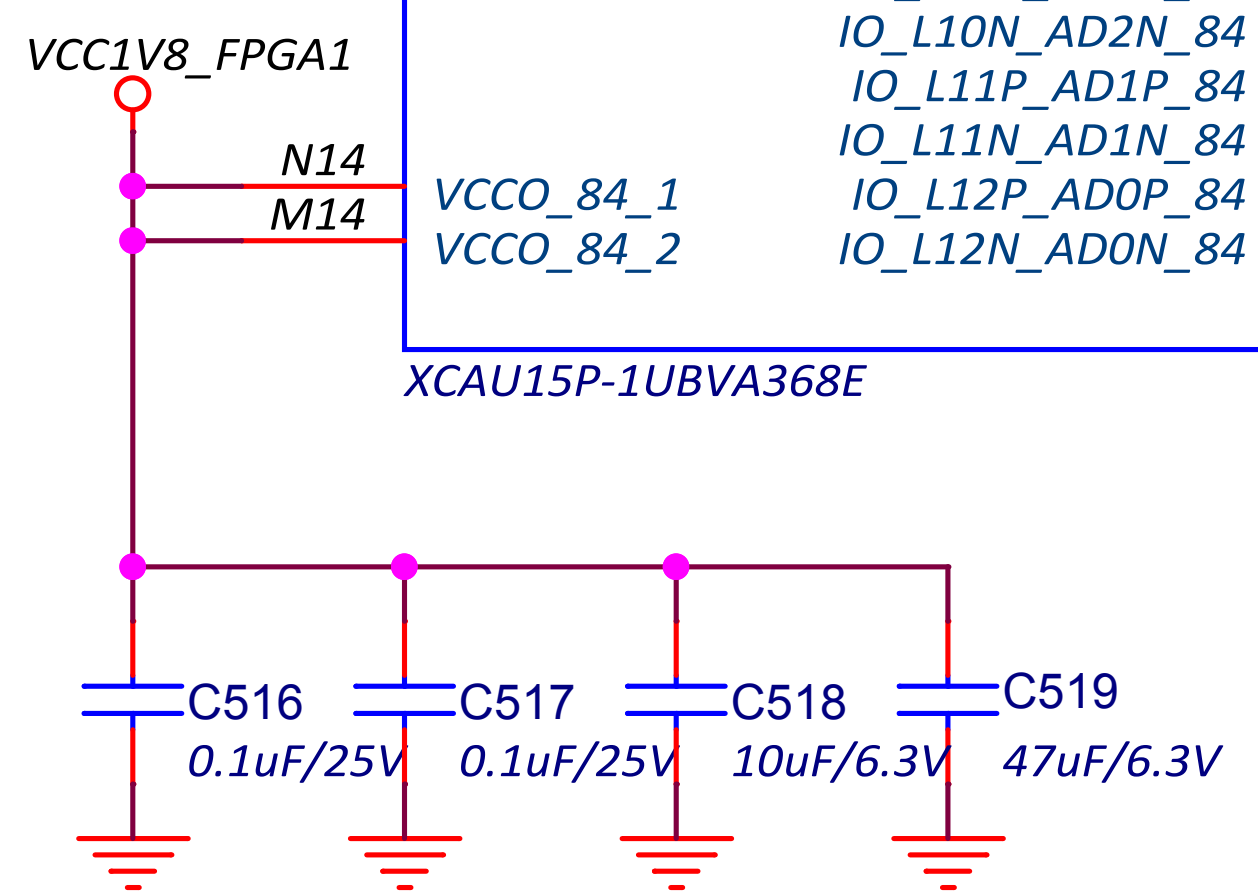
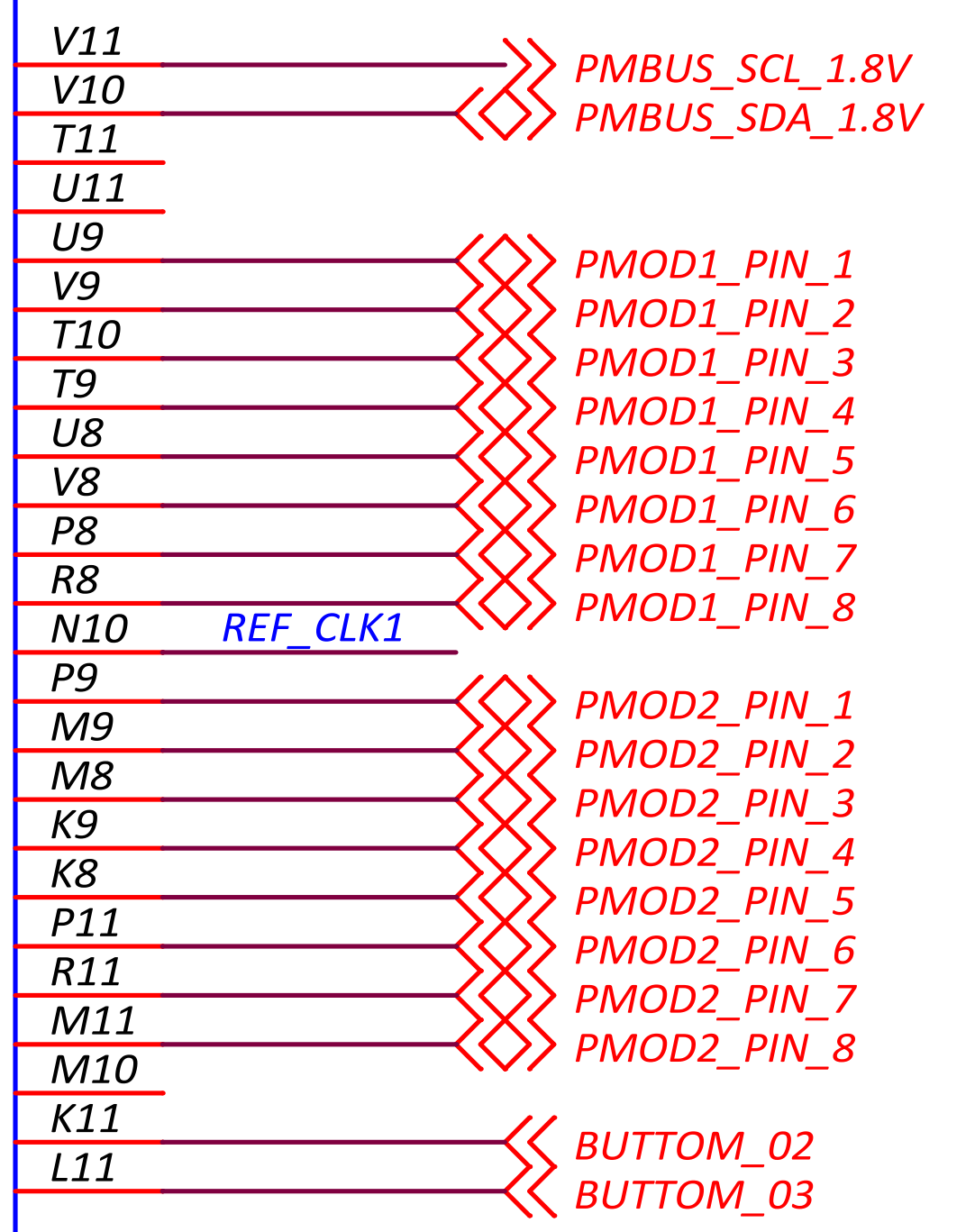
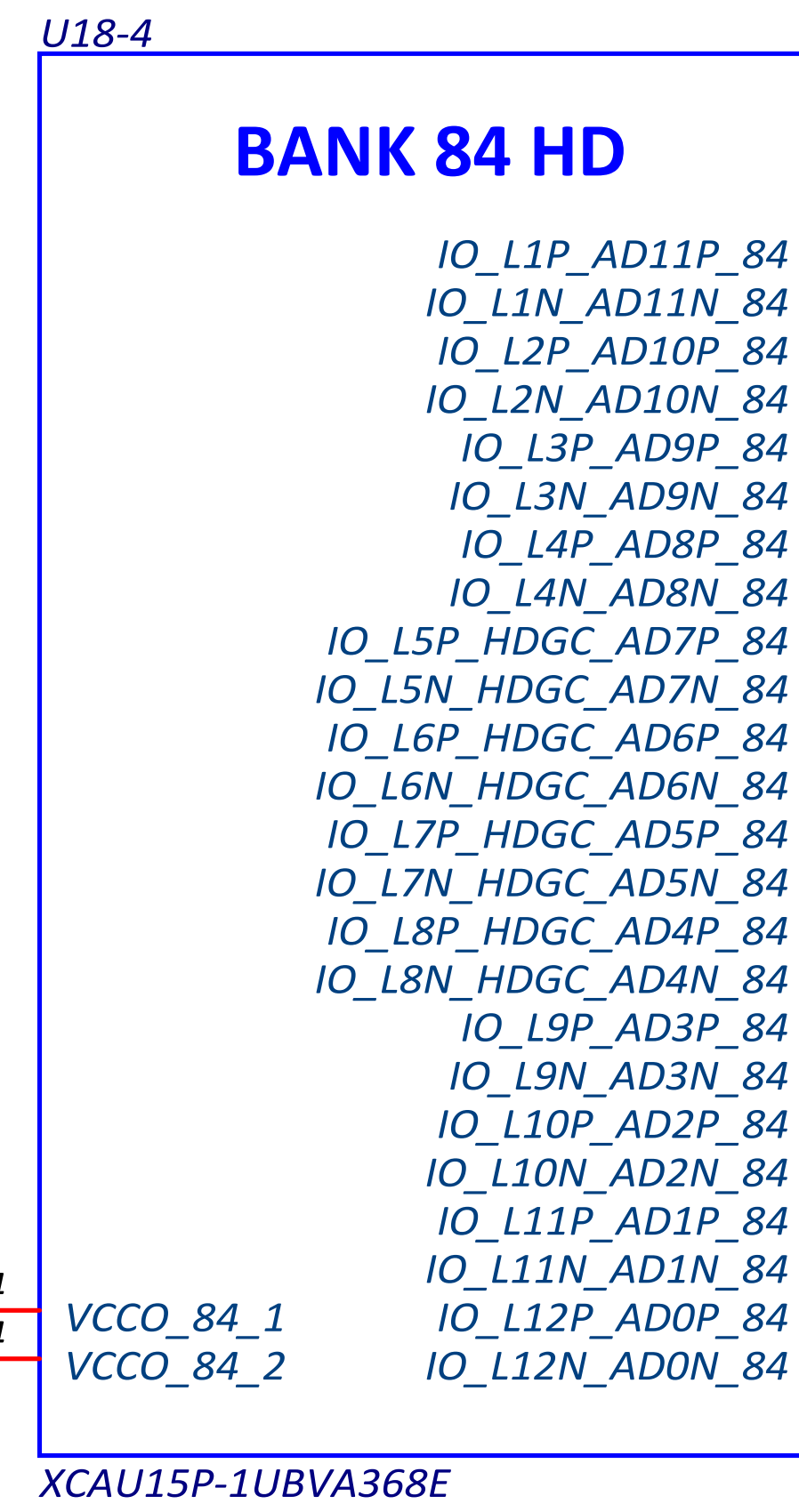
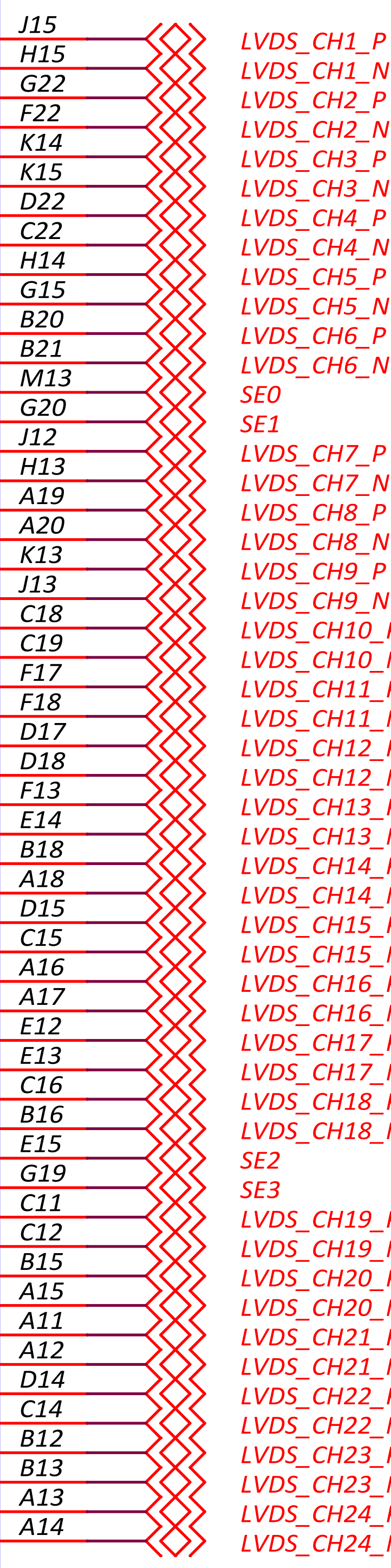
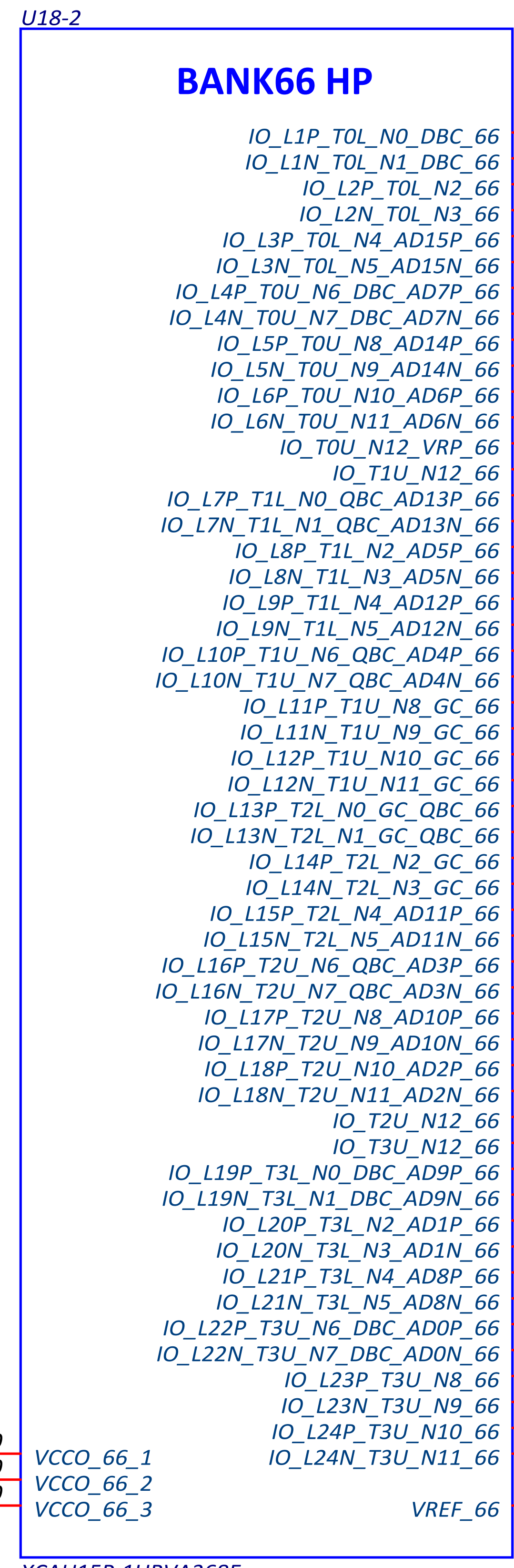
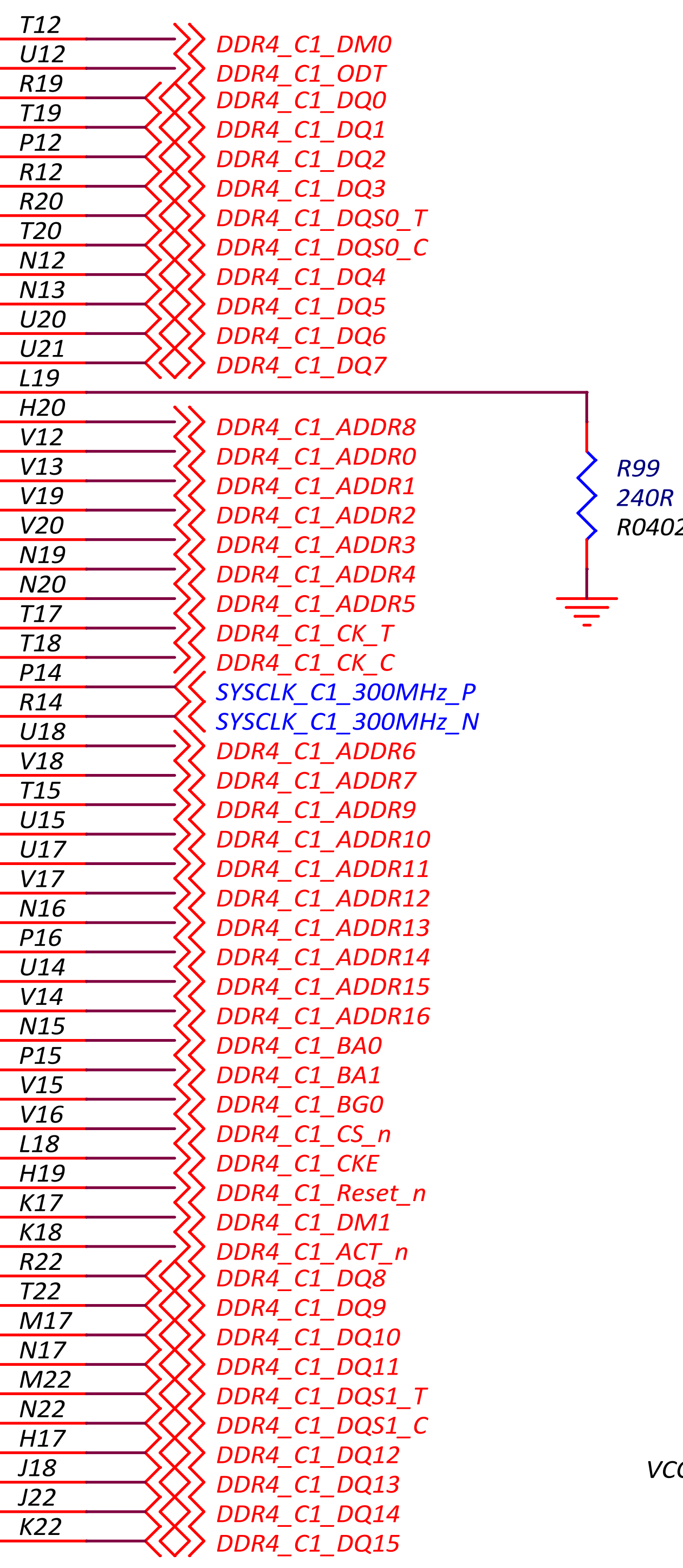
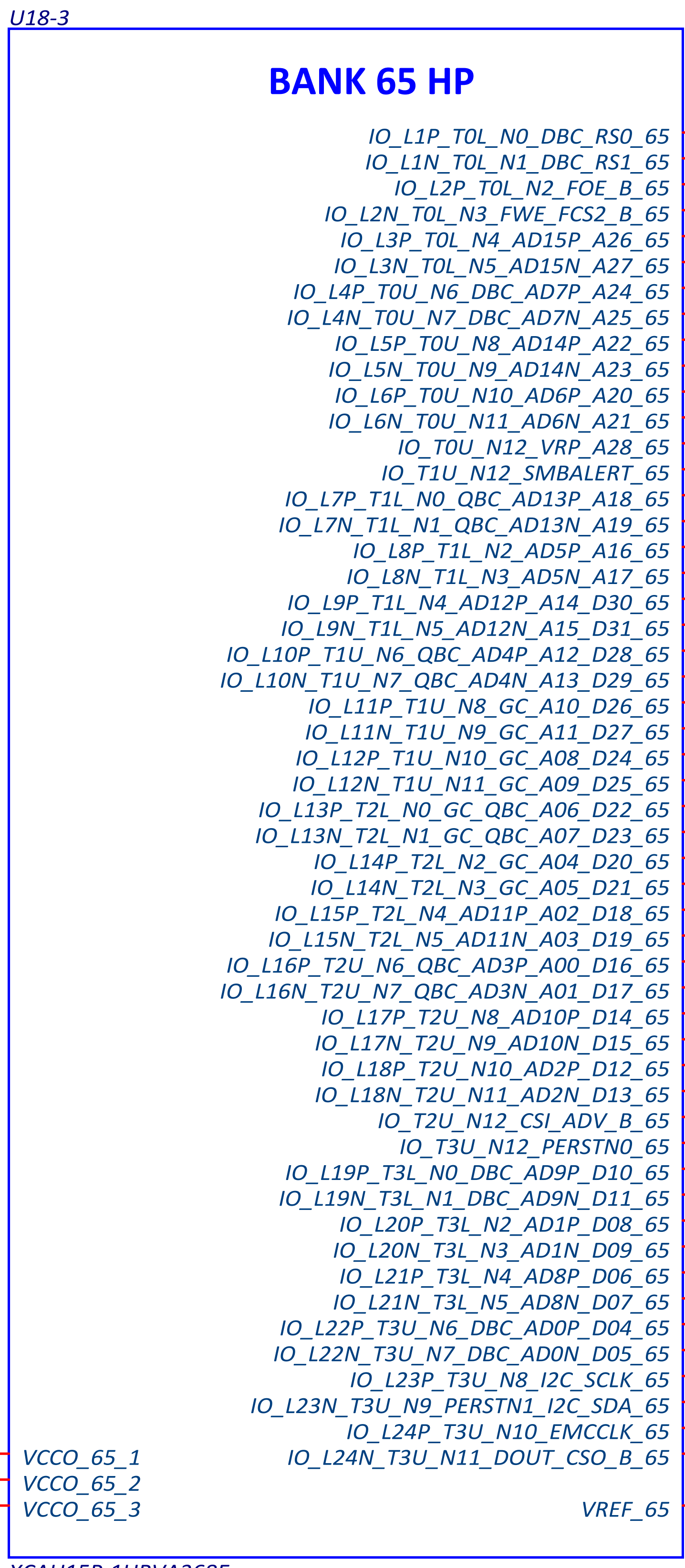
IC VOLT REF ,1.25V

Place the 0.1uF capacitor as close as possible to the package balls.



FPGA Mode SET DIP & Config Interface SW

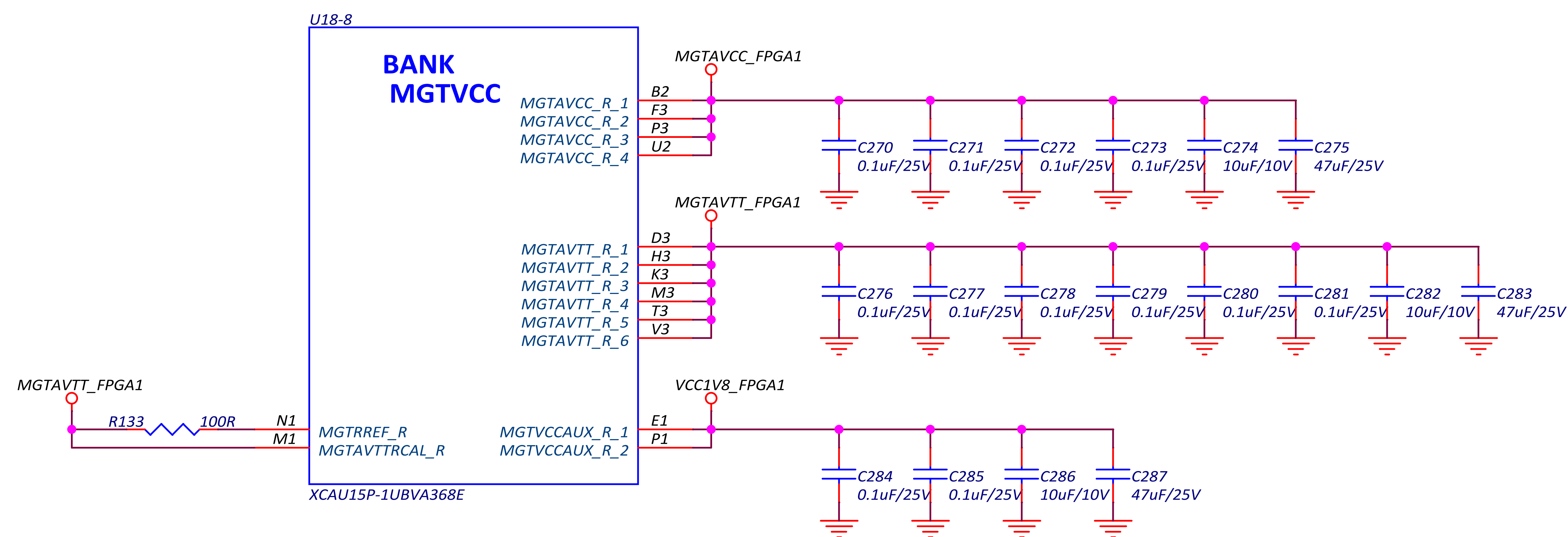
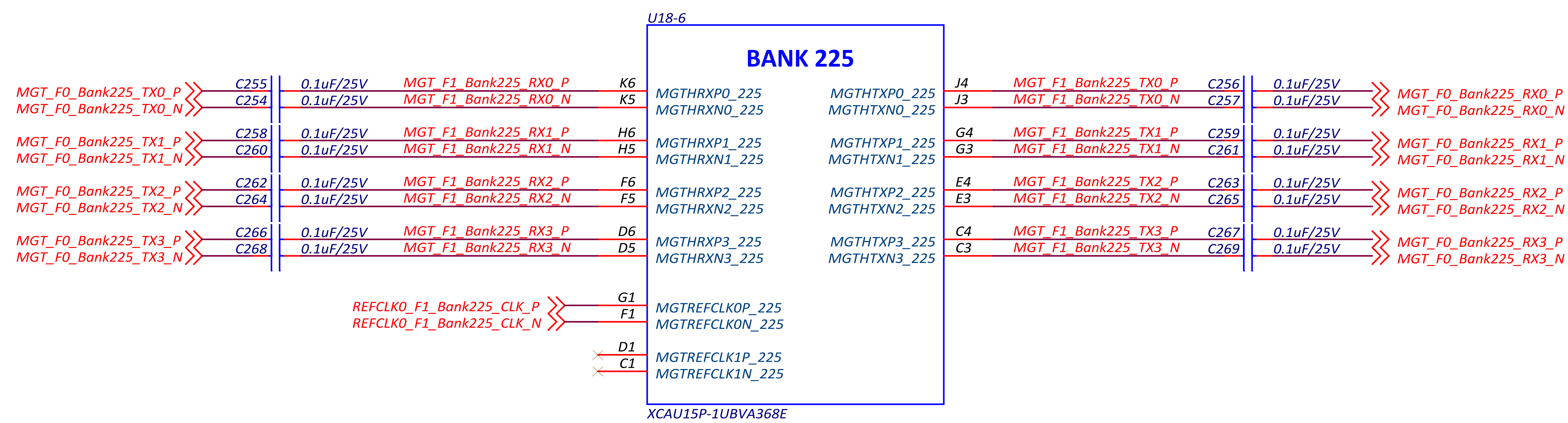
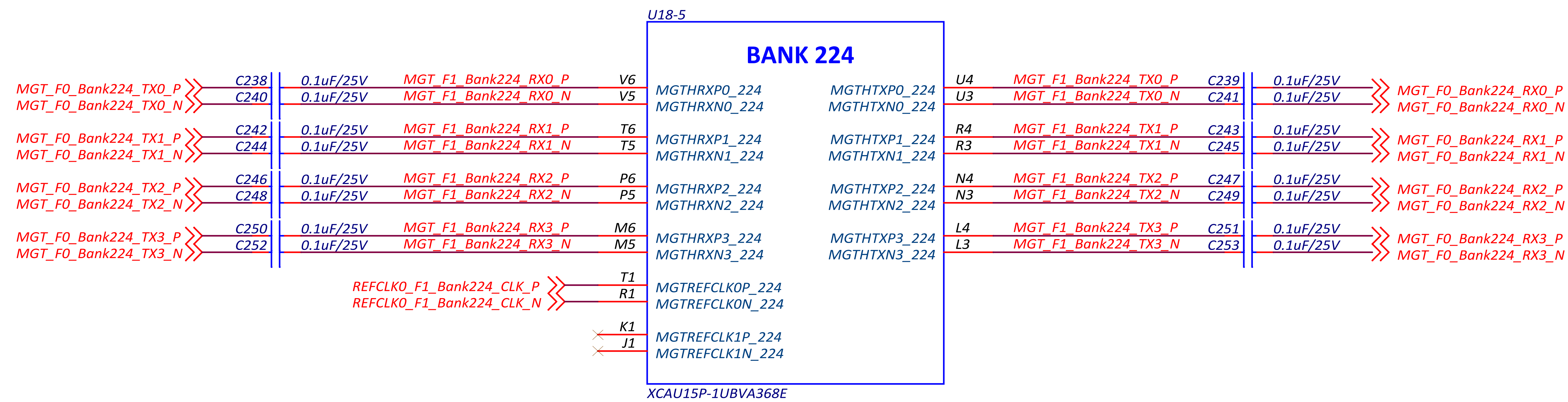
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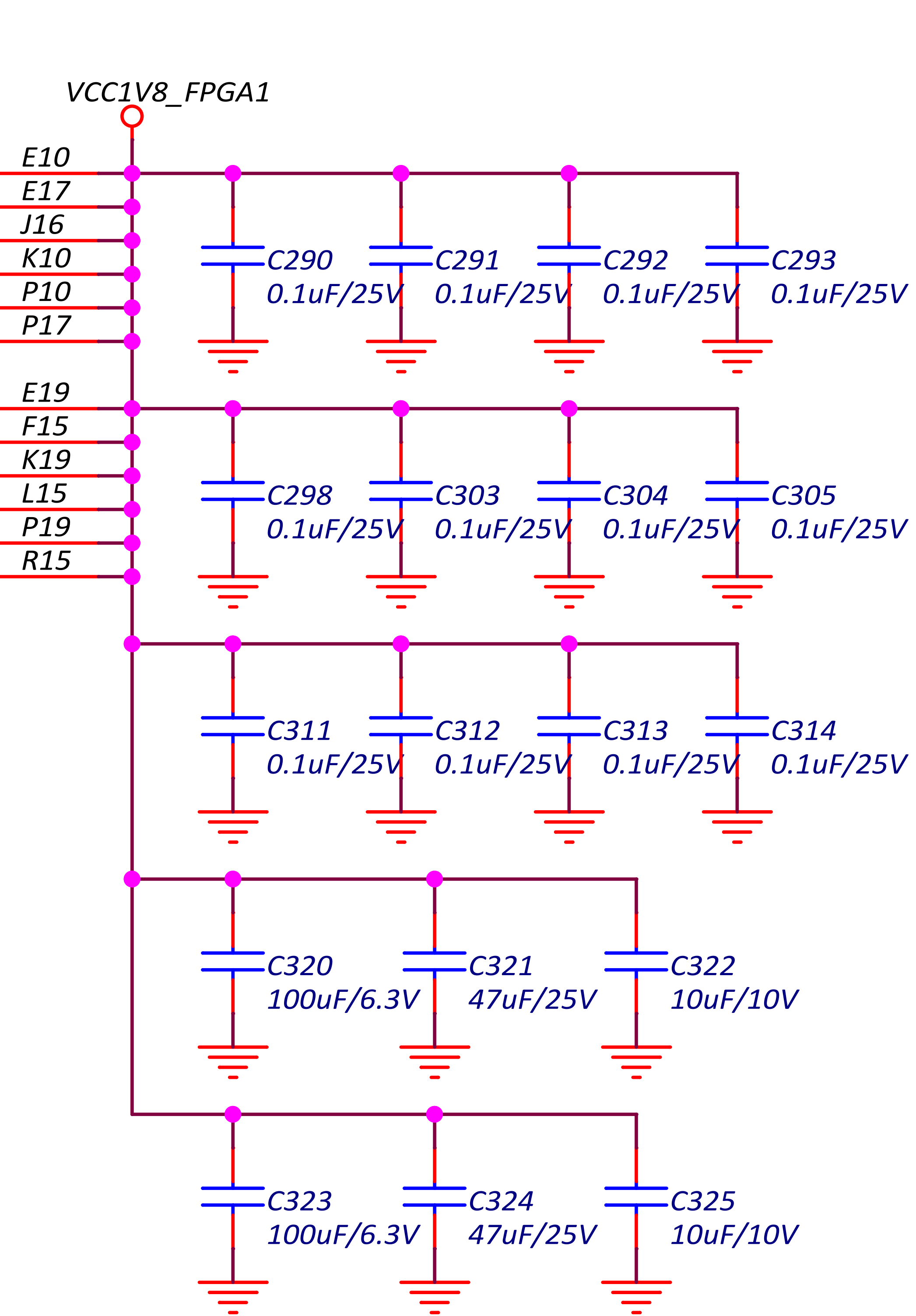
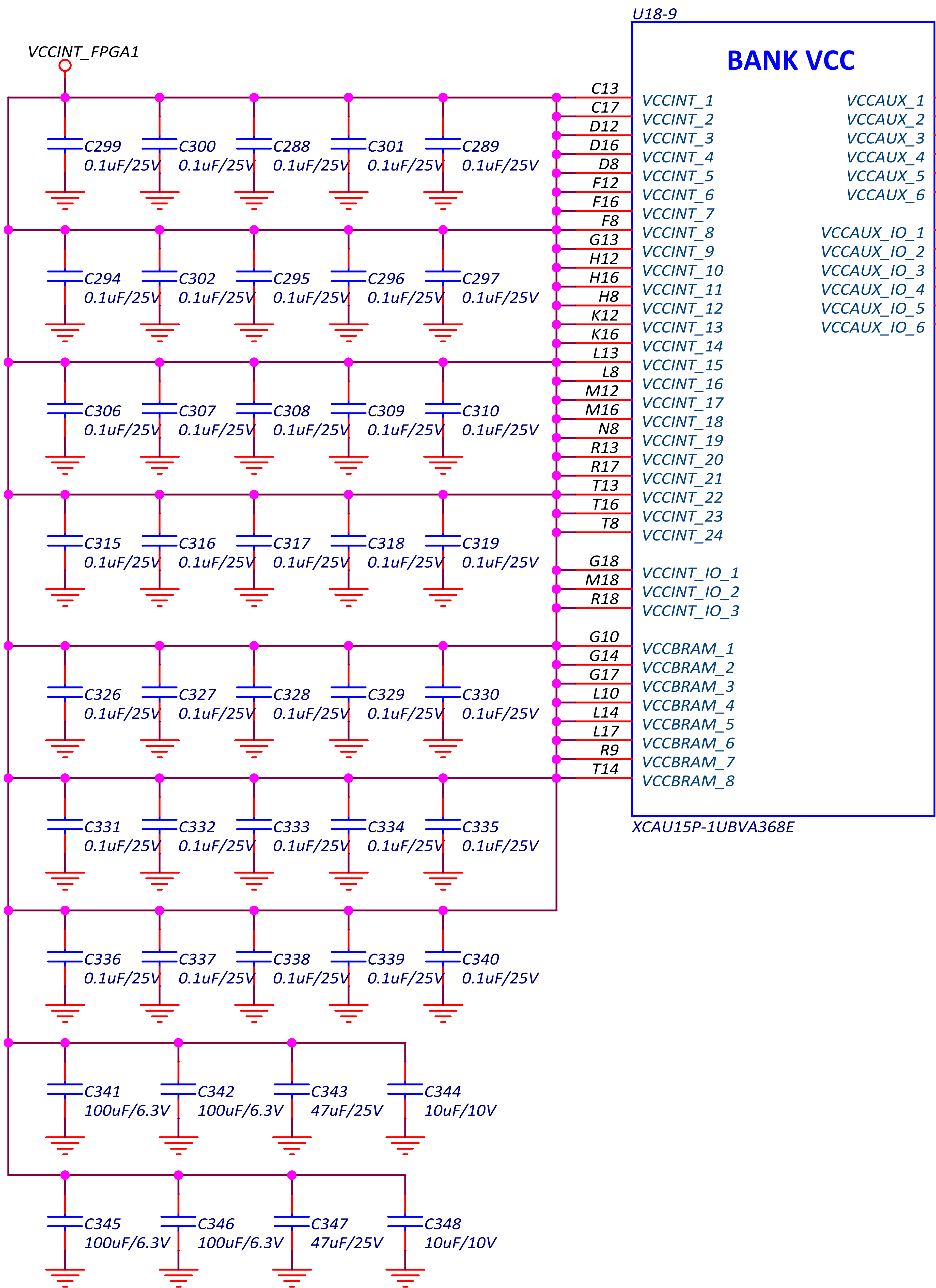
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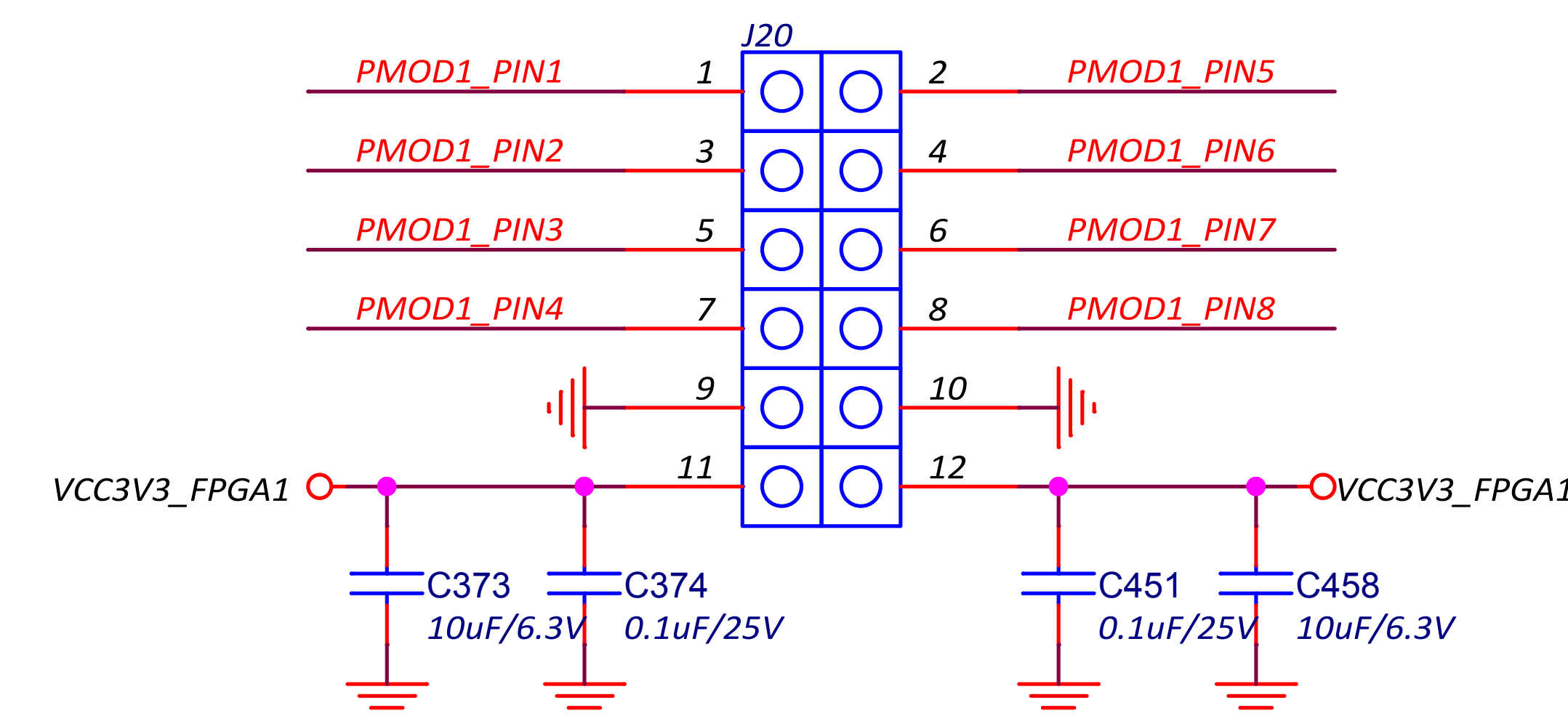
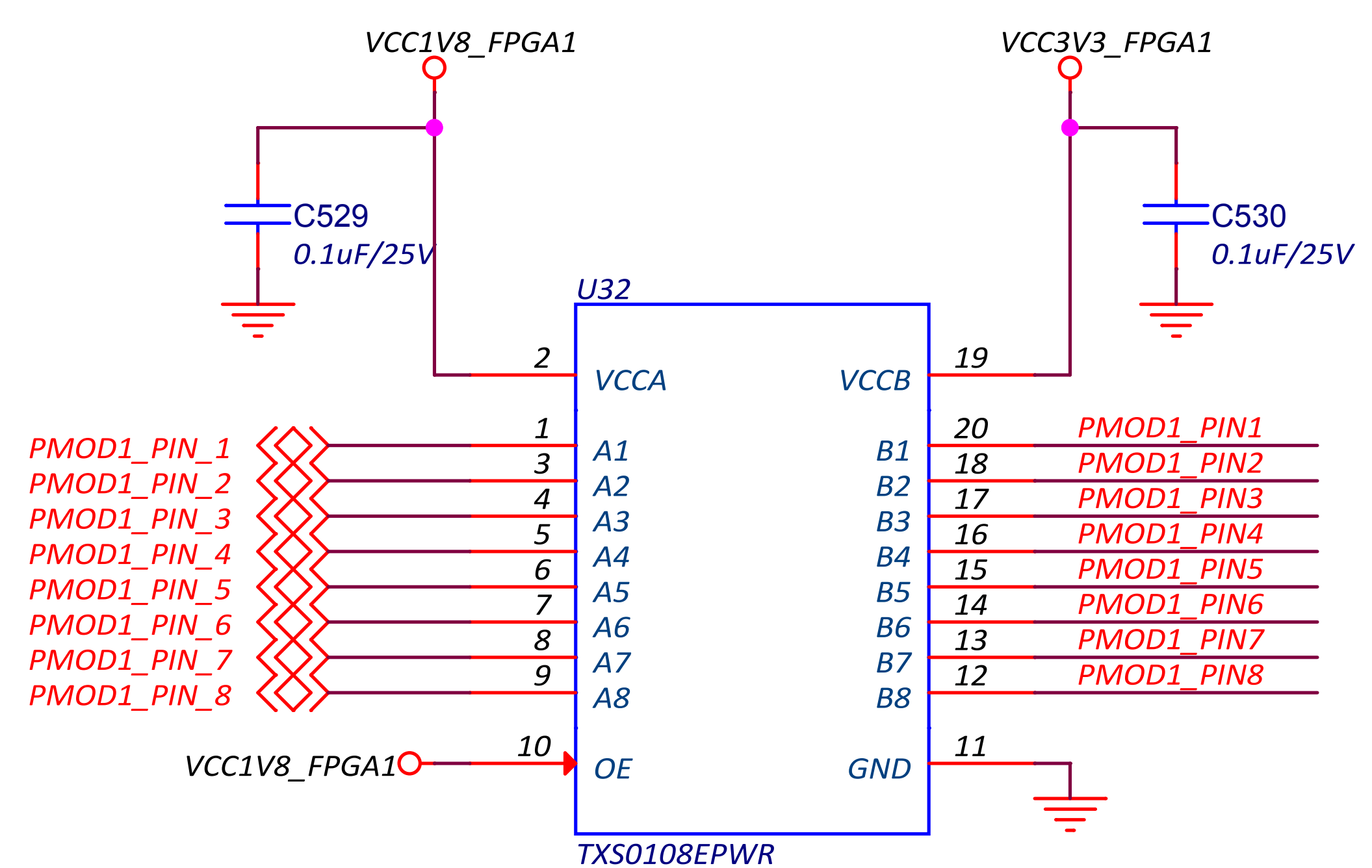
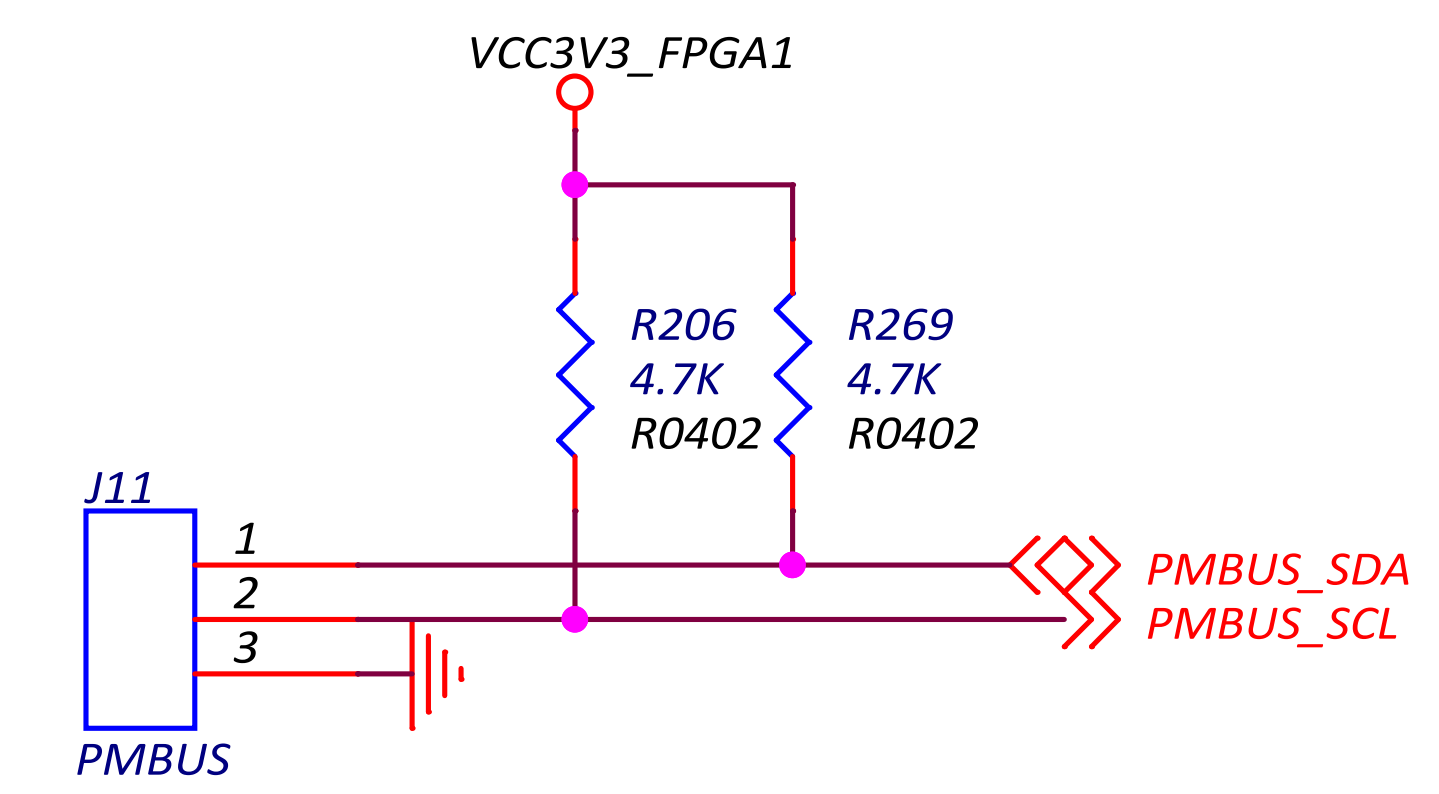
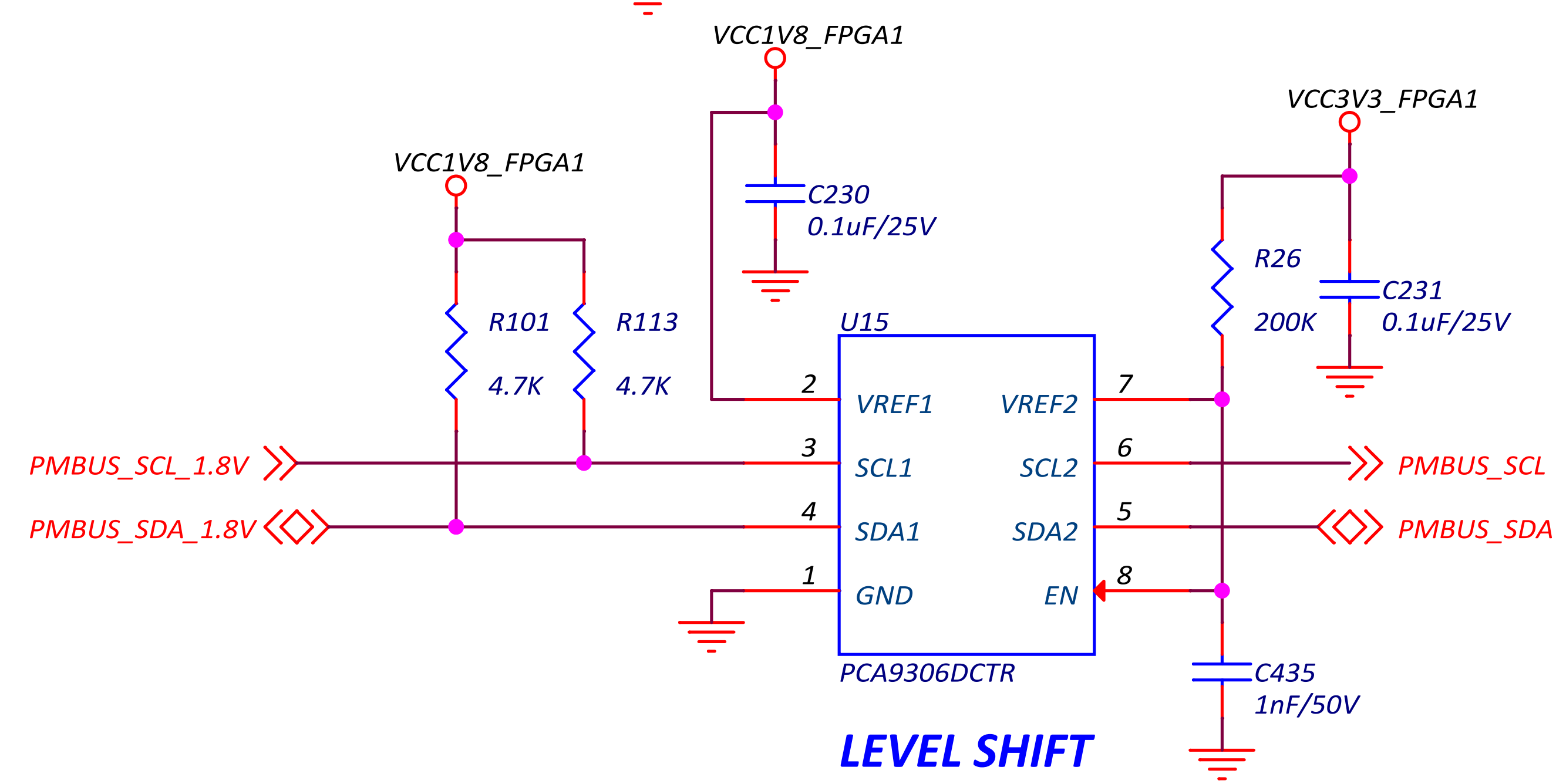
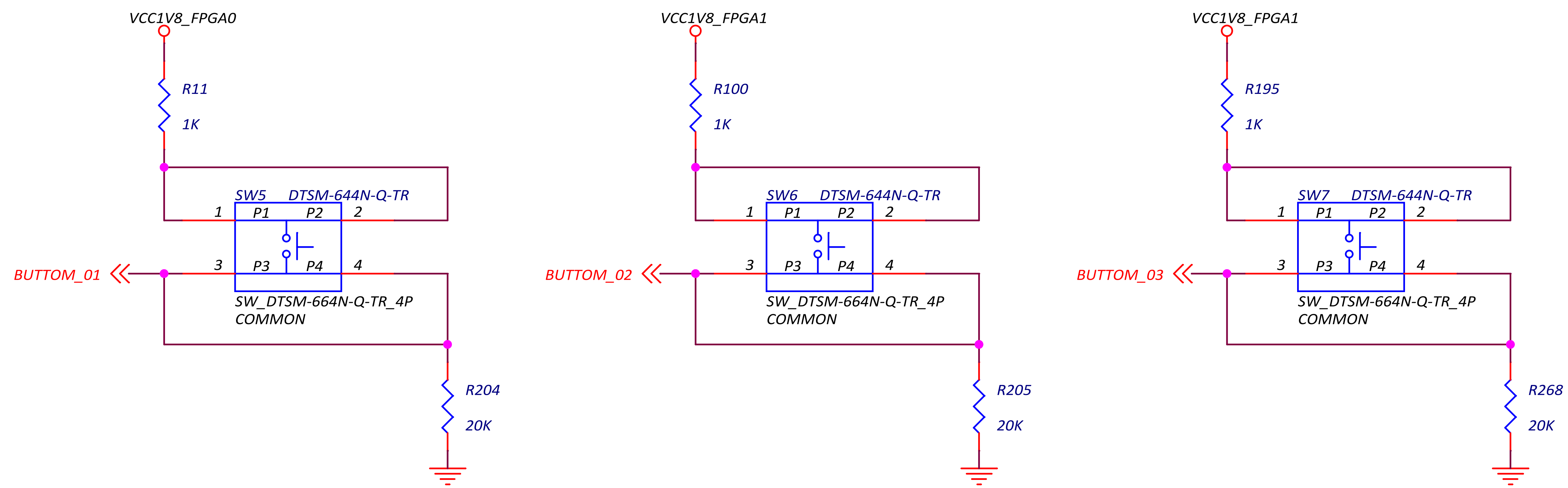
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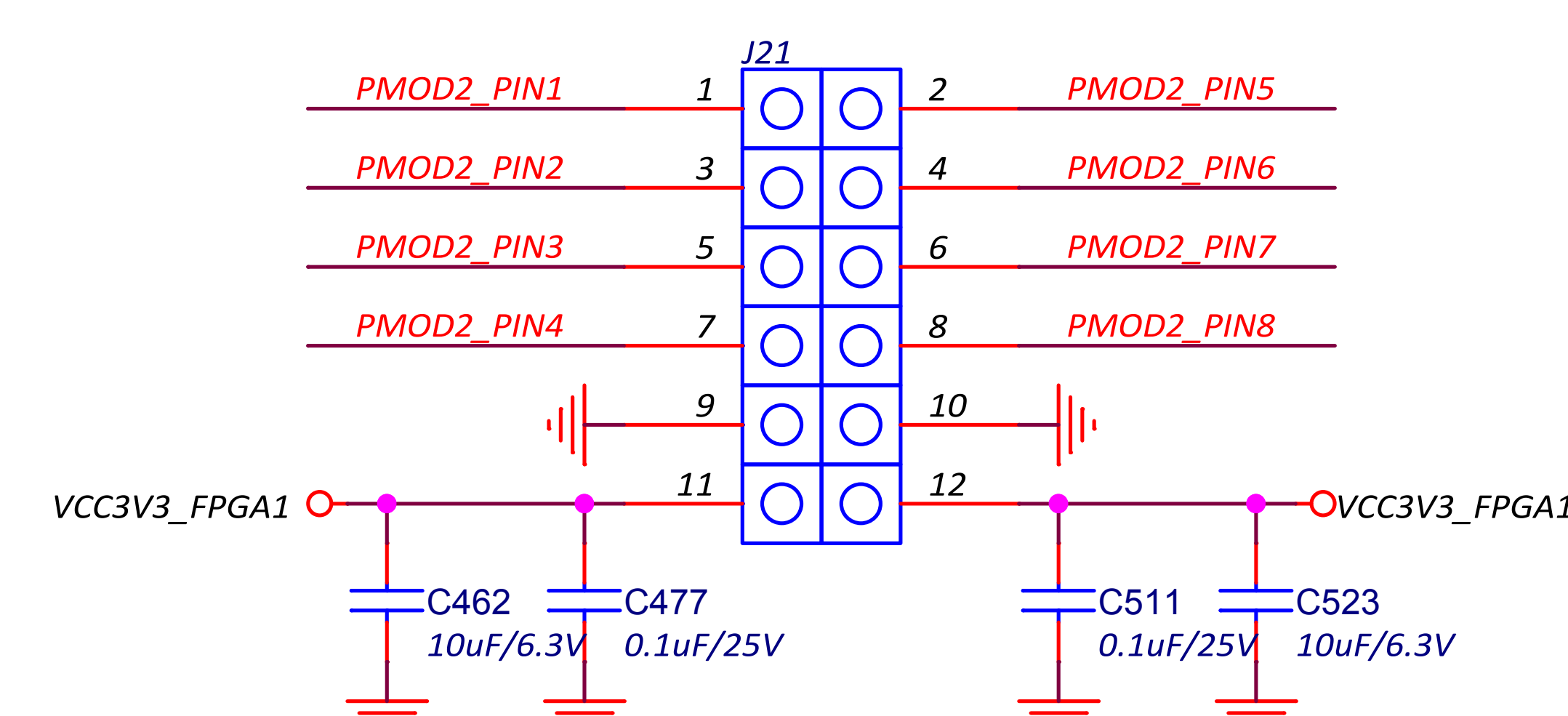
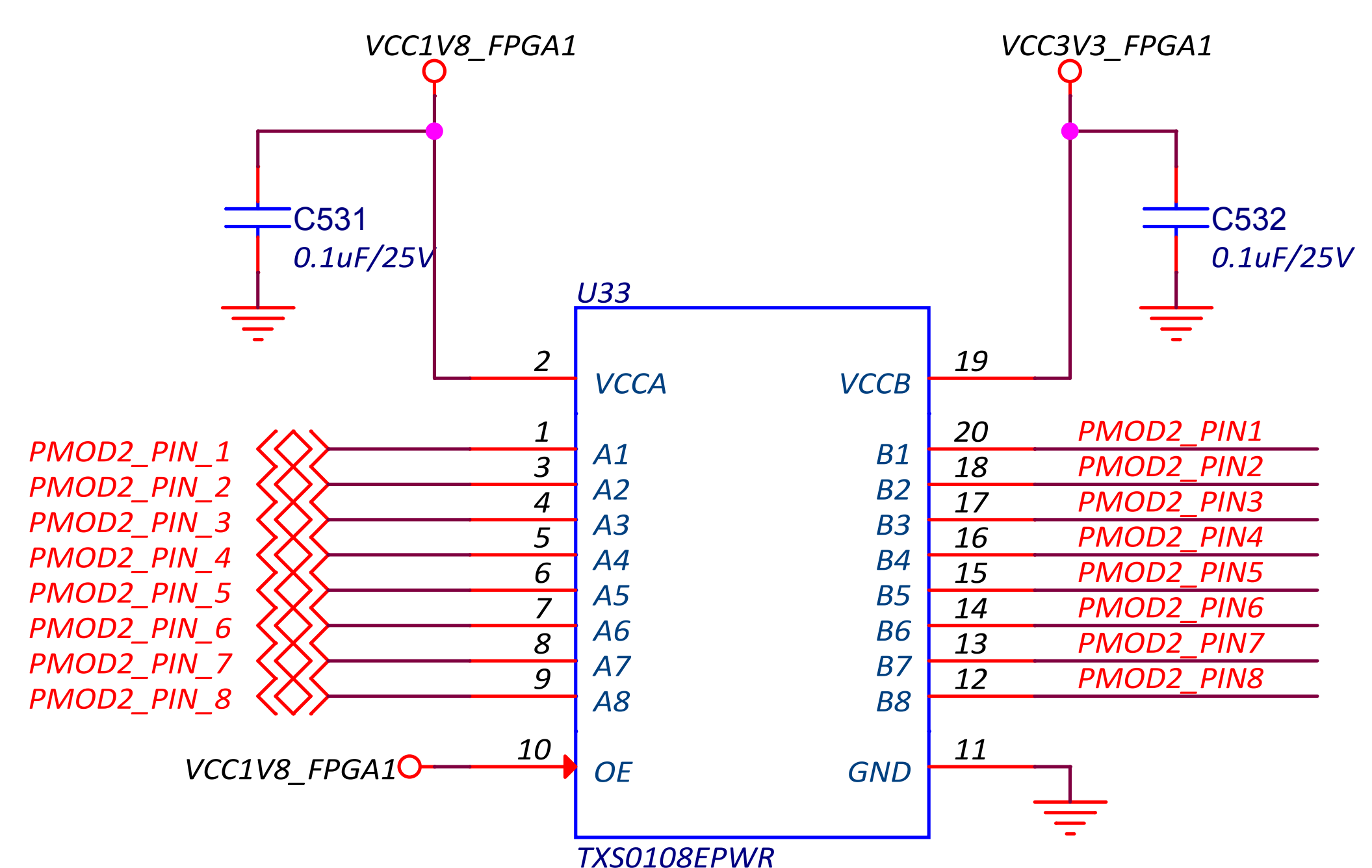


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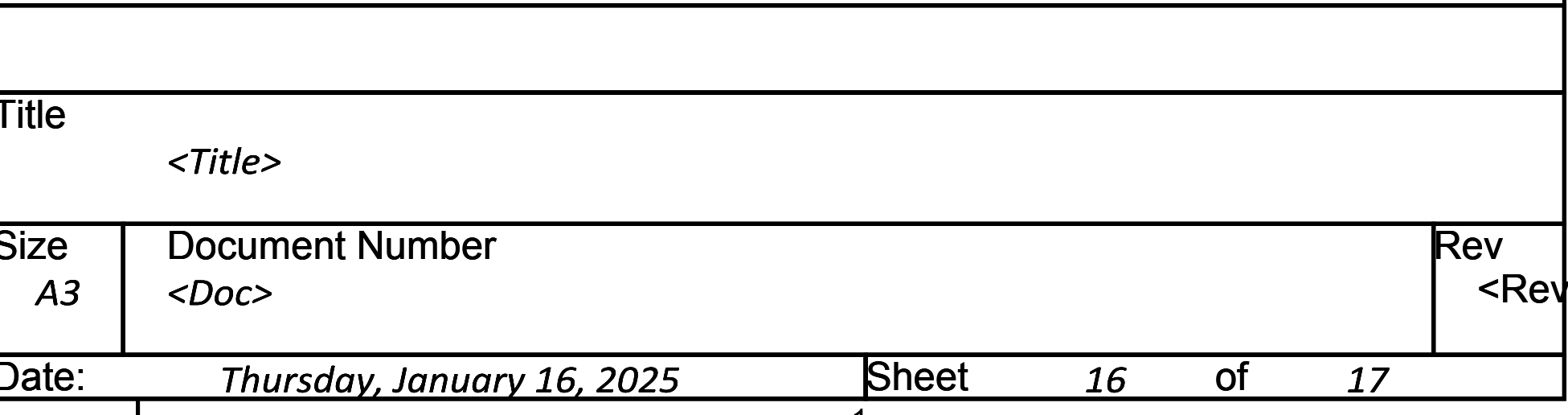




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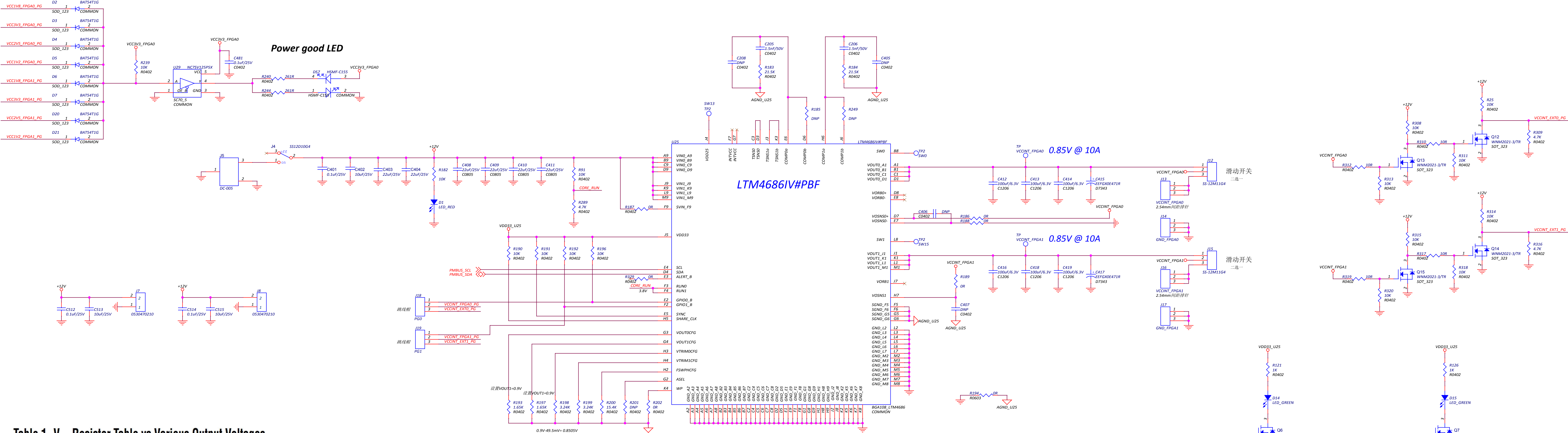


Table 1. V_{FB} Resistor Table vs Various Output Voltages

V_{OUT} (V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3	5.0
$R_{FB(BOT)}$ (k)	Open	90.9	60.4	40.2	30.1	19.1	13.3	8.25

