HTG_940 quick set up

Last Updates: 1/11 2024

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1. Introduction

- Populated with one Xilinx Virtex UltraScale+ VU9P, VU13P, or UltraScale VU190 FPGA, the HTG-940 provides access to wide range of FPGA gate densities, I/Os and memory for variety of different programmable applications.

  The HTG-940 architecture allows easy and versatile functional expansion through four Vita 57.4 compliant High-Pin-Count FPGA Mezzanine Card (FMC+) connectors. The FMC+ ports provide access to total of 370 single-ended FPGA I/Os and 72 GTY /GTH (30.5/16.0Gbps) serial transceivers. The FMC+ ports can host standard Vita57.4 or Vita57.1 daughter cards.

- The HTG-940 is supported by one 72-bit ECC DDR4 SODIMM socket providing access to up to 32 GB of SDRAM memory.

- The HTG-940 provides access to QSFP28 (100G), 100/1000 Ethernet and USB communication port

2. Software Requirements

- Windows 11

3. Equipment Requirements

Machine
- Win 11 Laptop

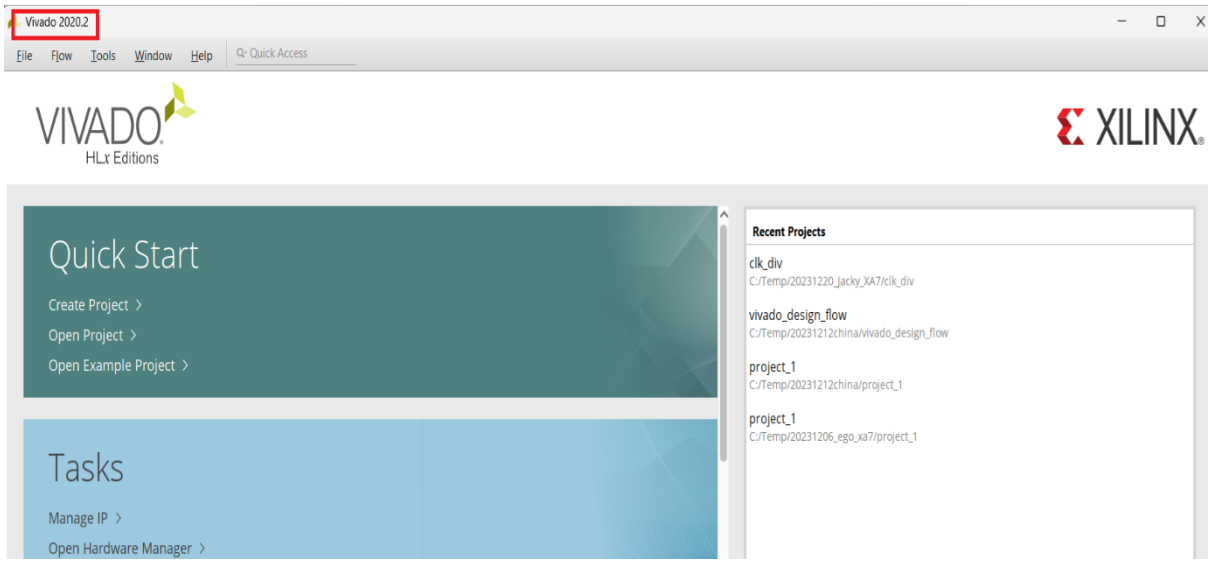
Power supply
- 120W(12V) Power Supply

Cable
- E-Element JTAG cable version2

4. Quick start guide

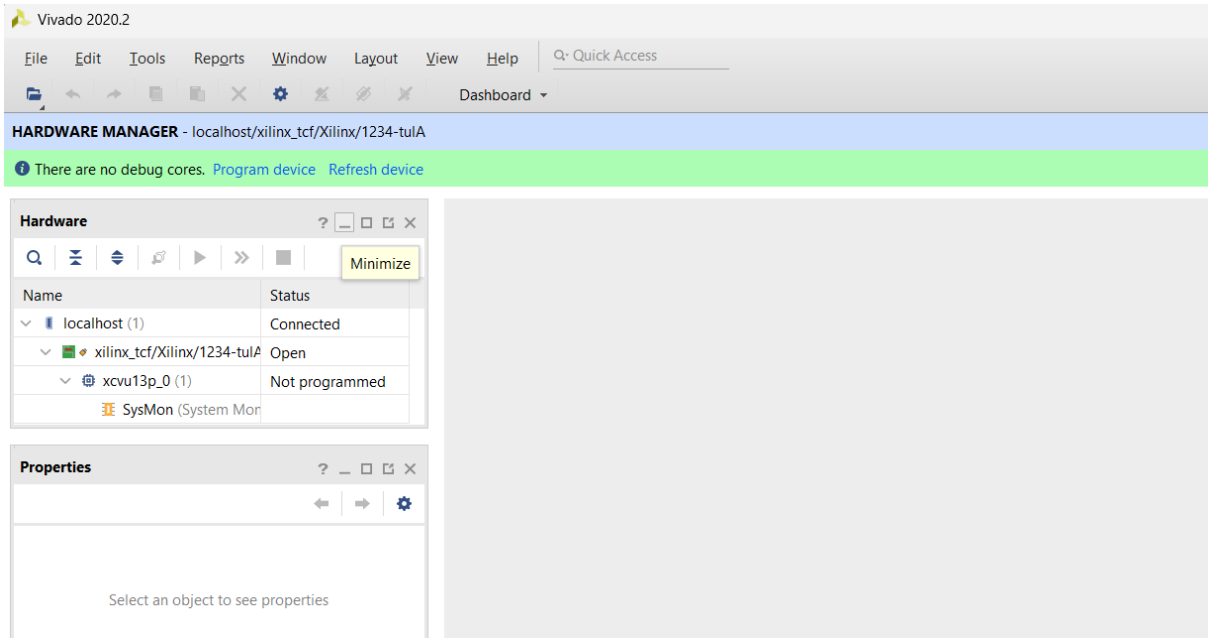
a. Setup as below

b. Open Vivado

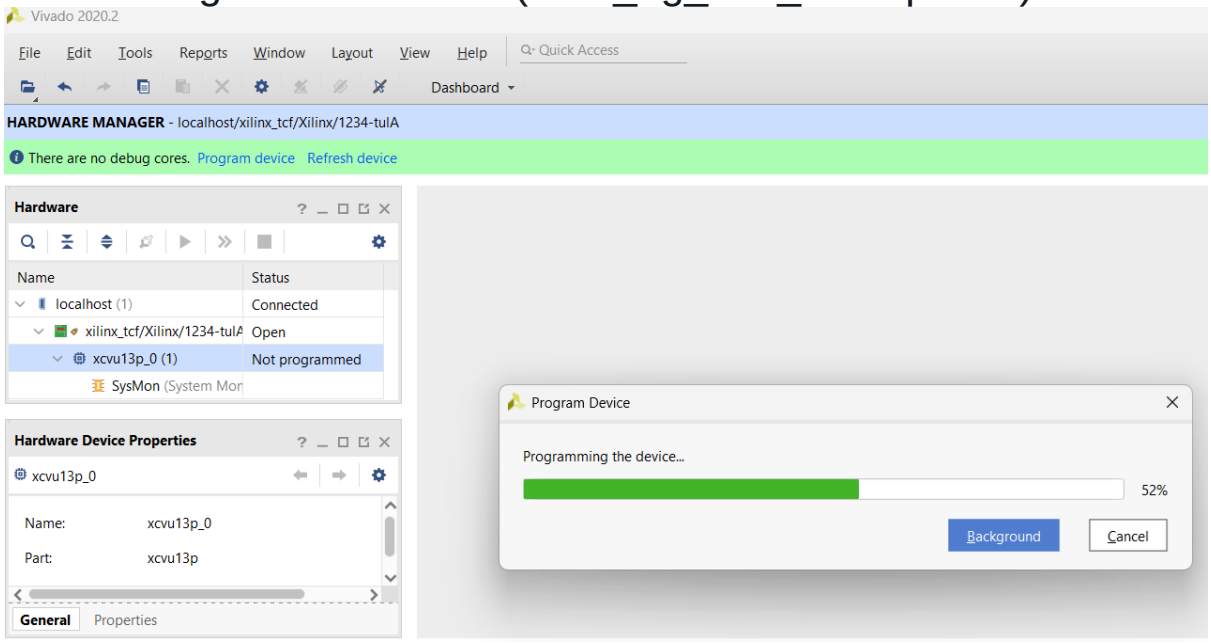


Power on with Device and vivado hardware can show

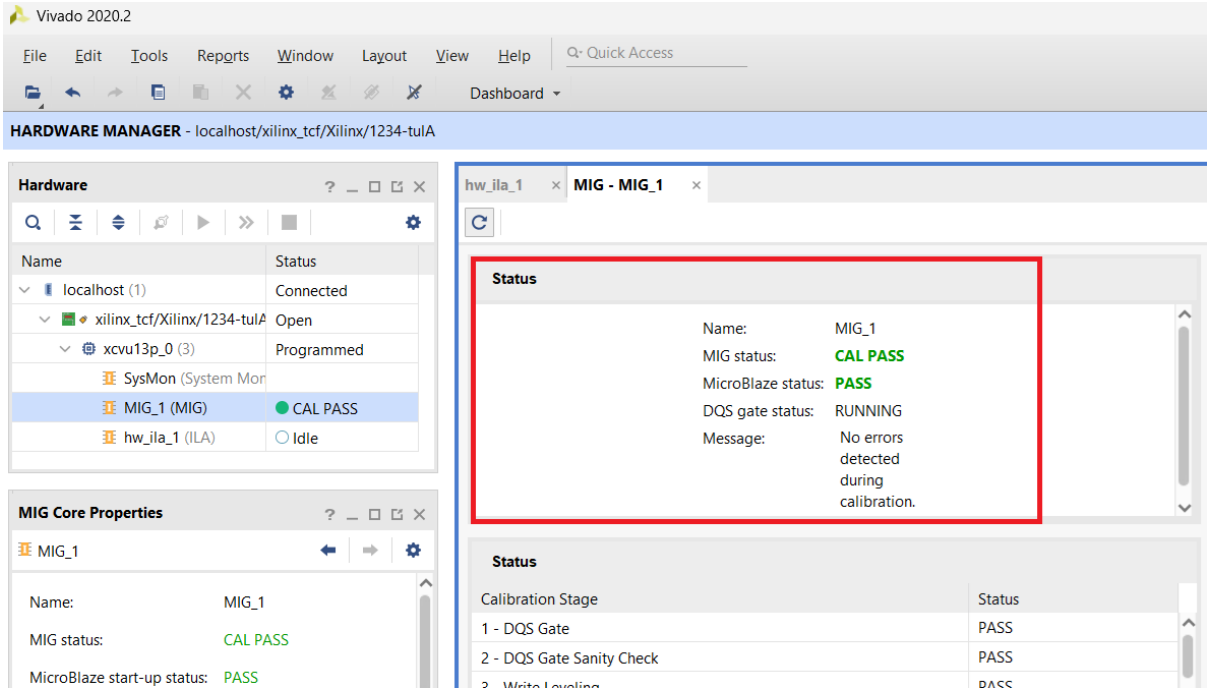
xcu13p(HTG_VU13P)



c. Program the device (ddr4_4g_x64_example.bit)



d. MIG-MIG1 show CAL PASS as below in green


Vivado 2020.2
File Edit Tools Reports Window Layout View Help
Quick Access
Dashboard
HARDWARE MANAGER - localhost/xilinx_tcf/Xilinx/1234-tulA
Hardware
Name
Status
localhost (1)
Connected
xilinx_tcf/Xilinx/1234-tulA
Open
xcvu13p_0 (3)
Programmed
SysMon (System Mon
MIG_1 (MIG)
CAL PASS
hw_ila_1 (ILA)
Idle
MIG Core Properties
MIG_1
Name:
MIG_1
MIG status:
CAL PASS
MicroBlaze start-up status:
PASS
hw_ila_1
MIG - MIG_1
Status
Name:
MIG_1
MIG status:
CAL PASS
MicroBlaze status:
PASS
DQS gate status:
RUNNING
Message:
No errors detected during calibration.
Status
Calibration Stage
Status
1 - DQS Gate
PASS
2 - DQS Gate Sanity Check
PASS