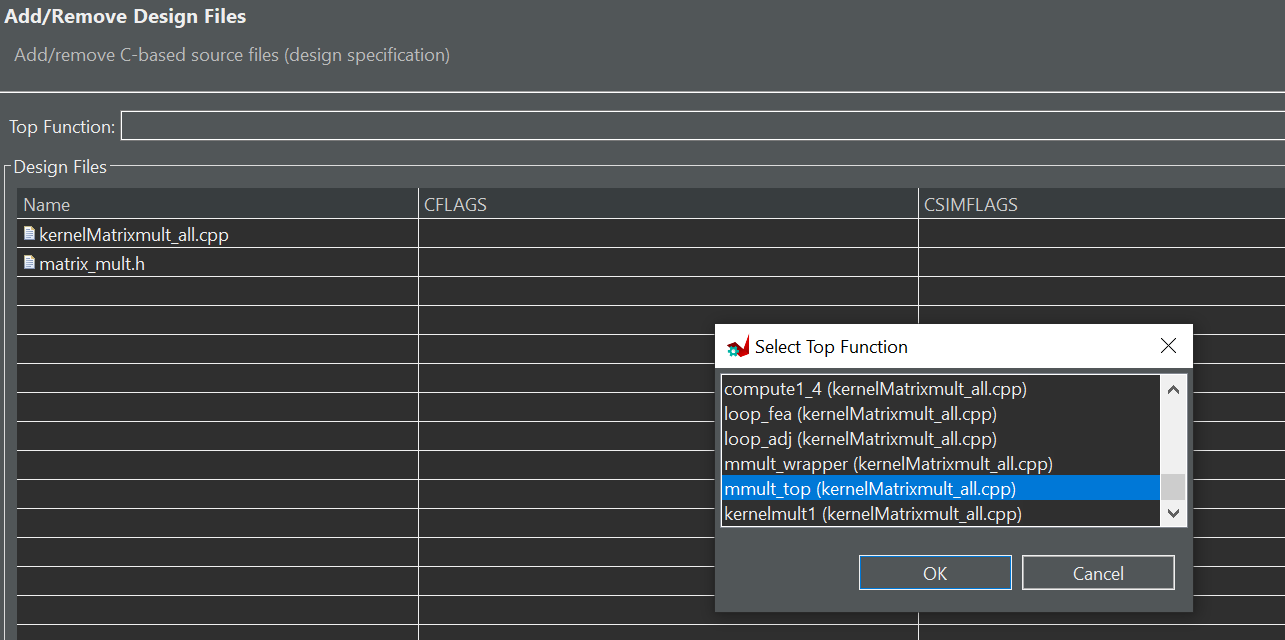
**BASIC SETUP of gFADES GNN accelerator using VITIS in GUI mode.**

1.Create project with Vitis HLS 2022.1 targeting device available in Pynq z2 device. Set clock to 10 ns (100MHz).

Add source files and select the right top function:

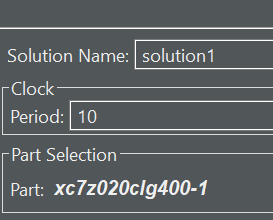


Add testbench files:

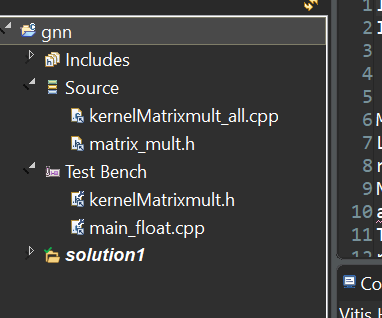
A screenshot of a computer

Description automatically generated

Select the right device for pynqz2 board:



Finish project generation and check that the sources look like this:



2. Simulation

Open matrix\_mult.h

Comment out the simulation setting (I use this to collect some values)

//#define simulation

Set precision to HALF (16bit floating point)

**#define** **HALF**

Most other precisions are not currently supported.

Set the configuration as below so there is 1t1t2c (1 adjacency thread, 1 feature thread, 2 compute units per thread) This should fit on the Pynq Z2.

**#define** **FEA\_THREADS** 1

**#define** **ADJ\_THREADS** 1

**#define** **A\_HEIGHT\_BLOCK** 1// 4096 //(512/4)

**#define** **B\_WIDTH\_BLOCK** 2 //the width of compute1 BLOCK BUFFER A\*B = C 16 //32 //64 //64 //128 // 64 //64 //64 //8//8// //16//32//1//32//1//32//1// 1//32//(128/4)

**#define** **C\_WIDTH\_BLOCK** 2 //the width of compute2 BLOCK BUFFER C\*D = F

**#define** **B\_BLOCK\_PARALLEL** 1

Do project -> run c simulation to check initial functionality. Things should look like this:

Running GNN accelerator

CPU  Total execution time = 5942.11 msec

out :data index= 0 0 kernel = 0.00196838

out :data index= 0 1 kernel = 0.477783

out :data index= 0 2 kernel = 0.59668

out :data index= 0 3 kernel = 0.0311279

out :data index= 0 4 kernel = 0.0022583

out :data index= 0 5 kernel = 0.564453

out :data index= 0 6 kernel = 0.53125

out :data index= 0 7 kernel = 0.0110474

out :data index= 0 8 kernel = 0.114624

out :data index= 0 9 kernel = 0.71582

out :data index= 0 10 kernel = 0.0994873

out :data index= 0 11 kernel = 0.142456

out :data index= 0 12 kernel = 0.652832

.....

3. Synthesis.

Do solution -> run c synthesis to perform C synthesis to RTL.

After the process completes you are ready to export project to Vivado as described in my notes.