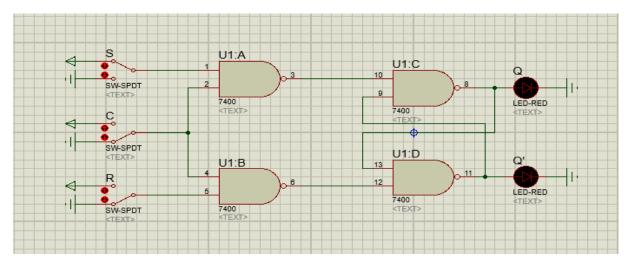
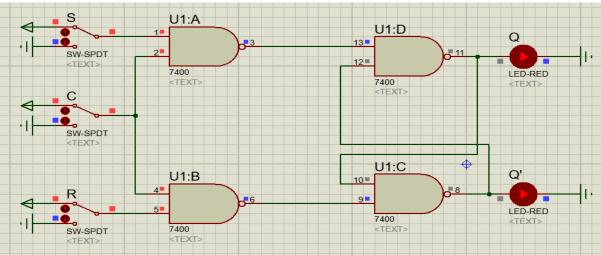
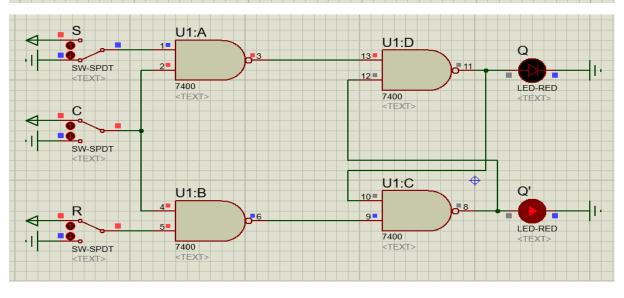
## SAYISAL TASARIM LAB. 5.DENEY PRELAB

## ELIF GENC - 152120151004

## 1.SORU

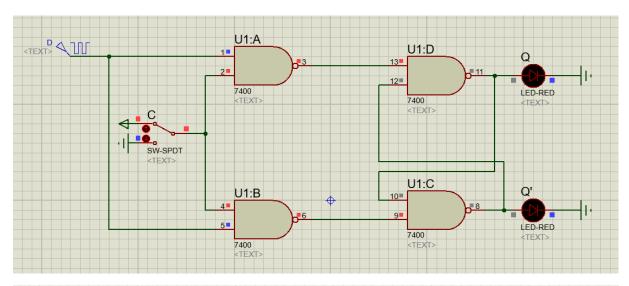


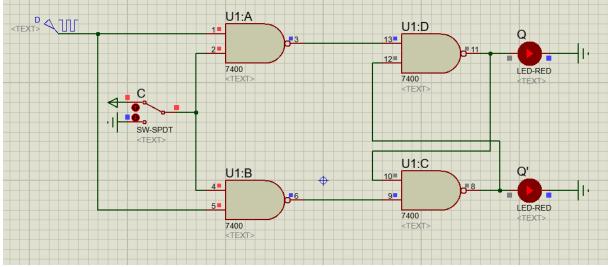


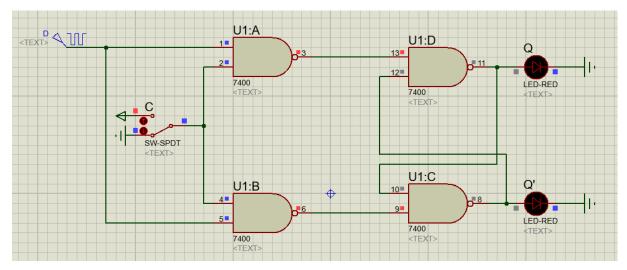


С	S	R	Q	Q'
1	1	0	1	0
1	0	0	0	0
1	0	1	0	1
0	1	0	0	0
0	0	1	0	0
1	1	0	1	0
1	1	1	1	1
0	0	1	0	0
0	1	1	0	0
1	0	0	0	0

## 2.SORU

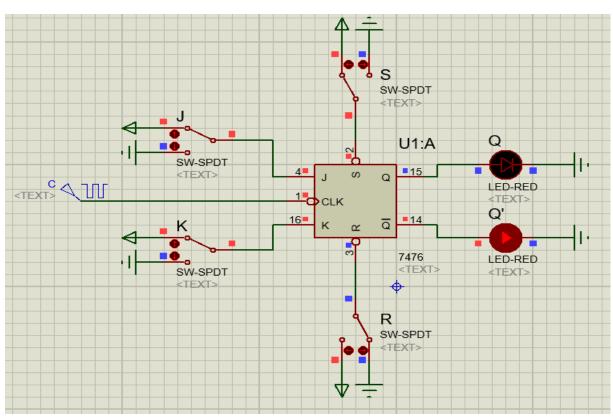


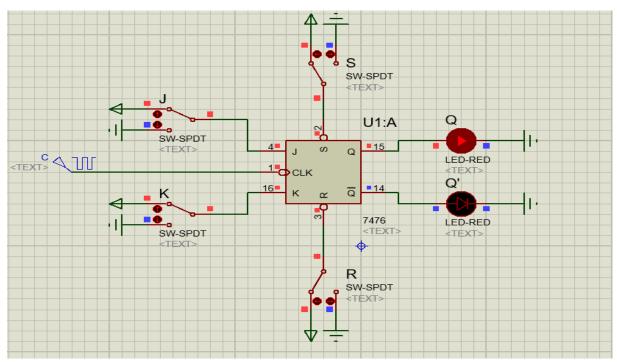


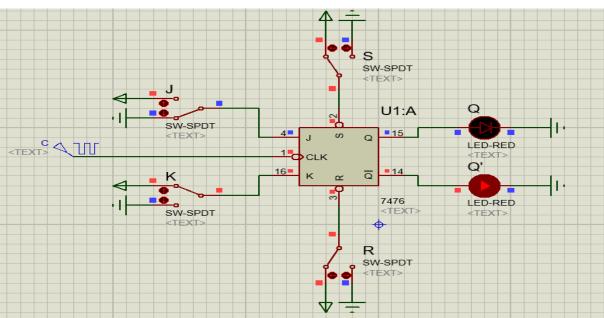


С	D	Q	Q'
1	1	1	1
1	0	0	0
1	1	1	1
0	0	0	0
1	0	0	0
0	1	0	0
1	1	1	1

# 3.SORU

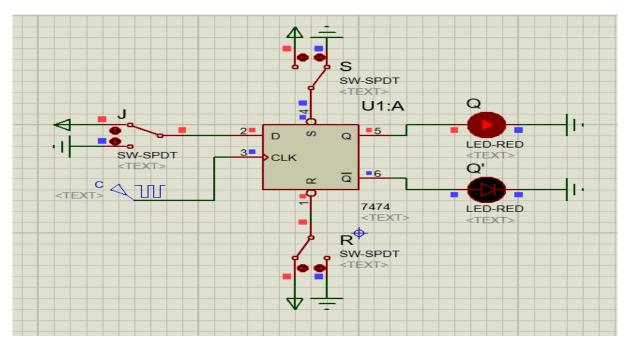


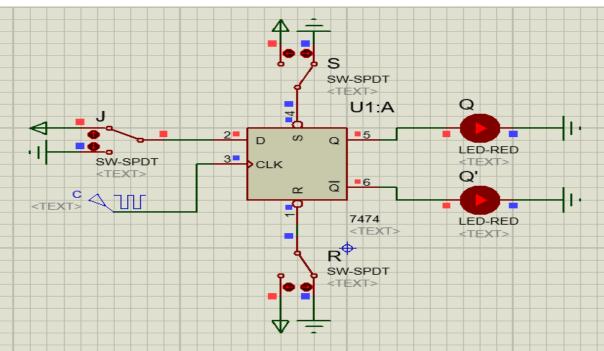




Input				Output		
Preset	Clear	Clock	J	K	Q	Q'
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1	1
1	1		0	0	No change	
1	1		0	1	0	1
1	1		1	0	1	0
1	1		1	1	То	ggle

## 4.SORU





Inputs			Outputs		
PR	CLR	CLK	D	Q	Q
L	Н	X	X	Н	L
н	L	×	×	L	н
L	L	×	×	н	н
н	н	1	н	н	L
н	н	1	L	L	н
н	Н	L	×	Q <sub>0</sub>	$\overline{Q}_0$

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