Lab 6: Synchronous Sequential Circuits and Counters

Objectives

- To construct and test various counter circuits.
- To design, build and test synchronous sequential circuits.

Apparatus

7404 hex inverter
7408 quad 2-input AND gate
7420 dual 4-input NAND gates
7432 Quadruple 2-input OR gates
7474 dual positive edge triggered D flip-flops
7486 quad 2-input XOR gate
74161 synchronous binary counter

PreLab Questions:

Q1. Design a synchronous sequential circuit with one input x, and one output z. When x=1, this circuit goes through the following repeated binary state sequence: 00, 01, 11, 10. When x=0, the state of the circuit remains the same. The output z=1 if the present state is either 00 or 11.

a. Draw the state diagram of the sequential circuit? Is it a Moore or Mealy machine? Explain your answer.
b. Obtain the state table for the given circuit.
c. Design this circuit by using D flip flops and external gates. Draw the logic circuit.

IC Description:

The 74161 is a synchronous 4-bit counter with standard reset. The pin assignment is shown in Fig 6. For normal operation (counting) the reset, preset, count enable and carry in inputs should all be high. When count enable is low the clock input is ignored and counting stops. Effects of the mode select inputs are given in table 4.

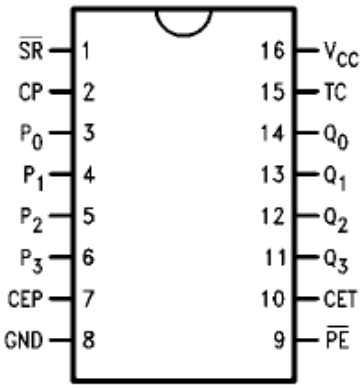

Figure 6

Table 4

$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

The 7474 IC contains two independent positive-edge-triggered D flip-flops with complementary outputs. The pin assignment is shown in Fig 7. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. A low logic level on the preset or clear inputs will

set or reset the outputs regardless of the logic levels of the other inputs. Effects of the mode select inputs are given in table 5.

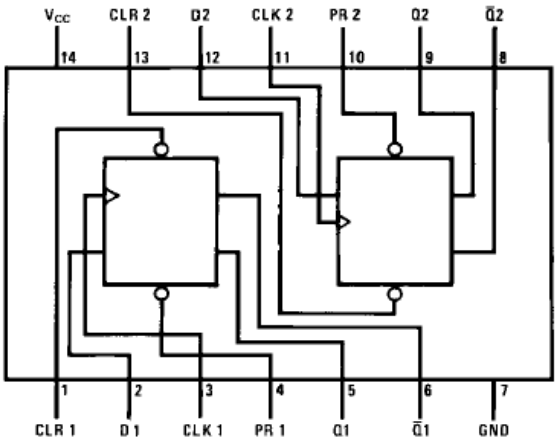

Figure 7

Table 5

Inputs				Outputs	
PR	**CLR**	**CLK**	**D**	**Q**	**$\overline{Q}$**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
L = LOW Logic Level
↑ = Positive-going Transition
Q_0 = The output logic level of Q before the indicated input conditions were established.

Note 1: This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (HIGH) level.

Procedure

1. Connect the BCD counter circuits you designed in prelab Q1.

2. Build the sequential circuit you designed in prelab Q2 by using IC 7474 and external gates (if it is required). Also connect the flip flop outputs to the leds to verify the counting sequences.