**Lab 5: Flip Flops**

**Objectives**

- To become familiar with flip-flops.
- To implement and observe the operation of different flip-flops.

**Apparatus**

7400 quad 2-input NAND gates (x2)
7476 dual JK master-slave flip-flops
7474 dual positive edge triggered D flip-flops

**Procedure**

**1.** Build the SR latch shown in Fig.1. Q and Q' outputs are connected to LED's of the CADET.

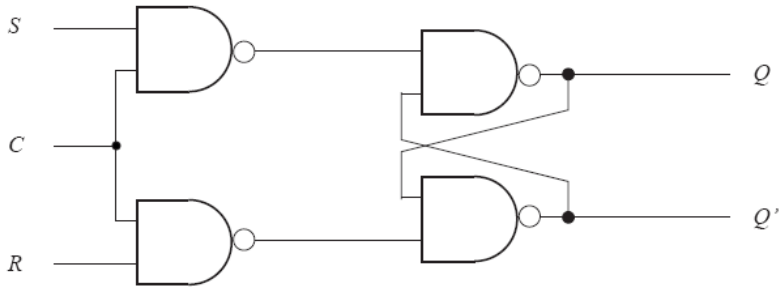


Figure. 1

Verify the truth table of SR latch experimentally.

| C | S | R | Q | Q' |
|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 |

**2.** Modify the basic RS latch into a D latch by adding the steering gates and the inverter shown in Fig.2. Connect the D input to the pulse generator of the CADET and set it at 1 Hz.

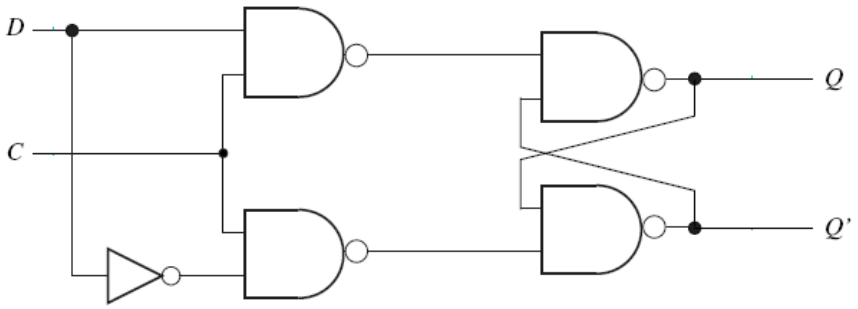


Figure 2.

Obtain the truth table experimentally.

| E | D | Q | Q' |
|---|---|---|---|
| 1 | 1 | | |
| 1 | 0 | | |
| 1 | 1 | | |
| 0 | 0 | | |
| 1 | 0 | | |
| 0 | 1 | | |
| 1 | 1 | | |

**3.** The 7476 is a dual JK master-slave flip-flops with preset and clear inputs. The function table given in Table 1 defines the operation of the flip-flop. The positive transition of the CLOCK (CP) pulse changes the master flip-flop, and the negative transition changes the slave flip-flop as well as the output of the circuit.

**Table 1**

| Input | | | | | Output | |
|---|---|---|---|---|---|---|
| Preset | Clear | Clock | J | K | Q | Q' |
| 0 | 1 | X | X | X | 1 | 0 |
| 1 | 0 | X | X | X | 0 | 1 |
| 0 | 0 | X | X | X | 1 | 1 |
| 1 | 1 | ↓ | 0 | 0 | No change | |
| 1 | 1 | ↓ | 0 | 1 | 0 | 1 |
| 1 | 1 | ↓ | 1 | 0 | 1 | 0 |
| 1 | 1 | ↓ | 1 | 1 | Toggle | |

In the lab, construct the circuit of Fig 3. Connect Q and Q' to the leds on the CADETT. Look at the data sheet for the 7476 and determine the inactive logic required at the PRE and CLR inputs.

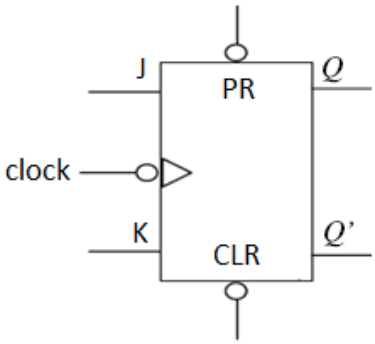


Figure 3.

Connect the 7476 for the SET mode by connecting J = 1, K = 0. With CLOCK (CP) = 0; test the effect of PRE, CLR by putting a 0 on each, one at a time. Verify the operation of the JK flip flop by experimentally obtaining the characteristic.

**4.** IC 7474 contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The function table given in Table 2 defines the operation of the flip-flop.

**Table 2.**

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| PR | CLR | CLK | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | $Q_0$ | $\overline{Q}_0$ |

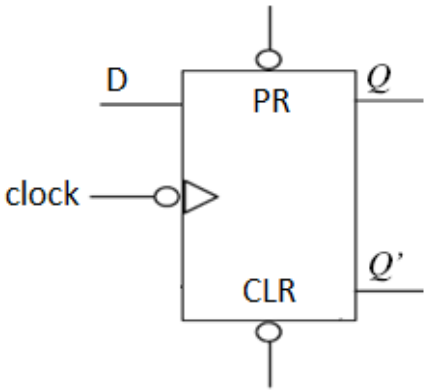


Figure 4.

In the lab, construct the circuit of Fig 4. Connect Q and Q' to the leds on the CADETT. Look at the data sheet for the 7474 and determine the inactive logic required at the PRE and CLR inputs. Verify the operation of the JK flip flop by experimentally obtaining the characteristic.