İZMİR INSTITUTE OF TECHNOLOGY

ELECTRICAL AND ELECTRONICS ENGINEERING DEPARTMENT

SUMMER PRACTICE REPORT

Name - Last Name : Emre Nedim Hepsağ

Turkish Identification # : 19243151332

Student # : 250206012

Company Name : DVL ARGE

Dates : 18/06/2021 - 16/07/2021

Summer Practice # : **EE300**

İZMİR

T.C.
İZMİR INSTITUTE OF TECHNOLOGY
FACULTY OF ENGINEERING
ELECTRICAL & ELECTRONICS ENGINEERING DEPARTMENT
SUMMER PRACTICE REPORT INNER COVER PAGE

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T.R. Identification # : 19243151332

Student # : 250206012

COMPANY / FIRM

Name : DVL ARGE

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Starting Date : 18.06.2021

Ending Date : 16.07.2021

SUPERVISOR AT COMPANY

Name – Last Name : Armağan Ergün

Title : Owner

Contact Info : armagan@dvlx.com

Signature and Stamp : .....

DVL ARGE MÜH. VE TİC.
ARMAĞAN ERGÜN
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Urla V.D. 357 031 2782
T.C. No:344 626 273 52

1. We encourage our students to start writing internship reports during their internships. In this way, they will have the chance to do an internship in awareness of what is required of them.

2. Internship reports must be prepared in accordance with the regulations defined in this document. **Reports that do not comply with these conditions are not assessed and the internship of the student is considered to be unsuccessful.**

3. The reports must be in English and written with computer with **your own words**. Drawing should conform to acceptable engineering standards). The report must not exceed **10 pages in total**.

4. When sources or documents are used in the report from other resources such as internet, company sources, books, data sheets etc., they should be specified both in the text where they are used and in the **References** section. The reports must not consist of cut and paste parts from other sources. The whole report must written in student's own words. In mandatory cases, the tables and figures can be copied, but still must be cited in the text and referenced in the **References** section of the report. The students are responsible for knowing the contents of their reports. When necessary, the students may be invited to the oral exam and respond to the questions about the content of their reports.

5. Internship reports should provide information indicating that engineering activities complementary to the education received at the department have been performed at the company.

6. In the internship reports, the name and contact info of the supervisor must be clearly indicated and the signature and the firm stamp must exist.

7. The reports should be prepared and printed on **A4** size white papers in **1,5 line** spacings in **justified** paragraphs using **12 pt Times New Roman** fonts, with the **top, bottom, and right on 2.2 cm**, and **left on 3 cm**. Main headings are centered and written in capital boldface. Subtitles should be written in small letters and boldface. Drawings should conform to acceptable engineering standards.

8. **Internship reports should be submitted in spiral bound or in filed form, and internship evaluation forms should be presented in closed envelops and approved form. Otherwise the reports will not be evaluated and the internship of the student will be considered as unsuccessful.**

EEE Department Internship Commission

I declare that I have prepared my internship report according to the regulations and notes above.

Student's Name and Last Name: Emre Nedim Hepsağ

Student's Signature: 

TABLE OF CONTENTS

1. DESCRIPTION OF THE COMPANY

I did my internship for 20 days in the department of research and development at DVL ARGE. My purpose was to learn chip designing process, computer architecture and PCB design. DVL ARGE is a research and development company which mostly does electronic based projects such as cube satellites, application specific integrated circuits, printed circuit board design, embedded systems etc. These projects are mostly for defense industry by order for ASELSAN, ROKETSAN and so on. Also, some projects are being done to develop new product. DVL ARGE locates in Teknopark İzmir and has one engineer actively working, Armağan Ergün who is an electric engineer and the owner of the company.

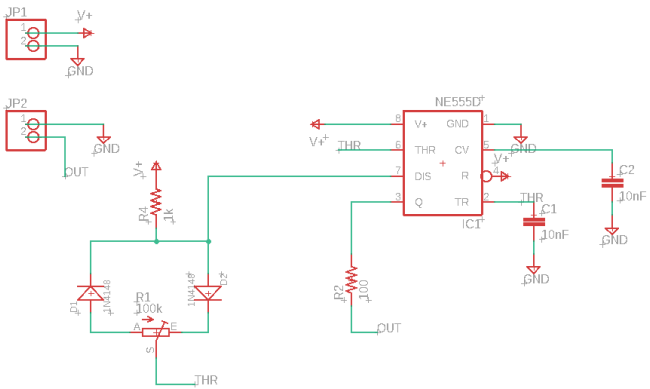
2. INTRODUCTION

The aim of my summer practice was to learn PCB design, VLSI system design and computer architecture and organization. My training continued for four weeks. In the first week, I designed 555 timer circuit board in EAGLE. Then, I soldered my smd component to the PCB with techniques of IPC-CID standards. To protect my board, I imported the PCB to Fusion 360 and with the size information, I designed a hard case for my board. Then I printed the case thanks to the 3D printer in DVL. In the second week, I started to learn physical design of VLSI systems. For that purpose, I installed a virtual Ubuntu to my PC. I learned to use Linux and its terminal. Then, I learned OpenLane software. I did physical design of an ALU module. In the third week, I started to learn RISC-V ISA and instruction set architectures. In the last week, I started to learn computer architecture and organization to acquire detailed knowledge about designing a chip. Then I tried to implement those knowledges to design my own RISC-V chip.

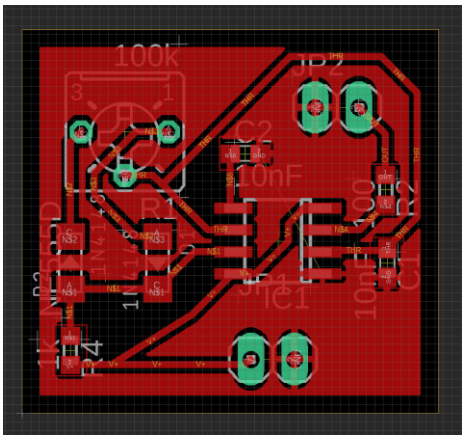
3. BODY OF THE REPORT

4.1 Week 1: PCB design, soldering and 3D design

In the first week of my summer internship, firstly, I learned how to use EAGLE EDA which is a software to design circuit schematic and printed circuit board and I learned to find commercial electronic components models for EDA tools on the internet. With that knowledge, I drew a 555 IC circuit schematic (as seen at visual 1) and board as seen (at visual 2) on EAGLE EDA.

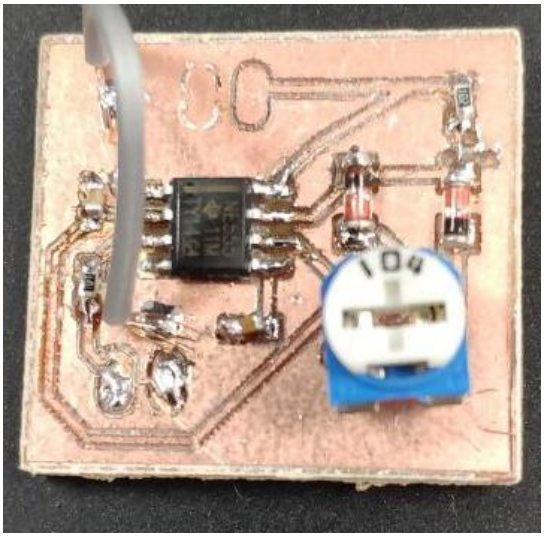


Visual 1. Schematics of 555 Circuit



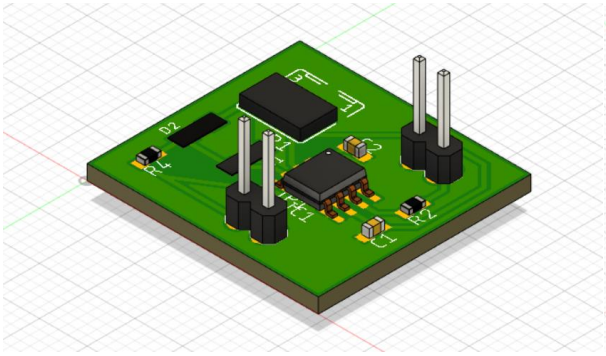
Visual 2. Board of 555 Circuit

Next day, we printed the PCB via CNC machine, and I collected my smd electronic components to solder than just like visual 3. However, before soldering I learnt soldering techniques and PCB design standards which is called IPC-CID standard. After, I soldered my components to the board and checked if it works with a power supply and a DC motor.

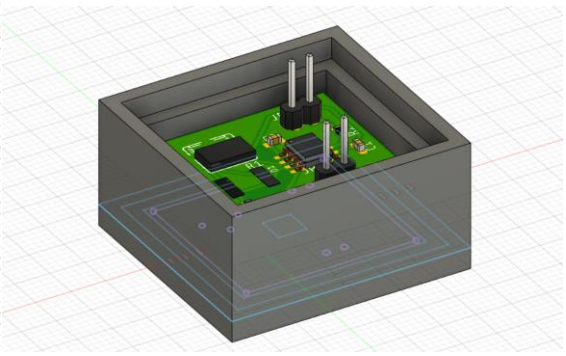


Visual 3. Soldered 555 Circuit

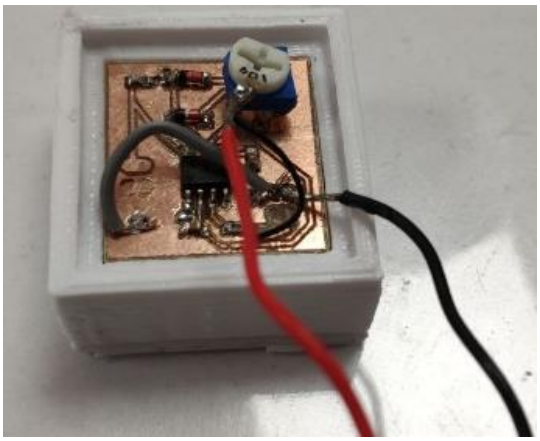
Next, I needed to build a case for the board protection. Thus, I learned 3D design on Fusion 360. I imported 3D files of my PCB into Fusion 360 which looks like visual 4 and designed my protection case as seen at visual 5. After that, with the specs of 3D printer available, I generated .fff file of the design via simplify3d and printed it. The result can be seen at visual 6.



Visual 4. 3D Design of 555 Circuit



Visual 5. 3D Design of Case

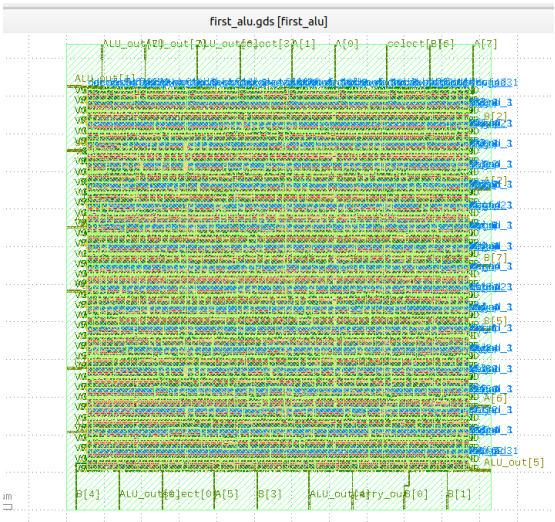


Visual 6. Final State of 555 Circuit

4.2 Week 2: Chip design and VLSI systems

In the second week, I started to learn chip designing. Chip designing has a lot of steps to be accomplished. Normally, VLSI companies has different specialized departments for every step such as front end, physical design and sign off. To explain what the steps are, at the very beginning of design, which is front end design, according to design specifications RTL coding is being done. After coding, function verifications are supposed to be done to check if there is any error. At the second stage which is back-end design, first logic design is being synthesized according to available PDK and check for errors. Then, in physical design, place and route routine is being done, which is quite complicated and has many steps such as floor planning, placement, and routing. Lastly, sign off step is being done to check timing violations before sending the GDSII file to vendors. [1]

Most software work on Linux, that is why I installed a virtual Ubuntu to my PC. I took time to learn a completely new operating system. I learnt to use terminal and use software in terminals such as text editors, containers etc. I mostly preferred open-source software for VLSI system designs. For that reason, I installed OpenLane platform and learnt how to use it. OpenLane is an open-source project which contains lots of software such as OpenROAD, yosys, Magic and KLayout to build a CPU from RTL coding to GDSII [2]. The some of the developers of OpenLane are currently active chip designers who are Tim Edwards, Mohammed Shalan and Ahmed Ghazy. Thanks to them, now chip designing is being able to do with all open-source software from start to end. Physical design has also many steps, thus it took time to learn logic behind them individually. To test myself, I obtained physical layout of my ALU design and SPM chip on KLayout which seems at visual 7.



Visual 7. Physical Layout of the ALU Module

Then I made research about OpenFPGA. Designing an FPGA is pretty complicated. Thus, OpenFPGA helps us greatly to generate open-source intellectual properties. Their aim is to democratize the FPGA designing just like OpenLane [3].

4.3 Week 3: Instruction set architecture, RISC-V and Assembly

In the third week, I started to learn RISC-V instruction set architecture. RISC-V is an open standard of reduced instruction set computer architecture set which aims to let people to design their VLSI systems with open-source standards [4]. Beside learning it, I made research about instruction set architectures and assembly language. Also, I got a training about building a RISC-V processor with TL-Verilog which is an extension to SystemVerilog to change the coding method of RTL design from event-based method to transection level and it claims that it is much more easier and compact [5]. I could not get used to the mechanics of TL-Verilog thus I changed my direction back to the conventional IEEE Verilog. I mostly followed online sources and courses.

4.4 Week 4: Verilog, computer architecture and organization

In the last week, I started to learn computer architecture and organization to design a RISC-V CPU with the book of Computer Organization and Design RISC-V Edition by David A. Patterson, John L. Hennessy. Computer architecture is a really detailed area to study. While learning technical stuffs, I tried to improve my Verilog skills. I learned to use VSCode to write the Verilog and Verilog testbench code then compiled it with Iverilog which is and open-source Verilog compiler. Then, I examined the results as a graph at GTKWave. With the all knowledge I have, I tried to build my own RISC-V CPU from scratch. First, I wrote my memory peripherals. Then, I designed my ALU and lastly, I tried to write my main CPU. I had lots of steps to be done, such as instruction interpretation, pipelining and register usage. In addition to that I build a battery charging tool with Tp4056 module to support another project in DVL.

4. CONCLUSION

From beginning to end of my summer internship I had extensive knowledge about PCB design and VLSI systems. The concepts were mostly new for me to learn.

At the beginning, I started my internship with designing a 555 IC circuit. The routing thickness, and other design constraints were made me learn real life circumstances. After, printing the PCB, the soldering process and learning the IPC-CID standards opened new area about physical implementation of PCB design for me. I did spend some time on 3D design, and it was definitely the most unfamiliar are for me.

After designing my 555 IC circuit, the process of learning almost every concept of designing a chip from instructions set architecture to physical design was challenging for me despite my admiration on that area. While learning physical design, I saw that designing chip in physical manner was impressively similar to designing a PCB. Thus, first week project helped me to comprehend the concept of it quickly. Also, the digital system design course which I got in last term greatly helped me to learn other parts of the chip designing such as static timing analysis and RTL coding, because I already had a base of those topics.

While learning instruction set architectures and RISC-V, I acquired profound knowledge about principle of computer at the lowest programming level which enlarged my vision. With that motivation, I started to learn computer architecture and organization. The area of computer architecture was the topic which I had most learning outcome. Everything just gathered up on that topic to create reasonable concepts in my mind. In other words, after I learnt the essential parts of it, I had connected my knowledge from the beginning of the internship to end. In the whole process, I saw that there is an open-source trend which tries to democratize the hardware designing process from beginning to end. For example, RISC-V, OpenLane, OpenFPGA and others.

To sum up, it was very demanding to obtain good amount of knowledge about chip and PCB design which I am enthusiastic about them individually. Consequently, that helped me to see the different areas and have realistic target for my future plan.

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