EE315 - Electronics Laboratory

Experiment - 7 Simulation
BJT Amplifier Frequency Response

Preliminary Work

1. Common emitter amplifier is characterized by high voltage gain (**A_V**) and current gain (**A_i**). A typical amplifier has a relatively high input resistance (**1-10kΩ**) and a fairly high output resistance. Therefore it is generally used to drive medium to high resistance loads. It is used in applications where a small voltage signal needs to be amplified to a larger voltage signal. Since the amplifier cannot drive low resistance loads, it is usually cascaded with a buffer that serves as a high-current driver.

a) Calculate the values of **R_C**, **R_E**, **R_1** and **R_2** in Figure **1** that will be used in the procedure according to the following requirements:

- **$V_{CEQ} \approx 5$ V**
- **$I_{CQ} \approx 5$ mA**
- **$R_1//R_2$** between **5 kΩ** and **10 kΩ**
- No-load (without **R_L**) voltage gain is **~50**.

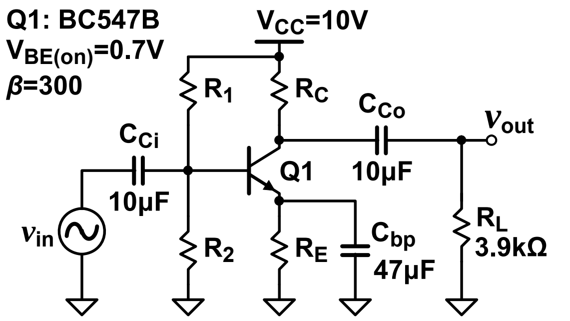

Figure 1: Common emitter amplifier

Hint: Voltage drop on **$R_C + R_E$** should be **5 V** when **$I_{CQ} = 5$ mA**. First, choose a couple of standard resistor values for **R_C** and **R_E** that will give **$R_C + R_E \approx 1$ kΩ**. Afterwards, set **$R_2 = 10$ kΩ** and calculate **R_1** to obtain **$I_{EQ} \approx I_{CQ} = 5$ mA**.

b) Calculate the cut-off frequency due to each capacitor.

2. The common collector amplifier (also called emitter-follower) is a unity voltage gain, high current gain amplifier. The input resistance for this type of amplifier is usually **1 kΩ** to **100 kΩ**. Because the amplifier has a voltage gain of one, it is useful as a buffer amplifier, providing isolation between two circuits while providing driving capability for low resistance loads.

a) Calculate the values of **R_C**, **R_E**, **R_1** and **R_2** in Figure **2** that will be used in the procedure according to the following requirements:

- **$V_{CEQ} \approx 5$ V**
- **$I_{CQ} \approx 5$ mA**
- **$R_1//R_2$** between **5 kΩ** and **10 kΩ**

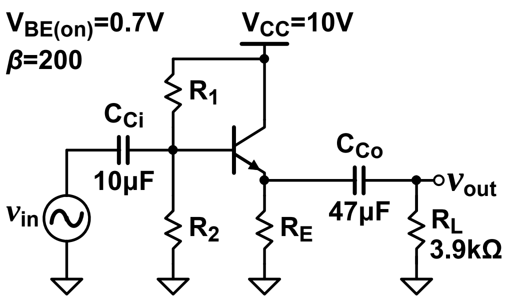

Figure 2: Common collector amplifier

b) Calculate the cut-off frequency due to each capacitor.

Procedure

1.a) Build the circuit given in Figure **1** using the values calculated in the preliminary work. Set the input voltage to **20 mV**peak. Record the values of v_{in}, v_{out} and calculate $A_V = 20 \log|v_{out}/v_{in}|$, sweeping the input frequency from **50 Hz** to **100 kHz**.

f (Hz)	v_{in} (V)	v_{out} (V)	A_V (dB)
50			
100			
200			
500			
1000			
2000			
5000			
10000			
20000			
50000			
100000			

1.b) Increase the input signal level until output voltage clipping occurs. Record the maximum input and output levels of undistorted sine wave signal.

1.c) Note the phase shift between output and input. Is your amplifier inverting or noninverting?

1.d) Is the bandwidth of your common emitter amplifier suitable for an audio amplifier? Which one of the three capacitors (C_{Ci}, C_{Co}, or C_{bp}) is the component that limits the bandwidth? What should be done to cover the frequency range required for an audio amplifier?

1.e) What will be the voltage gain of your common emitter amplifier, if $R_L = 8\Omega$ (input resistance of a common speaker)?

1.f) Right-click on the v_{in} source, select "**(none)**" as the source function and set **AC amplitude** to **1.0** in the **Small signal AC analysis (.AC)** section. Right-click on the "**.tran.....**" simulation command, select the **AC analysis** tab, select "**Decade**" sweep type with **100** points per decade resolution and set the frequency range from **50 Hz** to **100 kHz**. Run simulation and observe v_{out} as a function of frequency. Compare the AC analysis results with the A_V values found in **1.a**.

1.g) Increase stop frequency to **100Meg** in the **.AC** simulation command. Run simulation and record the **-3 dB** high frequency cut-off point.

F_{HFC} = __________

1.h) Typically there is a **10 pF** capacitance between two neighboring slots of a breadboard. In order to simulate the transistor behavior on a breadboard, connect a **10 pF** capacitor between base and collector pins of the transistor and connect another **10 pF** capacitor between base and emitter pins. Run simulation and record the **-3 dB** high frequency cut-off point with the added capacitors.

F_{HFC} = __________

Explain the change in the high cut-off frequency.

2.a) Build the circuit given in Figure **2** using the values computed in the preliminary work. Set the input voltage to **100 mVpeak**. Record the values of v_{in}, v_{out} and calculate $A_V = 20 \log|v_{out}/v_{in}|$, sweeping the input frequency from **50 Hz** to **100 kHz**.

f (Hz)	v_{in} (V)	v_{out} (V)	A_V (dB)
50			
100			
200			
500			
1000			
2000			
5000			
10000			
20000			
50000			
100000			

2.b) Set input frequency to **10 KHz** and increase the input signal level until output voltage clipping occurs. Record the maximum input and output levels of undistorted sine wave signal.

2.c) Is your amplifier inverting or noninverting?

2.d) Is the bandwidth of your common collector amplifier suitable for an audio amplifier?

2.e) What will be the voltage gain of your common collector amplifier, if $R_L = 8\Omega$? How will this change affect the bandwidth? What can be done to restore the bandwidth?

2.f) What is the main purpose of using the emitter follower?