EE315 - Electronics Laboratory

Experiment - 5 Simulation

MOSFET Characteristics and Small Signal Amplifier

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Preliminary Work

1-) $v_{in} = 3.0V$

$V_{OS} = 10V - 100 i_D$

$i_D = 50m(3-2)^2 = 50mA$

$V_{OS} = 10 - 5 = 5V$

$5 \geq (3-2)$ ✓

Saturation

$V_{in} = 3.5V$

$V_{OS} = 10V - 100 i_D$

$i_D = 50m(3.5-2)^2 = 112.5mA$

$V_{OS} = 10 - 11.25 = -1.25V$

$-1.25 \geq (3.5-2)$ ✗

not saturation

$i_D = 50m[2(3.5-2)(10-100i_D) - (10-100i_D)^2]$

$1000 i_D^2 - 168 i_D + 7 = 0$

$\Delta = 224$

$\sqrt{\Delta} = 14.967$

$x_1 = \frac{168 - 14.967}{2000} = 76.52mA$

$x_2 = \frac{168 - 14.967}{2000} = 91.48mA$ $V_{OS} < (V_{GS} - V_{TN})$

2-) $V_{OS} = (10 - (-10))/2 = 10$

$10 - 10m \times R_D - V_{OS} - 10m \cdot R_S + 10 = 0$

$10 - 10m \times 5.5 R_S = 0$

$R_S = 182\Omega$

$R_D = 819\Omega$

$\frac{R_D}{R_S} = 4.5$

$V_G = \frac{20 R_2}{R_1 + R_2} - 10$

$V_{out} = 10 - R_D i_D = 1.81V$

$1.81V = \frac{V_{DD} + V_G}{2} = \frac{10 R_2}{R_1 + R_2}$

$R_1 = 8.19k\Omega$

$R_2 = 1.81k\Omega$

Results

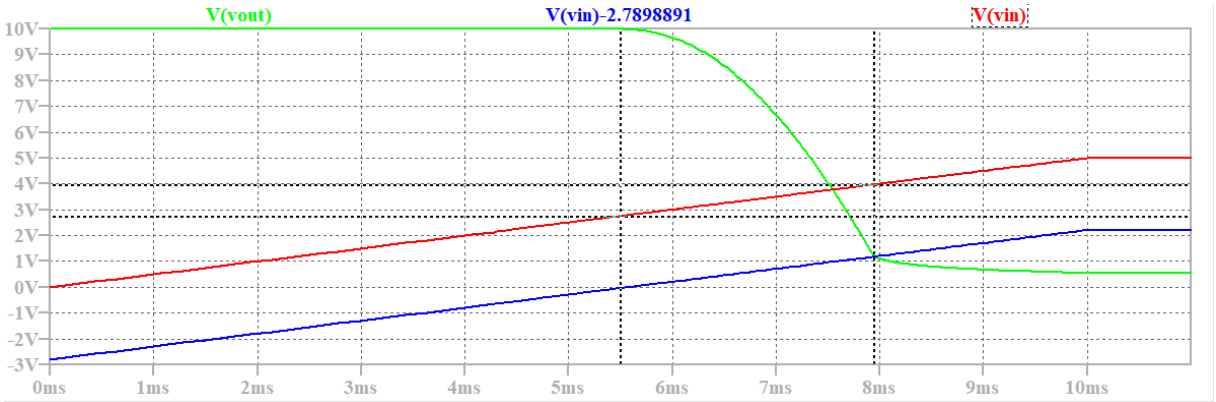
1.a) Build the inverter circuit given in Figure **1** using R_D **= 100 Ω** and V_{DD} **= 10 V**. Place a MOSFET using "**nmos**" symbol and select the MOSFET part number **BSS145**.

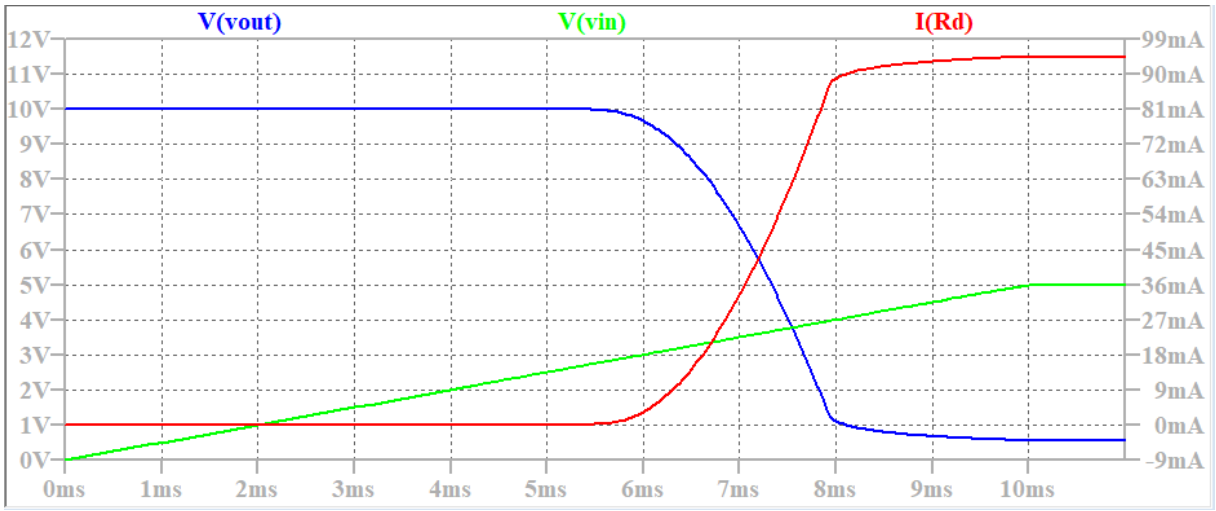
1.b) Use a ramp function (`PULSE(0 5 0 10m 1u 1m)`) as v_{in} that rises from **0 V** to **5 V** in **10 ms** and set simulation time to **10 ms**. Run simulation and display $v_{in} = v_{GS}$, $v_{out} = v_{DS}$ and $i_{RD} = i_D$ on the waveform window. Determine the v_{GS} threshold voltage V_{TN} and the drain current coefficient K_n based on the waveform plots.

V_{TN} =2.7898891V K_n = 66.946511mV-1/Ohm

>>To obtain K_n, if find out the saturation region which is when Vin is between 3.9767378V and 2.7484948V. Thus, I have chosen the middle point of it which is 3.36261 and according to this Vin value, I measured K_n with the equation of $K_n = i_D / (v_{in} - V_{TN})^2$.

(Saturation region)





1.c) Measure the drain current i_D for v_{in} = **3.0 V** and v_{in} = **3.5 V** on the plotted waveforms and fill in the following table. Calculate the drain current i_D again based on V_{TN} and K_n found above.

	i_D calculated in preliminary work	i_D measured on the plotted waveforms	i_D calculated based on V_{TN} and K_n above
v_{in} = **3.0 V**	50mA	3.3009239mA	2.95mA
v_{in} = **3.5 V**	88.48mA	33.344898mA	33.75mA

>>There is quite difference on the first column. Because, the V_{TN} and Kn values are note close to other two calculation.

2.a) Build the circuit in Figure **3** and apply an input ramp function as v_{in} that rises from **0 V** to **10 V**.

2.b) Run simulation and display v_{in}, $v_{GS} = v_G - v_S$, $v_{DS} = V_{DD} - v_S$ and $i_{RS} = i_D$ on the waveform window.

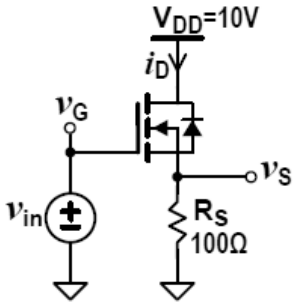
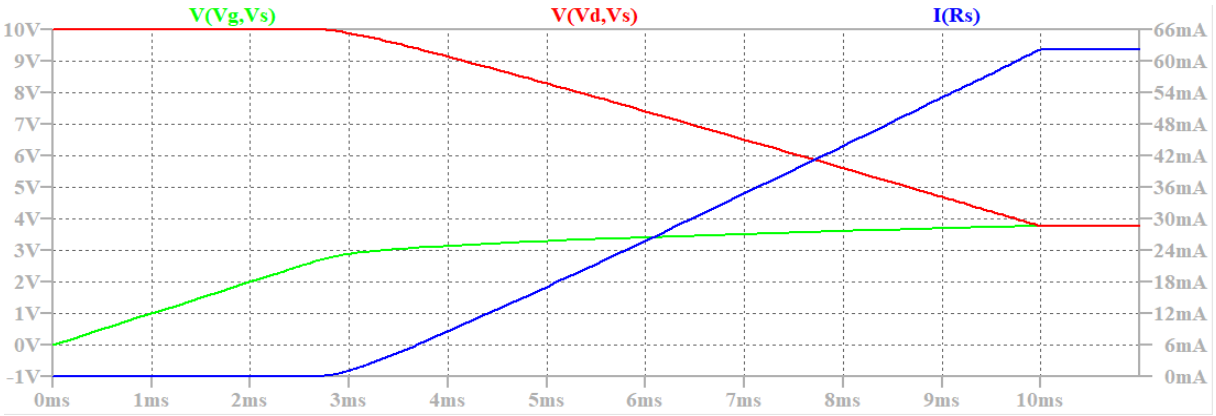
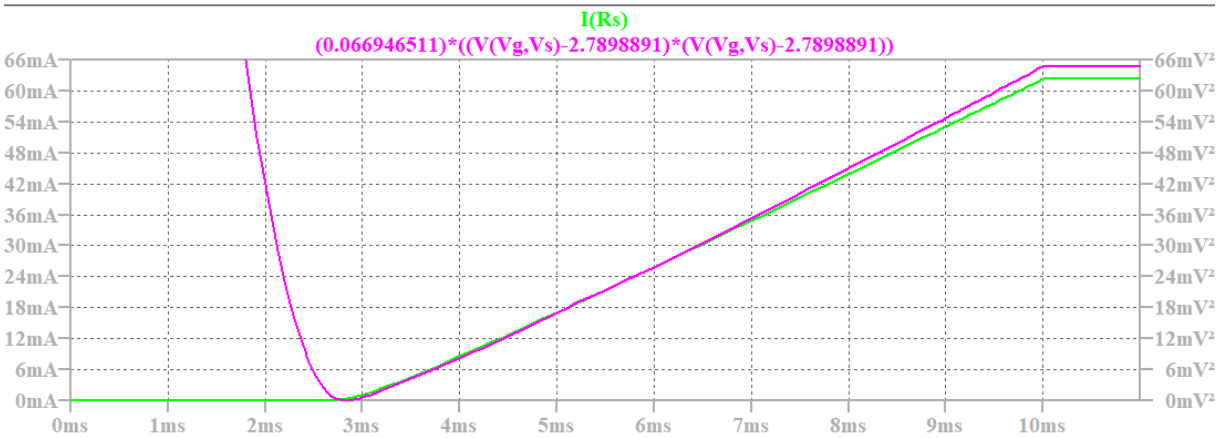


Figure 3



Verify that the values on drain current waveform can be calculated based on the V_{TN} and K_n values found above.



>>I used the equation of i_D with based on the V_{TN} and K_n values found above and I observed the almost same result.

2.c) Explain the linearized behavior of the drain current i_D as a function of the input voltage v_{in}.
Hint: Write i_D as a function of v_{in} and describe the feedback mechanism (if v_{in} rises then $i_{RS} = i_D$ increases ⇒ v_S rises ⇒ v_{GS} decreases ⇒ $i_{RS} = i_D$ decreases).

>>We can express v_{GS} as $v_G - v_S$ and $v_{in} - i_D * R_S$. Thus, our equation of i_D becomes, $i_D = K_n *(v_{in} - i_D * R_S - V_{TN})^2$. Which is telling us the same thing as the hint. When Vin increases, I_D increases and rise on I_D decreases V_{GS}. Because of this relationship, we do not observe quadratic growth, we see linear growth of i_D.

3.a) Build the circuit in Figure **4** using the resistor values you calculated in the preliminary work. Set v_{in} to obtain a **1 kHz** sinusoidal source with **1 Vpeak** amplitude.

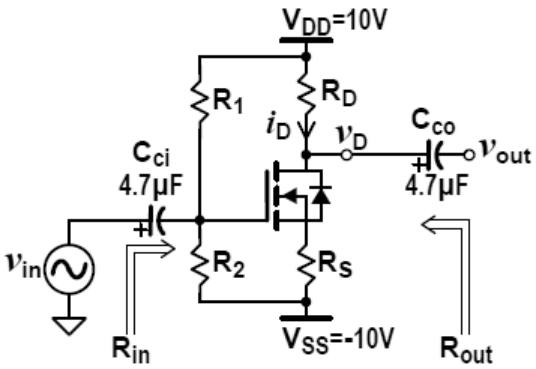


Figure 4

3.b) Run simulation and display v_{in}, v_{out}, v_D and $i_{RD} = i_D$ on the waveform window. Check the DC voltage at v_D and if necessary, adjust the resistor values to obtain a sinusoidal output without any clipping. If you changed any of the resistors, then explain why it was necessary.

Measure the output voltage and calculate the voltage gain.

V_{out} =7.9616836V A_v = 3.98

>>I changed R2 from 1.81kohm to 2.5kohm. Because, rise in R2 results V_G to increase due to the equation of $V_G = (V_{DD}-V_{SS})*R2/(R1+R2) + Vss$. When R2 was 1.81kohm, V_{GS} decreases under V_{TN}. Thus, we observe clipping on the output waveform.

3.c) Connect a **100 kΩ** resistor between the input voltage source and the coupling capacitor, **C_{ci}**. Measure the voltage gain and use the results from step **3.b** to deduce the amplifier input resistance, **R_{in}**.

>>V_G = Vin(Rin/(Rin+100k))

If we divide the same equation with the values above, 57.77 = (Rin + 100k)/Rin is found.

R_{in} = 1.931kohm

3.d) Measure the output resistance, **R_{out}**, of the amplifier.

R_{out} = 844ohm

3.e) Calculate **R_{in}** and **R_{out}** of the amplifier according to the circuit components and explain any deviations from the measured **R_{in}** and **R_{out}**.
>>Rin = R1||R2 = 8.19k||2.5k = 1.751kohm (%9.32 error)
>>Rout = R_D = 819ohm (%2.96 error)

Conclusion

>>In the first part of this experiment, we built an inverter NMOS circuit then we figured out how to find V_{TN} and K_n values of the transistor from the measurements and in **3c** we observed differences between preliminary work and simulation results. We saw pretty big difference, because the V_{TN} and K_n values are higher on preliminary work. On the other hand, when we use the values we found in simulation, we calculated pretty close results with small error.

In the second part of this experiment, we built another circuit and checked if our Kn value was consistent to the simulation and lastly we learned why we observe linear behavior of the drain current.

In the last part, we figured out how to find voltage gain, input resistance, output resistance from the simulation and by hand.