EE315 - Electronics Laboratory

Experiment - 3 Simulation
BJT Transistor and DC Biasing

Preliminary Work

1. For the circuit given in Figure **1**

a) Calculate the value of $\mathbf{R_{adj}}$ that makes $\mathbf{V_{CE}}$ equal to **5 V**.

b) Calculate $\mathbf{V_{RB}}$ (voltage drop accross $\mathbf{R_B}$).

c) Explain the reason for choosing $\mathbf{V_{CE}}$ equal to **5 V**.

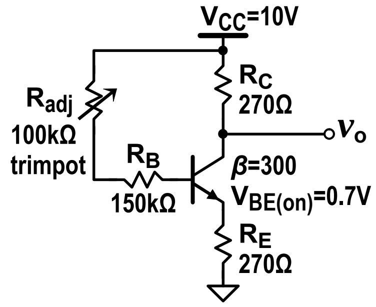


Figure 1. Emitter-stabilized bias circuit

2. For the circuit given in Figure **2**, determine $\mathbf{I_B}$, $\mathbf{I_C}$, $\mathbf{V_B}$, $\mathbf{V_E}$, and $\mathbf{V_{CE}}$.

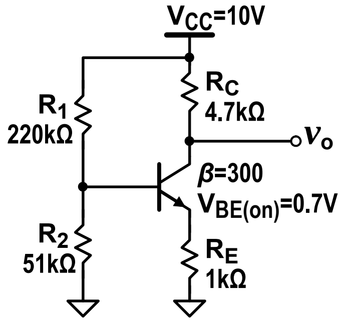


Figure 2. Voltage divider biasing circuit

3. For the circuit given in Figure **3**, derive an expression for $\boldsymbol{v_O = v_C}$ as a function of $\boldsymbol{v_{drv}}$. Specify the $\boldsymbol{v_{drv}}$ levels where the transistor turns off completely $(\boldsymbol{i_C = 0})$ and it goes into saturation $(\boldsymbol{i_C < \beta i_B})$.

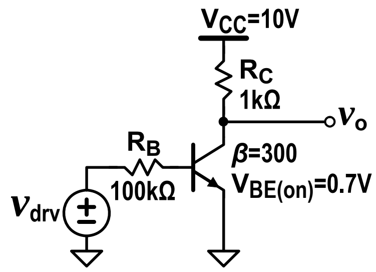


Figure 3. Switching circuit

4. For the circuit given in Figure **4**, find the values of $\mathbf{R_C}$ and $\mathbf{R_B}$, so that $\mathbf{I_{Csat} = 2\ mA}$ and $\boldsymbol{v_O}$ changes between **10 V** and **0 V** while $\boldsymbol{v_{drv}}$ is a **1 kHz** square wave signal switching between **0 V** and **10 V**.

Draw $\boldsymbol{v_{drv}}$ and $\boldsymbol{v_O}$ as a function of time.

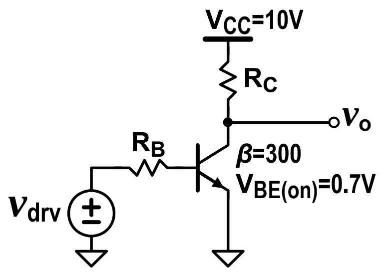


Figure 4. Switching circuit

Procedure

1. Build the circuit given in Figure **1**.
Place an NPN transistor on the schematic and select **BC547B** as the transistor model (right-click on the transistor figure and click on "Pick New Transistor").
You will use the same transistor model for all parts of the experiment.
Place a normal resistor as $\mathbf{R_{adj}}$ change its value until you obtain $\mathbf{V_{CE} = 5\ V}$ with less than **1%** error.

$\mathbf{R_{adj}}$ =

1.a) Measure $\mathbf{V_{BE}}$ and the voltages across $\mathbf{R_B}$, and $\mathbf{R_C}$ while $\mathbf{V_{CE}}$ is still at **5 V**. Also measure $\mathbf{I_B}$, $\mathbf{I_C}$, and $\boldsymbol{\beta}$.

$\mathbf{V_{BE}}$ = $\mathbf{V_{RB}}$ = $\mathbf{V_{RC}}$ =

$\mathbf{I_B}$ = $\mathbf{I_C}$ = $\boldsymbol{\beta}$ =

1.b) Change every one of the resistance values $\mathbf{R_B}$, $\mathbf{R_C}$, $\mathbf{R_E}$, and transistor parameters $\boldsymbol{\beta}$, and $\mathbf{V_{BE(on)}}$ by **1%** and record the new $\mathbf{I_C}$ values in the following table. Change only one of the resistor values or parameters at a time and keep the others at their original settings for each $\mathbf{I_C}$ measurement.

changed component	new value of I_C (mA)	percent change in I_C
R_B		
R_C		
R_E		
β		
$V_{BE(on)}$		

1.c) Which value(s) among $\mathbf{R_B}$, $\mathbf{R_C}$, $\mathbf{R_E}$, $\boldsymbol{\beta}$, and $\mathbf{V_{BE(on)}}$ has/have the most significant effect on $\mathbf{I_C}$?

2.a) Build the circuit in Figure **2**. Measure the values of $\mathbf{I_B}$, $\mathbf{I_C}$, $\mathbf{V_B}$, $\mathbf{V_{BE}}$, and $\mathbf{V_{CE}}$.

$\mathbf{I_B}$ = $\mathbf{I_C}$ = $\boldsymbol{\beta}$ =

$\mathbf{V_B}$ = $\mathbf{V_{BE}}$ = $\mathbf{V_{RC}}$ =

2.b) In practice, all component values are specified with a tolerance range. Tolerance range determines the minimum and maximum of the actual values that will be obtained if several of these components are tested. For example, a **100 kΩ** resistor with **5 %** tolerance may have an actual value between **95 kΩ** and **105 kΩ** . Similarly, the minimum and maximum values of $\boldsymbol{\beta}$ are given in transistor datasheets.

If thousands of this circuit are to be manufactured, then you had to make sure that $\mathbf{V_{CE}}$ will be reasonable within the tolerance range of all components. Indicate in the table below, which end ("**min**" or "**max**") of the tolerance range should be used for each parameter in calculation of the lowest and highest values of $\mathbf{V_{CE}}$.

component or parameter	For lowest V_{CE}	For highest V_{CE}
R_1		
R_2		
R_C		
R_E		
β		
$V_{BE(on)}$		

3.a) Build the circuit given in Figure **3**. Use a pulse waveform as v_{drv} that changes from **0 V** to **10 V** in **1 ms** (i.e. `PULSE(0 10 0 1m 1u 1m 3m)`).

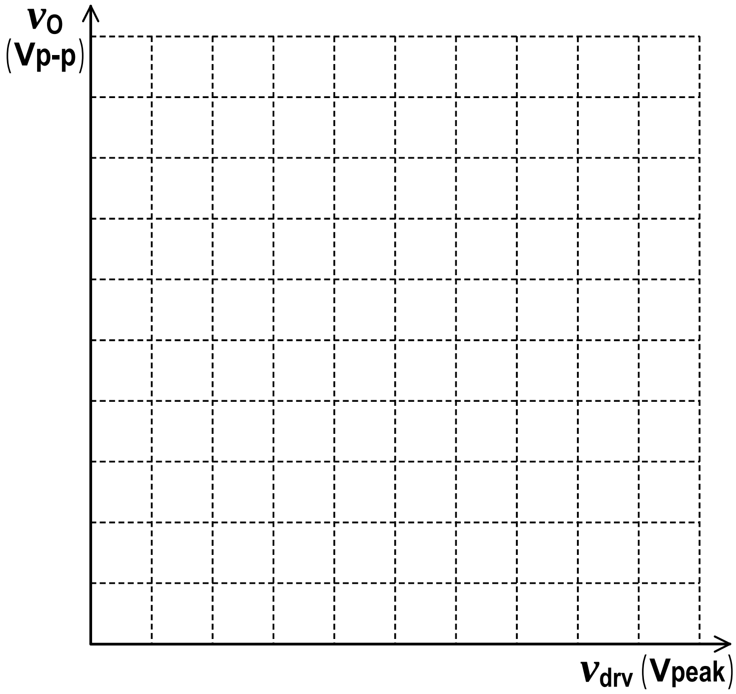
3.b) Measure the range of v_{drv} values in which the transistor acts as a switch.

$v_{drv\text{-}Low\text{-}Max}$ = (where v_O **> 90% of** V_{CC})

$v_{drv\text{-}High\text{-}Min}$ = (where v_O **< 10% of** V_{CC})

4.a) Setup the circuit in Figure **4** using the $\mathbf{R_B}$ and $\mathbf{R_C}$ values previously calculated in the preliminary work. Set v_{drv} source timing parameters to obtain a **10 kHz** pulse signal with **50 %** duty cycle (i.e. `PULSE(0 10 0 1u 1u 49u 100u)`). Keep the v_{drv} source **Trise** and **Tfall** settings at **1 µs** all the time. Set simulation time long enough to observe the steady state v_O waveform. Change the peak voltage of v_{drv} as in the following table and record the peak-to-peak v_O voltage.

Freq. (kHz)	v_{drv} (Vpeak)	v_O (Vp-p)
10	2	
	4	
	6	
	8	
	10	
	2	
	4	
	6	
	8	
	10	



4.b) Set v_{drv} peak voltage to **10 V** and increase v_{drv} frequency (reduce **Ton** and **Tperiod**) until the peak-to-peak v_O voltage decreases down to **5 V** roughly. Make sure that duty cycle of the v_{drv} remains as **50%** while the **Trise** and **Tfall** settings are **1 µs** all the time. Measure v_O for the other v_{drv} peak voltage settings and record the results in the table above. Plot v_O amplitude (**Vp-p**) versus v_{drv} (**Vpeak**) for the two freuency settings.

4.c) Comment on the difference in the output signals resulting from the changes in v_{drv} peak voltage and frequency.