EE315 - Electronics Laboratory

Experiment - 3 Simulation
BJT Transistor and DC Biasing

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Preliminary Work

1=> C-E KVL

$270 \times \beta \times i_B + 5 + 270 \times (\beta+1) \times i_B = 10$

$i_B \cong 30 \mu A$

B-E KVL $V_x = R_{adj} \times i_B$

$V_x + 150k \times i_B + 0.7 + 270 \times (\beta+1) \times i_B = 10$

$V_x = 2.36$

a => $R_{adj} \cong 78.67k$

b => $V_{RB} = 150k + 30\mu = 4.5V$

c => Because when $V_{CE} = 5V$ the circuit is in Quiescent point which is in the middle point of the active mode range. $\frac{10-0}{2} = 5V$.

2=> $V_{Th} = 10 \times \frac{51}{220+51} = 1.88V$

$R_{Th} = 220k // 51k = 41.4k\Omega$

B-E KVL

$V_{Th} = 41.4k \times i_B + 0.7V + 1k \times (\beta+1) \times i_B$

$I_B = 3.45 \mu A$

$I_C = I_B \times 300 = 1.035 mA$

$V_B = 1.88 - 41.4k \times 3.45\mu = 1.737V$

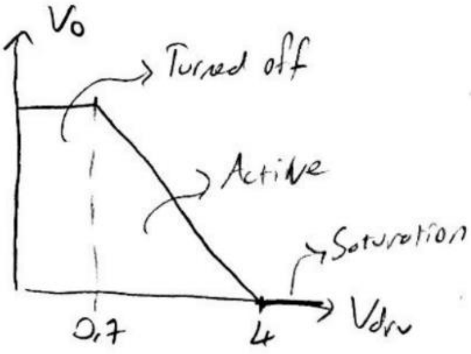
$V_E = 1k \times I_B \times (\beta+1) = 1.038V$

$V_{CE} = 10V - 4.7k \times I_B \times \beta - V_E = 4.088V$

3 => $V_{CE(sat)} = 0$

$I_C \geqslant 10mA \Rightarrow i_C < \beta i_B$

$I_B \geqslant 33\mu A$ and $V_{drv} \geqslant 4$ } In Saturation



$$i_B = \frac{V_{drv} - 0.7}{100k}$$

$$V_o = 10 - 1k \times i_B \times \beta$$

$$\vdots$$

$$V_o = 12.1 - 3V_{drv}$$

4 => $R_C \times I_{C(sat)} = 10V \Rightarrow R_C = 5k\Omega$

$0 \leq V_o \leq 10 \iff 0 \leq I_C \leq 2mA$

$V_{drv} = 0 \Rightarrow I_C = 0 \, , \, V_o = 10V$

$V_{drv(max)} = R_B \times \frac{2mA}{\beta} + 0.7$

$R_B = \frac{9.3}{2m} \times 300 = 1.395M\Omega$

Results

1. Build the circuit given in Figure **1**.
Place an NPN transistor on the schematic and select **BC547B** as the transistor model (right-click on the transistor figure and click on "Pick New Transistor").
You will use the same transistor model for all parts of the experiment.
Place a normal resistor as $\mathbf{R_{adj}}$ change its value until you obtain $\mathbf{V_{CE} = 5\ V}$ with less than **1%** error.

$\mathbf{R_{adj}}$ **=60.502k**

1.a) Measure $\mathbf{V_{BE}}$ and the voltages across $\mathbf{R_B}$, and $\mathbf{R_C}$ while $\mathbf{V_{CE}}$ is still at **5 V**. Also measure $\mathbf{I_B}$, $\mathbf{I_C}$, and $\boldsymbol{\beta}$.

$\mathbf{V_{BE}}$ **=700.60444mV** $\mathbf{V_{RB}}$ **=4.842024V** $\mathbf{V_{RC}}$ **=2.4956417V**

$\mathbf{I_B}$ **=32.280161µA** $\mathbf{I_C}$ **=9.2431172mA** $\boldsymbol{\beta}$ **=286.34049**

1.b) Change every one of the resistance values $\mathbf{R_B}$, $\mathbf{R_C}$, $\mathbf{R_E}$, and transistor parameters $\boldsymbol{\beta}$, and $\mathbf{V_{BE(on)}}$ by **1%** and record the new $\mathbf{I_C}$ values in the following table. Change only one of the resistor values or parameters at a time and keep the others at their original settings for each $\mathbf{I_C}$ measurement.

changed component	new value of $\mathbf{I_C}$ (mA)	percent change in $\mathbf{I_C}$
$\mathbf{R_{B+\%1}}$	9.1998833mA	‰4.68
$\mathbf{R_{C+\%1}}$	9.2406501mA	‰0.270
$\mathbf{R_{E+\%1}}$	9.2182383mA	‰2.69
$\boldsymbol{\beta}_{\mathbf{+\%1}}$	9.4211837mA	‰19.25
$\mathbf{V_{BE(on)\ +\%1}}$	9.2361631mA	‰0.757

1.c) Which value(s) among $\mathbf{R_B}$, $\mathbf{R_C}$, $\mathbf{R_E}$, $\boldsymbol{\beta}$, and $\mathbf{V_{BE(on)}}$ has/have the most significant effect on $\mathbf{I_C}$?

>>As we can see from the table above, $\boldsymbol{\beta}$ value has the most significant effect on $\mathbf{I_C}$. Because increment on $\boldsymbol{\beta}$ directly increases $\mathbf{I_C}$ then other variables.

2.a) Build the circuit in Figure **2**. Measure the values of I_B, I_C, V_B, V_{BE}, and V_{CE}.

I_B =3.6623608µA **I_C =1.0867461mA** **β =296.73376**

V_B =1.7302889V **V_{BE} =639.88048mV** **V_{RC} =5.1077065V**

2.b) In practice, all component values are specified with a tolerance range. Tolerance range determines the minimum and maximum of the actual values that will be obtained if several of these components are tested. For example, a **100 kΩ** resistor with **5 %** tolerance may have an actual value between **95 kΩ** and **105 kΩ** . Similarly, the minimum and maximum values of β are given in transistor datasheets.

If thousands of this circuit are to be manufactured, then you had to make sure that V_{CE} will be reasonable within the tolerance range of all components. Indicate in the table below, which end ("**min**" or "**max**") of the tolerance range should be used for each parameter in calculation of the lowest and highest values of V_{CE}.

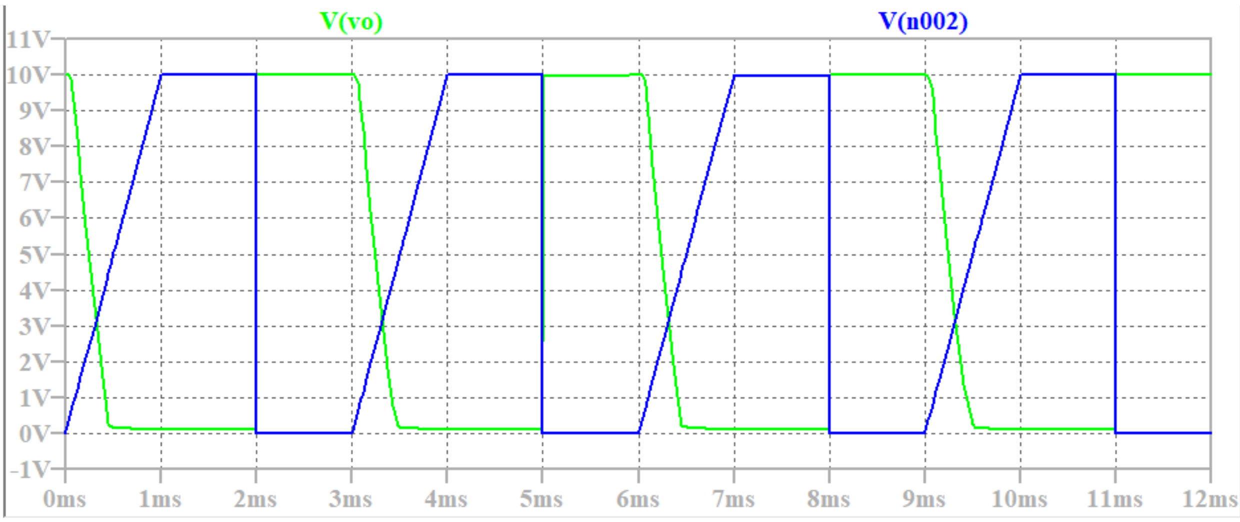
component or parameter	For lowest V_{CE}	For highest V_{CE}
R_1	min	max
R_2	max	min
R_C	max	min
R_E	min	max
β	max	min
$V_{BE(on)}$	min	max

3.a) Build the circuit given in Figure **3**. Use a pulse waveform as v_{drv} that changes from **0 V** to **10 V** in **1 ms** (i.e. `PULSE(0 10 0 1m 1u 1m 3m)`).

3.b) Measure the range of v_{drv} values in which the transistor acts as a switch.

$v_{drv\text{-}Low\text{-}Max}$ =0 to 839.16084mV (where v_O > 90% of V_{CC})

$v_{drv\text{-}High\text{-}Min}$ =3.986014V to 10V (where v_O < 10% of V_{CC})

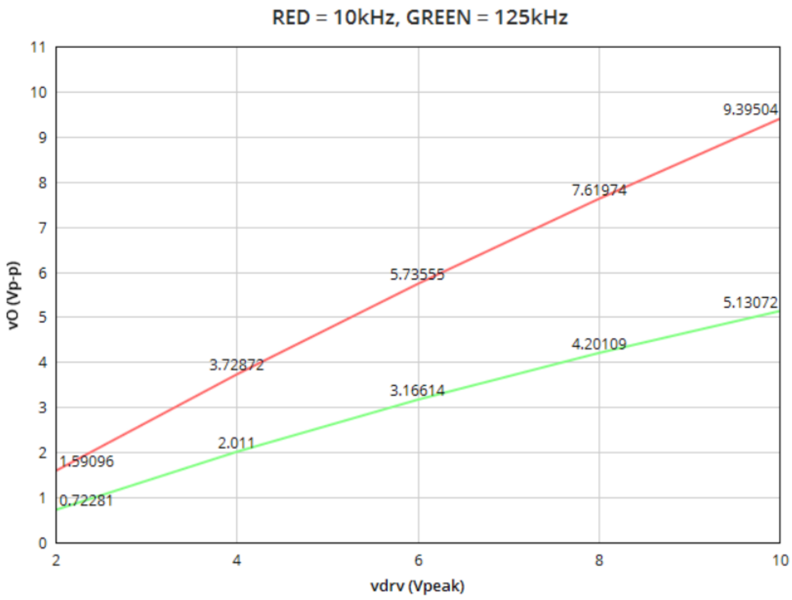


(Green line is Vout, Blue line is Vdrv)

4.a) Setup the circuit in Figure **4** using the **R_B** and **R_C** values previously calculated in the preliminary work. Set ***v_{drv}*** source timing parameters to obtain a **10 kHz** pulse signal with **50 %** duty cycle (i.e. `PULSE(0 10 0 1u 1u 49u 100u)`). Keep the ***v_{drv}*** source **Trise** and **Tfall** settings at **1 μs** all the time. Set simulation time long enough to observe the steady state ***v_O*** waveform. Change the peak voltage of ***v_{drv}*** as in the following table and record the peak-to-peak ***v_O*** voltage.

>>There is a small difference from input to output because of V_{BE}.

Freq. (kHz)	v_{drv} (Vpeak)	v_O (Vp-p)
10	2	1.59096V
	4	3.72872V
	6	5.73555V
	8	7.61974V
	10	9.39504V
125	2	0.72281V
	4	2.01100V
	6	3.16614V
	8	4.20109V
	10	5.13072V



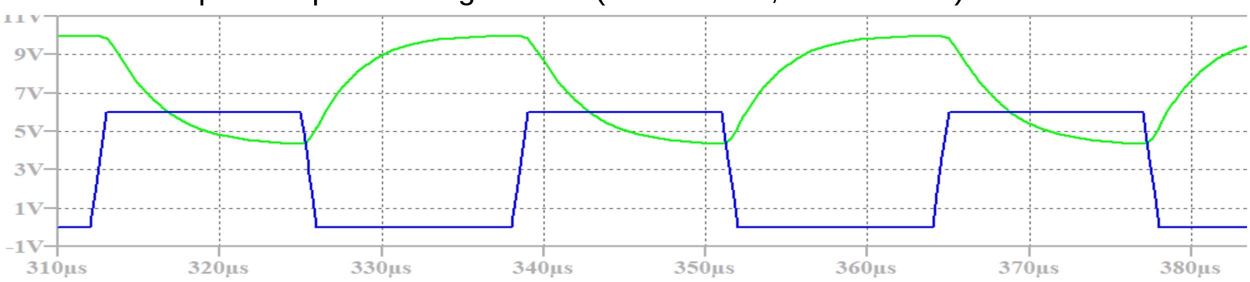
4.b) Set ***v_{drv}*** peak voltage to **10 V** and increase ***v_{drv}*** frequency (reduce **Ton** and **Tperiod**) until the peak-to-peak ***v_O*** voltage decreases down to **5 V** roughly. Make sure that duty cycle of the ***v_{drv}*** remains as **50%** while the **Trise** and **Tfall** settings are **1 μs** all the time. Measure ***v_O*** for the other ***v_{drv}*** peak voltage settings and record the results in the table above. Plot ***v_O*** amplitude (**Vp-p**) versus ***v_{drv}*** (**Vpeak**) for the two freuency settings.

>>I plotted above with the green line.

4.c) Comment on the difference in the output signals resulting from the changes in ***v_{drv}*** peak voltage and frequency.

>>For 4a we can formulize Vo with Vo = 10 – R_C * (V_{drv} – V_{BE})/R_B * β . Thus, when we increase the peak to peak voltage of V_{drv}, We obtain greater range of Vo which is the same thing as $Vo_{(peak-peak)}$. Due to this relationship,peak to peak voltage of Vo and V_{drv} are inversely proportional.

On the other hand, transistors are not responding to the signal instantaneously as we can see below. That's why, when we increase the frequency of V_{drv}, we are able to decrease the peak to peak voltage of Vo. (Green = Vo, Blue = Vdrv)



Conclusion

>>In the first experiment, we figured out how to measure the various values on the thansistor circuit and we saw which variable has the most significant effect on the collector current.

In the second experiment, we find out how components values affects the V_{CE} value. The relationship is proportional, for lowest V_{CE} value, we need the lowest value of the component. However, if it is inversely proportional, the relationship is exactly the opposite. This improved our approach on tolerance values.

In the third experiment, we observed the relation between Vdrv and Vcc on transitor switch circuit.

In the last experiment, we saw how a frequency and peak to peak voltage of Vdrv affects the behavior of the Vo. We observed that the bjt transistor has a switching speed which is called slew rate and it acts as a capacitor. It is more observable when we have high output impedance. When the driving signal is applied to the transistor input, some time is needed to charge the emiter-junction transition capacitance. Because of this delay time or transit time, we saw smaller peak to peak Vo voltage when there is high frequency.