Analysis and Design of High Speed Residue to Binary Reverse Converter for the Moduli Set {2n+ 1, 2n, 2n- 1}

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***Abstract*— Residue Number System (RNS) has the specific feature to perform addition, subtraction independently with carry-free propagation. In RNS, conversion is of two types: Forward Conversion and Reverse Conversion. Chinese Remainder Theorem (CRT) and Mixed Radix Conversion (MRC) are the two extensively used techniques adapted for reverse conversion and in this case, CRT is proved faster than MRC. This paper proposes a residue to binary reverse converter for three moduli set {2n+ 1, 2n, 2n- 1} by modifying the CRT. It is simplified in order to design a reverse converter that does not require modular operations. The operations required in the existing designs are mod (2n) mod (2n - 1) and mod (2n- 1) operations. The proposed design provides better results in terms of power, area, delay and number of cells over the existing CRT design and does not require mod operations which are however necessary in the existing CRT technique. This design has been simulated using NC Launch - Encounter tool in Cadence.**

Keywords - Residue Number System; Moduli Set; Forward Conversion; Reverse Conversion; Mixed Radix Conversion and Chinese Remainder Theorem.

I. INTRODUCTION

A non-weighed number system, Residue Number System provides the single step multiplication, carry-free addition and borrow-free subtraction [1]-[6]. Data conversion and moduli selection are the primary factors that determines the performance of RNS hardware and may limit the use of RNS in DSP applications [7]. RNS is used in digital signal processing applications i.e., digital filtering and convolutions [8].

Figure 1. General structure of RNS processor

The RNS operation is performed in three stages and the structure is shown in Fig. 1 [9]. They are (i). Forward Conversion, (ii). Modulo Channels, (iii). Reverse Conversion. Reverse conversion is of two types: Chinese Remainder Theorem (CRT), Mixed Radix Conversion (MRC). The CRT based conversion is parallel process where as MRC is a sequential process. MRC is a weighted system, used to implement the magnitude of comparison which is problematic in RNS [7]. In CRT, the limitations are the complex and delayed modulo (mod)-M operations [10]-[19]. The existing designs depend on mod (2n + 1) mod (2n - 1), mod (2n) mod (2n - 1) and mod (2n- 1) operations for the three moduli set [20]-[27]. An efficient reverse converter is proposed in this paper which does not require the mod operations for the moduli set.

The remaining sections of the paper are designed as follows. In section II, the conventional design, Proposed design, Simulated and RTL schematic results are presented in section III and IV respectively. Finally, the conclusion is drawn in section V.

II. CONVENTIONAL DESIGN

The reverse conversion is the process of converting the residue representations to binary/decimal conventional notations.

A. Mixed Radix Conversion

In the mixed radix conversion, each of the weight determines a distinct radix. The radices are m_n, $m_{n-1}\ldots m_1$, residue representation (r_n, r_{n-1}, $r_{n-2}\ldots r_1$) and number X can be expressed as [9]

$$X = (Z_n, Z_{n-1}, Z_{n-2}\ldots Z_1)$$

$$X = Z_n m_{n-1} m_{n-2} \ldots\ldots m_1 + \ldots.. + Z_3 m_2 m_1 + Z_2 m_1 + Z_1 \quad (1)$$

$$Z_1 = r_1$$

$$Z_2 = ||m_1^{-1}|_{m2} (r_2 - z_1)|_{m2} \text{ and so on}$$

$$Z_n = |(m_1 m_2 \ldots m_{n-1})^{-1}|m_n |(r_n - (r_{n-1} m_{n-2} \ldots . Z_2 m_1 + Z_1))|m_n$$

B. Chinese Remainder Theorem

In Chinese remainder theorem, (r_1, r_2, and r_3) are the residue representations of X with prime moduli m_1, m_2, m_3 and represented as [9]

$$|X|_M = |\sum_{i=1}^{N} ri \; |M_i^{-1}|m_i M_i|_M \quad (2)$$

where M is the dynamic range

$M = m_1.m_2.m_3$

The simplified expression of equation (2) is

$$|X|_M = |\frac{M}{2}(r_1 + r_3) + \frac{m_2 m_3}{2} - m_1 m_3 r_2 + \frac{m_1 m_2}{2} r_3|_M \quad (3)$$

The term ($r_1 + r_3$) can be either even or odd in the above equation (3).

If ($r_1 + r_3$) is odd, then

$$\left|\frac{M}{2}(r_1 + r_3)\right|_M = \frac{M}{2}$$

The equation can be rewritten as

$$|X|_M = |\frac{M}{2} + \frac{m_2 m_3}{2} - m_1 m_3 r_2 + \frac{m_1 m_2}{2} r_3|_M \quad (4)$$

If ($r_1 + r_3$) is even, then

$$\left|\frac{M}{2}(r_1 + r_3)\right|_M = 0$$

The equation can be rewritten as

$$|X|_M = |\frac{m_2 m_3}{2} - m_1 m_3 r_2 + \frac{m_1 m_2}{2} r_3|_M \quad (5)$$

According to [2], the simplified equations of (4) and (5) are as follows that uses mod (2n) mod (2n-1) operations in the process and the design is shown in Fig. 2.

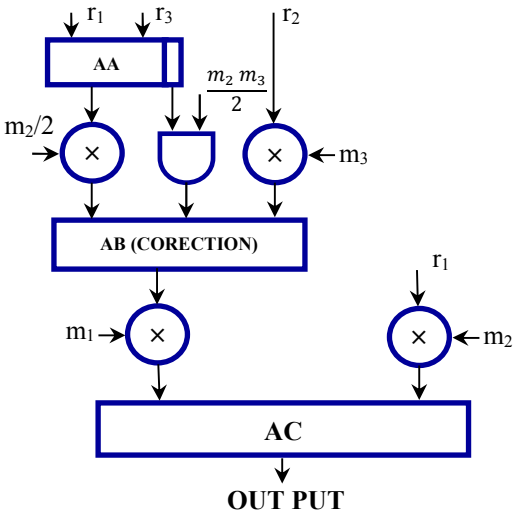

Figure 2. Structure of existing reverse converter [2]

If ($r_1 + r_3$) is odd, then

$$X = -m_2 r_1 + m_1 |\frac{m_2 m_3}{2} + \frac{m_2}{2}\left(\frac{r_1 + r_3}{2}\right) - m_3 r_2|_{m_2 m_3} \quad (6)$$

If ($r_1 + r_3$) is even, then

$$X = -m_2 r_1 + m_1 |\frac{m_2}{2}\left(\frac{r_1 + r_3}{2}\right) - m_3 x_2|_{m_2 m_3} \quad (7)$$

In adder AA, the inputs r_1 and r_3 are added and multiplied with $m_2/2$ which is one of the input to adder AB. The remaining inputs are one from multiplier $m_3(-m_3 r_2)$ and $m_2 m_3/2$. The output is multiplied with m_1 and provided as one of the input to adder AC. The output from the multiplier $m_2(m_2 r_1)$ is the other input to adder AC in which subtraction takes place to provide desired result.

According to [1], the simplified equations of (6) and (7) are as follows based on lemma given $|am_1|_{m1m2} = m_1 |a|_{m2}$ and $m_3 = m_2 - 1$ in the existing structure to perform mod 2n-1 operation and structure is shown in Fig. 3 [1].

If ($r_1 + r_3$) is odd,

$$X = m_2(r_2 - r_1) + r_2 + (m_1 m_2(|\frac{m_3}{2} + \left(\frac{(r_1 + r_3)}{2} - r_2\right)|_{m_3}) + m_3) \quad (8)$$

If ($r_1 + r_3$) is even,

$$X = m_2(r_2 - r_1) + r_2(m_1 m_2(|\left(\frac{(r_1 + r_3)}{2} - r_2\right)|_{m_3}) + m_3) \quad (9)$$

In Adder A, the residue r_1 is subtracted from r_2 and multiplied with m_2. The 3:2 carry save adder is used to implement Adder B to compute $((r_1 + r_3)/2 - r_2)$ with carry propagate adder. To compute mod $-m_3$ with the addition of $m_3/2$ and m_3, one corrective addition or subtraction is required and which is implemented by Adder C with the selection line from the comparator that compares the output.

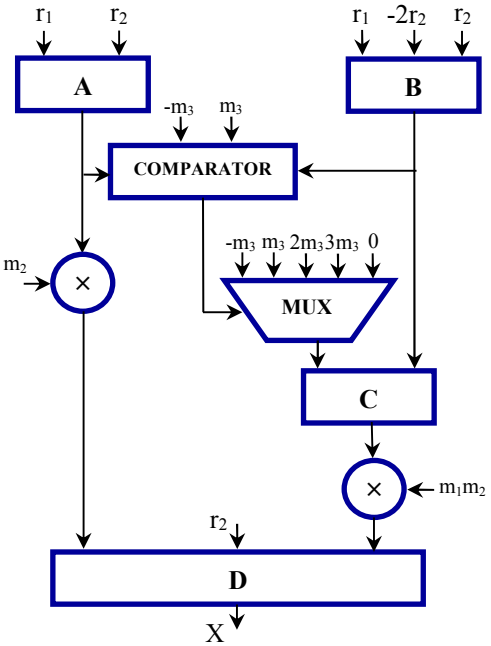

Figure 3. Structure of existing reverse converter [1]

The result is multiplied with $m_1 m_2$ which are added with inputs r_2 and onefrom the multiplier m_2 at Adder D. The adder D performs mod-M operation to the output.The output of adder D is the desired decimal equivalent of residues. The drawbacks in the existing design are more of hardware, power and area due to mod (2n-1) operation. A design has been proposed to install reduce power, hardware and area.

III. PROPOSED DESIGN

The existing design is based on mod (2n-1) operation which has limitation in the design that requires more hardware, power and area.

The equations (8) and (9) can be modified, which does not require the mod operations in the conversion processby

applying the mod operation. Thus, it reduces the complexity, power and area. The structure of proposed reverse converter is shown in Fig.4. The modified equations are as follows:

If $(r_1 + r_3)$ is odd,

$$X = m_2(r_2 - r_1) + r_2 + m_1 m_2\left(\frac{m_3}{2} + \left(\frac{(r_1+r_3)}{2} - r_2\right)\right) \quad (10)$$

If $(r_1 + r_3)$ is even,

$$X = m_2(r_2 - r_1) + r_2 + m_1 m_2\left(\frac{(r_1+r_3)}{2} - r_2\right) \quad (11)$$

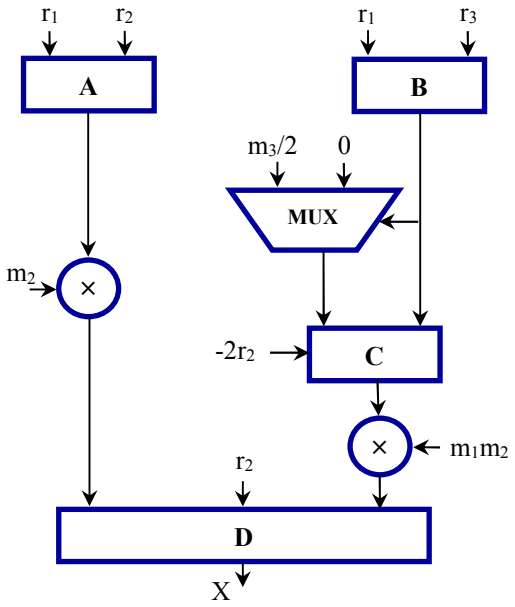

Figure 4. Structure of proposed reverse converter

In the proposed design, the residue r_2 is subtracted from r_1 at Adder A and is multiplied with m_2. Adder B is the ripple carry adder which has inputs r_1 and r_3. The LSB of output is used as selection input to multiplexer that provides either $m_3/2$ or 0 as output. The result is added with output of adder B and input $2r_2$. This result is multiplied with m_1m_2 which is given as one of the inputs of adder D. The other inputs are r_2 and output of multiplier m_2 that produces the output which is desired decimal equivalent. The examples are shown below for both cases in the proposed design.

IV. Simulation and RTL Schematic Results

The proposed design is simulated in NC launch simulation analysis environment (Sim-vision) using Cadence. The RTL schematic of existing and proposed reverse converters are shown in Fig. 5, 6 and 7. The number of components in the proposed design is less than the existing design form Fig. 5 and 6. Table.1 shows the comparision of conventionalreverse converters[1], [2], [3] in VHDL and implementing them on Xilinx Spartan 3 FPGA with Xilinx ISE 10.0.03 and theproposed design in Encounter tool for the moduli set {2n+1, 2n, 2n-1}. It is observed that from Table. 1, the proposed design has low power, delay and area than conventional designs.

The proposed design has been implemented in Cadence Encounter Digital Implementation RTL to GDSII system. The cell area for proposed reverse converter is shown in Table.1.

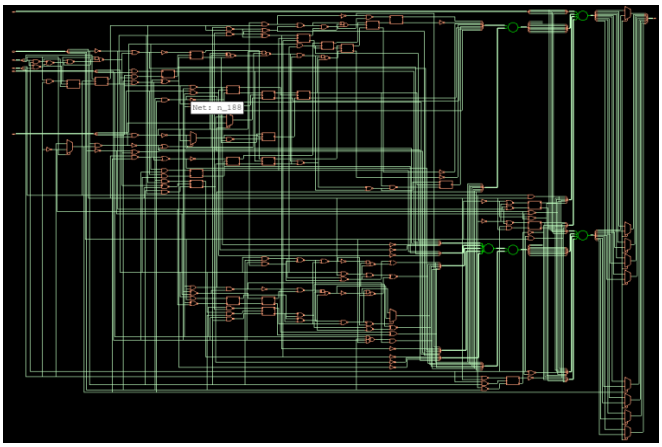

Figure 5. RTL Schematic of existing reverse converter [2].

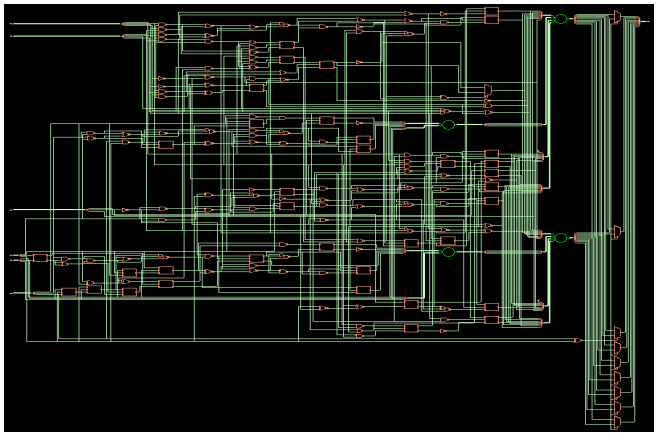

Figure 6. RTL Schematic of existing reverse converter [1].

TABLE 1. COMPARISON OF CONVENTIONALREVERSE CONVERTERSAND PROPOSED REVERSE CONVERTERIN VHDL XILINX ISE.

n	Proposed			[1]			[2]			[3]		
	Area (μm^2)	Delay (ps)	Power (mW)	Area (slices)	Delay (ps)	Power (mW)	Area (slices)	Delay (ps)	Power (mW)	Area (slices)	Delay (ps)	Power (mW)
4	2669.586	3935	0.207	28	19857	15	49	31865	16	41	28575	15
21	4938.772	6767	0.428	90	36262	19	121	44718	20	126	44999	22
129	12264.807	9721	1.848	101	37599	19	136	42329	22	141	41312	24
813	15335.550	12256	2.426	251	45543	33	328	53556	37	305	55609	42
32769	30964.021	17800	5.940	177	39256	25	218	44896	28	253	47955	34
1321123	49469.469	22862	11.187	589	57261	65	749	65295	68	735	71930	95

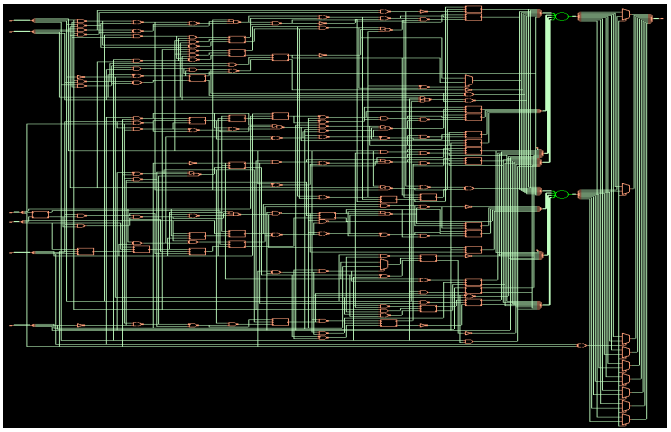

Figure 7. RTL Schematic of proposed reverse converter.

V. CONCLUSION

The proposed reverse converter does not require mod operations. This design has been proved advantageous in terms of power, cells, high speed and cell area over the existing ones. Table 1 demonstrates that the proposed structure provides low power, high speed and less area for implementing 90 nm technology. This RNS reverse conversion is used in the filtering and convolution process of DSP applications to minimize the faults and complexity.

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