ELP 831
IEC LAB-1

Report

MOD-5 Counter
RTL to GDSII

Submitted By:

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EEN212020

https://github.com/een212020/Task-1.git

Verilog

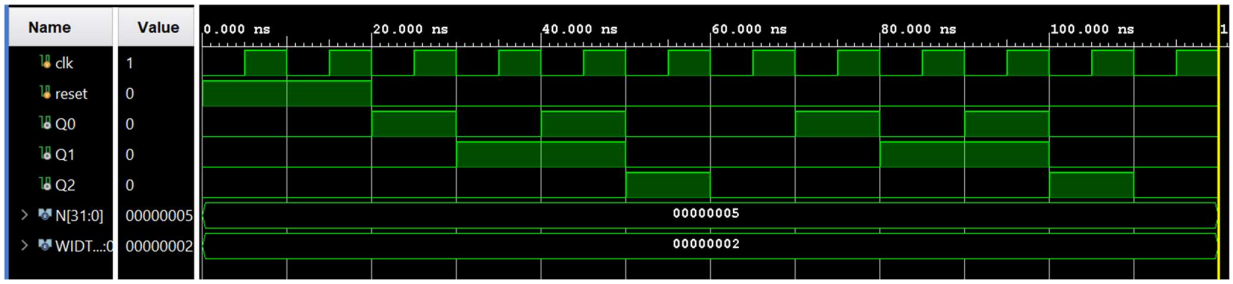
Code:

```
1   `timescale 1ns / 1ps
2
3   module mod5_counter(clk, reset, Q0, Q1, Q2);
4       parameter N = 5;
5       parameter WIDTH = 2;
6       input clk;
7       input reset;
8       reg [WIDTH:0] y;
9       output reg Q0, Q1, Q2;
10
11      initial
12      y = 0;
13
14      always @ (negedge clk)
15      begin
16          if (reset)
17              y <= 0;
18          else if (y==N-1)
19              y <= 0;
20          else
21              y <= y+1;
22      end
23
24      always @ (y)
25      begin
26          Q0 <= y[0];
27          Q1 <= y[1];
28          Q2 <= y[2];
29      end
30  endmodule
```

Testbench:

```
1   `timescale 1ns / 1ps
2
3   module testbench;
4       parameter N = 5;
5       parameter WIDTH = 2;
6
7       reg clk;
8       reg reset;
9       wire Q0, Q1, Q2;
10
11      initial begin
12          clk = 0 ;
13          reset = 1; #20;
14          reset = 0; #100;
15          $monitor("T = %0t Reset = %0b OUT = %0b %0b %0b", $time, reset, Q2, Q1, Q0);
16
17          $finish;
18      end
19
20      mod5_counter DUT(.clk(clk), .reset(reset), .Q0(Q0), .Q1(Q1), .Q2(Q2));
21
22      always #5 clk = ~clk;
23
24  endmodule
25
```

Waveform:


Name
Value
0.000 ns
20.000 ns
40.000 ns
60.000 ns
80.000 ns
100.000 ns
clk
1
reset
0
Q0
0
Q1
0
Q2
0
N[31:0]
00000005
00000005
WIDT...:0
00000002
00000002

Physical Design

File Path: /afs/iitd.ac.in/user/e/ee/een212020//Physical/MOD5Counter

Process:

- Synthesis Without DFT
    - TCL file: **counter.tcl**

```
set search_path "/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs"
set_attribute lib_search_path "/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs"
set_attribute hdl_search_path "./rtl/"
set_attribute library "uk65lscllmvbbr_100c25_tc_ccs.lib"

read_hdl counter.v
elaborate
check_design -unresolved
read_sdc ./synthesis/counter_sdc.sdc
synthesize -to_mapped -effort medium
write_hdl > ./typical/counter_netlist.v
write_sdc > ./typical/counter.sdc
```

    - SDC file: **counter_sdc.sdc**

```
set sdc_version 1.7

set_units -capacitance 1000.0fF
set_units -time 1000.0ps

# Set the current design
current_design counter

create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainity 0.1 [get_ports "clk"]
set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clk"]

set_wire_load_mode "top"
```

    - Starting tool

```
source ~/.bashrc
load_module encounter
rc
```

    -

```
legacy_genus:/> source ./synthesis/counter.tcl
```

- Generated Netlist

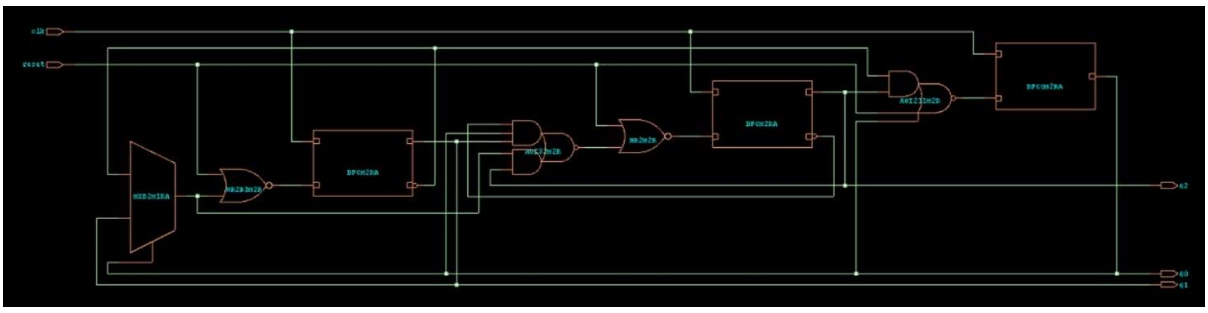
```
// Generated by Cadence Genus(TM) Synthesis Solution 19.12-s121_1
// Generated on: Oct 16 2021 20:44:54 IST (Oct 16 2021 15:14:54 UTC)

// Verification Directory fv/counter

module counter(clk, reset, Q0, Q1, Q2);
  input clk, reset;
  output Q0, Q1, Q2;
  wire clk, reset;
  wire Q0, Q1, Q2;
  wire n_0, n_1, n_2, n_3, n_4, n_5, n_6;
  NR2M2R g198(.A (reset), .B (n_5), .Z (n_6));
  AOI32M2R g200(.A1 (n_0), .A2 (Q0), .A3 (Q1), .B1 (n_3), .B2 (Q2), .Z
       (n_5));
  NR2B1M2R g202(.B (reset), .NA (n_3), .Z (n_4));
  DFCQM2RA \y_reg[0] (.CKB (clk), .D (n_2), .Q (Q0));
  MXB2M1RA g204(.A (n_1), .B (Q1), .S (Q0), .Z (n_3));
  AOI211M2R g203(.A1 (n_1), .A2 (Q2), .B (reset), .C (Q0), .Z (n_2));
  DFCM2RA \y_reg[1] (.CKB (clk), .D (n_4), .Q (Q1), .QB (n_1));
  DFCM2RA \y_reg[2] (.CKB (clk), .D (n_6), .Q (Q2), .QB (n_0));
endmodule
```

- Generated sdc file

```
# ###############################################################################

#  Created by Genus(TM) Synthesis Solution 19.12-s121_1 on Sat Oct 16 20:44:54 IST 2021

# ###############################################################################

set sdc_version 2.0

set_units -capacitance 1000fF
set_units -time 1000ps

# Set the current design
current_design counter

create_clock -name "clk" -period 10.0 -waveform {0.0 5.0} [get_ports clk]
set_clock_transition 0.1 [get_clocks clk]
set_clock_gating_check -setup 0.0
set_wire_load_mode "top"
```

- Graphical interface:

Schematic of counter

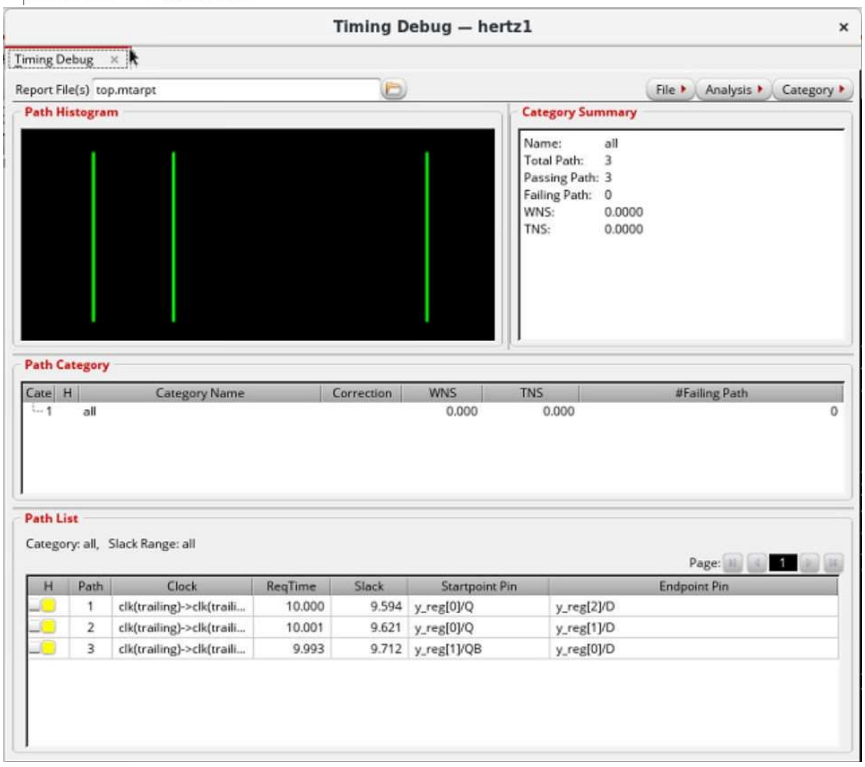


```
legacy_genus:/> write_sdf -timescale ns -nonegchecks -recrem split -edges check_edge -setuphold split > delays.sdf
```

- Writing reports:

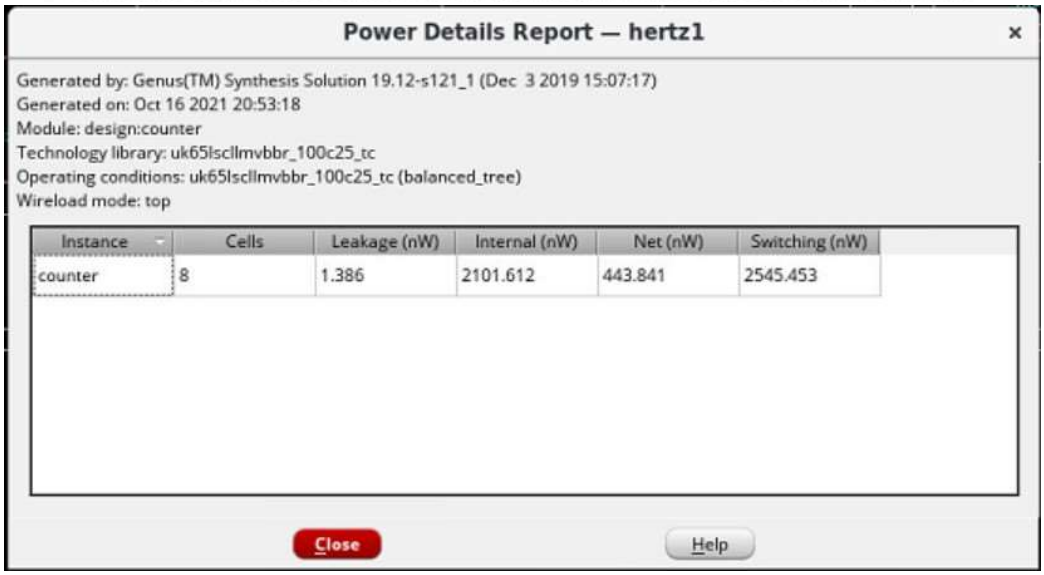
Timing Report

```
legacy_genus:/> report_timing
Warning : Timing problems have been detected in this design. [TIM-11]
        : The design is 'counter'.
        : Use 'check_timing_intent' or 'report timing -lint' to report more information.
============================================================
  Generated by:           Genus(TM) Synthesis Solution 19.12-s121_1
  Generated on:           Oct 16 2021  08:50:23 pm
  Module:                 counter
  Technology library:     uk65lscllmvbbr_100c25_tc
  Operating conditions:   uk65lscllmvbbr_100c25_tc (balanced_tree)
  Wireload mode:          top
  Area mode:              timing library
============================================================

    Pin         Type     Fanout Load Slew Delay Arrival
                              (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------
(clock clk)    launch                                5000 F
y_reg[0]/CKB                              100         5000 F
y_reg[0]/Q     DFCQM2RA       4  4.5   41  +205     5205 F
g204/S                                      +0     5205
g204/Z         MXB2M1RA       2  2.1   70   +93     5298 F
g200/B1                                     +0     5298
g200/Z         AOI32M2R       1  1.3   80   +74     5372 R
g198/B                                      +0     5372
g198/Z         NR2M2R         1  1.1   30   +34     5406 F
y_reg[2]/D     DFCM2RA                      +0     5406
y_reg[2]/CKB   setup                      100    +0     5406 F
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock clk)    capture                              15000 F
-------------------------------------------------------------
Cost Group   : 'clk' (path_group 'clk')
Timing slack :    9594ps
Start-point  : y_reg[0]/CKB
End-point    : y_reg[2]/D
```



Power Report

```
report_power
Info    : Joules engine is used. [RPT-16]
        : Joules engine is being used for the command report_power.
Instance: /counter
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------
       memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
     register     1.07410e-09  1.92893e-06  1.18859e-07  2.04886e-06  80.45%
        latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        logic     3.12232e-10  1.72687e-07  1.14982e-07  2.87981e-07  11.31%
         bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        clock     0.00000e+00  0.00000e+00  2.10000e-07  2.10000e-07   8.25%
          pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
           pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------
    Subtotal     1.38633e-09  2.10162e-06  4.43841e-07  2.54684e-06 100.01%
  Percentage           0.05%       82.52%       17.43%      100.00% 100.00%
  ------------------------------------------------------------------------
```

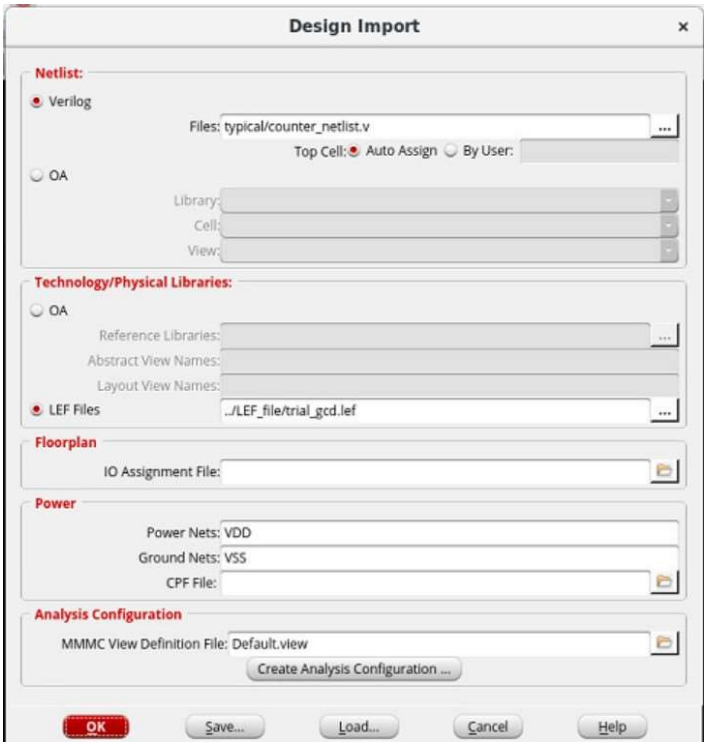


QOR Report

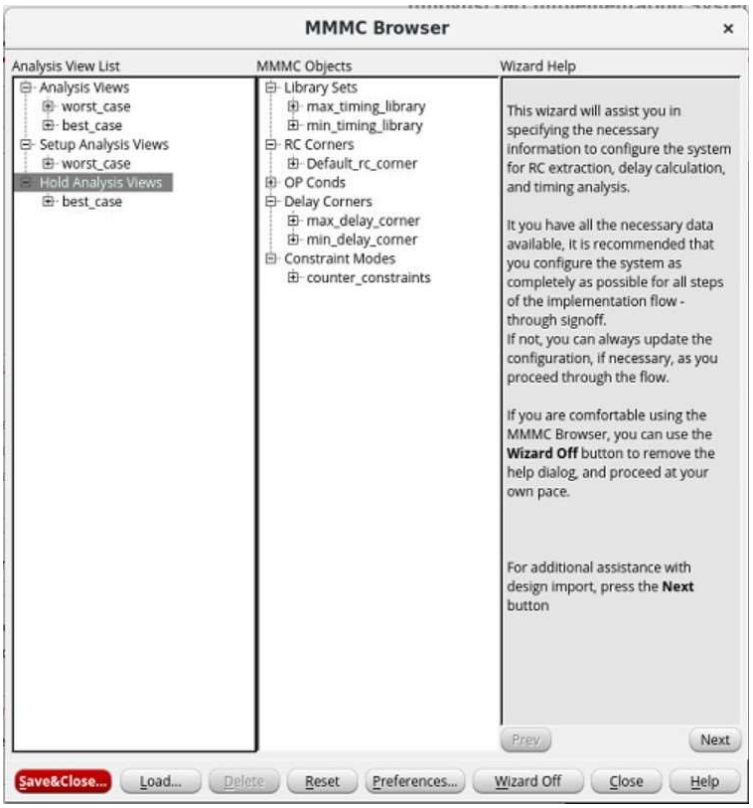
```
legacy_genus:/> report_qor
================================================================
  Generated by:           Genus(TM) Synthesis Solution 19.12-s121_1
  Generated on:           Oct 16 2021  08:55:03 pm
  Module:                 counter
  Technology library:     uk65lscllmvbbr_100c25_tc
  Operating conditions:   uk65lscllmvbbr_100c25_tc (balanced_tree)
  Wireload mode:          top
  Area mode:              timing library
================================================================

Timing
--------

Clock  Period
--------------
clk   10000.0


  Cost    Critical         Violating
 Group   Path Slack  TNS     Paths
-------------------------------------
clk          9593.5   0.0         0
default    No paths   0.0
-------------------------------------
Total                 0.0         0

Instance Count
--------------
Leaf Instance Count             8
Physical Instance count         0
Sequential Instance Count       3
Combinational Instance Count    5
Hierarchical Instance Count     0

Area
----
Cell Area                          34.200
Physical Cell Area                 0.000
Total Cell Area (Cell+Physical)    34.200
Net Area                           0.000
Total Area (Cell+Physical+Net)     34.200

Max Fanout                         4 (Q0)
Min Fanout                         1 (n_0)
Average Fanout                     2.1
Terms to net ratio                 2.6667
Terms to instance ratio            4.0000
Runtime                            86.945619 seconds
Elapsed Runtime                    654 seconds
Genus peak memory usage            1245.82
Innovus peak memory usage          no_value
Hostname                           hertz1.vlsi.ee.iitd.ac.in
```

- Exit

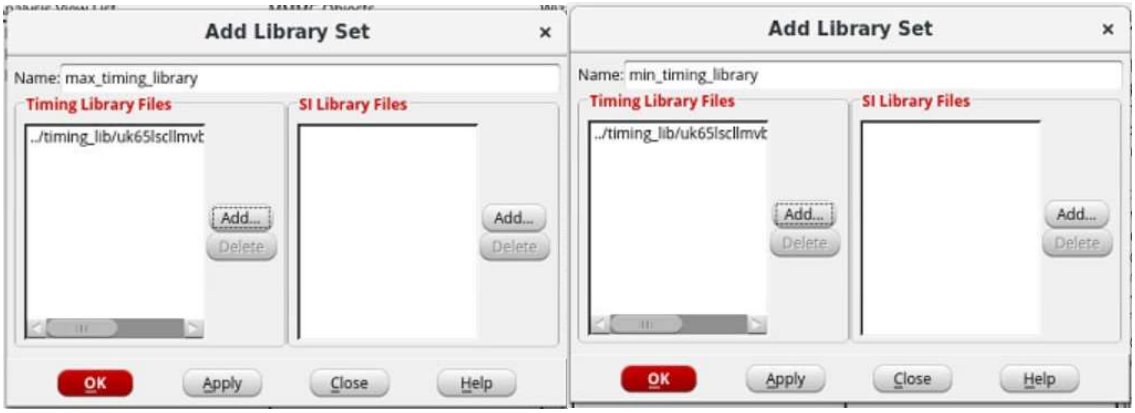
- Implementation using Innovus:
    - Command: encounter
    - File -> Import Design



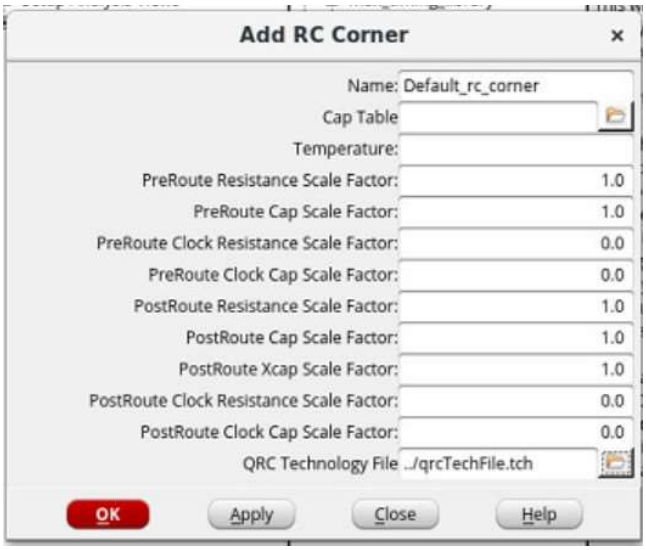
MMMC View

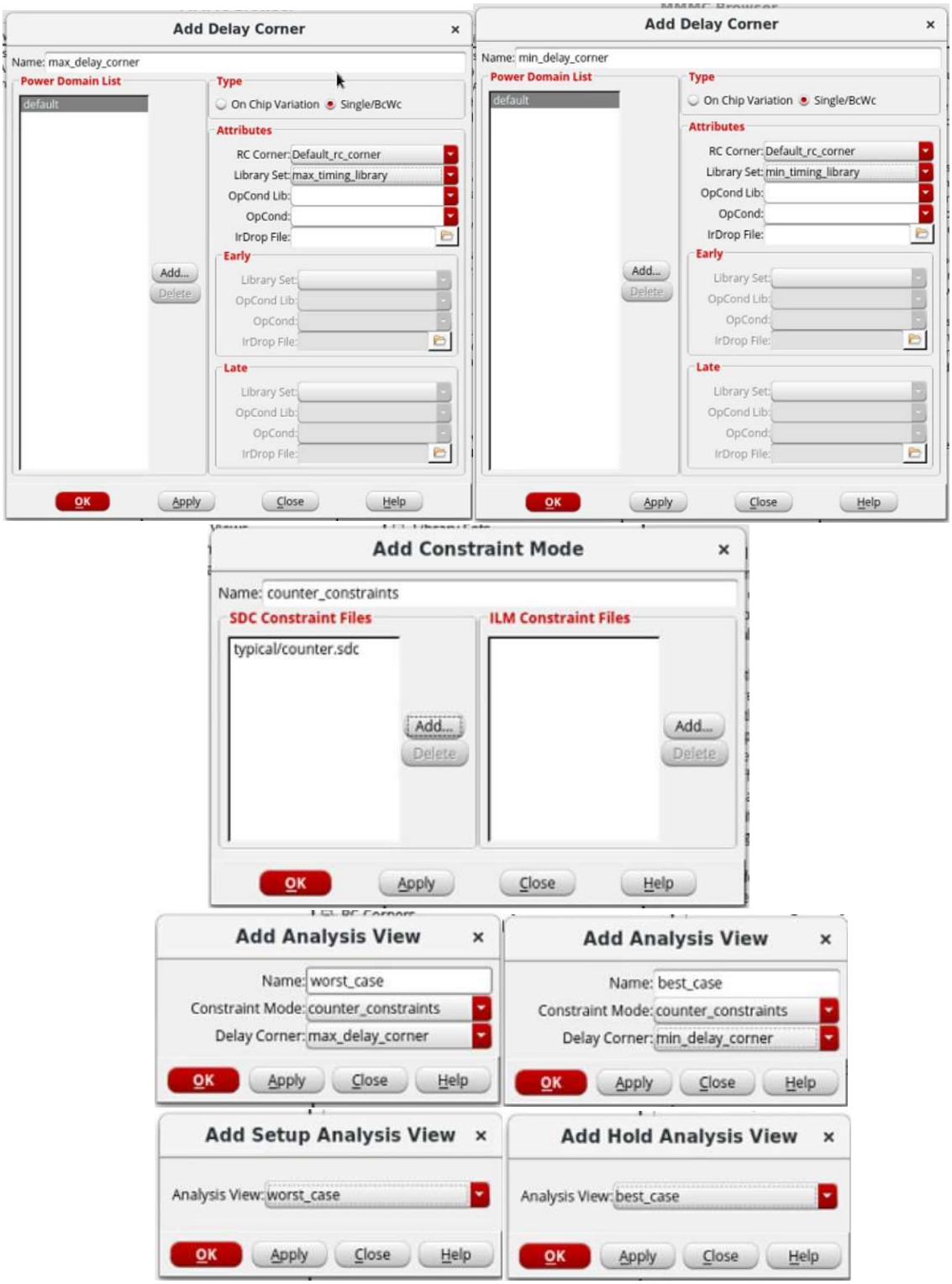


Path:
/afs/iitd.ac.in/user/e/ee/een212020//Physical/timing_lib/uk65lscllmvbbr_090c125_wc_ccs.lib
/afs/iitd.ac.in/user/e/ee/een212020//Physical/timing_lib/uk65lscllmvbbr_110c-40_bc_ccs.lib

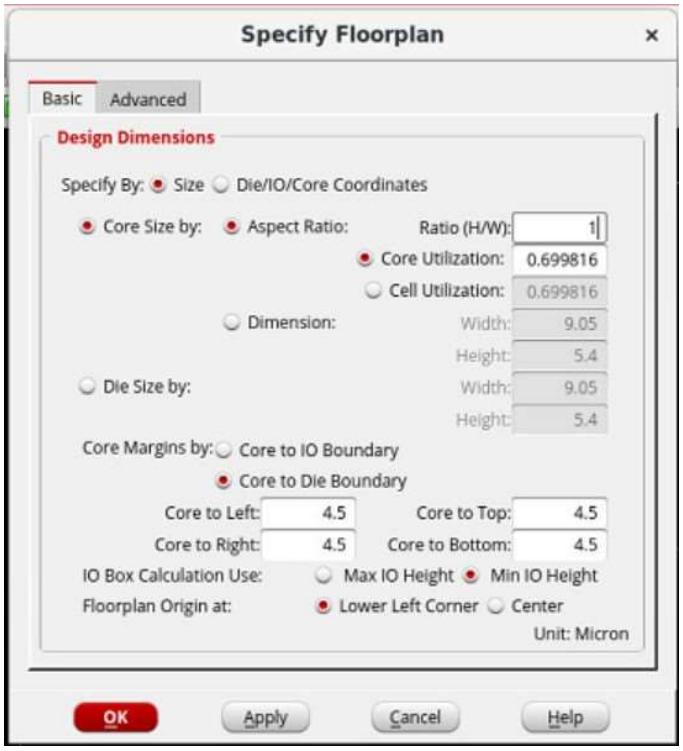


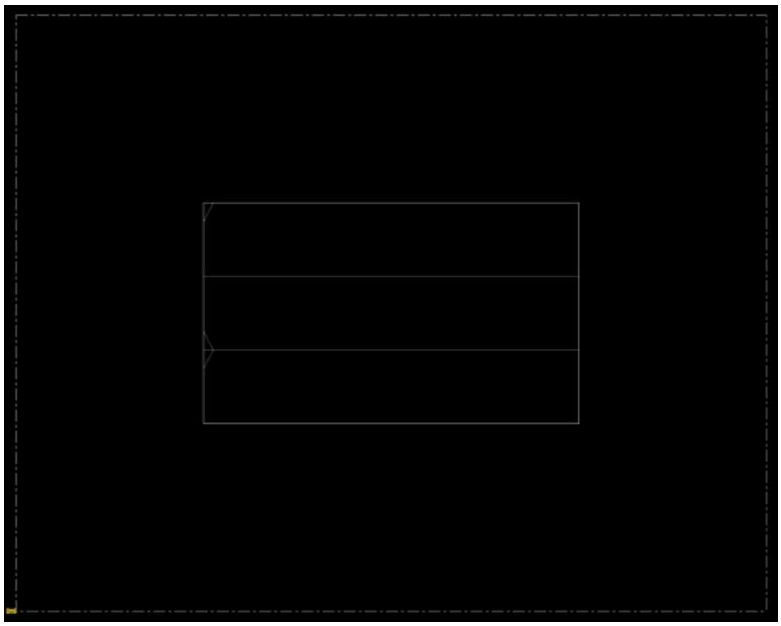
Path: /afs/iitd.ac.in/user/e/ee/een212020//Physical/qrcTechFile.tch




Add Delay Corner
Name: max_delay_corner
Power Domain List
default
Type
On Chip Variation
Single/BcWc
Attributes
RC Corner: Default_rc_corner
Library Set: max_timing_library
OpCond Lib:
OpCond:
IrDrop File:
Early
Late
Add...
Delete
OK
Apply
Close
Help
Add Delay Corner
Name: min_delay_corner
Power Domain List
default
Type
On Chip Variation
Single/BcWc
Attributes
RC Corner: Default_rc_corner
Library Set: min_timing_library
OpCond Lib:
OpCond:
IrDrop File:
Early
Late
Add...
Delete
OK
Apply
Close
Help
Add Constraint Mode
Name: counter_constraints
SDC Constraint Files
typical/counter.sdc
ILM Constraint Files
Add...
Delete
OK
Apply
Close
Help
Add Analysis View
Name: worst_case
Constraint Mode: counter_constraints
Delay Corner: max_delay_corner
OK
Apply
Close
Help
Add Analysis View
Name: best_case
Constraint Mode: counter_constraints
Delay Corner: min_delay_corner
OK
Apply
Close
Help
Add Setup Analysis View
Analysis View: worst_case
OK
Apply
Close
Help
Add Hold Analysis View
Analysis View: best_case
OK
Apply
Close
Help

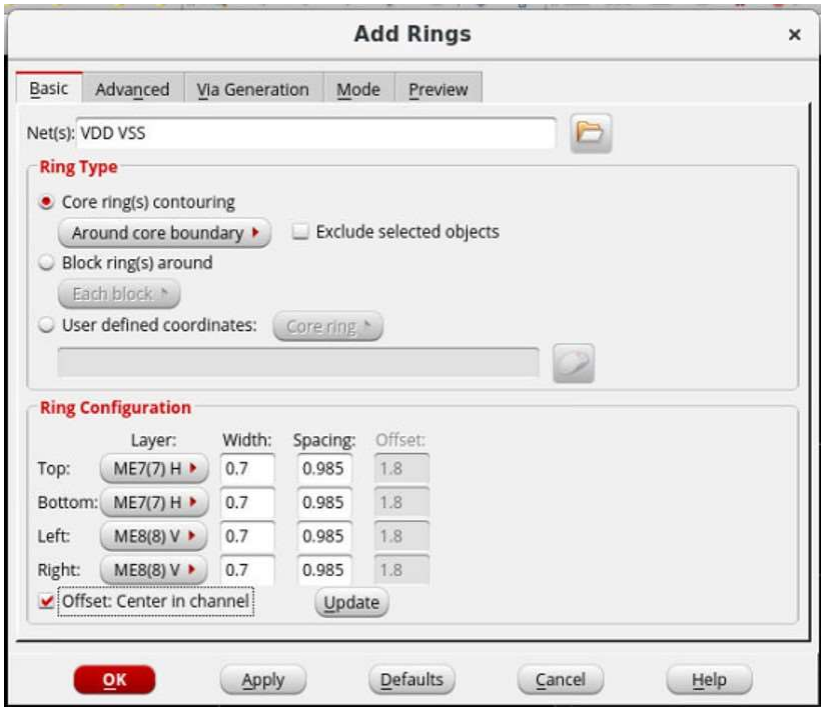
- Floorplan


Specify Floorplan
Basic
Advanced
Design Dimensions
Specify By: Size Die/IO/Core Coordinates
Core Size by: Aspect Ratio: Ratio (H/W): 1
Core Utilization: 0.699816
Cell Utilization: 0.699816
Dimension: Width: 9.05
Height: 5.4
Die Size by: Width: 9.05
Height: 5.4
Core Margins by: Core to IO Boundary
Core to Die Boundary
Core to Left: 4.5
Core to Top: 4.5
Core to Right: 4.5
Core to Bottom: 4.5
IO Box Calculation Use: Max IO Height Min IO Height
Floorplan Origin at: Lower Left Corner Center
Unit: Micron
OK
Apply
Cancel
Help

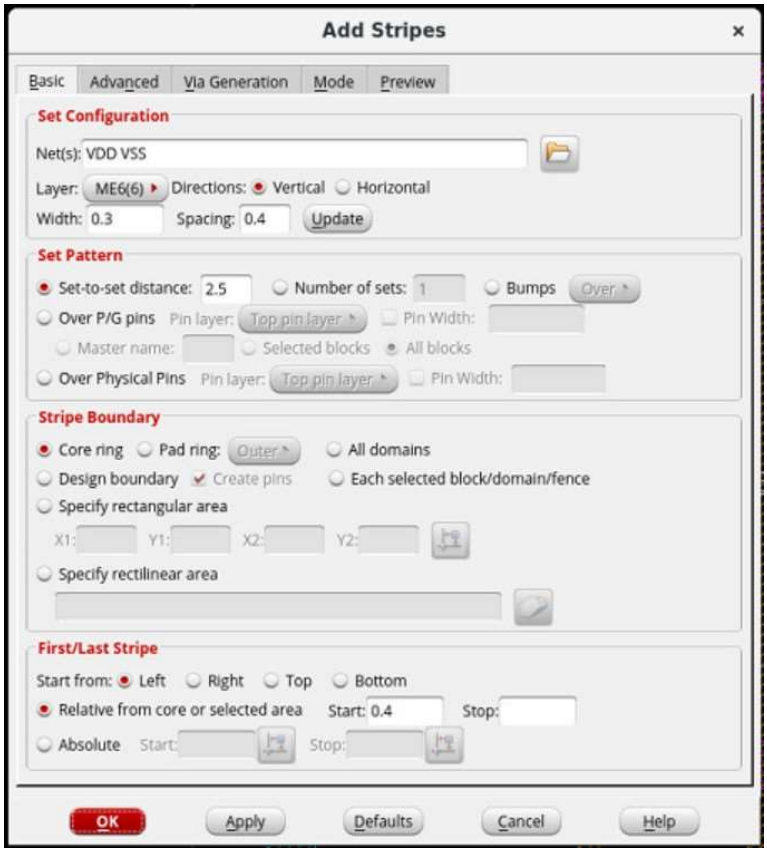


- Powerplan

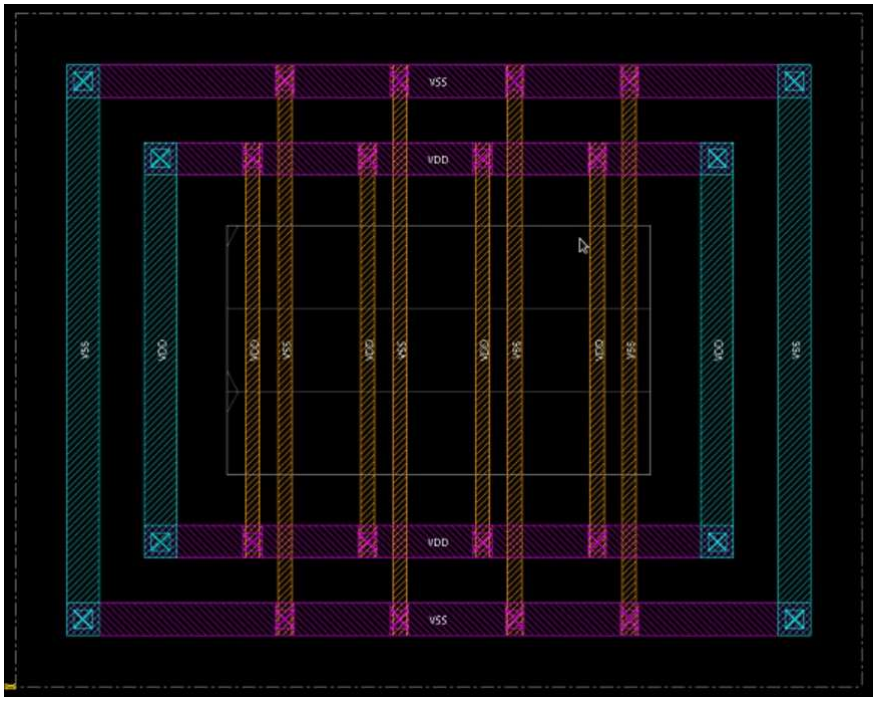
Adding Ring



Adding Stripes



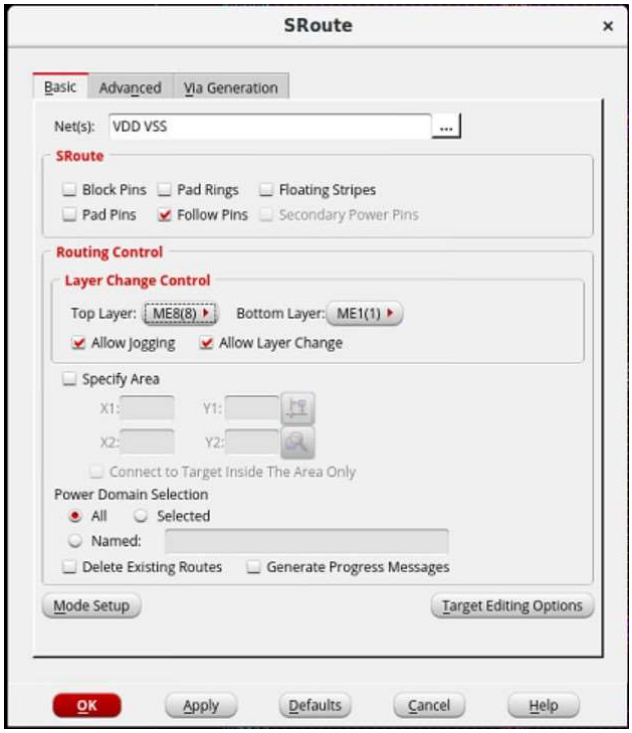
Floorplan

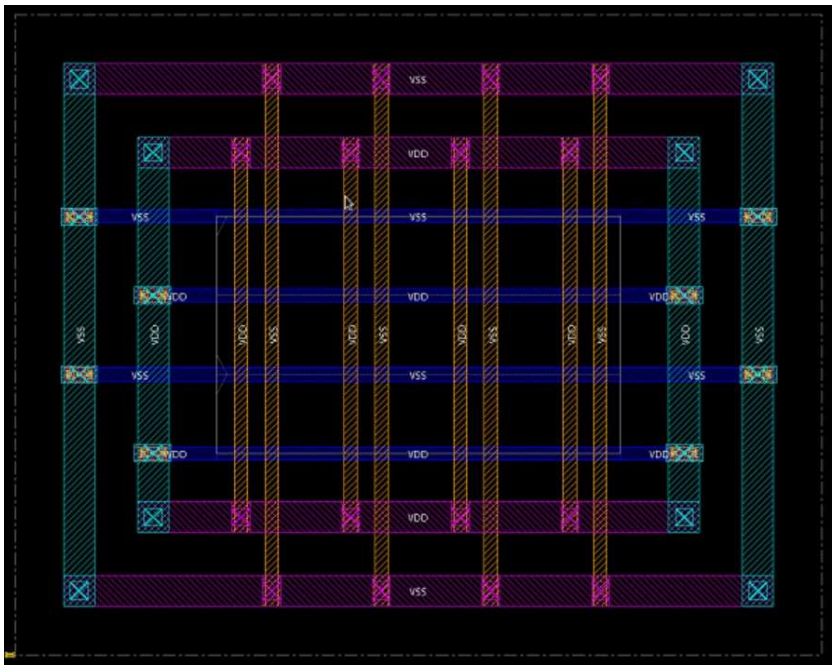


- Associate global VDD and VSS net names to the standard cell pin names

```
globalNetConnect VDD -type pgpin -pin VDD -instanceBaseName *
globalNetConnect VSS -type pgpin -pin VSS -instanceBaseName *
```

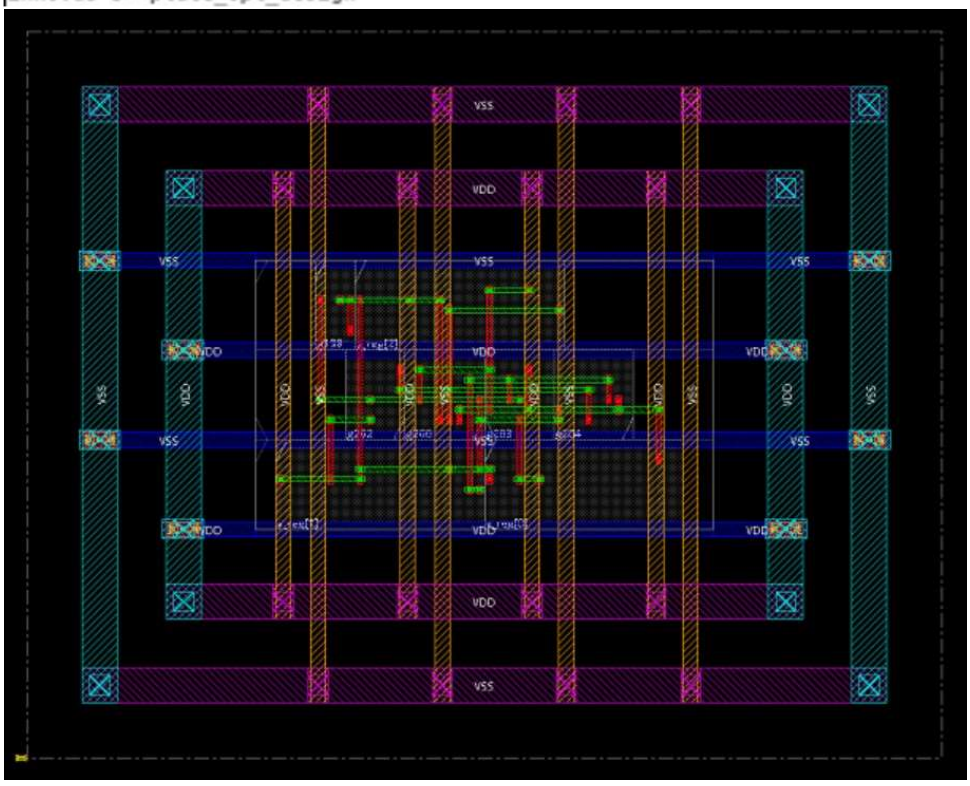
- Special Route





- Place cells

```
innovus 3> place_opt_design
```



- **Pre-CTS Timing Analysis**

Setup:

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 worst_case

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  4.915  |  9.199  |  4.915  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    3    |    3    |    3    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 68.841%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.29 sec
Total Real time: 0.0 sec
Total Memory Usage: 2124.792969 Mbytes
```

Hold:

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 best_case

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.102  |  0.102  |  4.965  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    3    |    3    |    3    |
+--------------------+---------+---------+---------+

Density: 68.841%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.29 sec
Total Real time: 1.0 sec
Total Memory Usage: 2103.371094 Mbytes
```

- **Clock Tree Synthesis**

```
innovus 5> create_ccopt_clock_tree_spec
innovus 6> ccopt_design
```

- **Post-CTS Timing Analysis**

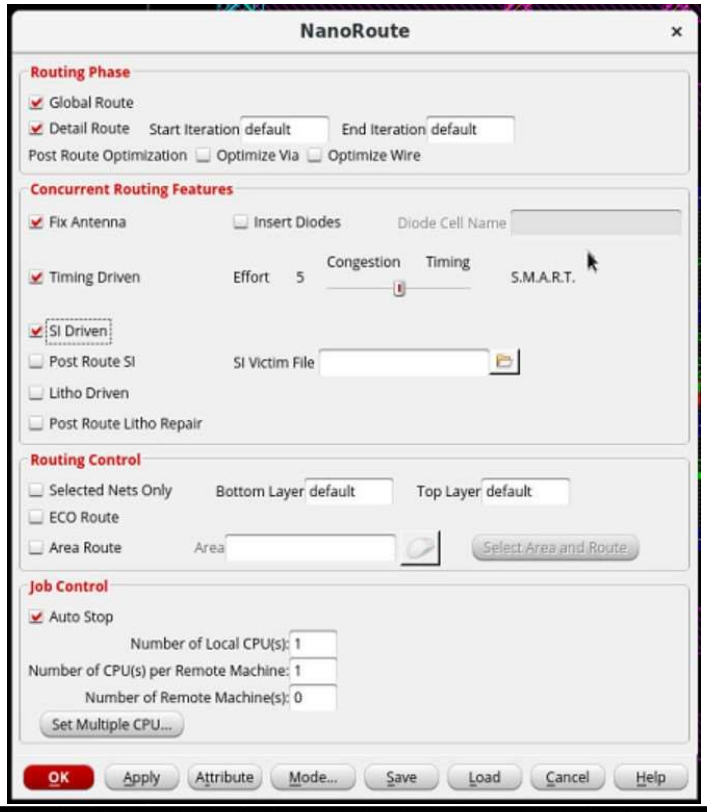
Setup:

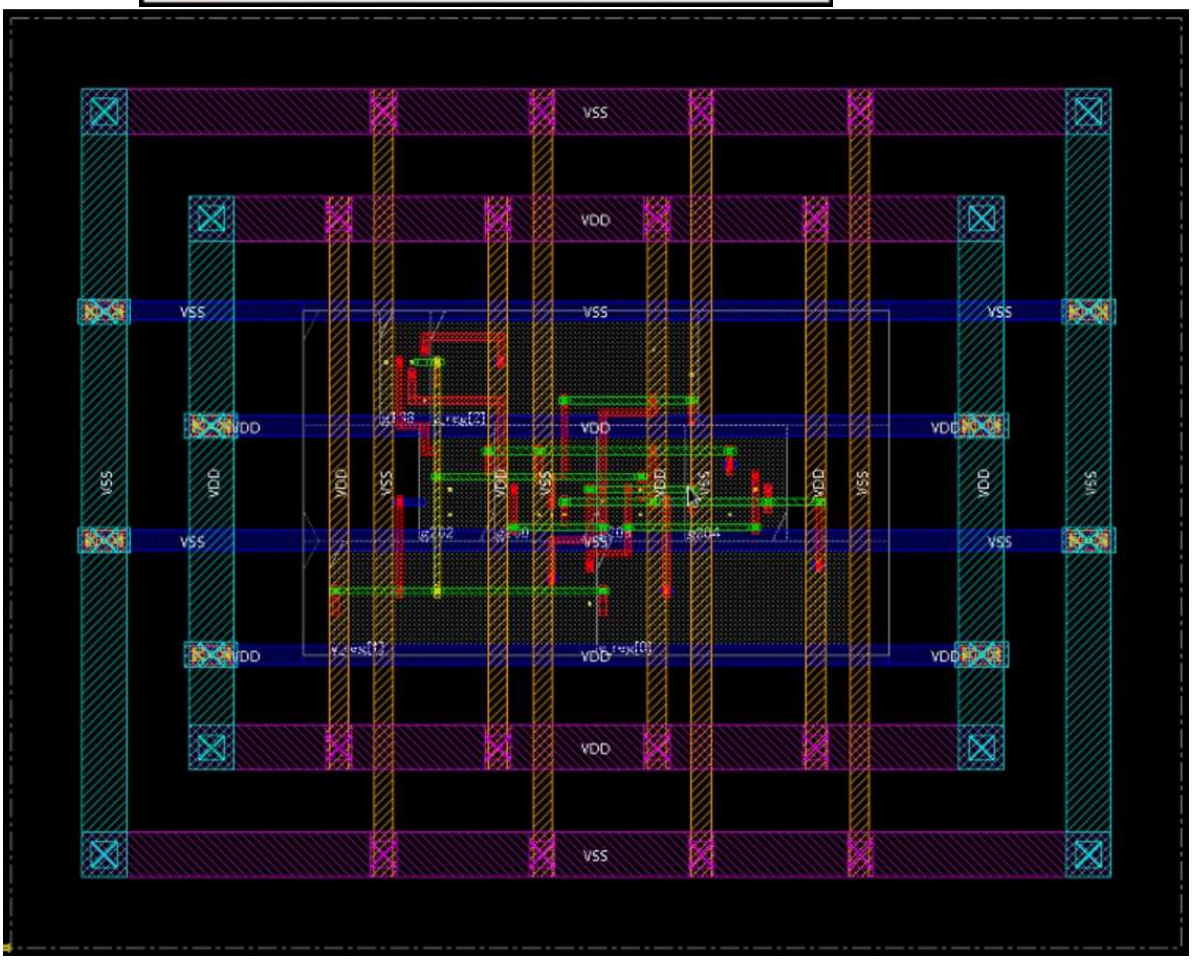
```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 worst_case

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  4.869  |  9.203  |  4.869  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    3    |    3    |    3    |
+--------------------+---------+---------+---------+

+---------------+-------------------------------+------------------+
|               |              Real             |       Total      |
|    DRVs       +------------------+------------+------------------|
|               |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+---------------+------------------+------------+------------------+
|   max_cap     |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran    |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout  |      0 (0)       |     0      |      0 (0)       |
|   max_length  |      0 (0)       |     0      |      0 (0)       |
+---------------+------------------+------------+------------------+

Density: 68.841%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.1 sec
Total Real time: 0.0 sec
Total Memory Usage: 2203.847656 Mbytes
```

Hold:

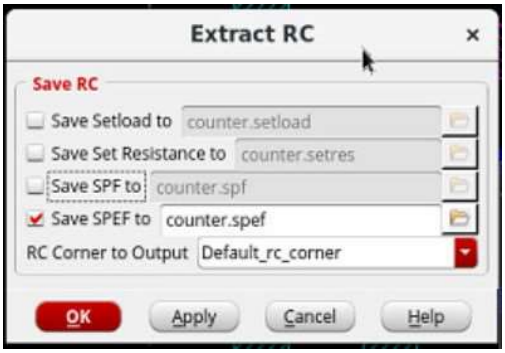
```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 best_case

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.100  |  0.100  |  4.997  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    3    |    3    |    3    |
+--------------------+---------+---------+---------+

Density: 68.841%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.29 sec
Total Real time: 0.0 sec
Total Memory Usage: 2181.691406 Mbytes
```

- Nanoroute

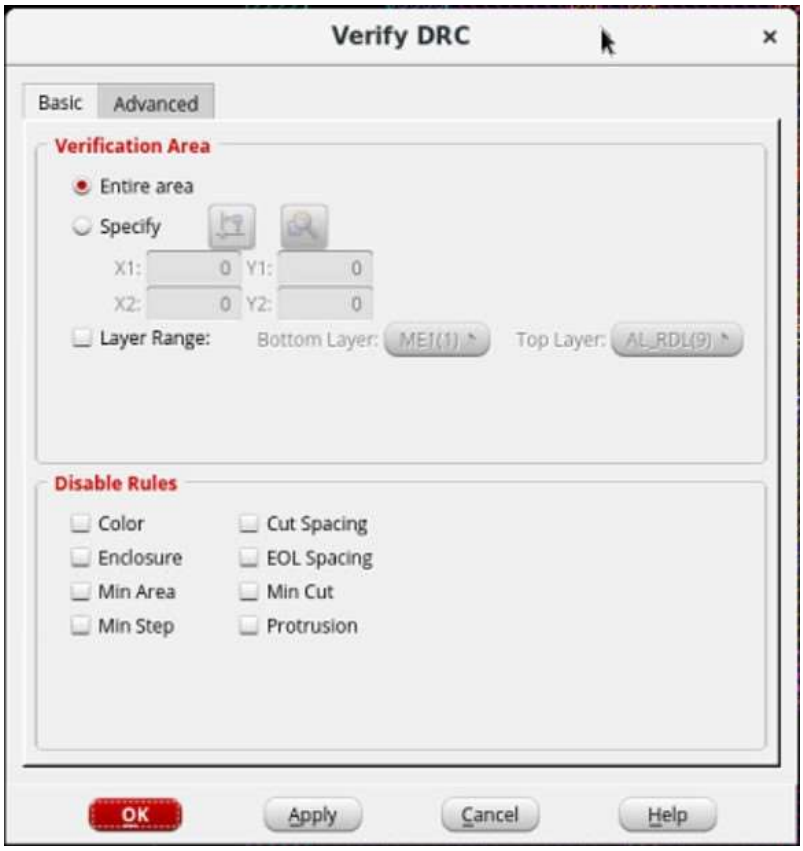

NanoRoute
Routing Phase
Global Route
Detail Route
Start Iteration default
End Iteration default
Post Route Optimization
Optimize Via
Optimize Wire
Concurrent Routing Features
Fix Antenna
Insert Diodes
Diode Cell Name
Timing Driven
Effort 5
Congestion
Timing
S.M.A.R.T.
SI Driven
Post Route SI
SI Victim File
Litho Driven
Post Route Litho Repair
Routing Control
Selected Nets Only
Bottom Layer default
Top Layer default
ECO Route
Area Route
Area
Select Area and Route
Job Control
Auto Stop
Number of Local CPU(s): 1
Number of CPU(s) per Remote Machine: 1
Number of Remote Machine(s): 0
Set Multiple CPU...
OK
Apply
Attribute
Mode...
Save
Load
Cancel
Help


VSS
VDD

- RC Extraction

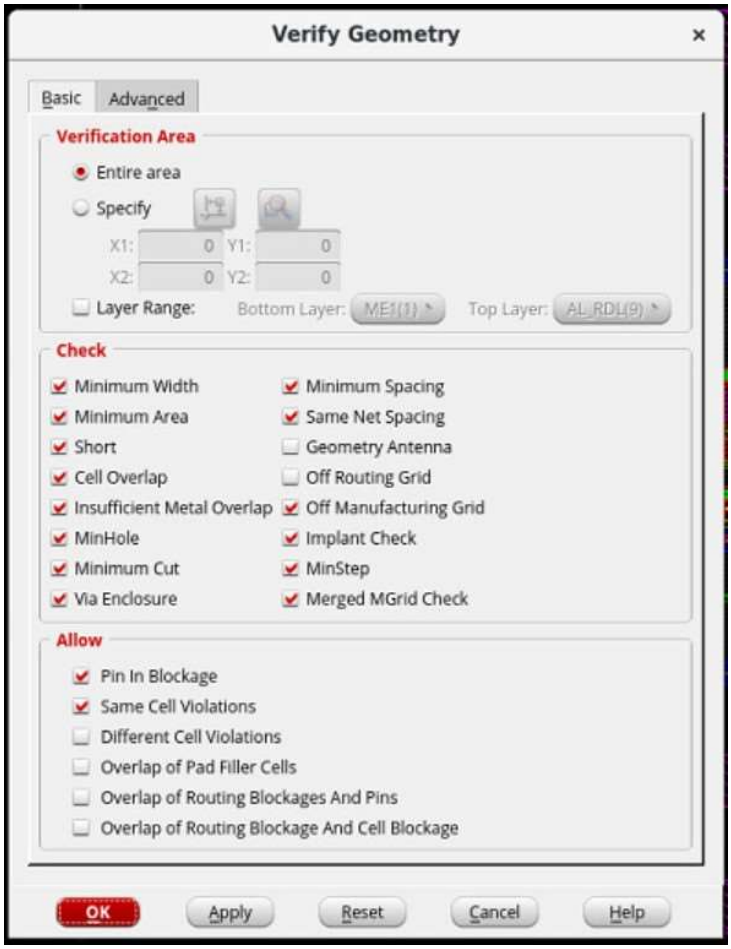


- DRC Verification



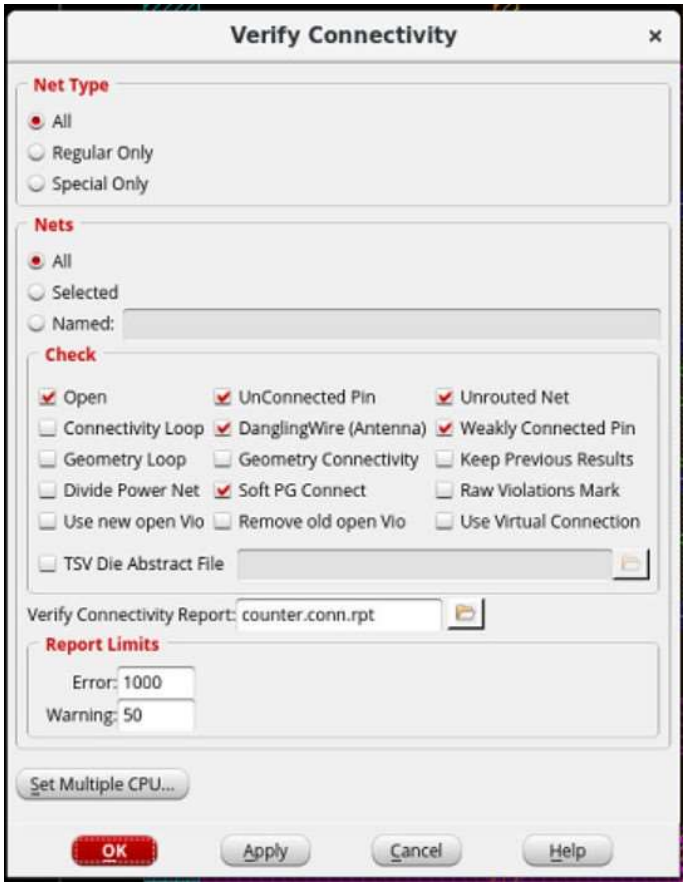
```
innovus 8> #-report counter.drc.rpt                # string, default="", user setting
 *** Starting Verify DRC (MEM: 2486.3) ***

  VERIFY DRC ..... Starting Verification
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
  VERIFY DRC ..... Using new threading
  VERIFY DRC ..... Sub-Area: {0.000 0.000 18.400 14.600} 1 of 1
  VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

  Verification Complete : 0 Viols.

 *** End Verify DRC (CPU: 0:00:00.0  ELAPSED TIME: 0.00  MEM: 0.0M) ***
```

- Geometry Verification




```
 *** Starting Verify Geometry (MEM: 2486.3) ***

**WARN: (IMPVFG-257):   verifyGeometry command is replaced by ver
  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                  ..... bin size: 2880
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells          :  0 Viols.
  VERIFY GEOMETRY ..... SameNet        :  0 Viols.
  VERIFY GEOMETRY ..... Wiring         :  0 Viols.
  VERIFY GEOMETRY ..... Antenna        :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:00.1  MEM: 106.6M)
```

- Connectivity Verification




```
innovus 8> VERIFY_CONNECTIVITY use new engine.

******** Start: VERIFY CONNECTIVITY ********
Start Time: Sat Oct 16 22:32:28 2021

Design Name: counter
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (18.4000, 14.6000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Sat Oct 16 22:32:28 2021
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)
```

- Power Analysis

```
*       Design: counter
*
*       Liberty Libraries used:
*               worst_case: ../timing_lib/uk65lscllmvbbr_090c125_wc_ccs.lib
*
*       Power Domain used:
*               Rail:        VDD        Voltage:        0.9
*
*       Power View : worst_case
*
*       User-Defined Activity : N.A.
*
*       Activity File: N.A.
*
*       Hierarchical Global Activity: N.A.
*
*       Global Activity: N.A.
*
*       Sequential Element Activity: N.A.
*
*       Primary Input Activity: 0.200000
*
*       Default icg ratio: N.A.
*
*       Global Comb ClockGate Ratio: N.A.
*
*       Power Units = 1mW
*
*       Time Units = 1e-09 secs
*
*       Temperature = 125
*
*       report_power -outfile ./run1/counter.rpt -rail_analysis_format VS
*
--------------------------------------------------------------------------------------
Cell                            Internal   Switching       Total     Leakage   Cell
                                   Power       Power       Power       Power   Name
--------------------------------------------------------------------------------------
y_reg[1]                       0.0005501   4.502e-05    0.000597   1.884e-06  DFCM2RA
y_reg[0]                       0.0005304   4.216e-05   0.0005741   1.569e-06  DFCQM2RA
y_reg[2]                       0.0004957   2.147e-05   0.0005191   1.889e-06  DFCM2RA
g204                           4.255e-05   2.657e-05   6.962e-05   5.004e-07  MXB2M1RA
g202                           3.982e-05   9.678e-06   4.987e-05   3.767e-07  NR2B1M2R
g200                           3.388e-05   1.138e-05   4.553e-05   2.599e-07  AOI32M2R
g203                           2.573e-05   9.648e-06   3.569e-05   3.128e-07  AOI211M2R
g198                           1.009e-05   5.463e-06   1.578e-05   2.253e-07  NR2M2R

--------------------------------------------------------------------------------------

Total (      8 of      8  )     0.001728   0.0001714   0.001907   7.017e-06
Total Capacitance                1.877e-14 F
Power Density                    *** No Die Area ***
```