IEC Lab 1

Layout and Simulation

1. Design a mod-5 synchronous counter using JK Flip Flop.
2. Take PMOS width to be 400nm and NMOS width to be 200nm.
3. 250MHz clock frequency.
4. Draw a transistor level schematic for each gate and use those gates to create higher level blocks.
5. Verify that the schematic works as intended.
6. Draw a layout for the entire design from scratch.
7. Aim for minimum possible area with rectangular shaped layout with height as 1400nm. Lower area will fetch more marks.
8. Clear the DRC errors, verify the LVS and perform a PEX analysis.
9. Present your work neatly. The link to upload your work will be provided in the Teams channel.
10. Deadline is 11:59pm, 17th September, 2021.