IEC LAB - I

TASK 1

Report

Submitted By:

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Objective:

Design a mod-5 synchronous counter using JK Flip Flop.

Specifications:

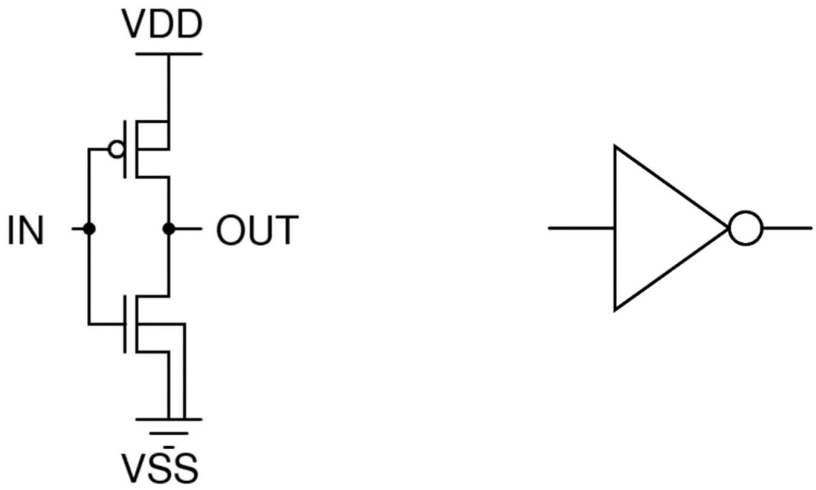
- Take PMOS width to be 400nm and NMOS width to be 200nm.
- 250MHz clock frequency.
- Draw a transistor level schematic for each gate and use those gates to create higher level blocks.
- Verify that the schematic works as intended.
- Draw a layout for the entire design from scratch.
- Aim for minimum possible area with rectangular shaped layout with height as 1400nm. Lower area will fetch more marks.
- Clear the DRC errors, verify the LVS and perform a PEX analysis.

Components Used:

- Inverter
- 2-Input NAND
- 3-Input NAND
- SR Latch
- JK Flipflop

Inverter/NOT

Schematic and Symbol

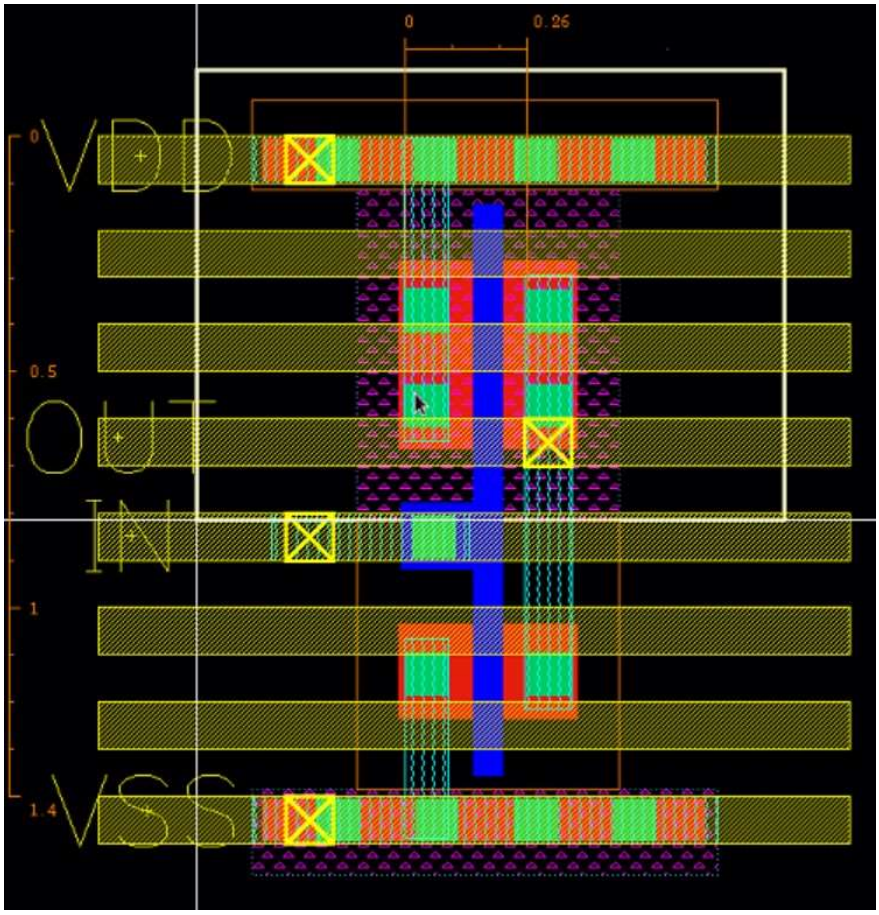


Truth Table

IN	OUT
0	1
1	0

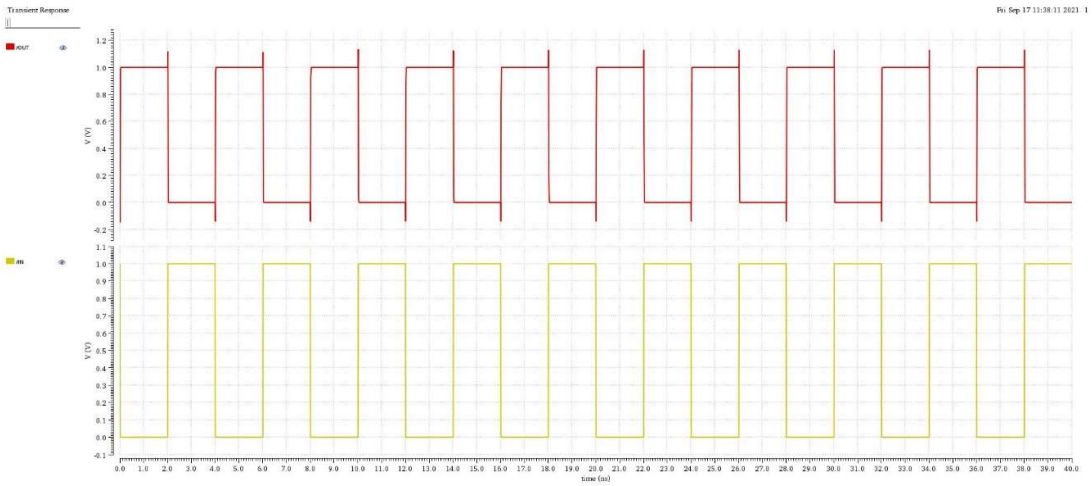
Layout

Width = **0.26 um**

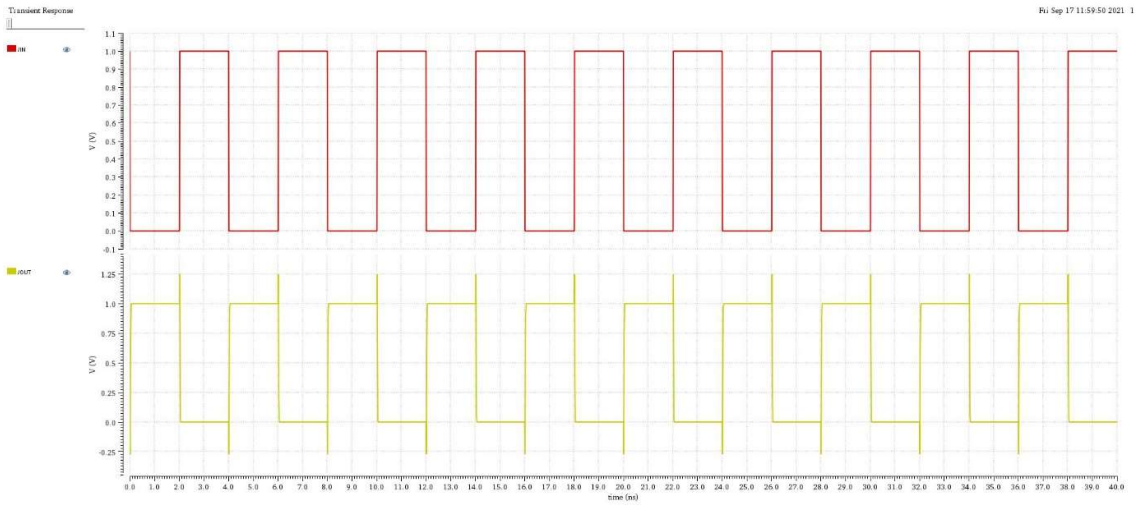


Waveform

Pre-layout Simulation



Post-layout Simulation



Timing Information

PRE LAYOUT SIMULATION

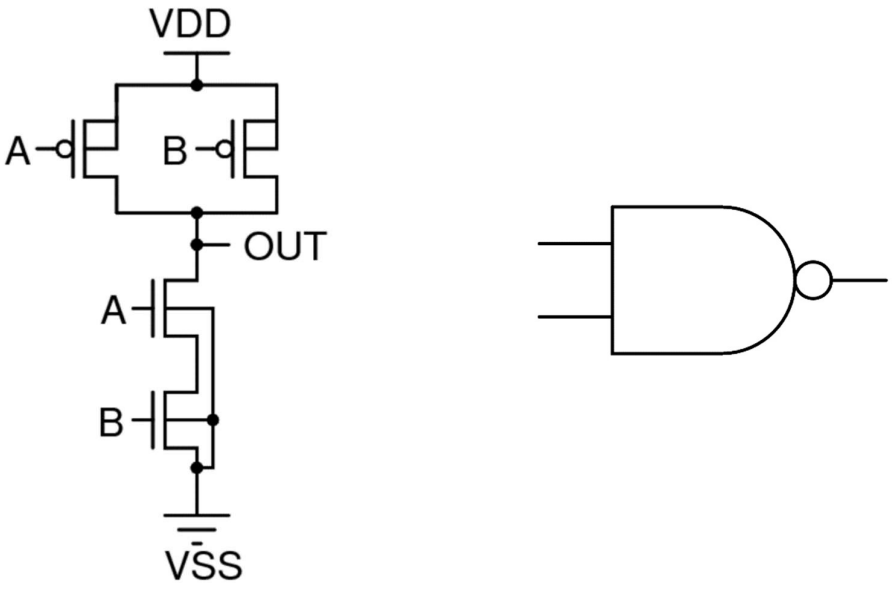
Signal	Rise Time (ps)	Fall Time (ps)	tpHL (ps)	tpLH (ps)	Propagation delay (ps)
IN	10	10			
OUT	7.68	6.4327	8	8	8

POST LAYOUT SIMULATION

Signal	Rise Time (ps)	Fall Time (ps)	tpHL (ps)	tpLH (ps)	Propagation delay (ps)
IN	10	10			
OUT	16.64	13.17	14	16	15

2-Input NAND

Schematic and Symbol

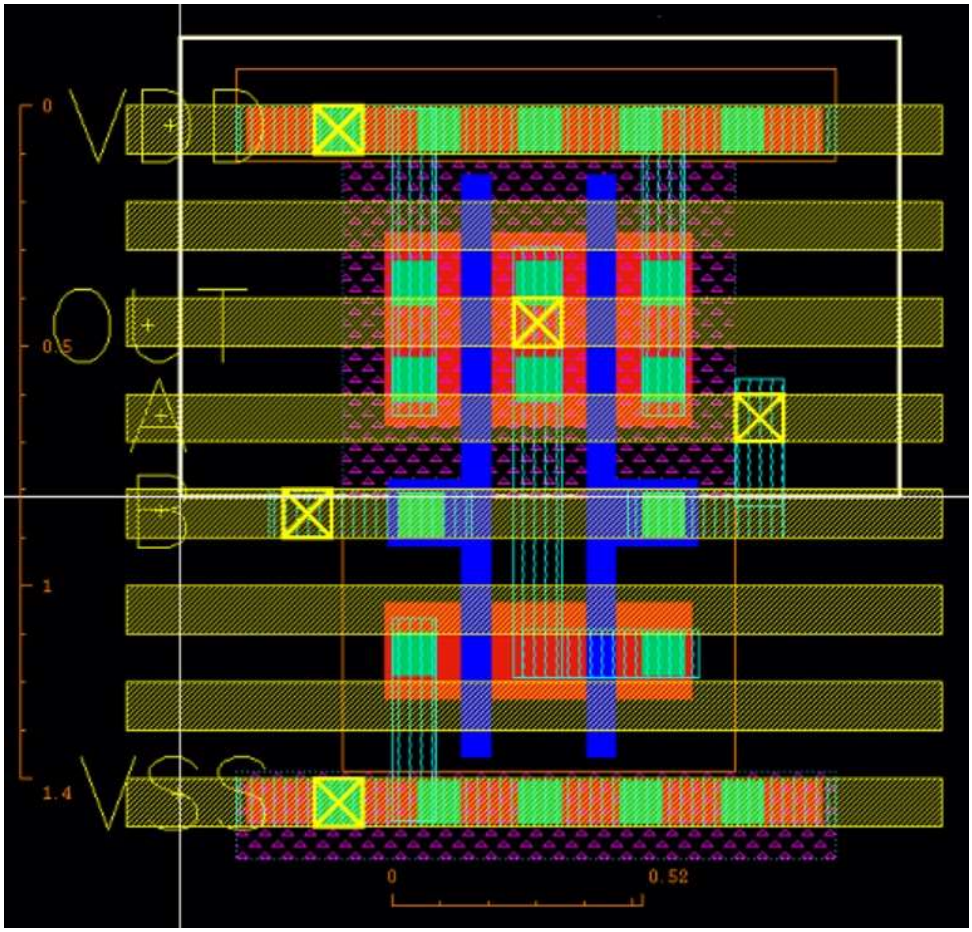


Truth Table

A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

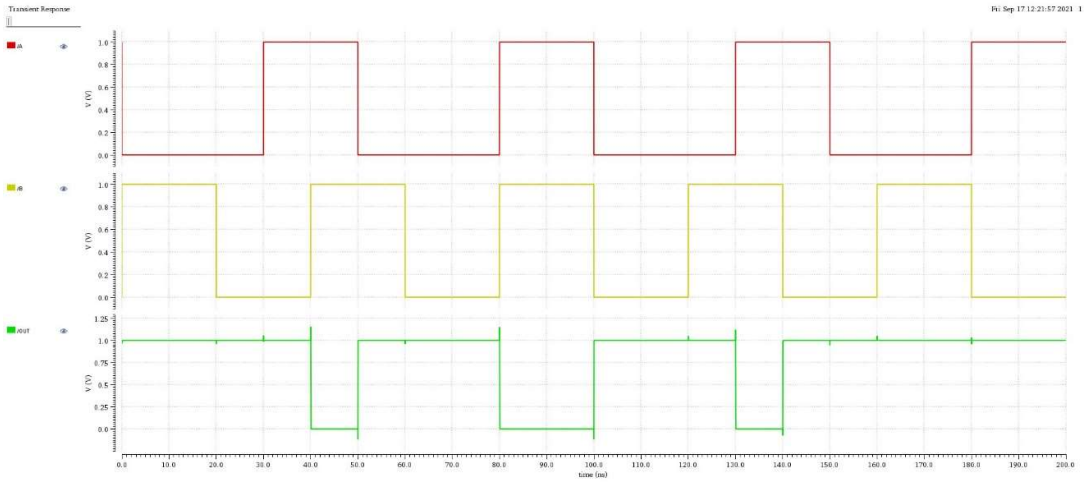
Layout

Width = **0.52 um**

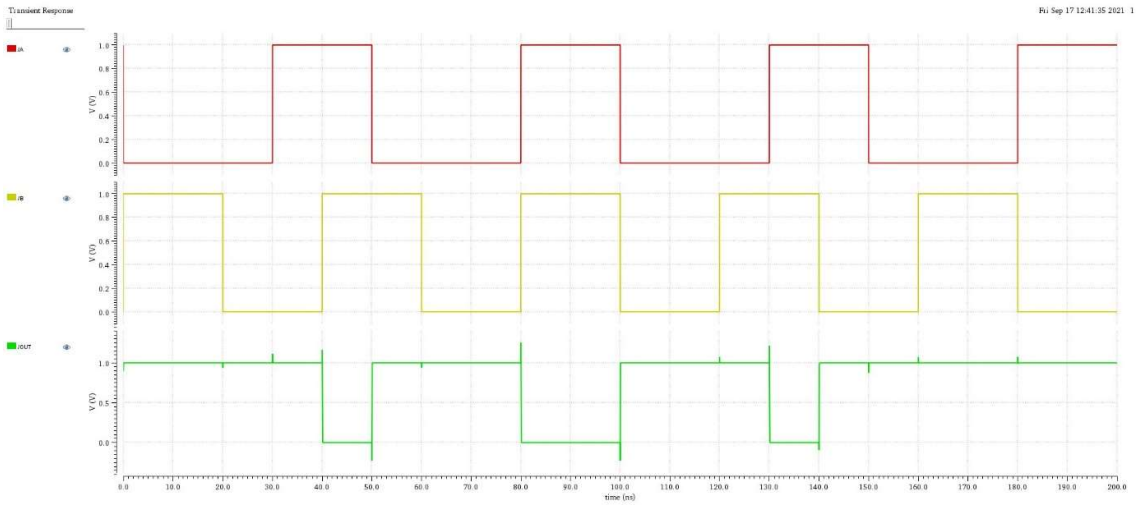


Waveform

Pre-layout Simulation



Post-layout Simulation



Timing Information

PRE LAYOUT SIMULATION

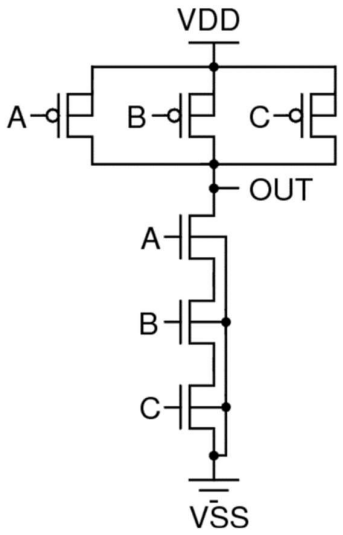
Signal	Rise Time (ps)	Fall Time (ps)	tpHL (ps)	tpLH (ps)	Propagation delay (ps)
A	10	10			
B	10	10			
OUT	12.33	21.17	20.85	10.39	15.62

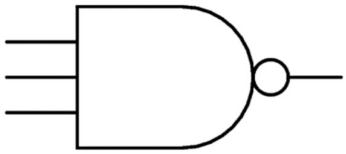
POST LAYOUT SIMULATION

Signal	Rise Time (ps)	Fall Time (ps)	tpHL (ps)	tpLH (ps)	Propagation delay (ps)
A	10	10			
B	10	10			
OUT	16.64	21.48	28.55	18.25	23.4

3-Input NAND

Schematic and Symbol



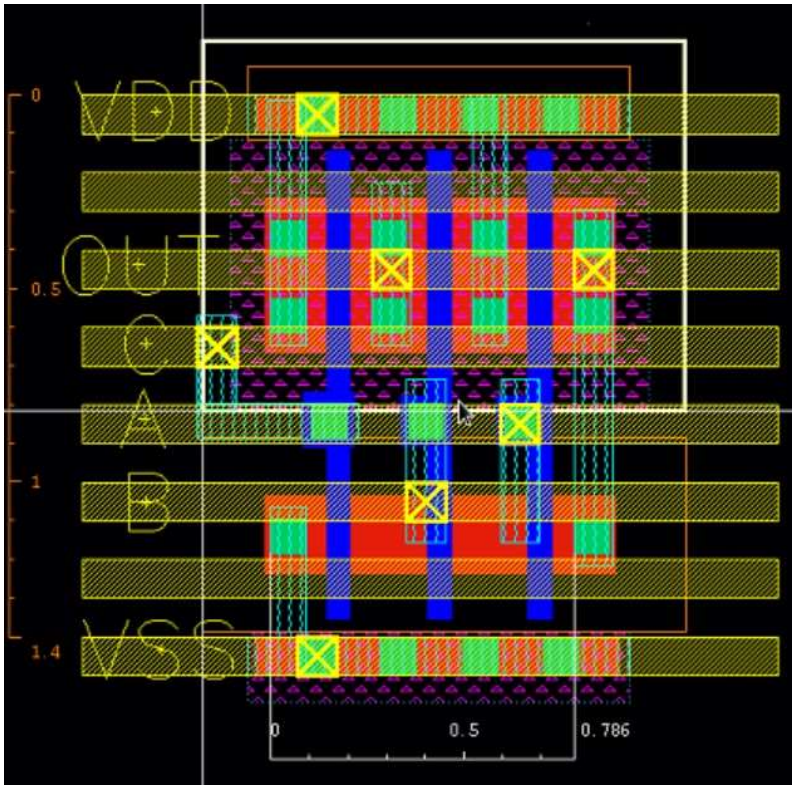


Truth Table

A	B	C	OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

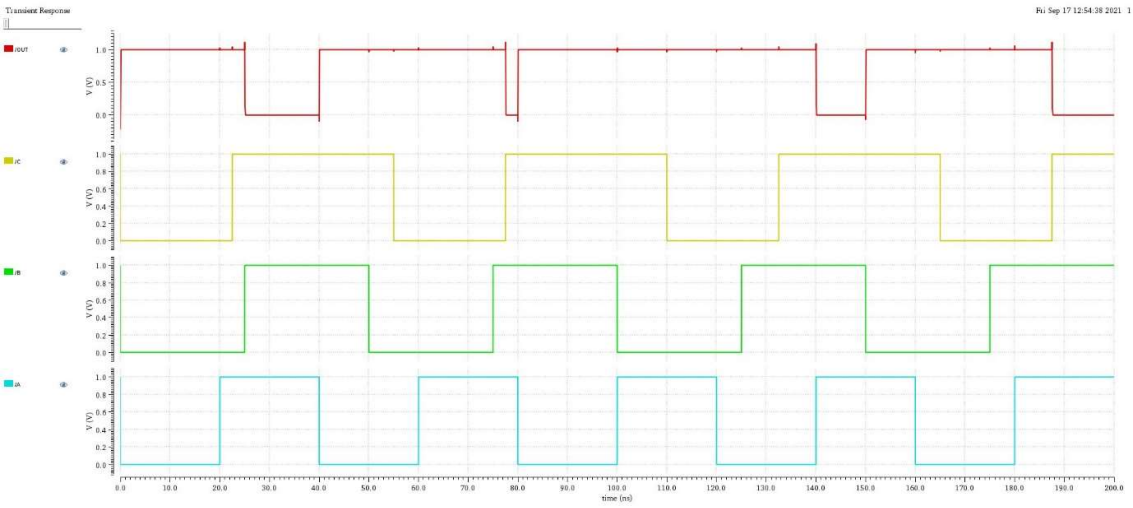
Layout

Width = **0.786 um**

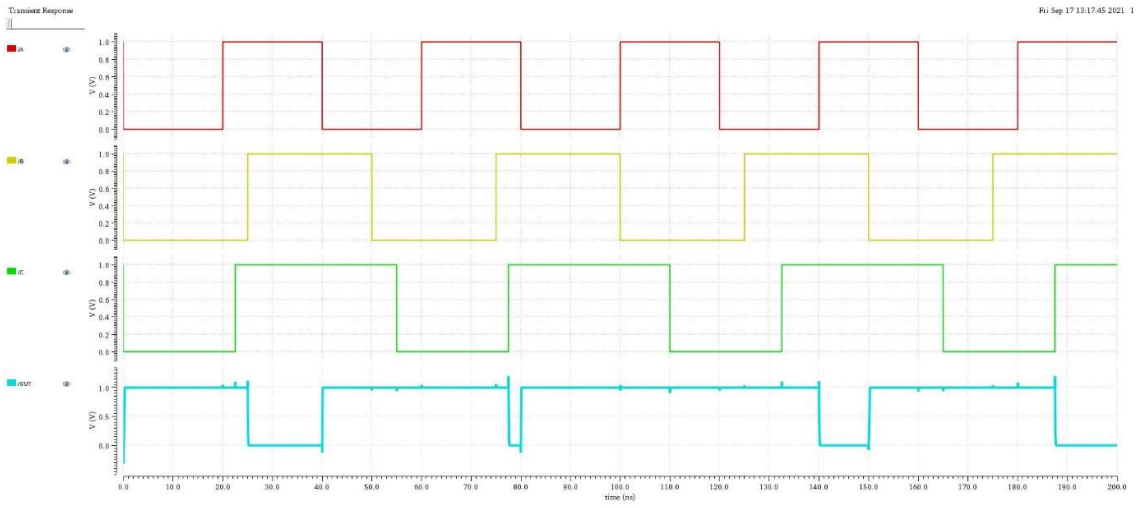


Waveform

Pre-layout Simulation



Post-layout Simulation



Timing Information

PRE LAYOUT SIMULATION

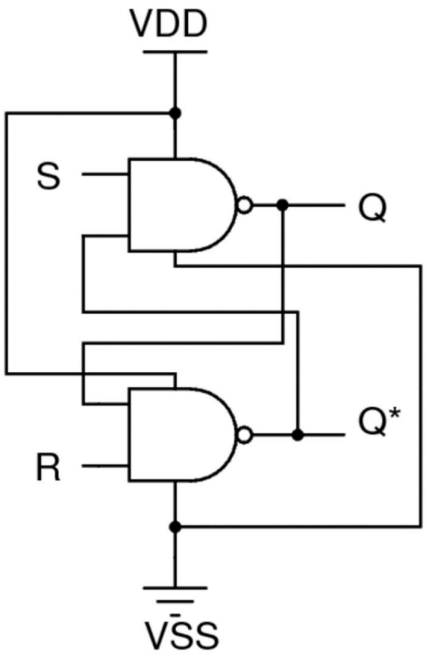
Signal	Rise Time (ps)	Fall Time (ps)	tpHL (ps)	tpLH (ps)	Propagation delay (ps)
A	10	10			
B	10	10			
C	10	10			
OUT	17.02	44.49	39.56	12.4	25.98

POST LAYOUT SIMULATION

Signal	Rise Time (ps)	Fall Time (ps)	tpHL (ps)	tpLH (ps)	Propagation delay (ps)
A	10	10			
B	10	10			
C	10	10			
OUT	28.29	63.86	55.8	19.91	37.855

SR Latch

Schematic and Symbol



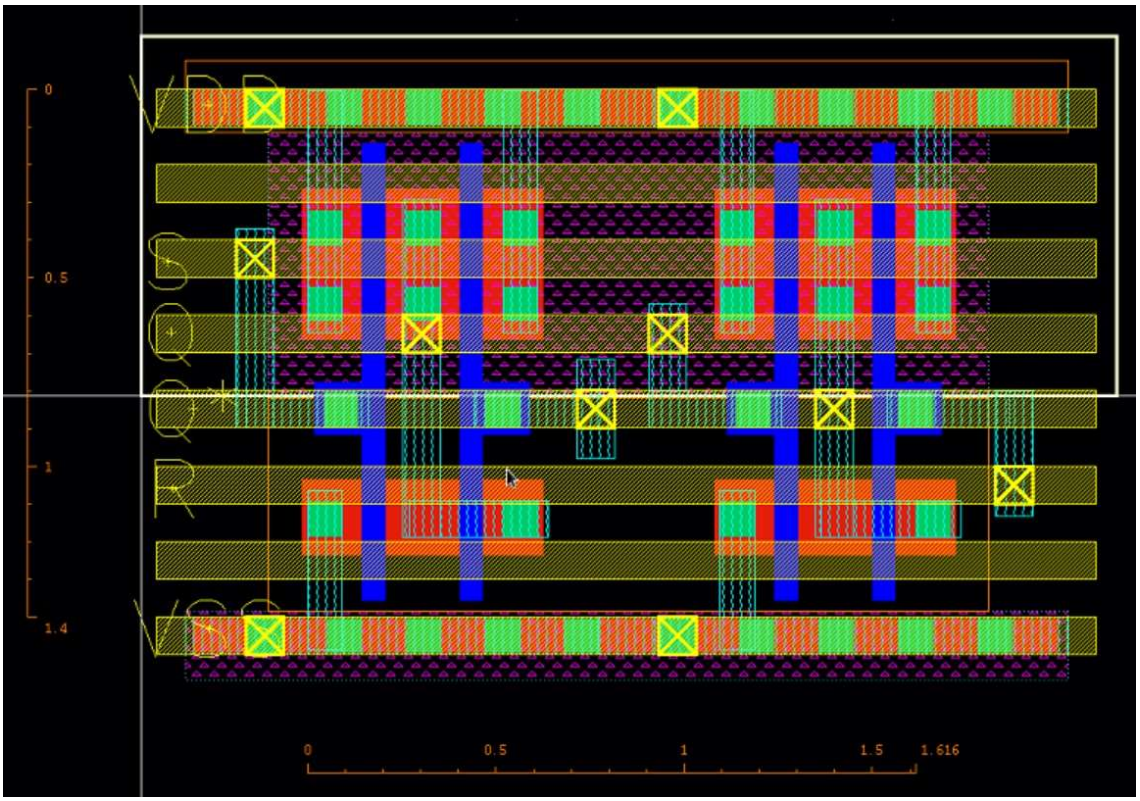
Truth Table

Characteristic equation: $Q_{next} = S + QR^*$

Characteristic Table				**Excitation Table**			
S	**R**	**Q_{next}**	**Action**	**Q**	**Q_{next}**	**S**	**R**
0	0	X	Not Allowed	0	0	X	0
0	1	1	Set	0	1	0	1
1	0	0	Reset	1	0	1	0
1	1	Q	Hold state	1	1	0	X

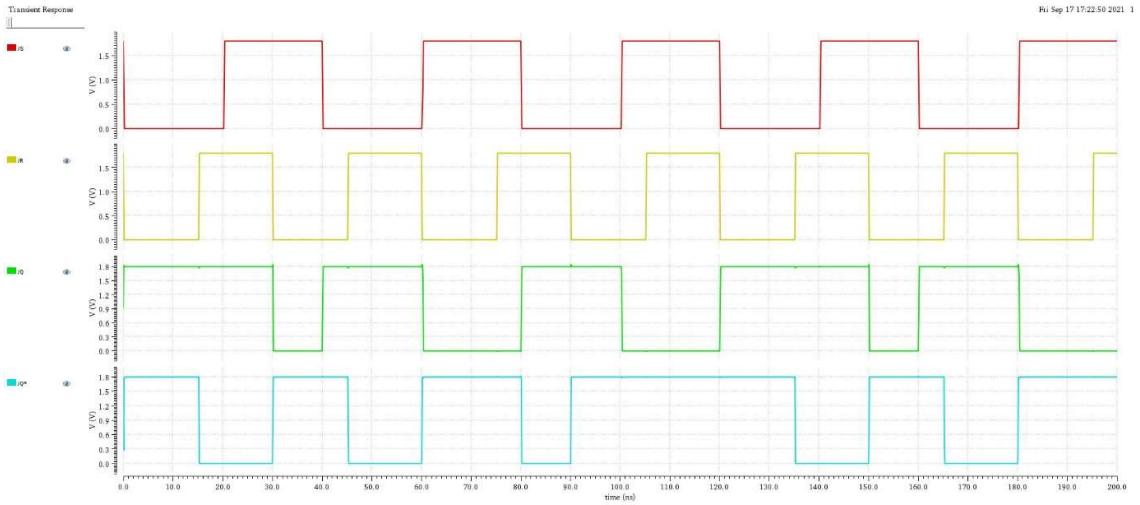
Layout

Width of SR Latch = **1.616 um**

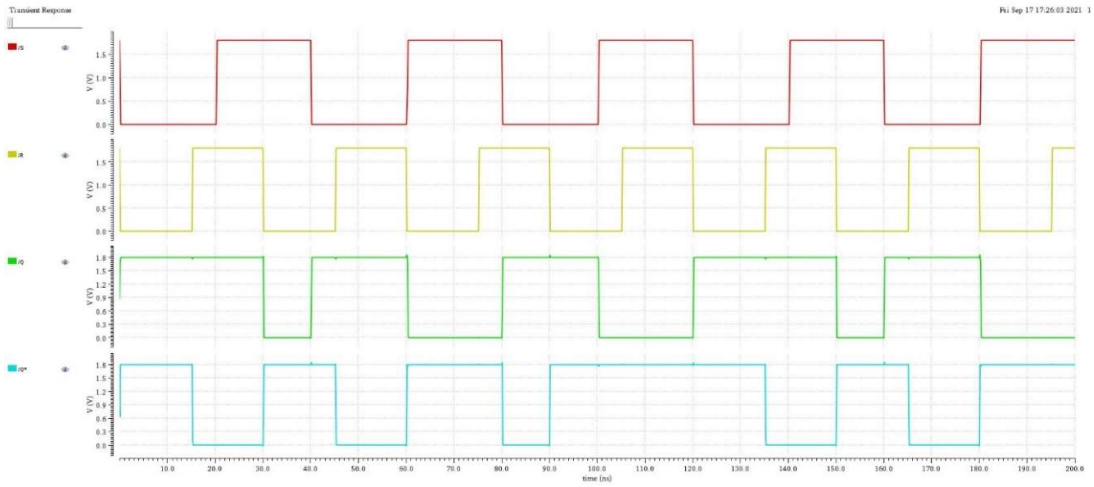


Waveform

Pre-layout Simulation



Post-layout Simulation



Timing Information

PRE LAYOUT SIMULATION

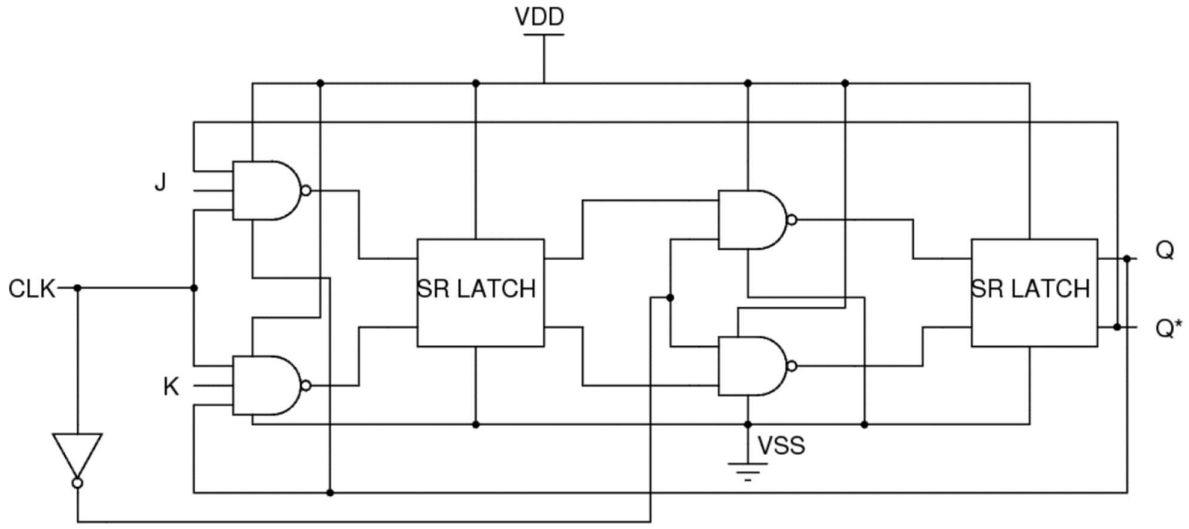
Signal	Rise Time (ps)	Fall Time (ps)	tpHL (ps)	tpLH (ps)	Propagation delay (ps)
S	10	10			
R	10	10			
Q	19.71	36.91	55.931	14.43	35.1805
Q*	26.15	38.12	29.15	16.77	22.96

POST LAYOUT SIMULATION

Signal	Rise Time (ps)	Fall Time (ps)	tpHL (ps)	tpLH (ps)	Propagation delay (ps)
S	10	10			
R	10	10			
Q	42.1	67.4	86	30	58
Q*	40	61.9	42.8	27	34.9

JK Flipflop

Schematic and Symbol



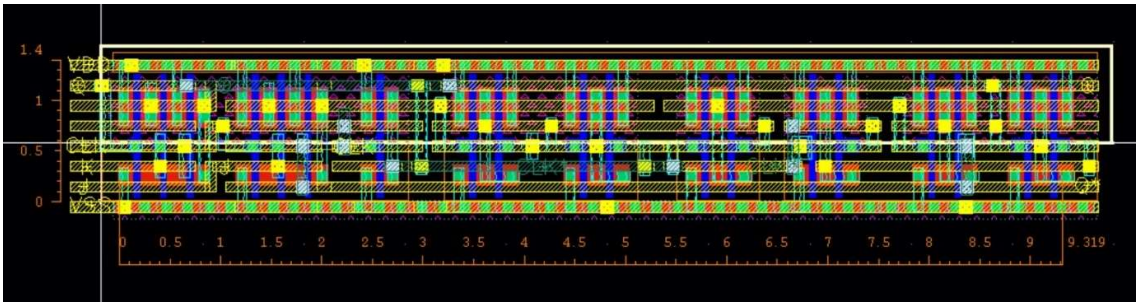
Truth Table

Characteristic equation: $Q_{next} = JQ^* + KQ$

Characteristic Table				**Excitation Table**			
J	**K**	**Q_{next}**	**Action**	**Q**	**Q_{next}**	**J**	**K**
0	0	Q	Hold	0	0	0	X
0	1	0	Reset	0	1	1	X
1	0	1	Set	1	0	X	1
1	1	Q*	Toggle	1	1	X	0

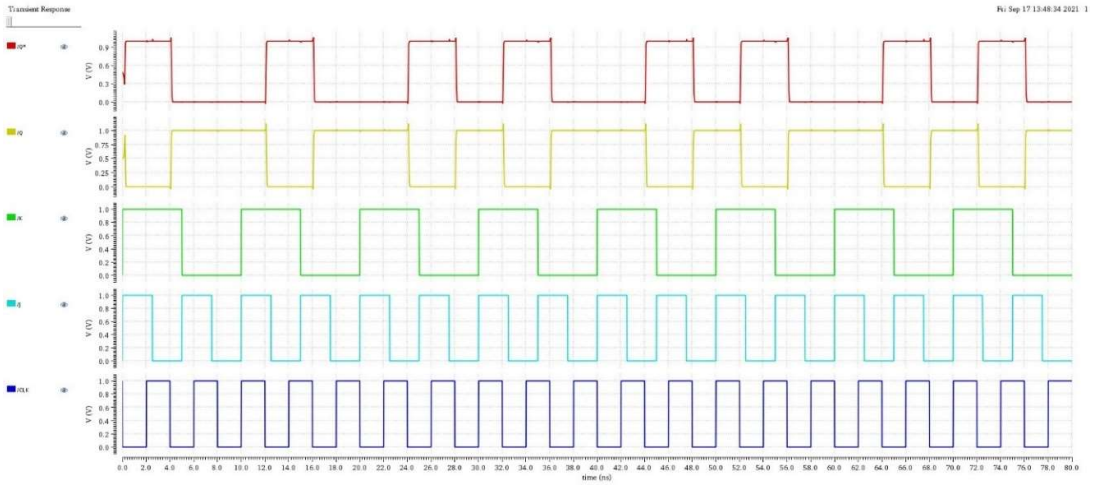
Layout

Width of JK FF = **9.319 um**

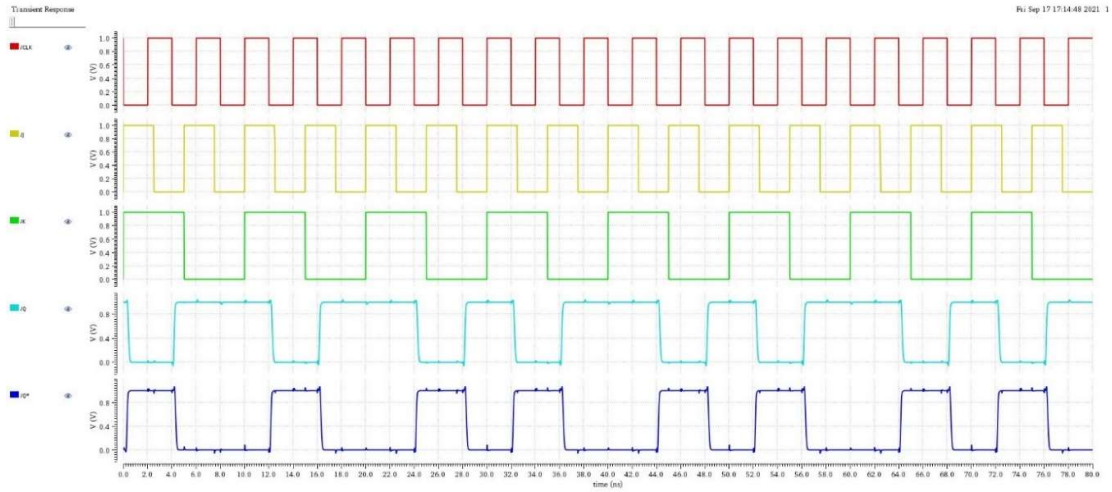


Waveform

Pre-layout Simulation



Post-layout Simulation



Timing Information

Maximum frequency = **2.5 GHz**

PRE LAYOUT SIMULATION

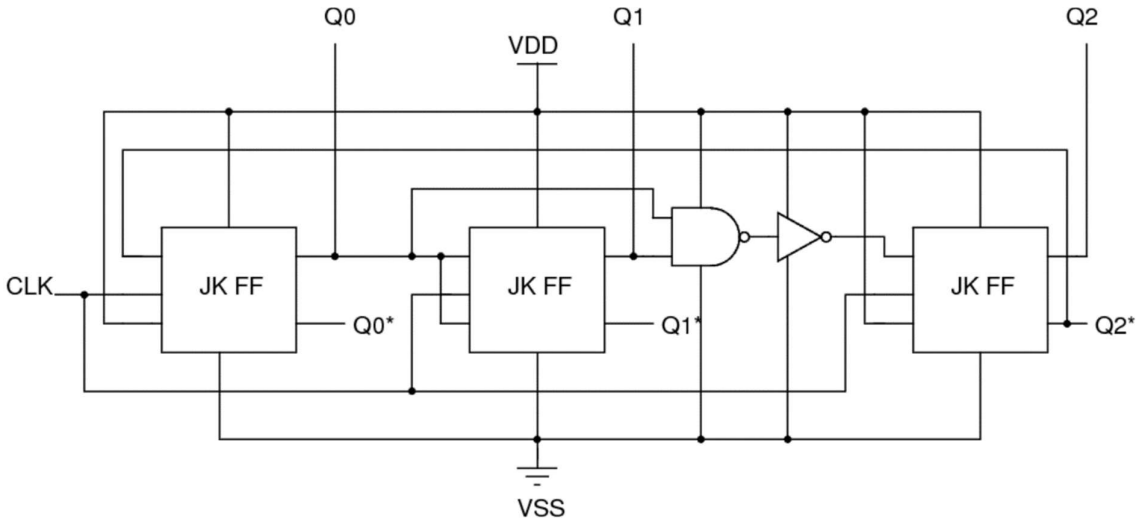
Signal	Rise Time (ps)	Fall Time (ps)	tpHL (ps)	tpLH (ps)	Propagation delay (ps)
J	10	10			
K	10	10			
CLK	10	10			
Q	39.93	53.35	134.27	85.93	110.1
Q*	41.1	54.45	128.35	84.55	106.45

POST LAYOUT SIMULATION

Signal	Rise Time (ps)	Fall Time (ps)	tpHL (ps)	tpLH (ps)	Propagation delay (ps)
J	10	10			
K	10	10			
CLK	10	10			
Q	117.35	157.453	292.1	196.59	244.345
Q*	110.8	149.67	322.7	172.2	247.45

MOD-5 Counter

Schematic



Truth Table

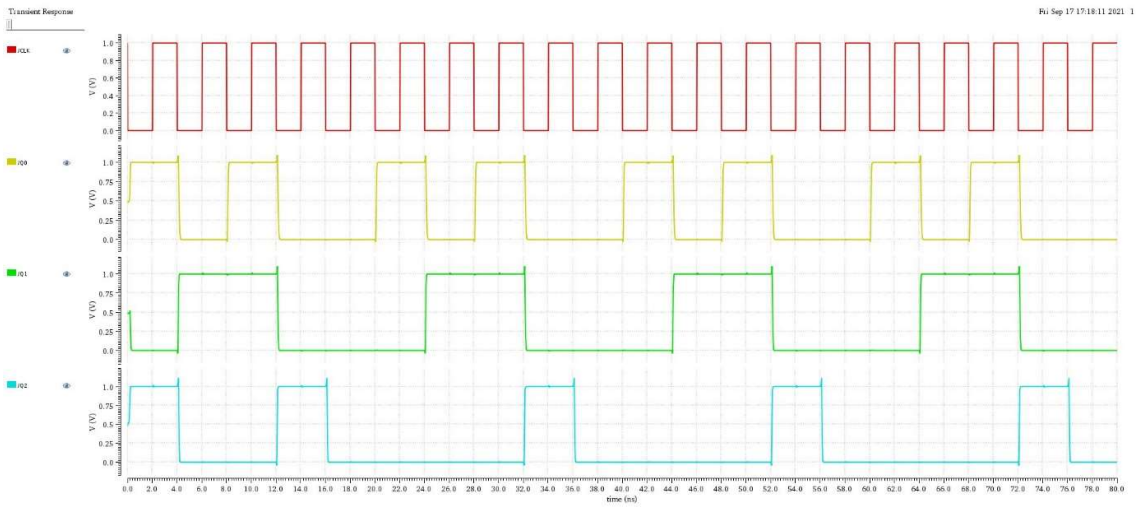
Present State			**Next State**			**Flipflop Inputs**					
Q2	**Q1**	**Q0**	**Q2**	**Q1**	**Q0**	**J2**	**K2**	**J1**	**K1**	**J0**	**K0**
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X

Layout

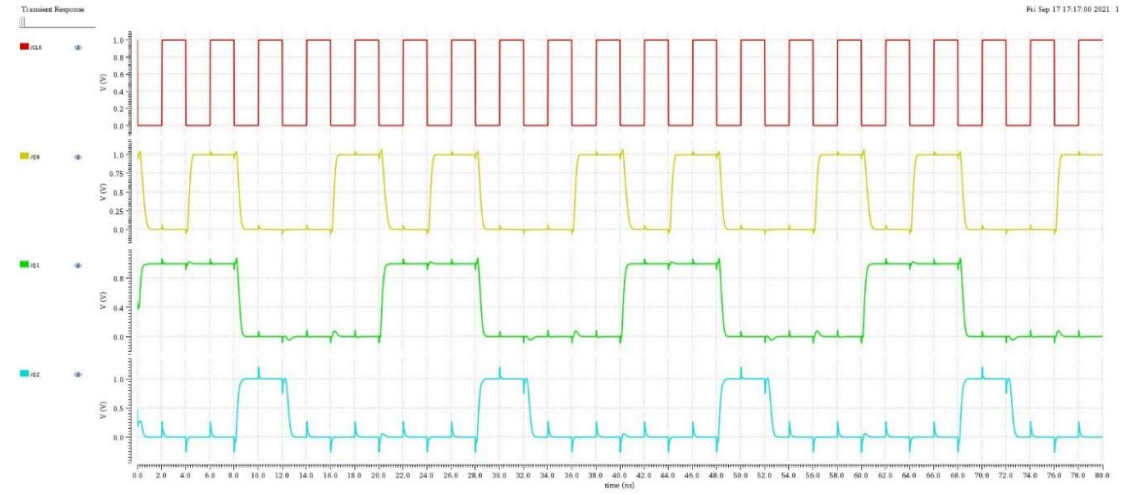
Width of counter = **30.941 um**

Waveform

Pre-layout Simulation



Post-layout Simulation



Timing Information

Maximum frequency = **1 GHz**

PRE LAYOUT SIMULATION

Signal	Rise Time (ps)	Fall Time (ps)	tpHL (ps)	tpLH (ps)	Propagation delay (ps)
CLK	10	10			
Q0	61.9	95.4	147.7	100.44	124.07
Q1	51.7	71.4	141.5	91.14	116.32
Q2	39.6	54	131.1	86	108.55

POST LAYOUT SIMULATION

Signal	Rise Time (ps)	Fall Time (ps)	tpHL (ps)	tpLH (ps)	Propagation delay (ps)
CLK	10	10			
Q0	291.7	459.5	503.6	287.9	395.75
Q1	312.9	336.5	437.7	268.8	353.25
Q2	302.3	374.1	507.7	287.8	397.75

Targets Achieved

- MOD-5 synchronous counter
- Schematics of all circuits
- Layout of all circuits
- DRC, LVS and PEX analysis of all circuits without errors
- Pre and post layout simulation waveforms for all circuits
- Timing Information of all circuits

Conclusion

A mod-5 counter design was achieved using JK flip flops.

The schematic, symbols and layouts of all components were constructed and their DRC, LVS and PEX analysis was completed. The pre-layout and post-layout waveforms were generated for all components and their timing information such as rise time, fall time, propagation delay, etc. were calculated.