

2-Input NAND Timing Report

PRE LAYOUT SIMULATION

Signal	Rise Time	Fall Time	tpHL	tpLH	Propagati on delay
	ps	ps	ps	ps	ps
A	10	10			
B	10	10			
OUT	12.33	21.17	20.85	10.39	15.62

POST LAYOUT SIMULATION

Signal	Rise Time	Fall Time	tpHL	tpLH	Propagati on delay
	ps	ps	ps	ps	ps
A	10	10			
B	10	10			
OUT	16.64	21.48	28.55	18.25	23.4