3-Input NAND Timing Report

PRE LAYOUT SIMULATION

Signal	Rise Time ps	Fall Time ps	tpHL ps	tpLH ps	Propagation delay ps
A	10	10			
B	10	10			
C	10	10			
OUT	17.02	44.49	39.56	12.4	25.98

POST LAYOUT SIMULATION

Signal	Rise Time ps	Fall Time ps	tpHL ps	tpLH ps	Propagation delay ps
A	10	10			
B	10	10			
C	10	10			
OUT	28.29	63.86	55.8	19.91	37.855