

Enhanced Product
AD7980-EP
FEATURES
16-bit resolution with no missing codes
Throughput: 1 MSPS
Low power dissipation
4 mW at 1 MSPS (VDD only)
7 mW at 1 MSPS (total)
70 μ W at 10 kSPS
INL: ± 0.6 LSB typical, ± 1.5 LSB maximum
SINAD: 91 dB @ 10 kHz
THD: -114 dB @ 10 kHz
Pseudo differential analog input range
0 V to V_{REF} with V_{REF} between 2.5 V to 5.5 V
No pipeline delay
Single-supply 2.5 V operation with 1.8 V/2.5 V/3 V/5 V logic interface
Proprietary serial interface
SPI/QSPI/MICROWIRE™/DSP compatible
Daisy-chain multiple ADCs and busy indicator
Supports defense and aerospace applications (AQEC)
Controlled manufacturing baseline
One assembly/test site
One fabrication site
Enhanced product change notification
Qualification data available on request
10-lead MSOP
Military temperature range: -55°C to +125°C
APPLICATIONS
Battery-powered equipment
Communications
ATE
Data acquisitions
Medical instruments
Table 1. MSOP, LFCSP 14-/16-/18-Bit PulSAR® ADC

Type	100 kSPS	250 kSPS	400 kSPS to 500 kSPS	≥ 1000 kSPS
18-Bit	AD7989-1¹	AD7691¹	AD7690¹ AD7989-5¹	AD7982¹
16-Bit	AD7680	AD7685¹	AD7686¹	AD7984¹
	AD7683	AD7687¹	AD7688¹	AD7980¹
	AD7684	AD7694	AD7693¹	AD7983¹
	AD7988-1¹		AD7988-5¹	
14-Bit	AD7940	AD7942¹	AD7946¹	

¹ Pin-for-pin compatible.

Rev. A

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TABLE OF CONTENTS

Features	1	Absolute Maximum Ratings	6
Applications.....	1	ESD Caution.....	6
Application Diagram Example.....	1	Pin Configurations and Function Descriptions	7
General Description	1	Typical Performance Characteristics	8
Revision History	2	Outline Dimensions.....	12
Specifications.....	3	Ordering Guide	12
Timing Specifications.....	5		

REVISION HISTORY

7/15—Rev. 0 to Rev. A

Changes to Product Title, Features Section, and Table 1	1
Added Patent Note, Note 1	1
Changes to Table 2.....	3
Changes to Table 3.....	4
Changes to Table 6.....	7
Changes to Figure 11, Figure 12, Figure 14, Figure 15	9
Changes to Figure 17, Figure 20, Figure 21.....	10
Changes to Ordering Guide	12

9/10—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.5 V, VIO = 2.3 V to 5.5 V, V_{REF} = 5 V, T_A = -55°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	IN+ – IN–	0		V _{REF}	V
Absolute Input Voltage	IN+	-0.1		V _{REF} + 0.1	V
	IN–	-0.1		+0.1	V
Analog Input CMRR	f _{IN} = 100 kHz		60		dB
Leakage Current @ 25°C	Acquisition phase		1		nA
ACCURACY					
No Missing Codes		16			Bits
Differential Linearity Error	REF = 5 V	-0.9	±0.4	+0.9	LSB ¹
	REF = 2.5 V		±0.55		LSB ¹
Integral Linearity Error	REF = 5 V	-1.5	±0.6	+1.5	LSB ¹
	REF = 2.5 V		±0.65		LSB ¹
Transition Noise	REF = 5 V		0.6		LSB ¹
	REF = 2.5 V		1.0		LSB ¹
Gain Error, T _{MIN} to T _{MAX} ²			±2		LSB ¹
Gain Error Temperature Drift			±0.35		ppm/°C
Zero Error, T _{MIN} to T _{MAX} ²		-0.62	±0.08	+0.62	mV
Zero Temperature Drift			0.54		ppm/°C
Power Supply Sensitivity	VDD = 2.5 V ± 5%		±0.1		LSB ¹
THROUGHPUT					
Conversion Rate	VIO ≥ 2.3 V up to 85°C, VIO ≥ 3.3 V above 85°C up to 125°C	0		1	MSPS
Transient Response	Full-scale step			290	ns
AC ACCURACY					
Dynamic Range	V _{REF} = 5 V		92		dB ³
	V _{REF} = 2.5 V		87		dB ³
Oversampled Dynamic Range	f _O = 10 kSPS		111		dB ³
Signal-to-Noise Ratio, SNR	f _{IN} = 10 kHz, V _{REF} = 5 V		91.5		dB ³
	f _{IN} = 10 kHz, V _{REF} = 2.5 V		87		dB ³
Spurious-Free Dynamic Range, SFDR	f _{IN} = 10 kHz		-110		dB ³
Total Harmonic Distortion, THD	f _{IN} = 10 kHz		-114		dB ³
Signal-to-(Noise + Distortion), SINAD	f _{IN} = 10 kHz, V _{REF} = 5 V		91		dB ³
	f _{IN} = 10 kHz, V _{REF} = 2.5 V		86.5		dB ³

¹ LSB means least significant bit. With the 5 V input range, 1 LSB is 76.3 µV.

² These specifications include full temperature range variation, but not the error contribution from the external reference.

³ All specifications in dB are referred to a full-scale input FSR. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

V_DD = 2.5 V, V_IO = 2.3 V to 5.5 V, V_REF = 5 V, T_A = -55°C to +125°C, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
REFERENCE					
Voltage Range		2.4		5.1	V
Load Current	1 MSPS, REF = 5 V		330		μA
SAMPLING DYNAMICS					
-3 dB Input Bandwidth			10		MHz
Aperture Delay	V _D D = 2.5 V		2.0		ns
DIGITAL INPUTS					
Logic Levels					
V _I L	V _I O > 3V	-0.3		0.3 × V _I O	V
V _I H	V _I O > 3V	0.7 × V _I O		V _I O + 0.3	V
V _I L	V _I O ≤ 3V	-0.3		0.1 × V _I O	
V _I H	V _I O ≤ 3V	0.9 × V _I O		V _I O + 0.3	μA
I _I L		-1		+1	μA
I _I H		-1		+1	μA
DIGITAL OUTPUTS					
Data Format		Serial 16 bits straight binary			
Pipeline Delay		Conversion results available immediately after completed conversion			
V _O L	I _{SINK} = 500 μA			0.4	V
V _O H	I _{SOURCE} = -500 μA	V _I O - 0.3			V
POWER SUPPLIES					
V _D D		2.375	2.5	2.625	V
V _I O	Specified performance	2.3		5.5	V
V _I O Range		1.8		5.5	V
Standby Current ^{1,2}	V _D D and V _I O = 2.5 V, 25°C		0.35		μA
Power Dissipation	V _D D = 2.625 V, V _R EF = 5 V, V _I O = 3 V				
Total	10 kSPS throughput		70		μW
	1 MSPS throughput		7.0	10	mW
V _D D Only			4		mW
REF Only			1.7		mW
V _I O Only			1.3		mW
Energy per Conversion			7.0		nJ/sample
TEMPERATURE RANGE					
Specified Performance	T _{MIN} to T _{MAX}	-55		+125	°C

¹ With all digital inputs forced to V_IO or GND as required.

² During the acquisition phase.

TIMING SPECIFICATIONS

–55°C to +125°C, VDD = 2.37 V to 2.63 V, VIO = 3.3 V to 5.5 V, unless otherwise stated. See Figure 2 and Figure 3 for load conditions.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t _{CONV}	500		710	ns
Acquisition Time	t _{ACQ}	290			ns
Time Between Conversions	t _{CYC}	1000			ns
CNV Pulse Width (\overline{CS} Mode)	t _{CNVH}	10			ns
SCK Period (\overline{CS} Mode)	t _{SCK}				ns
VIO Above 4.5 V		10.5			ns
VIO Above 3 V		12			ns
VIO Above 2.7 V		13			ns
VIO Above 2.3 V		15			ns
SCK Period (Chain Mode)	t _{SCK}				ns
VIO Above 4.5 V		11.5			ns
VIO Above 3 V		13			ns
VIO Above 2.7 V		14			ns
VIO Above 2.3 V		16			ns
SCK Low Time	t _{SCKL}	4.5			ns
SCK High Time	t _{SCKH}	4.5			ns
SCK Falling Edge to Data Remains Valid	t _{HSDO}	3			ns
SCK Falling Edge to Data Valid Delay	t _{DSDO}				
VIO Above 4.5 V			9.5		ns
VIO Above 3 V			11		ns
VIO Above 2.7 V			12		ns
VIO Above 2.3 V			14		ns
CNV or SDI Low to SDO D15 MSB Valid (\overline{CS} Mode)	t _{EN}				
VIO Above 3 V			10		ns
VIO Above 2.3 V			15		ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance (\overline{CS} Mode)	t _{DIS}			20	ns
SDI Valid Setup Time from CNV Rising Edge	t _{SSDICNV}	5			ns
SDI Valid Hold Time from CNV Rising Edge (\overline{CS} Mode)	t _{HSDICNV}	2			ns
SDI Valid Hold Time from CNV Rising Edge (Chain Mode)	t _{HSDICNV}	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	t _{SSCKCNV}	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	t _{HSCKCNV}	5			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	t _{SSDISCK}	2			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	t _{HSDISCK}	3			ns
SDI High to SDO High (Chain Mode with Busy Indicator)	t _{DSDOSDI}			15	ns

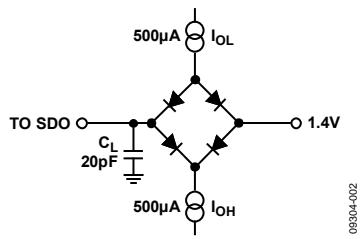
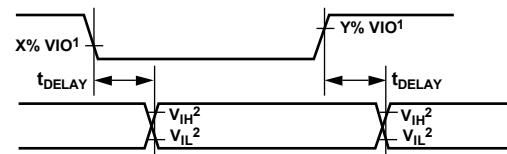


Figure 2. Load Circuit for Digital Interface Timing



¹FOR VIO \leq 3.0V, X = 90 AND Y = 10; FOR VIO > 3.0V X = 70, AND Y = 30.
²MINIMUM V_{IH} AND MAXIMUM V_{IL} USED. SEE DIGITAL INPUTS SPECIFICATIONS IN TABLE 3.

09304-003

Figure 3. Voltage Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Inputs IN+, IN– to GND	-0.3 V to $V_{REF} + 0.3$ V or ± 130 mA
Supply Voltage REF, VIO to GND	-0.3 V to +6 V
VDD to GND	-0.3 V to +3 V
VDD to VIO	+3 V to -6 V
Digital Inputs to GND	-0.3 V to VIO + 0.3 V
Digital Outputs to GND	-0.3 V to VIO + 0.3 V
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (10-Lead MSOP)	200°C/W
θ_{JC} Thermal Impedance (10-Lead MSOP)	44°C/W
Lead Temperature	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.
Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

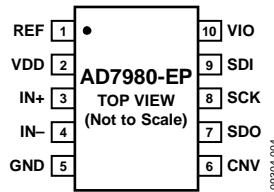


Figure 4. 10-Lead MSOP Pin Configuration

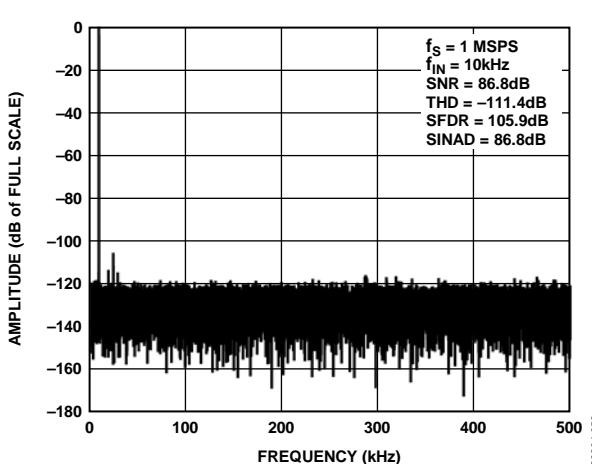
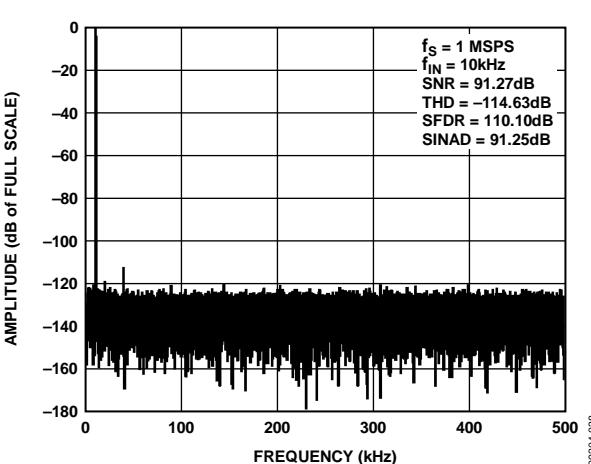
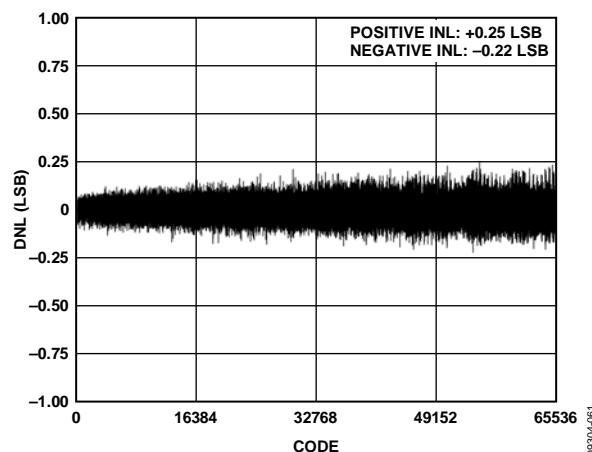
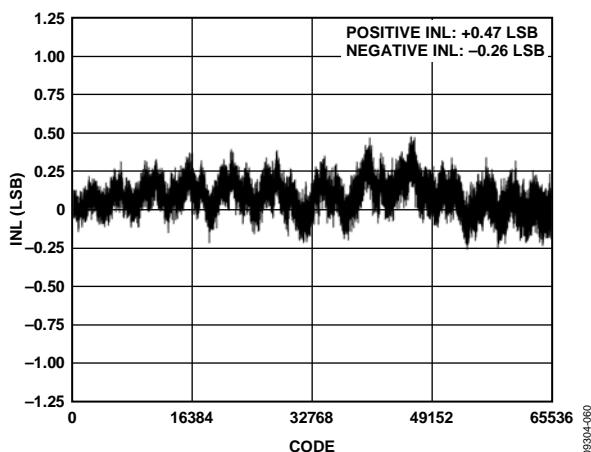
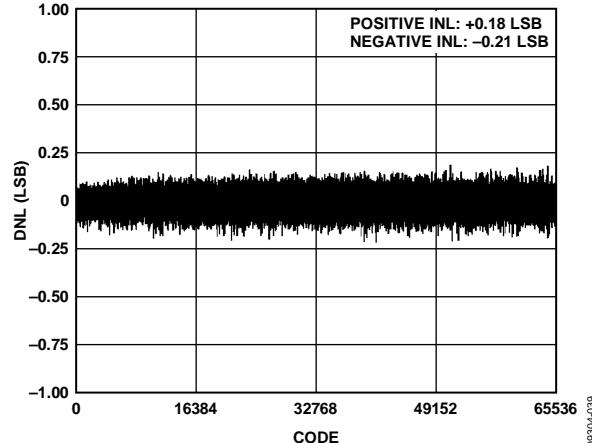
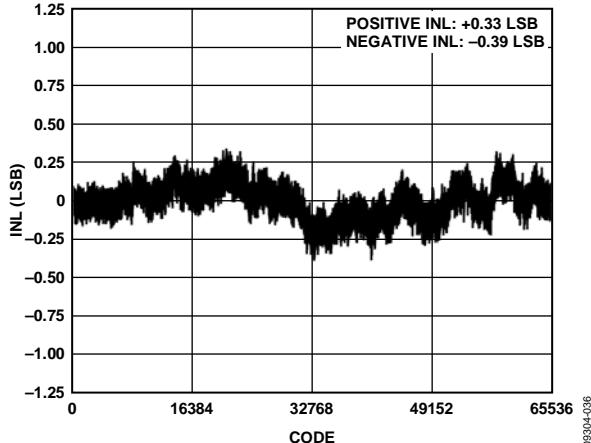
Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type ¹	Description
1	REF	AI	Reference Input Voltage. The REF range is from 2.4 V to 5.1 V. It is referred to the GND pin. This pin should be decoupled closely to the pin with a 10 μ F capacitor.
2	VDD	P	Power Supply.
3	IN+	AI	Analog Input. It is referred to IN-. The voltage range, for example, the difference between IN+ and IN-, is 0 V to V_{REF} .
4	IN-	AI	Analog Input Ground Sense. To be connected to the analog ground plane or to a remote sense ground.
5	GND	P	Power Supply Ground.
6	CNV	DI	Convert Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode of the part, chain, or CS mode. In CS mode, it enables the SDO pin when low. In chain mode, the data should be read when CNV is high.
7	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
8	SCK	DI	Serial Data Clock Input. When the part is selected, the conversion result is shifted out by this clock.
9	SDI	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows. Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. CS mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low; if SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled.
10	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).

¹AI = analog input, DI = digital input, DO = digital output, and P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 2.5 V, V_{REF} = 5.0 V, VIO = 3.3 V, unless otherwise noted.



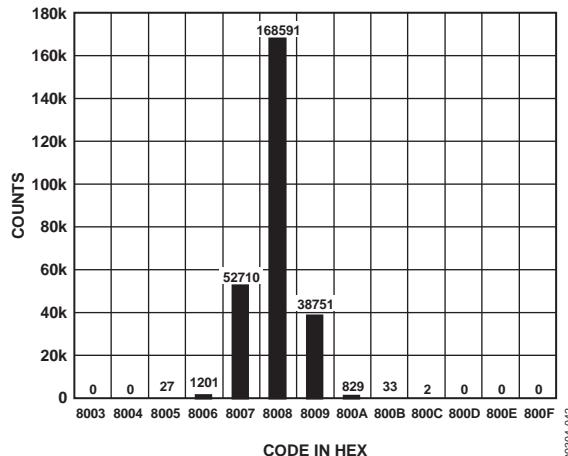


Figure 11. Histogram of a DC Input at the Code Center, REF = 5 V

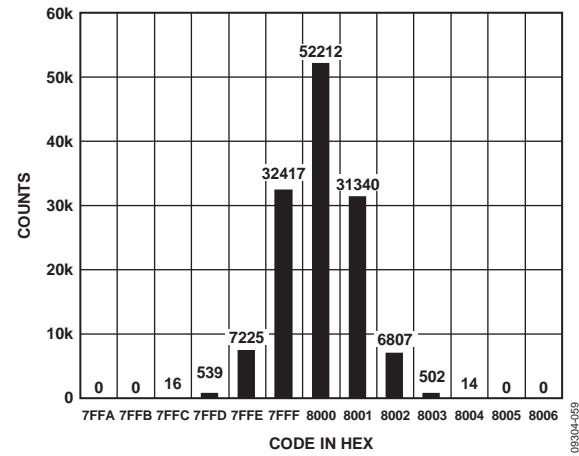


Figure 14. Histogram of a DC Input at the Code Center, REF = 2.5 V

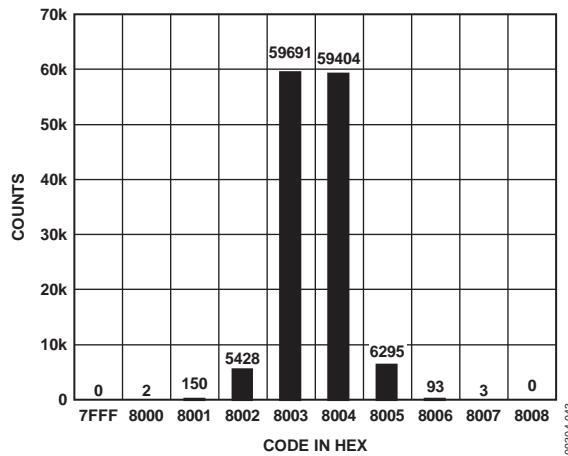


Figure 12. Histogram of a DC Input at the Code Transition, REF = 5 V

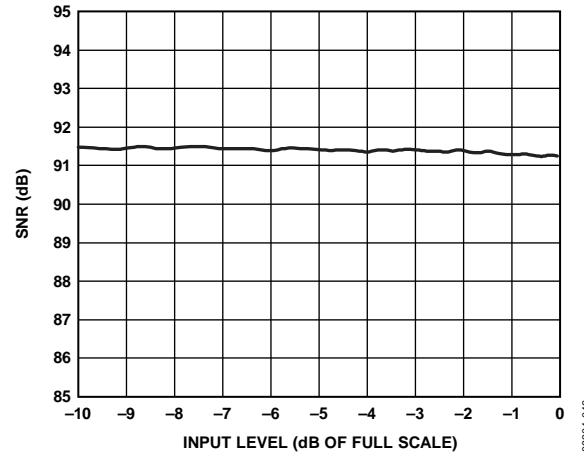


Figure 15. SNR vs. Input Level

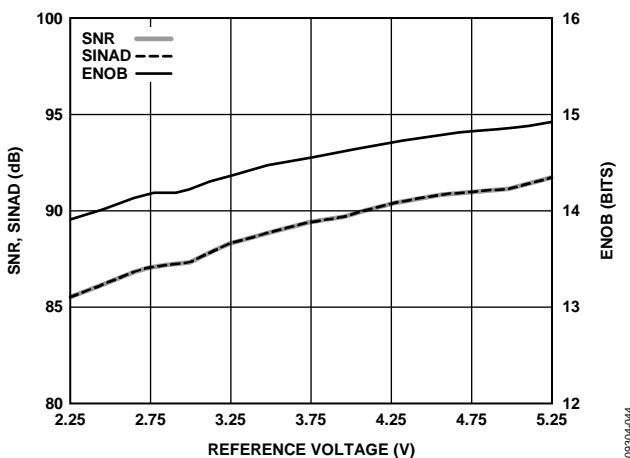


Figure 13. SNR, SINAD, and ENOB vs. Reference Voltage

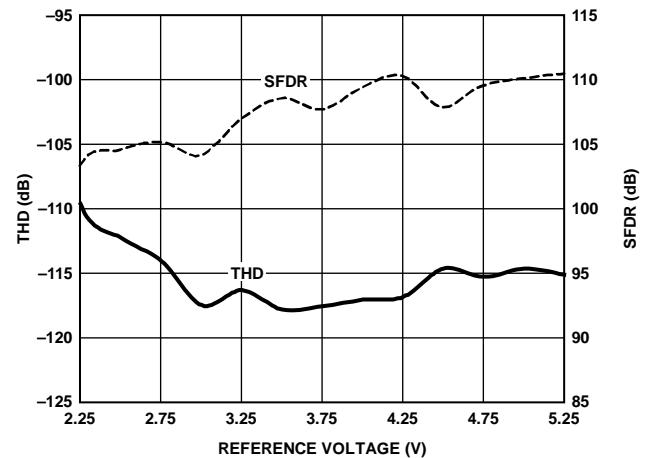


Figure 16. THD, SFDR vs. Reference Voltage

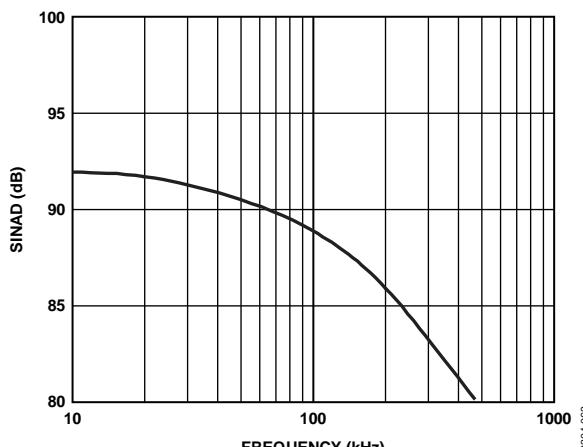


Figure 17. SINAD vs. Frequency

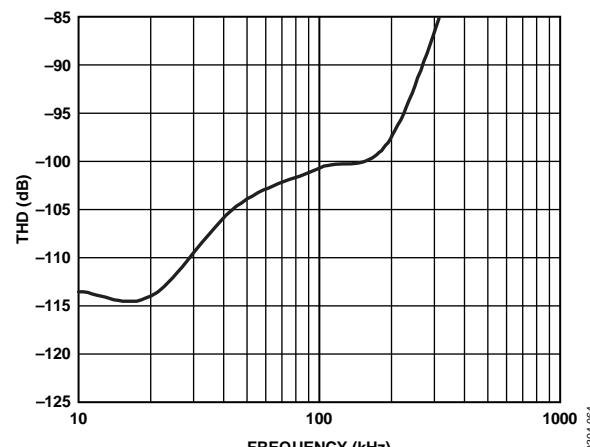


Figure 20. THD vs. Frequency

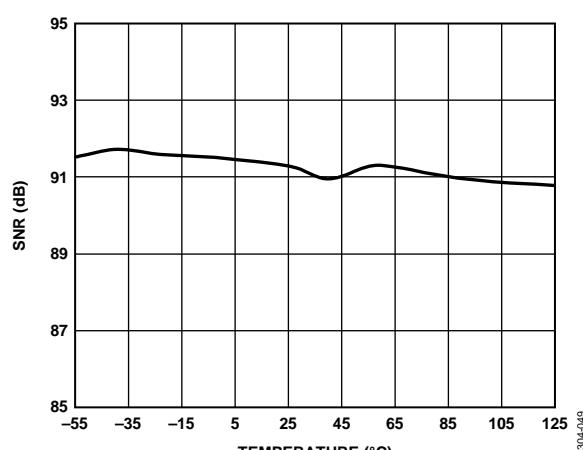


Figure 18. SNR vs. Temperature

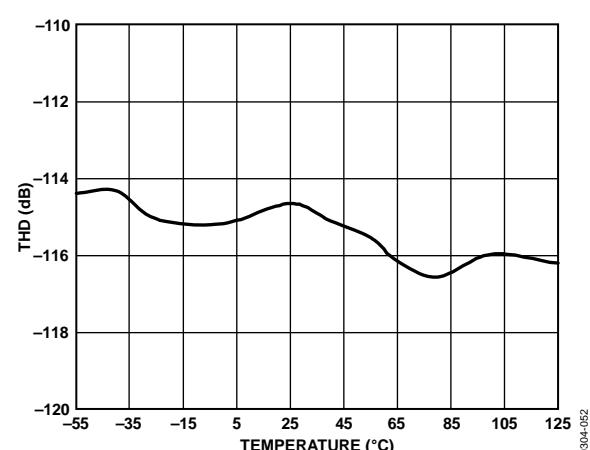


Figure 21. THD vs. Temperature

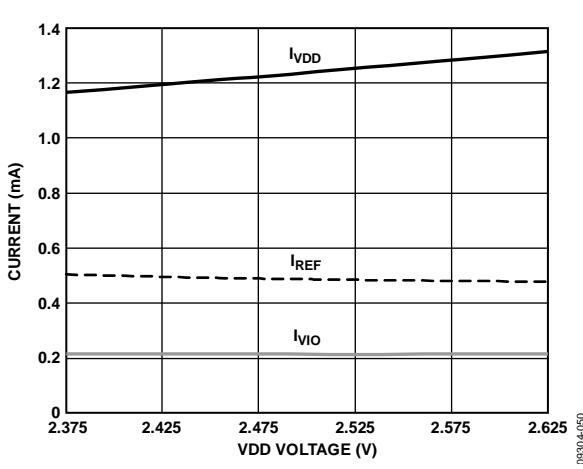


Figure 19. Operating Currents vs. Supply

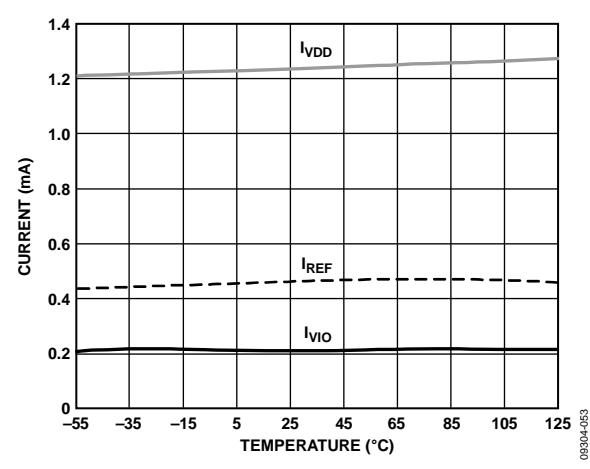


Figure 22. Operating Currents vs. Temperature

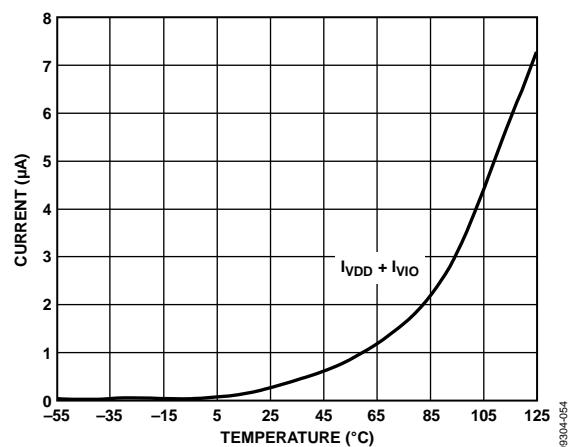
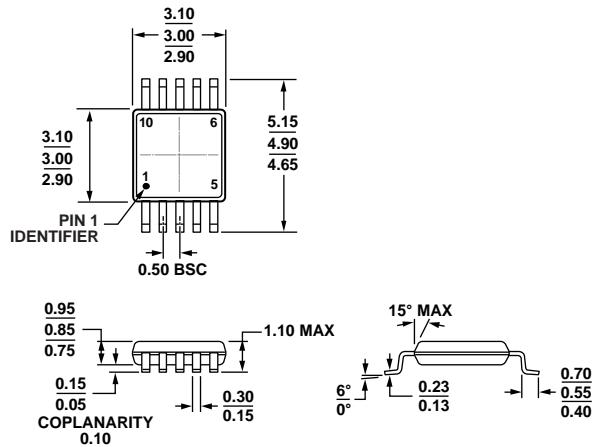


Figure 23. Power-Down Currents vs. Temperature

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

091709-A

Figure 24.10-Lead Mini Small Outline Package [MSOP]

(RM-10)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Integral Nonlinearity	Temperature Range	Ordering Quantity	Package Description	Package Option	Branding
AD7980SRMZ-EP-RL7	±1.5 LSB max	−55°C to +125°C	Reel, 1,000	10-Lead MSOP	RM-10	C78
AD7980SRMZ-EP	±1.5 LSB max	−55°C to +125°C		10-Lead MSOP	RM-10	C78

¹ Z = RoHS Compliant Part.