SPECIAL PROJECT-II

A

Report

on

Design of Two-Stage CMOS Operational Amplifier in 180nm Technology

Submitted by:

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Submitted to:

Dr. P Akhendra Kumar

Submitted on:

2nd May 2021.

IFHE

Faculty of Science and Technology, IFHE University

(May 2021).

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Prepared in partial fulfillment of the

SPECIAL PROJECT – II Course

SUBMITTED TO:

Dr. P Akhendra Kumar

Faculty of Science & Technology, IFHE University

(May 2021)

DECLARATION

We declare that the work contained in the Project Report is original and it has been done by our group under the supervision of **Dr. P. Akhendra Kumar**. The work has not been submitted to any other University for the award of any degree or diploma.

Date: 2nd May 2021.

Signature of the Student

Eeshwar Vannemreddy

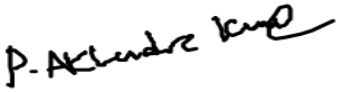
P. Sinduja

P. Venkata Ramya

CERTIFICATE

This is to certify that the Project Report entitled **Design of Two-Stage CMOS Operational Amplifier in 180nm Technology**, submitted by **our group** in the Department of **Electronics and Communication Engineering** (**ECE**) at **IcfaiTech** (Deemed to be University) for the award of the **degree of B.Tech** in the **Faculty of Science and Technology** is a record of bonafide work carried out under my guidance and supervision.

Date: 2nd May 2021.



Signature of the Supervisor

Name: **Dr. P. Akhendra Kumar**

Designation: **Professor**

Department: **ECE**

Institute: **IcfaiTech**

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ABSTRACT

Since the project is based on the "***Design of a Two-Stage CMOS Operational Amplifier in 180nm Technology***". Therefore, this paper presents the design and analysis of a high-gain, low-power, two-stage CMOS operational amplifier (op-amp) for a sigma-delta ADC. Op-amp topologies, such as folded cascade are discussed in this paper. The theoretical and topological analyses of each design are highlighted in detail, including the trade-off among various parameters such as gain, noise, output swings, and power consumption. The designs have been simulated using 0.18 μ m CMOS technology with EDA tools. From the simulation results, gain output swing, slew rate, and CMRR are calculated.

Keywords: Two-Stage CMOS Op-Amp, CMRR, Slew rate, Gain, power consumption.

Signature of Student

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Date: 2nd May 2021

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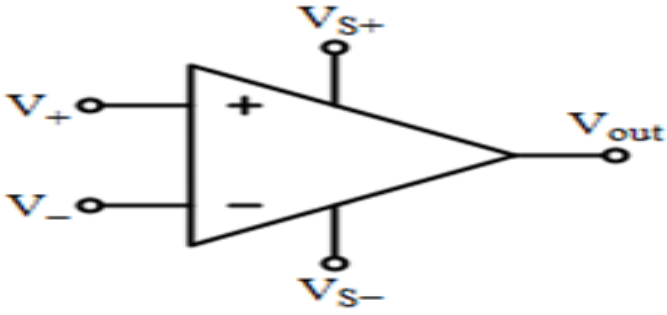
I. INTRODUCTION:

1.1. What is an Operational Amplifier?

The **Operational Amplifier** (op-amp) is a fundamental, versatile and integrated building block in analog circuit design. **Op-amp in general is a 3-terminal device** with an **inverting input** (denoted by "-" sign), a **non-inverting input** (denoted by "+" sign), and an **output terminal**. The basic principle used in an Op-amp is to "*have a high forward dc gain to implement the negative feedback so that when negative feedback is applied, the closed-loop transfer function of an op-amp is independent of its gain".* As the transistor channel length and supply voltages are shrinking, the CMOS is becoming a great success among all because it can be easily scaled down to dimensions like micrometer and nanometer. Due to scaling down of channel length, more transistors can be integrated on a single chip which leads to the need for high operating frequency which can be implemented with the help of CMOS op-amp. Op-amps are linear devices having applications in various scientific devices and are extensively used to perform mathematical operations like addition, subtraction, integration, and so on. Op-amps are also used in signal conditioning, in many biomedical applications to design a low-frequency active pass filter. Op-amps with two or more stages are widely used to achieve higher gain. One of the most popular Op-amps is a two-stage Op-amp which is the aim of this work.



- V_+ : non-inverting input
- V_- : inverting input
- V_{out} : output
- V_{S+} : positive power supply
- V_{S-} : negative power supply

Fig1. Schematic diagram of an Op-Amp.

1.2. OPERATIONAL AMPLIFIER INPUT MODES

Op-Amp has **3** types of input modes. They are:

1. Single-Ended Mode
2. Differential Mode / Double-Ended Mode
3. Common Mode.

1. **Single-Ended Mode:**

   If the input signal is applied to only one of the inputs and the other input terminal is connected to the ground it is said to be operating in Single-Ended Mode.

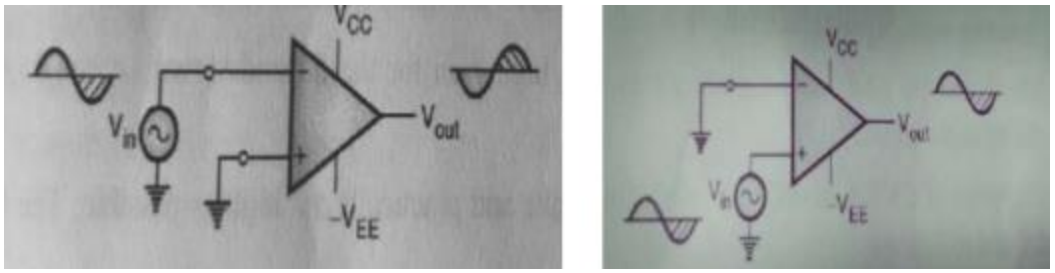


Fig2. Single-Ended Mode

2. **Differential Mode / Double-Ended Mode:**

   In this mode, two opposite polarity signals are applied to the two inputs of an op-amp. The difference between the input signals is amplified appears at the output.

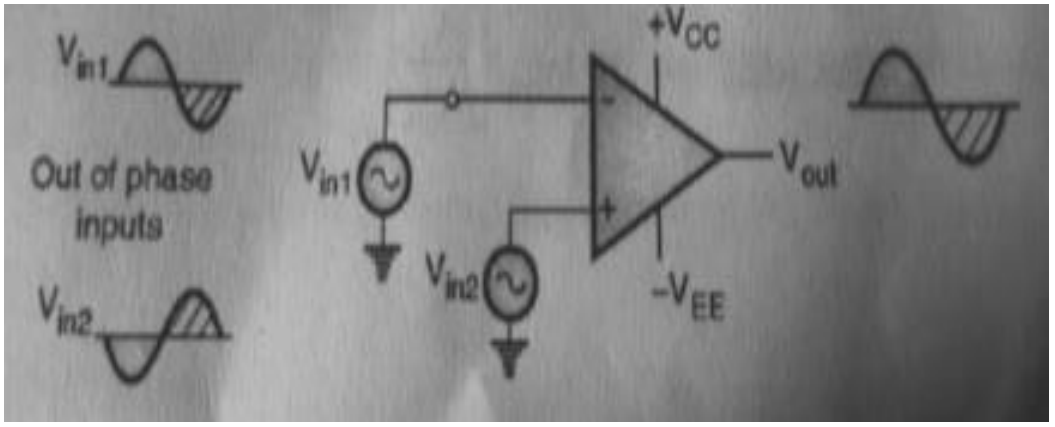


Fig3. Differential Mode / Double-Ended Mode

3. **Common Mode:**

In this mode of operation, the same input signal is applied to both the input terminals. Ideally, a zero voltage should be produced by the op-amp.

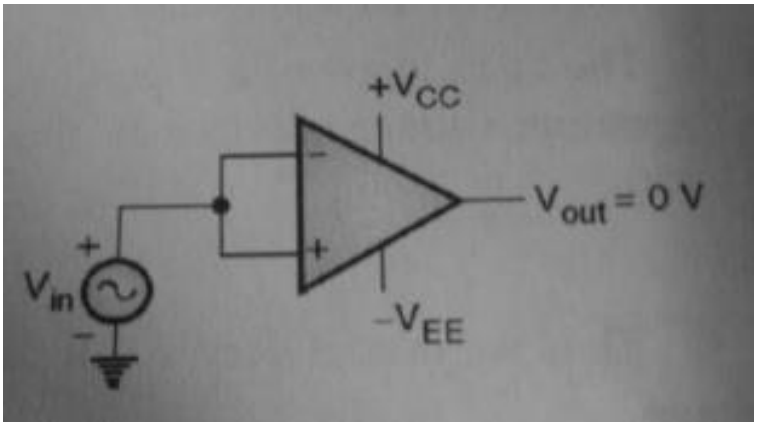


Fig4. Common Mode

1.3. Why is Op-Amp is not used as an amplifier in the open-loop configuration?

- Due to very open-loop gain, distortion is introduced in the amplified output signal.
- The open-loop gain does not remain constant but varies with temperature and power supply as well due to the mass production technique.
- The bandwidth of an Op-Amp is very small almost equal to zero.

Therefore for these above reasons, the open-loop Operational Amplifier is not used in the practice as an amplifier.

1.4. Applications of Operational Amplifier:

- Since Operational Amplifiers are popular building blocks in electronic circuits, they find applications in most consumer and industrial electronic systems.

- Operational amplifiers can be configured to work as inverting amplifiers, non-inverting amplifiers; to perform mathematical operations like addition, subtraction, multiplication, division, differentiation, and integration. It can also be used in the construction of filters (high-pass, low-pass, band-pass, and band-reject). If required, an open-loop op-amp can be forced to act as a comparator.

- Operational amplifiers with positive feedback can be used in the construction of oscillators. They are also used in non-linear circuits such as logarithmic and anti-logarithmic amplifiers.

- Operational amplifiers also discover applications as Voltage sources, Current sources, and Current sinks, and DC and AC Voltmeters. Op-amps are additionally utilized in signal handling circuits, for example, Sample-and-Hold circuits, Precision Rectifier, and Clamping circuits.

Few more applications of the op-amp are:

1. Inverting amplifier
2. Non-inverting amplifier
3. Differentiator
4. Integrator
5. Summing amplifier
6. Differential amplifier
7. Instrumentation amplifier

II. LITERATURE REVIEW:

2.1. Two-Stage CMOS Operational Amplifier:

A two-stage CMOS Op-amp consists of three stages. They are:

1. The *first stage* is a **differential amplifier**.
2. The *second* stage is the **gain stage** which can be a **common source** stage.
3. The *third stage* is an **output buffer**.

"The ***Output Buffer*** is used only if the Operational Amplifier is to drive large capacitive or/and resistive loads".

Op-amps can have different topologies, a two-stage CMOS op-amp is one such topology. The two-stage CMOS Opamp topology is used where high input impedance and low output impedance are required. **Figure 5** below shows the basic configuration of a two-stage CMOS Op-amp. Here transistors M1, M2, M3, M4 form the first stage which is the differential gain stage, and transistors M6 and M7 from the second stage which is the gain stage. In the first stage, transistor M5 provides the biasing to the entire circuit, transistors M1 and M2 form the differential input pair actively loaded by a current mirror pair formed by transistors M3 and M4. In the second stage, transistor M6 is a common source amplifier actively loaded by transistor M7.

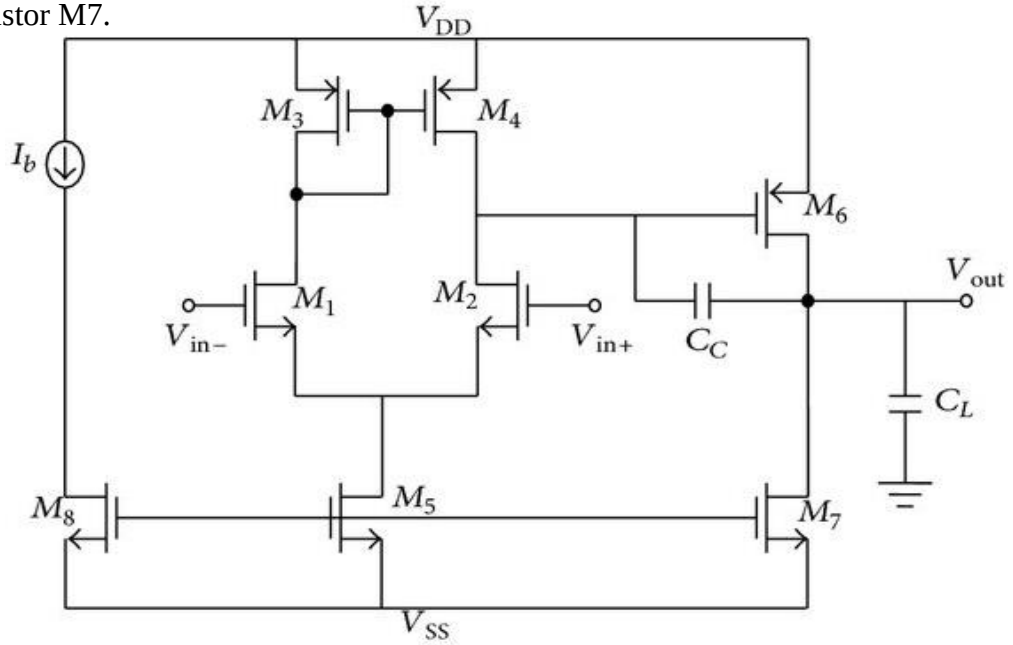


Fig.5. Two-stage CMOS Topology

2.2. Design of Two-Stage CMOS Operational Amplifier:

The generation towards low voltage low-power silicon chip systems has been growing due to the increasing demand for small size and longer battery life for portable applications in all marketing segments including telecommunication, medical, computers, and consumer electronics. The operational amplifier is doubtless one of the most useful devices in analog electronic circuitry. Op-amps are built with different levels of complexity to be used to obtain functions ranging from a simple dc bias generation to high-speed amplification or filtering. With only a handful of external components, it can perform a different type of analog signal processing tasks. Op-amps are among the most broadly used electronic devices today, being used in a huge array of consumer, industrial, and scientific devices. Operational Amplifiers, more commonly known as Op-amps, are among the most widely used building blocks in Analog Electronic Circuits. Op-amps are linear devices that have nearly all the properties required for not only ideal DC amplification but is used extensively for signal conditioning, filtering, and for performing mathematical calculations such as addition, subtraction, integration, differentiation, etc. Generally, an Operational Amplifier is a 3-terminal device. It consists mainly of an Inverting input denoted by a negative sign, (”-”) and the other a Non-inverting input denoted by a positive sign (” +”) is the symbol for the op-amp. Both these inputs are very high impedance. The output signals of an Operational Amplifier are the magnified difference between the two input signals. Generally, the input stage of an Operational amplifier is often a differential amplifier. An operational amplifier is a DC-coupled differential input voltage amplifier with a rather high gain. In most general-purpose op-amps there is a single-ended output. Usually, an op-amp produces an output voltage a million times broad than the voltage difference across its two input terminals. For most general applications of an op-amp, negative feedback is used to control the large voltage gain. The negative feedback also largely determines the magnitude of its output (” closed-loop”) voltage gain in numerous amplifier applications. The op-amp acts as a comparator when used without negative feedback, and even in certain applications with positive feedback for regeneration. An ideal Op-amp is characterized by a very high input impedance (ideally infinite) and low output impedance at the output terminal. To make it simple the op-amp is one type of differential amplifier. This section deeply discusses the basic concept of the op-amp. An amplifier with the general characteristics of very high voltage gain, very high input resistance, and very low output resistance generally is a touch on as an op-amp. Most analog applications use an Op-Amp that has some quantity of negative feedback. The Negative feedback is used to tell the Op-Amp how much to amplify a signal. And since op-amps are so highly used to

implement a feedback system, the required precision of the closed-loop circuit determines the open-loop gain of the system. For this design process, we will first demonstrate the formula of the main properties of an operational amplifier in Section, then we will introduce how we find the proper parameters for our design in Section III, the simulation result of the design will be presented in Section IV.

The theoretical and topological analyses of each design are highlighted in detail, including the trade-off among various parameters such as gain, noise, output swings, and power consumption. To design a CMOS OP-AMP the required steps include choosing the basic structure of the op-amp, deciding on a suitable configuration determination of the type of compensation needed for meeting the specification, selection of the dc currents and transistor sizes, physical implementation of the design, fabrication, and measurement. Here a CMOS two-stage operational amplifier has been used and operated at 1.8 V power supply at 0.18 micron (i.e., 180 NM) technology, where the input is dependent on Bias Current. The op-amp provides a gain of 63dB and a bandwidth of 140 kHz for a load of 1 pF. This op-amp has a Common Mode gain of -25 dB, an output slew rate of 32 V /μs, along with output voltage swing. The power consumption for the op-amp is 300μW. The designs have been simulated using 0.18 μ m CMOS technology with EDA tools. As we all know, when an ideal OP-AMP is given an input of very high impedance the output is low i.e ideally zero--thus, the op-amp is one type of differential amplifier. Therefore, in most of the analog applications, we use op-amp with some amount of negative feedback (negative feedback gives the amplifying value of the signal to op-amp). After we initially determine the parameters, we use Parameter Analysis in Cadence Virtuoso to optimize our final design and the simulation results. Therefore, this design satisfies all the parameters and mainly we achieved high differential-mode voltage gain(Adm), slew rate, and wide unity gain phase margin.

2.3. WORKING OF THE CIRCUIT:

Fig. 6 is equivalent to typical CMOS Op-Amp, includes three subsections: differential gain stage with next gain stage and bias stage.

The primary phase of Op-Amp is a differential amplifier made up of transistors M1, M2, M3, and M4. This is a current mirror (CM) with an active type of load utilized here has three particular preferences.

The second stage is used to deliver high gain to the amplifier and is made up of transistors M5 and M6.

The biasing circuit stage of the amplifier is accomplished with transistors M5, M6, M7, and M8

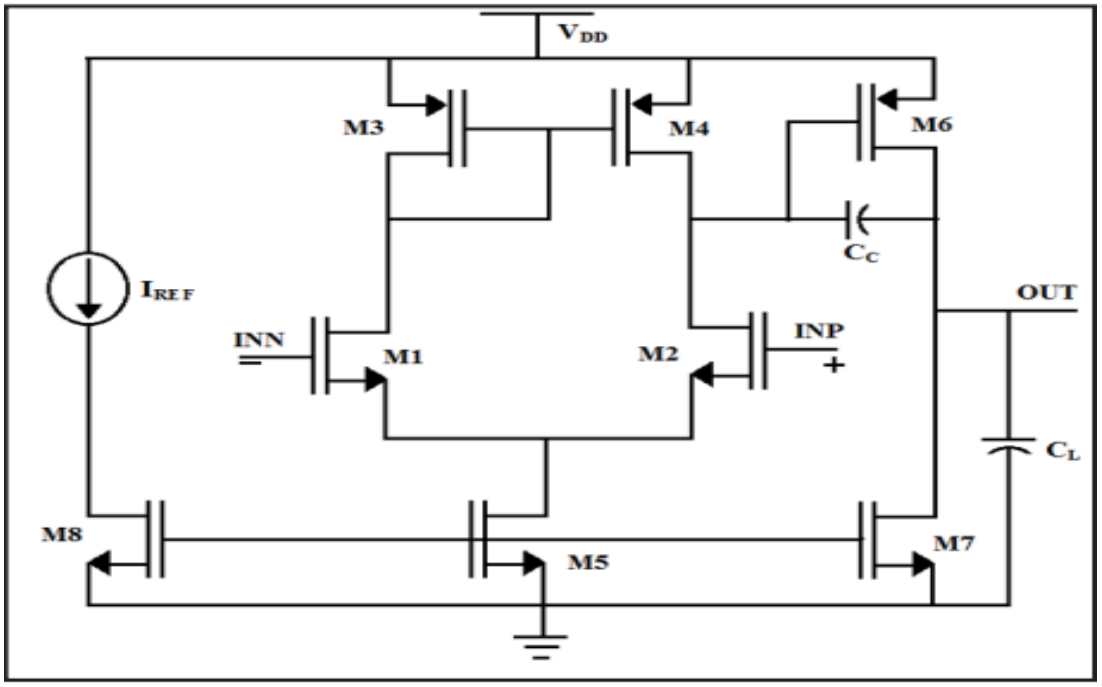


Fig.6: Stage CMOS Op-Amp

1) Design of Cc:

To satisfy the phase margin of 60◦ we need Cc > 0.22CL since we have CL = 1pF so we can use Cc > 220fF. To achieve slew rate 10V /|mus we need Cc = 10pf, to meet a balance between two requirements, and we choose Cc = 3pf

2) Design of M1 and M2:

We have **gm1 = GBW × Cc × 2π** and **GBW** is also called unity gain frequency, which is listed in the design goal with the value of 100MHZ. So we need to apply that gm1=100MHz × 5pF × 2π = 302μ and for convince we choose a litter larger value 510μ. Finally, (W/L) = 14.8 so we use 20 as the final value of the ratio.

3) Design of M3 and M4:

To get more than 800mV of the output range, we need to at least 800mV input common-mode voltage range before the zero points, where the gain is 1. This characteristic parameter can also be used to determine the size of the MOSFET M1 and M2. And by following the above application we finally get $(W/L)_{3,4} \approx 50$

4) Design of M5 and M8:

In the meanwhile, we also need to fit the proper value of ICMR(-) to determine the size of MOSFET M5. Approximately we can choose $(W/ L)_5 = 30$ and $(W/L)_8 = 10$

5) Design of M6:

And also we need $g_{m2} > g_{m1} / 0.22$, so we need $g_{m2} > 2318\mu$, we want $V_{DS3} = V_{DS4} = V_{DS6}$ and $V_{GS3} = V_{GS4} = V_{GS6}$, $(W/L)_6 = 150$.

6) Design of M7:

$(W/L)_7 = (W/L)_5 = 10$

7) Design of Rz:

$R_z = 1/g_{m2} = 5k$

8) Common and differential mode gain:

After initially determining the parameters of the MOSFETs, we need to check output voltage gain, then we may need to adjust the parameters to meet the requirements of common and differential mode voltage gain.

III. METHODOLOGY:

3.1. Specifications and Background:

The given design requirements are as follows:

- $A_{CL}(s) = 2$ (in-band gain for the closed-loop system)
- ω_{-3dB} (upper bandwidth limit for the closed-loop system)

  $= 2\pi * 15 * 106$ rad/s

- Slew Rate = 30 V/µs
- PM > 70°
- CL = 2 pF (load of the closed-loop system)
- C1 =C2 = 2 pF

The implementation of a CMOS OPAMP that combines a considerable dc gain with a high unity gain frequency is a challenge. The approach to this design has been by hand calculating and evaluating the deduced equations from the behavioral characteristics of NMOS and PMOS transistors followed by simulations using Cadence.

As per the given constraints for the circuit to be designed, it is supposed to be designed for a feedback factor $\beta = C1/(C1+C2) = 1/2$. To achieve a closed-loop gain of $A_{CL} = 2$ with the given β factor the circuit is supposed to have a very high open-loop gain of the order of approximately $10^2 \sim 10^6$ or higher.

High gain being a major requirement of the system a two-stage Operational Transconductance Amplifier (OTA) topology, which offers many advantages over its counterparts, has been chosen for the design.

For a closed-loop system, the upper bandwidth limit is multiplied by the feedback factor, i.e.,

Unity Gain Bandwidth Product (GBW) = feedback factor (β) * ω_{-3dB} (given)

Hence, **GBW = 2*2*pi*15*10^6** .

To meet the requirements of Phase Margin (PM) and stability for the circuit, the concept of Pole splitting was incorporated in the design using a compensation capacitor C_C between the first and second stages of the amplifier.

Process parameters like μC_{ox}, V_{th}, Input common-mode ranges (ICMR min and max) for both NMOS and PMOS transistors were determined by pre-design simulations.

3.2. Existing Optimized Solutions:

To design a two-stage operational amplifier various approaches are available which can be studied or chosen based on the requirements/constraints of the application. A few of the following methods that caught our attention can be used to optimize the design after following the standard hand calculation approach:

A. Nulling Resistor Approach:

A two-stage OTA has a Right-Hand Plane (RHP) zero in its transfer function which harms the Phase Margin and thus the stability of the system. Adding a resistance R_c in series with the compensation capacitor C_c can help improve the Phase Margin of the design. The value of R_c is usually decided by the transconductance of the input transistor of the second stage $gm_{in,2}$.

- For a value $R_C = 1/gm_{in,2}$ removes the RHP zero effectively.
- For $R_c > 1/gm_{in,2}$ pushes the RHP zero to a higher frequency.
- R_c can also be tuned to cancel the non-dominant pole of the system and thus stabilize it.

An optimized approach considering the different design trade-offs of Nulling resistor can result in an improved Gain Bandwidth Product (GBW).

B. Voltage Buffer Approach:

In this approach, a Common Drain stage along with the compensation capacitor C_c is usually employed to break the forward path. The output of the first stage is given as input to the source of this stage via C_c and the output of the whole system is taken from the gate of this stage. This buffer stage introduces a Left half-plane Zero which can be tuned to compensate with the 2^{nd} pole of the system. This approach works similar to the Nulling resistor approach; however, it greatly reduces the output swing barring its use in many applications.

C. Current Buffer Approach:

This method employs a common gate stage, receiving the output of the first stage at its drain as the input and gives out the output via C_C. at source. In this case, the open-loop gain is characterized by a dominant pole, a zero, and two complex conjugate poles which on tuning and considering the necessary tradeoffs help to optimize the GBW. Unlike the voltage buffer approach, it preserves the output swing.

3.3. Justifications for Designed Architecture:

A. Choice of Topology:

Performing standard hand calculations and simulations over a single-stage amplifier, gave us an insight into the fact that maintaining a good swing and achieving high gain at the same time using a single-stage is not easy. Thus the design of a two-stage amplifier was decided upon to meet the gain and swing requirements.

The telescopic topology has a limited output swing. It cannot be used as a unity gain buffer, i.e., we cannot short the output to the input as it may drive one of the cascade transistors into the triode region due to the limited V_{in} range. Also, the analysis of a telescopic topology suggests that it has a medium gain.

As far a unity gain buffer and output swing limitations go, a Folded Cascode can be used more effectively instead of the telescopic topology. But Folded cascode consumes higher power due to additional current sources needed for biasing of the transistors. Also, we only achieve a slightly higher gain as compared to telescopic topology but at the cost of more power consumption.

An Operational Transconductance Amplifier (OTA), has higher gain and better output swing as compared to its counterparts, viz, Telescopic and Folded Cascode topology. Also, it can be used as a unity gain amplifier. Thus a two Stage OTA topology was selected for this design.

B. Schematic:

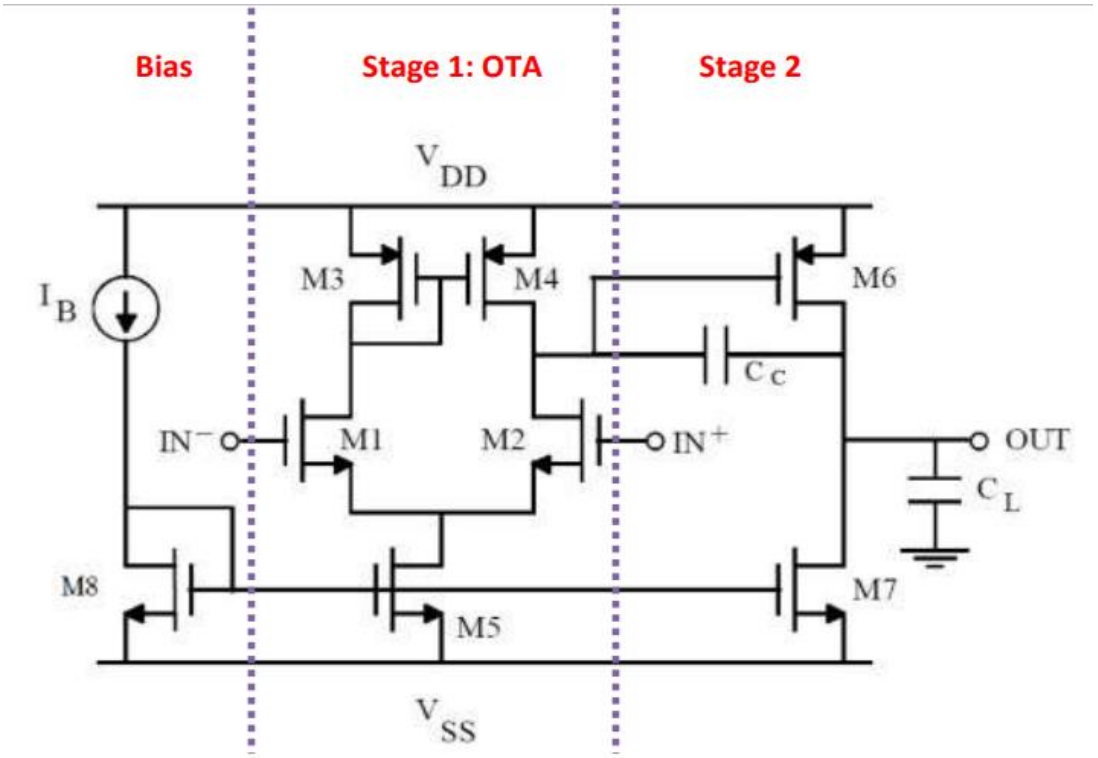


Fig.7: Schematic

- M1-M2 => Input MOS (Stage 1)
- M3-M4 => mirrors output of M1 to the output of M1 to make the circuit have a single-ended differential output
- M5 => MOS used as a current source for biasing of M1-M2
- M6-M7 => CS Amplifier (Stage 2)
- M8 and IB => Provide bias for the current source loads M5 and M7
  - Stage 1 is a differential amplifier with single-ended output. For Stage2 we use a PMOS (M6) for higher swing and M7 is the current source load for M6.
  - C_C is the compensation capacitor for effective pole splitting. It is feedback from output to input in the second stage.

C. Small-Signal Model:

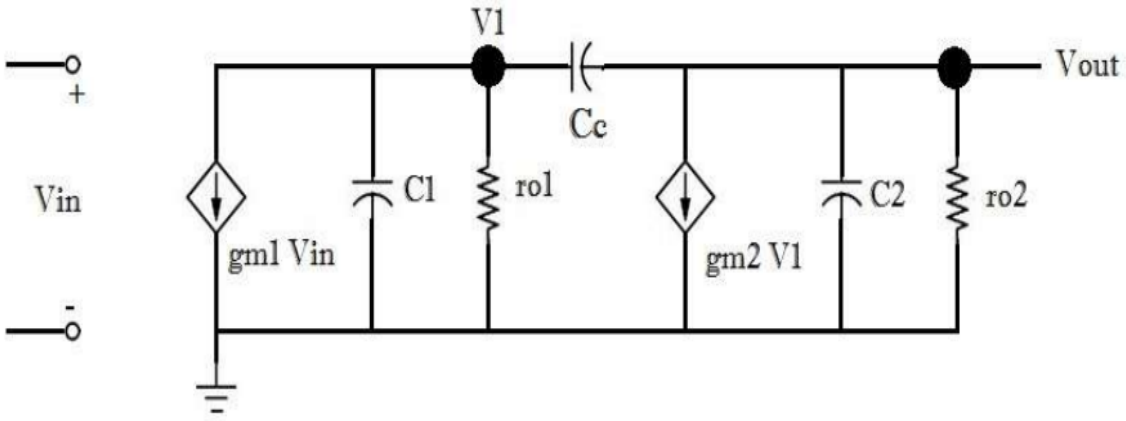


Fig.8: Small-signal model for Two-stage OTA

[Stage 1 parameters are denoted by subscript 1, Stage2 parameters are denoted by subscript 2]

- C1 represents parasitic capacitances by C_{GS}, C_{DS4}, and C_{DS2}. C2 is dominated by load capacitance C_L and hence other parasitic capacitances around C2 can be ignored. 'ro1' and 'ro2' are represented here as output resistances of Stage 1 and Stage 2 respectively.
- With each stage, we introduce a pole in the system. Thus our circuit is a 2 pole system.

3.4. Design Approach:

Analysis of the circuit:

Considering the Small-signal model in **Fig 8**,

The general equation for a 2 pole system is given as:

$$\frac{V_0}{V_{in}} = \frac{A_{DC}\,(1 - s/z)}{(1 + s/p_1)(1 + s/p_2)} = \frac{A_{DC}\,(1 - s/z)}{1 + s(1/p_1 + 1/p_2) + s^2(1/p_1\,p_2)}$$

Considering P_1 to be the dominant pole,

$$\boldsymbol{P_1 = \frac{1}{R_2(C_2+C_c)+R_1(C_1+C_c)+gm_2R_2R_1C_c} \approx \frac{1}{gm_2R_2R_1C_c}}$$

$$\boldsymbol{P_1P_2 = \frac{1}{R_1R_2(C_1+C_2+C_c)}}$$

$$\boldsymbol{\therefore P_2 = \frac{gm_2}{C_2}}$$

$$z = \frac{gm_2}{C_c} \qquad \therefore A_{DC} = gm_1R_1gm_2R_2 \qquad GBW = A_{DC} \times P_1 = \frac{gm_1}{C_c} \qquad SR = I_5/C_c$$

$$\angle V_o/V_{in} = -\tan^{-1}(\omega/z) - \tan^{-1}(\omega/P_1) - \tan^{-1}(\omega/P_2)$$

Considering $\omega = GBW$ and minimum value of $z \geq 10 \times GBW$

$$\angle V_o/V_{in} = -\tan^{-1}(1/10) - \tan^{-1}(A_{DC}) - \tan^{-1}(GBW/P_2)$$

Now, for a single pole system, the value of $\tan^{-1}(A_{DC})$ nearly equal to $90°$ and

$$\angle V_o/V_{in} = -180 + PM$$

Thus for a PM of around 80° and making a design assumption of $gm_2 \sim 10 * gm_1$

We get,

- **C_C = 3pF**
- **I_B = Slew Rate (SR) * C_C = 90 µA**

Manipulating above given equations and values along with

- $\mathbf{I_D = \mu C_{ox} * W * (V_{gs} - V_{th})^2 / 2 * L}$
- $\mathbf{gm = 2 * I_D / (V_{gs} - V_{th})}$

We deduce aspect ratios for our transistors.

The value of V_{DD} was chosen to be 3V since we expected and derived high aspect ratios and I_B for our transistors.

Pre-Design Test 1:

Diode-connected NMOS and PMOS are supplied with 50 µA of current and then µnCox and µpCox are calculated using Cadence.

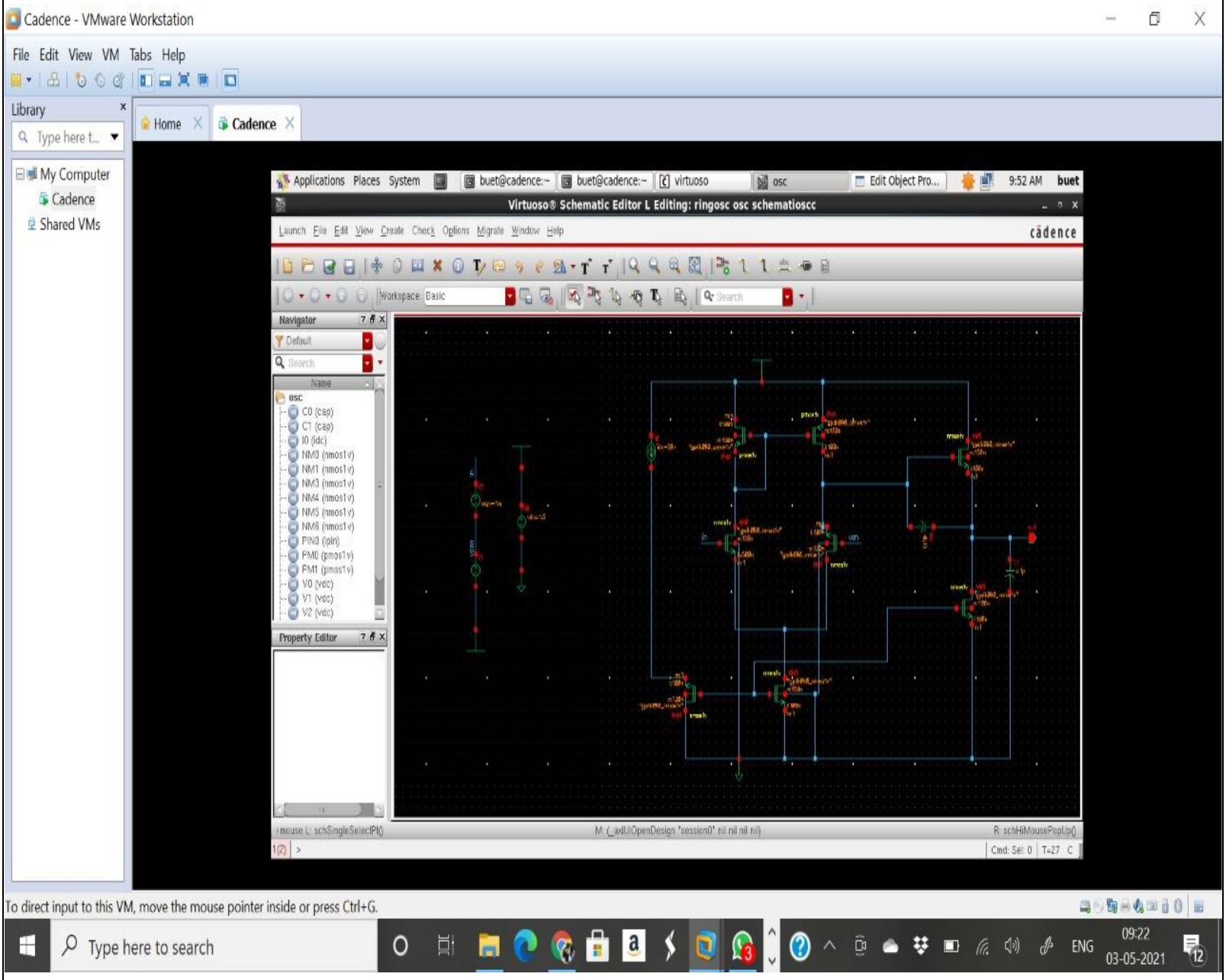
Pre-Design Test 2:

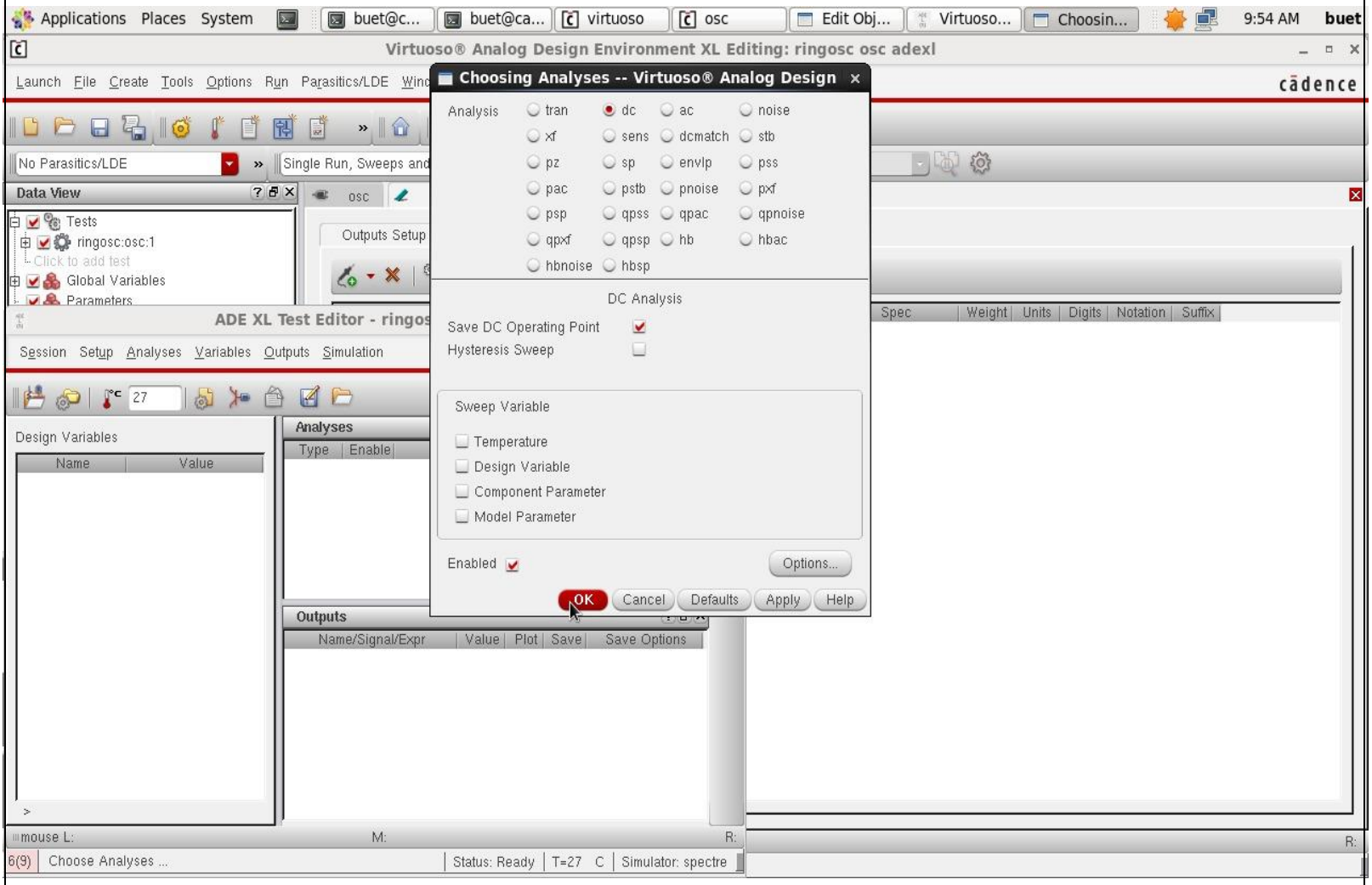
To determine Input common-mode range (ICMR), the test bench for the two-stage amplifier is constructed on cadence, and with a common-mode input given to both the input terminals, the region for which all transistors work as per requirement is found out.

Design Tests:

Iterate for (W/L) ratios for various transistors by observing the circuit's behavior over a range of frequencies.

IV. SIMULATIONS:

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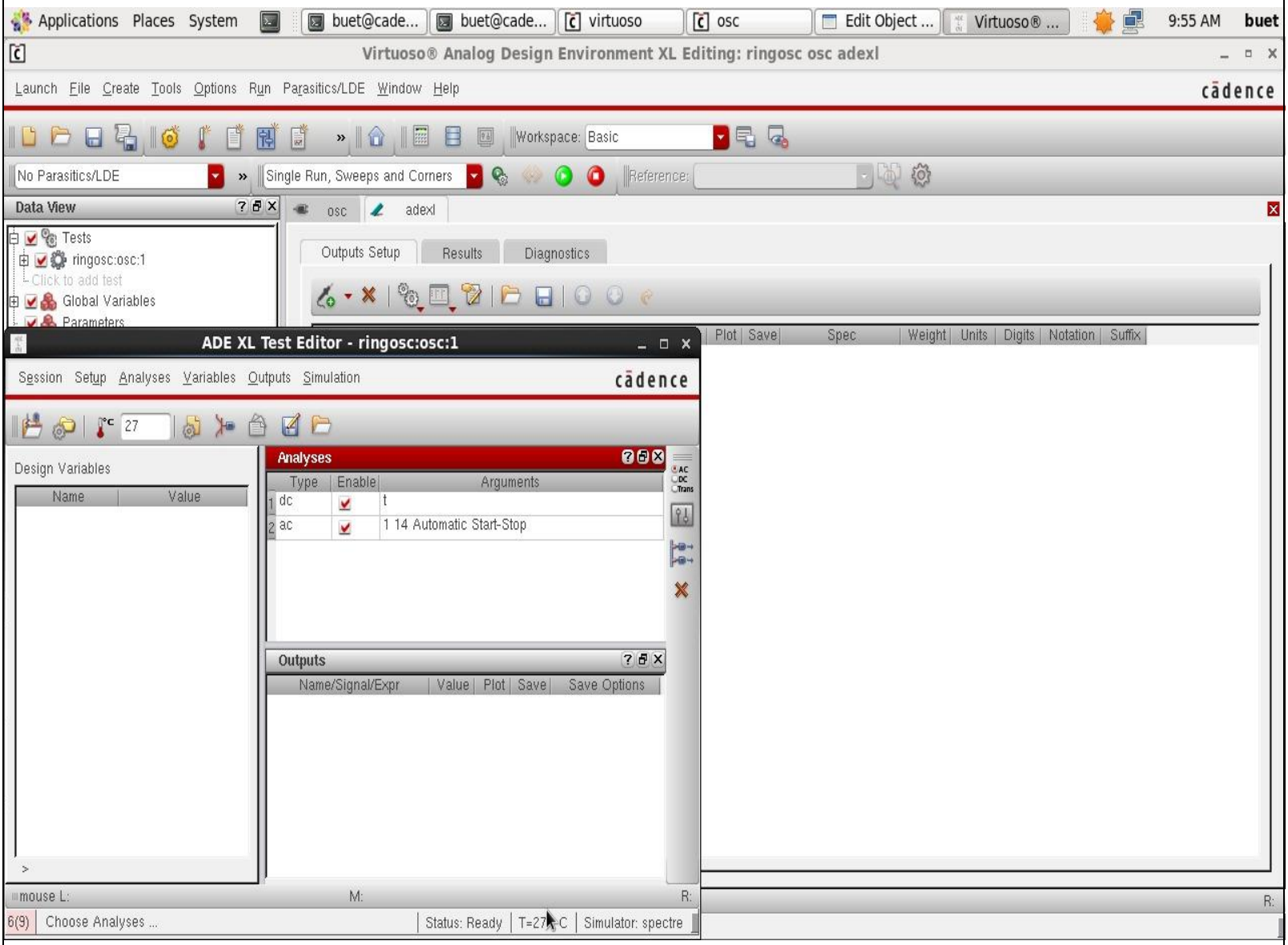
Save DC Operating Point
Hysteresis Sweep
Sweep Variable
Temperature
Design Variable
Component Parameter
Model Parameter
Enabled
Options...
OK
Cancel
Defaults
Apply
Help
No Parasitics/LDE
Single Run, Sweeps and
Data View
Tests
ringosc:osc:1
Click to add test
Global Variables
Parameters
Outputs Setup
ADE XL Test Editor - ringos
Session Setup Analyses Variables Outputs Simulation
Design Variables
Name
Value
Analyses
Type
Enable
Outputs
Name/Signal/Expr
Value
Plot
Save
Save Options
Spec
Weight
Units
Digits
Notation
Suffix
mouse L:
M:
R:
6(9)
Choose Analyses ...
Status: Ready
T=27 C
Simulator: spectre


Applications Places System
buet@cade...
buet@cade...
virtuoso
osc
Edit Object ...
Virtuoso® ...
9:55 AM
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Virtuoso® Analog Design Environment XL Editing: ringosc osc adexl
Launch File Create Tools Options Run Parasitics/LDE Window Help
cadence
Workspace: Basic
No Parasitics/LDE
Single Run, Sweeps and Corners
Reference:
Data View
Tests
ringosc:osc:1
Click to add test
Global Variables
Parameters
osc
adexl
Outputs Setup
Results
Diagnostics
Plot
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Notation
Suffix
ADE XL Test Editor - ringosc:osc:1
Session Setup Analyses Variables Outputs Simulation
cadence
27
Design Variables
Name
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1 dc
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Plot
Save
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R:
6(9)
Choose Analyses ...
Status: Ready
T=27°C
Simulator: spectre

V. CONCLUSION

An overview of a general approach to design a two-stage Operational Transconductance Amplifier has been described in this report. The procedure presented follows a pencil-and-paper method wherein the general equations obtained from behavioral characteristics of CMOS transistors are used to determine various design parameters of the transistor, to meet the prescribed system constraints. Necessary simulations and schematic diagrams implemented in Cadence have been added to the report. As for the future scope of the project, optimized designs for lower power dissipation and higher gain-bandwidth product can be obtained with fine-tuning of the trade-offs involved in the design.

VI. REFERENCES

1. Palmisano, G. and Palumbo, G., "A compensation strategy for two-stage CMOS opamps based on the current buffer." IEEE Trans. on Circuits and Systems (part I) 44(3), pp. 257–262, March 1997
2. G. Palmisano, G. Palumbo, and S. Pennisi, "Design Procedure for Two-Stage CMOS Transconductance Operational Amplifiers: A Tutorial", Analog Integrated Circuits and Signal Processing, 27, 179–189, 2001.
3. Anchal Verma, Deepak Sharma, Rajesh K. Singh, and Mukul K. Yadav, "Design of Two-Stage CMOS Operational Amplifier", IJETAE, vol 3, issue 12, December 2013.
4. T. H. Kim, "6.012 DP: CMOS Integrated Differential Amplifier," p. 9.
5. R. Sotner, J. Jerabek, R. Prokop, V. Kledrowetz, and J. Polak, "A CMOS Multiplied Input Differential Difference Amplifier: A New Active Device and Its Applications," Applied Sciences, vol. 7, no. 1, p. 106, Jan. 2017, DOI: 10.3390/app7010106.
6. R. A. El-mon's and A. W. Abdallah, "CMOS Two-Stage Amplifier Design Approach," p. 5.