EEZ DIB specification

Current version	*v1.2*
Status	*Active*
File repository	*https://github.com/eez-open/modular-psu/tree/master/DIB*
License	*TAPR v1.0*
Contributions	*C4.1 (Collective Code Construction Contract)*
Revision history	*2020-12-27:* ***v1.2*** • *ADIB pass thru connector added* *2020-06-12:* ***v1.1*** • *Two additional device select lines (SPI2_CSC and SPI3_CSC)*

The DIB (short for *DIY Instrument Bus*) is conceived to enable creation of *modular* T&M instruments that with their capabilities and complexity bridge the gap between DIY/hobbyist and professional solutions. Creation of this first DIB specification is an attempt to provide more flexibility and processing power for projects such as EEZ H24005 programmable power supply in a way to offer more freedom to select main processing resources (MCU, SoC, SBC), deploy various peripheral modules and offers “plug-and-play” functionalities in the best possible way.
This specification defines four physical connectors: two mandatory (MCU 40-pin and Peripheral module 28-pin) that are related to DIB backplane and two optional, one (16-pin) that defines power connection when the EEZ DIB AUX Power supply is used for powering MCU and backplane, and another (20-pin) that allows coupling of power sourcing module output terminals such as DCP405 power module.
Connector's pin mappings are shown on Fig. 1. All connectors contain two rows hence pin mappings description is separated in two columns (*A* and *B)*. Direction (*Dir* column) when applicable shows unidirectional signal flow referenced from the inserted module, not backplane.

For example, NRESET on the MCU module connector is assigned as an output (*O*). Therefore the same signal represents an input (*I*) on the peripheral module connector. Bidirectional signals have the same direction mark (*I/O*) on both sides (MCU and peripheral module).

MCU module connectivity

A 40-pin (2 x 20-pin) right angled pin header and receptacle with 0.1” pitch are used for making connection between MCU board and DIB backplane. Receptacle is used on the MCU board side while header is on the backplane side. The MCU module provides the following power and signaling lines:

- +5 V pass-thru power output (from the e.g. AUX Power Supply)
- +12 V pass-thru power output (from the e.g. AUX Power Supply)
- +3.3 V low power output (provided from the MCU board LDO, max. 20 mA per module)
- +3.3 V backup, low power battery backup output
- Reset output (active low) and Fault open-collector signal
- I2C bus (SSCL and SSDA, 3.3 V level) shared between all peripheral modules and AUX Power Supply
- Async UART (RX and TX, 3.3 V level) shared between all peripheral modules that can be used for firmware uploading of the peripheral modules' on-board MCU if it does not support SPI for such operation
- Three dedicated SPI buses (SCLK, MISO and MOSI for modules on slot #1, #2, and #3)
- Multiple device select lines (CSA and CSB for modules on slot #1, #2, and #3) that allows addressing of up to four SPI devices on the peripheral module (using 2-to-4 line decoder like SN74LVC1G139)
- Dedicated peripheral module interrupt (IRQ for module #1, #2, and #3)
- SYNC output for synchronizing activities between two or more peripherals, e.g. OE (Output Enable) of power sourcing peripheral modules.

MCU module (2 x 20-pin) — *Status: Mandatory*

	A	Dir			B	Dir	
1	GND			2	GND		
3	UART_RX	I	Shared UART RX	4	UART_TX	O	Shared UART TX
5	+VAUX	I/O	Backup DC power	6	NRESET	O	Master reset (active low)
7	+3V3	O	DC power	8	NFAULT	I	Fault (active low)
9	SPI3_IRQ	I	#3 IRQ	10	SYNC	O	Sync output
11	SPI3_CSA	O	#3 Chip select A	12	SSCL	O	Shared I²C SCL
13	SPI3_CSB	O	#3 Chip select B (#5 IRQ)	14	SSDA	I/O	Shared I²C SDA
15	GND			16	GND		
17	SPI3_SCLK	O	#3 SPI CLK	18	SPI3_MISO	I	#3 MISO
19	SPI2_IRQ	I	#2 IRQ	20	SPI3_MOSI	O	#3 MOSI
21	SPI2_CSB	O	#2 Chip select B (#4 IRQ)	22	SPI2_CSA	O	#2 Chip select A
23	SPI2_SCLK	O	#2 SPI CLK	24	SPI2_MISO	I	#2 MISO
25	SPI1_IRQ	I	#1 IRQ	26	SPI2_MOSI	O	#2 MOSI
27	SPI1_CSB	O	#1 Chip select B	28	SPI1_CSA	O	#1 Chip select A
29	GND			30	SPI2_CSC	O	#2 Chip select C
31	SPI1_MISO	I	#1 MISO	32	SPI1_SCLK	O	#1 SPI CLK
33	SPI1_MOSI	O	#1 MOSI	34	SPI3_CSC	O	#3 Chip select C
35	+5V	I	DC power	36	+5V	I	DC power
37	+12V	I	DC power	38	+12V	I	DC power
39	GND			40	GND		

Peripheral modules (2 x 14-pin) — *Status: Mandatory*

	A	Dir			B	Dir	
1	+3V3	I	DC power	2	+VAUX	I	Backup DC power
3	NFAULT	I/O	Fault (active low)	4	NRESET	I	Module reset (active low)
5	SSCL	I	Shared I²C SCL	6	SYNC	I	Sync input
7	GND			8	SSDA	I/O	Shared I²C SDA
9	CSA	I	Module Chip select A	10	IRQ	O	Module IRQ
11	GND			12	CSB	I	Module Chip select B
13	SCLK	I	Module SPI CLK	14	MISO	O	Module MISO
15	MOSI	I	Module MOSI	16	GND		
17	A0	I	I²C Address 0	18	A2	I	I²C Address 2
19	A1	I	I²C Address 1	20	GND		
21	+12V	I	DC power	22	+12V	I	DC power
23	+5V	I	DC power	24	+5V	I	DC power
25	GND			26	BOOT	I	Module bootloader select
							*Status: Optional**
27	UART_RX**	O	Shared UART RX	28	UART_TX**	I	Shared UART TX

AUX PS module (2 x 8-pin) — *Status: Recommended*

	A	Dir			B	Dir	
1	PE			2	N.C.	O	N.C.
3	+12V	O	DC power	4	+12V	O	DC power
5	+5V	O	DC power	6	+5V	O	DC power
7	GND			8	GND		
9	GND			10	+VAUX	I/O	Backup DC power
11	PWR_SSTART	I	AC soft-start	12	PWR_DIRECT	I	AC power on
13	SSCL	I	Shared I²C SCL	14	SSDA	I/O	Shared I²C SDA
15	NFAULT	I/O	Fault (active low)	16	+3V3	I	DC power

Power source module (2 x 10-pin) — *Status: Optional*

	A	Dir			B	Dir	
1	IN+	I	Power positive input	2	IN+	I	Power positive input
3	IN+	I	Power positive input	4	IN+	I	Power positive input
5	IN+	I	Power positive input	6	OUT+	O	Power positive output
7	OUT+	O	Power positive output	8	OUT+	O	Power positive output
9	OUT+	O	Power positive output	10	OUT+	O	Power positive output
11	OUT-	O	Power negative output	12	OUT-	O	Power negative output
13	OUT-	O	Power negative output	14	OUT-	O	Power negative output
15	OUT-	O	Power negative output	16	IN-	I	Power negative input
17	IN-	I	Power negative input	18	IN-	I	Power negative input
19	IN-	I	Power negative input	20	IN-	I	Power negative input

*) The first 26-pin of peripheral module connector is mandatory and last two pin are optional. New versions of DIB specification could introduce even more features but that will require also introduction of larger MCU connector or additional connector for the MCU

**) Connect module UART_RX to master MCU UART_TX and module UART_TX to master MCU UART_RX

Fig. 1: DIB v1.2 pin mappings

Although only three SPI buses are defined with DIB v1.2, that doesn't limit max. number of peripheral modules to three. The DIB backplane can be designed in a way that two or more peripheral module connectors share the same SPI bus. Two additional device select lines (SPI2_CSC and SPI3_CSC) can be used for such purposes. If module require dedicated IRQ line, then SPI2_CSB and SPI3_CSB can be used as alternative IRQ line (there should be a possibility of IRQ line selection on the module in that case).

Peripheral modules connectivity

Power and signaling lines for the peripheral modules are provided with 28-pin (2 x 14-pin) 0.1” pitch right angled pin header on the side of the peripheral module and receptacle on the backplane side. The peripheral module connection includes the following power and signal lines:

- +5 V input (from the AUX Power Supply)
- +12 V input (from the AUX Power Supply)
- +3.3 V low power input (provided from the MCU board LDO, max. 20 mA per module)
- +3.3 V backup , low power battery backup input for e.g. standby
- Reset input (active low) and Fault open-collector signals
- I2C bus (SSCL and SSDA) shared between all peripheral modules and AUX Power Supply
- SPI bus (SCLK, MISO and MOSI) and two device select lines (CSA and CSB)
- Interrupt output (IRQ)
- SYNC input for synchronizing activities between two or more peripherals initiated by MCU
- Module identification inputs (A0, A1, A2)
- BOOT input
- Shared async UART (optional)

The BOOT input can be used with peripheral modules that comes with on-board MCU and which firmware could be uploaded via SPI or UART. If BOOT input has to be dedicated (i.e. one per module) that only one on-board MCU can be put into bootloader mode after the reset (power up) a DIB backplane can be equipped with I2C I/O expander that could provide one BOOT control signal per module.

The module identification inputs can be used as device selection for I2C peripherals such as on-board EEPROM, temperature sensors, etc. When used for EEPROM addressing the 000 address cannot be used since it's assigned to the I2C EEPROM on the MCU board. Inputs A0-A2 require pull-up resistors connected to +3.3 V (e.g. 10 to 47 KΩ) on the peripheral module PCB. Module position on the backplane is defined by “hardcoded” wiring of A0-A2 to GND in the following manner:

Module position	A0	A1	A2
#0 (reserved)	*GND*	*GND*	*GND*
#1	*Open*	*GND*	*GND*
#2	*GND*	*Open*	*GND*
#3	*Open*	*Open*	*GND*
#4	*GND*	*GND*	*Open*
#5	*Open*	*GND*	*Open*
#6	*GND*	*Open*	*Open*
#7	*Open*	*Open*	*Open*

Please note that #0 position should not be used to avoid possible conflict with already mentioned EEPROM on the MCU board and also other devices in the future.

When selecting I2C EEPROM pay close attention on its addressing capabilities even if it provides three address inputs. Many low capacity devices can effectively use only a single input for addressing purposes.

If two or more modules have to be galvanically isolated (e.g. like in case of power modules with floating outputs) use appropriate isolators (e.g. Silabs Si86xx, Maxim MAX14850) for control and data lines.

AUX PS module connectivity

The main purpose of this connection is power delivery for MCU board and peripheral modules. Two voltages are specified with DIB v1.2: +5 V and +12 V. Additionally, two lines are assigned to +3.3 V auxiliary powers: a) +VAUX as (battery) backup and b) +3.3 V that is sourced from the MCU board LDO and can be used to power e.g. an I2C low-power (max. 20 mA) device like fan controller. This connection contains also the following functions:

- Shared I2C bus (SSCL, SSDA) for fan controller or similar devices
- AC Soft-start/Standby control inputs (PWR_SSTART, PWR_DIRECT)
- Reset input (active low) and Fault open-collector signal
- PE (Protective Earth) output
- MBOOT output for define MCU bootloader mode

Power sourcing module connectivity

This connection is optional, but its physical location should be taken into account when peripheral module PCB is designed to leave that area unpopulated to avoid possible issues with inserting peripheral module into the DIB backplane that includes this connectivity (e.g. EEZ DIB BP3C backplane). Therefore it is highly recommended to follow the peripheral module PCB template available on the project's GitHub repository.
A 20-pin (2 x 10-pin) 0.1” pitch right angled receptacle is used on the side of peripheral module and straight pin header on the DIB backplane side. Pinout scheme is rather simple: it provides power terminal inputs and outputs that are assigned on multiple pins for increased current capacity. Allocation of five pins per power lines should be sufficient to carry 5 A continuously.
The idea behind output terminal coupling is to avoid usage of external wiring as it is accomplished on the EEZ H24005's Arduino Shield board by using power relays for reliable connection under MCU control.
If peripheral module such as DCP405 power module is deployed, this connectivity becomes mandatory on the DIB backplane. If no coupling capabilities are provided, a simple pass-thru connection (i.e. IN+ to OUT+ and IN- to OUT-) has to be made to ensure normal operation of such module.

ADIB connectors

An ADIB (*Analog DIB*) connector has been introduced to simplify the wiring of modules working with analog signals. In this way wiring can be done internally and some functions will be able to be performed under firmware control. Up to two ADIB connectors are available in 10-pin IDC 2.0 mm format for greater connection flexibility.

ADIB (2 x 5-pin) *Status: Optional*

	A	Dir			B	Dir	
1	Guard-	I	AIN- guard	2	Guard+	I	Power positive input
3	AIN-	O	Analog input-	4	AIN+	O	Analog Input+
5	Guard-	I	AIN- guard	6	Guard+	I	Power positive output
7	ID0	O	ADIB module ID0	8	ID2	O	ADIB module ID2
9	ID1	O	ADIB module ID1	10	ID_Gnd	I	Master ADIB Gnd

Fig. 2: ADIB connector pinout

The pinout is shown in fig. 2. Each connector has two pins for analog signal AIN + and AIN- which have Guard signals on each side. The remaining 4 pins are used to identify the ADIB capable module: three for the ADIB address and a fourth for the Gnd of the ADIB "master" (e.g. MIO168 module) whose Gnd is not necessarily at the same potential as the Gnd of the module to which it will be connected by an ADIB cable. To detect the ADIB ID address, the "master" module should have a pull-up set at the inputs.

The table below shows the ADIB ID used so far.

ADIB ID	Module name	Description
#1	*SMX46*	*Switch matrix module*
#2	*MUX14D*	*2-wire dual 7:1 (14:1) Multiplexer*
#3	*N/A*	

#4	N/A
#5	N/A
#6	N/A
#7	N/A
#8	N/A

Peripheral module PCB dimensions

The DIB v1.2 specifies only the physical dimensions of the peripheral module and positions of related mandatory and optional connectors (i.e. 28-pin peripheral module connector, 20-pin power sourcing module and up to two 10-pin ADIB connectors). Dimensions of other parts of the system (e.g. MCU board, backplane, power supply module) can differ from project to project depending of e.g. chosen enclosure dictated by builder budget and appearance preferences. Allowed dimension of the peripheral module is shown on Fig. 3.

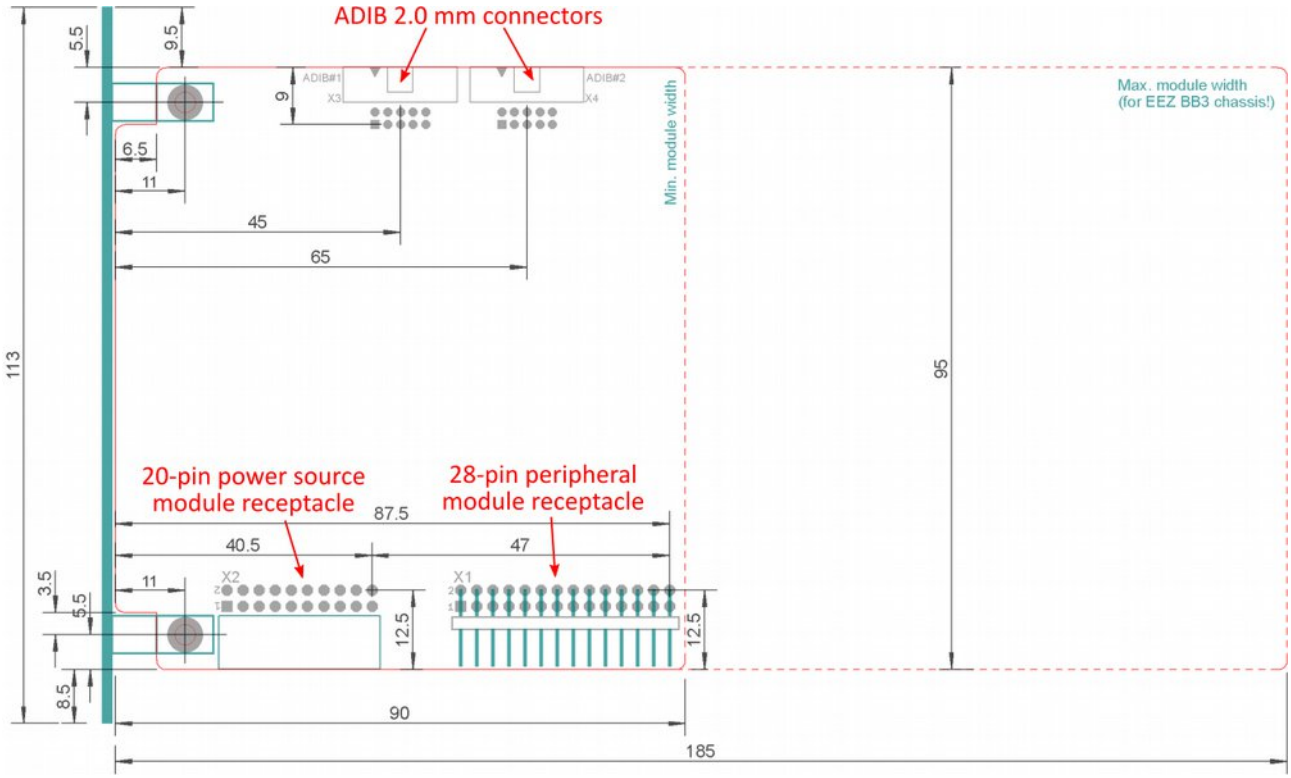

Fig. 3: DIB v1.2 peripheral module dimensions

Thanks to the fact that DIB connectors are located at the bottom end, the PCB width can vary and it could be anything from 90 to 185 mm. In fact it could be even wider, but this is recommended if the EEZ Bench Box 3 design is used. Recommended PCB height is 95 mm but it can also vary in accordance with selected enclosure, and that is a max. height for the EEZ Bench Box 3 design.
Distance (horizontal pitch) between two peripheral module connectors is 35.5 mm (7 HP) and could appear that is somewhat too large for today's standards and components. Such distance is selected to allow mounting of larger heatsink elements on the peripheral module that is beneficial for power sourcing and sinking modules where increased power dissipation is expected. Still, the specified modules distance does not limit builder to design a backplane that combine few DIB v1.0 modules (i.e. 7 HP wide to “comply” with specification) with thinner modules (e.g. 5 HP).

Note that even if peripheral module does not require 20-pin power sourcing module receptacle, related PCB area has to remain unpopulated to avoid issue with inserting peripheral module into DIB backplane which has that connector.

Peripheral module front panel is shown on Fig. 4. It contains two pairs of holes for fixing it on the peripheral module PCB and to the DIB enclosure front panel.

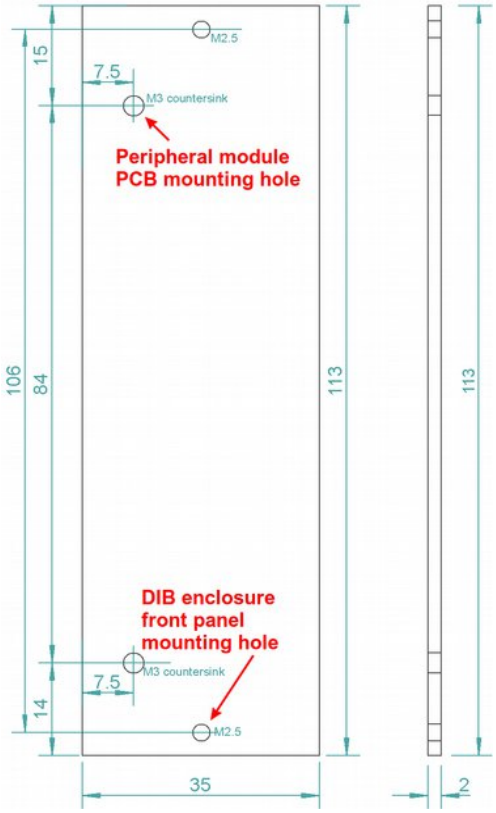

Fig. 4: DIB v1.2 Peripheral module front panel dimension

DIB 3-slot backplane example

The DIB backplane shown on Fig. 5. is an example of possible DIB v1.2 backplane design. Its design is used for making the BP3C backplane for the EEZ Bench Box 3. It provides connectivity to up to three peripheral modules which can also be a power sourcing modules. Therefore both 28-pin peripheral module connector and 20-pin power sourcing module connector are included for each slot.

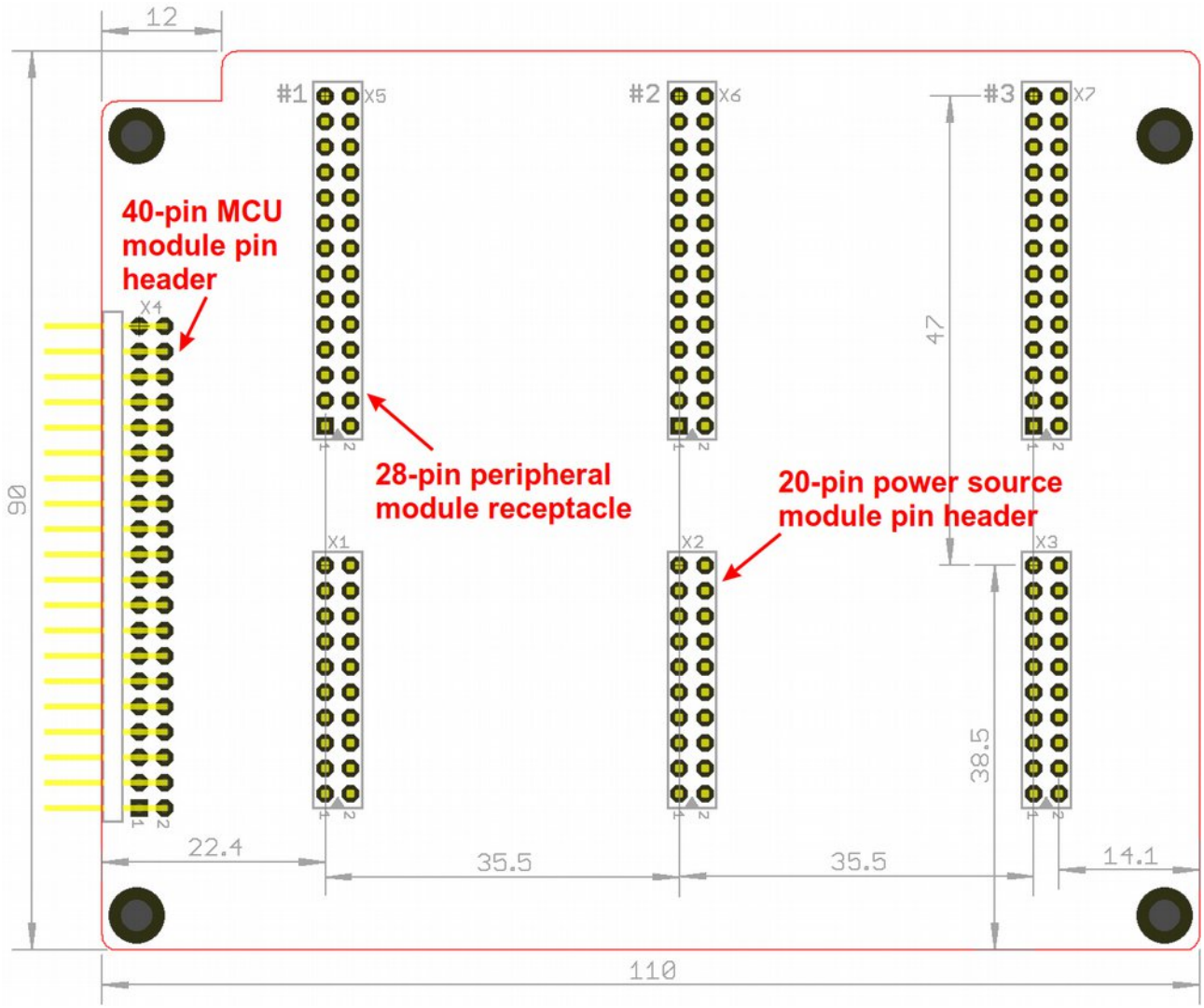

Fig. 5: DIB 3-slot backplane example

Peripheral modules are inserted in this backplane vertically, and this is a mandatory, while MCU board is connected horizontally which is not a mandatory orientation. If a backplane is designed to accept MCU board vertically, and positioned on the far right of the backplane, the same horizontal pitch (7 HP) has to be used for MCU 40-pin connector as for the peripheral module connectors.
It is recommended that PCB with min. two layers is used and filled with huge GND planes.