Power connector (2 x 11-pin) *Usage: Optional*

	A	Dir			B	Dir	
1	IN+	I	Power positive input	2	IN+	I	Power positive input
3	IN+	I	Power positive input	4	IN+	I	Power positive input
5	IN+	I	Power positive input	6	OUT+	O	Power positive output
7	OUT+	O	Power positive output	8	OUT+	O	Power positive output
9	OUT+	O	Power positive output	10	OUT+	O	Power positive output
11	OUT-	O	Power negative output	12	OUT-	O	Power negative output
13	OUT-	O	Power negative output	14	OUT-	O	Power negative output
15	IN-	I	Power negative input	16	IN-	I	Power negative input
17	IN-	I	Power negative input	18	IN-	I	Power negative input
19	SENSE-	I	Sense negative input	20	SENSE+	I	Sense negative input

Used on slots #1, #2 and #4 only

Examples of backplane connector models: PH2-20-UA, Examples of backplane connector models: PH2-20-UA, 77313-124-22LF, ZL202-20G, 10129381-922002BLF, ZL202-20G

Signal connector *Usage: Mandatory*

	A	Dir	Description		B	Dir	Description
1	+12V	I	DC power	1	+12V	I	DC power
2	+12V	I	DC power	2	+12V	I	DC power
3	+12V	I	DC power	3	GND		
4	GND			4	+3V3	I	DC power
5	+5V	I	DC power	5	+3V3	I	DC power
6	+5V	I	DC power	6	+VAUX	I	Backup DC power
7	GND			7	GND		
8	PE	I	Protective Earth	8	NRESET	I	Module reset (active low)
9	SMBUS_ALERT	O	Shared SMbus alert (active low)	9	NFAULT	I/O OD	Fault (open drain)
10	SCL/SMBCLK	I	Shared I^2C/SMbus Clock	10	SDA/SMBDAT	I/O	Shared I^2C/SMbus Data
11	GND			11	GND		
12	GND			12	GND		
13	QSPI_CLK	I	Shared Quad SPI CLK	13	OE_SYNC	I/O OD	Shared Sync (open drain)
14	QSPI_IO0	I/O	Shared Quad SPI I/O 0	14	AC_FREQ	I	AC Mains frequency
15	QSPI_IO1	I/O	Shared Quad SPI I/O 1	15	A0	I	Module Address 0
16	QSPI_IO2	I/O	Shared Quad SPI I/O 2	16	A1	I	Module Address 1
17	QSPI_IO3	I/O	Shared Quad SPI I/O 3	17	A2	I	Module Address 2
18	QSPI_NCS	I	Shared Quad SPI Bank Select	18	UART_RX*	O	Shared UART RX
19	RSVD1		Reserved	19	UART_TX*	I	Shared UART TX
20	RSVD2		Reserved	20	BOOTn	I	Module bootloader select
21	SCLK	I	Shared SPI CLK	21	GND		
22	MOSI	I	Shared MOSI	22	PCIe_CLK+	I	PCIe clock
23	MISO	O	Shared MISO	23	PCIe_CLK-	I	
24	IRQn	O	Module IRQ	24	GND		
25	CSAn	I	Module Chip select A	25	PCIe_RX-	I	PCIe RX
26	CSBn	I	Module Chip select B	26	PCIe_RX+	I	
27	HSD+	I/O	USB 2.0	27	PCIe_TX-	O	PCIe TX
28	HSD-	I/O		28	PCIe_TX+	O	
29	SSTX+	O	USB 3.0 Tx	29	PCIe_CLKREQ	I	PCIe clock request
30	SSTX-	O		30	PCIe_WAKE	I	PCIe wake
31	SSRX+	I	USB 3.0 Rx	31	GND		
32	SSRX-	I		32	ETH_SYNC	O	IEEE 1588 sync

*) Connect module UART_RX to master MCU UART_TX and module UART_TX to master MCU UART_RX

Examples of backplane connector models (gold plating of 0.25 um or thicker, not „flash”): 10018783-10101TLF, 10018783-11101TLF