

STM32 CubeMX

1. Description

1.1. Project

Project Name	H7R7L8H8
Board Name	custom
Generated with:	STM32CubeMX 6.15.0
Date	10/25/2025

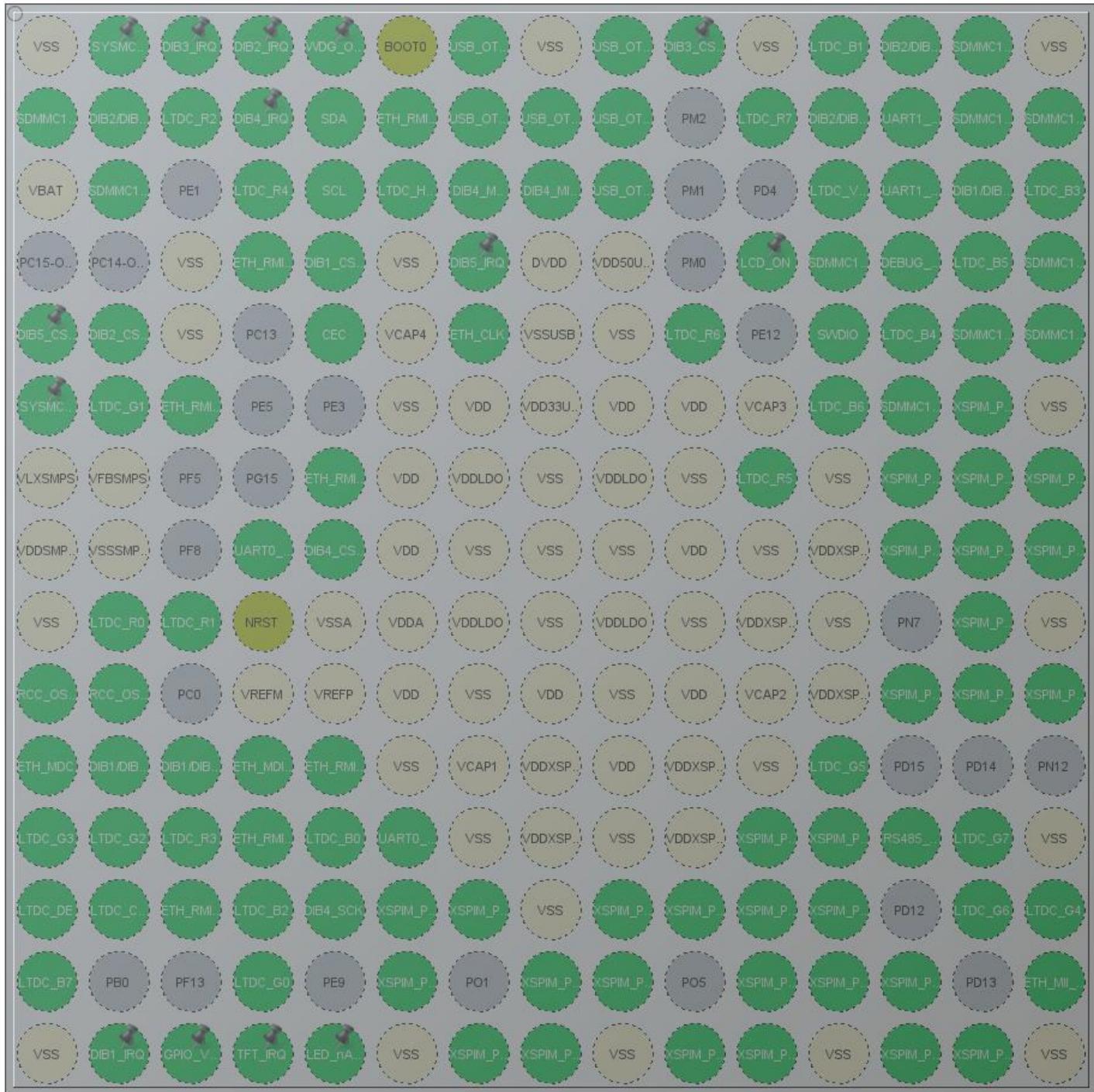
1.2. MCU

MCU Series	STM32H7RS
MCU Line	STM32H7R7/7S7
MCU name	STM32H7R7L8HxH
MCU Package	TFBGA225 HEXA SMPS
MCU Pin number	225

1.3. Core(s) information

Core(s)	ARM Cortex-M7
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2. Pinout Configuration



TFBGA225 HEXA SMPS (Top view)

3. Pins Configuration

Pin Number TFBGA225 HEXA SMPS	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	VSS	Power		
A2	PE0	I/O	GPIO_EXTI0	SYSMCU_IRQ
A3	PF3	I/O	GPIO_EXTI3	DIB3_IRQ
A4	PF2	I/O	GPIO_EXTI2	DIB2_IRQ
A5	PG3 *	I/O	GPIO_Output	WDG_OUT
A6	BOOT0	Boot		
A7	PM12	I/O	USB_OTG_FS_DM	
A8	VSS	Power		
A9	PM6	I/O	USB_OTG_HS_DP	
A10	PM3 *	I/O	GPIO_Output	DIB3_CSA
A11	VSS	Power		
A12	PD3	I/O	LTDC_B1	
A13	PE14	I/O	SPI4_MOSI	DIB2/DIB5_MOSI
A14	PD2	I/O	SDMMC1_CMD	
A15	VSS	Power		
B1	PB8	I/O	SDMMC1_D4	
B2	PE2	I/O	SPI4_SCK	DIB2/DIB5_SCK
B3	PB5	I/O	LTDC_R2	
B4	PF4	I/O	GPIO_EXTI4	DIB4_IRQ
B5	PF0	I/O	I2C2_SDA	SDA
B6	PD7	I/O	ETH_RMII_REF_CLK	
B7	PM11	I/O	USB_OTG_FS_DP	
B8	PM9	I/O	USB_OTG_HS_ID	
B9	PM5	I/O	USB_OTG_HS_DM	
B11	PG0	I/O	LTDC_R7	
B12	PE13	I/O	SPI4_MISO	DIB2/DIB5_MISO
B13	PD1	I/O	UART4_TX	UART1_TX/DOUT1
B14	PC10	I/O	SDMMC1_D2	
B15	PC11	I/O	SDMMC1_D3	
C1	VBAT	Power		
C2	PB9	I/O	SDMMC1_D5	
C4	PB3(JTDO/TRACESWO)	I/O	LTDC_R4	
C5	PF1	I/O	I2C2_SCL	SCL
C6	PG2	I/O	LTDC_HSYNC	
C7	PM13	I/O	SPI5_MOSI	DIB4_MOSI
C8	PM14	I/O	SPI5_MISO	DIB4_MISO

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Pin Number TFBGA225 HEXA SMPS	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
C9	PM8	I/O	USB_OTG_HS_VBUS	
C12	PE11	I/O	LTDC_VSYNC	
C13	PD0	I/O	UART4_RX	UART1_RX/DIN1
C14	PA12	I/O	SPI2_SCK	DIB1/DIB3_SCK
C15	PA11	I/O	LTDC_B3	
D3	VSS	Power		
D4	PB7	I/O	ETH_RMII_TXD1	
D5	PB4(NJTRST)	I/O	SPI2_NSS	DIB1_CSA
D6	VSS	Power		
D7	PD5	I/O	GPIO_EXTI5	DIB5_IRQ
D8	DVDD	Power		
D9	VDD50USB	Power		
D11	PE15 *	I/O	GPIO_Output	LCD_ON
D12	PC12	I/O	SDMMC1_CK	
D13	PA14(JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
D14	PA9	I/O	LTDC_B5	
D15	PC8	I/O	SDMMC1_D0	
E1	PE6 *	I/O	GPIO_Output	DIB5_CSA
E2	PE4	I/O	SPI4_NSS	DIB2_CSA
E3	VSS	Power		
E5	PB6	I/O	CEC	
E6	VCAP4	Power		
E7	PD6	I/O	ETH_CLK	
E8	VSSUSB	Power		
E9	VSS	Power		
E10	PG1	I/O	LTDC_R6	
E12	PA13(JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	SWDIO
E13	PA10	I/O	LTDC_B4	
E14	PC9	I/O	SDMMC1_D1	
E15	PC6	I/O	SDMMC1_D6	
F1	PG14 *	I/O	GPIO_Output	SYSMCU_CS
F2	PG12	I/O	LTDC_G1	
F3	PG11	I/O	ETH_RMII_TX_EN	
F6	VSS	Power		
F7	VDD	Power		
F8	VDD33USB	Power		
F9	VDD	Power		
F10	VDD	Power		
F11	VCAP3	Power		

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Pin Number TFBGA225 HEXA SMPS	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
F12	PA8	I/O	LTDC_B6	
F13	PC7	I/O	SDMMC1_D7	
F14	PN1	I/O	XSPIM_P2_NCS1	
F15	VSS	Power		
G1	VLXSMPS	Power		
G2	VFBSMPS	Power		
G5	PG13	I/O	ETH_RMII_TXD0	
G6	VDD	Power		
G7	VDDLDO	Power		
G8	VSS	Power		
G9	VDDLDO	Power		
G10	VSS	Power		
G11	PA15(JTDI)	I/O	LTDC_R5	
G12	VSS	Power		
G13	PN3	I/O	XSPIM_P2_IO1	
G14	PN0	I/O	XSPIM_P2_DQS0	
G15	PN11	I/O	XSPIM_P2_IO7	
H1	VDDSMPS	Power		
H2	VSSSMPS	Power		
H4	PF7	I/O	UART7_TX	UART0_TX/DOUT3
H5	PF6	I/O	SPI5_NSS	DIB4_CSA
H6	VDD	Power		
H7	VSS	Power		
H8	VSS	Power		
H9	VSS	Power		
H10	VDD	Power		
H11	VSS	Power		
H12	VDDXSPI2	Power		
H13	PN10	I/O	XSPIM_P2_IO6	
H14	PN9	I/O	XSPIM_P2_IO5	
H15	PN2	I/O	XSPIM_P2_IO0	
J1	VSS	Power		
J2	PF9	I/O	LTDC_R0	
J3	PF10	I/O	LTDC_R1	
J4	NRST	Reset		
J5	VSSA	Power		
J6	VDDA	Power		
J7	VDDLDO	Power		
J8	VSS	Power		

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Pin Number TFBGA225 HEXA SMPS	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
J9	VDDLDO	Power		
J10	VSS	Power		
J11	VDDXSPI2	Power		
J12	VSS	Power		
J14	PN6	I/O	XSPIM_P2_CLK	
J15	VSS	Power		
K1	PH0-OSC_IN(PH0)	I/O	RCC_OSC_IN	
K2	PH1-OSC_OUT(PH1)	I/O	RCC_OSC_OUT	
K4	VREFM	Power		
K5	VREFP	Power		
K6	VDD	Power		
K7	VSS	Power		
K8	VDD	Power		
K9	VSS	Power		
K10	VDD	Power		
K11	VCAP2	Power		
K12	VDDXSPI2	Power		
K13	PN8	I/O	XSPIM_P2_IO4	
K14	PN4	I/O	XSPIM_P2_IO2	
K15	PN5	I/O	XSPIM_P2_IO3	
L1	PC1	I/O	ETH_MDC	
L2	PC2	I/O	SPI2_MISO	DIB1/DIB3_MISO
L3	PC3	I/O	SPI2_MOSI	DIB1/DIB3_MOSI
L4	PA2	I/O	ETH_MDIO	
L5	PC4	I/O	ETH_RMII_RXD0	
L6	VSS	Power		
L7	VCAP1	Power		
L8	VDDXSPI1	Power		
L9	VDD	Power		
L10	VDDXSPI1	Power		
L11	VSS	Power		
L12	PB12	I/O	LTDC_G5	
M1	PA0	I/O	LTDC_G3	
M2	PA1	I/O	LTDC_G2	
M3	PA4	I/O	LTDC_R3	
M4	PA7	I/O	ETH_RMII_CRS_DV	
M5	PF11	I/O	LTDC_B0	
M6	PE7	I/O	UART7_RX	UART0_RX/DIN2
M7	VSS	Power		

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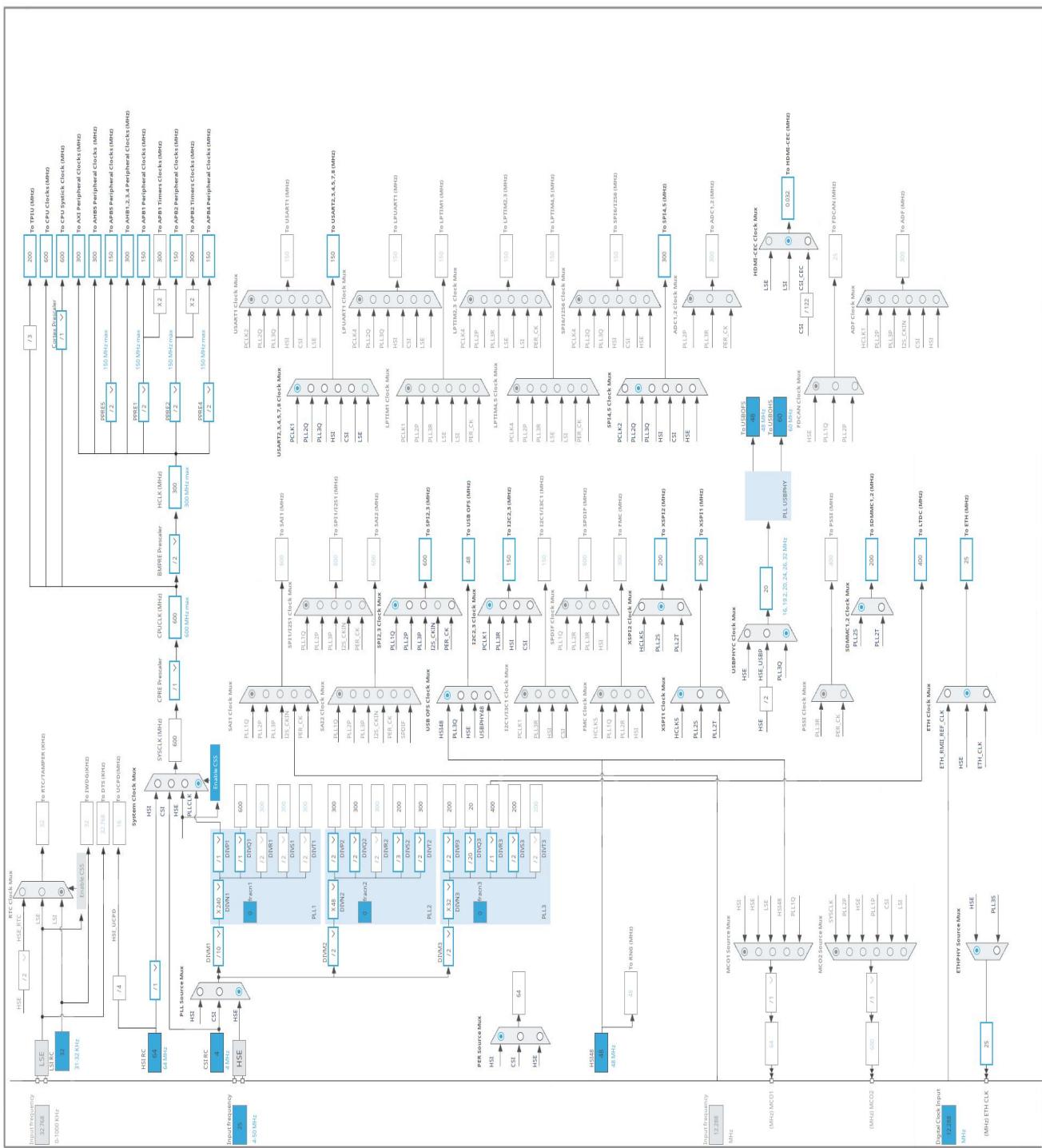
Pin Number TFBGA225 HEXA SMPS	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
M8	VDDXSPI1	Power		
M9	VSS	Power		
M10	VDDXSPI1	Power		
M11	PO3	I/O	XSPIM_P1_DQS1	
M12	PP10	I/O	XSPIM_P1_IO10	
M13	PB14	I/O	UART4_DE	RS485_TX_EN/DOUT2
M14	PB15	I/O	LTDC_G7	
M15	VSS	Power		
N1	PA3	I/O	LTDC_DE	
N2	PA5	I/O	LTDC_CLK	
N3	PC5	I/O	ETH_RMII_RXD1	
N4	PB2	I/O	LTDC_B2	
N5	PF15	I/O	SPI5_SCK	DIB4_SCK
N6	PP12	I/O	XSPIM_P1_IO12	
N7	PP14	I/O	XSPIM_P1_IO14	
N8	VSS	Power		
N9	PP2	I/O	XSPIM_P1_IO2	
N10	PP5	I/O	XSPIM_P1_IO5	
N11	PO2	I/O	XSPIM_P1_DQS0	
N12	PP1	I/O	XSPIM_P1_IO1	
N14	PB11	I/O	LTDC_G6	
N15	PB13	I/O	LTDC_G4	
P1	PA6	I/O	LTDC_B7	
P4	PF14	I/O	LTDC_G0	
P6	PP11	I/O	XSPIM_P1_IO11	
P8	PP15	I/O	XSPIM_P1_IO15	
P9	PP3	I/O	XSPIM_P1_IO3	
P11	PP0	I/O	XSPIM_P1_IO0	
P12	PP7	I/O	XSPIM_P1_IO7	
P13	PP8	I/O	XSPIM_P1_IO8	
P15	PB10	I/O	ETH_MII_RX_ER	
R1	VSS	Power		
R2	PB1	I/O	GPIO_EXTI1	DIB1_IRQ
R3	PF12	I/O	GPIO_EXTI12	GPIO_VREF
R4	PE8	I/O	GPIO_EXTI8	TFT_IRQ
R5	PE10 *	I/O	GPIO_Output	LED_nACT
R6	VSS	Power		
R7	PP13	I/O	XSPIM_P1_IO13	
R8	PP4	I/O	XSPIM_P1_IO4	

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Pin Number TFBGA225 HEXA SMPS	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
R9	VSS	Power		
R10	PO4	I/O	XSPIM_P1_CLK	
R11	PP6	I/O	XSPIM_P1_IO6	
R12	VSS	Power		
R13	PO0	I/O	XSPIM_P1_NCS1	
R14	PP9	I/O	XSPIM_P1_IO9	
R15	VSS	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H7R7/7S7
MCU	STM32H7R7L8HxH
Datasheet	DS000000_Rev1

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

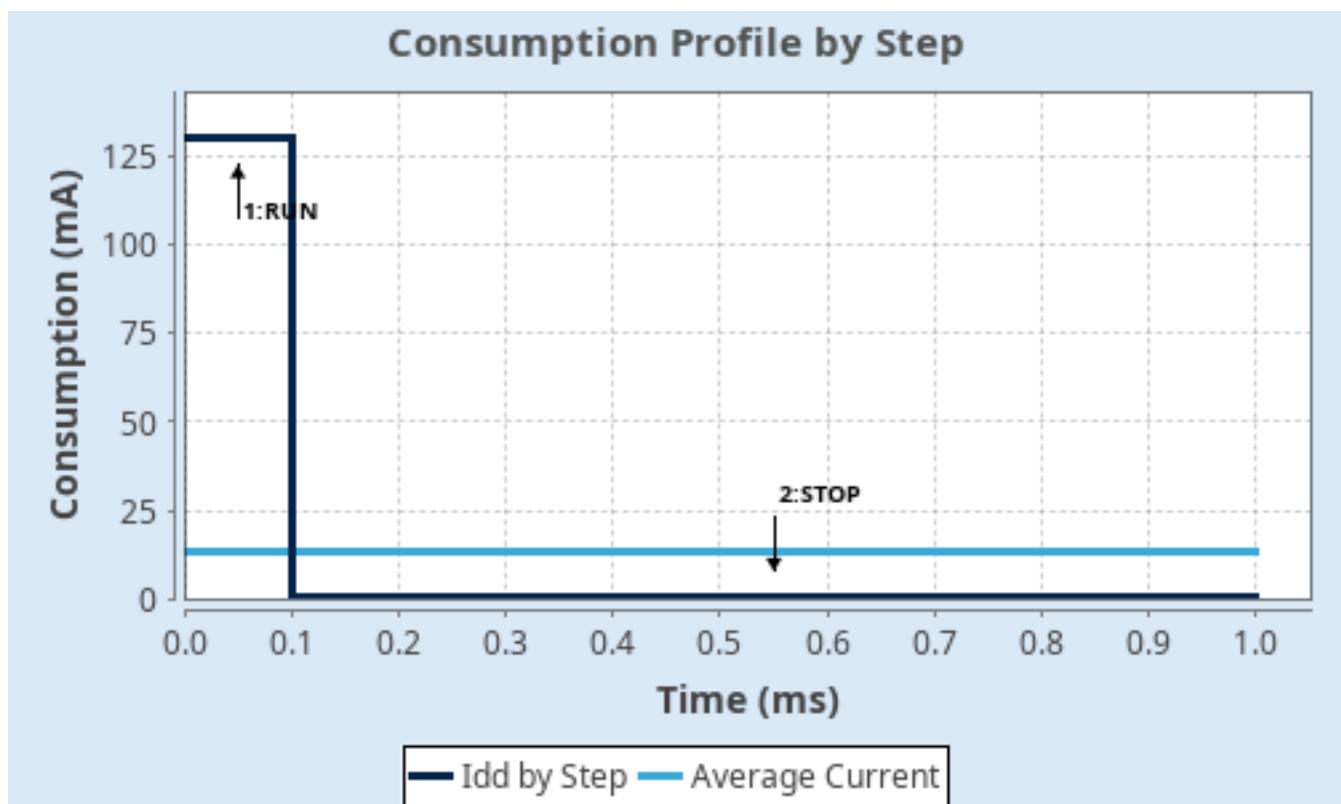
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS-HIGH	SVOS-LOW/SMPS
Fetch Type	AXISRAM3/FlashMode-ON/Cache/AlgoType-CoreMark	FLASH
CPU Frequency	600 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL_CLOCKS OFF
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	130 mA	265 µA
Duration	0.1 ms	0.9 ms
DMIPS	1284.0	0.0
T_a Max	107.45	124.96
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	13.24 mA
Battery Life	1 day, 23 hours	Average DMIPS	128.40001 DMIPS

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	H7R7L8H8
Project Folder	/home/denis/BACKUP/EEZ/PCB/KiCad/BB3plus CM5 STM32H7
Toolchain / IDE	EWARM V9.20
Firmware Package Name and Version	STM32Cube FW_H7RS V1.2.0
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c./h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls Boot

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC

2.4. Advanced Settings - Generated Function Calls Appl

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA2D_Init	DMA2D
4	MX_ETH_Init	ETH
5	MX_GFXMMU_Init	GFXMMU

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Rank	Function Name	Peripheral Instance Name
6	MX_GPU2D_Init	GPU2D
7	MX_HDMI_CEC_Init	HDMI_CEC
8	MX_I2C2_Init	I2C2
9	MX_JPEG_Init	JPEG
10	MX_LTDC_Init	LTDC
11	MX_SDMMC1_SDIO_Init	SDMMC1
12	MX_SPI2_Init	SPI2
13	MX_SPI4_Init	SPI4
14	MX_SPI5_Init	SPI5
15	MX_UART7_Init	UART7
16	MX_USB_OTG_FS_PCD_Init	USB_OTG_FS
17	MX_USB_OTG_HS_PCD_Init	USB_OTG_HS
18	MX_USB_OTG_HS_HCD_Init	USB_OTG_HS
19	MX_XSPI1_Init	XSPI1
20	MX_XSPI2_Init	XSPI2
21	MX_UART4_Init	UART4

2.5. Advanced Settings - Generated Function Calls ExtMemLoader

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC

3. Peripherals and Middlewares Configuration

3.1. DEBUG

Debug: Serial Wire

3.1.1. Core(s) Settings:

Context(s):	Boot
	Application

3.2. DMA2D

mode: Activated

3.2.1. Parameter Settings:

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	ARGB8888
Output Offset	0

Foreground layer Configuration:

DMA2D Input Color Mode	ARGB8888
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0
DMA2D ALPHA Inversion	Regular Alpha
DMA2D Red and Blue swap	Regular mode (RGB or ARGB)
DMA2D Chroma Sub-Sampling Mode	No chroma sub-sampling 4:4:4

3.3. ETH

Mode: RMII

mode: Activate Rx Err signal

3.3.1. Parameter Settings:

General : Ethernet Configuration:

Warning	The ETH can work only when RAM is pointing at 0x24000000
Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4
First Tx Descriptor Address	0x24020080 *

Rx Descriptor Length	4
First Rx Descriptor Address	0x24020000 *
Rx Buffers Address	0x24020100 *
Rx Buffers Length	1524

3.4. GFXMMU

mode: Activated

3.4.1. Parameter Settings:

Basic Parameters:

Block Size	12
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Address Translation:

Address translation	Disable
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Physical address of buffers:

Physical address of buffer 0	0
Physical address of buffer 1	0
Physical address of buffer 2	0
Physical address of buffer 3	0

Interruption enabling:

Interrupts activation	Enable
BUS master error interrupt	Disable
Buffer 0 overflow interrupt	Disable
Buffer 1 overflow interrupt	Disable
Buffer 2 overflow interrupt	Disable
Buffer 3 overflow interrupt	Disable

Packing:

Activation Buffer0	Disable
Mode Buffer0	GFXMMU_PACKING_MSB_REMOVE
Activation Buffer1	Disable
Mode Buffer1	GFXMMU_PACKING_MSB_REMOVE
Activation Buffer2	Disable
Mode Buffer2	GFXMMU_PACKING_MSB_REMOVE
Activation Buffer3	Disable
Mode Buffer3	GFXMMU_PACKING_MSB_REMOVE
Default Alpha	0

3.5. GPU2D

mode: Activated

3.5.1. Core(s) Settings:

Context(s): Application

3.6. HDMI_CEC

mode: Activated

3.6.1. Parameter Settings:

Configuration parameters:

Signal Free Time	2.5, 4 or 6 nominal data bit periods
Rx tolerance	Standard tolerance
Signal Free Time option	SFT timer starts when Transmission Start Of Message is set by software
Listening mode	Receive all messages

Address parameters:

Logical address 0	Disable
Logical address 1	Disable
Logical address 2	Disable
Logical address 3	Disable
Logical address 4	Disable
Logical address 5	Disable
Logical address 6	Disable
Logical address 7	Disable
Logical address 8	Disable
Logical address 9	Disable
Logical address 10	Disable
Logical address 11	Disable
Logical address 12	Disable
Logical address 13	Disable
Logical address 14	Disable
Received data buffer name	cec_receive_buffer

Error handling:

Stop reception on bit rising error	Reception is stopped
Generate error bit on bit rising error	No error bit generation
Generate error bit on long bit period error	No error bit generation
Avoid error bit generation on error detection in broadcast	Error bit generation

3.7. I2C2

I2C: I2C

3.7.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x20C0EDFF *

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

3.8. JPEG

mode: Activated

3.8.1. Parameter Settings:

Version:

JPEG version	jpeg1_v1_0
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JPEG Software options:

ENCODE	Enabled
DECODE	Enabled
RGB_FORMAT	JPEG_ARGB8888
JPEG_SWAP_RG	0

3.9. LTDC

Display Type: RGB888 (24 bits)

3.9.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	8
Horizontal Back Porch	7
Active Width	640
Horizontal Front Porch	6
HSync Width	7
Accumulated Horizontal Back Porch Width	14
Accumulated Active Width	654
Total Width	660

Synchronization for Height:

Vertical Synchronization Height	4
Vertical Back Porch	2
Active Height	480
Vertical Front Porch	2
VSync Height	3
Accumulated Vertical Back Porch Height	5
Accumulated Active Height	485
Total Height	487

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

Layer Default Color:

Red	0
Green	0
Blue	0

3.9.2. Layer Settings:

Layer Default Color:

Layer 0 - Alpha	0
Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0
Layer 1 - Alpha	0
Layer 1 - Blue	0
Layer 1 - Green	0
Layer 1 - Red	0

Number of Layers:

Number of Layers 2 layers

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	0
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	0
Layer 1 - Window Horizontal Start	0
Layer 1 - Window Horizontal Stop	0
Layer 1 - Window Vertical Start	0
Layer 1 - Window Vertical Stop	0

Pixel Parameters:

Layer 0 - Pixel Format	ARGB8888
Layer 1 - Pixel Format	ARGB8888

Blending:

Layer 0 - Alpha constant for blending	0
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant
Layer 1 - Alpha constant for blending	0
Layer 1 - Blending Factor1	Alpha constant
Layer 1 - Blending Factor2	Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	GFXMMU_VIRTUAL_BUFFER0_BASE
Layer 0 - Color Frame Buffer Line Length (Image Width)	0
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	0
Layer 1 - Color Frame Buffer Start Adress	GFXMMU_VIRTUAL_BUFFER0_BASE
Layer 1 - Color Frame Buffer Line Length (Image Width)	0
Layer 1 - Color Frame Buffer Number of Lines (Image Height)	0

3.10. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

mode: Digital Clock Input (ETH_RMII_REF_CLK)

mode: Digital Clock Input (ETH_CLK)

3.10.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_DIRECT_SMPS_SUPPLY
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Power Regulator Voltage Scale Power Regulator Voltage Scale 0

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
HSI Calibration Value	64

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

PLL range Parameters:

PLL1 input frequency range	Between 2 and 4 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL3 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	High VCO range
PLL2 clock Output range	High VCO range
PLL3 clock Output range	Wide VCO range

3.11. SDMMC1

Mode: SDIO 8 bits Wide bus

3.11.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMC clock divide factor	0
Is external transceiver present ?	no

3.12. SPI2

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

3.12.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	4 *
Baud Rate	150.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

CRC Parameters:

CRC Calculation	Disabled
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Advanced Parameters:

NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled
Ready Master Management	Internal
Ready Signal Polarity	High

3.13. SPI4

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

3.13.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	150.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

CRC Parameters:

CRC Calculation	Disabled
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Advanced Parameters:

NSSP Mode	Enabled
NSS Signal Type	Output Hardware

Fifo Threshold	Fifo Threshold 01 Data
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled
Ready Master Management	Internal
Ready Signal Polarity	High

3.14. SPI5

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

3.14.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	150.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

CRC Parameters:

CRC Calculation	Disabled
-----------------	----------

Advanced Parameters:

NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled
Ready Master Management	Internal
Ready Signal Polarity	High

3.15. UART4

Mode: Asynchronous

mode: Hardware Flow Control (RS485)

3.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration
Polarity	High
Assertion Time	0
Deassertion Time	0

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

3.16. UART7

Mode: Asynchronous

3.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
-----------	--------

Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

3.17. USB_OTG_FS

Mode: Device_Only

3.17.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Low power	Disabled
Battery charging	Disabled
Link Power Management	Disabled
VBUS sensing	Disabled
Use dedicated end point 1 interrupt	Disabled
Signal start of frame	Disabled

3.18. USB_OTG_HS

Internal HS Phy: OTG/Dual_Role_Device

Activate_VBUS: Activate-VBUS

3.18.1. Parameter Settings:

USB_OTG_Device_Configuration:

Speed_Device	Device High Speed 480MBit/s
Enable internal IP DMA Device	Disabled
Physical interface	Internal HS Phy
Low power	Disabled
Use dedicated endpoint 1 interrupt	Disabled
VBUS sensing	Enabled
Signal start of frame	Disabled

USB_OTG_Host_Configuration:

Host Channels	16
Speed_Host	Host High Speed 480MBit/s
Enable internal IP DMA Host	Disabled
Use external vbus	Enabled

OTG PHY reference clock selection:

Ref Clock Selection	16 Mhz
---------------------	--------

3.19. USB_OTG_HS1

mode: activate

3.19.1. Parameter Settings:

Internal_Phys_Host:

Host Channels	16
Speed_Host	High Speed 480MBit/s
Enable internal IP DMA Host	Disabled
Use external vbus	Enabled
Ref Clock Selection	16 Mhz
Physical interface	Internal HS Phy

3.20. XSPI1

Mode: Hexa SPI

Port: Port1 Hexa

Chip Select Override: NCS1 -- Port1 --

3.20.1. Parameter Settings:

Generic:

Fifo Threshold	1
----------------	---

Memory Mode	Disable
Memory Type	Micron
Memory Size	16 Bits
Chip Select High Time Cycle	1
Free Running Clock	Disable
Clock Mode	Low
Wrap Size	Not Supported
Clock Prescaler	0
Sample Shifting	None
Delay Hold Quarter Cycle	Disable
Chip Select Boundary	Disabled
Maximum Transfer	0
Refresh Rate	0
Memory Select	NCS1

3.21. XSPI2

Mode: Octo SPI

Port: Port2 Octo

Chip Select Override: NCS1 -- Port2 --

3.21.1. Parameter Settings:

Generic:

Fifo Threshold	1
Memory Mode	Disable
Memory Type	Micron
Memory Size	16 Bits
Chip Select High Time Cycle	1
Free Running Clock	Disable
Clock Mode	Low
Wrap Size	Not Supported
Clock Prescaler	0
Sample Shifting	None
Delay Hold Quarter Cycle	Disable
Chip Select Boundary	Disabled
Maximum Transfer	0
Refresh Rate	0
Memory Select	NCS1

* User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DEBUG	PA14(JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
	PA13(JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
ETH	PD7	ETH_RMII_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB7	ETH_RMII_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG11	ETH_RMII_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG13	ETH_RMII_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC4	ETH_RMII_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	ETH_RMII_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC5	ETH_RMII_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
HDMI_CEC	PB6	CEC	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PF0	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	SDA
I2C2	PF1	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	SCL
	PD3	LTDC_B1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
LTDC	PB5	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG0	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB3(JTDO/T RACESWO)	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG2	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA11	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG1	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA10	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG12	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low	

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Configuration Report

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
LTDC	PA15(JTDI)	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF9	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF10	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB12	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA0	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA4	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF11	LTDC_B0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA5	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB2	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF14	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PD6	ETH_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH0-OSC_IN(PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT(PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SDMMC1	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB8	SDMMC1_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB9	SDMMC1_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC6	SDMMC1_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC7	SDMMC1_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI2	PA12	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	DIB1/DIB3_SCK
	PB4(NJTRS T)	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	DIB1_CSA
	PC2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	DIB1/DIB3_MISO
	PC3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	DIB1/DIB3_MOSI
SPI4	PE14	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	DIB2/DIB5_MOSI
	PE2	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	DIB2/DIB5_SCK
	PE13	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	DIB2/DIB5_MISO

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Configuration Report

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE4	SPI4_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	DIB2_CSA
SPI5	PM13	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	DIB4_MOSI
	PM14	SPI5_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	DIB4_MISO
	PF6	SPI5_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	DIB4_CSA
	PF15	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	DIB4_SCK
UART4	PD1	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	UART1_TX/DOUT1
	PD0	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	UART1_RX/DIN1
	PB14	UART4_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	RS485_TX_EN/DOUT2
UART7	PF7	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	UART0_TX/DOUT3
	PE7	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	UART0_RX/DIN2
USB_OTG_FS	PM12	USB_OTG_FS_DM	n/a	n/a	n/a	
	PM11	USB_OTG_FS_DP	n/a	n/a	n/a	
USB_OTG_HS	PM6	USB_OTG_HS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PM9	USB_OTG_HS_ID	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PM5	USB_OTG_HS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PM8	USB_OTG_HS_VBUS	Input mode	No pull-up and no pull-down	n/a	
XSPI1	PO3	XSPIM_P1_DQS1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PP10	XSPIM_P1_IO10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PP12	XSPIM_P1_IO12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PP14	XSPIM_P1_IO14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PP2	XSPIM_P1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PP5	XSPIM_P1_IO5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PO2	XSPIM_P1_DQS0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PP1	XSPIM_P1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PP11	XSPIM_P1_IO11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PP15	XSPIM_P1_IO15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PP3	XSPIM_P1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PP0	XSPIM_P1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PP7	XSPIM_P1_IO7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PP8	XSPIM_P1_IO8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PP13	XSPIM_P1_IO13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PP4	XSPIM_P1_IO4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PO4	XSPIM_P1_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PP6	XSPIM_P1_IO6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

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Configuration Report

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PO0	XSPIM_P1_NCS_1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PP9	XSPIM_P1_IO9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
XSPI2	PN1	XSPIM_P2_NCS_1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PN3	XSPIM_P2_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PN0	XSPIM_P2_DQS_0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PN11	XSPIM_P2_IO7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PN10	XSPIM_P2_IO6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PN9	XSPIM_P2_IO5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PN2	XSPIM_P2_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PN6	XSPIM_P2_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PN8	XSPIM_P2_IO4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PN4	XSPIM_P2_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PN5	XSPIM_P2_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
GPIO	PE0	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	SYSMCU_IRQ
	PF3	GPIO_EXTI3	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	DIB3_IRQ
	PF2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	DIB2_IRQ
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WDG_OUT
	PM3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIB3_CSA
	PF4	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	DIB4_IRQ
	PD5	GPIO_EXTI5	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	DIB5_IRQ
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_ON
	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIB5_CSA
	PG14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SYSMCU_CS
	PB1	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	DIB1_IRQ
	PF12	GPIO_EXTI12	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	GPIO_VREF
	PE8	GPIO_EXTI8	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	TFT_IRQ
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_nACT

4.2. GPDMA1

4.2.1. Core(s) Settings:

Context(s): Boot
 Application
 ExternalMemoryLoader
Initialized Context: ExternalMemoryLoader
Power Domain:

4.3. HPDMA1

4.3.1. Core(s) Settings:

Context(s): Boot
 Application
 ExternalMemoryLoader
Initialized Context: ExternalMemoryLoader
Power Domain:

4.4. LINKEDLIST

4.4.1. Core(s) Settings:

Context(s): Boot
 Application
 ExternalMemoryLoader
Initialized Context: ExternalMemoryLoader
Power Domain:

4.5. NVIC configuration

4.5.1. NVIC1

Interrupt Table	Enable	Preenemption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
HDMI-CEC global interrupt	true	0	0
GPU2D global interrupt	true	0	0
GPU2D Error interrupt	true	0	0
PVD and PVM interrupts through EXTI line		unused	
RCC global interrupt		unused	
FLASH interrupts		unused	
FPU global interrupt		unused	
EXTI line0 interrupt		unused	
EXTI line1 interrupt		unused	
EXTI line2 interrupt		unused	
EXTI line3 interrupt		unused	
EXTI line4 interrupt		unused	
EXTI line5 interrupt		unused	
EXTI line8 interrupt		unused	
EXTI line12 interrupt		unused	
SPI2 global interrupt		unused	
SPI4 global interrupt		unused	
SPI5 global interrupt		unused	
I2C2 event interrupt		unused	
I2C2 error interrupt		unused	
UART4 global interrupt		unused	
UART7 global interrupt		unused	
USB OTG HS interrupt		unused	
Ethernet global interrupt		unused	
LTDC global interrupt		unused	
LTDC Error global Interrupt		unused	
DMA2D global interrupt		unused	
JPEG global interrupt		unused	
GFXMMU global interrupt		unused	

Interrupt Table	Enable	Preenmption Priority	SubPriority
XSPI1 global interrupt		unused	
XSPI2 global interrupt		unused	
SDMMC1 global interrupt		unused	
USB OTG FS interrupt		unused	
USB OTG HS Host interrupt		unused	

4.5.2. NVIC1 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
HDMI-CEC global interrupt	false	true	true
GPU2D global interrupt	false	true	true
GPU2D Error interrupt	false	true	true

4.5.3. NVIC2

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
PVD and PVM interrupts through EXTI line		unused	
RCC global interrupt		unused	
FLASH interrupts		unused	
FPU global interrupt		unused	
EXTI line0 interrupt		unused	
EXTI line1 interrupt		unused	
EXTI line2 interrupt		unused	

Interrupt Table	Enable	Preenmption Priority	SubPriority
EXTI line3 interrupt		unused	
EXTI line4 interrupt		unused	
EXTI line5 interrupt		unused	
EXTI line8 interrupt		unused	
EXTI line12 interrupt		unused	

4.5.4. NVIC2 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

* User modified value

5. System Views

5.1. Category view

5.1.1. Current

Category view Context Execution view Context Initialization view

Choose filters by Context Execution ... by Context Initialization

Boot Application ExternalMemoryLoader None

Middleware

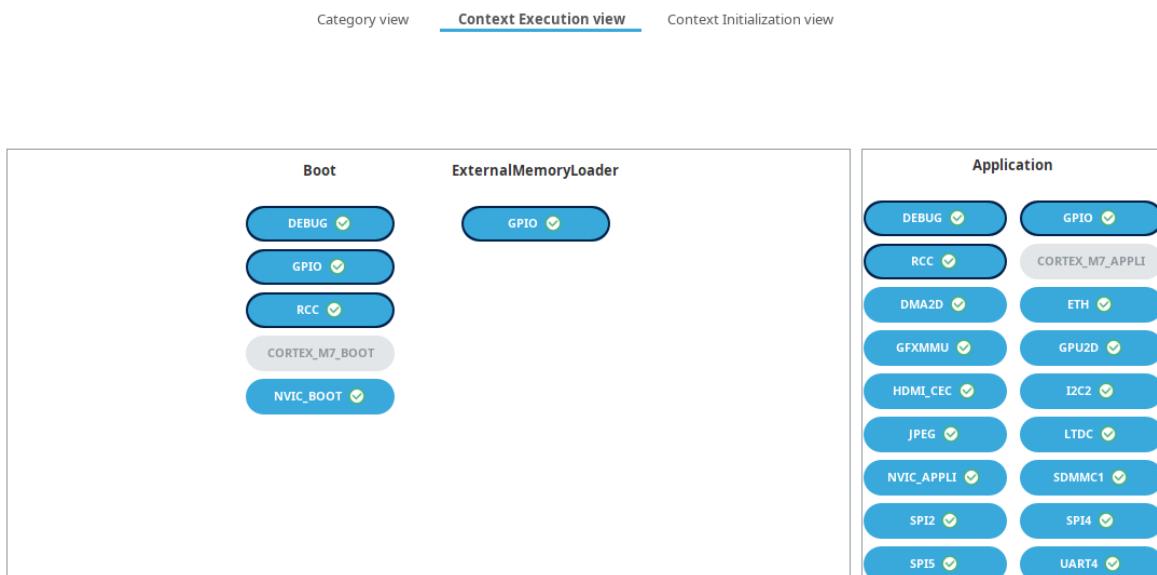
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Trace and Debug	Power and Thermal	Utilities	Other	
CORTEX_M7_APPLI			ETH ✓	I2C2 ✓	DMA2D ✓		DEBUG ✓			LINKEDLIST	USB_HS1 ✓
CORTEX_M7_BOOT			SDMMC1 ✓	SPI2 ✓	GFXMMU ✓						
GPDMA1			SPI4 ✓	SPI5 ✓	GPU2D ✓						
GPIO ✓			UART4 ✓	UART7 ✓	HDMI_CEC ✓						
HPDMA1			USB_FS ✓	USB_HS ✓	JPEG ✓						
NVIC_APPLI ✓			XSPI1 ✓	XSPI2 ✓	LTDC ✓						
NVIC_BOOT ✓											
RCC ✓											

5.1.2. Without filters

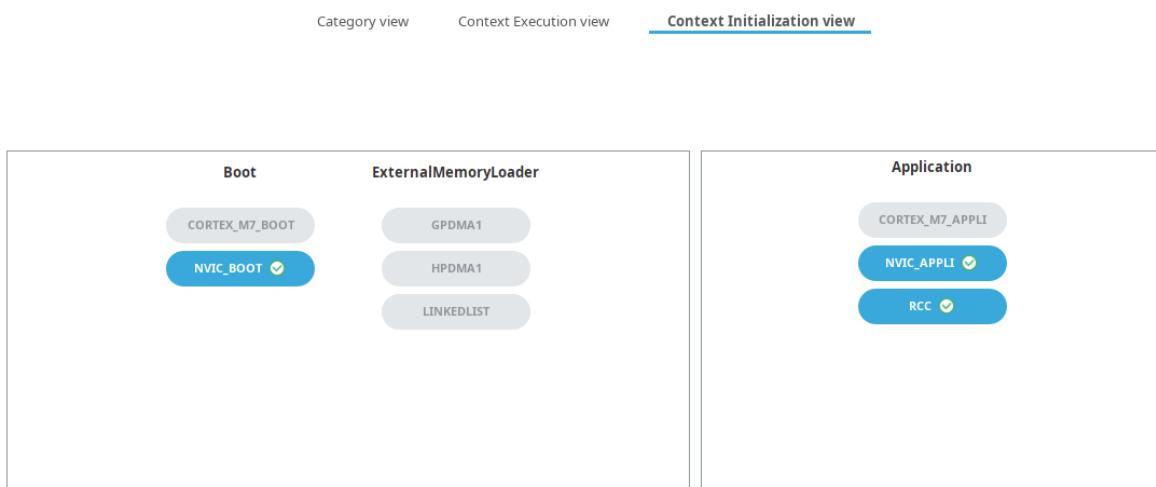
The screenshot shows the 'Category view' of the 'Middleware' section in the configuration tool. At the top, there are three tabs: 'Category view' (which is selected), 'Context Execution view', and 'Context Initialization view'. Below the tabs is a toolbar with icons for file operations (New, Open, Save, Refresh) and a search bar labeled 'Choose filters ...'. There are two filter sections: '... by Context Execution' containing checkboxes for 'Boot' (unchecked), 'Application' (unchecked), and 'ExternalMemoryLoader' (unchecked); and '... by Context Initialization' containing radio buttons for 'Boot' (unchecked), 'Application' (unchecked), 'ExternalMemoryLoader' (unchecked), and 'None' (checked). The main area is titled 'Middleware' and contains a grid of components. The components are organized into columns: System Core, Analog, Timers, Connectivity, Multimedia, Security, Computing, Trace and Debug, Power and Thermal, Utilities, and Other. Each component has a status indicator (green checkmark or red error icon) and a small description. For example, under 'System Core', components like CORTEX_M7_APPLI, CORTEX_M7_BOOT, GPDMA1, GPIO, HPDMA1, NVIC_APPLI, NVIC_BOOT, and RCC are listed. Under 'Connectivity', components like ETH, I2C2, DMA2D, SDMMC1, SPI2, GFXMMU, SPI4, SPI5, GPU2D, UART4, UART7, HDMI_CEC, USB_FS, USB_HS, JPEG, XSPI1, XSPI2, and LTDC are listed. The 'Trace and Debug' column contains a single component, 'DEBUG', which is highlighted with a blue background. The 'Utilities' and 'Other' columns are currently empty.

System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Trace and Debug	Power and Thermal	Utilities	Other	
CORTEX_M7_APPLI			ETH ✓	I2C2 ✓	DMA2D ✓		DEBUG ✓			LINKEDLIST	USB_HS1 ✓
CORTEX_M7_BOOT			SDMMC1 ✓	SPI2 ✓	GFXMMU ✓						
GPDMA1			SPI4 ✓	SPI5 ✓	GPU2D ✓						
GPIO ✓			UART4 ✓	UART7 ✓	HDMI_CEC ✓						
HPDMA1			USB_FS ✓	USB_HS ✓	JPEG ✓						
NVIC_APPLI ✓			XSPI1 ✓	XSPI2 ✓	LTDC ✓						
NVIC_BOOT ✓											
RCC ✓											

5.2. Context Execution view



5.3. Context Initialization view



6. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip
System View	https://www.st.com/resource/en/svd/stm32h7rs-svd.zip
Description	
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32h7rs-lines-overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-graphics-solution-overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-graphics-solutions-detailed.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32trust.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32h7rs.pdf
Security Bulletin	https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf
Security Bulletin	https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-

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Application Notes https://www.st.com/resource/en/application_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf

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sfsp-versions-for-stm32h7rx7sx-mcus-stmicroelectronics.pdf

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- Application Notes https://www.st.com/resource/en/application_note/an5450-stm32h7a37b3-lines-and-stm32h7b0-value-line-smart-power-management-expansion-package-for-stm32cube-stmicroelectronics.pdf
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- Design Notes & https://www.st.com/resource/en/design_tip/dt0117-microphone-array-beamforming-in-the-pcm-and-pdm-domain-stmicroelectronics.pdf
Tips
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Programming Manuals	https://www.st.com/resource/en/programming_manual/pm0253-stm32f7-series-and-stm32h7-series-cortexm7-processor-programming-manual-stmicroelectronics.pdf
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Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1163-description-of-wlcsp-for-microcontrollers-and-recommendations-for-its-use-stmicroelectronics.pdf
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