Key: Port unavailable if USB enabled on that tile
Port unavailable if RGMII enabled
Port unavailable if RGMII or USB enabled on tile 1 / tile 3 (as appropriate)

Note: I/O rail supply column only applies in packages where VDDIO is spplit into L and R. Please refer to the product datasheet.

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	Port						Reserved Pins		Features			Pin name	XE2xx package pin	I/O direction	EEZ eval. board function
	1b	4b	8b	16b	32b	Link	QSPI	RGMII	I/O rail	BANK	Drive mA		TQ128		
Tile 0	P1A0								IOL	0	4	X0D00	30	Out	SD_RAS
	P1B0					xlink3_tx2	SS		IOL	0	4	X0D01	27	Out	SD_CAS
		P4A0	P8A0	P16A0	P32A20				IOL	0	4	X0D02	37	In/out	SD_ADQ0
		P4A1	P8A1	P16A1	P32A21				IOL	0	4	X0D03	38	In/out	SD_ADQ1
		P4B0	P8A2	P16A2	P32A22		IO0		IOL	0	4	X0D04	31	In/out	SD_ADQ2
		P4B1	P8A3	P16A3	P32A23		IO1		IOL	0	4	X0D05	33	In/out	SD_ADQ3
		P4B2	P8A4	P16A4	P32A24		IO2		IOL	0	4	X0D06	34	In/out	SD_ADQ4
		P4B3	P8A5	P16A5	P32A25		IO3		IOL	0	4	X0D07	35	In/out	SD_ADQ5
		P4A2	P8A6	P16A6	P32A26				IOL	0	4	X0D08	39	In/out	SD_ADQ6
		P4A3	P8A7	P16A7	P32A27				IOL	0	4	X0D09	40	In/out	SD_ADQ7
	P1C0					xlink3_tx3	QSCLK		IOL	0	4	X0D10	28	Out	SD_WE
	P1D0								IOL	0	4	X0D11	32	Out (PWM)	LCD_BRIGHTNESS
	P1E0								IOR	1	4	X0D12	62	Out (PWM)	AUDIO_OUT
	P1F0								IOR	1	4	X0D13	63	Out	SD_CLK
		P4C0	P8B0	P16A8	P32A28				IOR	1	4	X0D14	57	In/out	SD_ADQ8
		P4C1	P8B1	P16A9	P32A29				IOR	1	4	X0D15	58	In/out	SD_ADQ9
		P4D0	P8B2	P16A10		xlink4_rx4			IOR	1	4	X0D16	68	In/out	SD_ADQ10
		P4D1	P8B3	P16A11		xlink4_rx3			IOR	1	4	X0D17	69	In/out	SD_ADQ11
		P4D2	P8B4	P16A12		xlink4_rx2			IOR	1	4	X0D18	70	In/out	SD_ADQ12
		P4D3	P8B5	P16A13		xlink4_rx1			IOR	1	4	X0D19	71	In/out	SD_ADQ13/BA0
		P4C2	P8B6	P16A14	P32A30				IOR	1	4	X0D20	59	In/out	SD_ADQ14/BA1
		P4C3	P8B7	P16A15	P32A31				IOR	1	4	X0D21	61	In/out	SD_ADQ15
	P1G0								IOR	1	4	X0D22	64	Out	LCD_VSYNC
	P1H0								IOR	1	4	X0D23	66	Out	LCD_DE
	P1I0					xlink7_rx0			IOR	2	4	X0D24	88	Out	LCD_CLK
	P1J0					xlink7_tx0			IOR	2	4	X0D25	89	Out	LCD_HSYNC
		P4E0	P8C0	P16B0		xlink7_tx3			IOR	2	4	X0D26	93	Out	SPI0_MOSI
		P4E1	P8C1	P16B1		xlink7_tx4			IOR	2	4	X0D27	94	Out	SPI1_CLK
		P4F0	P8C2	P16B2					IOR	2	4	X0D28	96	Out	SPI2_CLK
		P4F1	P8C3	P16B3					IOR	2	4	X0D29	98	Out	SPI2_MOSI
		P4F2	P8C4	P16B4					IOR	2	4	X0D30	99	Out	SPI1_MOSI
		P4F3	P8C5	P16B5					IOR	2	4	X0D31	100	Out	SPI0_CLK

Key: Port unavailable if USB enabled on that tile
Port unavailable if RGMII enabled
Port unavailable if RGMII or USB enabled on tile 1 / tile 3 (as appropriate)

Note: I/O rail supply column only applies in packages where VDDIO is spplit into L and R. Please refer to the product datasheet.

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	Port						Reserved Pins		Features			Pin name	XE2xx package pin	I/O direction	EEZ eval. board function
	1b	4b	8b	16b	32b	Link	QSPI	RGMII	I/O rail	BANK	Drive mA		TQ128		
		P4E2	P8C6	P16B6					IOR	2	4	X0D32	95	Out	SPI0_STROBE
		P4E3	P8C7	P16B7					IOR	2	4	X0D33	97	Out	SPI1_SELECT
	P1K0					xlink7_tx1			IOR	2	4	X0D34	90	Out	SPI2_SELECT
	P1L0					xlink7_tx2			IOR	2	4	X0D35	91	In	SPI1_MISO
	P1M0		P8D0	P16B8					IOL	3	4	X0D36	3	In	SPI2_MISO
	P1N0		P8D1	P16B9		xlink0_rx4			IOL	3	4	X0D37	4	In	SPI0_TOUCH
	P1O0		P8D2	P16B10		xlink0_rx3			IOL	3	4	X0D38	5	In/out	GPIO38
	P1P0		P8D3	P16B11		xlink0_rx2			IOL	3	4	X0D39	7	In/out	GPIO39
			P8D4	P16B12		xlink0_rx1			IOL	3	4	X0D40	8	In/out	XL_DN1 (Debug)
			P8D5	P16B13		xlink0_rx0			IOL	3	4	X0D41	9	In/out	XL_DN0 (Debug)
			P8D6	P16B14		xlink0_tx0			IOL	3	4	X0D42	10	In/out	XL_UP0 (Debug)
			P8D7	P16B15		xlink0_tx1			IOL	3	4	X0D43	12	In/out	XL_UP1 (Debug)

Key: Port unavailable if USB enabled on that tile
Port unavailable if RGMII enabled
Port unavailable if RGMII or USB enabled on tile 1 / tile 3 (as appropriate)

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	Port						Reserved Pins		Features			Pin name	XE2xx package pin	I/O direction	EEZ eval. board function
	1b	4b	8b	16b	32b	Link	QSPI	RGMII	I/O rail	BANK	Drive mA		TQ128		
Tile 1	P1A0					xlink7_rx2			IOR	0	4	X1D00	85	n/a	Eth lib reserved
	P1B0					xlink7_rx1			IOR	0	4	X1D01	86	n/a	Eth lib reserved
		P4A0	P8A0	P16A0	P32A20	xlink4_rx0			IOR	0	4	X1D02	72	n/a	USB lib?
		P4A1	P8A1	P16A1	P32A21	xlink4_tx0			IOR	0	4	X1D03	74	n/a	USB lib?
		P4B0	P8A2	P16A2	P32A22	xlink4_tx1			IOR	0	4	X1D04	75	n/a	USB lib?
		P4B1	P8A3	P16A3	P32A23	xlink4_tx2			IOR	0	4	X1D05	76	n/a	USB lib?
		P4B2	P8A4	P16A4	P32A24	xlink4_tx3			IOR	0	4	X1D06	77	n/a	USB lib?
		P4B3	P8A5	P16A5	P32A25	xlink4_tx4			IOR	0	4	X1D07	79	n/a	USB lib?
		P4A2	P8A6	P16A6	P32A26	xlink7_rx4			IOR	0	4	X1D08	82	n/a	USB lib?
		P4A3	P8A7	P16A7	P32A27	xlink7_rx3			IOR	0	4	X1D09	84	n/a	USB lib?
	P1C0								IOT	0	4	X1D10	121	In/out	MDIO
	P1D0								IOT	0	4	X1D11	122	Out	MDC
	P1E0								IOL	1	4	X1D12	N.C.		
	P1F0								IOL	1	4	X1D13	N.C.		
		P4C0	P8B0	P16A8	P32A28				IOR	1	4	X1D14	51	n/a	Eth lib dummy
		P4C1	P8B1	P16A9	P32A29				IOR	1	4	X1D15	53	n/a	Eth lib dummy
		P4D0	P8B2	P16A10		xlink3_rx1			IOL	1	4	X1D16	22	n/a	Eth lib dummy
		P4D1	P8B3	P16A11		xlink3_rx0			IOL	1	4	X1D17	23	n/a	Eth lib dummy
		P4D2	P8B4	P16A12		xlink3_tx0			IOL	1	4	X1D18	25	n/a	Eth lib dummy
		P4D3	P8B5	P16A13		xlink3_tx1			IOL	1	4	X1D19	26	n/a	Eth lib dummy
		P4C2	P8B6	P16A14	P32A30				IOR	1	4	X1D20	54	n/a	Eth lib dummy
		P4C3	P8B7	P16A15	P32A31				IOR	1	4	X1D21	55	n/a	Eth lib dummy
	P1G0					xlink3_tx4			IOL	1	4	X1D22	N.C.		
	P1H0								IOL	1	4	X1D23	N.C.		
	P1I0								IOR	2	4	X1D24	N.C.		
	P1J0								IOR	2	4	X1D25	N.C.		
		P4E0	P8C0	P16B0				**tx_clk**	IOT	2	8	X1D26	112	Out	TX_CLK
		P4E1	P8C1	P16B1				**tx_ctl**	IOT	2	8	X1D27	113	Out	TX_CTL
		P4F0	P8C2	P16B2				**rx_clk**	IOT	2	4	X1D28	114	In	RX_CLK
		P4F1	P8C3	P16B3				**rx_ctl**	IOT	2	4	X1D29	115	In	RX_CTL
		P4F2	P8C4	P16B4				**rx0**	IOT	2	4	X1D30	116	In	RX0
		P4F3	P8C5	P16B5				**rx1**	IOT	2	4	X1D31	117	In	RX1

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	Port						Reserved Pins		Features			Pin name	XE2xx package pin	I/O direction	EEZ eval. board function
	1b	4b	8b	16b	32b	Link	QSPI	RGMII	I/O rail	BANK	Drive mA		TQ128		
		P4E2	P8C6	P16B6				**rx2**	IOT	2	4	**X1D32**	**118**	In	RX2
		P4E3	P8C7	P16B7				**rx3**	IOT	2	4	**X1D33**	**119**	In	RX3
	P1K0					xlink0_tx2			IOL	2	4	**X1D34**	**N.C.**		
	P1L0					xlink0_tx3			IOL	2	4	**X1D35**	**13**	In	SPI_INT
	P1M0		P8D0	P16B8		xlink0_tx4			IOL	3	4	**X1D36**	**15**	In	ETH_RX_ER
	P1N0		P8D1	P16B9		xlink3_rx4			IOL	3	4	**X1D37**	**18**	Out	ETH_RST
	P1O0		P8D2	P16B10		xlink3_rx3			IOL	3	4	**X1D38**	**20**		
	P1P0		P8D3	P16B11		xlink3_rx2			IOL	3	4	**X1D39**	**21**		
			P8D4	P16B12				**tx3**	IOT	3	8	**X1D40**	**106**	In/out	TX3
			P8D5	P16B13				**tx2**	IOT	3	8	**X1D41**	**107**	Out	TX2
			P8D6	P16B14				**tx1**	IOT	3	8	**X1D42**	**108**	Out	TX1
			P8D7	P16B15				**tx0**	IOT	3	8	**X1D43**	**109**	Out	TX0

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	Port						Reserved Pins		Features			Pin name	XE2xx package pin	I/O direction	EEZ eval. board function
	1b	4b	8b	16b	32b	Link	QSPI	RGMII	I/O rail	BANK	Drive mA		TQ128		
USB 0												USB_DM	47		USB_D_N
												USB_DP	46		USB_D_P
												USB_ID	43		TP6 (test point)
												USB_RTUNE	48		Resistor 43R2 to GND
												USB_VBUS	45		USB_VBUS
												USB_VDD	49		1V0
Power/Gnd/JTAG												CLK	125		24M_CLK
												RST_N	124		RST_N
												TCK	128		TCK (Debug)
												TDI	2		TDI (Debug)
												TDO	1		TDO (Debug)
												TMS	127		TMS (Debug)
												TRST_N	123		RST_N
												PLL_AVDD	103		1V0
												PLL_AGND	104		GND
												OTP_VCC	105		3V3
												VSS	PADDLE		GND
												VDD	101 102 11 120 126 16 17 24 36 41 56 60 73 80 81 87		1V0
												USB_VDD33	44		3V3
												VDDIOL	6 14 19 29 42		3V3
												VDDIOR	52 67 78 83 92		3V3
												VDDIOT	110 111		3V3