
STM32
CubeMX

1. Description

1.1. Project

Project Name	stm429_oberon_station
Board Name	STM32F429I-DISC1
Generated with:	STM32CubeMX 6.10.0
Date	02/18/2024

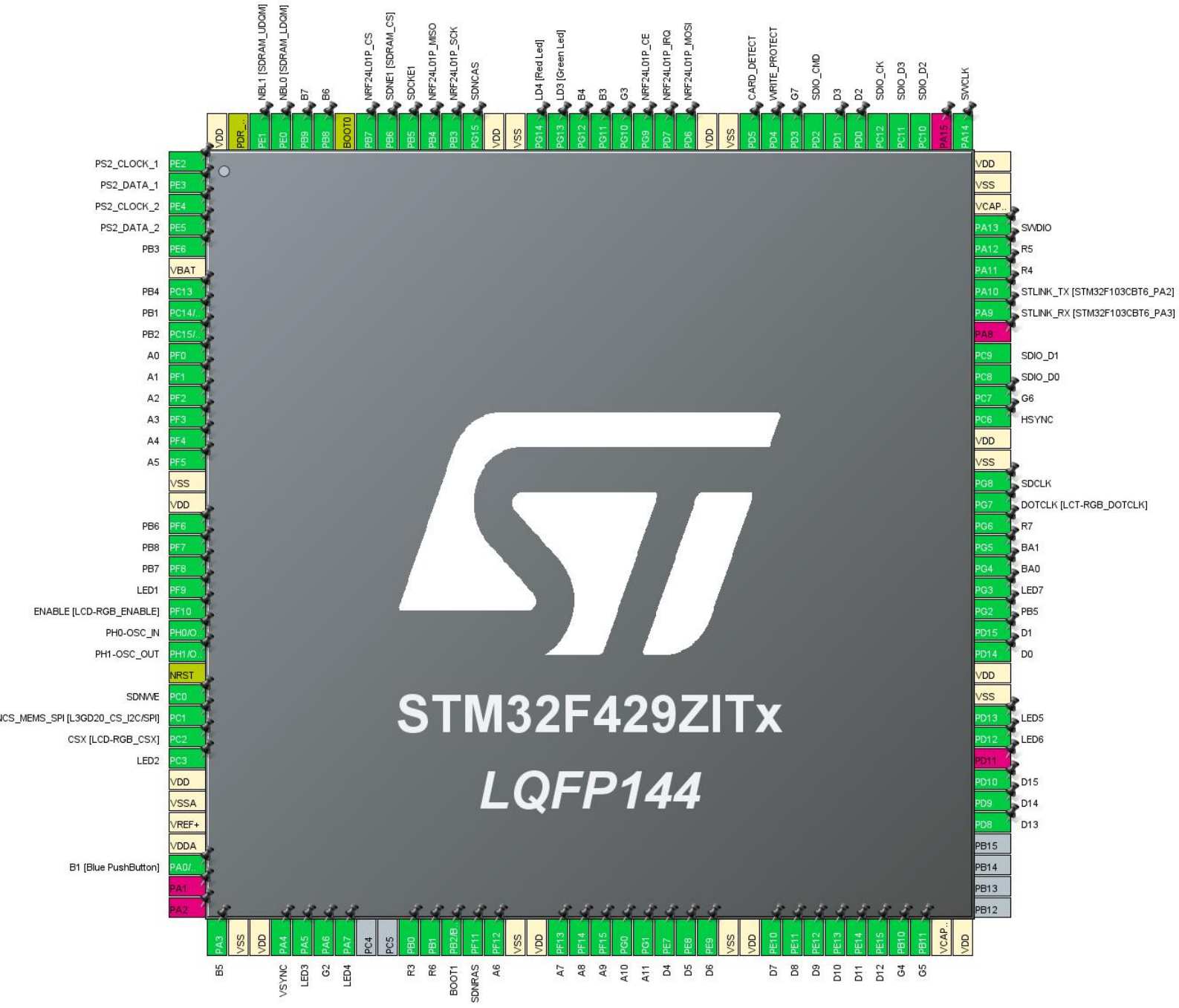
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F429ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	GPIO_EXTI2	PS2_CLOCK_1
2	PE3 *	I/O	GPIO_Input	PS2_DATA_1
3	PE4	I/O	GPIO_EXTI4	PS2_CLOCK_2
4	PE5 *	I/O	GPIO_Input	PS2_DATA_2
5	PE6 *	I/O	GPIO_Input	PB3
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	PB4
8	PC14/OSC32_IN	I/O	GPIO_EXTI14	PB1
9	PC15/OSC32_OUT *	I/O	GPIO_Input	PB2
10	PF0	I/O	FMC_A0	A0
11	PF1	I/O	FMC_A1	A1
12	PF2	I/O	FMC_A2	A2
13	PF3	I/O	FMC_A3	A3
14	PF4	I/O	FMC_A4	A4
15	PF5	I/O	FMC_A5	A5
16	VSS	Power		
17	VDD	Power		
18	PF6 *	I/O	GPIO_Input	PB6
19	PF7 *	I/O	GPIO_Input	PB8
20	PF8 *	I/O	GPIO_Input	PB7
21	PF9 *	I/O	GPIO_Output	LED1
22	PF10	I/O	LTDC_DE	ENABLE [LCD-RGB_ENABLE]
23	PH0/OSC_IN	I/O	RCC_OSC_IN	PH0-OSC_IN
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	PH1-OSC_OUT
25	NRST	Reset		
26	PC0	I/O	FMC_SDNWE	SDNWE
27	PC1 *	I/O	GPIO_Output	NCS_MEMS_SPI [L3GD20_CS_I2C/SPI]
28	PC2 *	I/O	GPIO_Output	CSX [LCD-RGB_CSX]
29	PC3 *	I/O	GPIO_Output	LED2
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	GPIO_EXTI0	B1 [Blue PushButton]

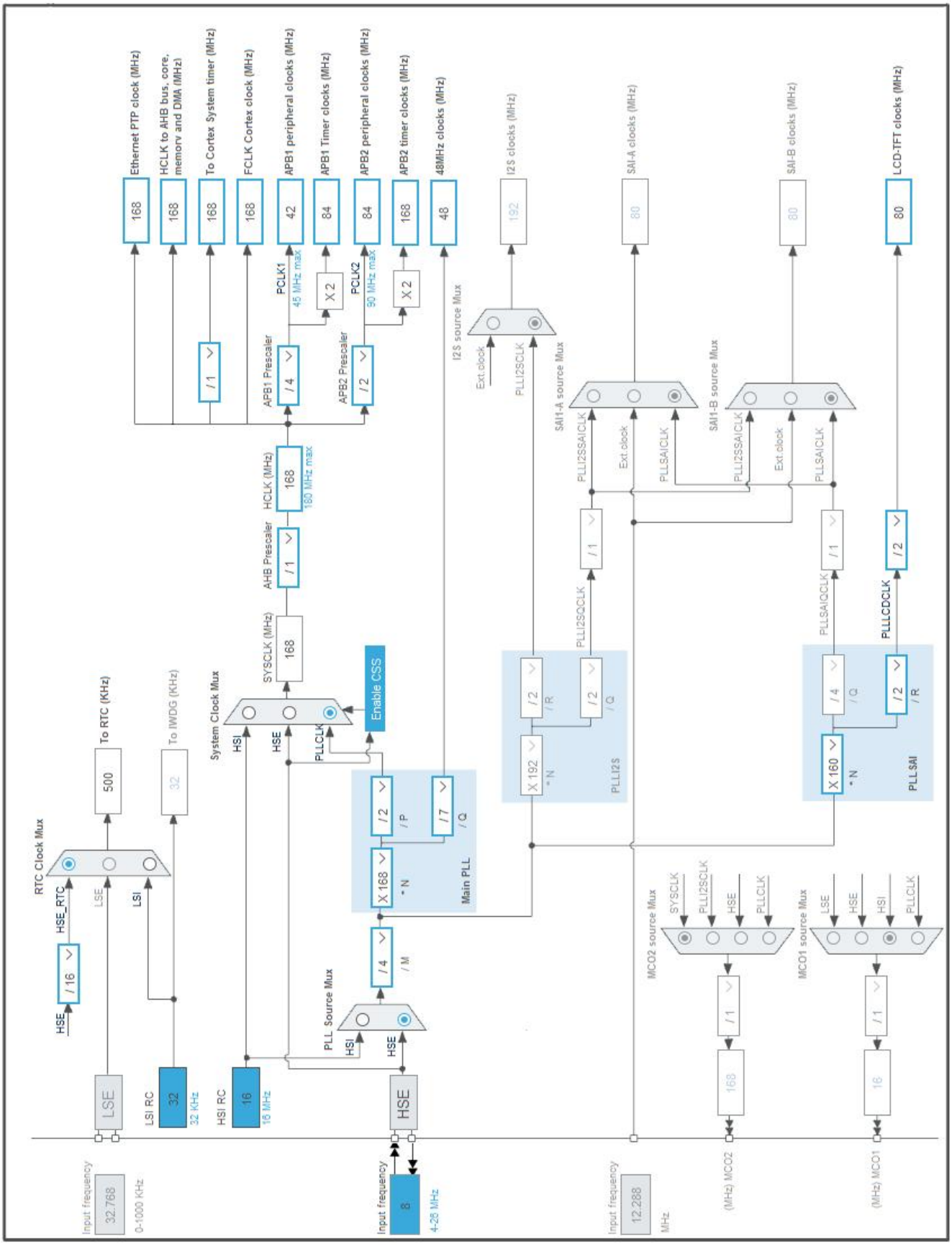
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
35	PA1	I/O		
36	PA2	I/O		
37	PA3	I/O	LTDC_B5	B5
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	LTDC_VSYNC	VSYNC
41	PA5 *	I/O	GPIO_Output	LED3
42	PA6	I/O	LTDC_G2	G2
43	PA7 *	I/O	GPIO_Output	LED4
46	PB0	I/O	LTDC_R3	R3
47	PB1	I/O	LTDC_R6	R6
48	PB2/BOOT1 *	I/O	GPIO_Input	BOOT1
49	PF11	I/O	FMC_SDNRAS	SDNRAS
50	PF12	I/O	FMC_A6	A6
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	FMC_A7	A7
54	PF14	I/O	FMC_A8	A8
55	PF15	I/O	FMC_A9	A9
56	PG0	I/O	FMC_A10	A10
57	PG1	I/O	FMC_A11	A11
58	PE7	I/O	FMC_D4	D4
59	PE8	I/O	FMC_D5	D5
60	PE9	I/O	FMC_D6	D6
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FMC_D7	D7
64	PE11	I/O	FMC_D8	D8
65	PE12	I/O	FMC_D9	D9
66	PE13	I/O	FMC_D10	D10
67	PE14	I/O	FMC_D11	D11
68	PE15	I/O	FMC_D12	D12
69	PB10	I/O	LTDC_G4	G4
70	PB11	I/O	LTDC_G5	G5
71	VCAP_1	Power		
72	VDD	Power		
77	PD8	I/O	FMC_D13	D13
78	PD9	I/O	FMC_D14	D14
79	PD10	I/O	FMC_D15	D15

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
80	PD11	I/O		
81	PD12 *	I/O	GPIO_Output	LED6
82	PD13 *	I/O	GPIO_Output	LED5
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FMC_D0	D0
86	PD15	I/O	FMC_D1	D1
87	PG2 *	I/O	GPIO_Input	PB5
88	PG3 *	I/O	GPIO_Output	LED7
89	PG4	I/O	FMC_BA0	BA0
90	PG5	I/O	FMC_BA1	BA1
91	PG6	I/O	LTDC_R7	R7
92	PG7	I/O	LTDC_CLK	DOTCLK [LCT-RGB_DOTCLK]
93	PG8	I/O	FMC_SDCLK	SDCLK
94	VSS	Power		
95	VDD	Power		
96	PC6	I/O	LTDC_HSYNC	HSYNC
97	PC7	I/O	LTDC_G6	G6
98	PC8	I/O	SDIO_D0	
99	PC9	I/O	SDIO_D1	
100	PA8	I/O		
101	PA9	I/O	USART1_TX	STLINK_RX [STM32F103CBT6_PA3]
102	PA10	I/O	USART1_RX	STLINK_TX [STM32F103CBT6_PA2]
103	PA11	I/O	LTDC_R4	R4
104	PA12	I/O	LTDC_R5	R5
105	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	SWCLK
110	PA15	I/O		
111	PC10	I/O	SDIO_D2	
112	PC11	I/O	SDIO_D3	
113	PC12	I/O	SDIO_CK	
114	PD0	I/O	FMC_D2	D2
115	PD1	I/O	FMC_D3	D3
116	PD2	I/O	SDIO_CMD	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
117	PD3	I/O	LTDC_G7	G7
118	PD4 *	I/O	GPIO_Input	WRITE_PROTECT
119	PD5 *	I/O	GPIO_Input	CARD_DETECT
120	VSS	Power		
121	VDD	Power		
122	PD6	I/O	SPI3_MOSI	NRF24L01P_MOSI
123	PD7	I/O	GPIO_EXTI7	NRF24L01P_IRQ
124	PG9 *	I/O	GPIO_Output	NRF24L01P_CE
125	PG10	I/O	LTDC_G3	G3
126	PG11	I/O	LTDC_B3	B3
127	PG12	I/O	LTDC_B4	B4
128	PG13 *	I/O	GPIO_Output	LD3 [Green Led]
129	PG14 *	I/O	GPIO_Output	LD4 [Red Led]
130	VSS	Power		
131	VDD	Power		
132	PG15	I/O	FMC_SDNCAS	SDNCAS
133	PB3	I/O	SPI3_SCK	NRF24L01P_SCK
134	PB4	I/O	SPI3_MISO	NRF24L01P_MISO
135	PB5	I/O	FMC_SDCKE1	SDCKE1
136	PB6	I/O	FMC_SDNE1	SDNE1 [SDRAM_CS]
137	PB7 *	I/O	GPIO_Output	NRF24L01P_CS
138	BOOT0	Boot		
139	PB8	I/O	LTDC_B6	B6
140	PB9	I/O	LTDC_B7	B7
141	PE0	I/O	FMC_NBL0	NBL0 [SDRAM_LDQM]
142	PE1	I/O	FMC_NBL1	NBL1 [SDRAM_UDQM]
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	stm429_oberon_station
Project Folder	K:\projets\STM32\STMicroelectronics\stm429_oberon_station
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.27.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x0
Minimum Stack Size	0x1000

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_FMC_Init	FMC
5	MX_LTDC_Init	LTDC
6	MX_USART1_UART_Init	USART1
7	MX_SDIO_SD_Init	SDIO
8	MX_SPI3_Init	SPI3
9	MX_CRC_Init	CRC
10	MX_RTC_Init	RTC

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F429ZITx
Datasheet	DS9405_Rev9

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

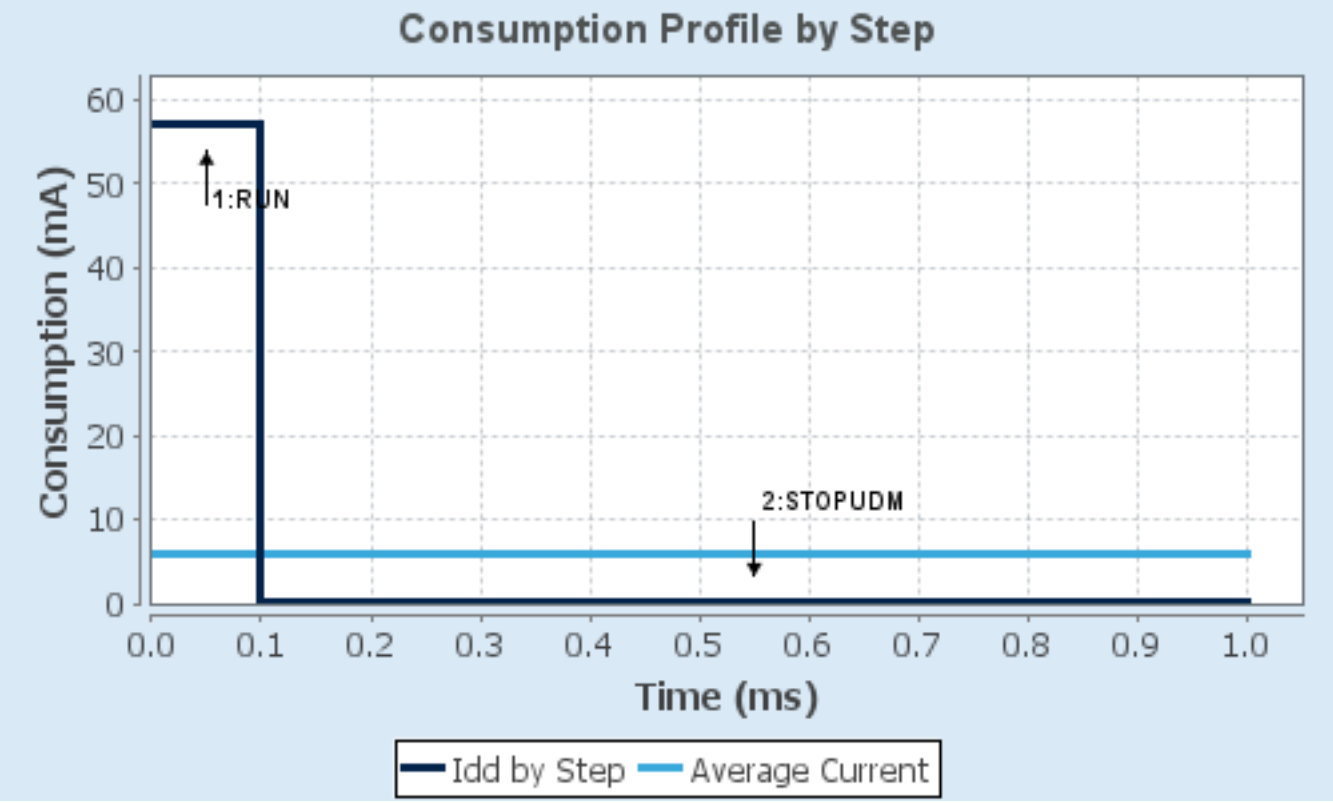
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	57 mA	100 µA
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	97.48	104.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	5.79 mA
Battery Life	24 days, 10 hours	Average DMIPS	225.0 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
60
50
40
30
20
10
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Peripherals and Middlewares Configuration

2.1. CRC

mode: Activated

2.2. FMC

SDRAM 1

Clock and chip enable: SDCKE1+SDNE1

Internal bank number: 4 banks

Address: 12 bits

Data: 16 bits

Byte enable: set

2.2.1. SDRAM 1:

SDRAM control:	
Bank	SDRAM bank 2
Number of column address bits	8 bits
Number of row address bits	12 bits
CAS latency	**3 memory clock cycles ***
Write protection	Disabled
SDRAM common clock	**2 HCLK clock cycles ***
SDRAM common burst read	**Enabled ***
SDRAM common read pipe delay	**1 HCLK clock cycle ***
SDRAM timing in memory clock cycles:	
Load mode register to active delay	**2 ***
Exit self-refresh delay	**7 ***
Self-refresh time	**4 ***
SDRAM common row cycle delay	**7 ***
Write recovery time	**3 ***
SDRAM common row precharge delay	**2 ***
Row to column delay	**2 ***

2.3. LTDC

Display Type: RGB565 (16 bits)

2.3.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	**144 ***
Horizontal Back Porch	**213 ***
Active Width	**1366 ***
Horizontal Front Porch	**70 ***
HSync Width	143
Accumulated Horizontal Back Porch Width	356
Accumulated Active Width	1722
Total Width	1792

Synchronization for Height:

Vertical Synchronization Height	4
Vertical Back Porch	**24 ***
Active Height	**768 ***
Vertical Front Porch	**3 ***
VSync Height	3
Accumulated Vertical Back Porch Height	27
Accumulated Active Height	795
Total Height	798

Signal Polarity:

Horizontal Synchronization Polarity	**Active High ***
Vertical Synchronization Polarity	**Active High ***
Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

Layer Default Color:

Red	0
Green	0
Blue	0

2.3.2. Layer Settings:

Layer Default Color:

Layer 0 - Alpha	0
Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	**1366 ***

Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	**768 ***

Pixel Parameters:

Layer 0 - Pixel Format	**L8 ***

Blending:

Layer 0 - Alpha constant for blending	**255 ***
Layer 0 - Blending Factor1	**Alpha constant x Pixel Alpha ***
Layer 0 - Blending Factor2	**Alpha constant x Pixel Alpha ***

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	**0xD0000000 ***
Layer 0 - Color Frame Buffer Line Length (Image Width)	**1366 ***
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	**768 ***

Number of Layers:

Number of Layers	**1 layer ***

2.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

2.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	**3 ***
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Disabled

2.5. RTC

mode: Activate Clock Source

mode: Activate Calendar

2.5.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	**124 ***
Synchronous Predivider value	**3999 ***

Calendar Time:

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	**Daylightsaving Add1h ***
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	0

2.6. SDIO

Mode: SD 4 bits Wide bus

2.6.1. Parameter Settings:

SDIO parameters:

Clock transition on which the bit capture is made	Rising transition
SDIO Clock divider bypass	Disable
SDIO Clock output enable when the bus is idle	Disable the power save for the clock
SDIO hardware flow control	The hardware control flow is disabled
SDIOCLK clock divide factor	0

2.7. SPI3

Mode: Full-Duplex Master

2.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**5.25 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

2.8. SYS

Debug: Serial Wire

Timebase Source: SysTick

2.9. USART1

Mode: Asynchronous

2.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	A0
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	A1
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	A2
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	A3
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	A4
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	A5
	PC0	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDNWE
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDNRAS
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	A6
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	A7
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	A8
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	A9
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	A10
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	A11
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D4
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D5
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D6
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D7
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D8
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D9
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D10
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D11
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D12
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D13
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D14
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D15
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D0
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D1
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	BA0
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	BA1
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDCLK
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D2
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D3
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDNCAS
	PB5	FMC_SDCKE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDCKE1
	PB6	FMC_SDNE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDNE1 [SDRAM_CS]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	NBL0 [SDRAM_LDQM]
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	NBL1 [SDRAM_UDQM]
LTDC	PF10	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENABLE [LCD-RGB_ENABLE]
	PA3	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	B5
	PA4	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	VSYNC
	PA6	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	G2
	PB0	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	R3
	PB1	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	R6
	PB10	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	G4
	PB11	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	G5
	PG6	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	R7
	PG7	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	DOTCLK [LCT-RGB_DOTCLK]
	PC6	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	HSYNC
	PC7	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	G6
	PA11	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	R4
	PA12	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	R5
	PD3	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	G7
	PG10	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	G3
	PG11	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	B3
	PG12	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	B4
	PB8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	B6

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB9	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	B7
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	PH0-OSC_IN
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	PH1-OSC_OUT
SDIO	PC8	SDIO_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDIO_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDIO_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDIO_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDIO_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDIO_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI3	PD6	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	NRF24L01P_MOSI
	PB3	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	NRF24L01P_SCK
	PB4	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	NRF24L01P_MISO
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	STLINK_RX [STM32F103CBT6_PA3]
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	STLINK_TX [STM32F103CBT6_PA2]
GPIO	PE2	GPIO_EXTI2	**External Interrupt Mode with Rising/Falling edge**	No pull-up and no pull-down	n/a	PS2_CLOCK_1
	PE3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PS2_DATA_1
	PE4	GPIO_EXTI4	**External Interrupt Mode with Rising/Falling edge**	No pull-up and no pull-down	n/a	PS2_CLOCK_2
	PE5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PS2_DATA_2
	PE6	GPIO_Input	Input mode	**Pull-up ***	n/a	PB3
	PC13	GPIO_Input	Input mode	**Pull-up ***	n/a	PB4
	PC14/OSC32_IN	GPIO_EXTI14	**External Interrupt Mode with Falling edge trigger detection**	**Pull-up ***	n/a	PB1
	PC15/OSC32_OUT	GPIO_Input	Input mode	**Pull-up ***	n/a	PB2
	PF6	GPIO_Input	Input mode	**Pull-up ***	n/a	PB6
	PF7	GPIO_Input	Input mode		n/a	PB8

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
				Pull-up *		
	PF8	GPIO_Input	Input mode	**Pull-up ***	n/a	PB7
	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NCS_MEMS_SPI [L3GD20_CS_I2C/SPI]
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CSX [LCD-RGB_CSX]
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PA0/WKUP	GPIO_EXTI0	**External Event Mode with Rising edge trigger detection ***	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED3
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED4
	PB2/BOOT1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BOOT1
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED6
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED5
	PG2	GPIO_Input	Input mode	**Pull-up ***	n/a	PB5
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED7
	PD4	GPIO_Input	Input mode	**Pull-up ***	n/a	WRITE_PROTECT
	PD5	GPIO_Input	Input mode	**Pull-up ***	n/a	CARD_DETECT
	PD7	GPIO_EXTI7	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	NRF24L01P_IRQ
	PG9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NRF24L01P_CE
	PG13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Green Led]
	PG14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD4 [Red Led]
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NRF24L01P_CS

3.2. DMA configuration

DMA request	Stream	Direction	Priority
MEMTOMEM	DMA2_Stream0	Memory To Memory	Low
SDIO_RX	DMA2_Stream3	Peripheral To Memory	Low
SDIO_TX	DMA2_Stream6	Memory To Peripheral	Low

MEMTOMEM: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Src Memory Increment:	**Enable ***
Dst Memormy Increment:	**Enable ***
Src Memory Data Width:	**Word ***
Dst Memormy Data Width:	**Word ***
Src Memory Burst Size:	Single
Dst Memormy Burst Size:	Single

SDIO_RX: DMA2_Stream3 DMA request Settings:

Mode:	**Peripheral Flow Control ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	Word
Peripheral Burst Size:	**4 Increment ***
Memory Burst Size:	4 Increment

SDIO_TX: DMA2_Stream6 DMA request Settings:

Mode:	**Peripheral Flow Control ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***

Peripheral Data Width:	**Word ***
Memory Data Width:	Word
Peripheral Burst Size:	**4 Increment ***
Memory Burst Size:	4 Increment

3.3. NVIC configuration

3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	1	0
Undefined instruction or illegal state	true	1	0
System service call via SWI instruction	true	15	0
Debug monitor	true	1	0
Pendable request for system service	true	15	0
System tick timer	true	10	0
EXTI line2 interrupt	true	0	0
EXTI line4 interrupt	true	0	0
EXTI line[9:5] interrupts	true	0	0
EXTI line[15:10] interrupts	true	0	0
SDIO global interrupt	true	0	0
DMA2 stream0 global interrupt	true	1	0
DMA2 stream3 global interrupt	true	1	0
DMA2 stream6 global interrupt	true	1	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USART1 global interrupt	unused		
FMC global interrupt	unused		
SPI3 global interrupt	unused		
FPU global interrupt	unused		
LTDC global interrupt	unused		
LTDC global error interrupt	unused		

3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	false	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false

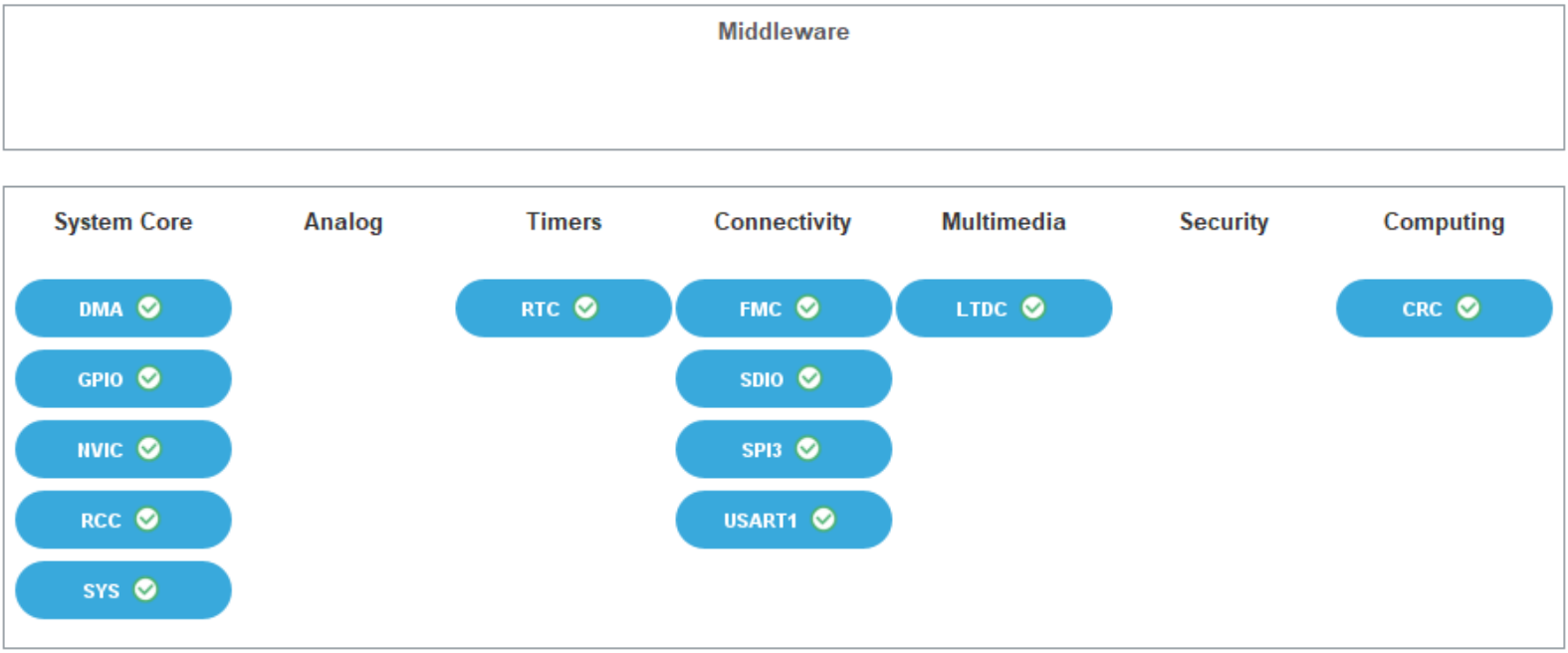
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line2 interrupt	false	true	true
EXTI line4 interrupt	false	true	true
EXTI line[9:5] interrupts	false	true	true
EXTI line[15:10] interrupts	false	true	true
SDIO global interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true
DMA2 stream3 global interrupt	false	true	true
DMA2 stream6 global interrupt	false	true	true

*** User modified value**

4. System Views

4.1. Category view

4.1.1. Current



5. Docs & Resources

Type	Link