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> PROCESSOR SYSTEM DESIGN AND.



diverger (/s/profile/0052E00000N3LrvQAF) (Member) asked a question.

June 1, 2019 at 7:59 AM (/s/question/0D52E00006hpmj5SAA/1gbps-wont-achieved-on-board-based-on-zynq-7020)

## 1Gbps won't achieved on board based on Zynq 7020

I designed a board with Zynq 7020 and Marvell's 88E1512. I try to run the echo standalone Lwip example, but the speed always autonegotiated at 100Mbps:

Start PHY autonegotiation

Waiting for PHY to complete autonegotiation.

autonegotiation complete

link speed for phy address 0: 100

I expected it will work at 1000bps. I wonder if I missed something in the Vivado or SDK configurations. Any suggestion?

PROCESSOR SYSTEM DESIGN AND AXI (/S/TOPIC/0TO2E000000YKXZWA4/)

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stephenm (/s/profile/0052E00000N2nOZQAZ) (AMD)

Edited by wcassell May 29, 2022 at 3:17 PM

\*\*BEST SOLUTION\*\*

I created a wiki to read the phy registers over jtag. You may need to change the script to suit your setup. The script assumes you are using gem3 on zynq ultrascale.

https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/69271643/PHY+Register+dump+over+JTAG (https://xilinx-

wiki.atlassian.net/wiki/spaces/A/pages/69271643/PHY+Register+dump+over+JTAG)

Admin Note - This thread was edited to update links as a result of our community migration. The original post date was 2019-06-02.

Selected as Best Like

All Answers

stephenm (/s/profile/0052E00000N2nOZQAZ) (AMD)

6 years ago

Can you check the GEM clocking in vivado is set to 1000M

Like Reply 1 like

drjohnsmith (/s/profile/0052E00000N2no4QAB) (Member)

6 years ago

Something that has caught us out once,

if the cable does not have all 4 pairs correct,

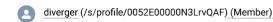
the Ethernet drops back to 100,

Like Reply

diverger (/s/profile/0052E00000N3LrvQAF) (Member)

Yes, the cable is a standard cable with all 8 wires connected. And it's only about 2 meters long.

Like Reply



Ummm, I checked it, the clock settings in the Vivado's PS configuration wizard is as below:

Component	Clock Source	Requested Frequ	Actual Frequency(	Range(MHz)
<ul> <li>Processor/Memory C</li> </ul>	locks			
CPU	ARM PLL 🗸	767	766.666687	50.0 : 767.0
DDR	DDR PLL 🗸	533.333333 🛞	533.333374	200.000000 : 534.000
V IO Peripheral Clocks				
SMC	IO PLL	100	10.000000	10.000000 : 100.000000
QSPI	IO PLL 🗸	200 🚳	200.000000	10.000000 : 200.000000
ENET0	IO PLL V	1000 Mbps 🗸	125.000000	

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stephenm (/s/profile/0052E00000N2nOZQAZ) (AMD)

6 years ago

Looks fine. How about your host settings. Is this set to auto neg, or 1000?

Like Reply

ericv (/s/profile/0052E00000N39QqQAJ) (Member)

Edited by User1632152476299482873 September 25, 2021 at 3:32 PM

@stephenm (https://support.xilinx.com/s/profile/0052E00000N2nOZQAZ)

Most PHYs provide access to the rate/duplexing involved during auto-negotiation. It may help checking what the local PHY and other end report. The local PHY has likely a register with the other end reported capabilities.

Like Reply

diverger (/s/profile/0052E00000N3LrvQAF) (Member)

6 years ago

I've tried connect the host side of the cable to a gigabytes switch and a laptop. I think their default settings should be auto neg enabled. Because my developing machine connect to the same switch, and the link status shows 1Gbps.

BTW, the upstream of the Ethernet switch is only 100Mbps, I don't think it will affect the neg of the downstream port connection's speed negotiations, right?

stephenm (/s/profile/0052E00000N2nOZQAZ) (AMD)

Edited by wcassell May 29, 2022 at 3:17 PM

\*\*BEST SOLUTION\*\*

I created a wiki to read the phy registers over itag. You may need to change the script to suit your setup. The script assumes you are using gem3 on zyng ultrascale.

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Selected as Best Like Reply

diverger (/s/profile/0052E00000N3LrvQAF) (Member)

6 years ago

I finally solve the problem. I rechecked the entire design from code to PCB. And found that I've overlooked the PoE part (my design is ethernet with PoE), after I removing the connections relative to PoE, it can work at 1000Mbps. So, I think I need redesign the PCB now.

Thanks for all your suggestions/help.

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