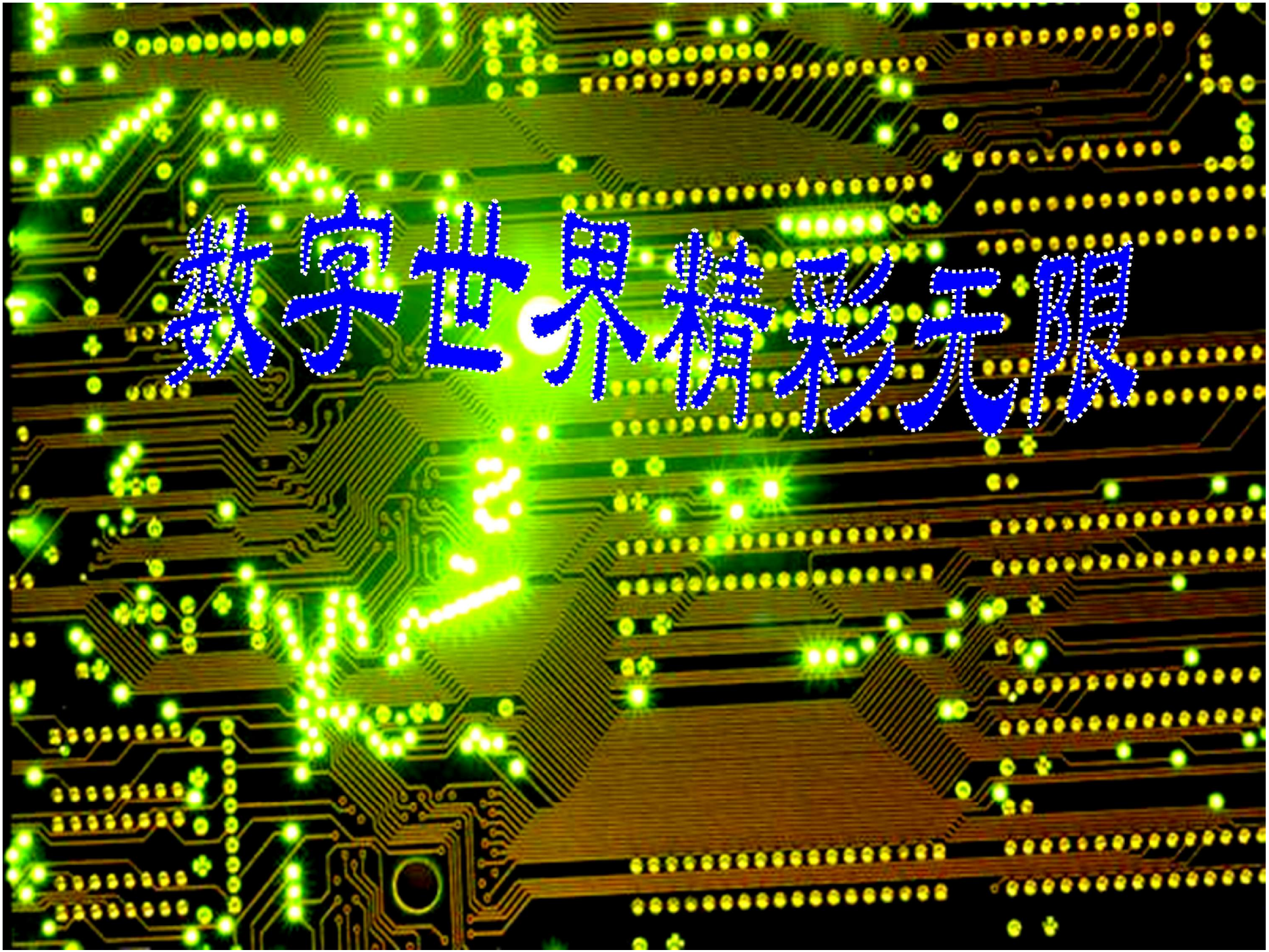
数字世界精彩无限

数字逻辑设计

Digital Logic Design

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Unit 5 Multi-Level Gate Circuits NAND and NOR Gates

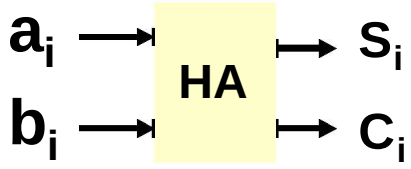
- **多级门电路（Multi-Level Circuits）**
- **两级门电路的设计**
- **多输出电路的设计**
- **Some Examples （半加器等）**

Some Examples

Example 5

半加器（Half adder）

功能：对两个1位二进制数执行相加运算

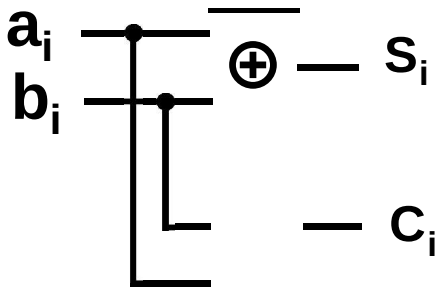


$$S_i = a_i \oplus b_i$$

$$C_i = a_i b_i$$

真值表

a_i	b_i	S_i	C_i
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

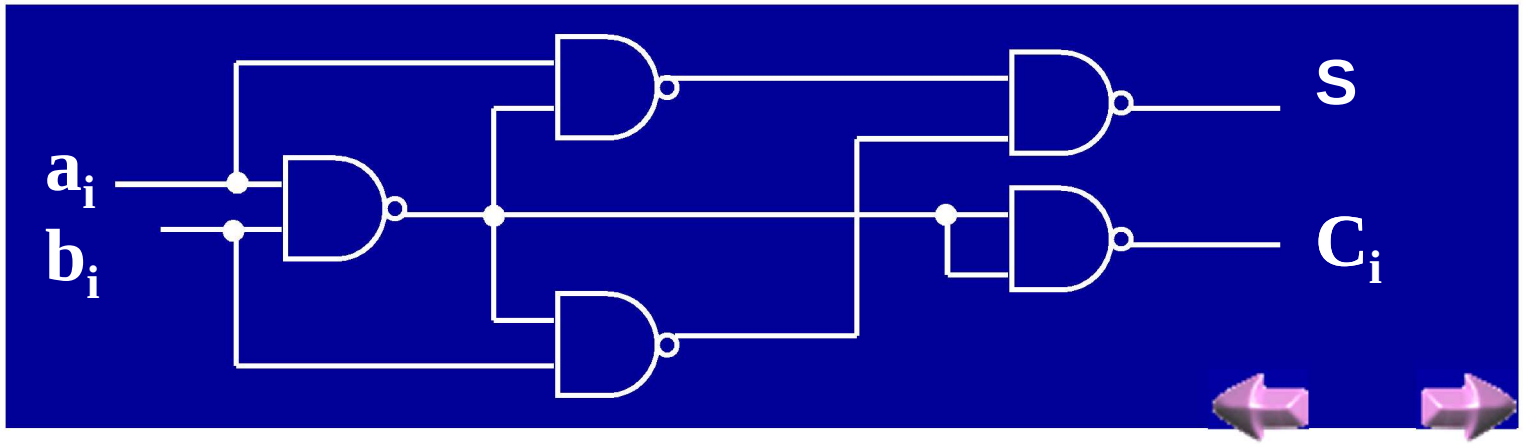


Example 5

Some Examples

利用单一逻辑门与非门实现半加器

$$
\begin{cases}
S_i = \overline{a}_i b_i + a_i \overline{b}_i = \overline{a}_i b_i + a_i \overline{b}_i + a_i \overline{a}_i + b_i \overline{b}_i \\
\quad = a_i (\overline{a}_i + \overline{b}_i) + b_i (\overline{a}_i + \overline{b}_i) = a_i \overline{a_i b_i} + b_i \overline{a_i b_i} \\
\quad = \overline{a_i \overline{a_i b_i} \; b_i \overline{a_i b_i}} \\
C_i = \overline{a_i b_i}
\end{cases}
$$



Some Examples

Example 6

全加器（Full adder）

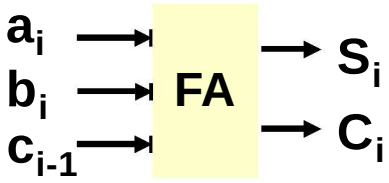
$$
\begin{array}{rl}
 & 1\ 0\ 1\ 1 \ldots\ldots\ldots\ A \\
 & 1\ 1\ 1\ 0 \ldots\ldots\ldots\ B \\
+ & 1\ 1\ 0\ 0 \ldots\ldots\ldots\ C_{i-1} \\
\hline
 & 1\ 1\ 0\ 0\ 1 \ldots\ldots\ldots\ S_i
\end{array}
$$

$A = a_3\, a_2\, a_1\, a_0 = 1011$

$B = b_3\, b_2\, b_1\, b_0 = 1110$

Some Examples

Example 6



a_i	b_i	C_{i-1}	S_i	C_i
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

S_i

a_i \ $b_i c_{i-1}$	00	01	11	10
0	0	1	0	1
1	1	0	1	0

C_i

a_i \ $b_i c_{i-1}$	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$$S_i = \bar{a}_i\bar{b}_i c_{i-1} + \bar{a}_i b_i \bar{c}_{i-1} + a_i \bar{b}_i \bar{c}_{i-1} + a_i b_i c_{i-1}$$
$$= (\bar{a}_i\bar{b}_i + a_i b_i)\, c_{i-1} + (\bar{a}_i b_i + a_i \bar{b}_i)\, \bar{c}_{i-1}$$
$$= \overline{(a_i \oplus b_i)}\, c_{i-1} + (a_i \oplus b_i)\, \bar{c}_{i-1}$$
$$= a_i \oplus b_i \oplus C_{i-1}$$

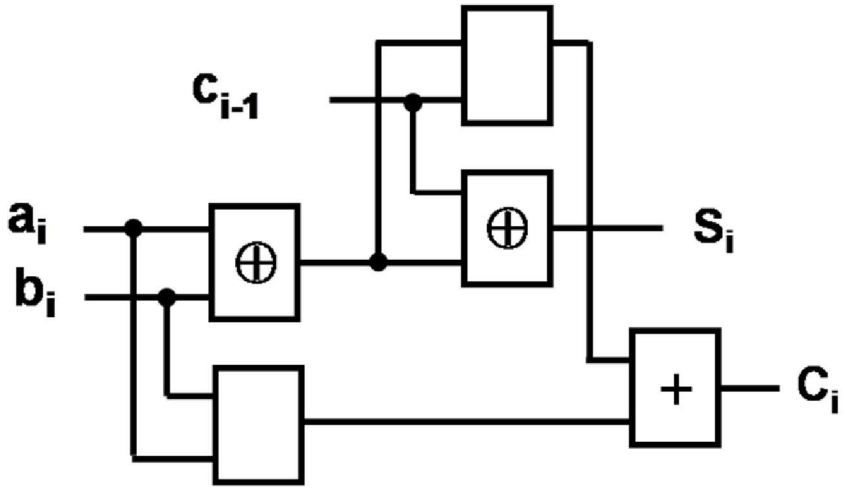
$$C_i = (a_i \oplus b_i)\, C_{i-1} + a_i b_i$$

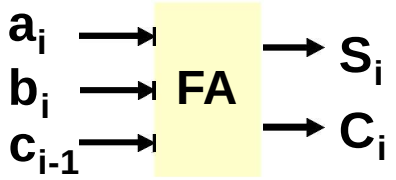
Some Examples

Example 6

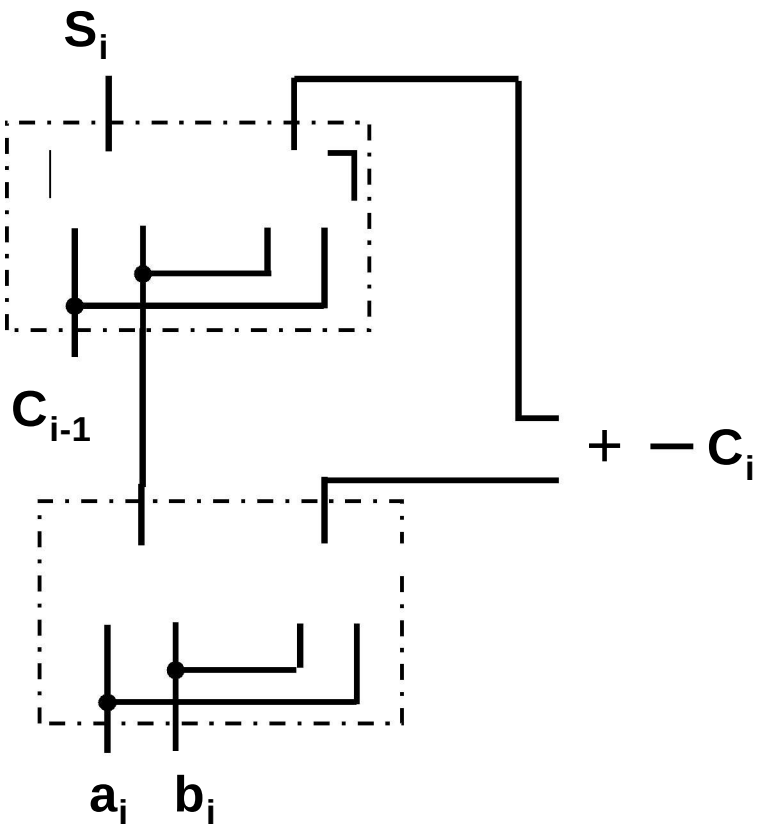
- **solution 1：**

$$\begin{cases} S_i = a_i \oplus b_i \oplus C_{i-1} \\ C_i = (a_i \oplus b_i)\, C_{i-1} + a_i b_i \end{cases}$$





Some Examples



♦ **solution 2：**

$$S_i = a_i \oplus b_i \oplus C_{i-1}$$

$$C_i=(a_i \oplus b_i)\, C_{i-1} + a_i b_i$$

$$\begin{cases} S_i = a_i \oplus b_i \\ C_i = a_i b_i \end{cases}$$

Some Examples

Example 6

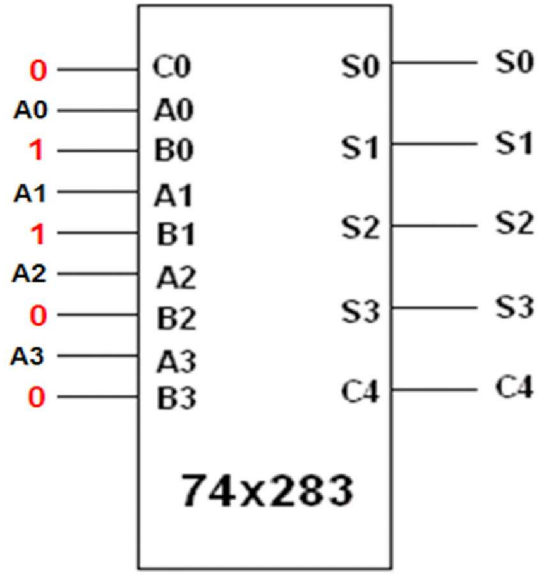
全加器（Full adder）

典型芯片

- **74LS82** ： 2-bit adder
- **74LS283** ： 4-bit adder

二进制数 $A_3\ A_2\ A_1\ A_0$	余三码 $S_3\ S_2\ S_1\ S_0$	二进制数 $A_3\ A_2\ A_1\ A_0$	余三码 $S_3\ S_2\ S_1\ S_0$
0 0 0 0	0 0 1 1	1 0 0 0	1 0 1 1
0 0 0 1	0 1 0 0	1 0 0 1	1 1 0 0
0 0 1 0	0 1 0 1	1 0 1 0	×
0 0 1 1	0 1 1 0	1 0 1 1	×
0 1 0 0	0 1 1 1	1 1 0 0	×
0 1 0 1	1 0 0 0	1 1 0 1	×
0 1 1 0	1 0 0 1	1 1 1 0	×
0 1 1 1	1 0 1 0	1 1 1 1	×

应用——余3码产生器



$A_3A_2A_1A_0$: 输入 8421 BCD码

$S_3S_2S_1S_0$: 输出余3 码

S = A+0011

Some Examples

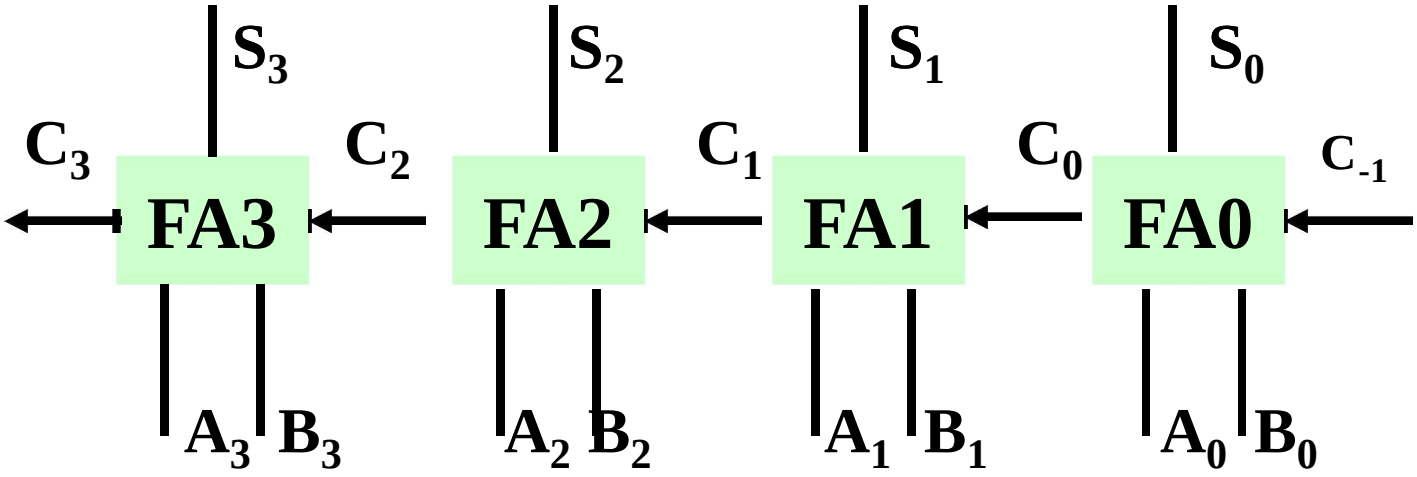
Example 7

4位并行加法器

$S_i = a_i \oplus b_i \oplus C_{i-1}$

$C_i=(a_i \oplus b_i)\, C_{i-1} + a_i b_i$

（1）串行进位



- 缺点：串行进位，运算速度慢
- 优点：线路简单
- 关键：进位形成时间
- 解决方案：改串行进位为并行进位

Some Examples

Example 7

（2） 超前进位

$A = A_3A_2A_1A_0 = 1011$

$B = B_3B_2B_1B_0 = 1110$

$C_i=(A_i \oplus B_i)\, C_{i-1} + A_iB_i$

$C_i=P_iC_{i-1} + G_i$

$P_i= A_i \oplus B_i$

$G_i= A_iB_i$

——进位迭代公式

$C_0= P_0C_{-1}+G_0$

$C_1= P_1C_0+G_1 = P_1P_0C_{-1}+P_1G_0+G_1$

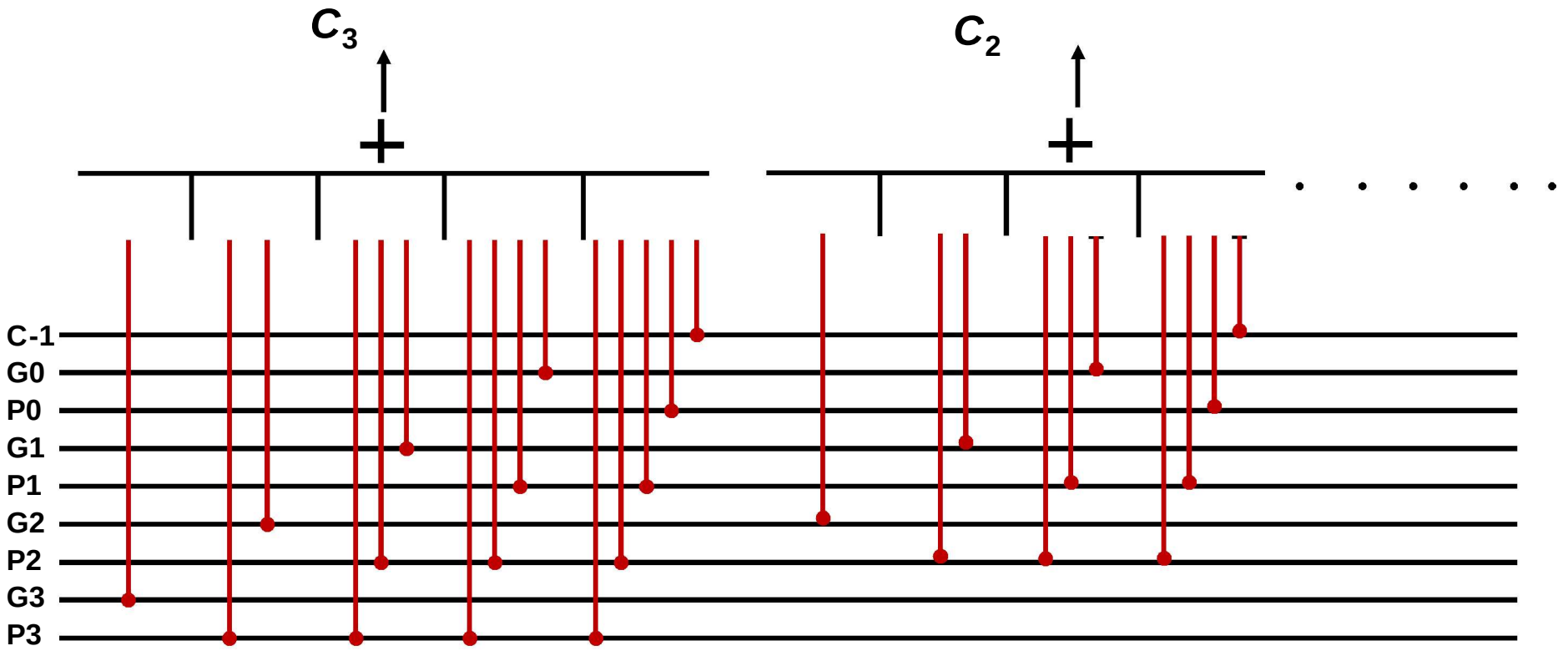
$C_2= P_2C_1+G_2 = P_2P_1P_0C_{-1}+P_2P_1G_0+P_2G_1+G_2$

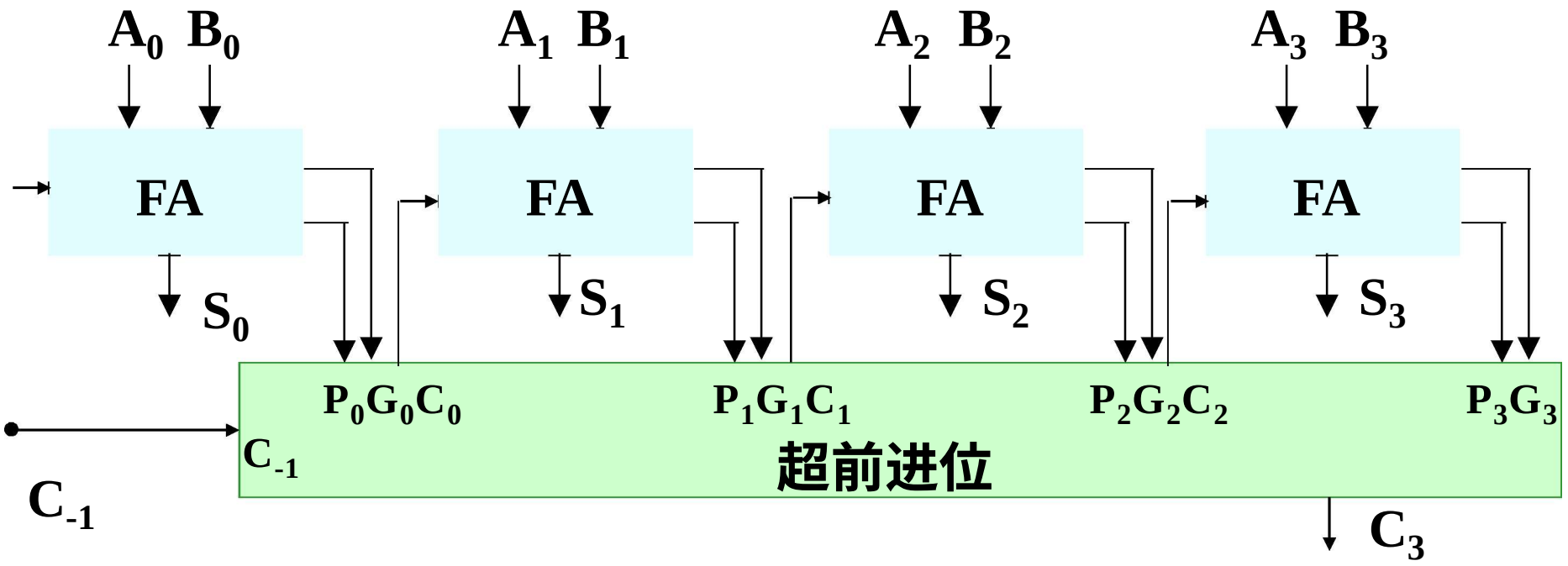
$C_3= P_3C_2+G_3 = P_3P_2P_1P_0C_{-1}+P_3P_2P_1G_0+P_3P_2G_1+P_3G_2+G_3$

Some Examples

Example 7

（2） 超前进位





$$P_i = A_i \oplus B_i \qquad G_i = A_i B_i$$

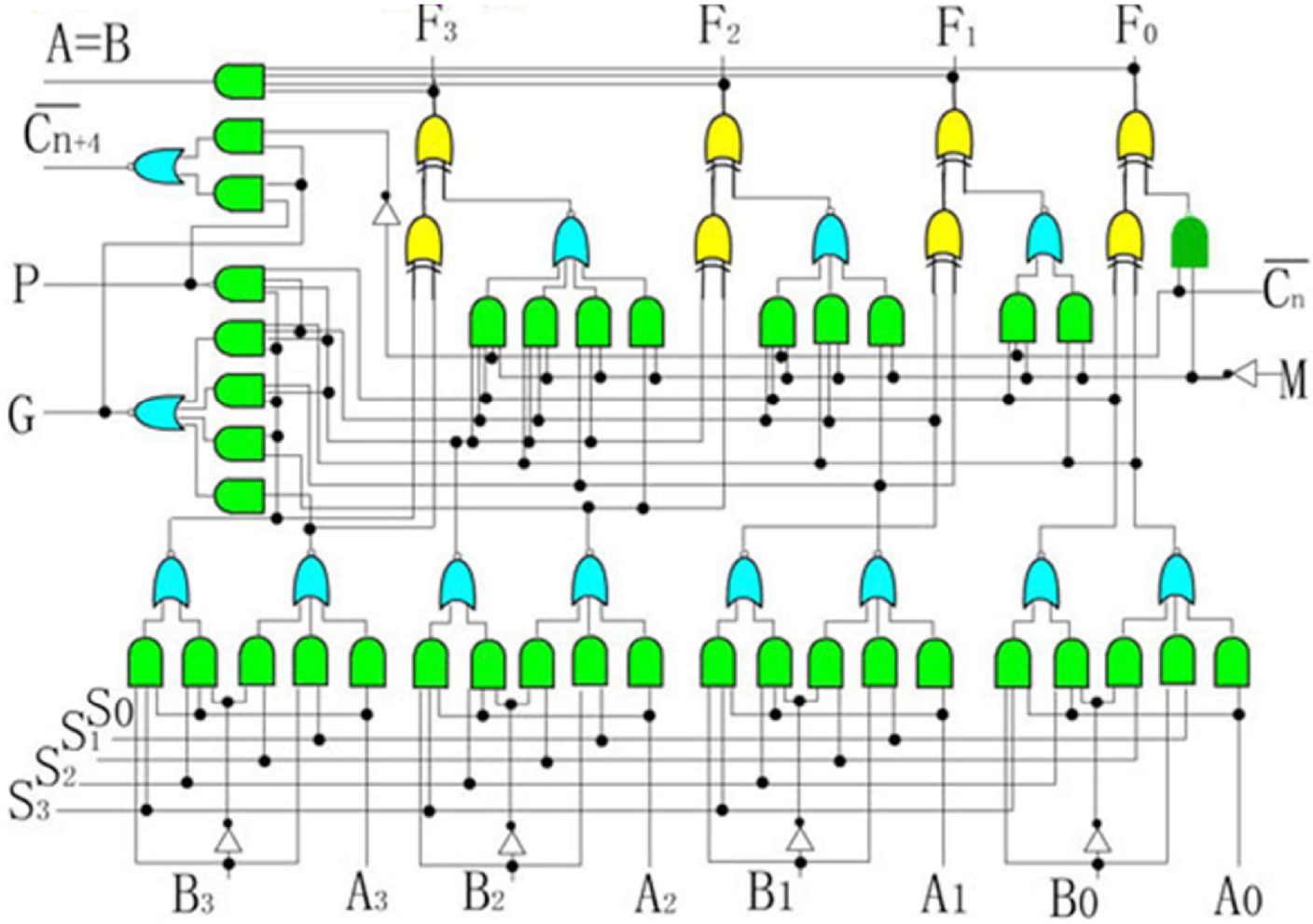
$$C_0 = P_0 C_{-1} + G_0$$

$$C_1 = P_1 C_0 + G_1 = P_1 P_0 C_{-1} + P_1 G_0 + G_1$$

$$C_2 = P_2 C_1 + G_2 = P_2 P_1 P_0 C_{-1} + P_2 P_1 G_0 + P_2 G_1 + G_2$$

$$C_3 = P_3 C_2 + G_3 = P_3 P_2 P_1 P_0 C_{-1} + P_3 P_2 P_1 G_0 + P_3 P_2 G_1 + P_3 G_2 + G_3$$

ALU



***M*=0 ， addition**

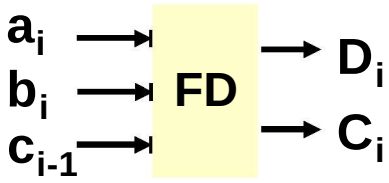
***M*=1 ， logic operation**

Some Examples

Example 8

全减器（Binary Full Subtracter）

$$
\begin{array}{rl}
 & 1\ 1\ 1\ 0 \quad \ldots\ldots\ldots\ A \\
 & 1\ 0\ 1\ 1 \quad \ldots\ldots\ldots\ B \\
- & 0\ 0\ 1\ 1\ 0 \quad \ldots\ldots\ldots\ldots C_{i-1} \\
\hline
 & 0\ 0\ 1\ 1 \quad \ldots\ldots\ldots\ D_i
\end{array}
$$



A= $a_3\ a_2\ a_1\ a_0$ =1110

B = $b_3\ b_2\ b_1\ b_0$=1011

真值表

a_i	b_i	C_{i-1}	D_i	C_i
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Some Examples

Example 8

真值表

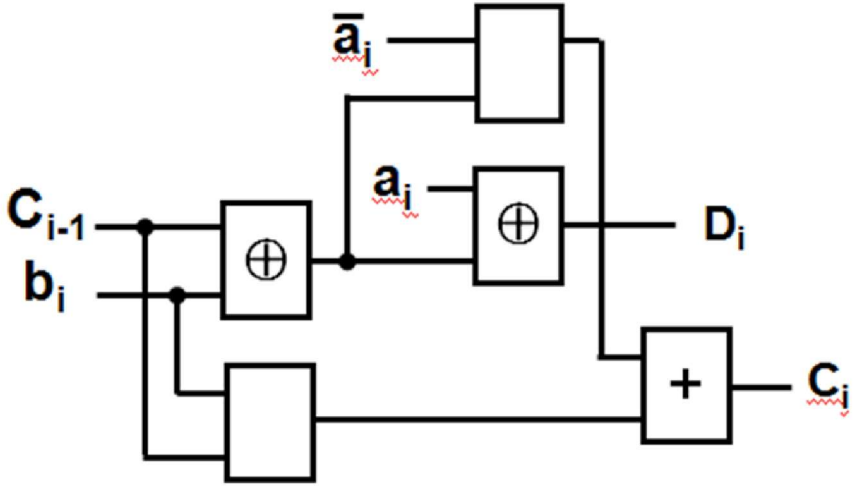
a_i	b_i	C_{i-1}	D_i	C_i
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

D_i

a_i \ b_iC_{i-1}	00	01	11	10
0	0	1	0	1
1	1	0	1	0

C_i

a_i \ b_iC_{i-1}	00	01	11	10
0	0	1	1	1
1	0	0	1	0



$$\begin{cases} D_i = a_i \oplus b_i \oplus C_{i-1} \\ C_i = (C_{i-1} \oplus b_i)\,\bar{a}_i + C_{i-1} b_i \end{cases}$$

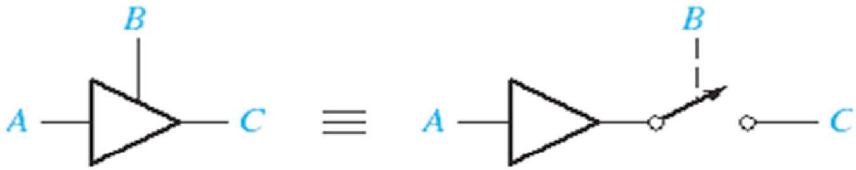
Some Examples

Example 9

三态门（Three-State Buffers）

三态——

- **0**
- **1**
- **Z: 高阻态**



三态门（恒等）

B：使能端，高电平有效

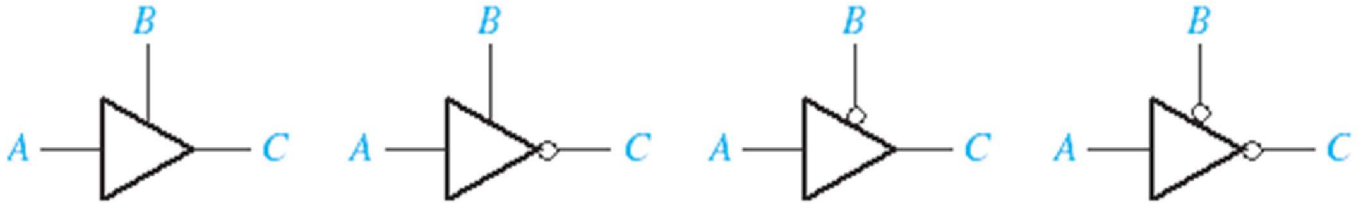
- **包括三态恒等门、三态非门、三态与非门等，商品名称为缓冲器（驱动门）。**
- **用途之一：可用来增强输出驱动能力**

真值表

B	A	C
0	0	Z
0	1	Z
1	0	0
1	1	1

Some Examples

三态门（Three-State Buffers）



B	A	C
0	0	Z
0	1	Z
1	0	0
1	1	1

(a)

B	A	C
0	0	Z
0	1	Z
1	0	1
1	1	0

(b)

B	A	C
0	0	0
0	1	1
1	0	Z
1	1	Z

(c)

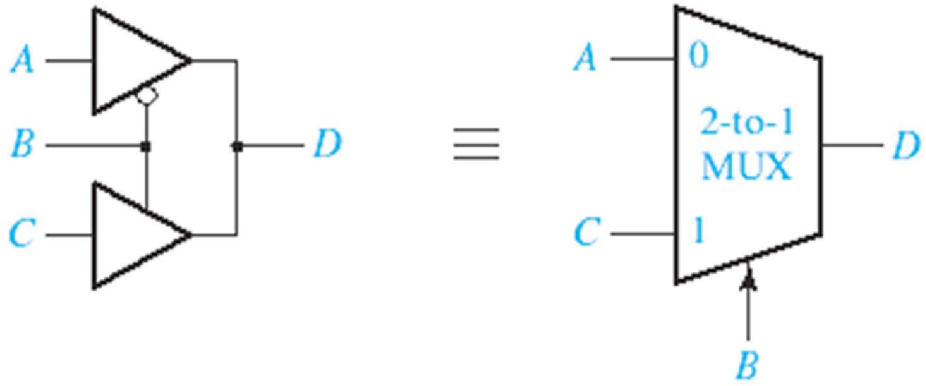
B	A	C
0	0	1
0	1	0
1	0	Z
1	1	Z

(d)

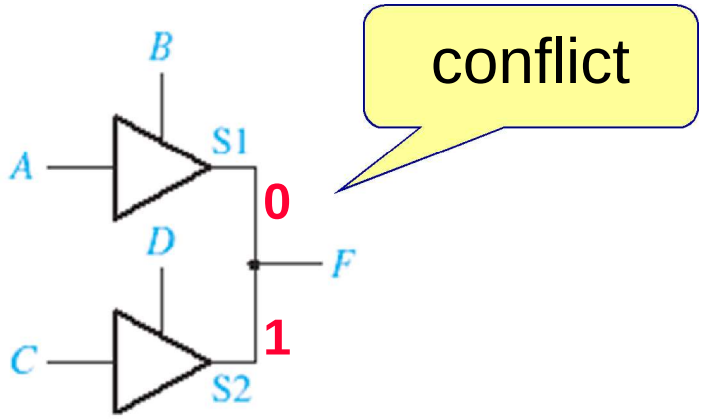
理解三态门——

- **高阻态：电阻很大，相当于开路**
- **高阻态相当于该门同与它连接的电路处于断开的状态。（实际电路中你不可能去断开它）**

Three-State Buffers



D=B'A+BC

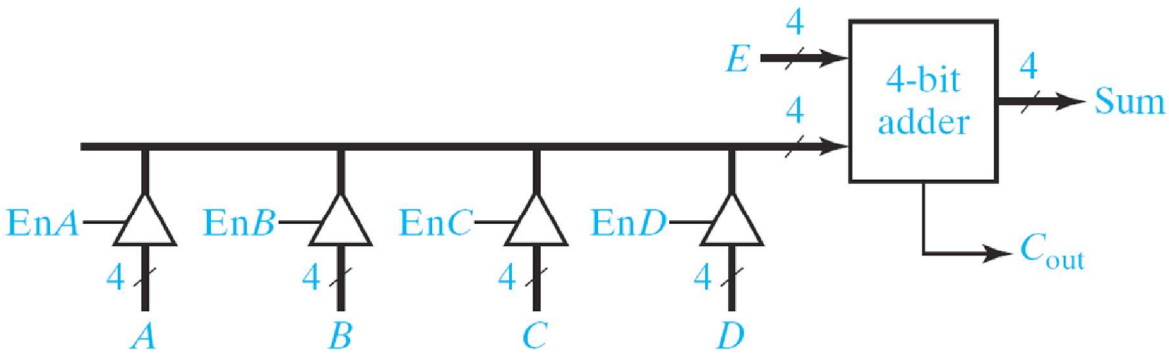


S_1 \ S_2	X	0	1	Z
X	X	X	X	X
0	X	0	X	0
1	X	X	1	1
Z	X	0	1	Z

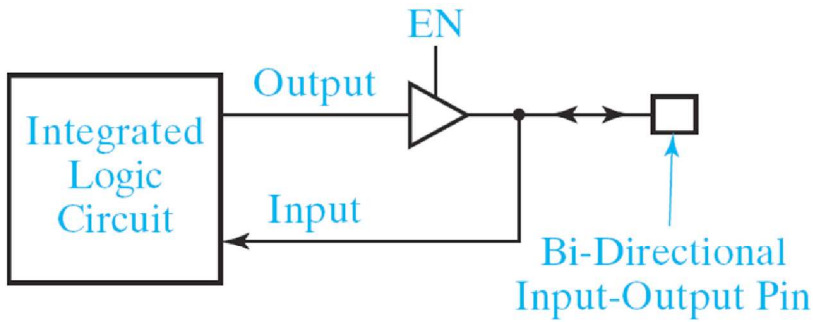
Three-State Buffers

应用

- 三态总线



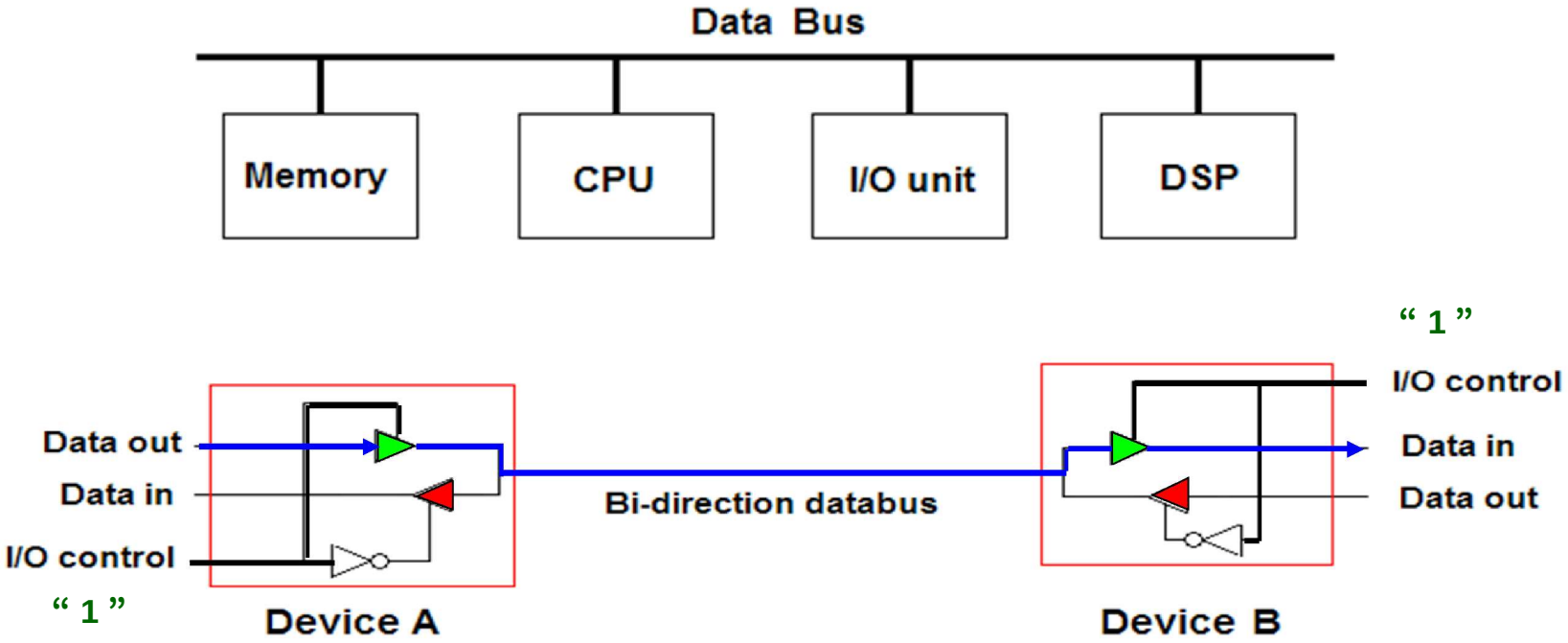
- 管脚输入输出可编程



Three-State Buffers

应用

- 双向数据总线



Three-State Buffers

理解三态门——

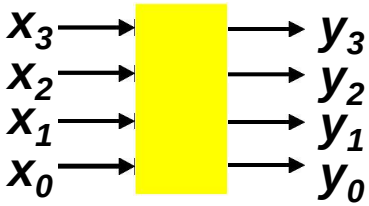
内存里的一个存储单元

- 读写控制线处于低电位时，可以写入；
- 读写控制线处于高电位时，可以读出
- 但是不读不写，就要用高阻态

Three-State Buffers

Example

$X=X_3X_2X_1X_0$为8421BCD码，设计一个MOD 5选择电路，要求选择那些能被5整除的数输出。



①真值表(F为控制信号)

X_3 X_2 X_1 X_0	F	X_3 X_2 X_1 X_0	F
0 0 0 0	1	1 0 0 0	0
0 0 0 1	0	1 0 0 1	0
0 0 1 0	0	1 0 1 0	×
0 0 1 1	0	1 0 1 1	×
0 1 0 0	0	1 1 0 0	×
0 1 0 1	1	1 1 0 1	×
0 1 1 0	0	1 1 1 0	×
0 1 1 1	0	1 1 1 1	×

Three-State Buffers

② 化简

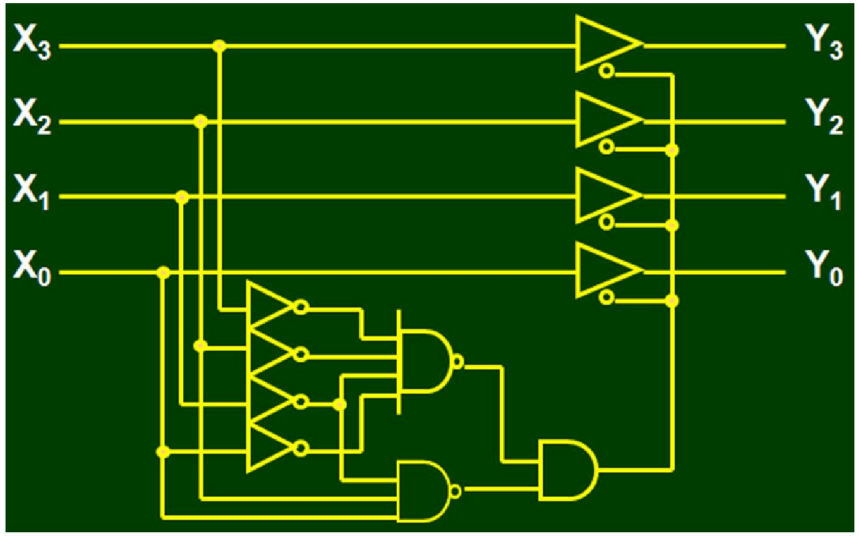
x_3x_2 \ x_1x_0	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	×	×	×	×
10	0	0	×	×

$$F=X_2\bar{X}_1X_0+\bar{X}_3\bar{X}_2\bar{X}_1\bar{X}_0$$

$$=\overline{(X_2\bar{X}_1X_0)}\ \overline{(\bar{X}_3\bar{X}_2\bar{X}_1\bar{X}_0)}$$

③ 逻辑图

$$\bar{F}=\overline{(X_2\bar{X}_1X_0)}\ \overline{(\bar{X}_3\bar{X}_2\bar{X}_1\bar{X}_0)}$$



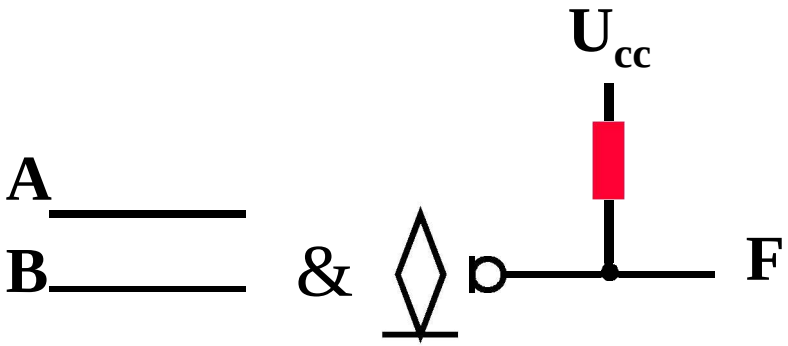
Example 10

Some Examples

OC门 (Open Collector Gate)

- 几个OC门的输出端可以直接互连
- 使用时必须加负载电阻

$$F = \overline{AB}$$

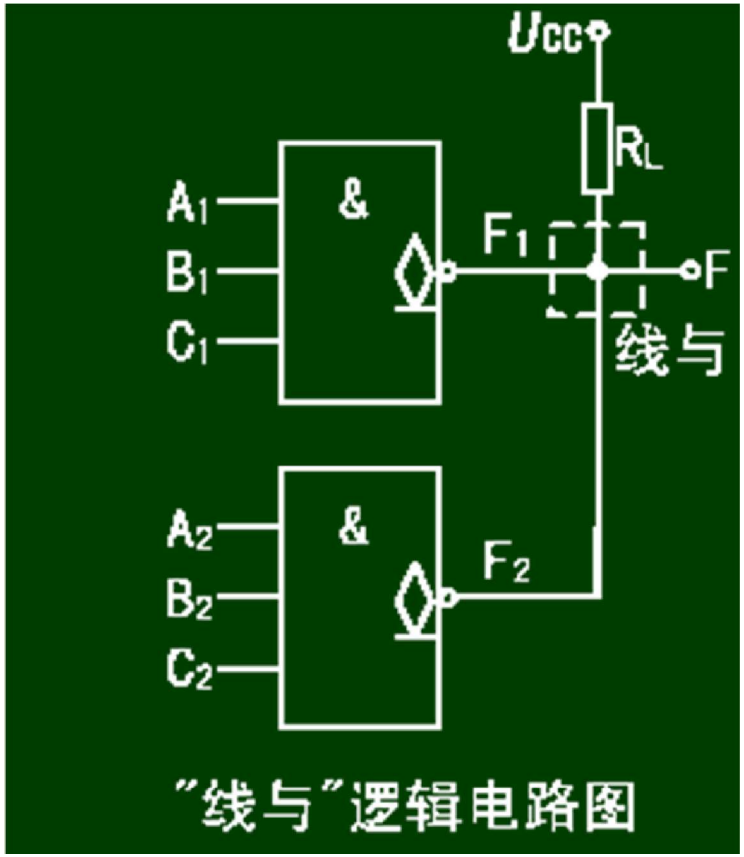


Some Examples

Example 11

OC门 (Open Collector Gate)

$$F=F_1 \cdot F_2=\overline{A_1B_1C_1} \cdot \overline{A_2B_2C_2}$$



Unit 5 Multi-Level Gate Circuits

- 多级门电路
- 两级门电路的设计
- 多输出电路的设计
- Some Examples