

数字世界精彩无限

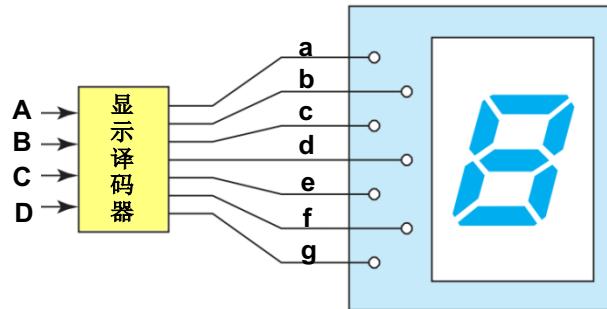
逻辑设计基础

Fundamentals of Logic Design

秦阳
School of Computer Science
csyqin@hit.edu.cn

3. 显示译码器

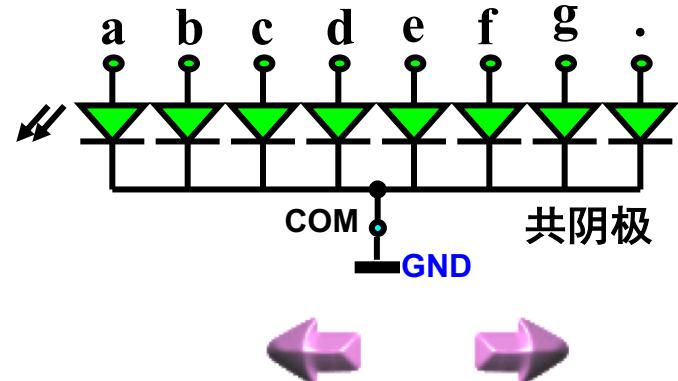
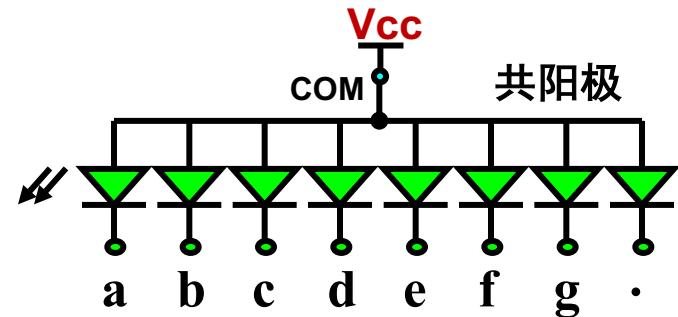
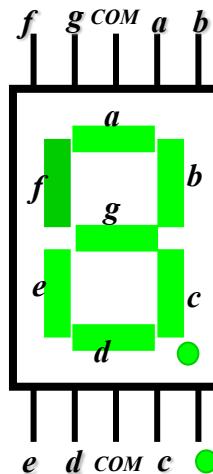
显示译码器：与显示器件（如数码管）配合，将输入代码转换为十进制码或特定编码，并在显示器件上显示相应的字形



8421BCD码驱动的共阴极七段
数码管显示译码器功能表

输入				译码输出							字形
A	B	C	D	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	0	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	0	1	1	1	1	1	6
0	1	1	1	1	1	0	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	1	0	1	1	9

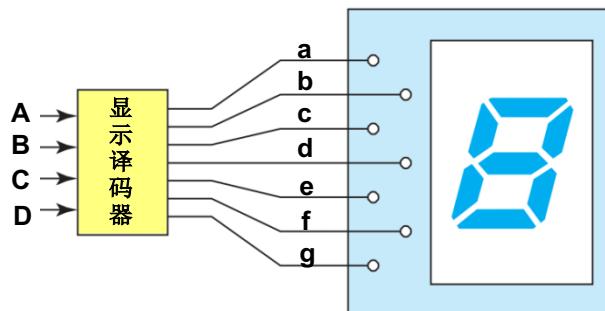
七段数码管



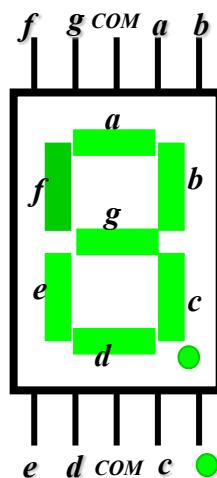
Exp 1:

2. Decoders

Design an 8-4-2-1 BCD code converter to drive a seven-segment indicator (Low active), by using **And-Or-Not** gates

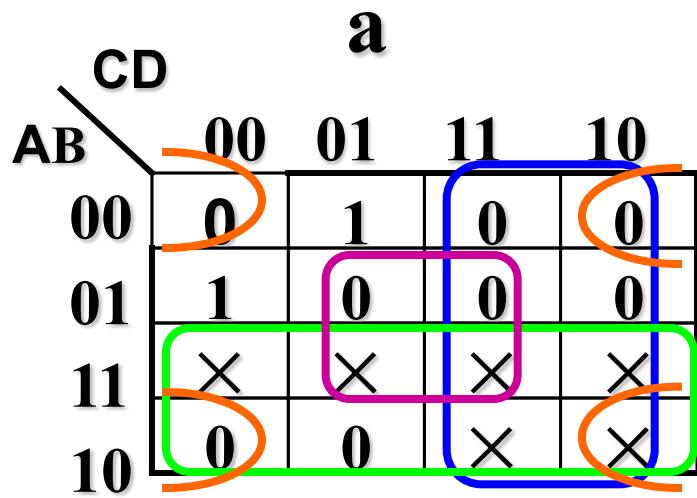


七段数码管

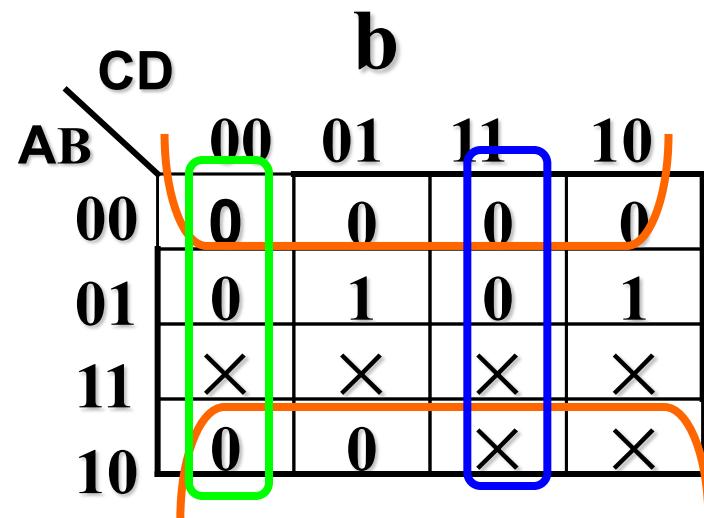


Digits	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0
3	0	0	1	1	0	0	0	0	1	1	0
4	0	1	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	0	1	0	0
6	0	1	1	0	0	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	0	1	0	0

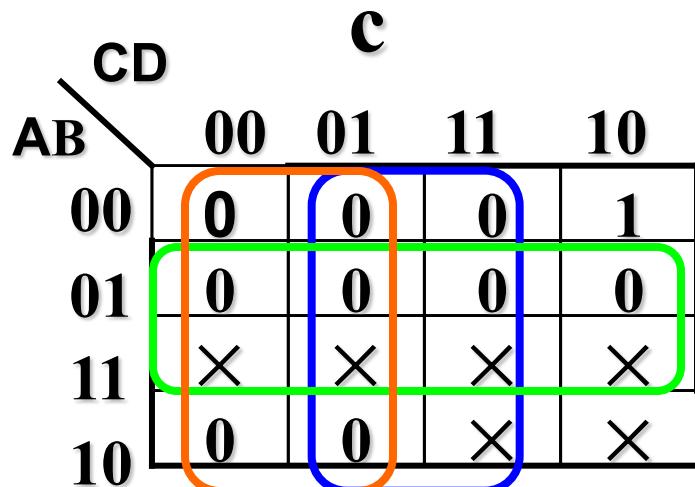




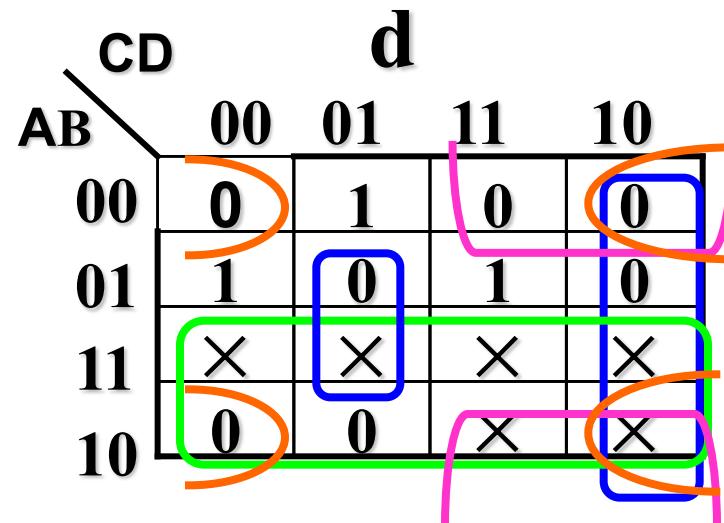
$$\bar{a} = A + C + BD + \bar{B}\bar{D}$$



$$\bar{b} = \bar{B} + \bar{C}\bar{D} + CD$$



$$\bar{c} = B + \bar{C} + D$$



$$\bar{d} = A + \bar{C}\bar{D} + \bar{B}C + \bar{B}\bar{D} + B\bar{C}D$$

e

	CD	00	01	11	10
AB	00	0	1	1	0
	01	1	1	1	0
	11	x	x	x	x
	10	0	1	x	x

$$\bar{e} = CD + \bar{B}\bar{D}$$

f

	CD	00	01	11	10
AB	00	0	1	1	1
	01	0	0	1	0
	11	x	x	x	x
	10	0	0	x	x

$$\bar{f} = A + \bar{C}\bar{D} + B\bar{C} + B\bar{D}$$

g

	CD	00	01	11	10
AB	00	1	1	0	0
	01	0	0	1	0
	11	x	x	x	x
	10	0	0	x	x

$$\bar{g} = A + C\bar{D} + \bar{B}C + B\bar{C}$$


Unit 7 Multiplexers and Decoders

- 数据选择器 (Multiplexers)
- 译码器 (Decoders)
- 编码器 (Encoders)
- 利用MSI设计组合逻辑电路



Design with MSI blocks

- ① 了解各类典型集成电路芯片的功能、外特性；
- ② 学会查阅器件资料；
- ③ 能灵活运用，完成最佳设计。

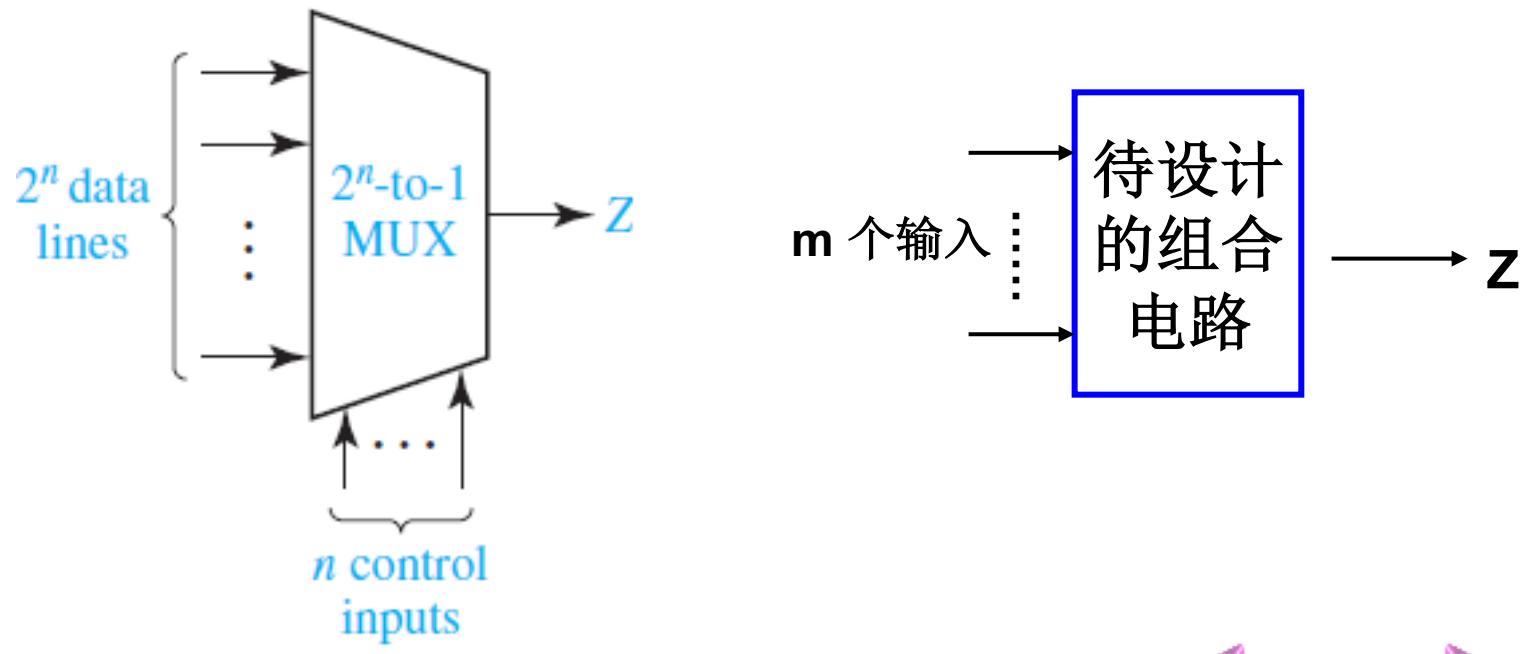
MSI blocks {

- Multiplexers
- Decoders

1. Combinational Logic Design with multiplexers

(1) $m = n$

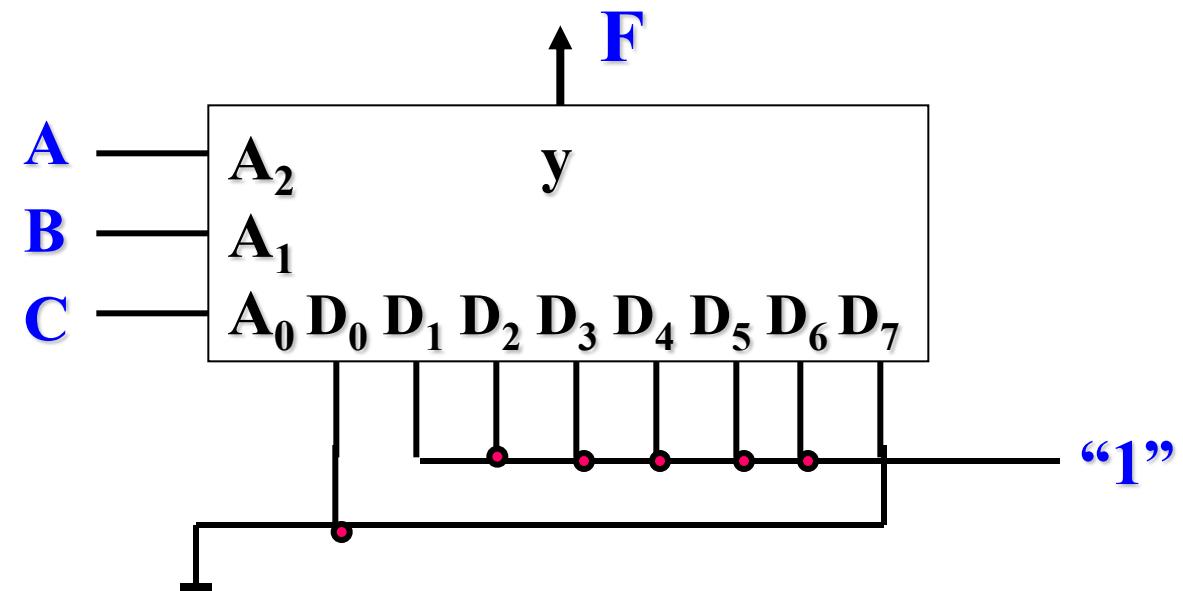
→ 数据选择器的控制端个数
→ 组合电路的输入变量个数



Example

Use 8 to 1 MUX realize $F = A\bar{B} + \bar{A}C + BC$

$A_2 A_1 A_0$	y
0 0 0	D_0
0 0 1	D_1
0 1 0	D_2
0 1 1	D_3
1 0 0	D_4
1 0 1	D_5
1 1 0	D_6
1 1 1	D_7



K.Map of F

BC	00	01	11	10
0	0	1	1	1
1	1	1	0	1

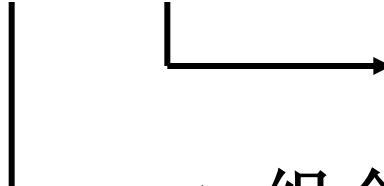
K.Map of MUX

$A_1 A_0$	00	01	11	10
0	D_0	D_1	D_3	D_2
1	D_4	D_5	D_7	D_6



1. Combinational Logic Design with multiplexers

(2) $m = n+1$

 数据选择器的控制端个数
组合电路的输入变量个数

Method: 降维

Example

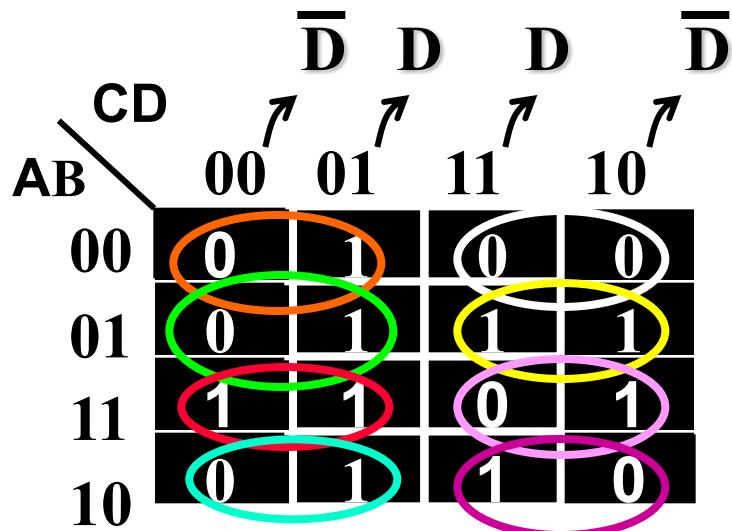
利用 8 to 1 MUX 设计组合逻辑：

$$F(A,B,C,D) = \sum m(1,5,6,7,9,11,12,13,14)$$

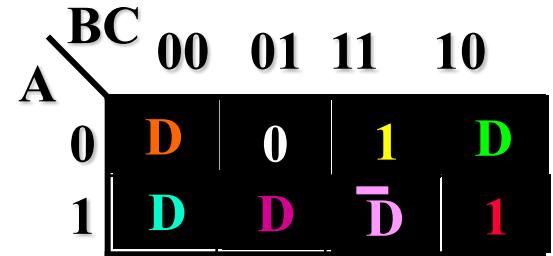


1. Combinational Logic Design with multiplexers

$$F(A,B,C,D) = \sum m(1,5,6,7,9,11,12,13,14)$$



降维



$$f(x_1 x_2 \dots x_i \dots \underline{x_n})$$

$$= x_i \cdot f(x_1 x_2 \dots 1 \dots \underline{x_n}) + \bar{x}_i \cdot f(x_1 x_2 \dots 0 \dots \underline{x_n})$$

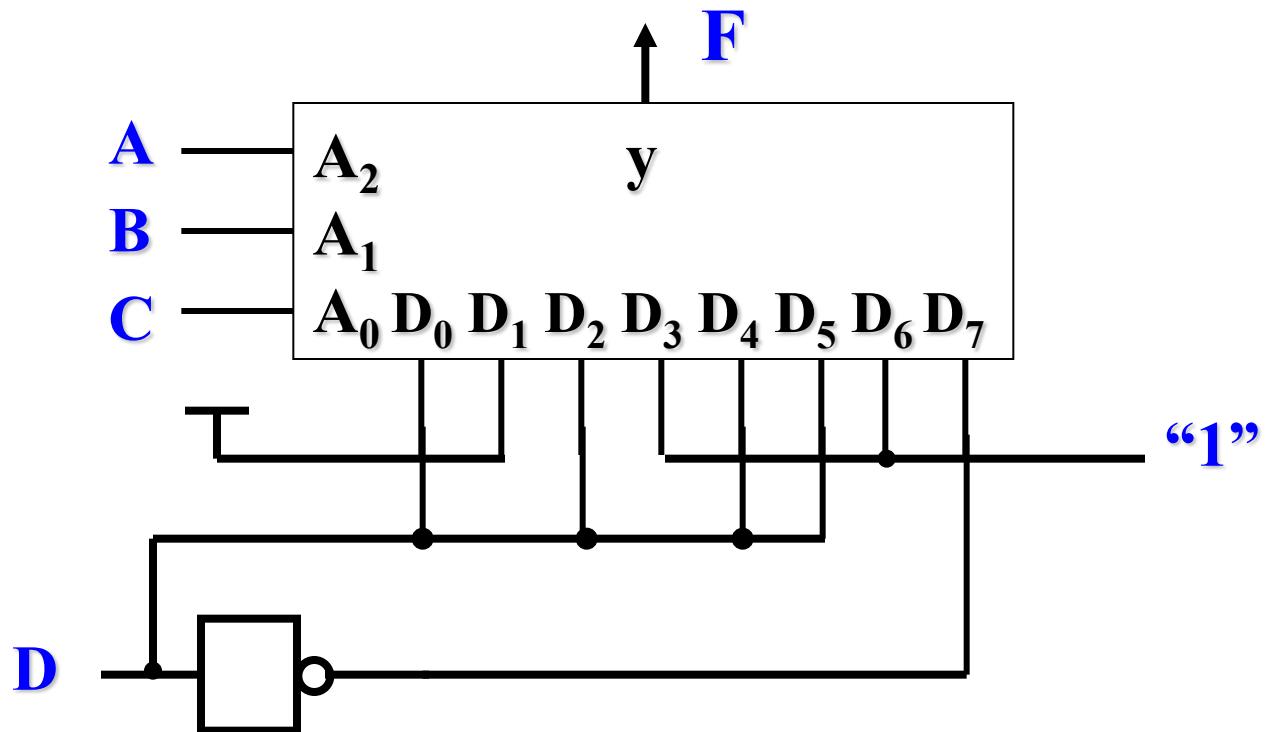


	$A_1 A_0$	00	01	11	10
A_2	0	D_0	D_1	D_3	D_2
1	1	D_4	D_5	D_7	D_6

K.Map of MUX

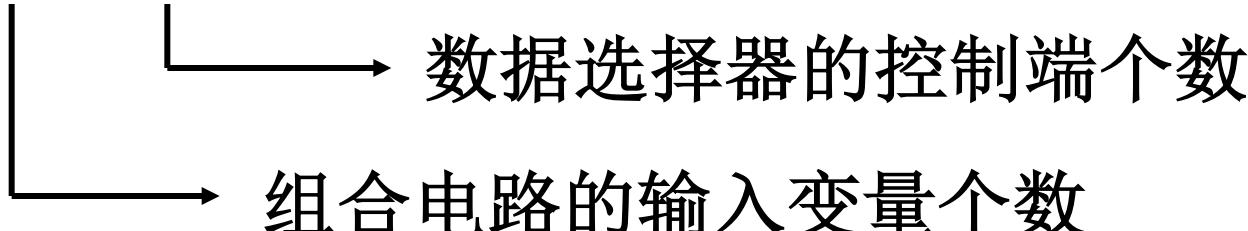
	BC	00	01	11	10
A	0	D	0	1	D
1	1	D	D	\bar{D}	1

K.Map of F



1. Combinational Logic Design with multiplexers

$$(3) m = n+2$$

 数据选择器的控制端个数
组合电路的输入变量个数

Method: 降维

Example

Use 4-to-1 MUX realize :

$$F(A,B,C,D) = \sum m(0,1,5,6,7,9,10,14,15)$$

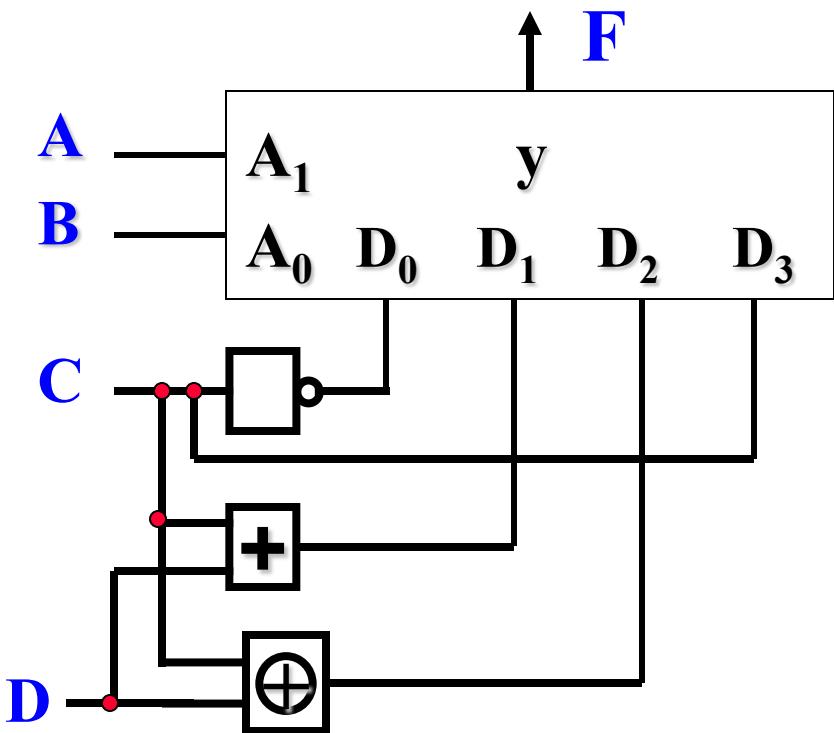


	\bar{D}	D	D	\bar{D}
CD	00	01	11	10
AB	00	11	00	00
00	1 0	1 1	0 1	0 1
01	0 1	1 1	1 1	1 1
11	0 0	0 0	1 1	1 1
10	0 1	1 0	0 1	0 1

降维

	\bar{D}	D	\bar{D}	
BC	00	01	11	10
A	0	1	0	1
0	1 D	0 \bar{D}	1 1	D 0
1	D 0	1 1	0 1	1 0

降维



B	0	1
0	\bar{C}	$C+D$
1	$C \oplus D$	C



利用4-to-1 MUX 设计组合逻辑

$$F(A,B,C,D,E) = \sum m(0,5,8,9,10,11,17,18,19,20,22,23,28,30,31)$$

	A	B	C	D	E	F
00	0	0	0	0	1	1
			1	0	0	0
	0	1	0	0	0	0
			1	0	0	0
	1	0	0	0	0	0
			1	1	1	1
	1	1	0	0	0	0
			1	0	0	0
01	0	0	0	0	1	1
			1	1	1	1
	0	1	0	0	1	1
			1	1	1	1
	1	0	0	0	0	0
			1	0	0	0
	1	1	0	0	0	0
			1	0	0	0

\bar{E}

0

E

0

1

1

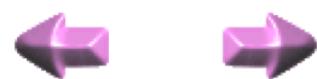
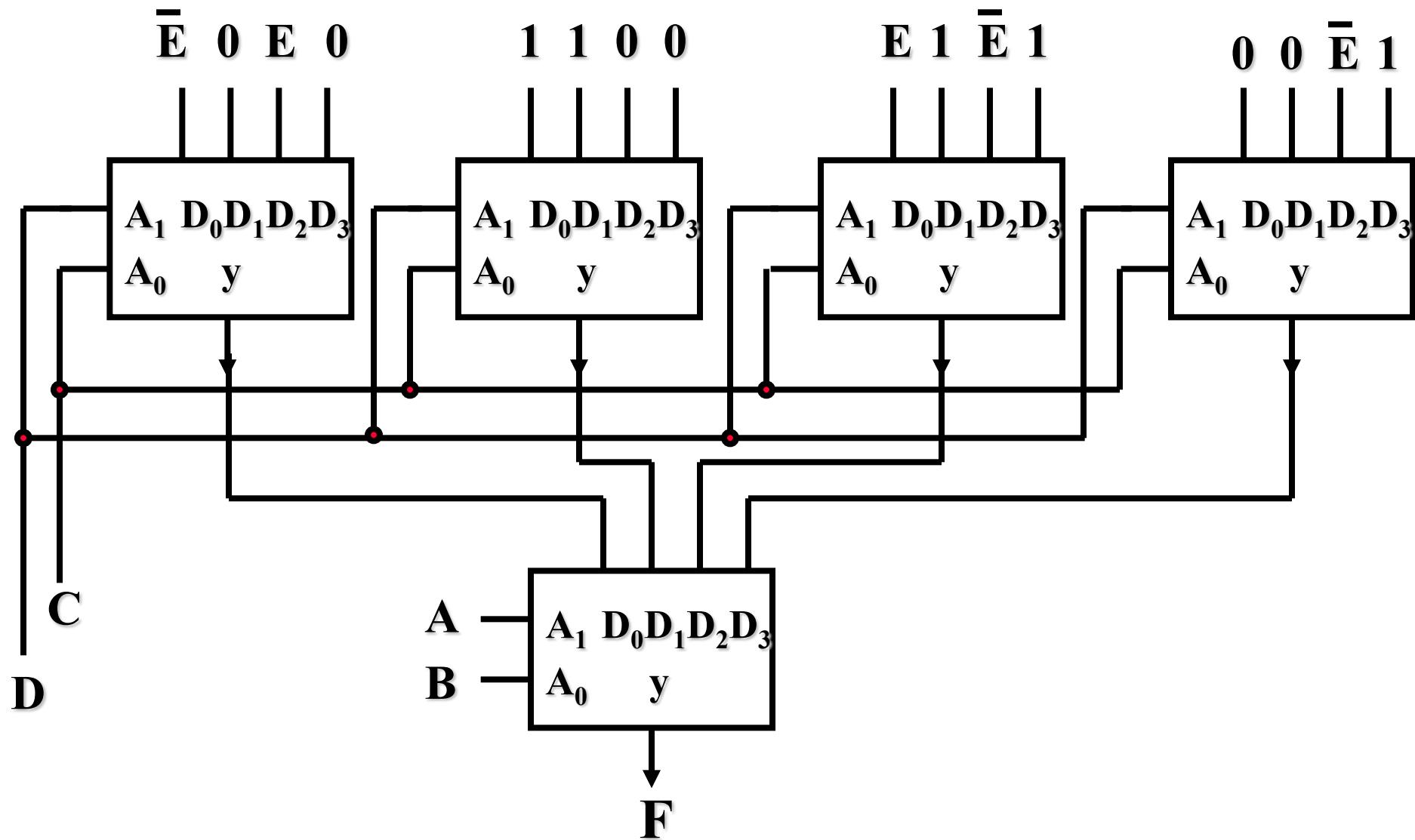
0

0

	A	B	C	D	E	F
10	0	0	0	0	0	0
			1	1	1	1
	0	1	0	0	1	1
			1	1	1	1
	1	0	0	0	1	1
			1	0	0	0
	1	1	0	0	1	1
			1	1	1	1
11	0	0	0	0	0	0
			1	0	0	0
	0	1	0	0	0	0
			1	0	0	0
	1	0	0	0	1	1
			1	0	0	0
	1	1	0	0	1	1
			1	1	1	1

E
1
 \bar{E}
1
 \bar{E}
1
0
0
 \bar{E}
1
0
0
 \bar{E}
1

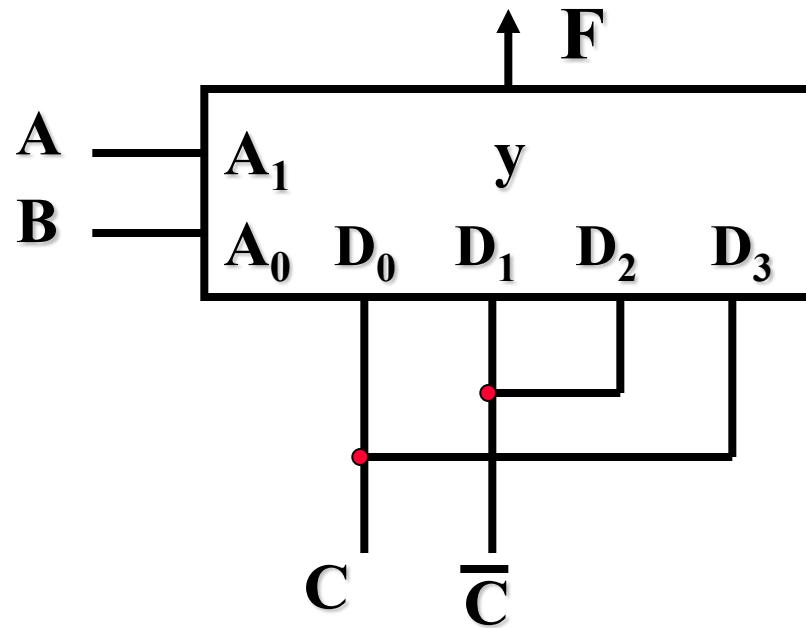




1. Combinational Logic Design with multiplexers

Example

Write the expression of F



$$F = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$



1. Combinational Logic Design with multiplexers

Example

Use 4-to-1 MUX realize

$$F(A,B,C,D) = \sum m(1,2,4,9, 10, 11, 12, 14, 15)$$

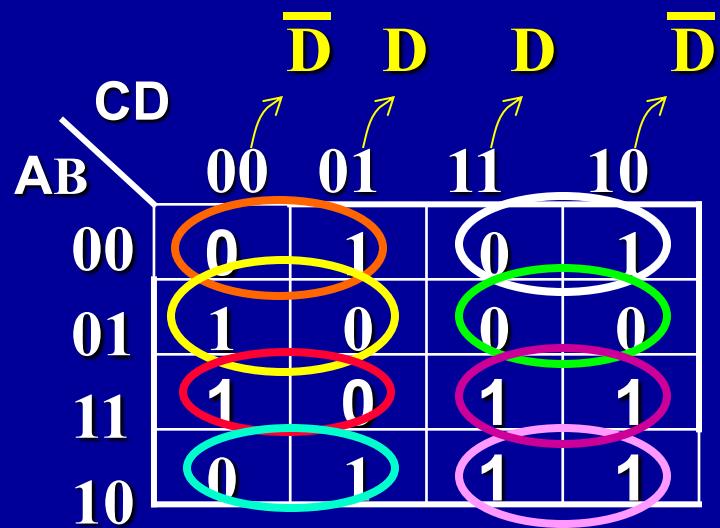
Method: 降维

从函数的多个输入变量中选出2个作为MUX的选择控制变量。原则上讲，这种选择是任意的，但选择合适时可使设计简化。

- ① Choose A and B



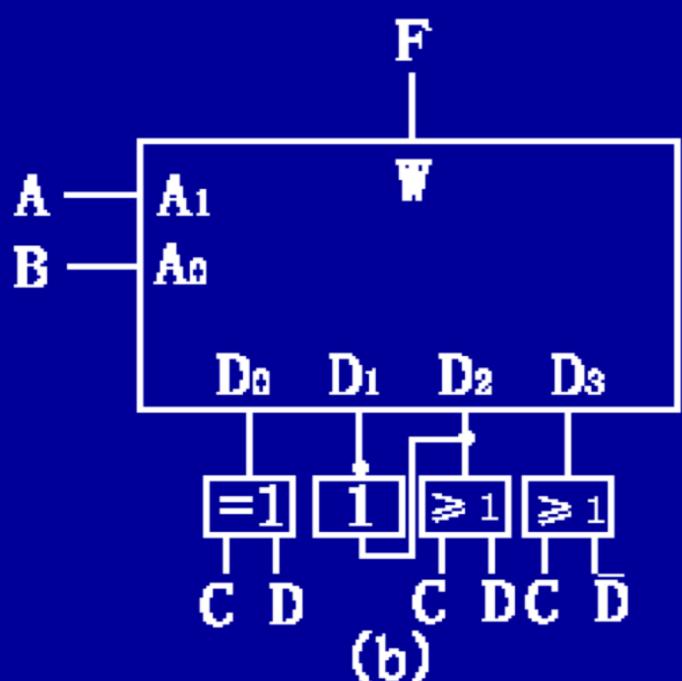
① Choose A and B



降维

$A \backslash BC$	00	01	11	10
0	D	\bar{D}	0	\bar{D}
1	D	1	1	\bar{D}

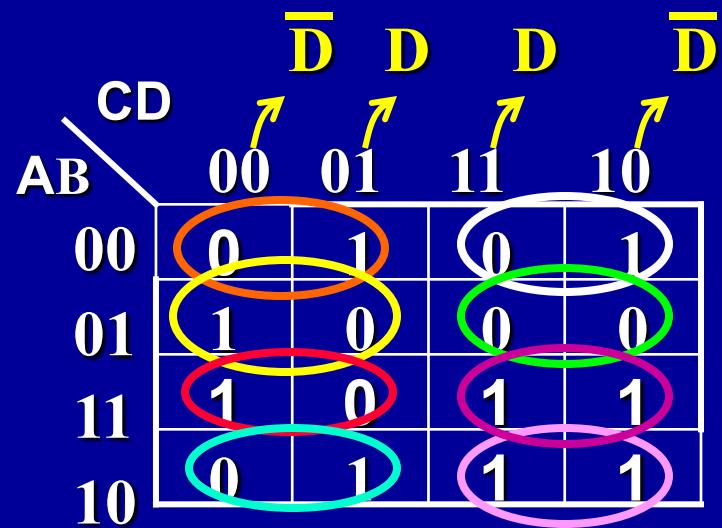
降维



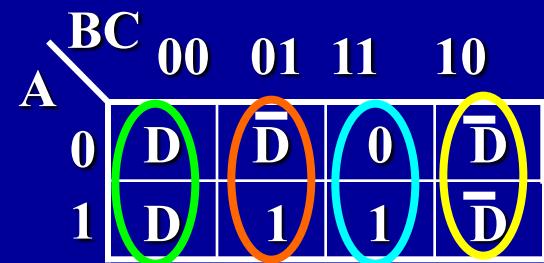
$A \backslash B$	0	1
0	$C \oplus D$	$\bar{C}\bar{D}$
1	$C+D$	$C+\bar{D}$



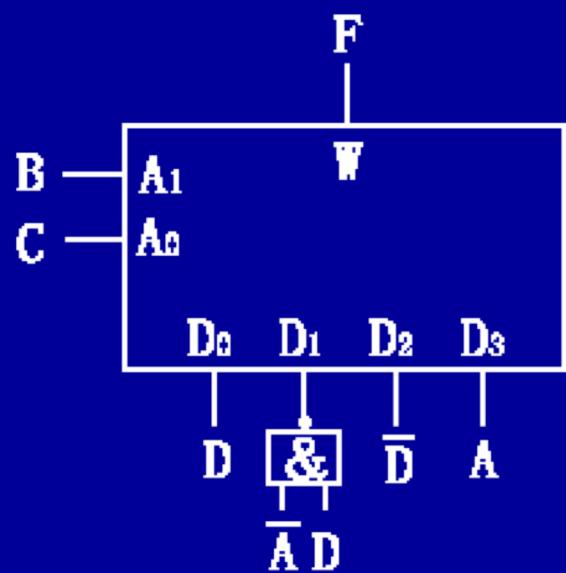
② Choose B and C



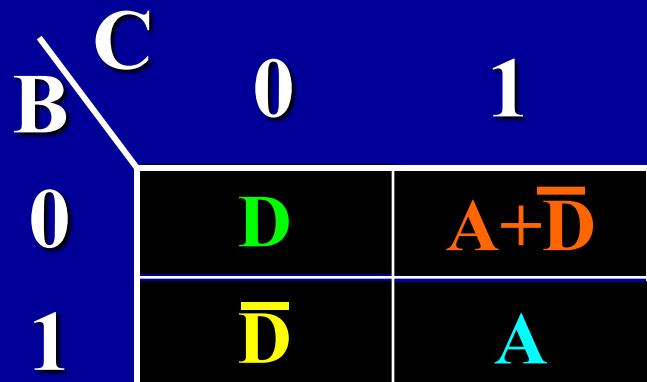
降维



降维

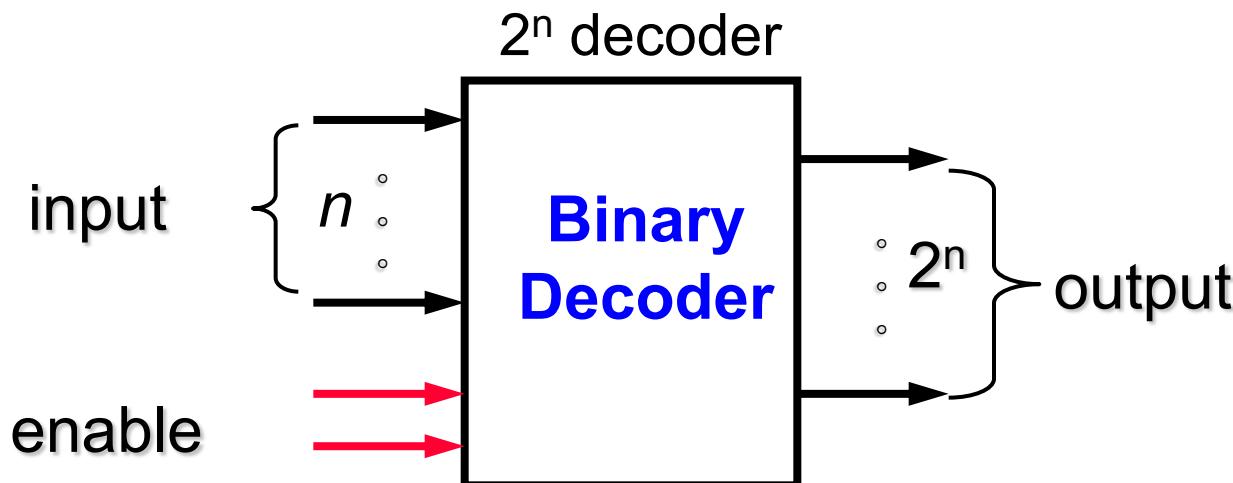


(d)



2. Combinational Logic Design with Decoders

- MSI blocks {
- Multiplexers
 - Decoders



$$y_i = m_i, \quad i = 0 \text{ to } 2^n - 1 \quad (\text{noninverted outputs})$$

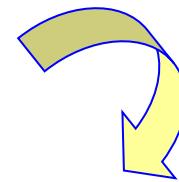
$$y_i = m'_i = M_i, \quad i = 0 \text{ to } 2^n - 1 \quad (\text{inverted outputs})$$



2. Combinational Logic Design with Decoders

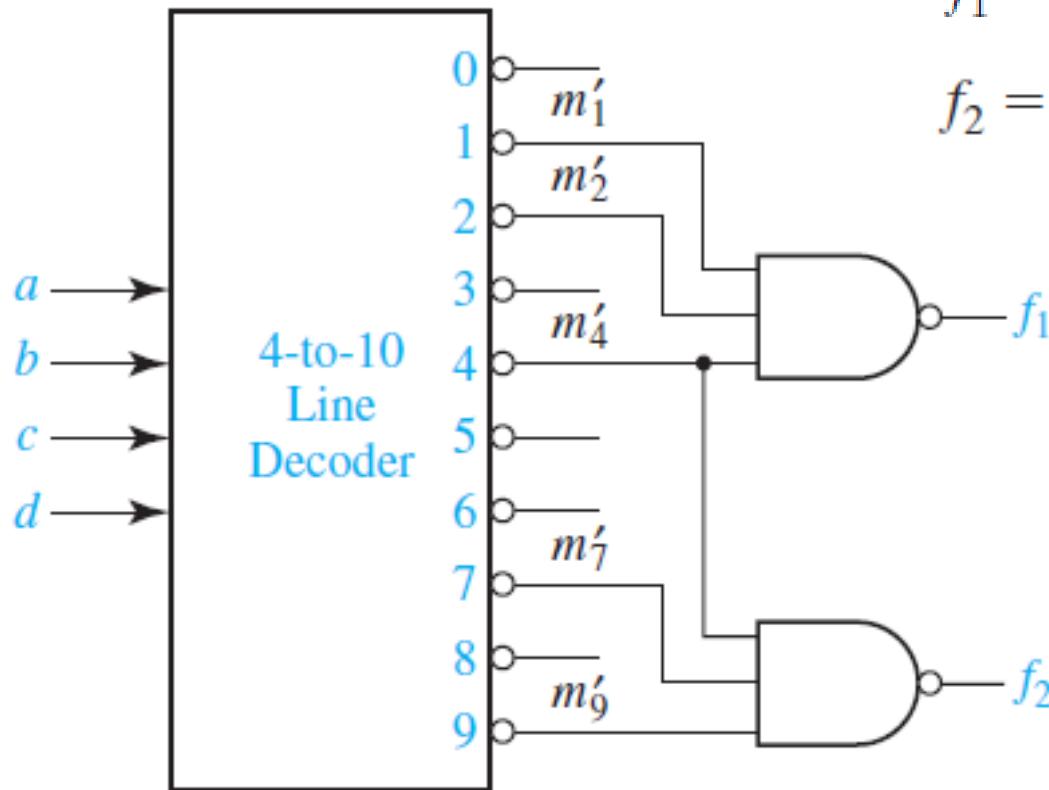
$$f_1(a, b, c, d) = m_1 + m_2 + m_4$$

$$f_2(a, b, c, d) = m_4 + m_7 + m_9$$



$$f_1 = (m'_1 m'_2 m'_4)'$$

$$f_2 = (m'_4 m'_7 m'_9)'$$



2. Combinational Logic Design with Decoders

Example

利用 74LS138 设计 1-bit FA

a_i	b_i	C_{i-1}	S_i	C_i
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

使能端			输入			译码输出							
G_1	G_{2A}	G_{2B}	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	1	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	1	1	1	1	1	1	0	1	1
1	0	0	1	1	0	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0

$$y_i = \bar{m}_i$$

$$S_i = \sum (1, 2, 4, 7) = \overline{\bar{m}_1} \overline{\bar{m}_2} \overline{\bar{m}_4} \overline{\bar{m}_7}$$

$$C_{i-1} = \sum (3, 5, 6, 7) = \overline{\bar{m}_3} \overline{\bar{m}_5} \overline{\bar{m}_6} \overline{\bar{m}_7}$$



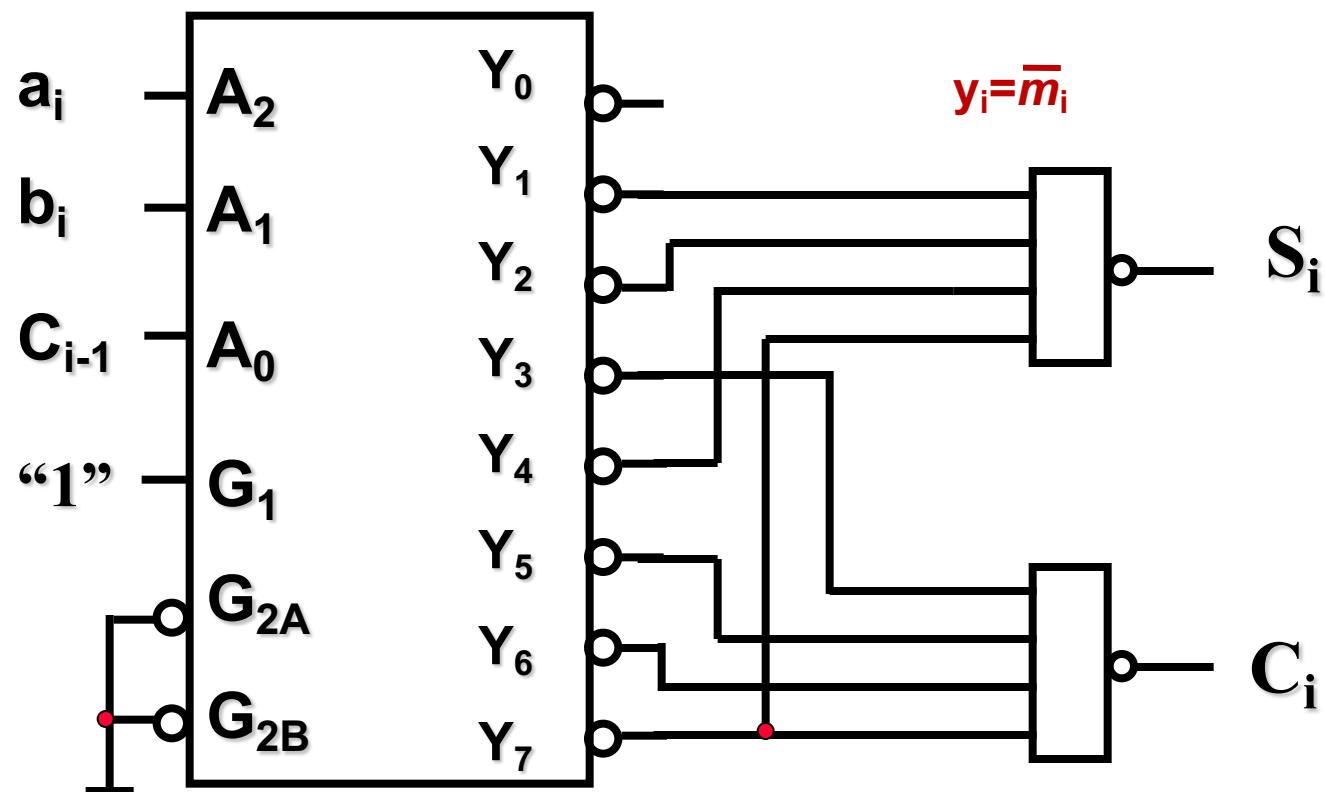
74138功能表

使能端			输入			译码输出							
G ₁	G _{2A}	G _{2B}	C	B	A	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
0	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	1	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	1	1	1	1	1	1	0	1	1
1	0	0	1	1	0	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0

$$S_i = \sum (1, 2, 4, 7) = \overline{m}_1 \overline{m}_2 \overline{m}_4 \overline{m}_7$$

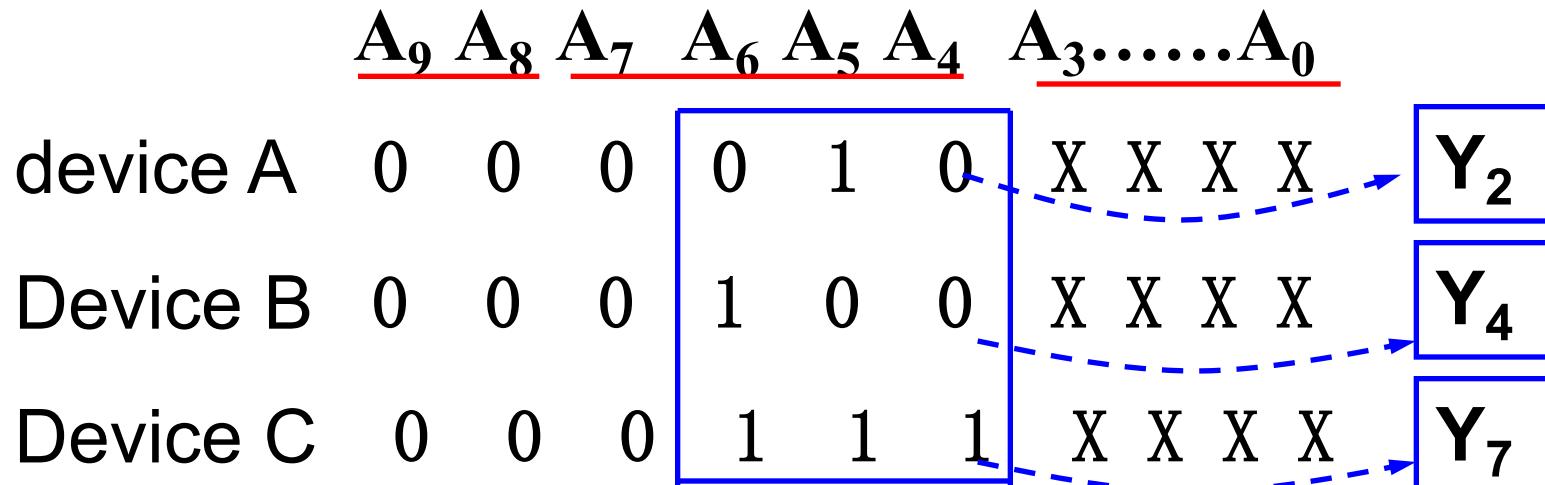
$$c_{i-1} = \sum (3, 5, 6, 7) = \overline{m}_3 \overline{m}_5 \overline{m}_6 \overline{m}_7$$

74LS138



2. Combinational Logic Design with Decoders

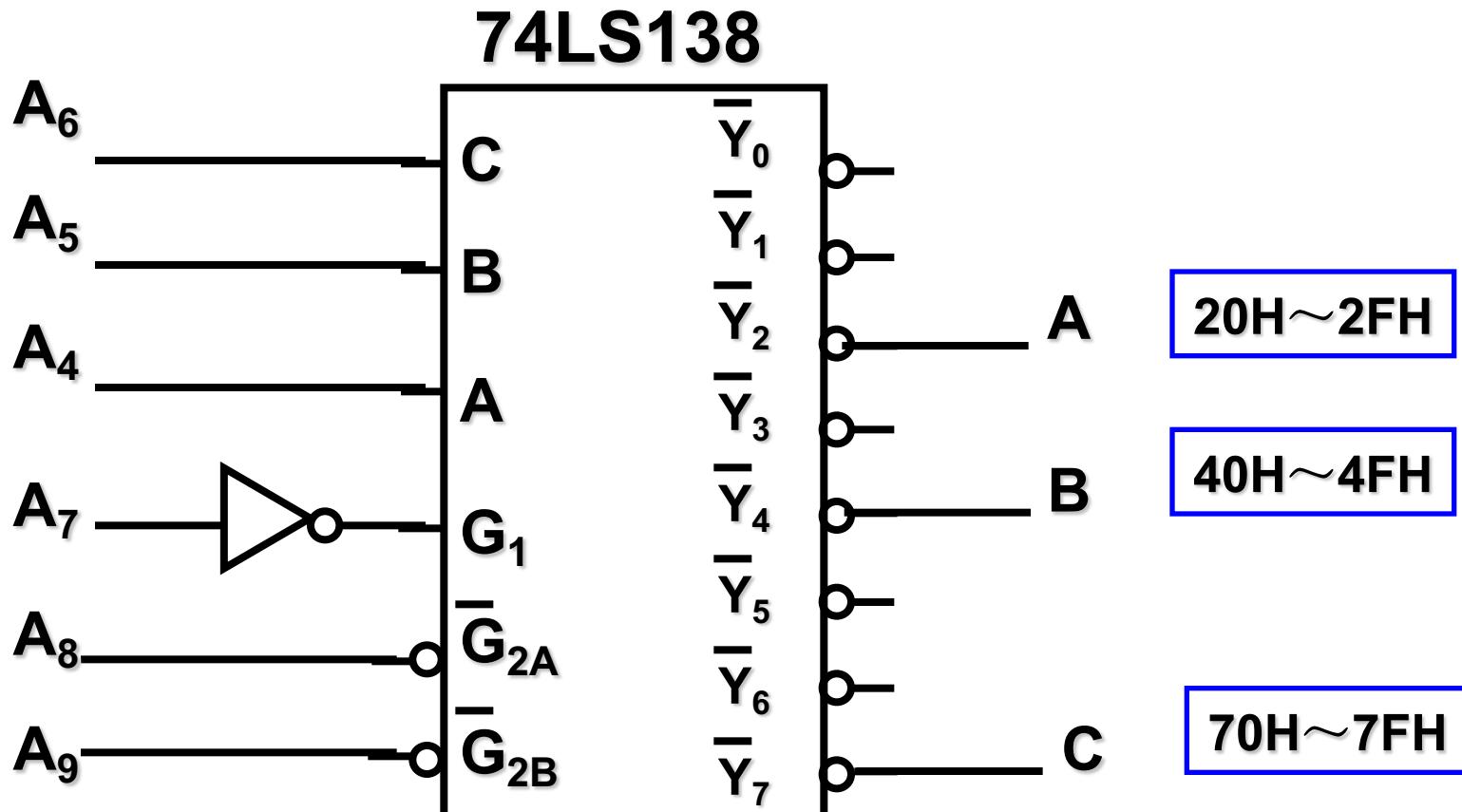
Address lines $A_9 A_8 \dots A_0$ will be used to select devices A, B and C. The address assignment is 20H~2FH, 40H~4FH and 70H~7FH respectively, design the *address decoder* (地址译码器)。



3-8 decoder

2. Combinational Logic Design with Decoders

Circuit



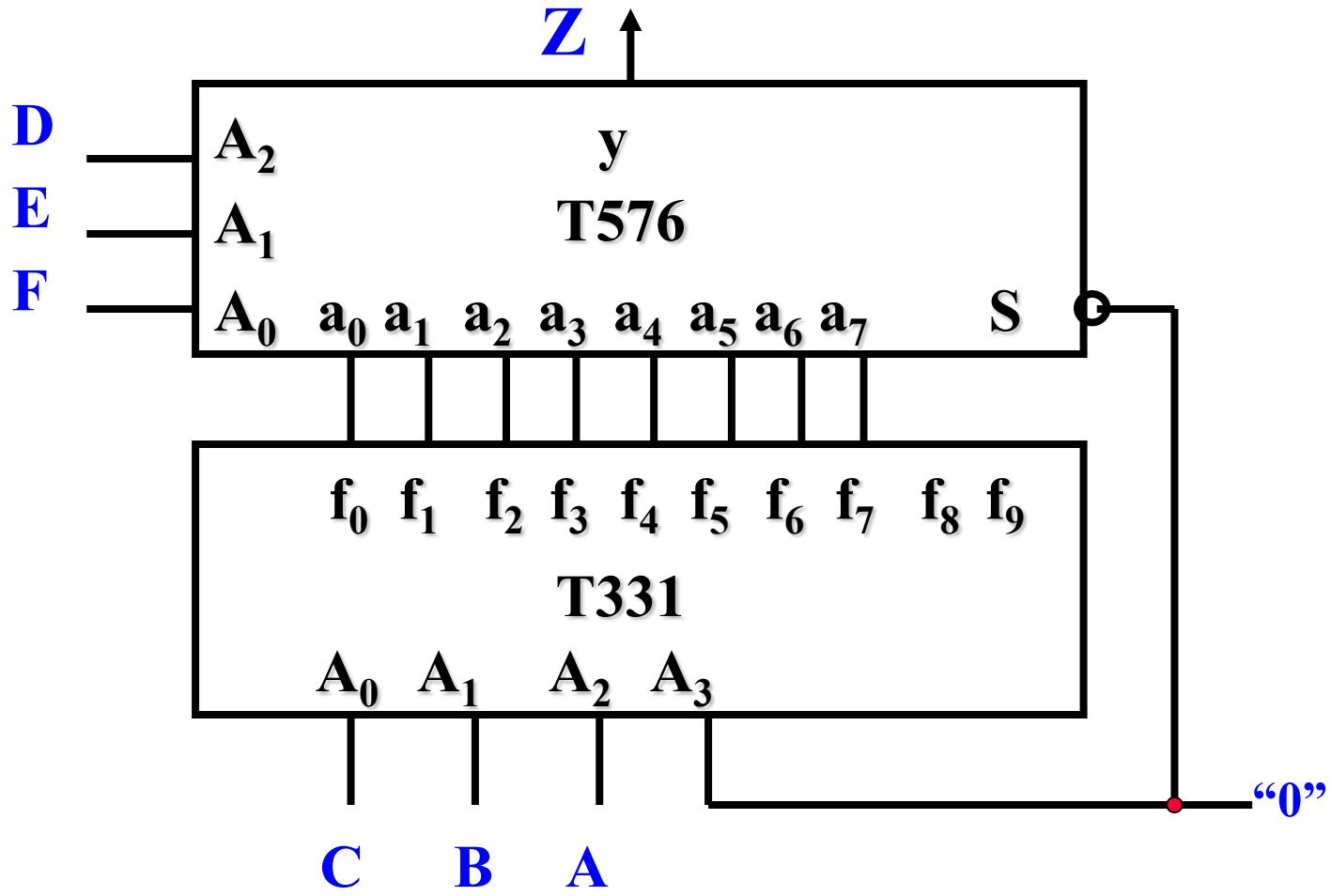
Example

利用 8-to -1 MUX 以及 4-10线译码器设计一个能实现2组3位数码等值比较的电路。

$A_3\ A_2\ A_1\ A_0$	$f_0\ f_1\ f_2\ f_3\ f_4\ f_5\ f_6\ f_7\ f_8\ f_9$
0 0 0 0	0 1 1 1 1 1 1 1 1 1
0 0 0 1	1 0 1 1 1 1 1 1 1 1
0 0 1 0	1 1 0 1 1 1 1 1 1 1
0 0 1 1	1 1 1 0 1 1 1 1 1 1
0 1 0 0	1 1 1 1 0 1 1 1 1 1
0 1 0 1	1 1 1 1 1 0 1 1 1 1
0 1 1 0	1 1 1 1 1 1 0 1 1 1
0 1 1 1	1 1 1 1 1 1 1 0 1 1
1 0 0 0	1 1 1 1 1 1 1 1 0 1
1 0 0 1	1 1 1 1 1 1 1 1 1 0

8-to -1 MUX

S	$A_2\ A_1\ A_0$	y
1	× × ×	0
0	0 0 0	a_0
0	0 0 1	a_1
0	0 1 0	a_2
0	0 1 1	a_3
0	1 0 0	a_4
0	1 0 1	a_5
0	1 1 0	a_6
0	1 1 1	a_7



if: $ABC = 110$, then $f_6 = a_6 = 0$

If $ABC = DEF$

if: $DEF = 110$, then $y = a_6 = 0$



Then $Z = 0$

if: $DEF = 111$, then $y = a_7 = 0$



Unit 7 Multiplexers and Decoders

- 数据选择器 (Multiplexers)
- 译码器 (Decoders)
- 编码器 (Encoders)
- 利用MSI设计组合逻辑电路