**Variante A**

Q: I want to instantiate a library cell  
A: Answer from [@Matt Venn](https://open-source-silicon.slack.com/team/U0172QZ342D) in other thread is to use this: set ::env(SYNTH\_READ\_BLACKBOX\_LIB) 1

Q: Hot to use Openlane Interactive Mode  
A: <https://openlane-docs.readthedocs.io/en/rtd-develop/doc/advanced_readme.html>

Q: Cell design rules?  
A: <https://github.com/nickson-jose/vsdstdcelldesign> (fixed\_bbox, port settings, unithd, LEFclass/source)

Q: FIXED\_BBOX size?  
A: for HD: X:0.460 Y:0.340  
property FIXED\_BBOX {0 0 N\*0,92 8\*0,68} weil scale=0.5

Q: P&R Grid?  
A: grid 0.46um 0.34um 0.23um 0.17um

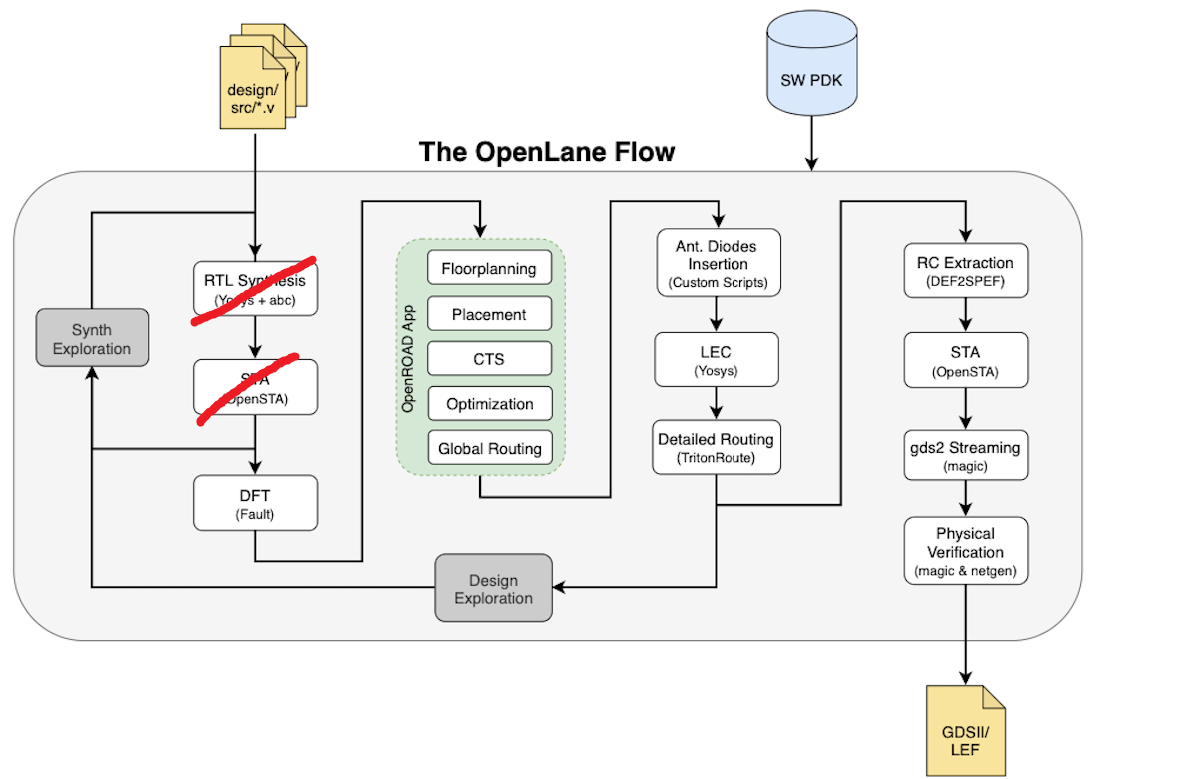
Q: Root changes?  
A: in openlane/scripts/floorplan disable basic macro floorplanning, macros not available if synth file read as blackbox

**Shape abutment?**

**Variante B**

**Gate-Level to GDSII with OpenLane**

The usual openlane-flow is RTL to GDSII, but we have no RTL file in this example. Instead, we want to skip Synthesis and convert a **Gate-Level-Design to GDSII** without further optimization and altering of cells.

  
*Image from* [*https://github.com/The-OpenROAD-Project/OpenLane/raw/master/docs/\_static/openlane.flow.1.png*](https://github.com/The-OpenROAD-Project/OpenLane/raw/master/docs/_static/openlane.flow.1.png)

To achieve this, we must skip RTL-synthesis manually and prevent the tool from altering our cells. This is a possible workflow:

New openlane designs are usually initialized with ./flow.tcl -init-design-config , but this does not work in the docker environment. Instead, copy one of the design templates

* from /foss/tools/openlane/2022.07/designs/<designname>
* to /designs/<project-name>/openlane/<yournewdesignname>

Write your Verilog HDL-file in the format as shown in the image below. You can find names for the standard cells in [https://antmicro-skywater-pdk-docs.readthedocs.io](https://antmicro-skywater-pdk-docs.readthedocs.io/en/test-submodules-in-rtd/contents/libraries/sky130_fd_sc_hd/cells/clkdlybuf4s50/README.html) and the PDK Verilog-library at /foss/pdk/sky130A/libs.ref/sky130\_fd\_sc\_hd/verilog/sky130\_fd\_sc\_hd.v  
  
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Automatisch generierte Beschreibung

Change the config /designs/<project-name>/openlane/<yourdesignname>/config.tcl

* + Links to your Verilog-file
  + Name of your project
  + Prevent the router and placer from altering your cells by specifying
    1. set ::env(PL\_RESIZER\_TIMING\_OPTIMIZATIONS) {0}
    2. set ::env(PL\_RESIZER\_DESIGN\_OPTIMIZATIONS) {0}
    3. set ::env(GLB\_RESIZER\_TIMING\_OPTIMIZATIONS) {0}
  + Optional: set your pin order and fanout orientations with
    1. set ::env(FP\_PIN\_ORDER\_CFG) $::env(DESIGN\_DIR)/pin\_order.cfg

start a terminal at /designs/<project-name>/openlane/

run flow-tcl -interactive -design <yourdesignname> -tag <run-name>

type package require openlane, console should return 0.9

Before you start synthesis, copy your already synthesized file into   
..openlane/<yourdesignname>/runs/<run-name>/results/synthesis

Type run\_synthesis in the console, synthesizer should recognize there is already a file (which is exactly what we want)  
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Automatisch generierte Beschreibung

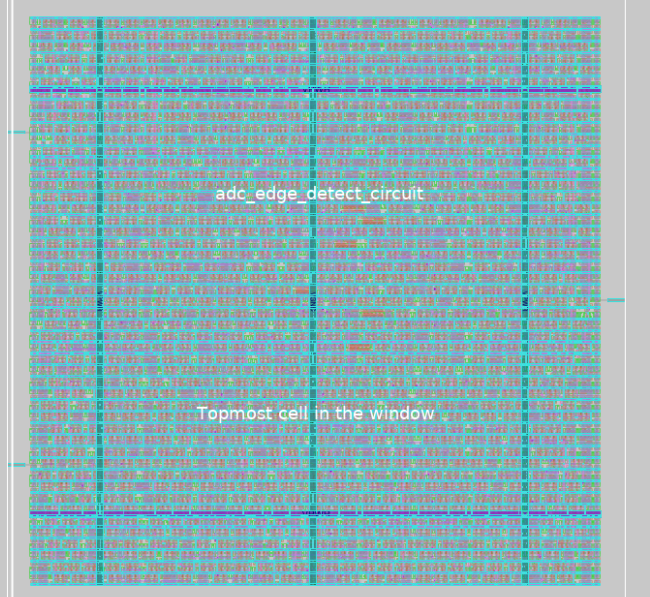
Type run\_floorplan

Type run\_placement

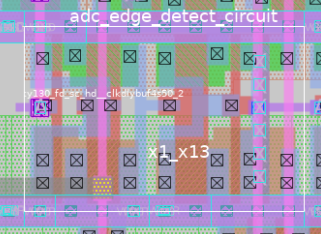
Type run\_routing

Type run\_magic

Result in runs/<run-name>/results/signoff/<project-name>.mag



…which is using the exact cell-type specified in our gate-level-design.



**Appendix A: list of interactive openlane commands**

<https://github.com/The-OpenROAD-Project/OpenLane/blob/master/docs/source/advanced_readme.md>

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Automatisch generierte Beschreibung

**Appendix B: Configuration file of a CLKDLYBUF\_4S50\_2 combinatorial Delay-cell**

**Folder structure:**

/foss/designs/SKY130\_SAR-ADC

-/verilog

-/adc\_edge\_detect\_circuit/ adc\_edge\_detect\_circuit.v

-/openlane

-/adc\_edge\_detect\_circuit/

-/runs/

-/config.tcl

-/pin\_order.cfg

**Contents of config.tcl:**

set ::env(DESIGN\_NAME) "adc\_edge\_detect\_circuit"

set filename $::env(DESIGN\_DIR)/$::env(PDK)\_$::env(STD\_CELL\_LIBRARY)\_config.tcl

if { [file exists $filename] == 1} {

source $filename

}

set ::env(VERILOG\_FILES) "/foss/designs/SKY130\_SAR-ADC/verilog/adc\_edge\_detect\_circuit/adc\_edge\_detect\_circuit.v"

# set ::env(CLOCK\_PERIOD) "10.000"

set ::env(CLOCK\_PORT) "clk"

set ::env(CLOCK\_NET) $::env(CLOCK\_PORT)

# Floorplanning

set ::env(FP\_SIZING) "relative"

set ::env(FP\_ASPECT\_RATIO) {1}

set ::env(FP\_CORE\_UTIL) {75}

set ::env(FP\_PDN\_VPITCH) {100}

set ::env(FP\_PDN\_HPITCH) {100}

set ::env(FP\_PIN\_ORDER\_CFG) $::env(DESIGN\_DIR)/pin\_order.cfg

# Placement

set ::env(PL\_TARGET\_DENSITY) {0.80}

# set ::env(PL\_TIME\_DRIVEN) {0}

set ::env(PL\_RESIZER\_TIMING\_OPTIMIZATIONS) {0}

set ::env(PL\_RESIZER\_DESIGN\_OPTIMIZATIONS) {0}

#Clocktreesynthesis - unused

# set ::env(CLOCK\_TREE\_SYNTH) {0}

# set ::env(FILL\_INSERTION) {0}

# Router

set ::env(GLB\_RESIZER\_TIMING\_OPTIMIZATIONS) {0}

set ::env(CELL\_PAD) {0}