

Caravel Board Requirements Specifications

Date	Author	Notes
May 4, 2021	mshalan	Document creation; initial daughter and carrier boards design
May 5, 2021	mshalan	Updates to clarify things; added daughter board form factors; minor updates to the boards design
May 7, 2021	mshalan	Made some of the daughter board components optional
May 20, 2021	mshalan	Daughter board design update Added daughter board schematic and formfactor
May 24, 2021	jdicorpo	Removed narrow daughter board form factor and deleted texted.

1. Introduction

The purpose of this document is to outline the requirements for the board used to test and demonstrate the Caravel chip. As the Caravel chip function depends on the user's project, a two-board solution will be used.

- Daughter board: Contains Caravel and the necessary components to bring it up and running
- Carrier (Project) Board: A design specific board; contains peripherals and testing infrastructure to interface with the user's area I/Os.

2. The Daughter Board

This board is meant to be the same for all user's projects. It provides means to:

- Power the Management SoC
- Clock and reset the management SoC

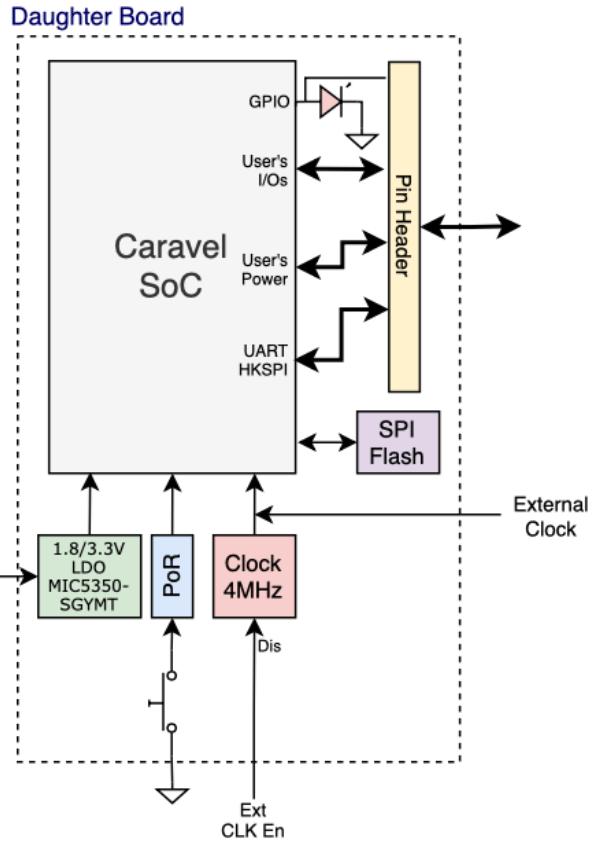


Figure 1. The Daughter Board Blockdiagram

2.1 Daughter Board Form Factor

We suggest a stamp like form factor with castellated pins. The castellated pins pitch is 1mm. Figure 2 shows 2 suggested layouts for 56 pins.

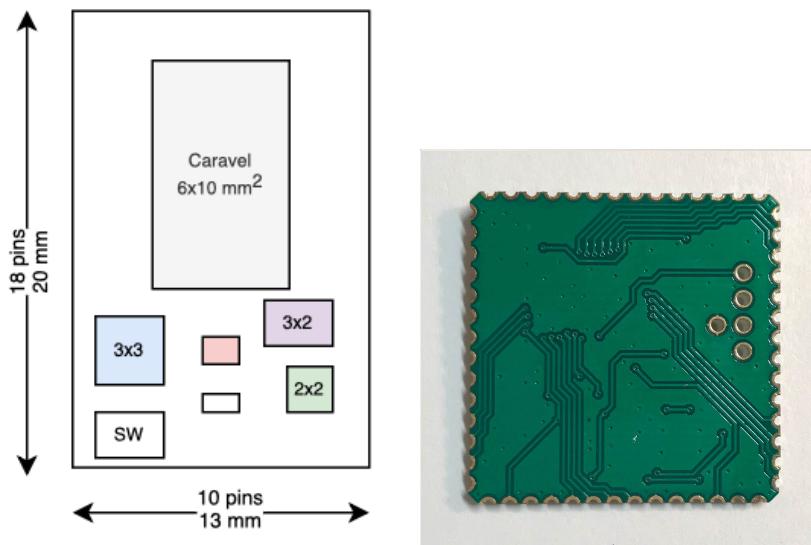


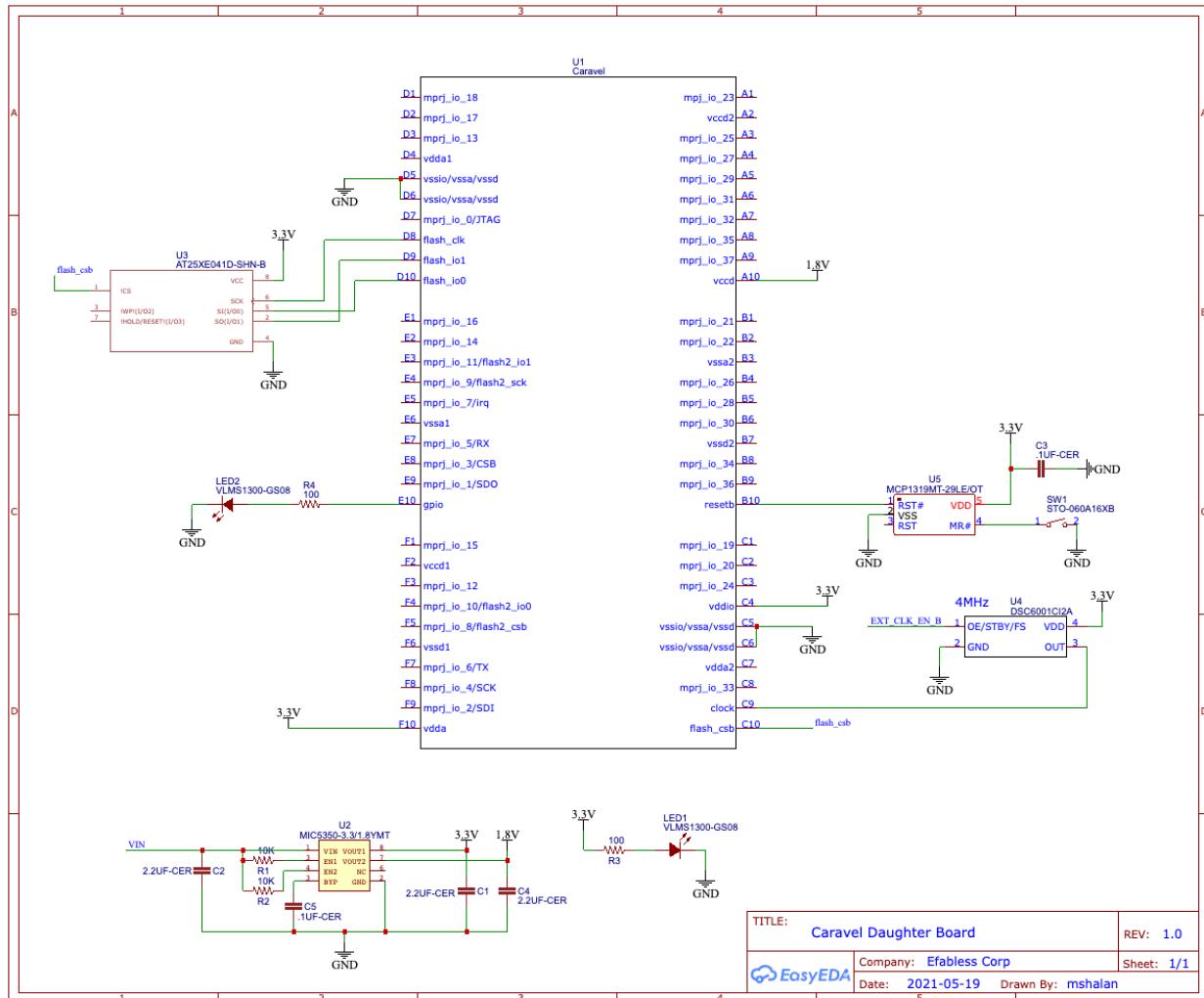
Figure 2. Proposed Form Factor

The daughter board pins are:

- 38 x User's IO pins
- 8 User's Power pins
- 1 x MPRJ GPIO pin
- 2 x MPRG supply pins (5V & GND)
- 1 x MPRG Ext Clock Enable pin
- 1 x MPRJ Ext Clock pin

Target number of pins = 51 pins

2.2 Daughter Schematic



Component	Part Number	Footprint (mm ²)
PoR	MCP1319MT-29	
LDO	MIC5350-SGYMT	2x2
Clock	DSC6001	1.6x1.2

FLASH	AT25XE041D-MAHN-T	3x2
LED	VLMS1300-GS08	Package: 0603
Tactile Switch	STO-060A16XB	
Resistors & Capacitors		Package 0402

3. The Carrier (Project) Board

The board design is not fixed and depends on the user's project design. This board provides any extra components (not in the daughter board) needed to demonstrate the user's project. Figure 3, shows a possible board design used to test/demonstrate a simple SoC implemented into the user's area. This sample design will be used as the starting point for designing a carrier board for a specific user's design.

The sample board provides the following features

- Programmable clock source (for testing)
- Programmable Power Supply (for testing)
- USB bridge for
 - Controlling the programmable clock source
 - Controlling the programmable power supply
 - UART/SPI/I2C interfacing
- QSPI Flash (SoC Program Memory)
- PSRAM (SoC External RAM)
- LEDs and Push buttons

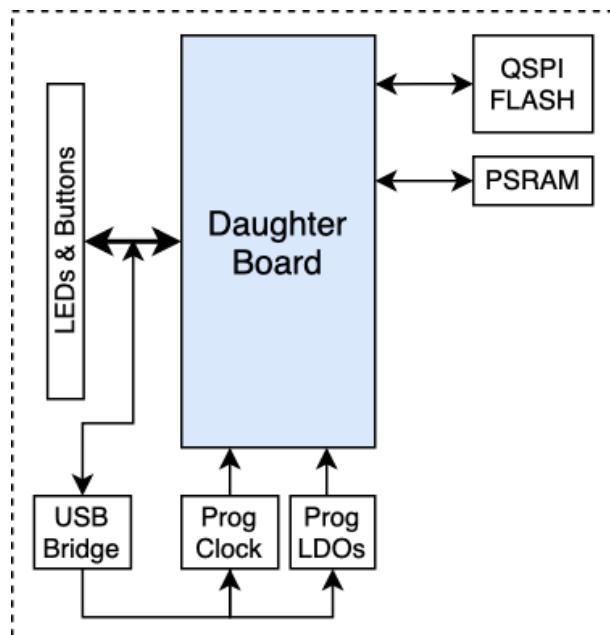


Figure 3. The block diagram of a sample carrier board for a simple SoC