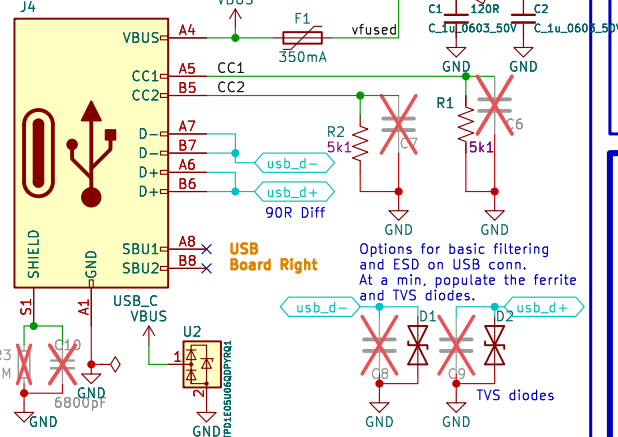


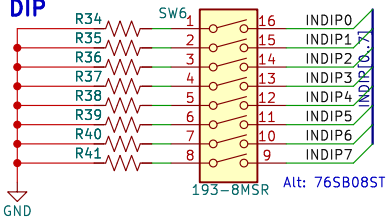
Chiplgnite/Efabless Explain FPGA ASIC Teaching Board

USB connector

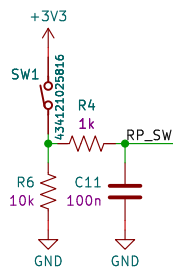
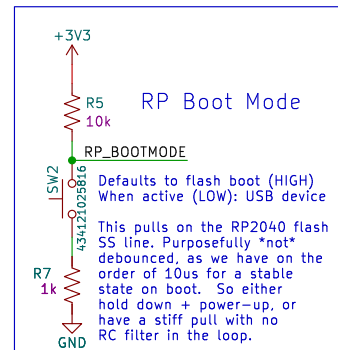
Power and USB2



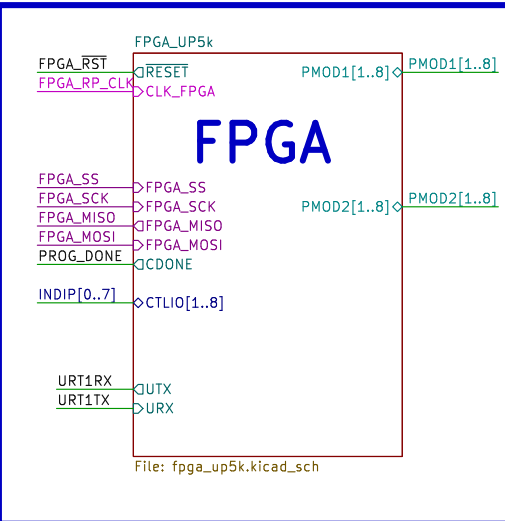
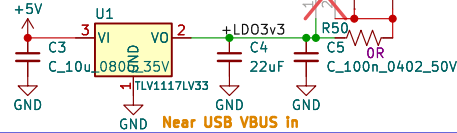
Input DIP



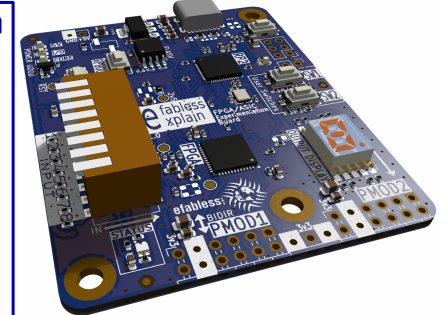
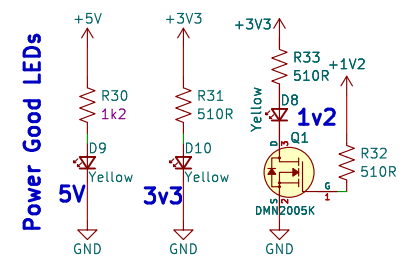
RP2040 MCU



3V3 LDO

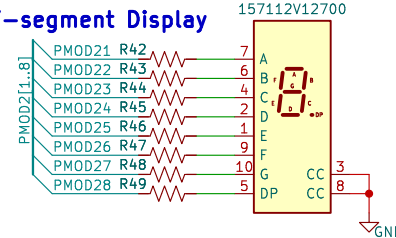


Indication

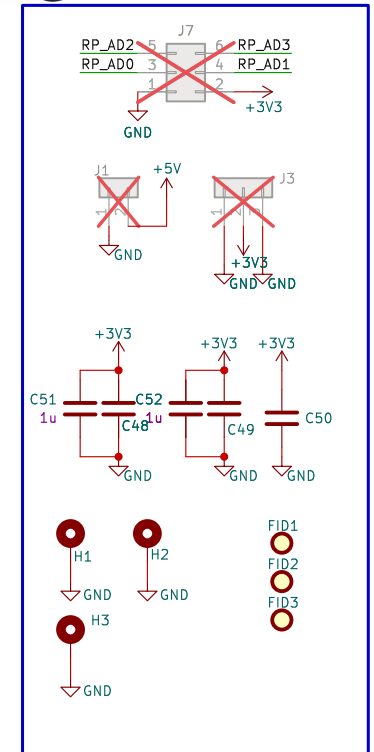
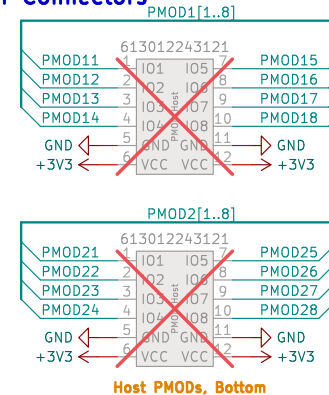


Output and External

7-segment Display



User Connectors



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Psychogenic Technologies for efabless

Sheet: /
File: ChiplgniteExplain.kicad_sch

Title: Chiplgnite Explain

Size: A4 Date: 2025-02-21
KiCad E.D.A. 8.0.8

Rev: 1.1
Id: 1/3

RP2040 and Support

IOVDD □ IOVDD

Logic supply, nominally 3v3.

BOOT_MODE □ QSPL_SS

When held low on powerup, flash SS determines boot mode
(HIGH == flash boot, LOW == USB device)

USB_VDD supplies USB PHY, nominal 3v3. If IOVDD is 3v3, can share supply.

In fact, in this and many applications, IOVDD, USB_VDD and ADC_AVDD are all powered directly from a single 3v3 supply, with the 1v1 digital core being handle by on-board regulator.

VREG_VOUT: Int core regulator, 1.1V
Can supply DVDD
Place 1uF in/out bypass near pin.

RP2
Right of FPGA
Orient 1>
Top Right

CDONE up here

MOSI
MISO
CS
SCK
SPI CRAM

J10 Short to hold in reset

RUN

GND

QSPL_SD0

QSPL_SS

QSPL_CLK

QSPL_SD1

+3V3

Flash program header
Note: should we replace 3v3 with RUN, to be able to reset/hold while updating flash?

RP2 xtal must be "exactly" 12MHz.
Recommended is ABM8-272-T3
Cload 10pF
Maybe go with ABM8W-12.0000MHZ-7-81U-T3
Cload 7pF
for 10ppm rather than 30ppm stab.

Rule of thumb
C1, C2 = 2 * CL - 2 * Cstray
Using a stray cap of 5pF, gives
Cn = 4pF

Into:
 $CL = (C1 * C2) / (C1 + C2) + Cstray$
These Cn = 4pF give
CL = 7pF -- just what we need.

WE 830108206909:
CFPX-180 model
10 ppm tol, 20ppm stab
CL 8pF

SWCLKD 24
SWDIO 25

TESTEN 19

GND Factory test mode: GND

GND

GND

GND

GND

GND

GND

GND

GND

GND

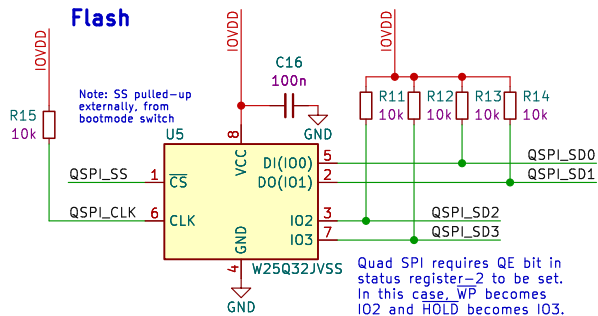
GND

GND

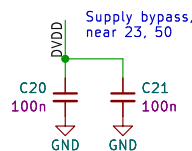
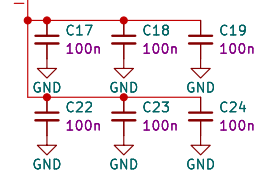
GND

GND

Flash



Supply bypass, place near 1, 10, 22, 33, 42, 49



GPIO	F1	F2	F3	F4	F5	F6	F7	F8	F9
0	SPI0 RX	UART0 TX	I2C0 SDA	PWM0 A	SIO	PI00	PI01		USB OVCUR DET
1	SPI0 CSn	UART0 RX	I2C0 SCL	PWM0 B	SIO	PI00	PI01		USB VBUS DET
2	SPI0 SCK	UART0 CTS	I2C1 SDA	PWM1 A	SIO	PI00	PI01		USB VBUS EN
3	SPI0 TX	UART0 RTS	I2C1 SCL	PWM1 B	SIO	PI00	PI01		USB OVCUR DET
4	SPI0 RX	UART1 TX	I2C0 SDA	PWM2 A	SIO	PI00	PI01		USB VBUS DET
5	SPI0 CSn	UART1 RX	I2C0 SCL	PWM2 B	SIO	PI00	PI01		USB VBUS EN
6	SPI0 SCK	UART1 CTS	I2C1 SDA	PWM3 A	SIO	PI00	PI01		USB OVCUR DET
7	SPI0 TX	UART1 RTS	I2C1 SCL	PWM3 B	SIO	PI00	PI01		USB VBUS DET
8	SPI1 RX	UART1 TX	I2C0 SDA	PWM4 A	SIO	PI00	PI01		USB VBUS EN
9	SPI1 CSn	UART1 RX	I2C0 SCL	PWM4 B	SIO	PI00	PI01		USB OVCUR DET
10	SPI1 SCK	UART1 CTS	I2C1 SDA	PWM5 A	SIO	PI00	PI01		USB VBUS DET
11	SPI1 TX	UART1 RTS	I2C1 SCL	PWM5 B	SIO	PI00	PI01		USB VBUS EN
12	SPI1 RX	UART0 TX	I2C0 SDA	PWM6 A	SIO	PI00	PI01		USB OVCUR DET
13	SPI1 CSn	UART0 RX	I2C0 SCL	PWM6 B	SIO	PI00	PI01		USB VBUS DET
14	SPI1 SCK	UART0 CTS	I2C1 SDA	PWM7 A	SIO	PI00	PI01		USB VBUS EN
15	SPI1 TX	UART0 RTS	I2C1 SCL	PWM7 B	SIO	PI00	PI01		USB OVCUR DET
16	SPI0 RX	UART0 TX	I2C0 SDA	PWM0 A	SIO	PI00	PI01		USB VBUS DET
17	SPI0 CSn	UART0 RX	I2C0 SCL	PWM0 B	SIO	PI00	PI01		USB VBUS EN
18	SPI0 SCK	UART0 CTS	I2C1 SDA	PWM1 A	SIO	PI00	PI01		USB OVCUR DET
19	SPI0 TX	UART0 RTS	I2C1 SCL	PWM1 B	SIO	PI00	PI01		USB VBUS DET
20	SPI0 RX	UART1 TX	I2C0 SDA	PWM2 A	SIO	PI00	PI01	CLOCK GPIN0	USB VBUS EN
21	SPI0 CSn	UART1 RX	I2C0 SCL	PWM2 B	SIO	PI00	PI01	CLOCK GPIN1	USB OVCUR DET
22	SPI0 SCK	UART1 CTS	I2C1 SDA	PWM3 A	SIO	PI00	PI01	CLOCK GPIN2	USB VBUS DET
23	SPI0 TX	UART1 RTS	I2C1 SCL	PWM3 B	SIO	PI00	PI01	CLOCK GPIN3	USB VBUS EN
24	SPI1 RX	UART1 TX	I2C0 SDA	PWM4 A	SIO	PI00	PI01	CLOCK GPIN4	USB OVCUR DET
25	SPI1 CSn	UART1 RX	I2C0 SCL	PWM4 B	SIO	PI00	PI01	CLOCK GPIN5	USB VBUS DET
26	SPI1 SCK	UART1 CTS	I2C1 SDA	PWM5 A	SIO	PI00	PI01		USB VBUS EN
27	SPI1 TX	UART1 RTS	I2C1 SCL	PWM5 B	SIO	PI00	PI01		USB OVCUR DET
28	SPI1 RX	UART0 TX	I2C0 SDA	PWM6 A	SIO	PI00	PI01		USB VBUS DET
29	SPI1 CSn	UART0 RX	I2C0 SCL	PWM6 B	SIO	PI00	PI01		USB VBUS EN

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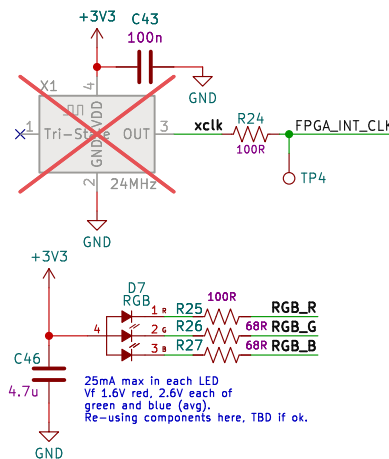
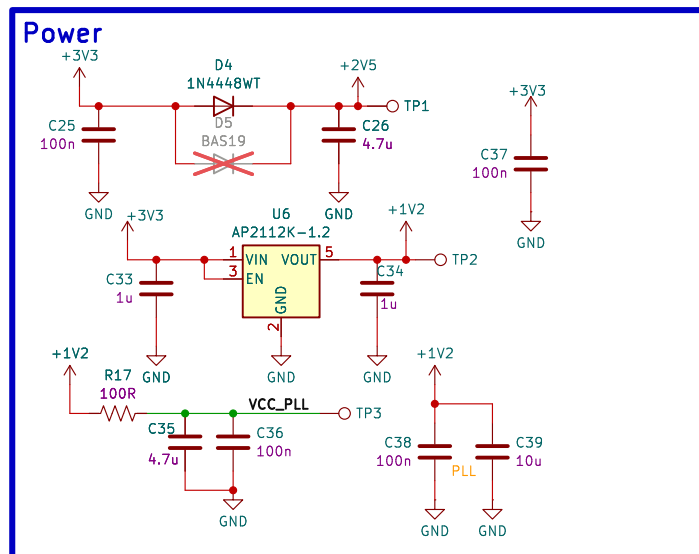
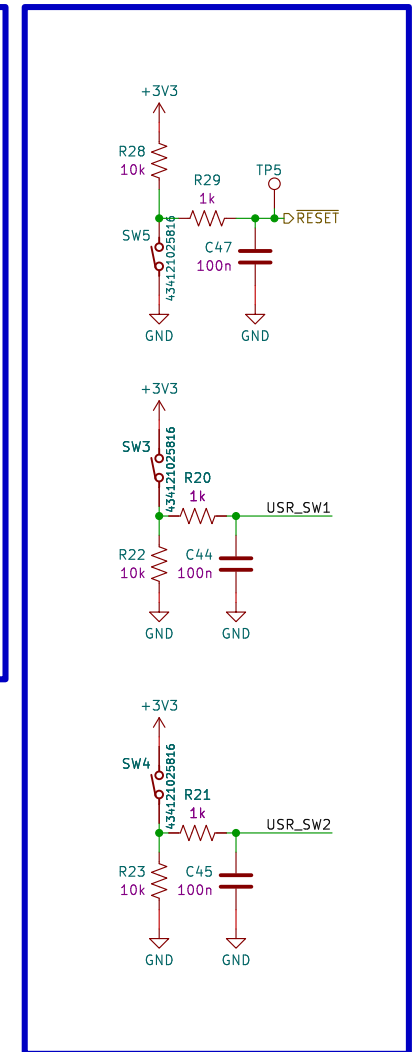
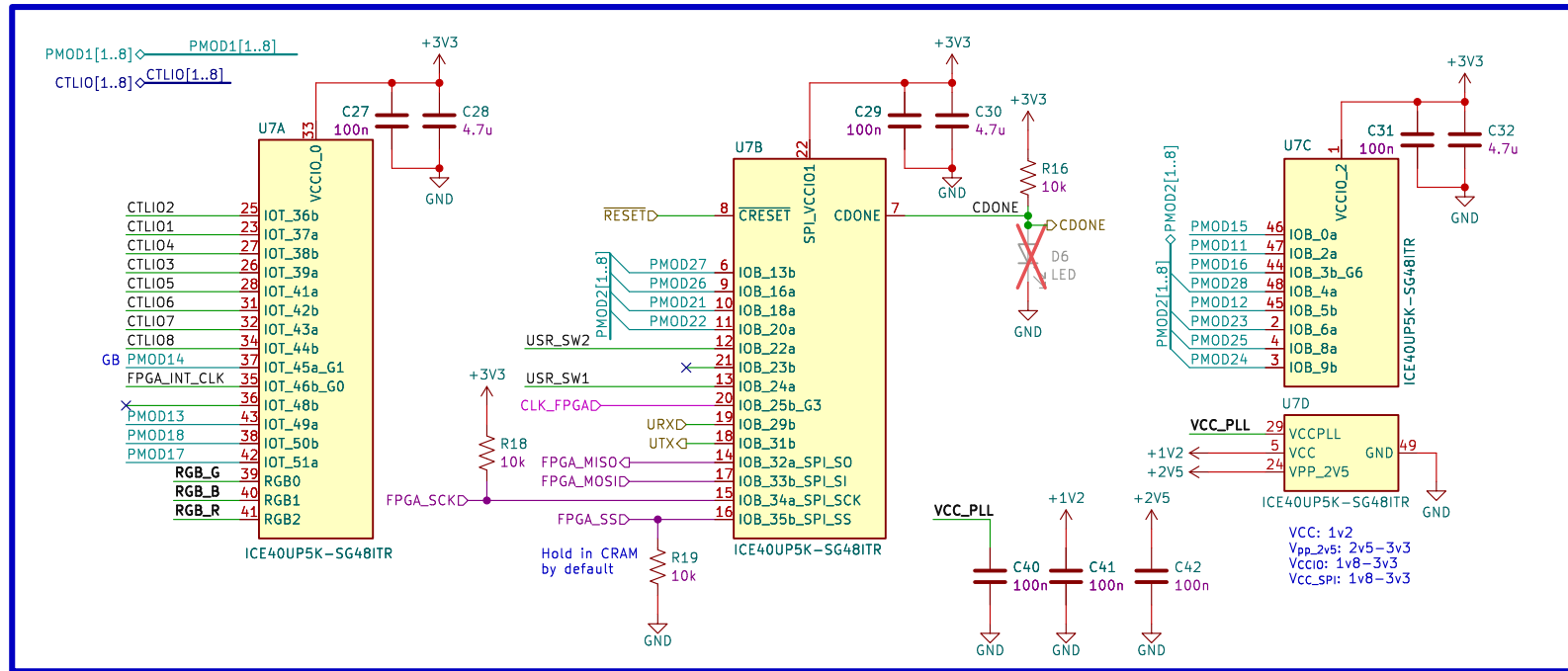
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Rev: 1.0

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UP5K FPGA and Support



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Rev:

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