

Standard NeuroMem Open Source architecture (4 clusters x 32 neurons → 128) (~ 480 LUT/neuron, does not fit on ZYNQ7020)

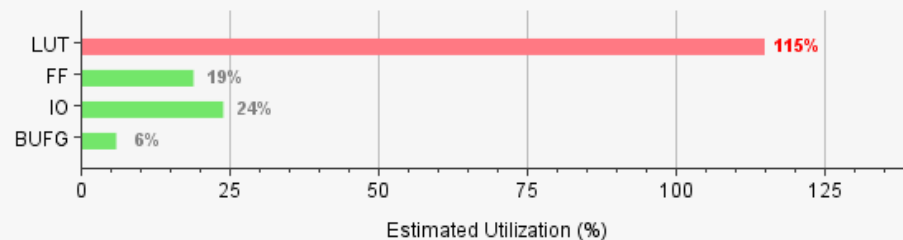
C:/Users/Guy/X_projects/NeuroMem2018/NeuroMem2018.runs/synth_1/nm_top_utilization_synth.rpt

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	60945	0	53200	114.56
LUT as Logic	60945	0	53200	114.56
LUT as Memory	0	0	17400	0.00
Slice Registers	20521	0	106400	19.29
Register as Flip Flop	20521	0	106400	19.29
Register as Latch	0	0	106400	0.00
F7 Muxes	1688	0	26600	6.35
F8 Muxes	0	0	13300	0.00

Utilization

Post-Synthesis | Post-Implementation

Graph | Table



FTGA NeuroMem low cost architecture (4 clusters x 32 neurons → 128) (~ 350 LUT/neuron, ZYNQ7020 extra 16% space available for feature extraction)

C:/Users/Guy/X_projects/FTGA_ZYNQ_7020/FTGA_ZYNQ_7020.runs/synth_1/nm_top_utilization_synth.rpt

30	+-----+-----+-----+-----+-----+				
31	Site Type	Used	Fixed	Available	Util%
32	+-----+-----+-----+-----+-----+				
33	Slice LUTs*	44870	0	53200	84.34
34	LUT as Logic	44870	0	53200	84.34
35	LUT as Memory	0	0	17400	0.00
36	Slice Registers	18342	0	106400	17.24
37	Register as Flip Flop	18342	0	106400	17.24
38	Register as Latch	0	0	106400	0.00
39	F7 Muxes	24	0	26600	0.09
40	F8 Muxes	0	0	13300	0.00
41	+-----+-----+-----+-----+-----+				

Utilization

Post-Synthesis | Post-Implementation

Graph | Table

