Proposal for bandgap-referenced PoR development for the Efabless 2024 Chipalooza challenge

IP Block name: *bandgap-referenced PoR*
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Circuit description:
Basic circuit description from the specification. Elaborate if needed.

A low-complexity bandgap-referenced Power-on-Reset (POR) circuit is proposed to take advantage of comparator hysteresis and offset voltages to achieve both power-on-reset (POR) and brown-out reset (BOR) functions. THe circuit is implemented in the open skywater 130nm process with power consumption of less than 6uW.

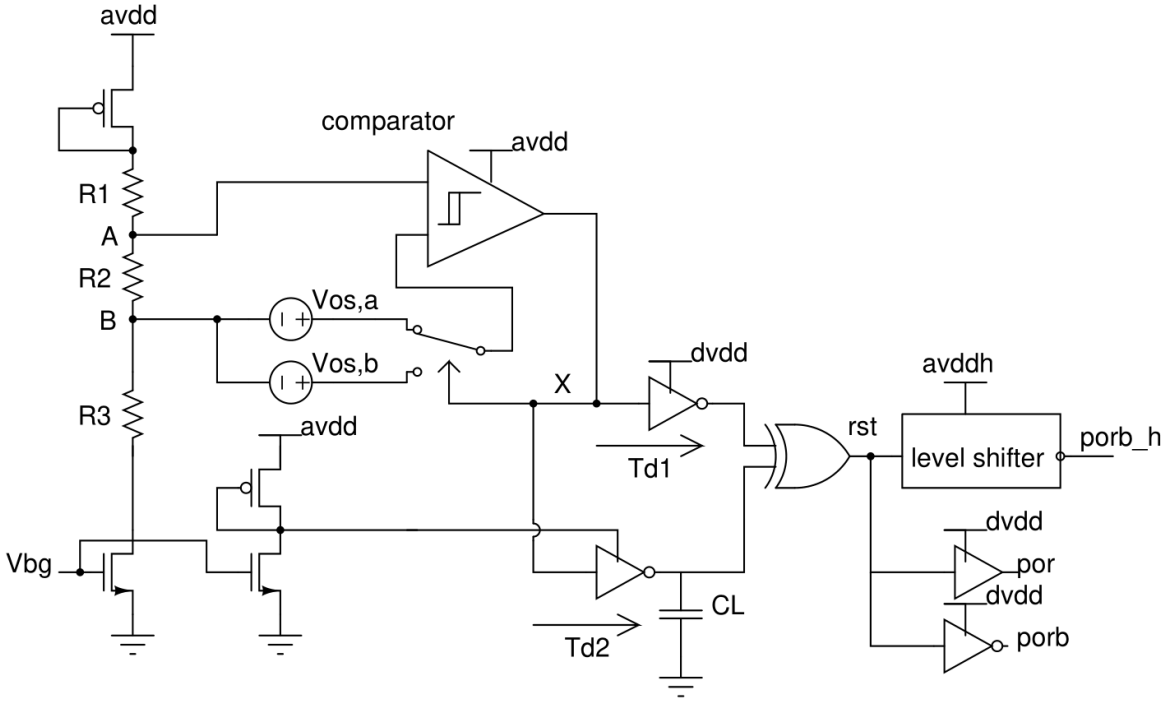

Figure 1. Proposed POR architecture based on offset voltages

The above figure shows the proposed POR circuit.The two input offset voltages, $V_{os,a}$ and $V_{os,b}$ of the comparator working in the subthreshold region is set by the size ratio of k between input differential-pair transistors.

In the POR phase, when the *avdd* powering up, the voltage difference, $V_A - V_B$ between A and B nodes, increases from 0 to $V_{os,a}$, and then X node voltage is locked to high. The *rst* pulse signal is achieved by two different delay paths. Meanwhile, the offset voltage is switched to $V_{os,b}$.

For the BOR phase, when there is a glitch in avdd, the comparator output becomes low. The comparator hysteresis window is equal to $V_{os,a} - V_{os,b}$.

Circuit pinout:

Note any changes from the specification, such as if trim bits have been added.

PIN NAME	Default	Use
avdd	3.3	Analog VDD
avddh	5	Analog VDD
avss	0	Analog ground
dvdd	1.8	Digital VDD
dvss	0	Digital ground
vbg	1.2	Input bandgap reference
por	reset	Active high
porb	Reset bar	Active low
porb_h	Reset bar	Active low for avddh
por_test	Reset testing signal	Testing purpose

Circuit architecture:

Describe the underlying architecture, citing any sources used. Sources must be public and may not contain patented material.

External resources (if any) (all resources must be open source):

No external resources needed.

Specification challenges:
List all specifications which may be difficult to attain, and what circuit design methods will be used to meet those specifications. Note where specifications will be affected by layout considerations, such as mismatch, crosstalk, and I-R drop.

- Low power consumption is challenging

Testbenches required for verifying circuit performance:
List what testbenches are used for each of the electrical parameters to be tested, and briefly describe the testbench circuit setup and how it measures the specified parameter.

Testbenches:

- Transient analysis with PVT to check the reset pulse width, temperature insensitive, and power supply rejection
- Monte carlo simulation to check comparator hysteresis

Connections required for standalone (breakout) implementation:

There is no need for standalone testing.

Test plan for standalone (breakout) implementation:

Buffer the por signal to a digital testing pad for testing purposes.