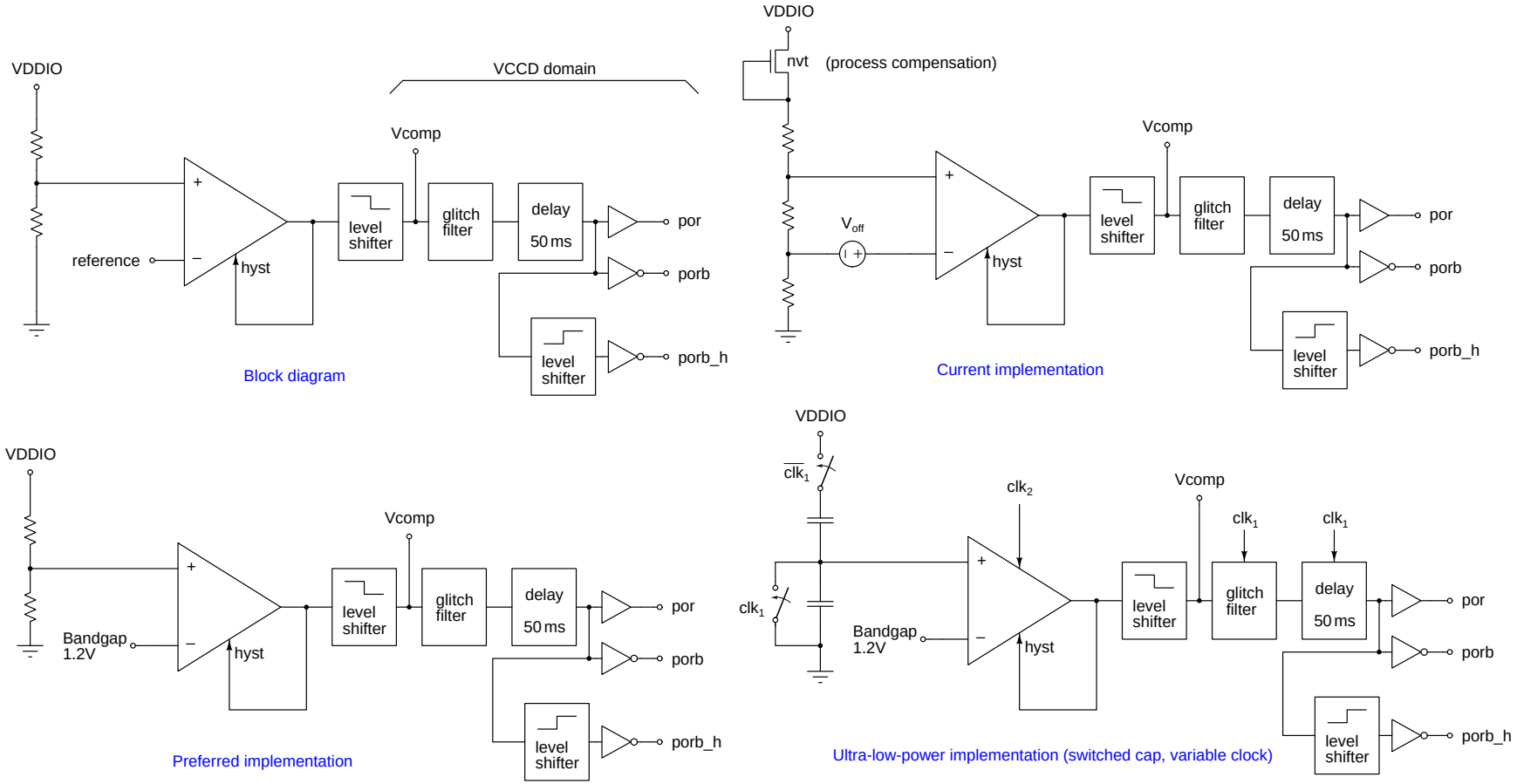
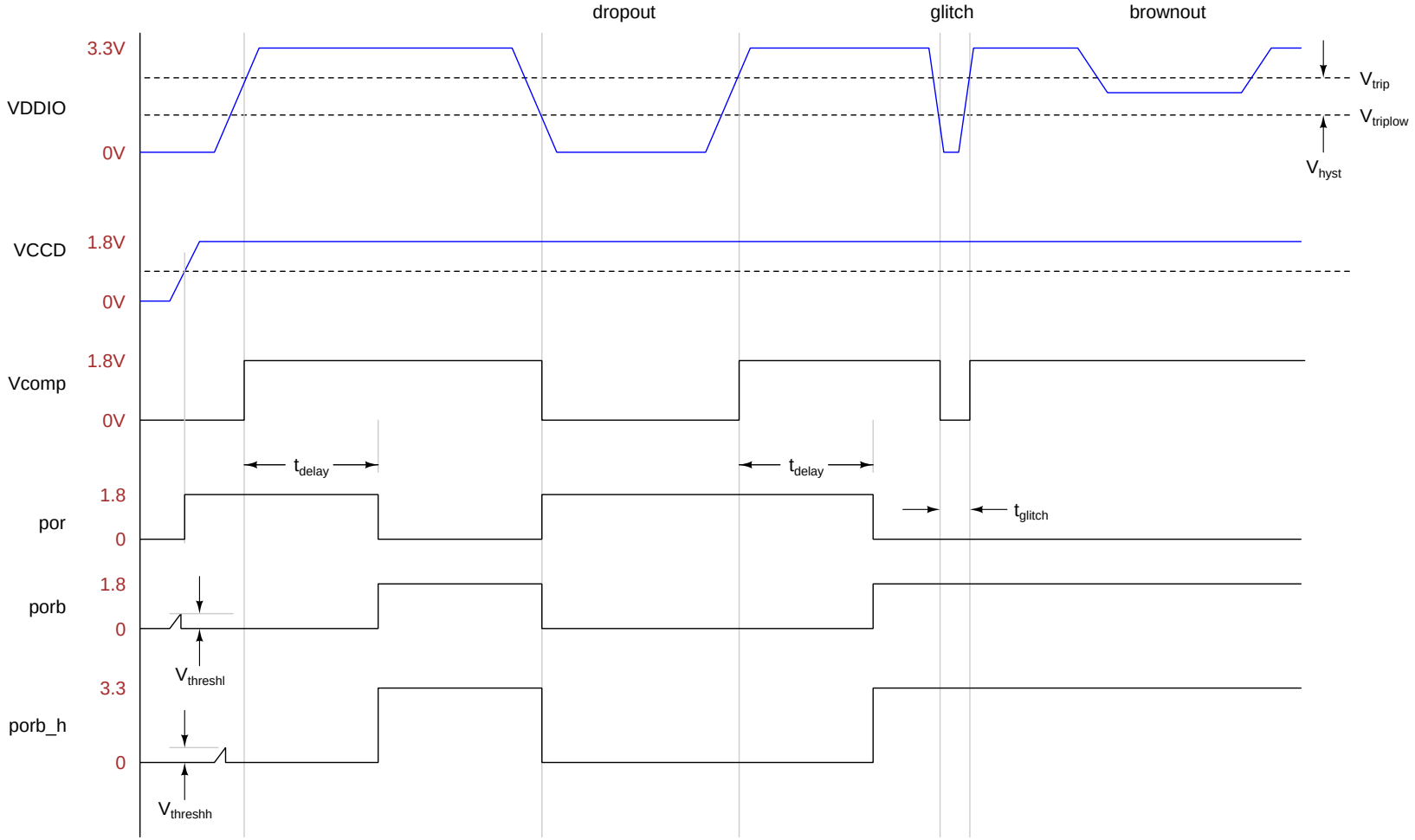
Power-on Reset circuit implementation



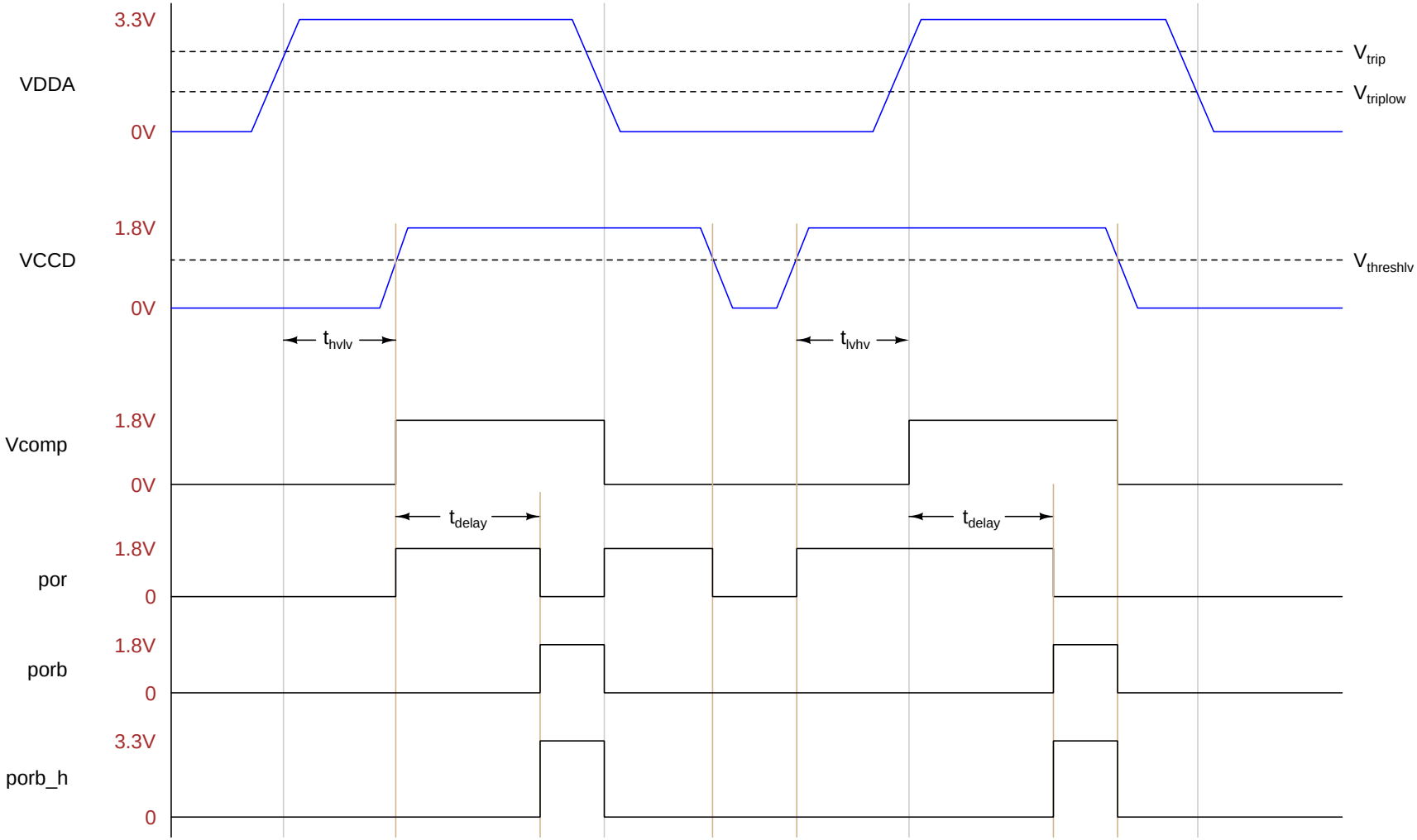
1. V_{off} offset is effectively implemented inside the comparator by using an asymmetric input stage.
2. Ultra-low-power implementation replaces the resistor voltage divider with a sampled capacitive voltage divider.

Power-on-reset behavior—Dropout levels and glitch rejection



1. A glitch is defined when VDDIO < $V_{triplow}$ for a duration less that t_{glitch}
2. A brownout condition is defined as V_{trip} > VDDIO > V_{hyst}
3. por is low when VDDIO is low only when VCCD is also low (see next page)
4. porb is expected to follow VCCD to some maximum level $V_{threshl}$ before it asserts low.
5. porb_h is expected to follow VCCIO to some maximum level $V_{threshh}$ before it asserts low.
6. This diagram shows behavior when VCCD is applied prior to VDDIO and remains high during a VDDIO dropout. This is not necessarily a common use case.

Power-on-reset behavior—Order of power supplies



1. Vcomp output cannot operate when VCCD is below $V_{threshlv}$.
2. por cannot assert when VCCD is low; therefore porb is recommended to drive chip asynchronous reset.