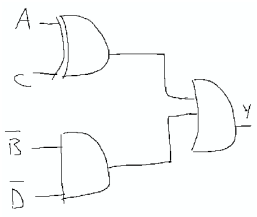
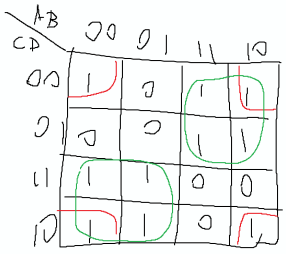


CS223 – DIGITAL DESIGN

HOMEWORK # 1

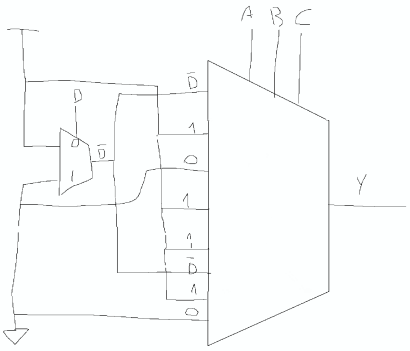


Q1. Given the Boolean function $F(A,B,C,D) = \sum(0,2,3,6,7,8,9,10,12,13)$

(a) Find a minimal Boolean equation for the function by using Karnaugh map method only (don't use Boolean algebra). $\bar{A}C + A\bar{C} + \bar{B}\bar{D}$ $A \oplus C + \bar{B}\bar{D}$

(b) Draw a circuit diagram implementing the function **F** using logic gates (the complements of input variables are available).

(c) Implement the function **F** by using only a 8:1 multiplexer and a 2:1 multiplexer (the complements of input variables are **NOT** available, do not use any other logic gate. Logic levels **1 and 0** are available)



Q2. Simplify the following equations using the theorems of Boolean algebra.

(a) $Y = \overline{(A+B)}\,\overline{(\bar{B}\cdot C)}$ $A + \bar{B} + C$

(b) $Y = \bar{A}BC + D\bar{B} + C\bar{D} + ABCD$ $C + \bar{B}D$

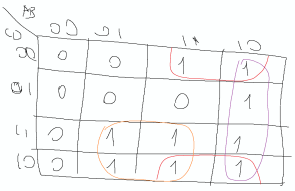
$B\bar{C} + C\bar{D} + \bar{B}D$ $+\bar{B}DC$

Q3. Write the following Boolean equations in product-of-sums (POS) canonical form.

(a) $Y(A,B,C,D) = \bar{A}\,\bar{B} + BC + \bar{B}\,\bar{C}\,D$ $(A+\bar{B}+C+D)(A+\bar{B}+C+\bar{D})(\bar{A}+B+C+D)(\bar{A}+B+\bar{C}+D)(\bar{A}+B+\bar{C}+\bar{D})(A+B+C+D)(A+B+\bar{C}+D)(A+B+C+\bar{D})$

(b) $Y(A,B,C) = \bar{A}\,\bar{B}\,\bar{C} + A\,\bar{B}\,\bar{C} + \bar{A}\,B\,\bar{C} + \bar{A}\,\bar{B}\,C$ $(A+\bar{B}+\bar{C})(\bar{A}+B+\bar{C})(\bar{A}+\bar{B}+C)(\bar{A}+\bar{B}+\bar{C})$

Q4. Simplify the following equation using the Karnaugh map method.

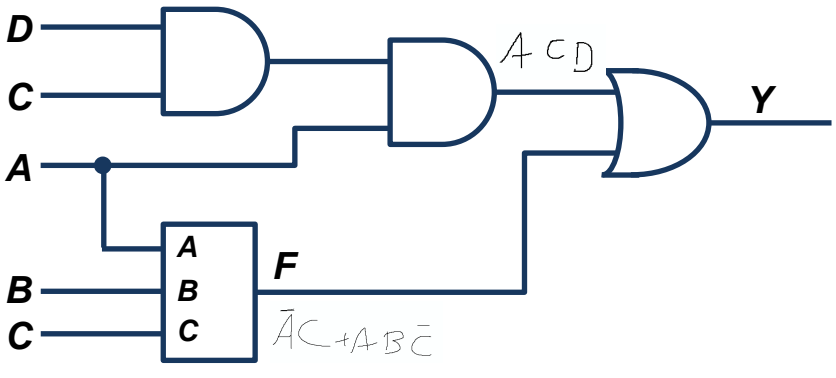


$$Y = B\,C + A\,C + A\,\bar{B} + A\,B\,\bar{C}\,\bar{D}$$

$B\bar{C} + A\bar{B} + A\bar{D}$

Q5. You are given the following circuit and the Boolean function F defined by the truth table.

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0



Find a **minimal** Boolean equation for the output of the circuit $Y(A,B,C,D)$.

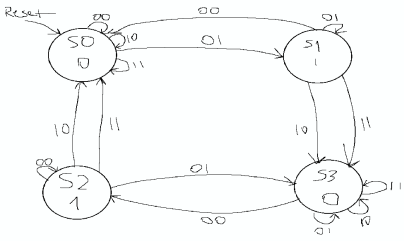
$\bar{A}C + CD + A\bar{B}\bar{C}$

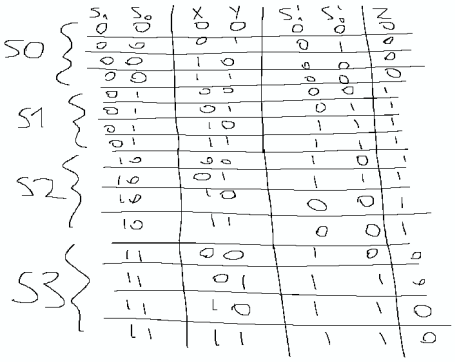
Q6. A sequential circuit with two state variables S_1 and S_0 has two inputs **X** and **Y**. The boolean equations for next state logic and output logic functions are given as follows;

$$S_0' = \overline{X}\,Y + XS_0$$

$$S_1' = \overline{X}S_1 + XS_0$$

$$z = S_0 \oplus S_1$$





(a) Write the state transition table

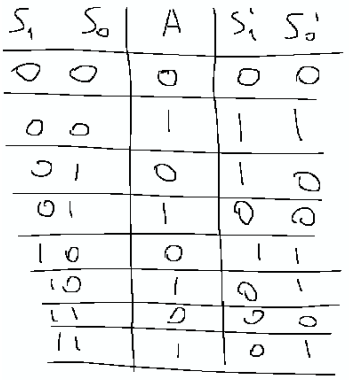
(b) Draw state transition diagram

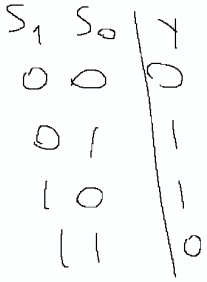
Q7. A sequential circuit design with input A and output Y is shown in the following diagram.

(a) Write the state transition and output tables with binary encodings.

(b) Write the Boolean equations for the next-state and output logic.

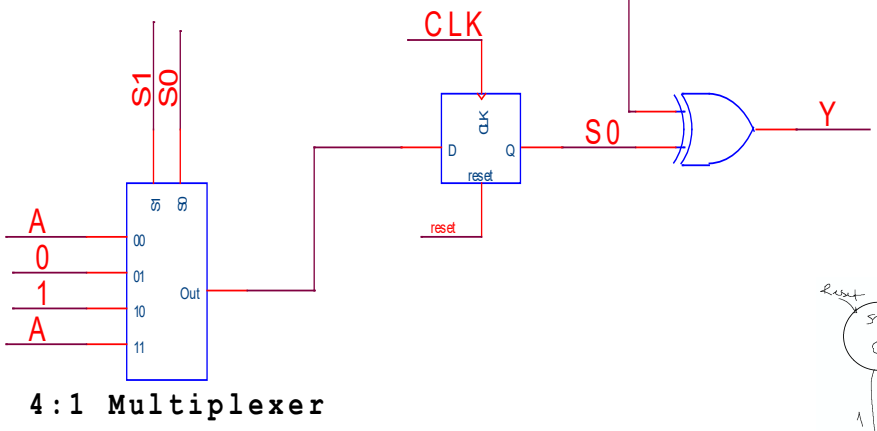
(c) Sketch the state transition diagram.

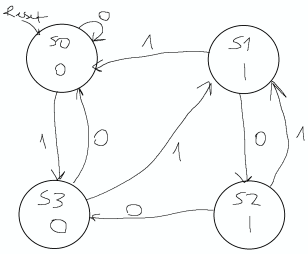


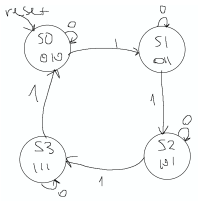


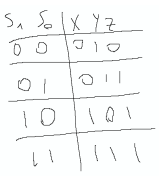
$$S_0' = S_1\bar{A} + \bar{S}_0 A + S_1\bar{S}_0$$

$$S_1' = \bar{S}_1\bar{S}_0 A + \bar{S}_1 S_0 \bar{A} + S_1\bar{S}_0\bar{A}$$









$S_0' = S_0\bar{B} + \bar{S}_0 B$

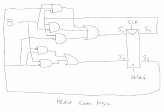
$S_1' = S_1\bar{B} + S_1\bar{S}_0 + \bar{S}_1 S_0 B$

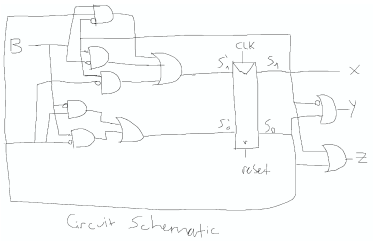
$X = S_1$

$Y = \bar{S}_1 + S_0$

$Z = S_1 + S_0$

Q8. Design a sequential circuit with input **B** and three outputs **xyz** which is used as a counter that counts through the **3-bit prime numbers**.





Circuit Schematic

On reset circuit outputs are xyz=010.

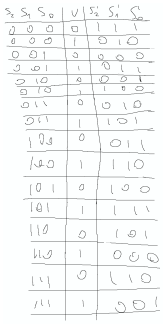
If B=0, output will not change, else if B=1 output will change as follows

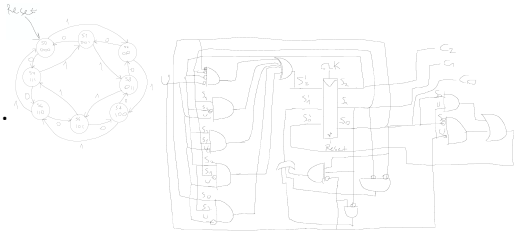
011, 101, 111, 010, 011, 101, 111, 010, ...

Show the state diagram and state table of FSM, use binary encoding for the states.

Write next state equations and output equations, implement the **next state logic**, **sketch** the circuit schematic.

Q9. Design a Finite State Machine (FSM) which has a one-bit input $\boldsymbol{U}$ and **three-bit** output $\boldsymbol{C}$. If $\boldsymbol{U} = \mathbf{1}$, the circuit will count up two-by-two and if $\boldsymbol{U} = \mathbf{0}$, the circuit will count down one-by-one. The circuit will count up as follows: 0, 2, 4, 6, 0, 2, 4, 6, ... or 1, 3, 5, 7, 1, 3, 5, 7, ... and it will count down as follows: 0, 7, 6, 5, 4, 3, 2, 1, 0, 7, 6, 5, 4, ... On reset, its output will be $\mathbf{000}$.



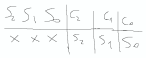


(a) Sketch the state transition diagram.

(b) Write the state transition and output tables with binary encodings.

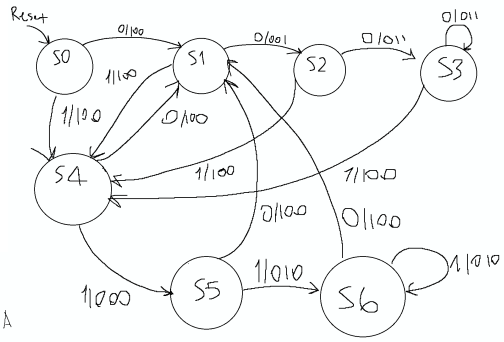
(c) Write the Boolean equations for the next-state and output logic.

(d) Sketch the circuit schematic for the FSM.



$S_0' = \bar{S}_0\bar{U} + S_0 U \quad C_2 = S_2 \quad C_1 = S_1 \quad C_0 = S_0$

Q10. Design a Finite State Machine (FSM) with one input and one output. The circuit should read one-bit data at every rising edge of the clock. According to the data input, the circuit will produce the following output. On reset, its output will be $\mathbf{100}$.



If the input bit sequence is $\mathbf{11}$ then the output will be $\mathbf{000}$.

If the input bit sequence is $\mathbf{00}$ then the output will be $\mathbf{001}$.

If the input bit sequence is $\mathbf{111}$ then the output will be $\mathbf{010}$.

If the input bit sequence is $\mathbf{000}$ then the output will be $\mathbf{011}$.

Otherwise, the output will be $\mathbf{100}$.

$S_2' = A$

$S_1' = \bar{S}_1 S_0 \bar{A} + \bar{S}_2 S_1 \bar{A} + S_2 S_0 A + S_2 S_1 A$

$S_2' = \bar{S}_0 \bar{A} + S_1 \bar{A} + S_2 \bar{A} + S_2 \bar{S}_1 \bar{S}_0$

(a) Sketch the state transition diagram.

(b) Write the state transition and output tables with binary encodings.

(c) Write the Boolean equations for the next-state and output logic.

(d) Sketch the circuit schematic for the FSM.