

## CS223 – DIGITAL DESIGN

### HOMEWORK # 1

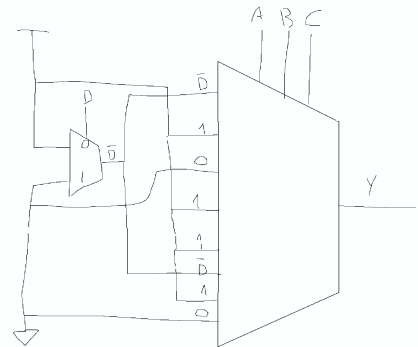
AB \ CD	00	01	11	10
00	1	0	1	1
01	0	0	1	1
11	1	1	0	0
10	1	1	0	1

**Q1.** Given the Boolean function  $F(A, B, C, D) = \sum(0, 2, 3, 6, 7, 8, 9, 10, 12, 13)$

- Find a minimal Boolean equation for the function by using Karnaugh map method only (don't use Boolean algebra).  $\bar{A}C + \bar{A}\bar{C} + \bar{B}\bar{D} \quad (A \oplus 1) + (\bar{B}\bar{D})$
- Draw a circuit diagram implementing the function  $F$  using logic gates (the complements of input variables are available).
- Implement the function  $F$  by using only a 8:1 multiplexer and a 2:1 multiplexer (the complements of input variables are **NOT** available, do not use any other logic gate. Logic levels **1** and **0** are available)

**Q2.** Simplify the following equations using the theorems of Boolean algebra.

- $Y = \overline{(A+B)}(\overline{B \cdot C}) \quad A + B + C$
- $Y = \bar{A}BC + D\bar{B} + C\bar{D} + ABCD \quad C + \bar{B}D$   
 $BC + C\bar{D} + \bar{B}D \quad (+ \bar{B}D)$



**Q3.** Write the following Boolean equations in product-of-sums (POS) canonical form.

- $Y(A, B, C, D) = \bar{A}\bar{B} + BC + \bar{B}\bar{C}D \quad (\bar{A} + \bar{B} + C + D)(\bar{A} + \bar{B} + C + \bar{D})(\bar{A} + B + C + D)(\bar{A} + B + C + \bar{D})(\bar{A} + B + \bar{C} + D)(\bar{A} + B + \bar{C} + \bar{D})$
- $Y(A, B, C) = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C \quad (\bar{A} + \bar{B} + \bar{C})(\bar{A} + B + \bar{C})(\bar{A} + \bar{B} + C)(\bar{A} + B + C)$

**Q4.** Simplify the following equation using the Karnaugh map method.

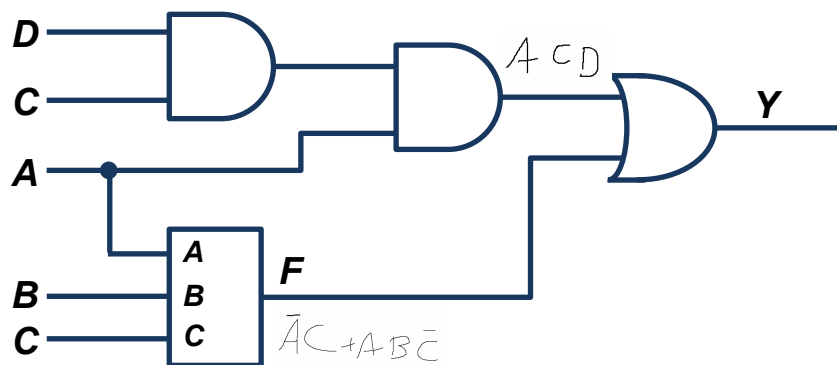
$$Y = BC + AC + A\bar{B} + AB\bar{C}\bar{D}$$

$$BC + A\bar{B} + A\bar{D}$$

AB \ CD	00	01	11	10
00	0	0	1	1
01	0	0	0	1
11	0	1	1	1
10	0	1	1	1

**Q5.** You are given the following circuit and the Boolean function  $F$  defined by the truth table.

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0



Find a **minimal** Boolean equation for the output of the circuit  $Y(A, B, C, D)$ .

$$\bar{A}C + CD + A\bar{B}\bar{C}$$

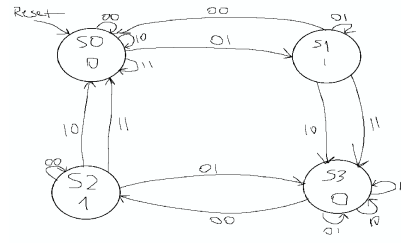
**Q6.** A sequential circuit with two state variables  $S_1$  and  $S_0$  has two inputs  $X$  and  $Y$ . The boolean equations for next state logic and output logic functions are given as follows;

$$S_0' = \bar{X}Y + XS_0$$

$$S_1' = \bar{X}S_1 + XS_0$$

$$z = S_0 \oplus S_1$$

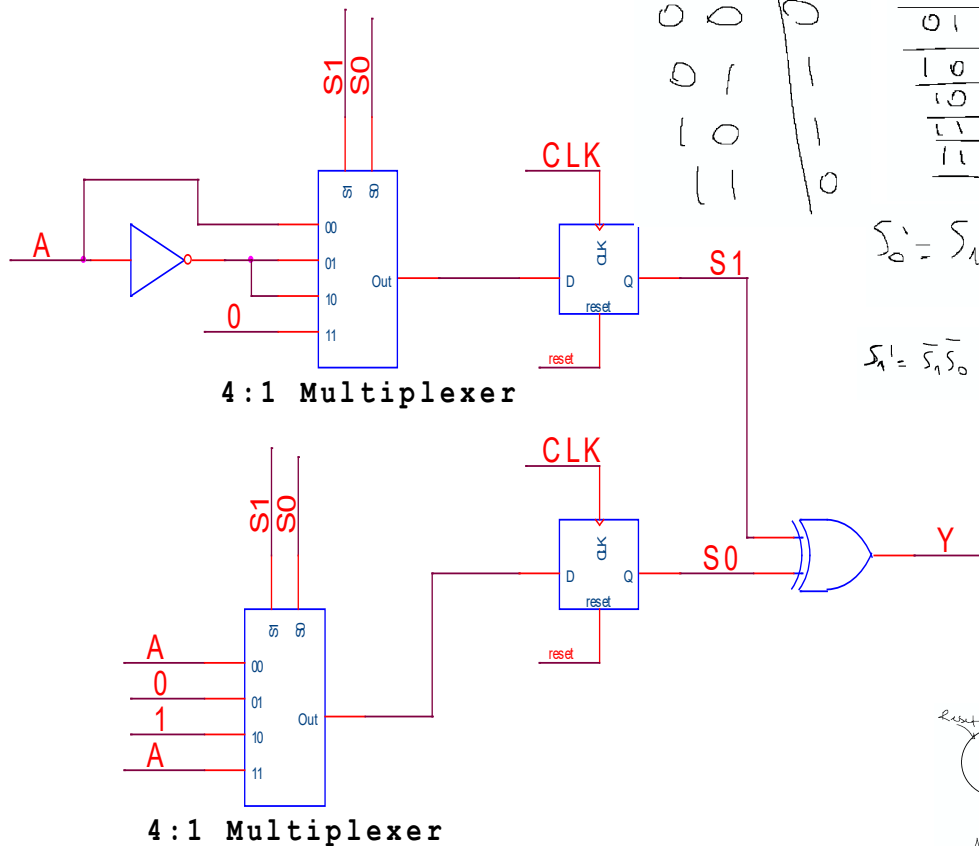
- (a) Write the state transition table  
(b) Draw state transition diagram



$S_1$	$S_0$	$X$	$Y$	$S_1'$	$S_0'$	$Z$
0	0	0	0	0	0	0
0	0	0	1	0	1	1
0	0	1	0	1	0	1
0	0	1	1	1	1	0
0	1	0	0	0	0	0
0	1	0	1	0	1	1
0	1	1	0	1	0	1
0	1	1	1	1	1	0
1	0	0	0	0	0	0
1	0	0	1	0	1	1
1	0	1	0	1	0	1
1	0	1	1	1	1	0
1	1	0	0	0	0	0
1	1	0	1	0	1	1
1	1	1	0	1	0	1
1	1	1	1	1	1	0

**Q7.** A sequential circuit design with input  $A$  and output  $Y$  is shown in the following diagram.

- (a) Write the state transition and output tables with binary encodings.  
(b) Write the Boolean equations for the next-state and output logic.  
(c) Sketch the state transition diagram.

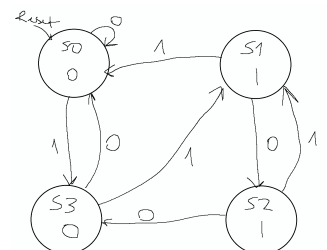


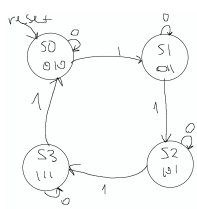
$S_1$	$S_0$	$Y$
0	0	0
0	1	1
1	0	1
1	1	0

$S_1$	$S_0$	$A$	$S_1'$	$S_0'$
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	0	1

$$S_0' = S_1 A + \bar{S}_0 A + S_1 \bar{S}_0$$

$$S_1' = \bar{S}_1 \bar{S}_0 A + \bar{S}_1 S_0 \bar{A} + S_1 \bar{S}_0 \bar{A}$$





$S_1$	$S_0$	$B$	$S_1'$	$S_0'$
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

$S_1$	$S_0$	$X$	$Y$	$Z$
0	0	0	1	0
0	1	0	1	1
1	0	1	0	1
1	1	1	1	1

$$S_0' = S_0 \bar{B} + \bar{S}_0 B$$

$$S_1' = S_1 \bar{B} + S_1 \bar{S}_0 + \bar{S}_1 S_0 B$$

$$X = S_1$$

$$Y = \bar{S}_1 + S_0$$

$$Z = S_1 + S_0$$

**Q8.** Design a sequential circuit with input **B** and three outputs **xyz** which is used as a counter that counts through the **3-bit prime numbers**.

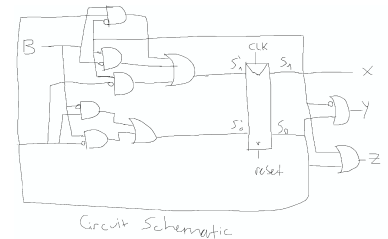
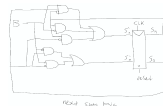
On reset circuit outputs are **xyz=010**.

If **B=0**, output will not change, else if **B=1** output will change as follows

**011, 101, 111, 010, 011, 101, 111, 010, ....**

Show the state diagram and state table of FSM, use binary encoding for the states.

**Write** next state equations and output equations, implement the **next state logic**, sketch the circuit schematic.



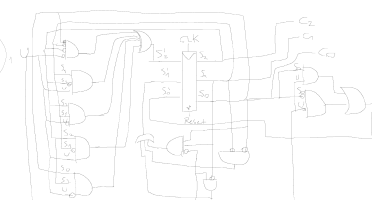
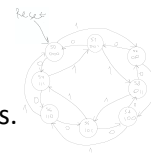
**Q9.** Design a Finite State Machine (FSM) which has a one-bit input **U** and **three-bit** output **C**. If **U = 1**, the circuit will count up two-by-two and if **U = 0**, the circuit will count down one-by-one. The circuit will count up as follows: 0, 2, 4, 6, 0, 2, 4, 6, ... or 1, 3, 5, 7, 1, 3, 5, 7, ... and it will count down as follows: 0, 7, 6, 5, 4, 3, 2, 1, 0, 7, 6, 5, 4, ... On reset, its output will be **000**.

(a) Sketch the state transition diagram.

(b) Write the state transition and output tables with binary encodings.

(c) Write the Boolean equations for the next-state and output logic.

(d) Sketch the circuit schematic for the FSM.



$S_2$	$S_1$	$S_0$	$U$	$S_2'$	$S_1'$	$S_0'$
0	0	0	0	0	0	0
0	0	0	1	0	1	0
0	0	1	0	0	0	0
0	0	1	1	0	1	1
0	1	0	0	0	1	0
0	1	0	1	1	1	0
0	1	1	0	0	0	1
0	1	1	1	1	0	1
1	0	0	0	0	1	1
1	0	0	1	1	1	1
1	0	1	0	1	0	1
1	0	1	1	0	0	0
1	1	0	0	1	1	0
1	1	0	1	0	0	1
1	1	1	0	1	1	1
1	1	1	1	0	0	0

$S_2$	$S_1$	$S_0$	$C_2$	$C_1$	$C_0$
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

$$S_2' = \bar{S}_2 \bar{S}_1 \bar{S}_0 U + \bar{S}_2 \bar{S}_1 U + \bar{S}_2 S_1 \bar{S}_0 U + \bar{S}_2 S_1 S_0 U$$

$$S_1' = \bar{S}_2 \bar{S}_0 U + S_2 U$$

$$S_0' = \bar{S}_2 \bar{S}_0 U + S_2 \bar{S}_0 U$$

$$C_2 = S_2 \quad C_1 = S_1 \quad C_0 = S_0$$

**Q10.** Design a Finite State Machine (FSM) with one input and one output. The circuit should read one-bit data at every rising edge of the clock. According to the data input, the circuit will produce the following output. On reset, its output will be **100**.

If the input bit sequence is **11** then the output will be **000**.

If the input bit sequence is **00** then the output will be **001**.

If the input bit sequence is **111** then the output will be **010**.

If the input bit sequence is **000** then the output will be **011**.

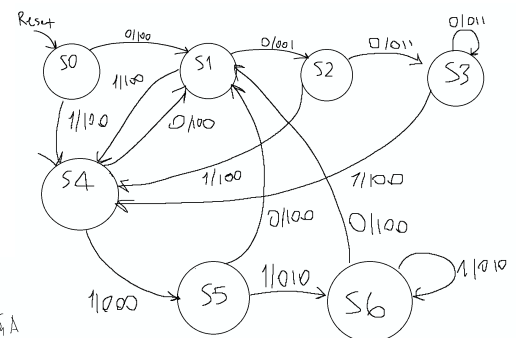
Otherwise, the output will be **100**.

(a) Sketch the state transition diagram.

(b) Write the state transition and output tables with binary encodings.

(c) Write the Boolean equations for the next-state and output logic.

(d) Sketch the circuit schematic for the FSM.



$$S_0' = A$$

$$S_1' = \bar{S}_2 \bar{S}_0 \bar{A} + \bar{S}_2 S_1 \bar{A} + S_2 \bar{S}_0 A + S_2 S_1 A$$

$$S_2' = \bar{S}_0 \bar{A} + S_1 \bar{A} + S_2 \bar{A} + S_2 S_1 \bar{S}_0$$

$S_2$	$S_1$	$S_0$	$A$	$S_2'$	$S_1'$	$S_0'$
0	0	0	0	0	0	1
0	0	0	1	0	0	0
0	0	1	0	0	1	0
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	0	1	1	0	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	1	0	0
1	0	0	1	1	0	1
1	0	1	0	0	0	1
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	1	0	0
1	1	1	0	1	1	0
1	1	1	1	0	0	0

States	$A$	$B_2$	$B_1$	$B_0$
S0	0	1	0	0
S1	0	1	0	0
S2	0	1	0	1
S3	0	1	0	0
S4	0	1	0	0
S5	0	1	0	0
S6	0	1	0	0
S7	0	1	0	0
S8	0	1	0	0
S9	0	1	0	0
S10	0	1	0	0
S11	0	1	0	0
S12	0	1	0	0
S13	0	1	0	0
S14	0	1	0	0
S15	0	1	0	0
S16	0	1	0	0
S17	0	1	0	0
S18	0	1	0	0
S19	0	1	0	0
S20	0	1	0	0
S21	0	1	0	0
S22	0	1	0	0
S23	0	1	0	0
S24	0	1	0	0
S25	0	1	0	0
S26	0	1	0	0
S27	0	1	0	0
S28	0	1	0	0
S29	0	1	0	0
S30	0	1	0	0
S31	0	1	0	0
S32	0	1	0	0
S33	0	1	0	0
S34	0	1	0	0
S35	0	1	0	0
S36	0	1	0	0
S37	0	1	0	0
S38	0	1	0	0
S39	0	1	0	0
S40	0	1	0	0
S41	0	1	0	0
S42	0	1	0	0
S43	0	1	0	0
S44	0	1	0	0
S45	0	1	0	0
S46	0	1	0	0
S47	0	1	0	0
S48	0	1	0	0
S49	0	1	0	0
S50	0	1	0	0
S51	0	1	0	0
S52	0	1	0	0
S53	0	1	0	0
S54	0	1	0	0
S55	0	1	0	0
S56	0	1	0	0
S57	0	1	0	0
S58	0	1	0	0
S59	0	1	0	0
S60	0	1	0	0
S61	0	1	0	0
S62	0	1	0	0
S63	0	1	0	0
S64	0	1	0	0
S65	0	1	0	0
S66	0	1	0	0
S67	0	1	0	0
S68	0	1	0	0
S69	0	1	0	0
S70	0	1	0	0
S71	0	1	0	0
S72	0	1	0	0
S73	0	1	0	0
S74	0	1	0	0
S75	0	1	0	0
S76	0	1	0	0
S77	0	1	0	0
S78	0	1	0	0
S79	0	1	0	0
S80	0	1	0	0
S81	0	1	0	0
S82	0	1	0	0
S83	0	1	0	0
S84	0	1	0	0
S85	0	1	0	0
S86	0	1	0	0
S87	0	1	0	0
S88	0	1	0	0
S89	0	1	0	0
S90	0	1	0	0
S91	0	1	0	0
S92	0	1	0	0
S93	0	1	0	0
S94	0	1	0	0
S95	0	1	0	0
S96	0	1	0	0
S97	0	1	0	0
S98	0	1	0	0
S99	0	1	0	0
S100	0	1	0	0
S101	0	1	0	0
S102	0	1	0	0
S103	0	1	0	0
S104	0	1	0	0
S105	0	1	0	0
S106	0	1	0	0
S107	0	1	0	0
S108	0	1	0	0
S109	0	1	0	0
S110	0	1	0	0
S111	0	1	0	0
S112	0	1	0	0
S113	0	1	0	0
S114	0	1	0	0
S115	0	1	0	0
S116	0	1	0	0
S117	0	1	0	0
S118	0	1	0	0
S119	0	1	0	0
S120	0	1	0	0
S121	0	1	0	0
S122	0	1	0	0
S123	0	1	0	0
S124	0	1	0	0
S125	0	1	0	0
S126	0	1	0	0
S127	0	1	0	0
S128	0	1	0	0
S129	0	1	0	0
S130	0	1	0	0
S131	0	1	0	0
S132	0	1	0	0
S133	0	1	0	0
S134	0	1	0	0
S135	0	1	0	0
S136	0	1	0	0
S137	0	1	0	0
S138	0	1	0	0
S139	0	1	0	0
S140	0	1	0	0
S141	0	1	0	0
S142	0	1	0	0
S143	0	1	0	0
S144	0	1	0	0
S145	0	1	0	0
S146	0	1	0	0
S147	0	1	0	0
S148	0	1	0	0
S149	0	1	0	0
S150	0	1	0	0
S151	0	1	0	0
S152	0	1	0	0
S153	0	1	0	0
S154	0	1	0	0
S155	0	1	0	0
S156	0	1	0	0
S157	0	1	0	0
S158	0	1	0	0
S159	0	1	0	0
S160	0	1	0	0
S161	0	1	0	0
S162	0	1	0	0
S163	0	1	0	0
S164	0	1	0	0
S165	0	1	0	0
S166	0	1	0	0
S167	0	1	0	0
S168	0	1	0	0
S169	0	1	0	0
S170	0	1	0	0
S171	0	1	0	0
S172	0	1	0	0
S173	0	1	0	0
S174	0	1	0	0
S175	0	1	0	0
S176	0	1	0	0
S177	0	1	0	0
S178	0	1	0	0
S179	0	1	0	0
S180	0	1	0	0
S181	0	1	0	0
S182	0	1	0	0
S183	0	1	0	0
S184	0	1	0	0
S185	0	1	0	0
S186	0	1	0	0
S187	0	1	0	0
S188	0	1	0	0
S189	0	1	0	0
S190	0	1	0	0
S191	0	1	0	0
S192	0	1	0	0