

**CS224**

**Section No: 1**

**Spring 2021**

**Lab No: 6**

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**Report for matrix size 10000:**

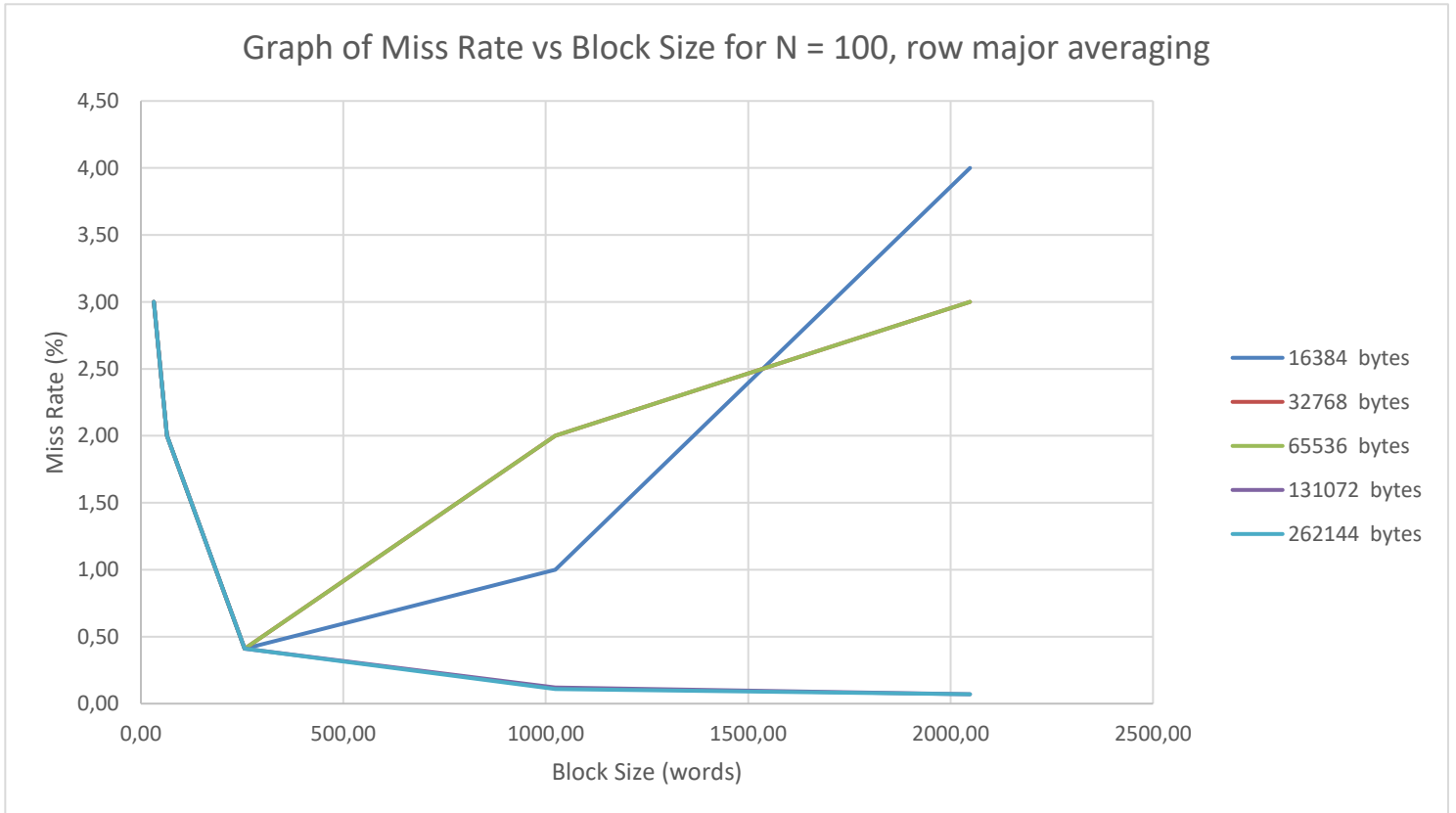
**a) Direct Mapped Caches**

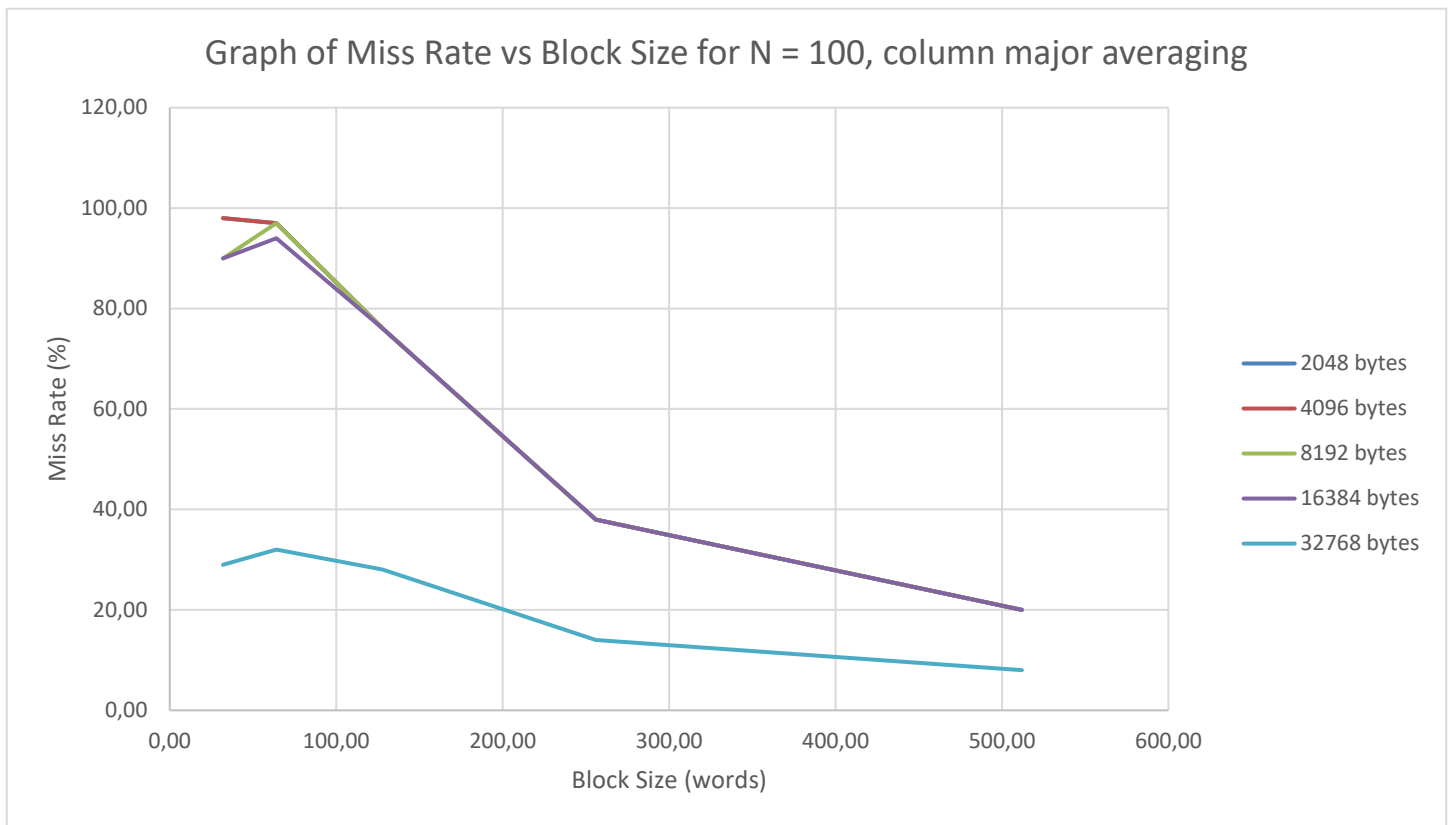
	<b>Block Size 32</b>	<b>Block Size 64</b>	<b>Block Size 256</b>	<b>Block Size 1024</b>	<b>Block Size 2048</b>
<b>Cache Size 16384 bytes</b>	Miss rate: 3% # of misses: 317	Miss rate: 2% # of misses: 160	Miss rate: 0.41% # of misses: 42	Miss rate: 1% # of misses: 101	Miss rate: 4% # of misses: 410
<b>Cache Size 32768 bytes</b>	Miss rate: 3% # of misses: 313	Miss rate: 2% # of misses: 160	Miss rate: 0.41% # of misses: 42	Miss rate: 2% # of misses: 160	Miss rate: 3% # of misses: 317
<b>Cache Size 65536 bytes</b>	Miss rate: 3% # of misses: 321	Miss rate: 2% # of misses: 160	Miss rate: 0.41% # of misses: 42	Miss rate: 2% # of misses: 162	Miss rate: 3% # of misses: 314
<b>Cache Size 131072 bytes</b>	Miss rate: 3% # of misses: 317	Miss rate: 2% # of misses: 160	Miss rate: 0.41% # of misses: 42	Miss rate: 0.12% # of misses: 12	Miss rate: 0.07% # of misses: 7
<b>Cache Size 262144 bytes</b>	Miss rate: 3% # of misses: 318	Miss rate: 2% # of misses: 160	Miss rate: 0.41% # of misses: 42	Miss rate: 0.11% # of misses: 10	Miss rate: 0.07% # of misses: 7

**Table 1: Table for row major averaging**

	Block Size 32	Block Size 64	Block Size 128	Block Size 256	Block Size 512
<b>Cache Size 16384 bytes</b>	Miss rate: 90% # of misses: 9236	Miss rate: 94% # of misses: 9619	Miss rate: 76% # of misses: 7827	Miss rate: 38% # of misses: 3927	Miss rate: 20% # of misses: 2002
<b>Cache Size 32768 bytes</b>	Miss rate: 29% # of misses: 3025	Miss rate: 32% # of misses: 3314	Miss rate: 28% # of misses: 2901	Miss rate: 14% # of misses: 1476	Miss rate: 8% # of misses: 814
<b>Cache Size 2048 bytes</b>	Miss rate: 98% # of misses: 10004	Miss rate: 97% # of misses: 10003	Miss rate: 76% # of misses: 7818	Miss rate: 38% # of misses: 3918	Miss rate: 20% # of misses: 2002
<b>Cache Size 4096 bytes</b>	Miss rate: 98% # of misses: 10004	Miss rate: 97% # of misses: 10003	Miss rate: 76% # of misses: 7818	Miss rate: 38% # of misses: 3918	Miss rate: 20% # of misses: 2002
<b>Cache Size 8192 bytes</b>	Miss rate: 90% # of misses: 9236	Miss rate: 97% # of misses: 10003	Miss rate: 76% # of misses: 7818	Miss rate: 38% # of misses: 3918	Miss rate: 20% # of misses: 2002

**Table 2: Table for column major averaging**





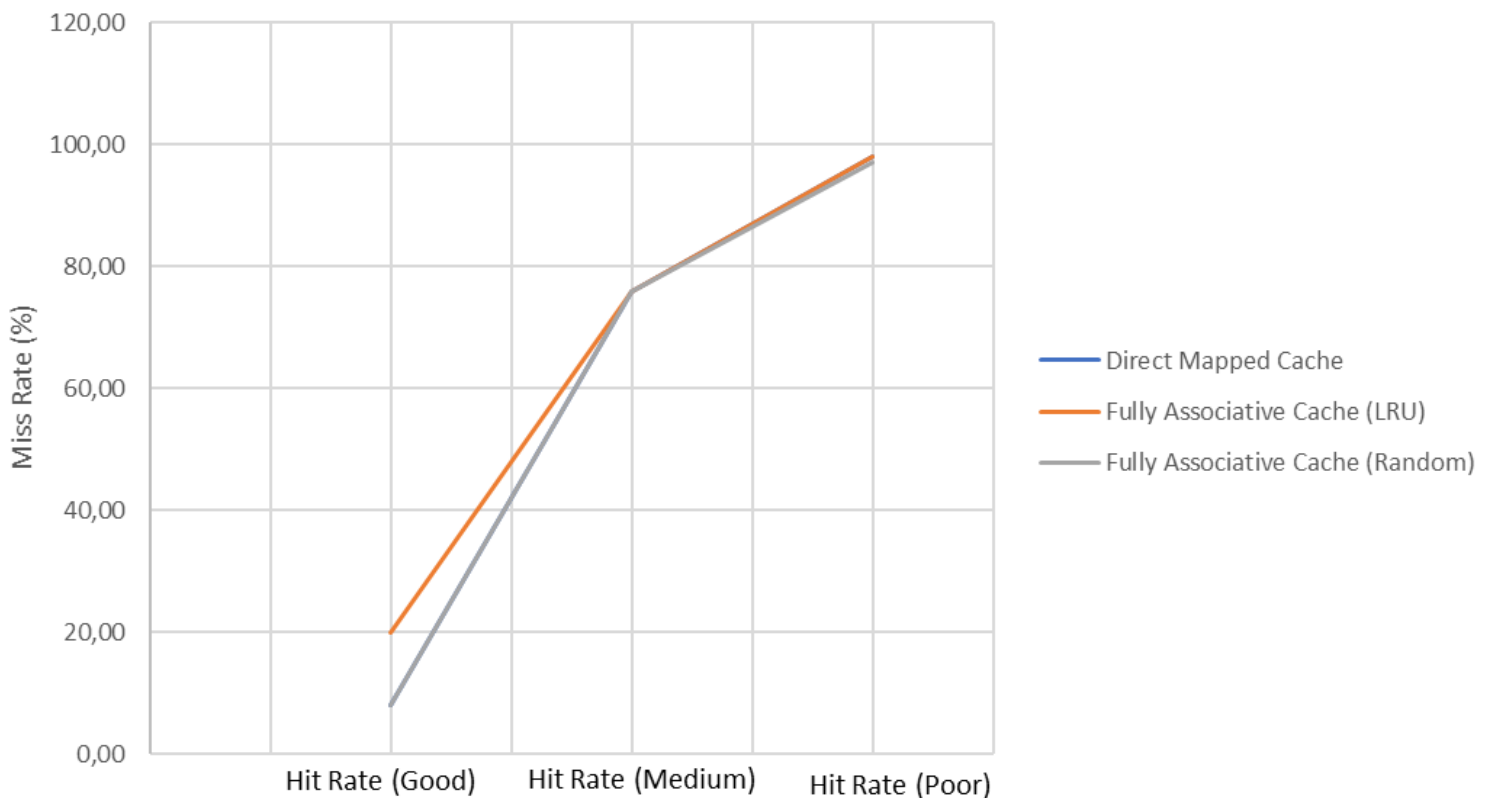
### b) Fully Associative Caches

	Hit Rate (Poor) Cache Size: 2048 bytes Block Size: 32	Hit Rate (Medium) Cache Size: 4096 bytes Block Size: 128	Hit Rate (Good) Cache Size: 32768 bytes Block Size: 512
Direct Mapped Cache	Miss Rate: 98% Number of misses: 10004	Miss Rate: 76% Number of misses: 7818	Miss Rate: 8% Number of misses: 814
Fully Associative Cache (LRU)	Miss Rate: 98% Number of misses: 10004	Miss Rate: 76% Number of misses: 7818	Miss Rate: 20% Number of misses: 4003
Fully Associative Cache (Random)	Miss Rate: 97% Number of misses: 9991	Miss Rate: 76% Number of misses: 7818	Miss Rate: 8% Number of misses: 774

There is a 12% difference between the results of the good hit rate between fully associative cache with LRU and direct mapped cache. Fully associative cache with LRU has a higher miss rate. However, for the medium hit rate, the fully associative cache with LRU and the direct mapped cache have the same miss rates. For the poor hit rate case, they both have the same miss rate of 98%. Overall, the switch from the direct mapped cache to fully associative cache didn't affect the results too much, and the good case got even worse while the other cases remained more or less the same.

When the replacement policy is switched to random, the poor case is almost the same for all caches, and the medium case is also the same. The good case however, has the same miss rate with direct mapped cache and is smaller than fully associative cache with LRU. It is seen that the replacement policy doesn't make a very huge difference in terms of miss rates and only the good case is affected visibly.

Graph for part b, N = 100, column major averaging



### c) N-way Set Associative Caches

	N = 2	N = 4	N = 8	N = 16
Hit Rate (Poor) Cache Size: 2048 bytes Block Size: 32	Hit Rate: 2% Miss Rate: 98% # of misses: 10004	Hit Rate: 2% Miss Rate: 98% # of misses: 10004	Hit Rate: 2% Miss Rate: 98% # of misses: 10004	Hit Rate: 2% Miss Rate: 98% # of misses: 10004

	N = 1	N = 2	N = 4	N = 8
Hit Rate (Medium) Cache Size: 4096 bytes Block Size: 128	Hit Rate: 24% Miss Rate: 76% # of misses: 7827	Hit Rate: 24% Miss Rate: 76% # of misses: 7827	Hit Rate: 24% Miss Rate: 76% # of misses: 7827	Hit Rate: 24% Miss Rate: 76% # of misses: 7827

	N = 2	N = 4	N = 8	N = 16
Hit Rate (Good) Cache Size: 32768 bytes Block Size: 512	Hit Rate: 88% Miss Rate: 12% # of misses: 1210	Hit Rate: 80% Miss Rate: 20% # of misses: 2002	Hit Rate: 80% Miss Rate: 20% # of misses: 2002	Hit Rate: 80% Miss Rate: 20% # of misses: 2002

For poor and medium hit rate conditions, the set size doesn't make a difference and the hit rates stay constant for different set sizes. For the good hit rate conditions, the hit rate is the best with 88% when N = 2. As the set size is increased, the hit rate reduces to 80% and remains constant after.

## Report for matrix size 40000:

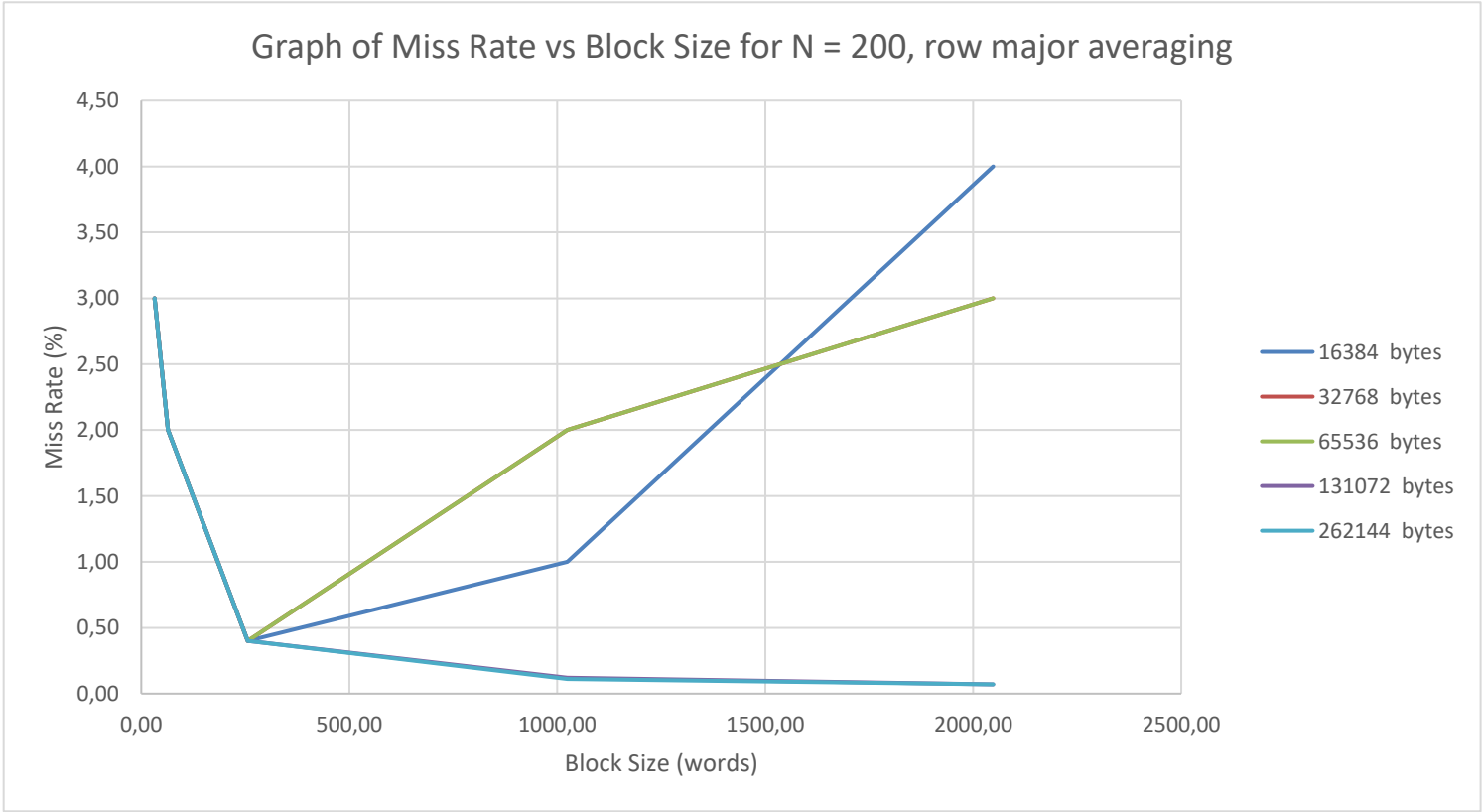
### a) Direct Mapped Caches

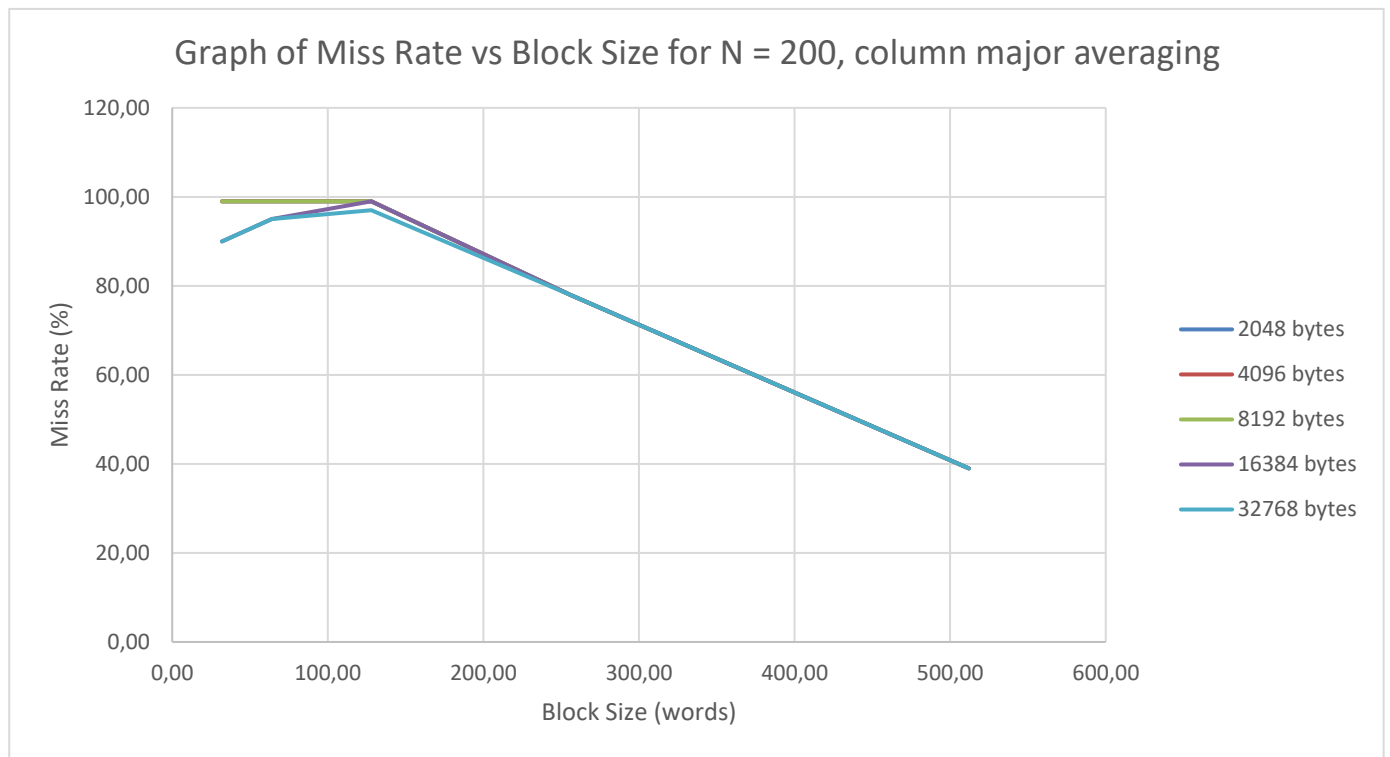
	Block Size 32	Block Size 64	Block Size 256	Block Size 1024	Block Size 2048
<b>Cache Size 16384 bytes</b>	Miss rate: 3% # of misses: 1255	Miss rate: 2% # of misses: 629	Miss rate: 0.4% # of misses: 159	Miss rate: 1% # of misses: 402	Miss rate: 4% # of misses: 1610
<b>Cache Size 32768 bytes</b>	Miss rate: 3% # of misses: 1253	Miss rate: 2% # of misses: 631	Miss rate: 0.4% # of misses: 159	Miss rate: 2% # of misses: 805	Miss rate: 3% # of misses: 1207
<b>Cache Size 65536 bytes</b>	Miss rate: 3% # of misses: 1255	Miss rate: 2% # of misses: 627	Miss rate: 0.4% # of misses: 160	Miss rate: 2% # of misses: 804	Miss rate: 3% # of misses: 1205
<b>Cache Size 131072 bytes</b>	Miss rate: 3% # of misses: 1250	Miss rate: 2% # of misses: 630	Miss rate: 0.4% # of misses: 163	Miss rate: 0.12% # of misses: 48	Miss rate: 0.07% # of misses: 29
<b>Cache Size 262144 bytes</b>	Miss rate: 3% # of misses: 1251	Miss rate: 2% # of misses: 629	Miss rate: 0.4% # of misses: 168	Miss rate: 0.11% # of misses: 42	Miss rate: 0.07% # of misses: 28

**Table 1: Table for row major averaging**

	Block Size 32	Block Size 64	Block Size 128	Block Size 256	Block Size 512
<b>Cache Size 16384 bytes</b>	Miss rate: 90% # of misses: 36434	Miss rate: 95% # of misses: 38221	Miss rate: 99% # of misses: 40002	Miss rate: 78% # of misses: 31291	Miss rate: 39% # of misses: 15666
<b>Cache Size 32768 bytes</b>	Miss rate: 90% # of misses: 36420	Miss rate: 95% # of misses: 38211	Miss rate: 97% # of misses: 39106	Miss rate: 78% # of misses: 31322	Miss rate: 39% # of misses: 15778
<b>Cache Size 2048 bytes</b>	Miss rate: 99% # of misses: 40004	Miss rate: 99% # of misses: 40003	Miss rate: 99% # of misses: 40002	Miss rate: 78% # of misses: 31322	Miss rate: 39% # of misses: 15778
<b>Cache Size 4096 bytes</b>	Miss rate: 99% # of misses: 40004	Miss rate: 99% # of misses: 40003	Miss rate: 99% # of misses: 40002	Miss rate: 78% # of misses: 31322	Miss rate: 39% # of misses: 15778
<b>Cache Size 8192 bytes</b>	Miss rate: 99% # of misses: 40004	Miss rate: 99% # of misses: 40003	Miss rate: 99% # of misses: 40002	Miss rate: 78% # of misses: 31322	Miss rate: 39% # of misses: 15778

**Table 2: Table for column major averaging**



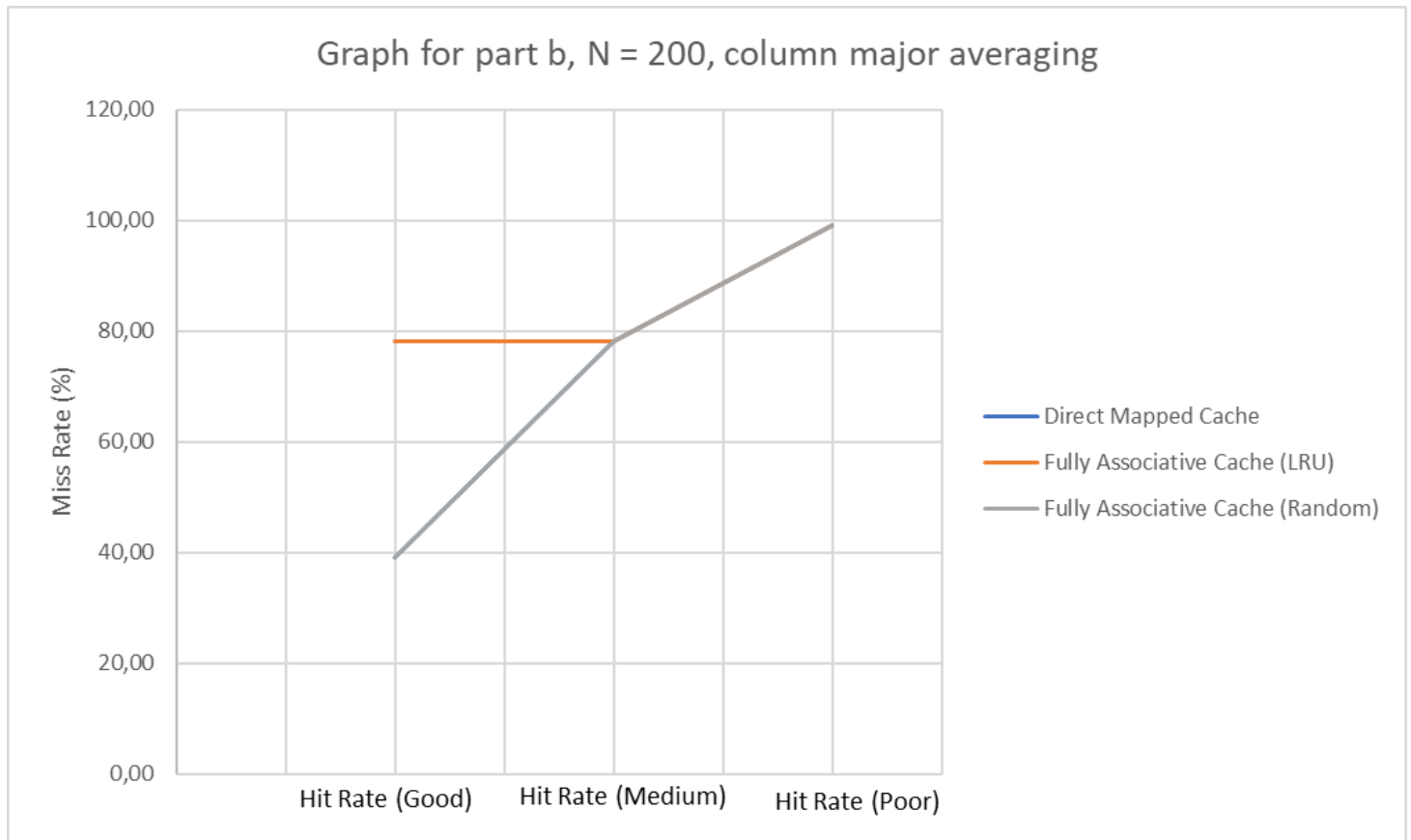


## b) Fully Associative Caches

	Hit Rate (Poor) Cache Size: 2048 bytes Block Size: 32	Hit Rate (Medium) Cache Size: 8192 bytes Block Size: 256	Hit Rate (Good) Cache Size: 16384 bytes Block Size: 512
Direct Mapped Cache	Miss Rate: 99% Number of misses: 40004	Miss Rate: 78% Number of misses: 31322	Miss Rate: 39% Number of misses: 15778
Fully Associative Cache (LRU)	Miss Rate: 99% Number of misses: 40004	Miss Rate: 78% Number of misses: 31322	Miss Rate: 78% Number of misses: 31322
Fully Associative Cache (Random)	Miss Rate: 99% Number of misses: 40004	Miss Rate: 78% Number of misses: 31322	Miss Rate: 39% Number of misses: 15778



For the poor rate conditions, the change to fully associative cache architectures didn't make a difference as the hit rates remained the same. The medium case also remained the same accross both architectures and different replacement policies. For the good hit rate conditions, the fully associative cache with LRU had a higher miss rate than the other ones.



### c) N-way Set Associative Caches

	N = 2	N = 4	N = 8	N = 16
Hit Rate (Poor) Cache Size: 2048 bytes Block Size: 32	Hit Rate: 1% Miss Rate: 99% # of misses: 40004	Hit Rate: 1% Miss Rate: 99% # of misses: 40004	Hit Rate: 1% Miss Rate: 99% # of misses: 40004	Hit Rate: 1% Miss Rate: 99% # of misses: 40004

	N = 1	N = 2	N = 4	N = 8
Hit Rate (Medium) Cache Size: 8192 bytes Block Size: 256	Hit Rate: 22% Miss Rate: 78% # of misses: 31322	Hit Rate: 22% Miss Rate: 78% # of misses: 31322	Hit Rate: 22% Miss Rate: 78% # of misses: 31322	Hit Rate: 22% Miss Rate: 78% # of misses: 31322

	N = 1	N = 2	N = 4	N = 8
Hit Rate (Good) Cache Size: 16384 bytes Block Size: 512	Hit Rate: 61% Miss Rate: 39% # of misses: 15778	Hit Rate: 61% Miss Rate: 39% # of misses: 15778	Hit Rate: 61% Miss Rate: 39% # of misses: 15778	Hit Rate: 61% Miss Rate: 39% # of misses: 15778

For every condition, good, medium and bad, the rates remain the same as the set size is changed. There is no improvement as  $N$  is increased. The good conditions give the best hit rate of 61% for every  $N$ .