CS224

Section No: 1

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Lab No: 6

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1.1)

No.	Cache Size KB	N way cache	Word Size in bits	Block size (no. of words)	No. of sets	Tag Size in bits	Index Size (Set No.) in bits	Word Block Offset Size in bits	Byte Offset Size in bits	Block Replacement Policy Needed (Yes/No)
1	8	1	8	8	1024	16	10	3	0	No
2	8	2	16	8	256	17	8	3	1	Yes
3	8	4	16	4	256	18	8	2	1	Yes
4	8	Full	16	4	1	26	0	2	1	Yes
9	32	1	16	2	8192	14	13	1	1	No
10	32	2	16	2	4096	15	12	1	1	Yes
11	32	4	8	8	1024	16	10	3	0	Yes
12	32	Full	8	8	1	26	0	3	0	Yes

1.2)

a)

Instruction	1	2	3	4	5
lw $t1, 0xA4($0)	Compulsory	Hit	Hit	Hit	Hit
lw $t2, 0xA8($0)	Hit	Hit	Hit	Hit	Hit
lw $t3, 0xAC($0)	Hit	Hit	Hit	Hit	Hit

b)

The byte offset is 2 bits, block offset is also 2 bits and for the index, only 1 bit is needed. So the tag is 27 bits, then there is one valid bit in each set, and 4 words of 32 bits each. As a result, one set has a size of 1 (valid) + 27 (tag) + 32 x 4 (words) = 156 bits.

Since there are two sets, the total number of bits is 156 x 2 = 312 bits. Total cache size is 312 bits.

c)

A 4-1 mux is needed to select the data, one equality comparator is needed to compare tags and an AND gate is required to compare the valid bit and the result of the equality comparator and decide if the word can be taken. As a result, 1 4-1 MUX, 1 comparator and 1 AND gate is needed to implement the cache memory.

1.3)

a)

Instruction	1	2	3	4	5
lw $t1, 0xA4($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t2, 0xA8($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t3, 0xAC($0)	Compulsory	Capacity	Capacity	Capacity	Capacity

b)

For a set, only 1 bit for the LRU policy is needed because N = 2. Since the entire cache has one set, the total number of bits needed for the LRU policy 1.

N = 2 and C = 2, so there is one set in the cache. In this set, one bit for the LRU policy is needed, also 2 bits are needed for the valid bits of the two words. There is only the byte offset of two bits, so the tag is 30 bits and there are two tags for the two words. The two words are 32 bits each. So, the total cache memory size is 1 (LRU) + 2 (valid bits) + 30 x 2 (tags) + 32 x 2 (words) = 127 bits.

c)

Two equality comparators are needed to compare the tags of the two words with the tag of the address that is searched. Two AND gates are needed to compare the V bits and the results of the equality comparators. An OR gate is needed to compare the results of the AND gates to determine if there is a hit. A 2-1 MUX is needed to select between the two words. So, 2 equality comparators, 2 AND gates, 1 OR gate and 1 2-1 MUX is needed.