CSE211 Digital Design

Akdeniz University

Week13: Sequential Logic Part 2

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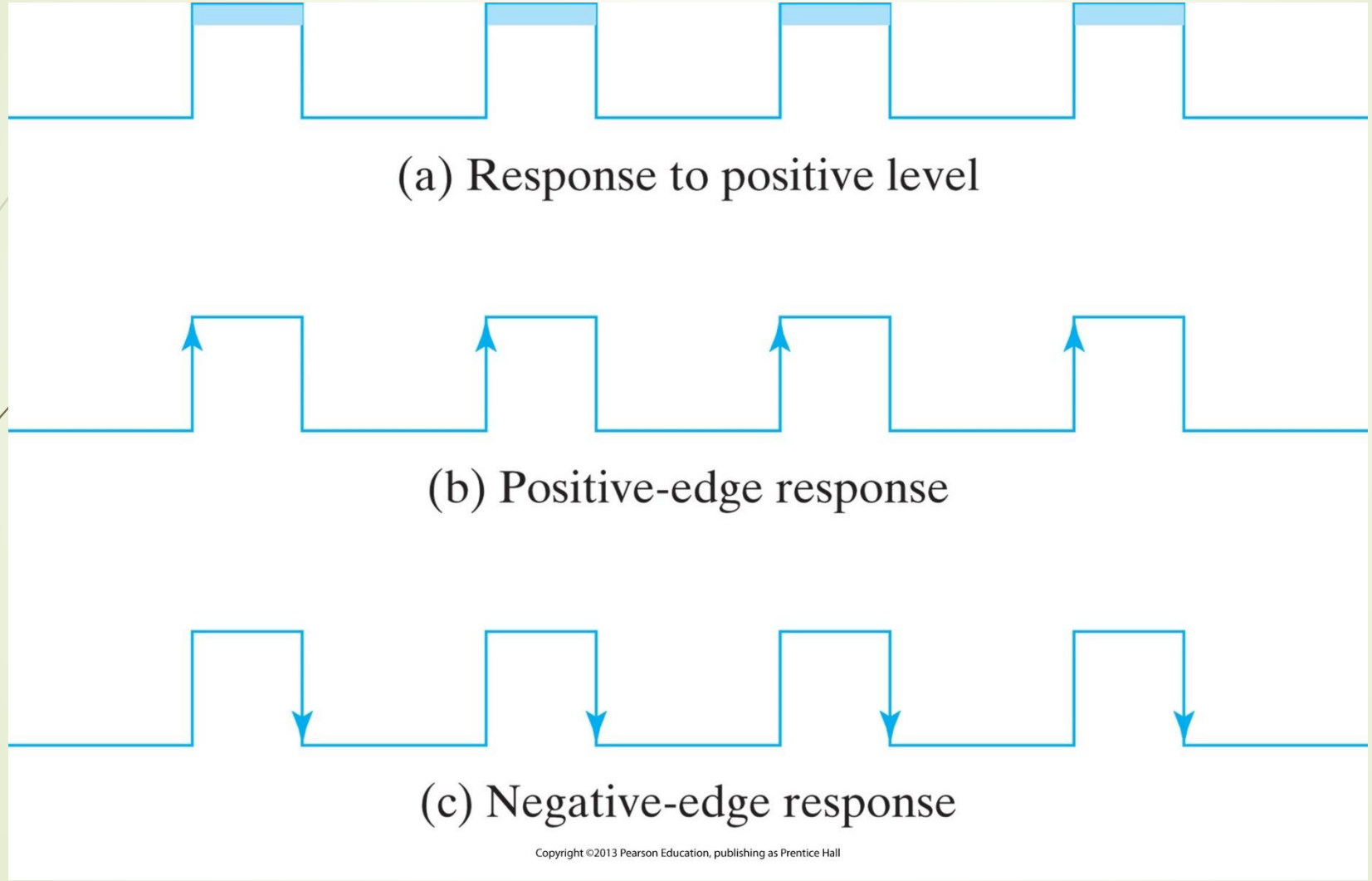
5.4 Storage Elements: Flip-Flops

- The state of a latch or flip-flop is switched by a change in the control input. This momentary change is called a ***trigger***
- The problem with the latch is that it responds to a change in the *level* of a clock pulse. Glitches are problematic.

Clock response in latch and flip-flop

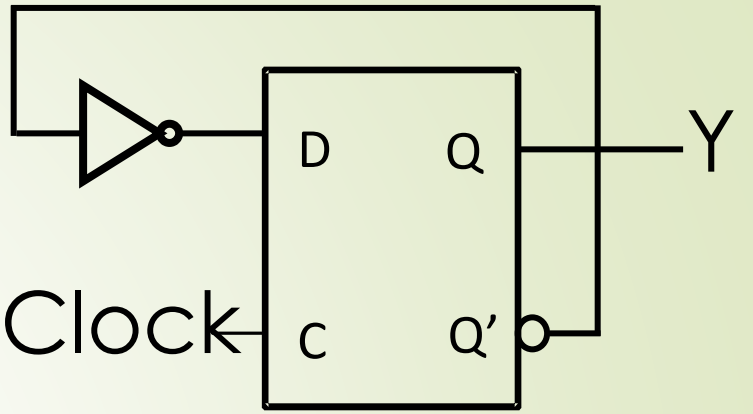


Flip-Flops

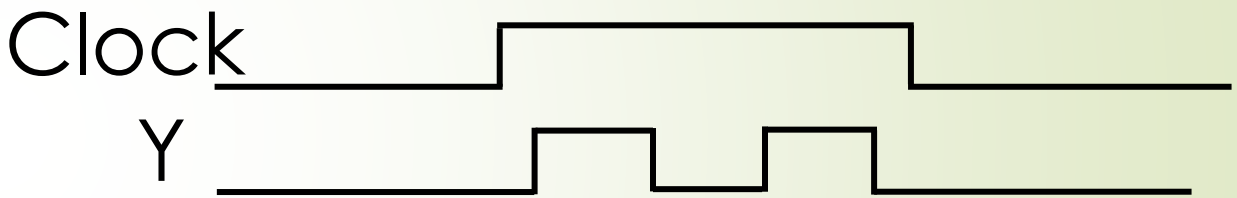
- The latch timing problem
- Edge-triggered flip-flop
- Master-slave flip-flop
- Direct inputs to flip-flops
- Flip-flop timing

The Latch Timing Problem

- Consider the following circuit:



- Suppose that initially Y = 0.



- As long as C = 1, the value of Y continues to change!
- The changes are based on the delay present on the loop through the connection from Y back to Y.
- This behavior is clearly unacceptable.
- Desired behavior: Y changes only once per clock pulse

Master–slave D flip-flop

- The circuit samples the *D* input and **changes** its output Q only at the **negative edge** of the synchronizing or controlling clock.
- Another say, *a change in the output of the flip-flop can be triggered only by and during the transition of the clock from 1* to 0.