CSE211 Digital Design

Akdeniz University

Week13: Sequential Logic Part 2

Assoc.Prof.Dr. Taner Danışman

tdanisman@akdeniz.edu.tr

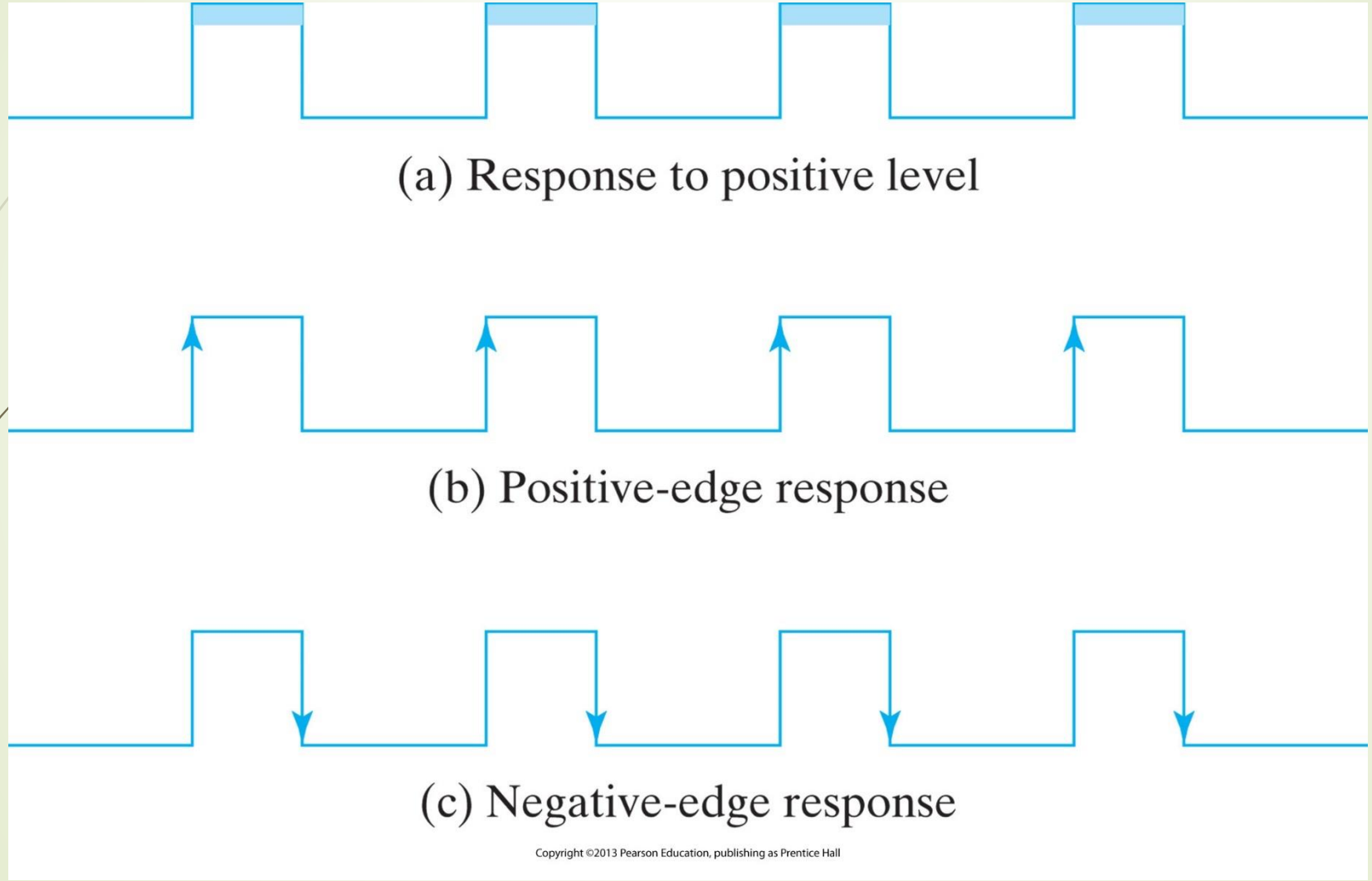
Course program

Week 01	09/16/2024	Introduction
Week 02	09/23/2024	Digital Systems and Binary Numbers I
Week 03	09/30/2024	Digital Systems and Binary Numbers II
Week 04	10/07/2024	Boolean Algebra and Logic Gates I
Week 05	10/14/2024	Boolean Algebra and Logic Gates II
Week 06	10/21/2024	Gate Level Minimization
Week 07	10/28/2024	Karnaugh Maps
Week 08	11/04/2024	Karnaugh Maps
Week 09	11/11/2024	Midterm
Week 10	11/18/2024	Combinational Logic
Week 11	11/25/2024	Combinational Logic
Week 12	12/02/2024	Timing, delays and hazards
Week 13	12/09/2024	Synchronous Sequential Logic
Week 14	12/16/2024	Synchronous Sequential Logic

5.4 Storage Elements: Flip-Flops

- The state of a latch or flip-flop is switched by a change in the control input. This momentary change is called a ***trigger***
- The problem with the latch is that it responds to a change in the *level* of a clock pulse. Glitches are problematic.

Clock response in latch and flip-flop

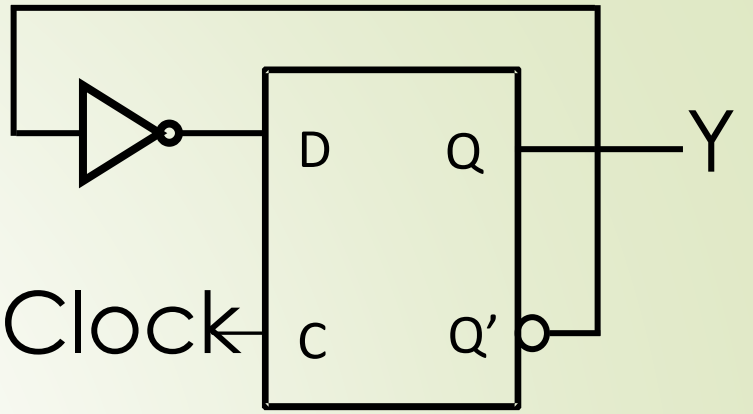


Flip-Flops

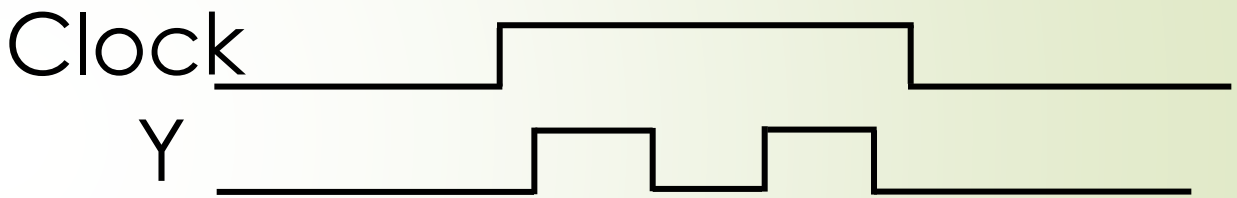
- The latch timing problem
- Edge-triggered flip-flop
- Master-slave flip-flop
- Direct inputs to flip-flops
- Flip-flop timing

The Latch Timing Problem

- Consider the following circuit:



- Suppose that initially Y = 0.



- As long as C = 1, the value of Y continues to change!
- The changes are based on the delay present on the loop through the connection from Y back to Y.
- This behavior is clearly unacceptable.
- Desired behavior: Y changes only once per clock pulse

Master–slave D flip-flop

- The circuit samples the *D* input and **changes** its output Q only at the **negative edge** of the synchronizing or controlling clock.
- Another say, *a change in the output of the flip-flop can be triggered only by and during the transition of the clock from 1* to 0.