

CSE211:

Digital Design

Original slides from
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<http://www.ece.iastate.edu/~alexs/classes/>

T Flip-Flops & JK Flip-Flops

*CprE 281: Digital Logic
Iowa State University, Ames, IA
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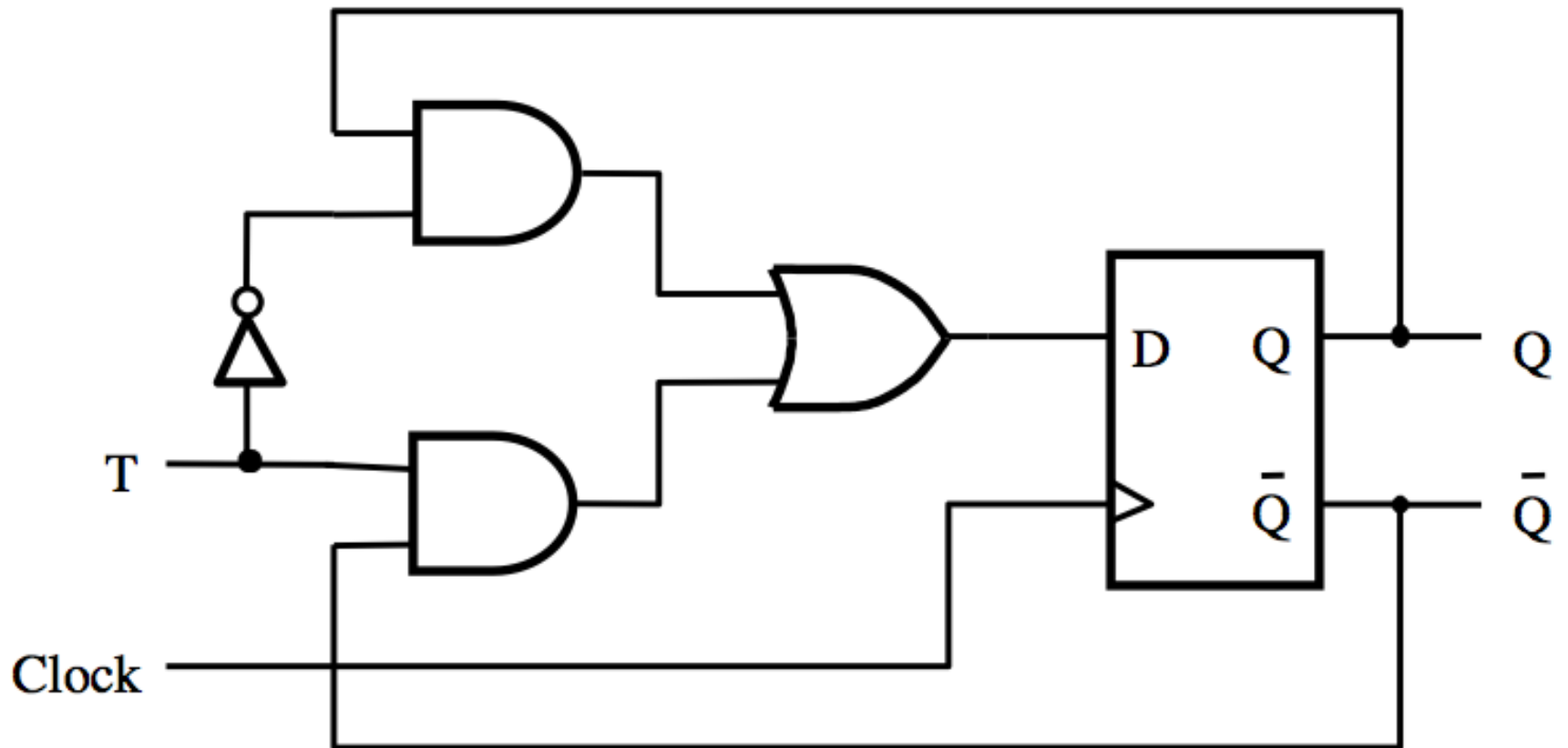
T Flip-Flop

Motivation

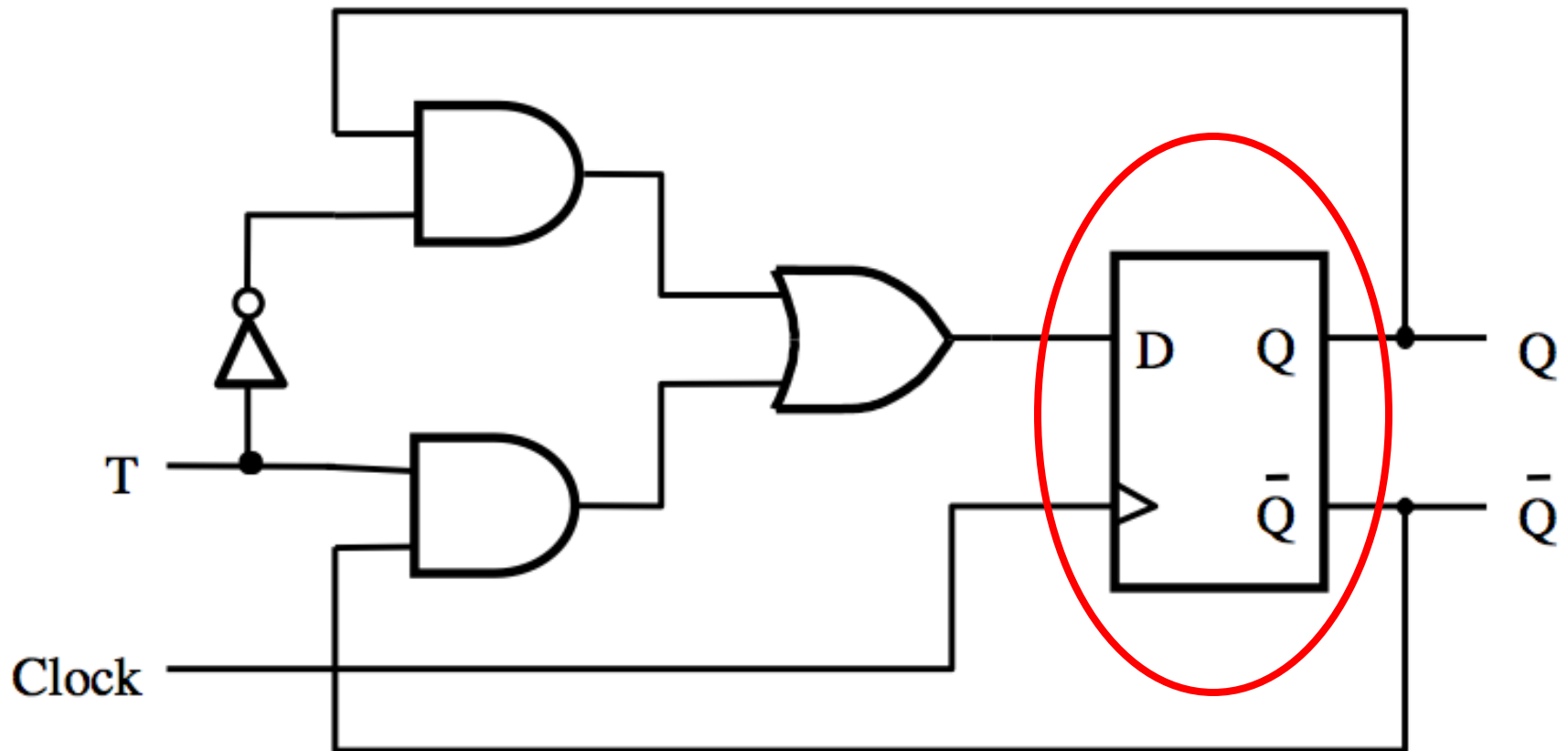
A slight modification of the D flip-flop that can be used for some nice applications.

In this case, T stands for Toggle.

T Flip-Flop

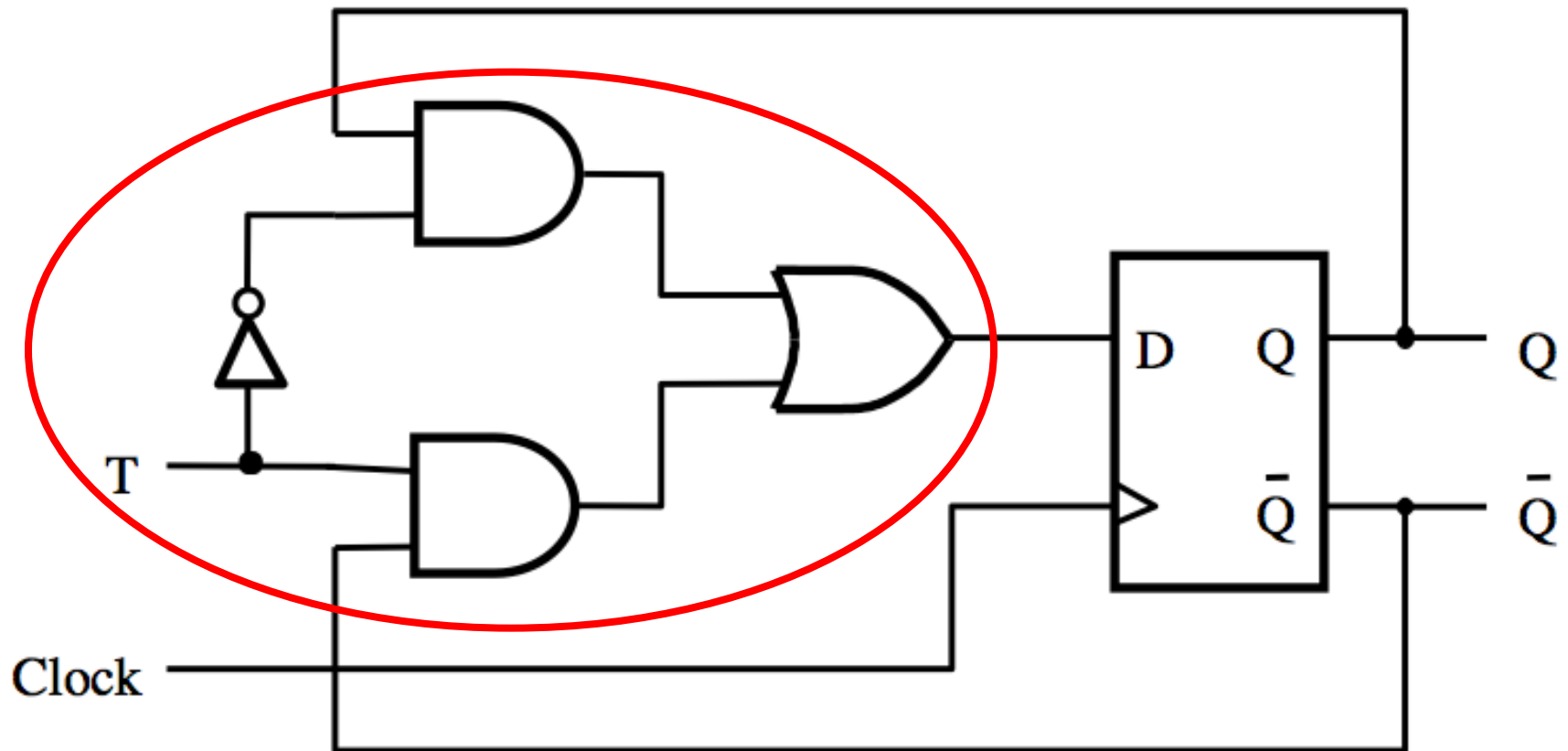


T Flip-Flop



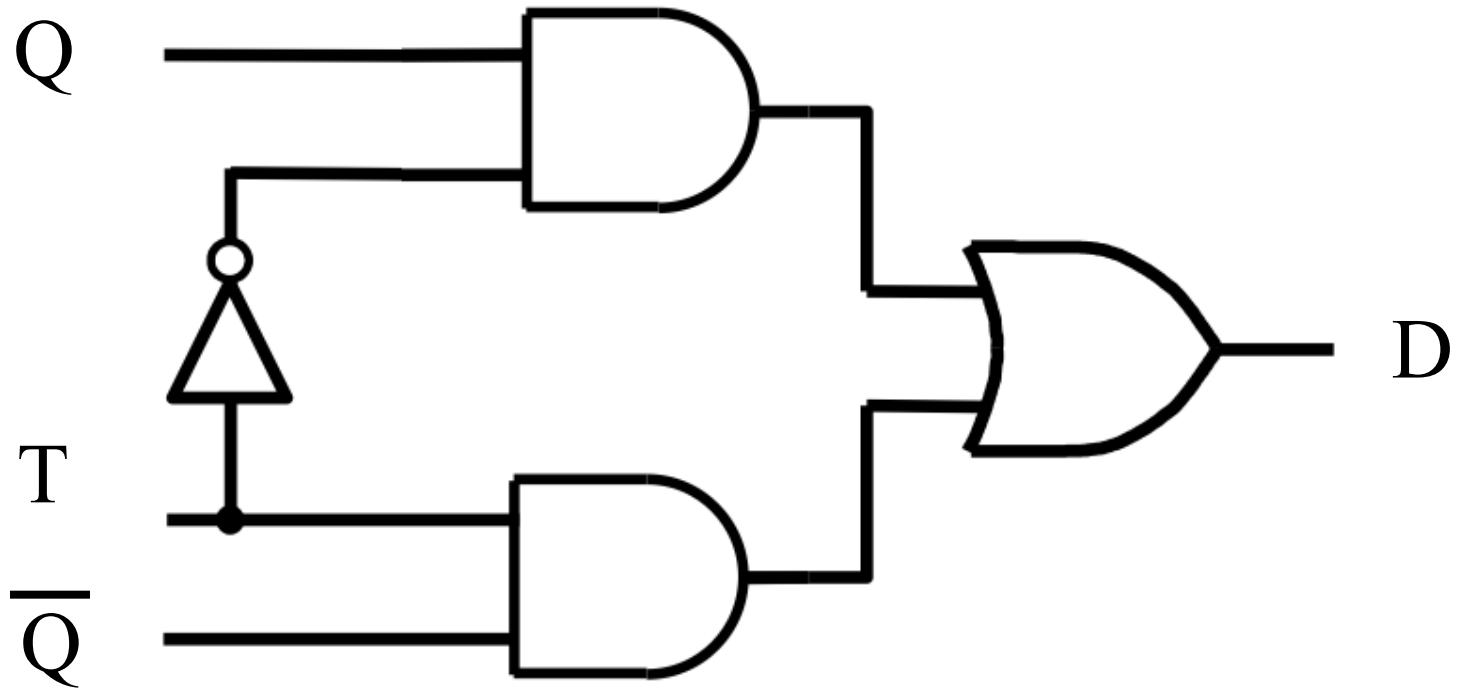
Positive-edge-triggered
D Flip-Flop

T Flip-Flop

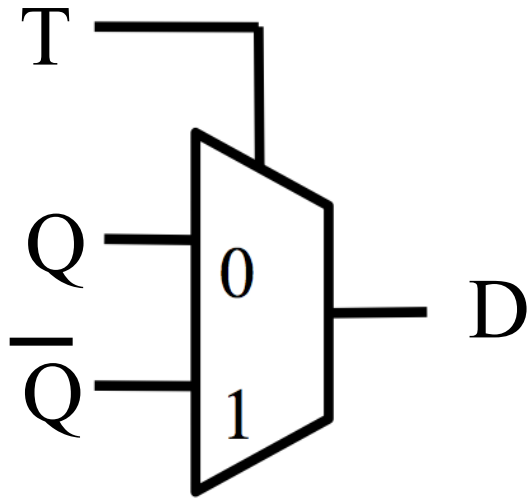


What is this?

What is this?

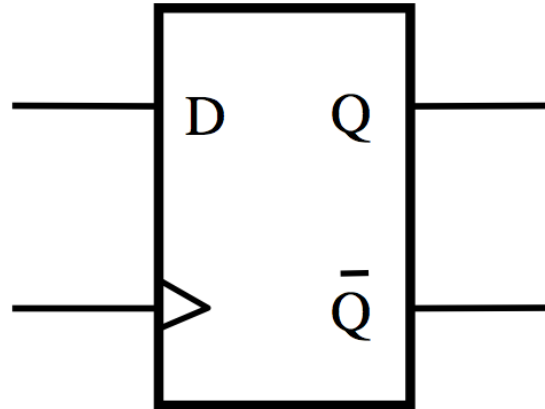


What is this?



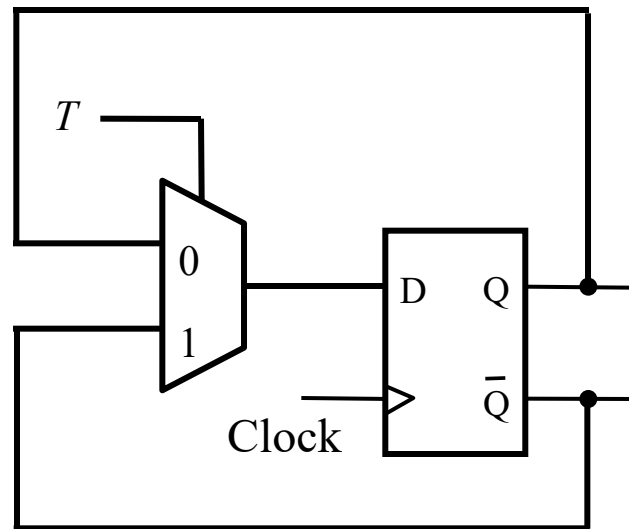
+

Clock

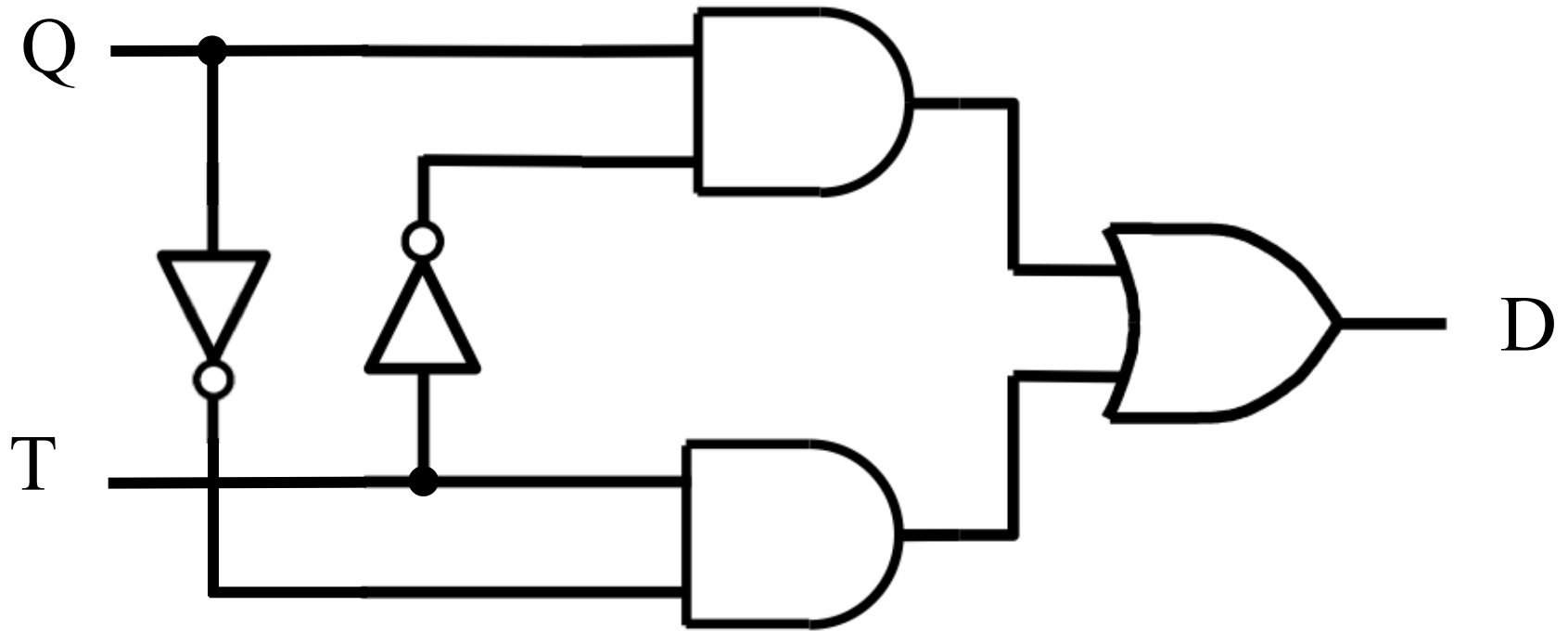


= ?

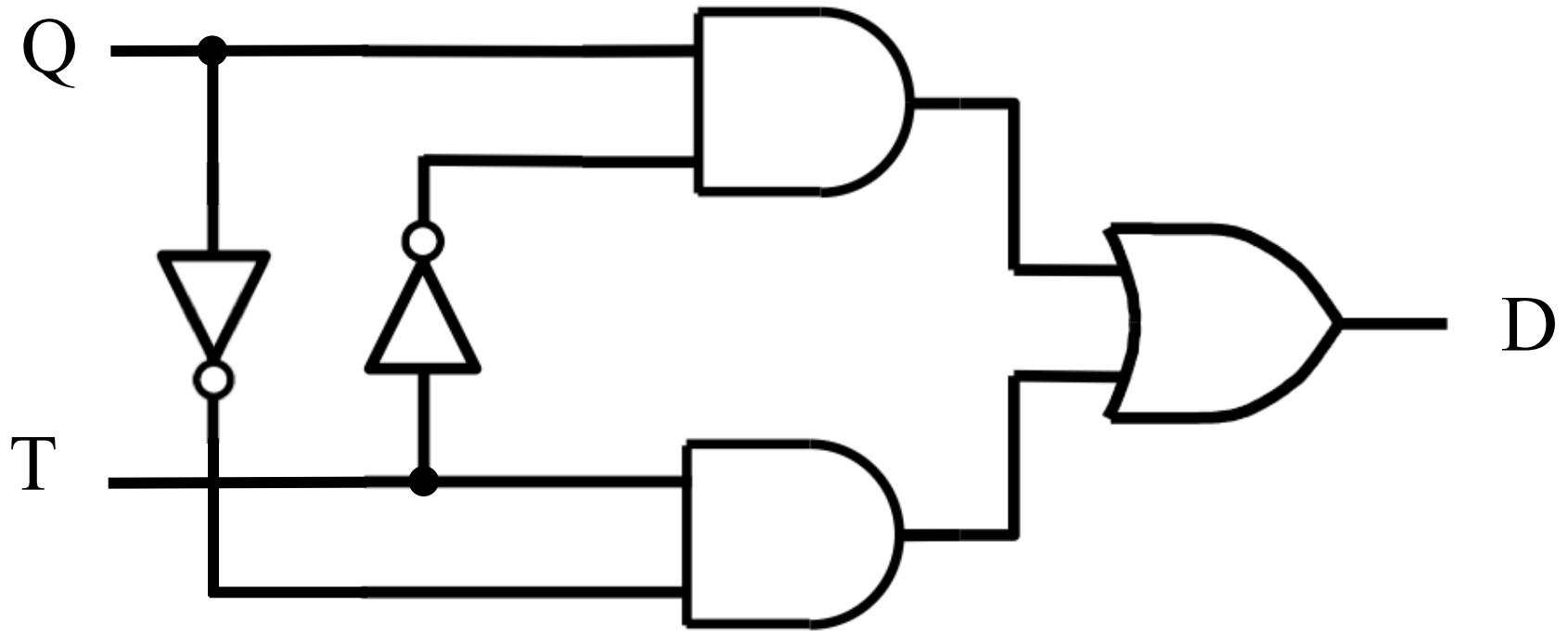
T Flip-Flop



What is this?

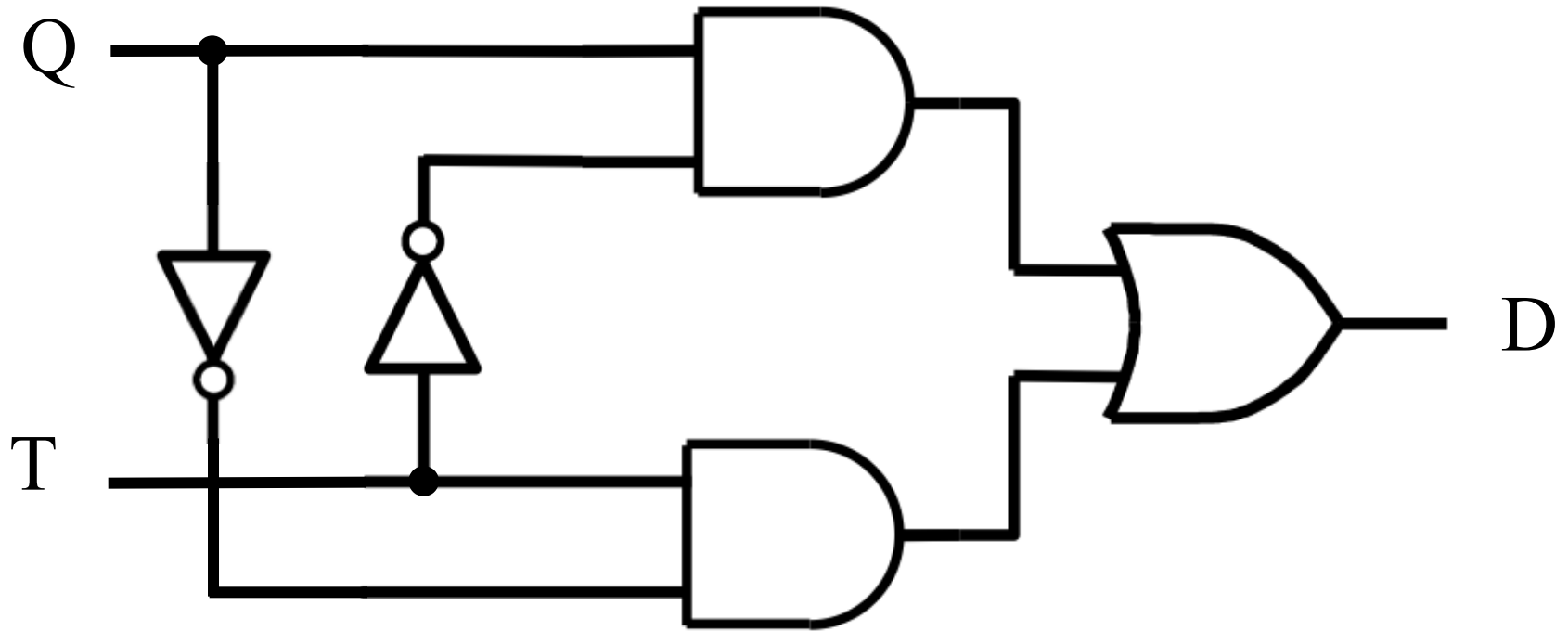


What is this?



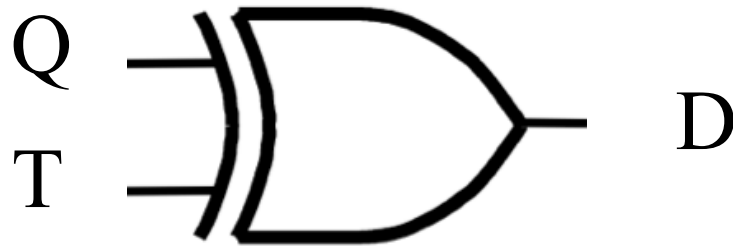
$$D = \overline{Q}T + Q\overline{T}$$

What is this?



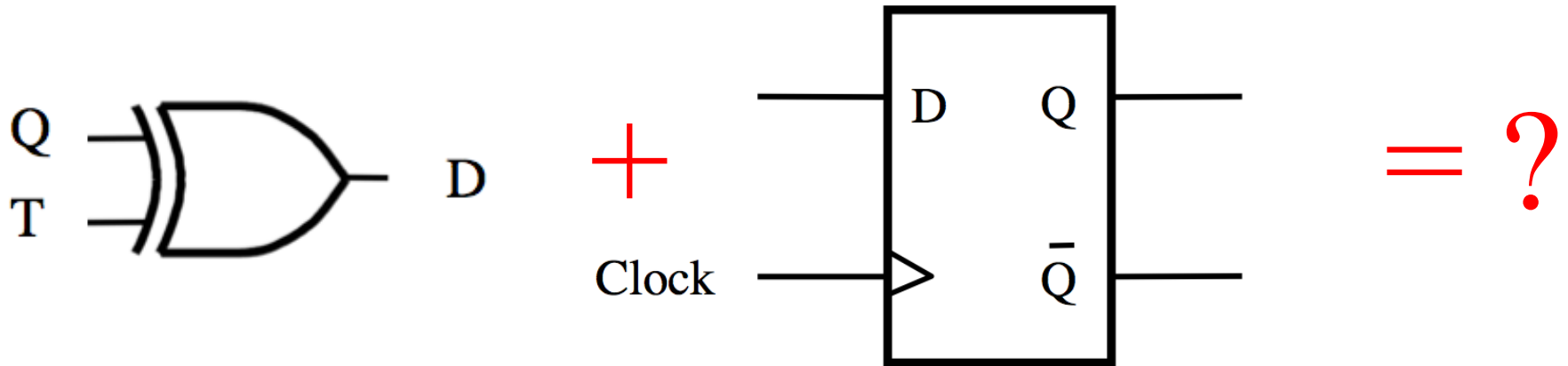
$$D = Q \oplus T$$

What is this?

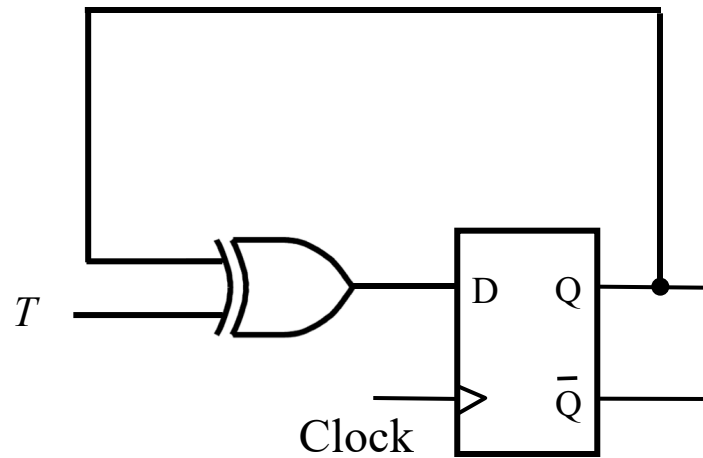


$$D = Q \oplus T$$

What is this?



T Flip-Flop



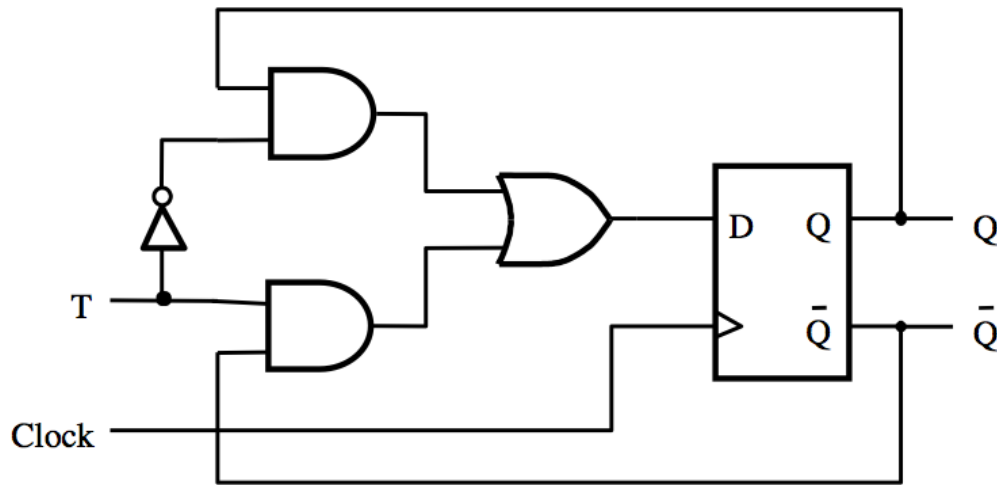
T Flip-Flop (How it Works)

If $T=0$ then it stays in its current state

If $T=1$ then it reverses its current state

In other words the circuit “toggles” its state when $T=1$. This is why it is called T flip-flop.

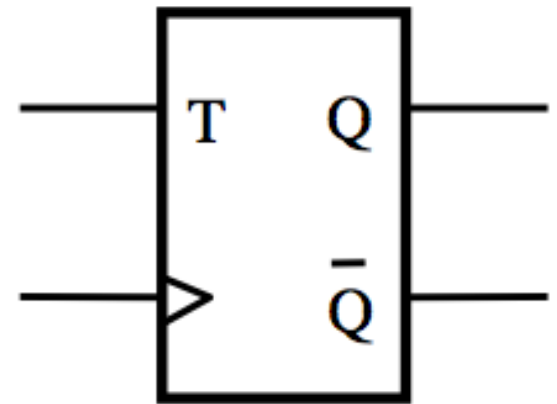
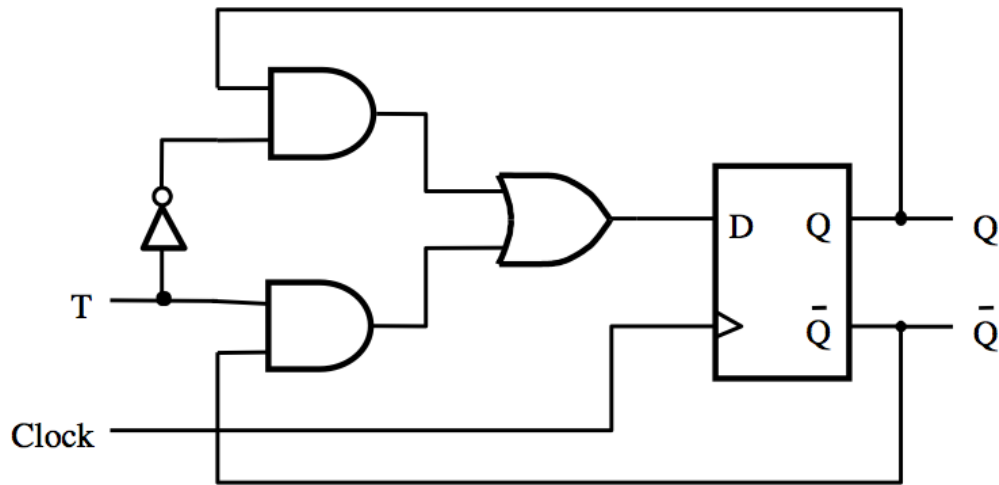
T Flip-Flop (circuit and truth table)



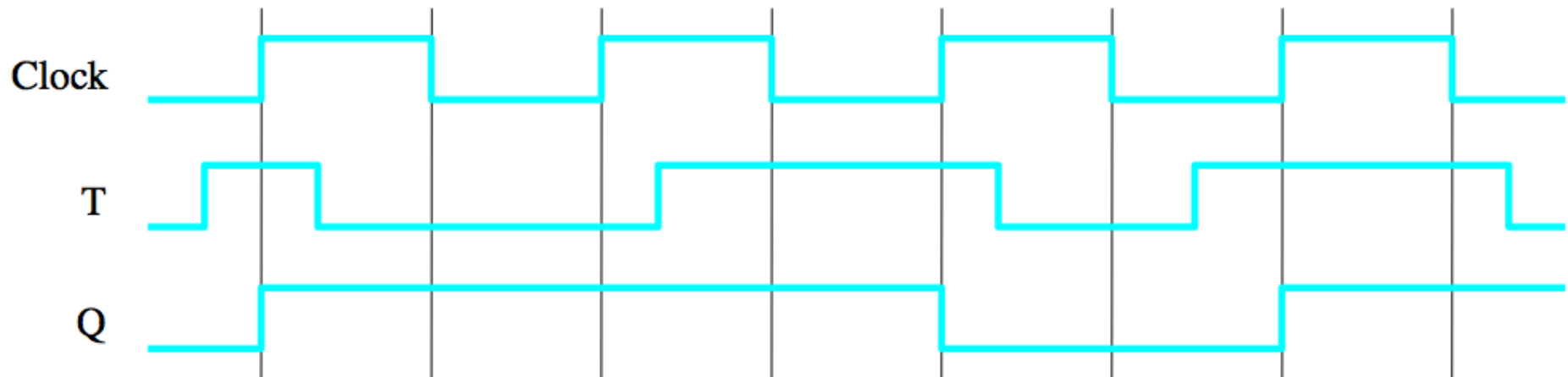
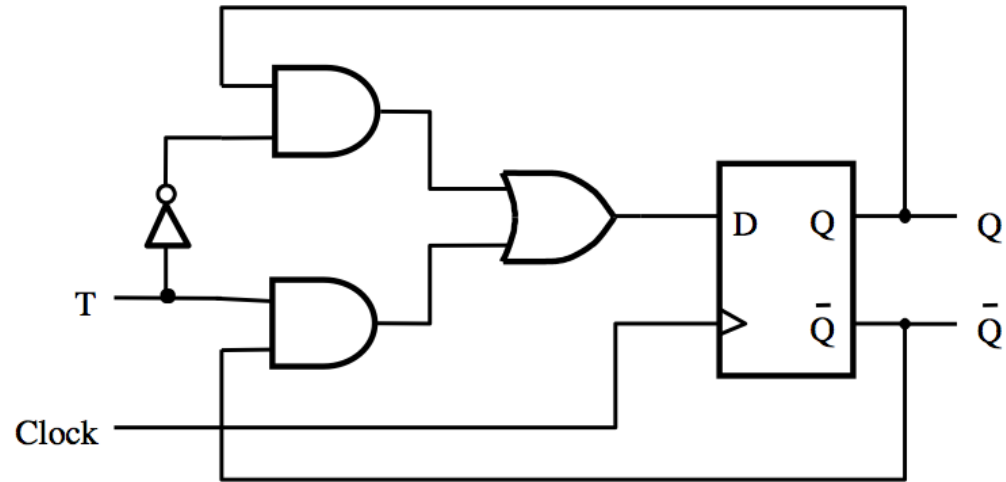
T	$Q(t+1)$
0	$Q(t)$
1	$\overline{Q(t)}$

T Flip-Flop

(circuit and graphical symbol)

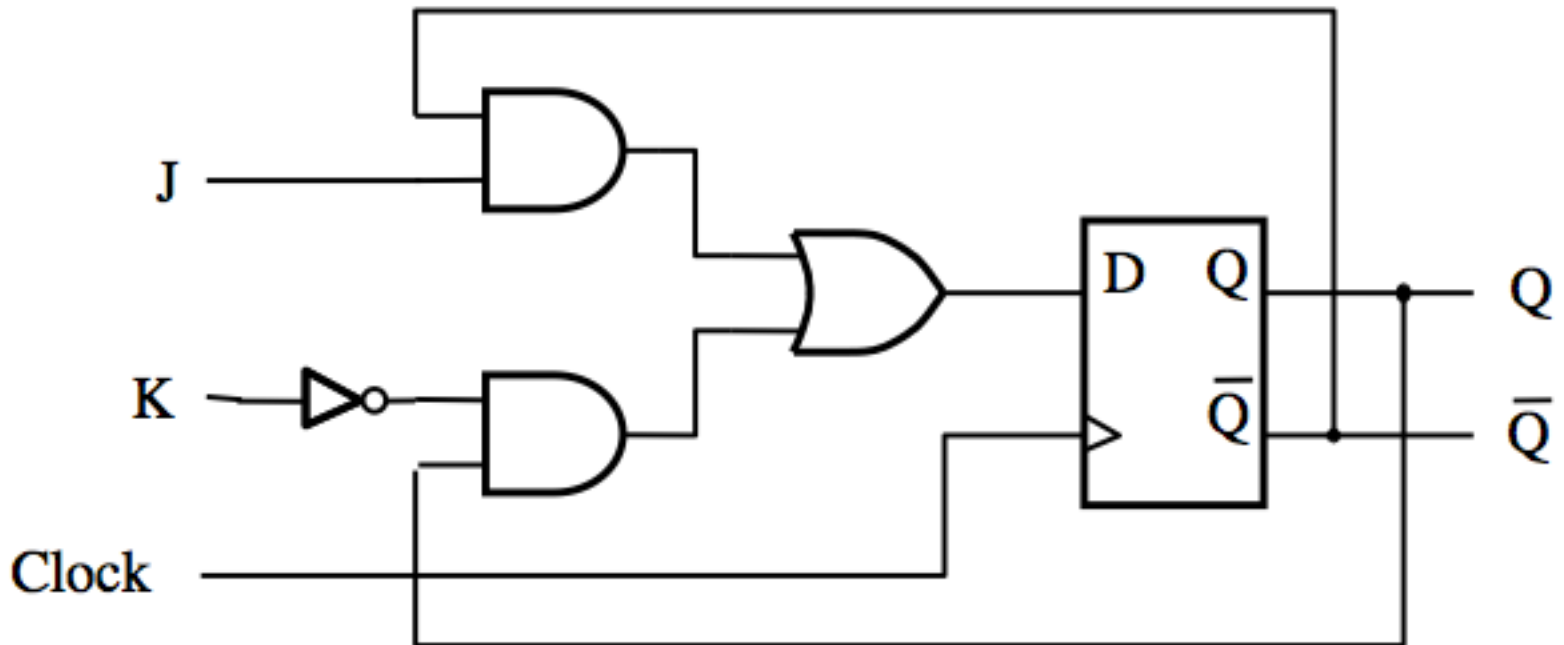


T Flip-Flop (Timing Diagram)



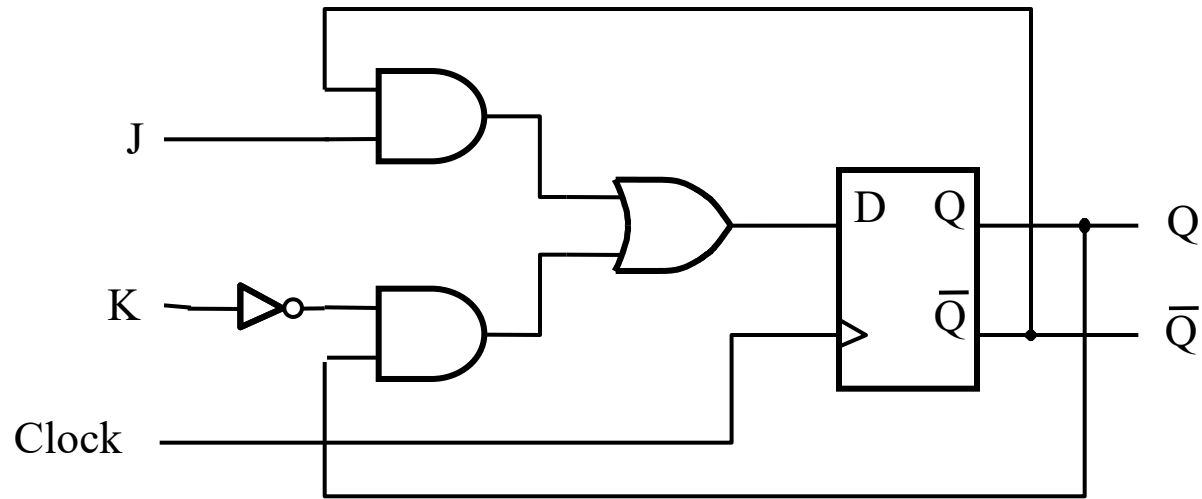
JK Flip-Flop

JK Flip-Flop



$$D = \bar{J}Q + \bar{K}Q$$

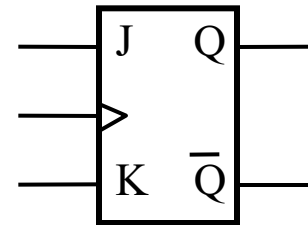
JK Flip-Flop



(a) Circuit

J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$\bar{Q}(t)$

(b) Truth table



(c) Graphical symbol

JK Flip-Flop (How it Works)

A versatile circuit that can be used both as a SR flip-flop and as a T flip flop

If $J=0$ and $S=0$ it stays in the same state

Just like SR It can be set and reset

$J=S$ and $K=R$

If $J=K=1$ then it behaves as a T flip-flop

THE END