AKDENIZ UNIVERSITY

Computer Engineering Department

CSE 211 Digital Design (2024-2025 Fall)

Lab02 – Gate Level Minimization – 21.10.2024

	Student No	Student Full Name	Group No
1			
2			
3			
4			

Lab Study 1

Design the logical circuit given in the figure, and based on the experiment results fill the truth table.

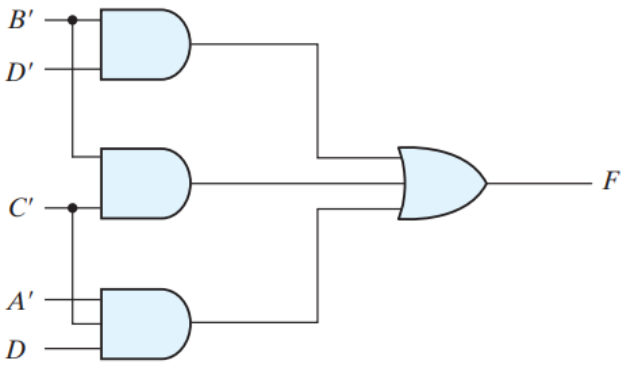


Table 1 - Truth Table of Study 1

A	B	C	D	F
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Lab Study 2

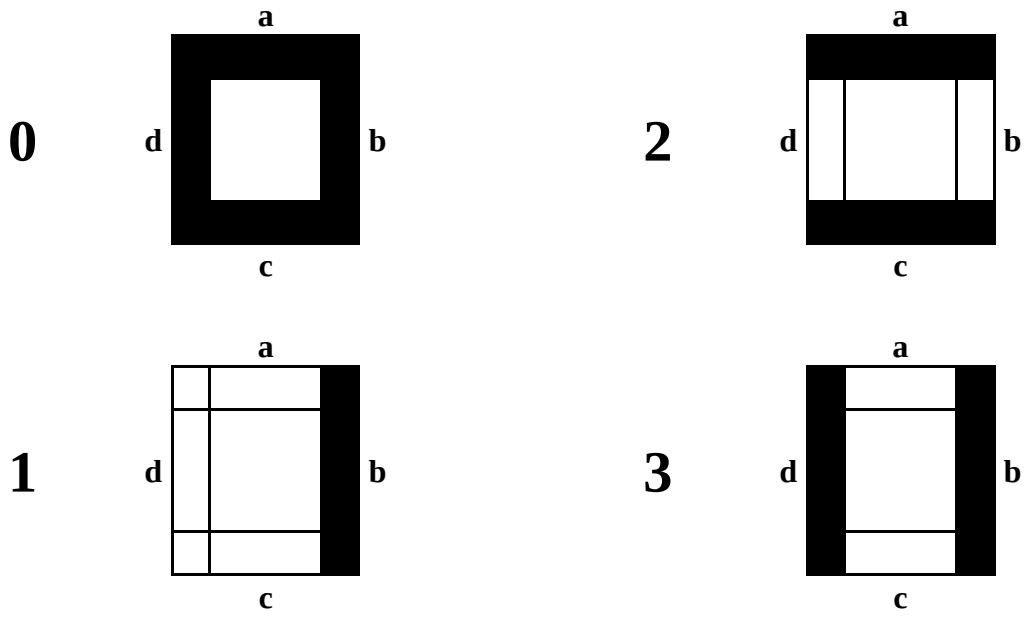
Design F=A'C+AB using only NAND gates. First draw the circuit in the box below.

Table 2: Truth table of Study 2

A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Lab Study 3

4 Segment Display: Your task is to design a 4-Segment display that shows the numbers from 0 to 3 as shown in the following combination below. The 4-Segments consist of 4 LED's (a,b,c,d). You must control the display with only 2 inputs (A and B). If any of the led is on it is filled with black color, and if off it is filled with white color. Follow the following steps to design the circuit.



- **Step 3.1 – Fill the truth table**

Decimal Value	INPUTS		OUTPUTS (LED)			
	A	B	a	b	c	d
0	0	0				
1	0	1				
2	1	0				
3	1	1				

- **Step 3.2 – Calculate the boolean functions for each LED by drawing Karnough Maps.**

Led a

A \ B	0	1
0		
1		

$F_a =$

Led b

A \ B	0	1
0		
1		

$F_b =$

Led c

A \ B	0	1
0		
1		

$F_c =$

Led d

A \ B	0	1
0		
1		

$F_d =$

- **Step 3.3 – Realize the Boolean functions you calculated. And validate your 4-segment display is working as described.**