AKDENIZ UNIVERSITY

Computer Engineering Department

CSE 211 Digital Design (2024-2025 Fall)

Lab06 – Synchronous Sequential Logic – 20.12.2024

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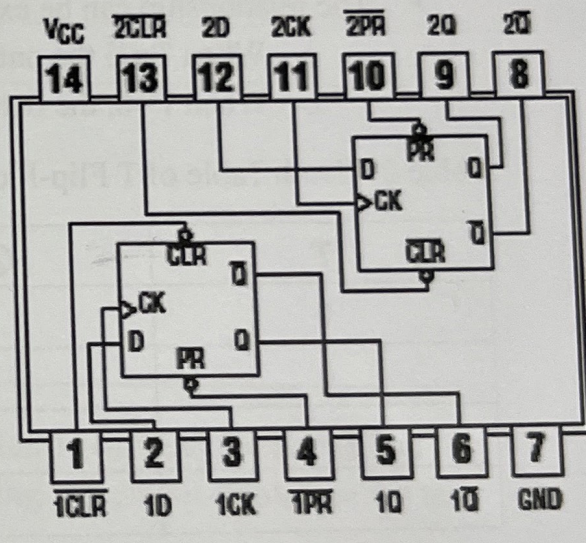
Lab Study 1 - Understanding the 7474 D-Type Flip-Flop

Task: Observe and verify the basic operation of the 7474 D Flip-Flop.

Circuit Setup:

- Connect Vcc to 5V and GND to ground.
- Connect D, CLR and PR to switches:
  - D: Data input.
  - CLK: Clock input.
  - CLR: Active-low reset.
  - PR: Active-low set.
- Attach LEDs to Q and Q' outputs to observe the flip-flop's state.



Input Test Cases:

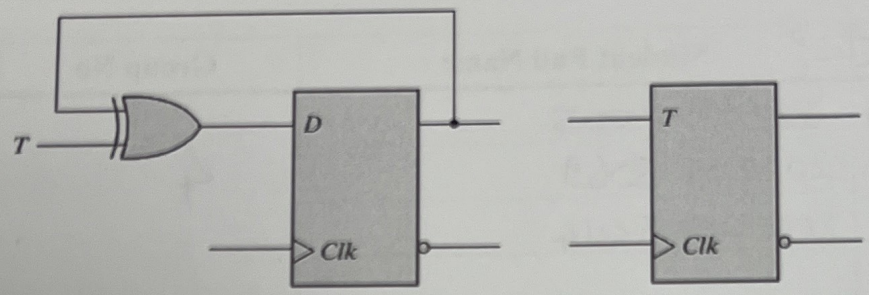
- Apply different combinations of D, CLR, and PR.

Table 1 - Truth Table of D Flip-Flop

CLR	PR	CLK	D	Q	Q'
0	1	X	X		
1	0	X	X		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

Lab Study 2 - Using the D Flip-Flop as a T Flip-Flop

Task: Convert the D Flip-Flop into a T Flip-Flop using an XOR gate. The circuit diagram is given below. Build the circuit and observe the behavior of T Flip-Flop. Then fill the truth table.



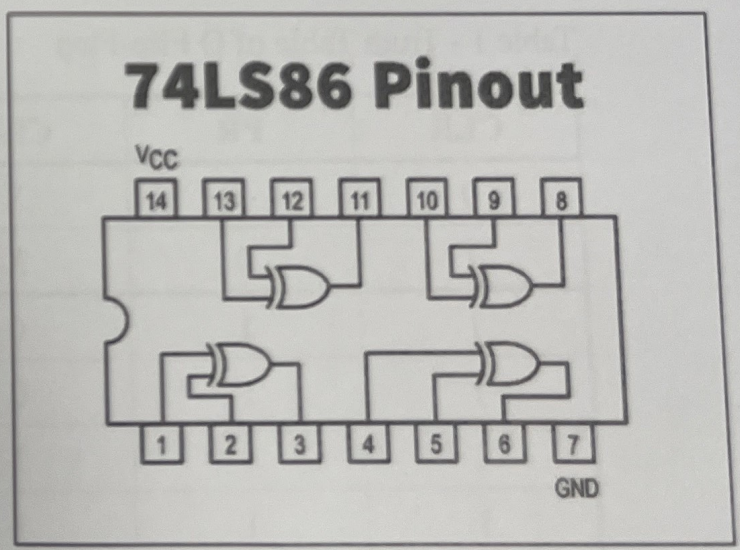
(b) From *D* flip-flop (c) Graphic symbol

Concept:

- A T Flip-Flop toggles its output on each clock pulse if T=1.
- The relationship can be expressed as D=T⊕Q
  - When *T*=1, the output toggles.
  - When *T*=0, the output remains unchanged.

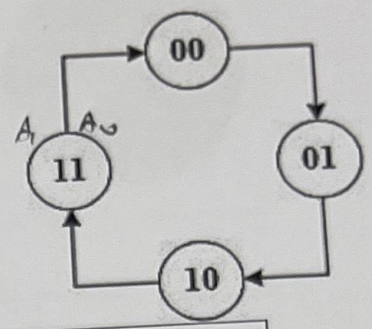
Table 2 - Truth Table of T Flip-Flop

T	$Q(t)$	$Q(t+1)$
0	0	0
0	1	1
1	0	1
1	1	0



Lab Study 3 - Designing a Binary Counter Using T Flip-Flops

Task: Build a 2-bit binary counter using T Flip-Flops. The state diagram of the counter is given.

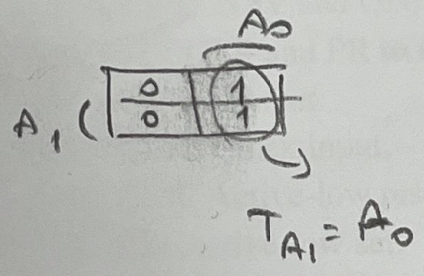
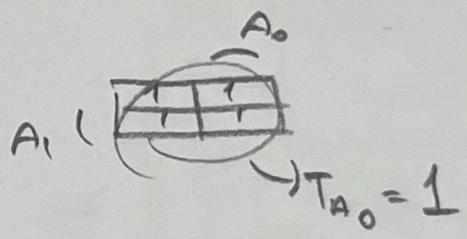


Based on the state machine diagram

1. Fill out the truth table below

Present State		Next State		Flip-Flop Inputs	
A_1	A_0	A_1	A_0	T_{A_1}	T_{A_0}
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

2. Draw the K-Maps and find the functions of T_{A_0} and T_{A_1}.

T_{A_1}	T_{A_0}
	

3. Complete the circuit diagram of the 2-bit binary counter. Then build the circuit and observe the counter's behavior. Show the numbers using 7-segment display on the test set.