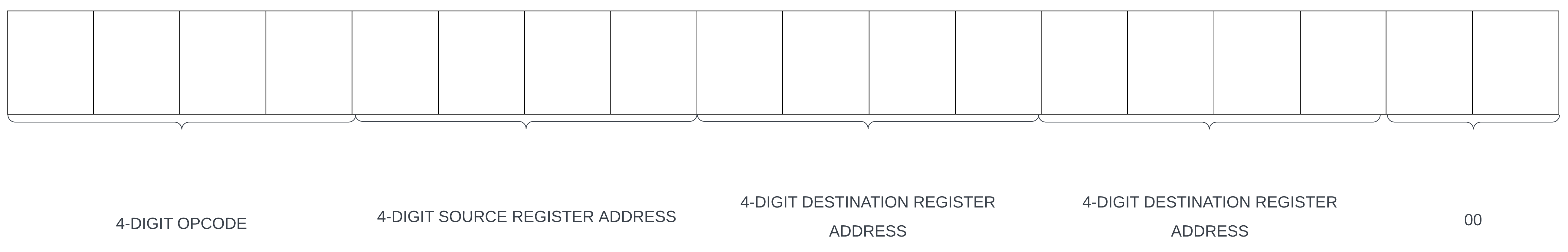
4-DIGIT OPCODE
4-DIGIT SOURCE REGISTER ADDRESS
4-DIGIT DESTINATION REGISTER ADDRESS
4-DIGIT DESTINATION REGISTER ADDRESS
00

ADD

In Assembly Language: ADD R1, R2, R3 (R1 = R2 + R3)
OPCODE: 0000
Destination Register (DST): Binary code of R1
Source Register 1 (SRC1): Binary code of R2
Source Register 2 (SRC2): Binary code of R3

The binary representation would follow this structure:
OPCODE (4 bits) - DST (4 bits) - SRC1 (4 bits) - SRC2 (4 bits)-00

AND

In Assembly Language: AND R1, R2, R3 (R1 = R2 AND R3)
OPCODE: 1011
Destination Register (DST): Binary code of R1
Source Register 1 (SRC1): Binary code of R2
Source Register 2 (SRC2): Binary code of R3

The binary representation would follow this structure:
OPCODE (4 bits) - DST (4 bits) - SRC1 (4 bits) - SRC2 (4 bits)-00

NAND

In Assembly Language: NAND DST, SRC1, SRC2 (DST = NOT (SRC1 AND SRC2))
Binary Code Generation:
OPCODE: 1110
Destination Register (DST): Binary code for DST
Source Register 1 (SRC1): Binary code for SRC1
Source Register 2 (SRC2): Binary code for SRC2
Binary Code:
OPCODE (4 bits) - DST (4 bits) - SRC1 (4 bits) - SRC2 (4 bits)-00

NOR

In Assembly Language: NOR DST, SRC1, SRC2 (DST = NOT (SRC1 NOR SRC2))
Binary Code Generation:
OPCODE: 1100
Destination Register (DST): Binary code for DST
Source Register 1 (SRC1): Binary code for SRC1
Source Register 2 (SRC2): Binary code for SRC2
Binary Code:
OPCODE (4 bits) - DST (4 bits) - SRC1 (4 bits) - SRC2 (4 bits)-00

ADDI

In Assembly Language: ADDI DST, SRC1, IMM (DST = SRC1 + IMM)
Binary Code Generation:
OPCODE: 0001
Destination Register (DST): Binary code for DST
Source Register 1 (SRC1): Binary code for SRC1
Immediate Value (IMM): Binary code for IMM
Binary Code:
0001 - DST (4 bits) - SRC1 (4 bits) - IMM (6 bits)

ANDI

In Assembly Language: ANDI DST, SRC1, IMM (DST = SRC1 AND IMM)
Binary Code Generation:
OPCODE: 1101
Destination Register (DST): Binary code for DST
Source Register 1 (SRC1): Binary code for SRC1
Immediate Value (IMM): Binary code for IMM
Binary Code:
OPCODE (4 bits) - DST (4 bits) - SRC1 (4 bits) - IMM (6 bits)

LD

In Assembly Language: LD DST, ADDR (DST = Memory[ADDR])
Binary Code Generation:
OPCODE: 0011
Destination Register (DST): Binary code for DST
Memory Address (ADDR): Binary code for ADDR
Binary Code:
0011 - DST (4 bits) - ADDR(10 bits)

ST

In Assembly Language: ST SRC, ADDR (Memory[ADDR] = SRC)
Binary Code Generation:
OPCODE: 0100
Destination Register (SRC): Binary code for SRC
Memory Address ADDR): Binary code for ADDR
Binary Code:
0100 - SRC (4 bits) - ADDR (8 bits)

CMP

In Assembly Language: CMP OP1, OP2
Binary Code Generation:
OPCODE: 0101
Comparison Operand 1 (OP1): Binary code for OP1
Comparison Operand 2 (OP2): Binary code for OP2
Binary Code:
0101 - OP1 (7 bits) - OP2 (7 bits)

JUMP

In Assembly Language: JUMP ADDR
Binary Code Generation:
OPCODE: 0010
Jump Address (ADDR): Binary code for ADDR
Binary Code:
0010 - ADDR (14 bits)

JE

In Assembly Language: JE ADDR (Increment PC to ADDR if ZF=1 and CF=0)
Binary Code Generation:
OPCODE: 0110
Jump Address (ADDR): Binary code for ADDR
Binary Code:
0110 - ADDR (14 bits)

JA

In Assembly Language: JA ADDR (Jump to ADDR if ZF=0, CF=0)
Binary Code Generation:
OPCODE: 0111
Jump Address (ADDR): Binary code for ADDR
Binary Code:
0111 - ADDR(14 bits)

JB

In Assembly Language: JB ADDR (Increment PC to ADDR if ZF=0 and CF=1)
Binary Code Generation:
OPCODE: 1000
Jump Address (ADDR): Binary code for ADDR
Binary Code:
1000 - ADDR (14 bits)

JAE

In Assembly Language: JAE ADDR (Jump to ADDR if CF=0)
Binary Code Generation:
OPCODE: 1001
Jump Address (ADDR): Binary code for ADDR
Binary Code:
1001 - ADDR (14 bits)

JBE

In Assembly Language: JBE ADDR (Increment PC to ADDR if ZF=1 or CF=1)
Binary Code Generation:
OPCODE: 1010
Jump Address (ADDR): Binary code for ADDR
Binary Code:
1010 - ADDR (14 bits)