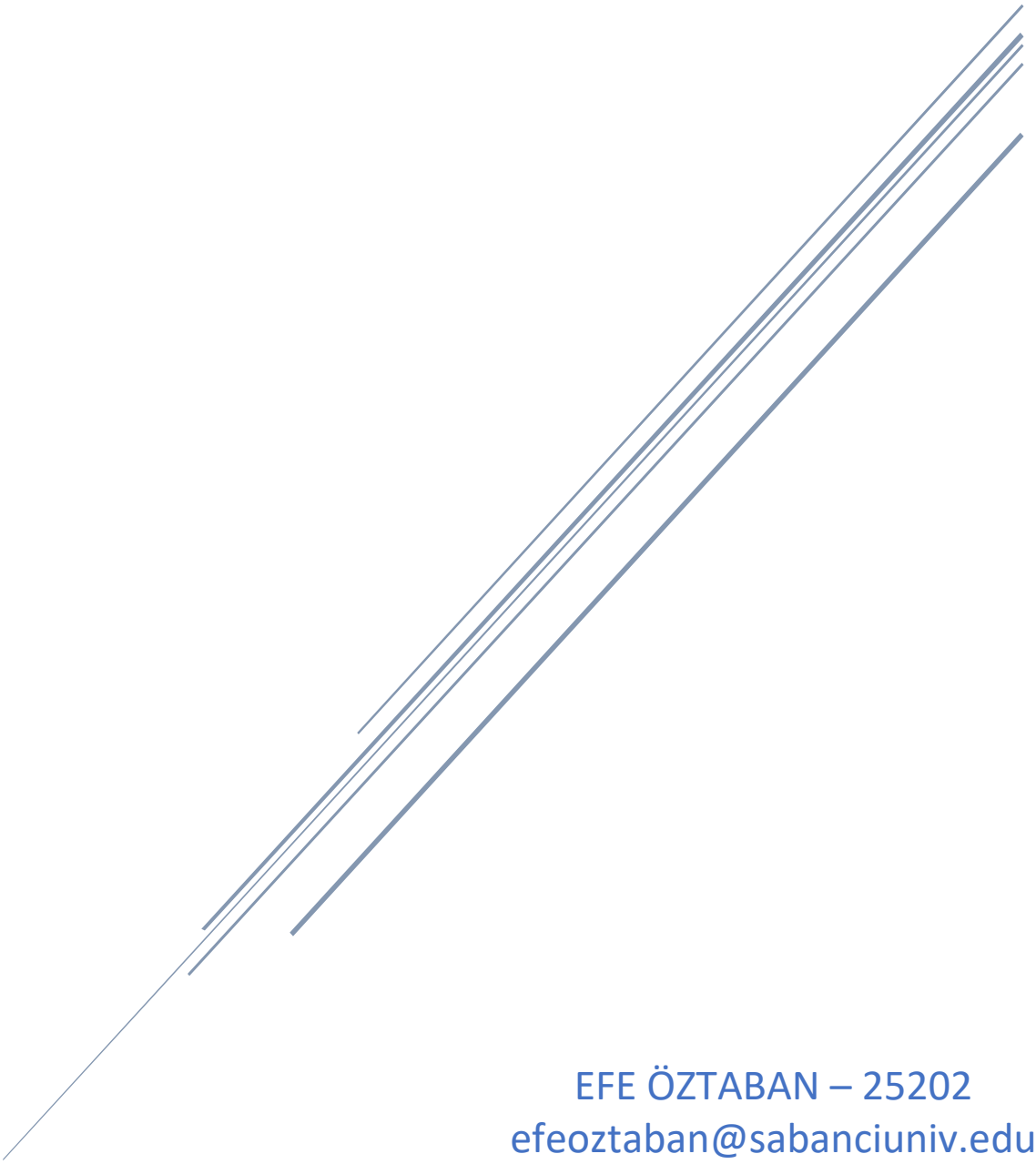
EE 402 VLSI SYSTEM DESIGN II

Lab Report for Lab #3



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1. Introduction

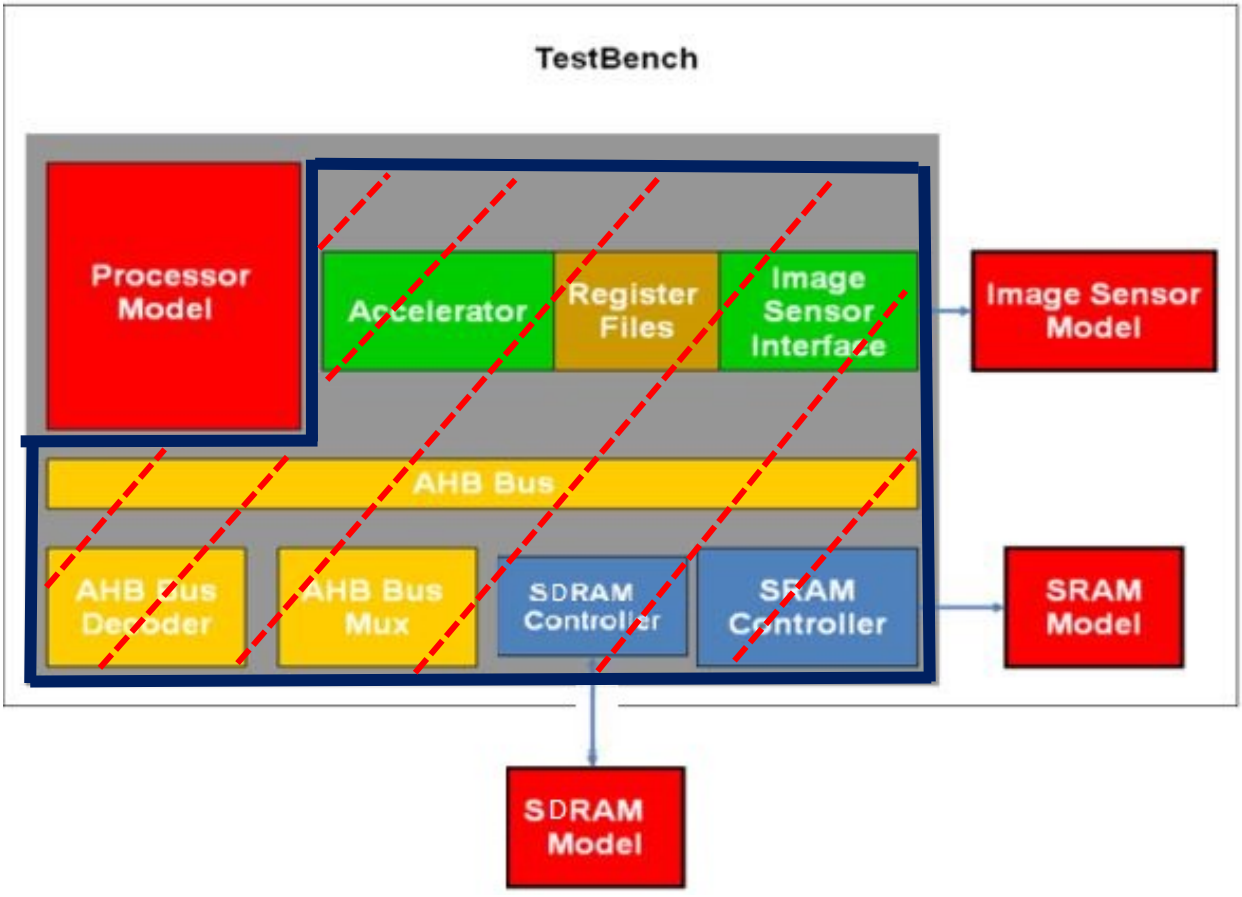
In this laboratory assignment, a System-on-Chip ASIC prototype is given as the Verilog RTL implementation. This prototype was changed with the new requirements in lab2. These requirements were adding a SDRAM controller and SDRAM module. Processor is using the SDRAM to save the results of its calculations. It is writing the results to the SDRAM and read the results from SDRAM to compare them with the results of accelerator.

The SoC ASIC implementation is simulated with Mentor Graphics QuestaSim and Xilinx ISE in the laboratory assignment. The simulation results are given in the related section of the report.

The SoC ASIC implementation is synthesised with logic synthesis tool for this laboratory assignment. Timing constraint for the synthesis is given as 5 nm clock period for the synthesis. After the synthesis is done, timing report and area report are achieved.

Timing report meets the requirements. Area report is giving the required area for the chip. Also, there is no errors during the synthesis.

The parts pointed in the figure below is used in the synthesis.



2. Simulation Results

The simulations for the given SoC ASIC are performed with Mentor Graphics QuestaSim and Xilinx ISE.

It can be seen that the simulation is runed correctly from the results below:

```
VSIM 3> run -all
#         0 OK
#         1 OK
#         2 OK
#         3 OK
#         4 OK
#         5 OK
#         6 OK
#         7 OK
#         8 OK
#         9 OK
#        10 OK
#        11 OK
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#        54 OK
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#        57 OK
#        58 OK
#        59 OK
#        60 OK
#        61 OK
#        62 OK
#        63 OK
```
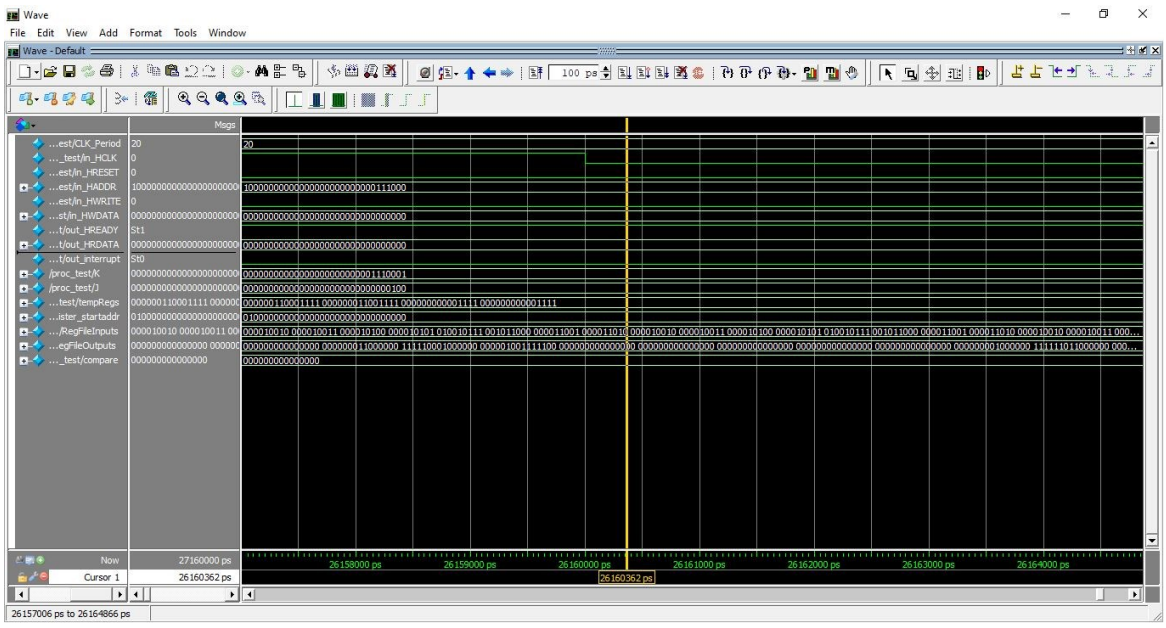
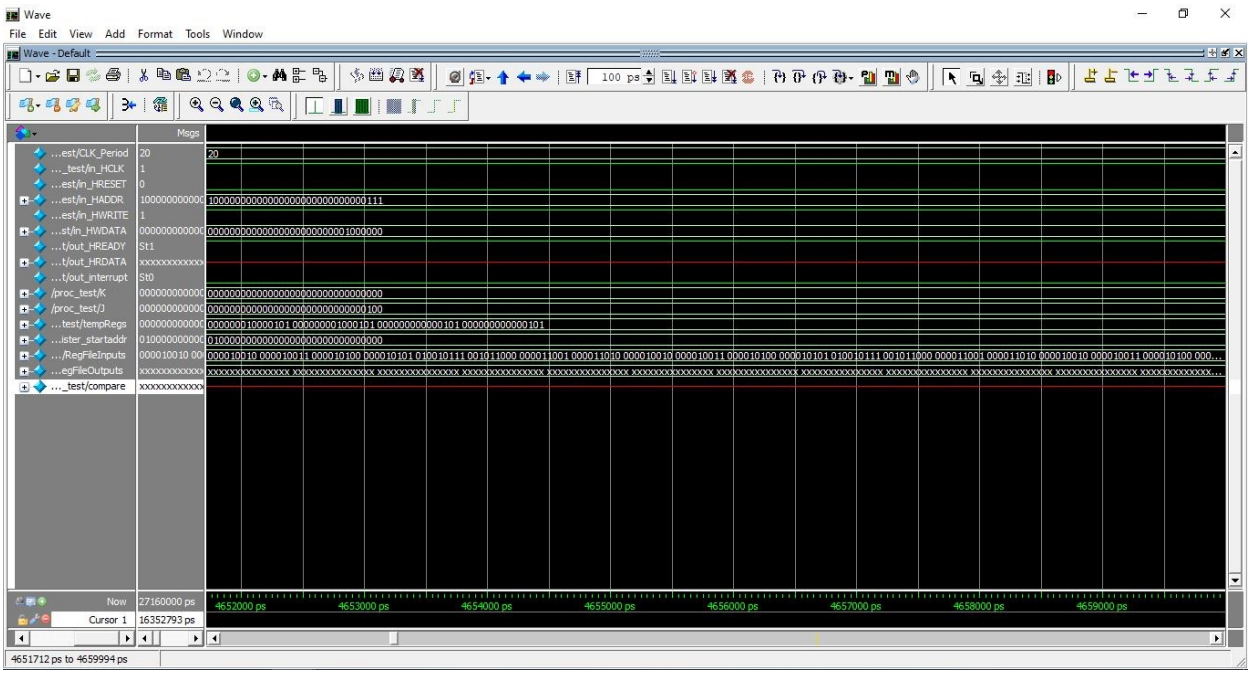
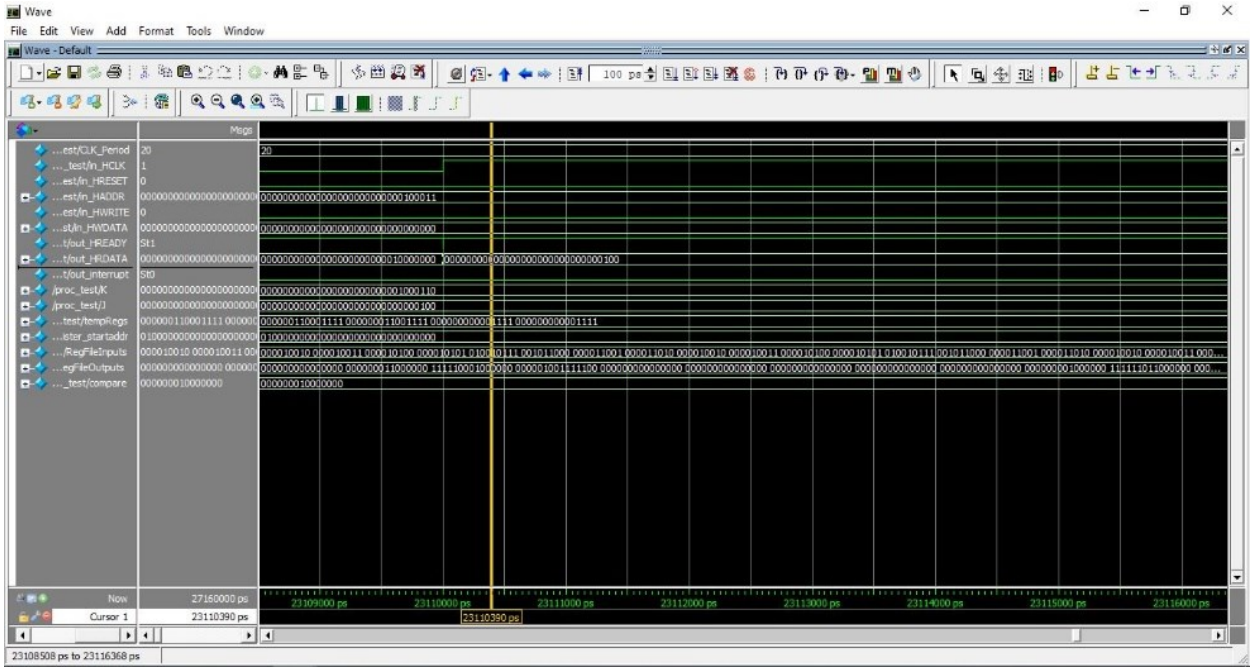
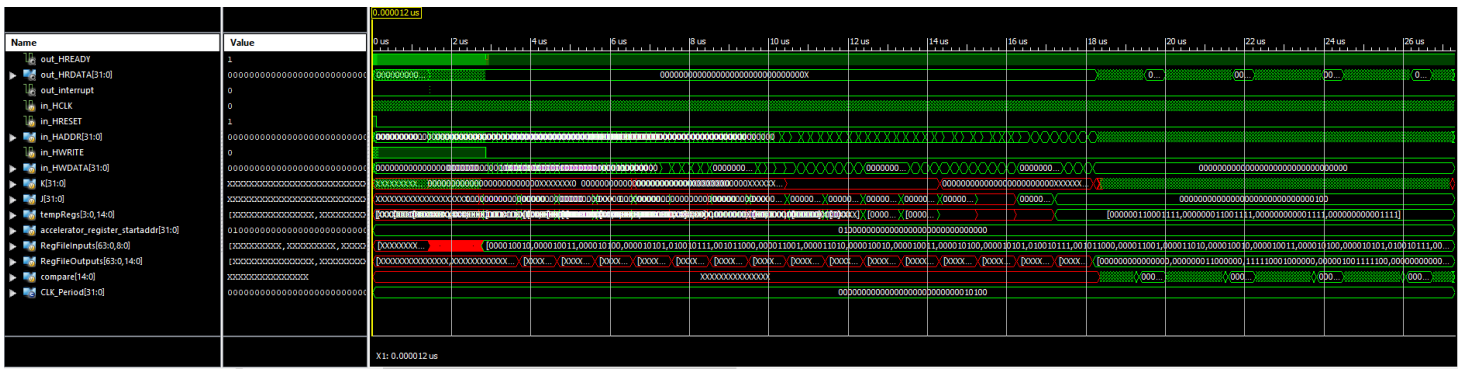

The simulation results from the Mentor Graphics QuestaSim are given with waveform below:







Also, the simulation result of the design in Xilinx ISE is given below:



3. Synthesis Results

a. Timing Report

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 5
Design : forward_transform_soc
Version: H-2013.03-SP4
Date   : Thu Jun 23 14:00:01 2022
****************************************

Operating Conditions: WORST   Library: saed90nm_max
Wire Load Model Mode: enclosed

  Startpoint: in_SDRAM_r_DATA[4]
              (input port clocked by clk)
  Endpoint: out_HRDATA[4]
            (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  forward_transform_soc
                     140000                saed90nm_max
```

```
Point                                                   Incr       Path
--------------------------------------------------------------------------
clock clk (rise edge)                                   0.00       0.00
clock network delay (ideal)                             0.00       0.00
input external delay                                    0.00       0.00 f
in_SDRAM_r_DATA[4] (in)                                 0.00       0.00 f
sdram_controller/in_read_data[4] (sdram_controller)     0.00       0.00 f
sdram_controller/out_HRDATA[4] (sdram_controller)       0.00       0.00 f
mux/in_HRDATA_SDRAMController[4] (ahb_mux_s2m)          0.00       0.00 f
mux/U14/Q (AO222X1)                                     0.72       0.72 f
mux/out_HRDATA[4] (ahb_mux_s2m)                         0.00       0.72 f
out_HRDATA[4] (out)                                     0.00       0.72 f
data arrival time                                                  0.72

clock clk (rise edge)                                   5.00       5.00
clock network delay (ideal)                             0.00       5.00
clock uncertainty                                      -0.20       4.80
output external delay                                   0.00       4.80
data required time                                                 4.80
--------------------------------------------------------------------------
data required time                                                 4.80
data arrival time                                                 -0.72
--------------------------------------------------------------------------
slack (MET)                                                        4.08
```

```
 Point                                                   Incr       Path
 ------------------------------------------------------------------------
 clock clk (rise edge)                                   0.00       0.00
 clock network delay (ideal)                             0.00       0.00
 input external delay                                    0.00       0.00 f
 in_SDRAM_r_DATA[0] (in)                                 0.00       0.00 f
 sdram_controller/in_read_data[0] (sdram_controller)     0.00       0.00 f
 sdram_controller/out_HRDATA[0] (sdram_controller)       0.00       0.00 f
 mux/in_HRDATA_SDRAMController[0] (ahb_mux_s2m)          0.00       0.00 f
 mux/U10/Q (AO222X1)                                     0.72       0.72 f
 mux/out_HRDATA[0] (ahb_mux_s2m)                         0.00       0.72 f
 out_HRDATA[0] (out)                                     0.00       0.72 f
 data arrival time                                                  0.72

 clock clk (rise edge)                                   5.00       5.00
 clock network delay (ideal)                             0.00       5.00
 clock uncertainty                                      -0.20       4.80
 output external delay                                   0.00       4.80
 data required time                                                 4.80
 ------------------------------------------------------------------------
 data required time                                                 4.80
 data arrival time                                                 -0.72
 ------------------------------------------------------------------------
 slack (MET)                                                        4.08
```

b. Area Report

```
****************************************
Report : area
Design : forward_transform_soc
Version: H-2013.03-SP4
Date   : Thu Jun 23 14:00:00 2022
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    saed90nm_max (File: /home/efeoztaban/forward_transform_soc/saed90nm_max.db)

Number of ports:                          292
Number of nets:                           445
Number of cells:                            6
Number of combinational cells:              0
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       6

Combinational area:              56419.926822
Buf/Inv area:                     4947.450183
Noncombinational area:           54709.584394
Macro/Black Box area:                0.000000
Net Interconnect area:            6719.624813

Total cell area:                111129.511216
Total area:                     117849.136029
1
```