EE 402 VLSI SYSTEM DESIGN II
Spring 2022

Project Part2
Due Date: 25 May 2022

You should do the following modifications and additions to the Verilog RTL implementation of the prototype System-on-Chip (SoC) ASIC and its Verilog testbench given to you in Project Part1.

You should add an SDRAM controller as a slave to AHB bus at address 32'b10000…000. The SDRAM controller will receive memory access requests from AHB bus. It will service these requests by accessing off-chip SDRAM.

You should add an SDRAM model which models a 1 Gb off-chip single data rate SDRAM with 4 banks, 2 clock cycles RAS-CAS latency and the following interface: Address (14-bit), Bank Address (2-bit), Data (32-bit), CS (1-bit), WE (1-bit), RAS (1-bit), CAS (1-bit), CLK (1-bit).

You should modify the processor model such that it writes the H.264 forward transform results into off-chip SDRAM memory instead of its internal memory. After both the accelerator and processor model finish H.264 forward transform, processor model should read the accelerator results from off-chip SRAM using SRAM controller, it should read its results from off-chip SDRAM using SDRAM controller, and it should compare them.

You should verify your Verilog RTL implementation and testbench by simulating them using Mentor Graphics QuestaSim.

You should then write a short report explaining which Verilog files you modified and which Verilog files you added, the modifications and additions you have done, the status of your implementation and verification. You should also include QuestaSim Waveform Screen Shot showing the simulation results in your report.

Put all your Verilog files and report into a zip file and submit this zip file to EE402 SUCourse+.