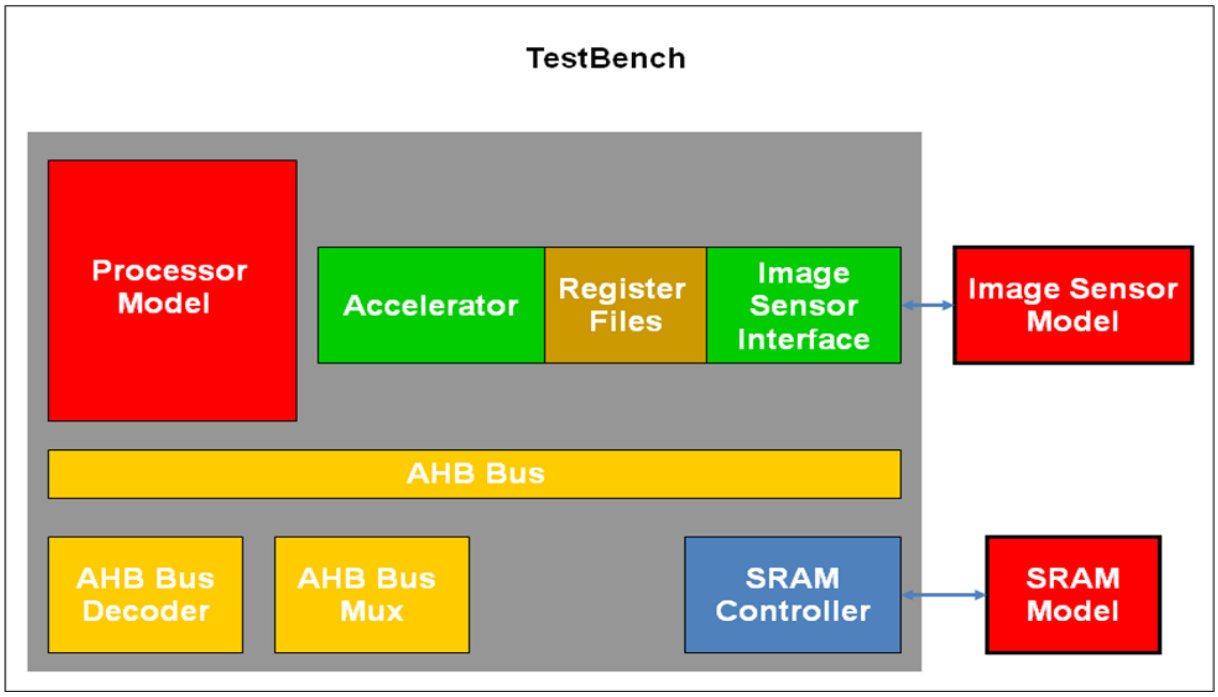
EE 402 VLSI SYSTEM DESIGN II
Spring 2022

Project Part1
Due Date: 20 April 2022

You are given Verilog RTL implementation of the following prototype System-on-Chip (SoC) ASIC and the Verilog testbench for verifying the implementation. You should analyze the Verilog RTL codes and the Verilog testbench codes. You should simulate them using Mentor Graphics QuestaSim. You should then write a report explaining the module hierarchy, the operations performed by each module and the memory map. You should draw a figure showing each module and main interconnects between them. You should include this figure and QuestaSim Waveform Screen Shot showing the simulation results in your report. Submit your report in PDF format to EE402 SUCourse+.



Accelerator implements H.264 forward transform algorithm. Processor model and peripherals communicate using Arm AHB bus. Processor model is the only Master on the AHB bus. There is a Decoder and a Slave-to-Master Multiplexer on the bus. Decoder selects the proper Slave on the bus based on the system memory map. In this ASIC, image sensor interface (ISI) and accelerator are tightly coupled. They appear as a single Slave on the AHB bus, and they have a single address space on the system memory map. Static RAM (SRAM) controller is also a Slave on the AHB bus. The SRAM controller receives memory access requests from AHB bus. It services these requests by accessing off-chip SRAM. There is also a Default Slave on the AHB bus.

After power-on-reset, processor model starts the accelerator by writing to a control register in it. The accelerator first gets an 8x8 image from the image sensor through image sensor interface (ISI). ISI sends a frame capture signal to the image sensor. It then gets an 8x8 image from the image sensor and stores it into a 64x8 register file. The ISI receives 8 bits in each clock cycle from the image sensor. After the image is stored into the register file, the accelerator informs processor model by sending an interrupt signal. Processor model and the accelerator then perform H.264 forward transform on the image stored in the register file in parallel. Accelerator has direct access to the register file, and it writes the H.264 forward transform results into SRAM using SRAM controller. Processor model reads the register file through the AHB bus, and it writes the H.264 forward transform results into its internal memory. After the accelerator finishes H.264 forward transform, it informs the processor model by setting a status register. After both the accelerator and processor model finish H.264 forward transform, processor model reads the accelerator results from SRAM using SRAM controller and compares them with its results.

Verilog testbench has behavioral power-on-reset and clock generation, behavioral models of an image sensor and a Static RAM (SRAM). After receiving a frame capture signal from the ASIC, the image sensor model captures an 8x8 grayscale image and sends this image to the ASIC with an 8 bit parallel data interface. The SRAM model models a 1 MB off-chip SRAM (32Kx32) with the following interface: Address (15-bit), Data (32-bit), CS (1-bit), WE (1-bit), OE (1-bit).