KS0032

16 COM / 80 SEG DRIVER & CONTROLLER FOR STN LCD

June. 1999.

Ver. 0.5

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KS0032 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	Feb.1999
0.1	ECKON pad added POR circuit added	Mar.1999
0.2	Page 5: (4/5) x V0 → (3/5) x V0 (3/5) x V0 → (2/5) x V0 Page 6: E_RD signal description is changed E_RD: Active low signal for writing command in 6800 mode or high enable signal for reading command in 8080 mode. → E_RD: Active low signal for writing command or high enable signal for reading command in 6800 mode, low enable signal for reading command in 8080 mode.	Apr.1999
0.3	Page 6: LCD DRIVER OUTPUT added Page 18: Power ON / OFF timing added Page 29: I_{DD1} (V_{DD} = 2.4~3.6V): 150μA → 50μA Page 30: I_{DD1} (V_{DD} = 3.6~5.5V): 250μA → 80μA	May.1999
0.4	Page 1, 2, 11: CGROM character size is changed from 256 to 254.	Jun.1999
0.5	Page 6: RW_WR active low -> active high Page 6: RW_WR active low -> low enable Page 20: Wait for more than 1.2us or Busy Check -> delete “or Busy Check” Page 21: Wait for more than 1.2us or Busy Check -> delete “or Busy Check”	Jun.1999

CONTENTS

INTRODUCTION

This character driver and controller LSI for liquid crystal dot matrix display systems can display 2-line of 16 characters with the 5 x 8 dots format. It is capable of interfacing various microprocessors, supporting the 4-bit or 8-bit parallel mode. Voltage follower and bias circuit is built in the IC.

FEATURES

Driver Output Circuits

– 16 common outputs / 80 segment outputs

Applicable Duty Ratio

Font size	Display size	Duty	Contents of outputs
5 x 8	2-line x 16 characters	1/16	2 x 16 characters

On-chip Display Data RAM

– Character Generator ROM (CGROM): 10,160 bits (254 characters x 5 x 8 dots)
– Character Generator RAM (CGRAM): 80 bits (2 characters x 5 x 8 dots)
– Display Data RAM (DDRAM): 256 bits (16 characters x 2-line)

Microprocessor Interface

– 8-bit parallel interface with 6800-series or 8080-series MPU
– 4-bit parallel interface with 6800-series or 8080-series MPU

Function Set

– Simple instruction set
– COM / SEG bi-directional (4 types of LCD application available)
– Hardware reset (RESETB)

On-chip Analog Circuit

– Internal RC oscillator circuit
– Voltage follower & bias circuit
– Automatic power on reset circuit

Operating Voltage Range

– Supply voltage (V_{DD}): 2.4 to 5.5V
– LCD driving voltage (V_{LCD} = V0 - V_{SS}): 6.0V Max.

Low Power Consumption

Package Type

– Gold bumped chip

BLOCK DIAGRAM

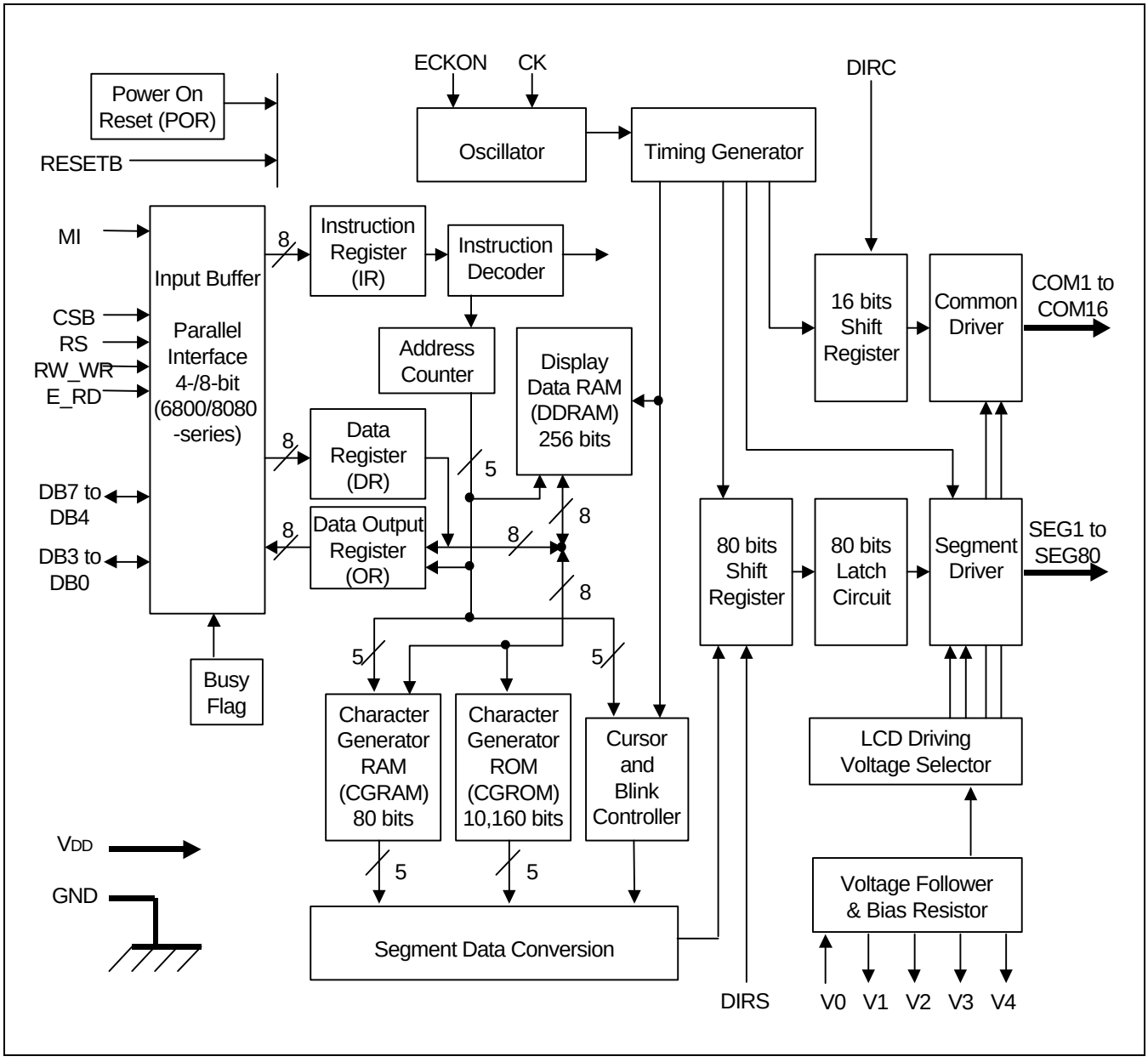


Figure 1. Block Diagram

PAD CONFIGURATION

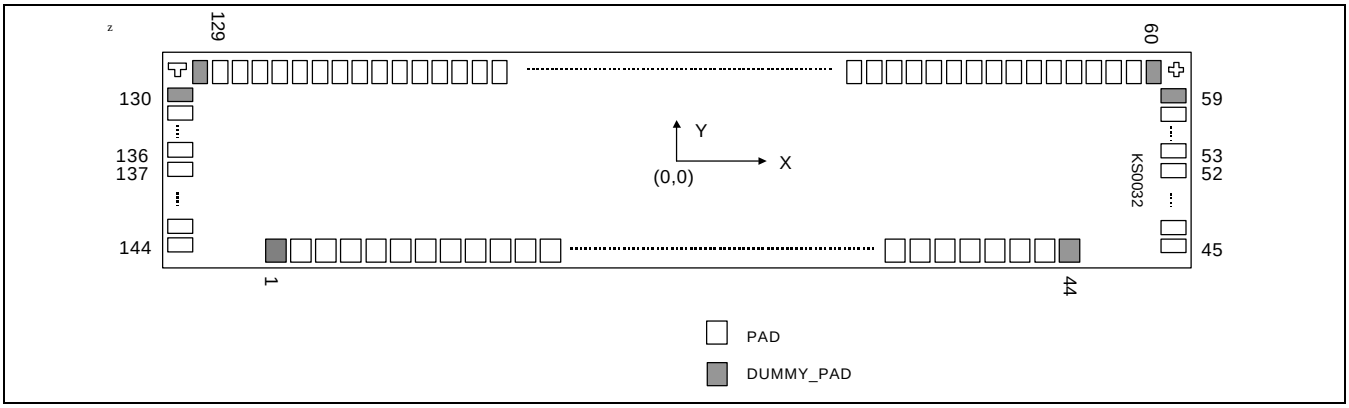
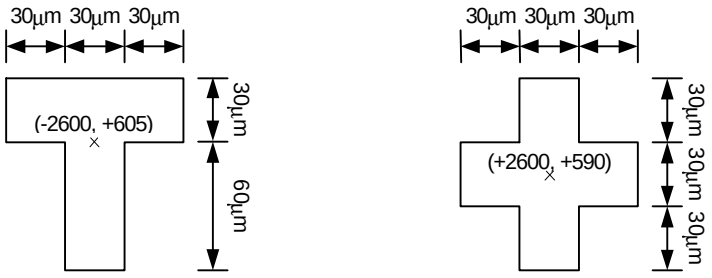


Figure 2. KS0032 Chip Configuration

Table 1. KS0032 Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	5430	1410	µm
Pad pitch	1 to 44	90		
	45 to 144	70		
Bumped pad size	1 to 44	52	92	
	45 to 59	92	42	
	60 to 129	42	92	
	130 to 144	92	42	
Bumped pad height	1 to 144	17 (Typ.)		

COG Align Key Coordinate



PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: μm]

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	DUMMY	-1935	-595	51	COM7	2605	-135	101	SEG47	-455	595
2	VSS	-1845	-595	52	COM8	2605	-65	102	SEG48	-525	595
3	VSS	-1755	-595	53	SEG1	2605	5	103	SEG49	-595	595
4	VSS	-1665	-595	54	SEG2	2605	75	104	SEG50	-665	595
5	ECKON	-1575	-595	55	SEG3	2605	145	105	SEG51	-735	595
6	VDD	-1485	-595	56	SEG4	2605	215	106	SEG52	-805	595
7	V4	-1395	-595	57	SEG5	2605	285	107	SEG53	-875	595
8	V3	-1305	-595	58	SEG6	2605	355	108	SEG54	-945	595
9	V2	-1215	-595	59	DUMMY	2605	425	109	SEG55	-1015	595
10	V1	-1125	-595	60	DUMMY	2415	595	110	SEG56	-1085	595
11	CK	-1035	-595	61	SEG7	2345	595	111	SEG57	-1155	595
12	VDD	-945	-595	62	SEG8	2275	595	112	SEG58	-1225	595
13	VDD	-855	-595	63	SEG9	2205	595	113	SEG59	-1295	595
14	VDD	-765	-595	64	SEG10	2135	595	114	SEG60	-1365	595
15	V0	-675	-595	65	SEG11	2065	595	115	SEG61	-1435	595
16	V0	-585	-595	66	SEG12	1995	595	116	SEG62	-1505	595
17	VDD	-495	-595	67	SEG13	1925	595	117	SEG63	-1575	595
18	VDD	-405	-595	68	SEG14	1855	595	118	SEG64	-1645	595
19	VDD	-315	-595	69	SEG15	1785	595	119	SEG65	-1715	595
20	RESETB	-225	-595	70	SEG16	1715	595	120	SEG66	-1785	595
21	RS	-135	-595	71	SEG17	1645	595	121	SEG67	-1855	595
22	RW_WR	-45	-595	72	SEG18	1575	595	122	SEG68	-1925	595
23	VSS	45	-595	73	SEG19	1505	595	123	SEG69	-1995	595
24	E_RD	135	-595	74	SEG20	1435	595	124	SEG70	-2065	595
25	VDD	225	-595	75	SEG21	1365	595	125	SEG71	-2135	595
26	DB0	315	-595	76	SEG22	1295	595	126	SEG72	-2205	595
27	DB1	405	-595	77	SEG23	1225	595	127	SEG73	-2275	595
28	DB2	495	-595	78	SEG24	1155	595	128	SEG74	-2345	595
29	DB3	585	-595	79	SEG25	1085	595	129	DUMMY	-2415	595
30	DB4	675	-595	80	SEG26	1015	595	130	DUMMY	-2605	425
31	DB5	765	-595	81	SEG27	945	595	131	SEG75	-2605	355
32	DB6	855	-595	82	SEG28	875	595	132	SEG76	-2605	285
33	DB7	945	-595	83	SEG29	805	595	133	SEG77	-2605	215
34	CSB	1035	-595	84	SEG30	735	595	134	SEG78	-2605	145
35	VSS	1125	-595	85	SEG31	665	595	135	SEG79	-2605	75
36	MI	1215	-595	86	SEG32	595	595	136	SEG80	-2605	5
37	VDD	1305	-595	87	SEG33	525	595	137	COM16	-2605	-65
38	TEST	1395	-595	88	SEG34	455	595	138	COM15	-2605	-135
39	VSS	1485	-595	89	SEG35	385	595	139	COM14	-2605	-205
40	DIRC	1575	-595	90	SEG36	315	595	140	COM13	-2605	-275
41	VDD	1665	-595	91	SEG37	245	595	141	COM12	-2605	-345
42	DIRS	1755	-595	92	SEG38	175	595	142	COM11	-2605	-415
43	VSS	1845	-595	93	SEG39	105	595	143	COM10	-2605	-485
44	DUMMY	1935	-595	94	SEG40	35	595	144	COM9	-2605	-555
45	COM1	2605	-555	95	SEG41	-35	595	145			
46	COM2	2605	-485	96	SEG42	-105	595	146			
47	COM3	2605	-415	97	SEG43	-175	595	147			
48	COM4	2605	-345	98	SEG44	-245	595	148			
49	COM5	2605	-275	99	SEG45	-315	595	149			
50	COM6	2605	-205	100	SEG46	-385	595	150			

PIN DESCRIPTION

POWER SUPPLY

Table 3. Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>VDD</td><td>Supply</td><td>Power supply</td></tr>
<tr><td>VSS</td><td>Supply</td><td>Ground</td></tr>
<tr><td>V0</td><td>I</td><td>Bias voltage Input for LCD driving</td></tr>
<tr><td>V1
V2
V3
V4</td><td>O</td><td>LCD driving voltage outputs.
Voltages should have the following relationship;
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS
These voltages are generated as following table.
<table>
<tr><th>LCD bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/5 bias</td><td>(4/5) x V0</td><td>(3/5) x V0</td><td>(2/5) x V0</td><td>(1/5) x V0</td></tr>
</table></td></tr>
</table>

SYSTEM CONTROL

Table 3. Pin Description (Continued)

Name	I/O	Description
ECKON	I	Clock source selection input When ECKON = "High", External clock by CK pin is used as system clock, and internal oscillator circuit is turned OFF. When ECKON = "Low", internal oscillator is used.
CK	I	External clock input (When ECKON = "High") It must be fixed "High" or "Low" when the internal oscillation circuit is used (When ECKON = "Low").
MI	I	MPU interface selection input MI = "Low", 8080-series MPU MI = "High", 6800-series MPU
DIRC	I	COM direction selection input When DIRC = "Low", COM1 → COM2 - - - - → COM15 → COM16 When DIRC = "High", COM16 → COM15 - - - - → COM2 → COM1
DIRS	I	SEG direction selection input When DIRS = "Low", SEG1 → SEG2 - - - - → SEG79 → SEG80 When DIRS = "High", SEG80 → SEG79 - - - - → SEG2 → SEG1

MPU INTERFACE

Table 3. Pin Description (Continued)

Name	I/O	Description
RESETB	I	Reset input Initialization is performed by "Low" level sensing of the RESETB signal.
CSB	I	Chip selection input KS0032 is selected while CSB is "Low".
RS	I	Register selection input When RS = "Low", instruction register When RS = "High", data register
RW_WR	I	In 8080-series MPU interface mode, this pin is connected to WR pin of MPU and is an active high write signal. In 6800-series MPU interface mode, this pin is connected to R/W pin of MPU. When RW_WR = "High", read mode When RW_WR = "Low", write mode
E_RD	I	In 8080-series MPU interface mode, this pin is connected to RD pin of MPU and is a low enable read signal. In 6800-series MPU interface mode, this pin is connected to E pin of MPU and enables read or write command according to RW_WR signal.
DB0 to DB3 DB4 to DB7	I/O	When 8-bit interface mode, used as bi-directional data bus DB0 to DB7 During 4-bit bus mode, only DB4 to DB7 are used. In this case DB0 - DB3 pins are don't care (connect to "High", "Low" or open).

LCD DRIVER OUTPUT

Table 3. Pin Description (Continued)

Name	I/O	Description
COM1 to COM16	O	Common signal output for character display
SEG1 to SEG80	O	Segment signal output for character display

TEST

Table 3. Pin Description (Continued)

Name	I/O	Description
TEST	I	Test pin This pin is not used for normal operation and should be connect to "Low".

*NOTE: **DUMMY – These pins should be opened (floated).**

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

KS0032 has two kinds of interface type with MPU: 4-bit bus or 8-bit bus. 4-bit bus and 8-bit bus is selected by the DL bit in the instruction register, and 6800-series MPU or 8080-series MPU is selected by MI pin.

Table 4. Various Kinds of MPU Interface according to MI and DL Bit

MI	DL	CSB	RS	RW_WR	E_RD	DB0 to DB3	DB4 to DB7
6800 series (H)	8-bit (H)	CSB	RS	R/W	E	DB0 to DB3	DB4 to DB7
	4-bit (L)	CSB	RS	R/W	E	-	DB4 to DB7
8080 series (L)	8-bit (H)	CSB	RS	WR	RD	DB0 to DB3	DB4 to DB7
	4-bit (L)	CSB	RS	WR	RD	-	DB4 to DB7

NOTE: "-" - Don't care ("High", "Low" or Open)
(H): fixed "High" (V_{DD})
(L): fixed "Low" (V_{SS})

MI: "High" = 6800-series MPU, "Low" = 8080-series MPU
DL: "High" = 8-bit mode, "Low" = 4-bit mode
CSB: "High" = chip is not selected, "Low" = chip is selected
RS: "High" = data register, "Low" = instruction register
RW_WR: read / write indicating signal in 6800 mode, active high signal for writing command in 8080 mode.
E_RD: Active low signal for writing command or high enable signal for reading command in 6800 mode, low enable signal for reading command in 8080 mode.

Parallel Interface

During writing operation, two 8-bit registers, data register (DR) and instruction register (IR), are used. The data register (DR) is used as temporary data storage place for being written into DDRAM / CGRAM. Target RAM is selected by RAM address set instruction. The Instruction register (IR) is used only to store instruction code transferred from MPU. To select DR or IR register, RS input pin is used.

During reading operation, 8-bit output data register (OR) is used. The output data register (OR) is used as temporary data storage place for being read from DDRAM / CGRAM. Destination RAM is selected by RAM address set instruction. After RAM address set, the first reading in the 8-bit bus mode (first and second reading in the 4-bit bus mode) is a dummy cycle (figure 3, 4, 5, 6). The valid data comes from the second reading in the 8-bit bus mode (from the 3rd reading in 4-bit bus mode). The dummy cycle makes the address counter (AC) indicate the correct address. So it is recommended to set address before writing. The instruction read operation is supported for indicating internal operation is being processed (Busy Flag).

In the 4-bit bus mode, it is needed to transfer 4-bit data (through DB4 to DB7) by two times. The high order bits (for 8-bit mode DB4 to DB7) are transferred before the low order bits (for 8-bit mode DB0 to DB3) in read and write transaction. The DB0 to DB3 pins are floated in this 4-bit bus mode.

After RESETB operation, KS0032 considers the first 4-bit data from MPU as the high order bits in the 4-bit bus mode.

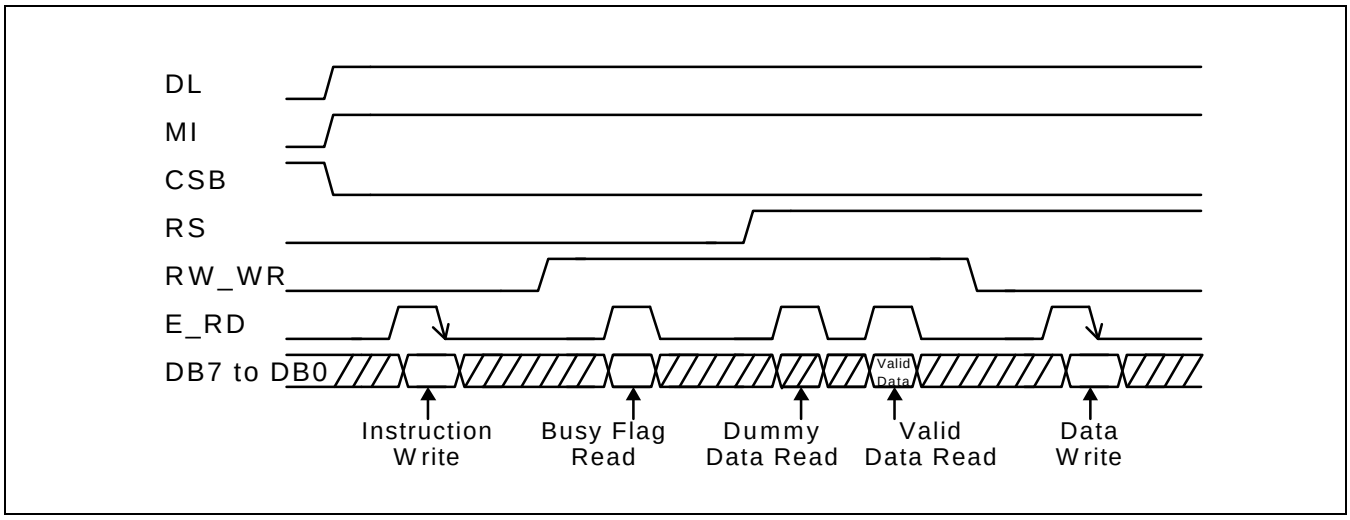


Figure 3. Timing Diagram of 8-bit Parallel Bus Mode Data Transfer (6800-series MPU Mode)

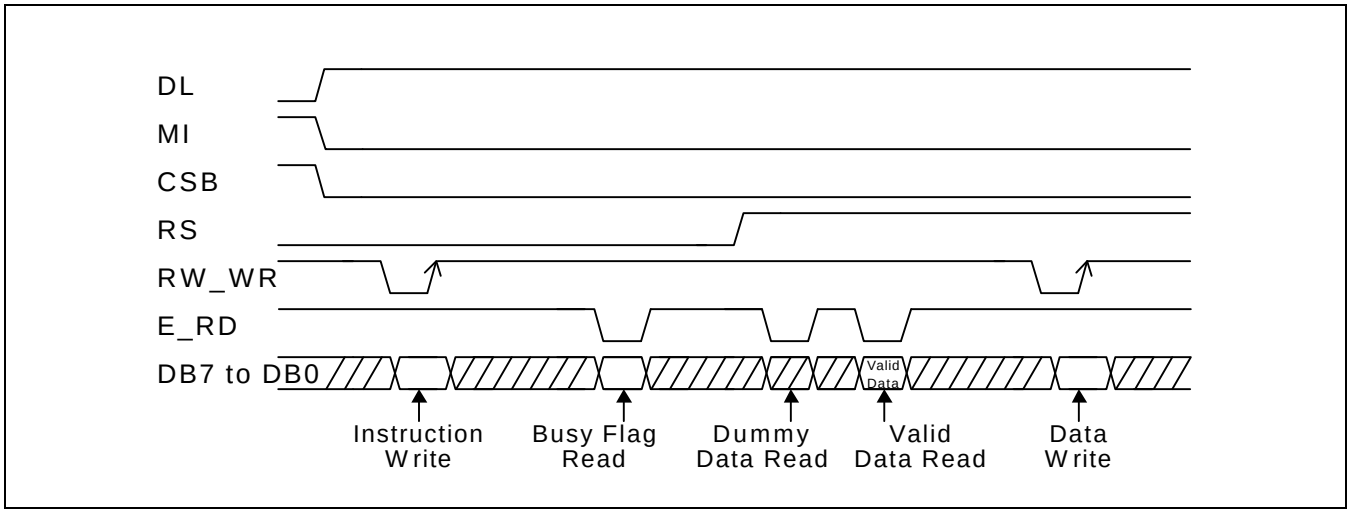


Figure 4. Timing Diagram of 8-bit Parallel Bus Mode Data Transfer (8080-series MPU Mode)

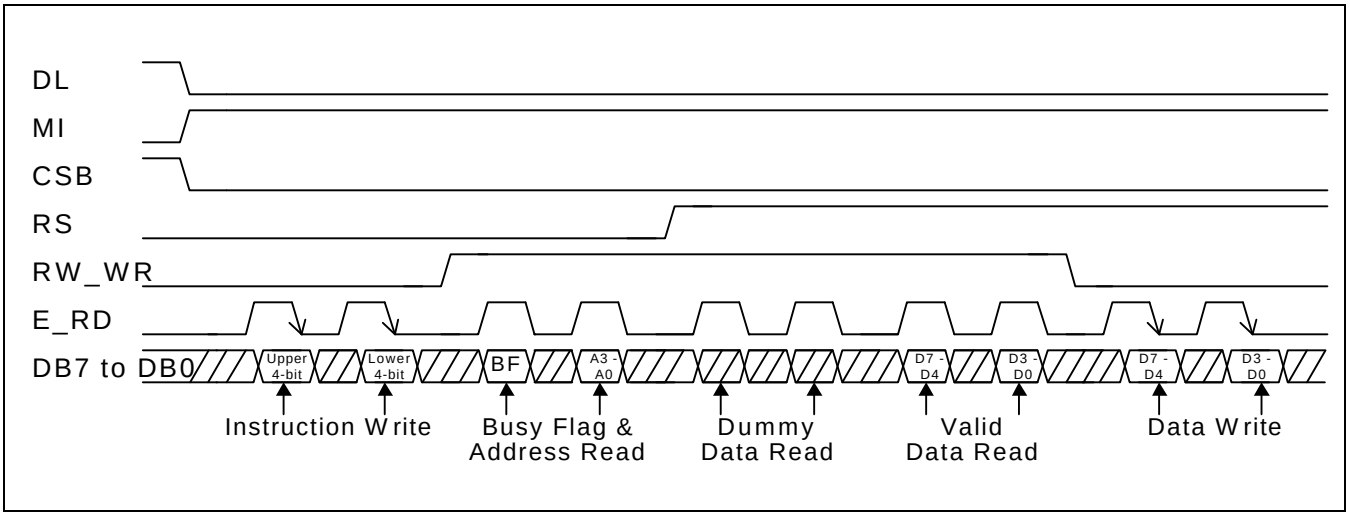


Figure 5. Timing Diagram of 4-bit Parallel Bus Mode Data Transfer (6800-series MPU Mode)

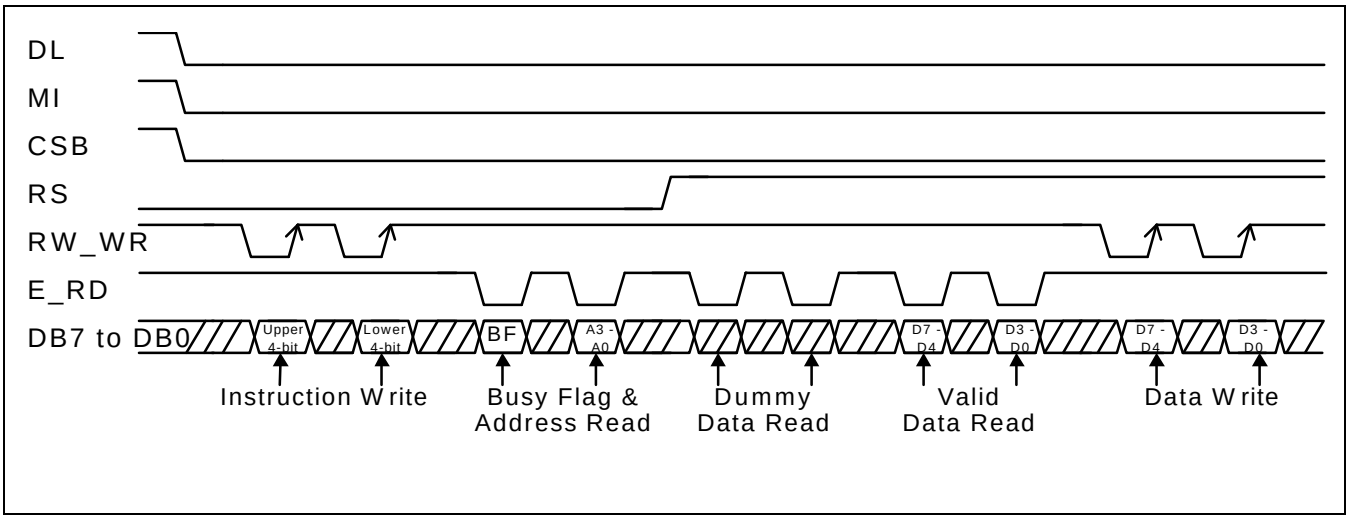


Figure 6. Timing Diagram of 4-bit Parallel Bus Mode Data Transfer (8080-series MPU Mode)

Busy Flag

When DB7 is "High" in read status operation, it indicates that the internal operation is in busy status and can accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, except display clear instruction.

ADDRESS COUNTER (AC)

Address Counter (AC) in KS0032 stores DDRAM / CGRAM address. After writing into or reading from DDRAM / CGRAM, AC is automatically increased or decreased by 1 according to the entry mode.

DISPLAY DATA RAM (DDRAM)

DDRAM stores display data of maximum 32 x 8 bits (32 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

(a) Display shift is not performed

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	00
41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	40

(b) Display shift left is performed

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
4F	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

(c) Display shift right is performed

Figure 7. DDRAM Address

CHARACTER GENERATOR ROM (CGROM)

CGROM has 5 x 8-dot 254 characters. The CGROM character code 00h and 01h are CGRAM character data area.

Table 5. CGROM Character Code (00)

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CGRAM CHAR #1															
LLLH	CGRAM CHAR #2															
LLHL																
LLHH																
LHLL																
LHLH																
LHHL																
LHHH																
HLLL																
HLLH																
HLHL																
HLHH																
HHLL																
HHLH																
HHHL																
HHHH																

CHARACTER GENERATOR RAM (CGRAM)

CGRAM has up to 5 x 8-dot 2 characters. By writing font data to CGRAM, user defined character can be used.

Table 6. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

Character code (DDRAM data)	CGRAM address	CGRAM data	Pattern number
D7 D6 D5 D4 D3 D2 D1 D0	A3 A2 A1 A0	P7 P6 P5 P4 P3 P2 P1 P0	
0 0 0 0 0 0 0 0 (00h)	0 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1	- - - 0 1 0 1 0 - - - 1 0 1 0 1 - - - 0 1 0 1 0 - - - 1 0 1 0 1 - - - 0 1 0 1 0 - - - 1 0 1 0 1 - - - 0 1 0 1 0 - - - 1 0 1 0 1	Pattern 1
0 0 0 0 0 0 0 1 (01h)	1 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	- - - 0 0 0 0 0 - - - 1 1 1 1 1 - - - 0 0 0 0 0 - - - 1 1 1 1 1 - - - 0 0 0 0 0 - - - 1 1 1 1 1 - - - 0 0 0 0 0 - - - 1 1 1 1 1	Pattern 2

NOTE: "-" - Don't care

LCD DRIVER CIRCUIT

LCD Driver circuit has 16 common and 80 segment signals for driving LCD. Data from CGRAM / CGROM are transferred to 80-bit segment register serially, and then they are stored to 80-bit shift latch. COM1 to COM16 have 1/16 duty ratio. SEG bi-directional function is selected by DIRS input, and COM shift direction is selected by DIRC input.

Table 7. SEG Data Shift Direction

DIRS pin	SEG data shift direction
Low	SEG1 → SEG2 → SEG3 → - - - - - - - → SEG78 → SEG79 → SEG80
High	SEG80 → SEG79 → SEG78 → - - - - - - - → SEG3 → SEG2 → SEG1

Table 8. COM Data Shift Direction

DIRC pin	COM data shift direction
Low	COM1 → COM2 → COM3 → - - - - - - - - → COM14 → COM15 → COM16
High	COM16 → COM15 → COM14 → - - - - - - - - → COM3 → COM2 → COM1

INSTRUCTION DESCRIPTION

Table 9. Instruction Table

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
*Clear display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC
Return home	0	0	0	0	0	0	0	0	1	-	DDRAM address is set to 00h from AC and the cursor returns to 00h position. The contents of DDRAM are not changed.
Entry mode set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display
Display ON / OFF control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) ON / OFF control
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data
Function set	0	0	0	0	1	DL	-	-	-	-	Set interface data length (DL: 4-bit / 8-bit) instruction
CGRAM address set	0	0	0	1	0	0	A3	A2	A1	A0	Set CGRAM address in address counter.
DDRAM address set	0	0	1	A6	A5	A4	A3	A2	A1	A0	Set DDRAM address in address counter.
Read busy flag and address	0	1	BF	A6	A5	A4	A3	A2	A1	A0	Whether in internal operation or not can be known by reading BF, The contents of address counter can also be read
Write data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into DDRAM / CGRAM
Read data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from DDRAM / CGRAM

("-": Don't care)

NOTES:

1. Instruction execution time depends on the internal process time of KS0032, therefore it is necessary to provide a time larger than one MPU interface cycle time (tc) between execution of two successive instructions.
2. "Clear Display" instruction has 850µs execution time (when fosc = 40.0kHz), so check the Busy flag or wait for more than 850µs after using "Clear Display" instruction.

Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code of CGROM) to all the DDRAM address, and set the DDRAM address to "00H" into AC (address counter). For this instruction, the CGROM address "20H" have to set space code. If the display position has shifted then it returns to the original positions. Namely, when display data is shifted and cursor or blinking is displayed, bring the cursor to the left edge on first line of the display. It makes entry mode to increment (I/D = "High").

Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Return Home instruction field makes cursor return home. DDRAM address is set to 00h from AC and the cursor returns to 00h position. The contents of DDRAM are not changed.

Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display after data writing or reading instruction.

I/D: Increment / decrement of DDRAM / CGRAM address (cursor or blink)
After DDRAM / CGRAM data write/read operation, DDRAM/CGRAM address is increased (I/D = "High") or decreased (I/D = "Low") by 1. So in case of DDRAM data transfer operation and cursor or blink is turned on, cursor or blink moves to right (I/D = "High") or left (I/D = "Low"), but in CGRAM data transfer operation, cursor or blink does not move.

SH: Shift of entire display
When DDRAM read (CGRAM read/write) operation or SH = "Low", entire display is not shift. Only when SH = "High" and DDRAM write operation, entire display is shift according to I/D value (I/D = "1": shift left, I/D = "0": shift right).

Display ON / OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display / cursor/blink ON / OFF 1 bit register

D: Display ON / OFF Control Bit
When D = "High", entire display is turned ON.
When D = "Low", entire display is turned OFF, but display data is remained in DDRAM.

C: Cursor ON / OFF Control Bit
When C = "High", cursor is turned ON.
When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

B: Cursor Blink ON / OFF Control Bit
When B = "High", cursor blink is ON, that performs alternate between all high data (black pattern) and display character at the cursor position.
When B = "Low", blink is OFF.

Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Without writing or reading of display data, shift right / left the cursor position or display. This instruction is used to correct or search display data (refer to table 10). Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

Table 10. Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	-	-	-	-

DL: Interface Data Length Control Bit

When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU.
When 4-bit bus mode, it needs to transfer 4-bit data by two times.

CGRAM Address Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	A3	A2	A1	A0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU for user defined character pattern. CGRAM address is from 00h to 0Fh.

DDRAM Address Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	A6	A5	A4	A3	A2	A1	A0

Set DDRAM address to AC. Before writing / reading data into / from the RAM, set the address by RAM Address Set instruction. Next, when data are written / read in succession, the address is automatically increased by 1 (when I/D = "High") or decreased by 1 (when I/D = "Low"). The address ranges are 00h to 0Fh (1st line) and 40h to 4Fh (2nd line).

Read Busy Flag and Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	A6	A5	A4	A3	A2	A1	A0

This instruction shows whether KS0032 is in internal operation or not. If the resultant BF is "High", it means the internal operation is in progress and you have to wait until BF to be "Low", and then the next instruction can be performed. In this instruction you can read also the value of address counter.

Write Data

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8- / 5- bit data to DDRAM / CGRAM. The selection of RAM from DDRAM / CGRAM is set by the previous address set instruction (DDRAM address set, CGRAM address set). After write operation, the address is automatically increased / decreased by 1, according to the entry mode.

Read Data

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8- / 5- bit data from DDRAM / CGRAM. The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, and the first data would be incorrect, because there is no time margin to transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction: it also transfers RAM data to output data register. After read operation address counter is automatically increased / decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, after this operation, AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction. RAM address is dummy data, so the correct RAM data come from the second read transaction. After reading operation, the address is increased by 1 automatically.

INITIALIZING

HARDWARE RESET

When the power is turned on, KS0032 is initialized automatically by the power on reset circuit (refer to figure 8). In case of RESETB pin becomes "Low" and durable the state for more than 1.2μs (VDD = 3V), KS0032 can be initialized too. During the initialization, the following instructions are executed, and BF (Busy Flag) is kept "High" (busy state) to the end of initialization.

Display Clear
All the DDRAM data is set to "20H"

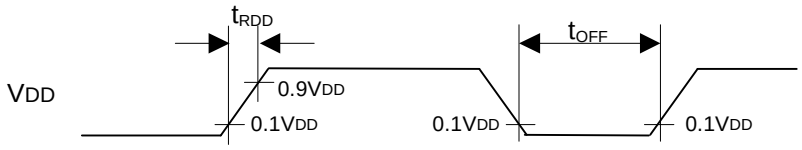
Return Home
Address counter = "00H"

Entry Mode Set Instruction
I/D = 1: Address counter is set to increment mode.
SH = 0: Entire display shift is disabled.

Display ON / OFF Control Instruction
C = 0: cursor OFF
B = 0: blink OFF
D = 0: display OFF

Function Set Instruction
DL = 1: 8-bit interface mode

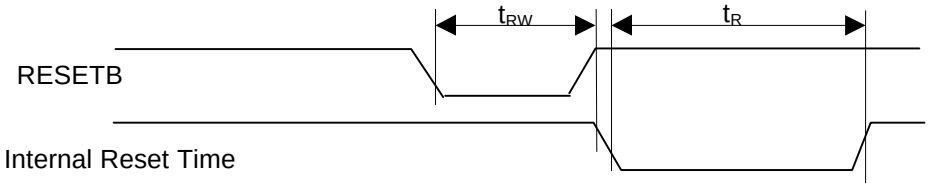
CGRAM / DDRAM Address
RAM address counter is set to "00H".



VDD Rising Time	t_{RDD}	≤ 1 ms
Power OFF Time	t_{OFF}	> 1 ms

Note: If the upper power conditions are not satisfied in power ON / OFF sequence, the internal Power On Reset (POR) circuit will not operates normally.

Figure 8. Power ON / OFF Timing



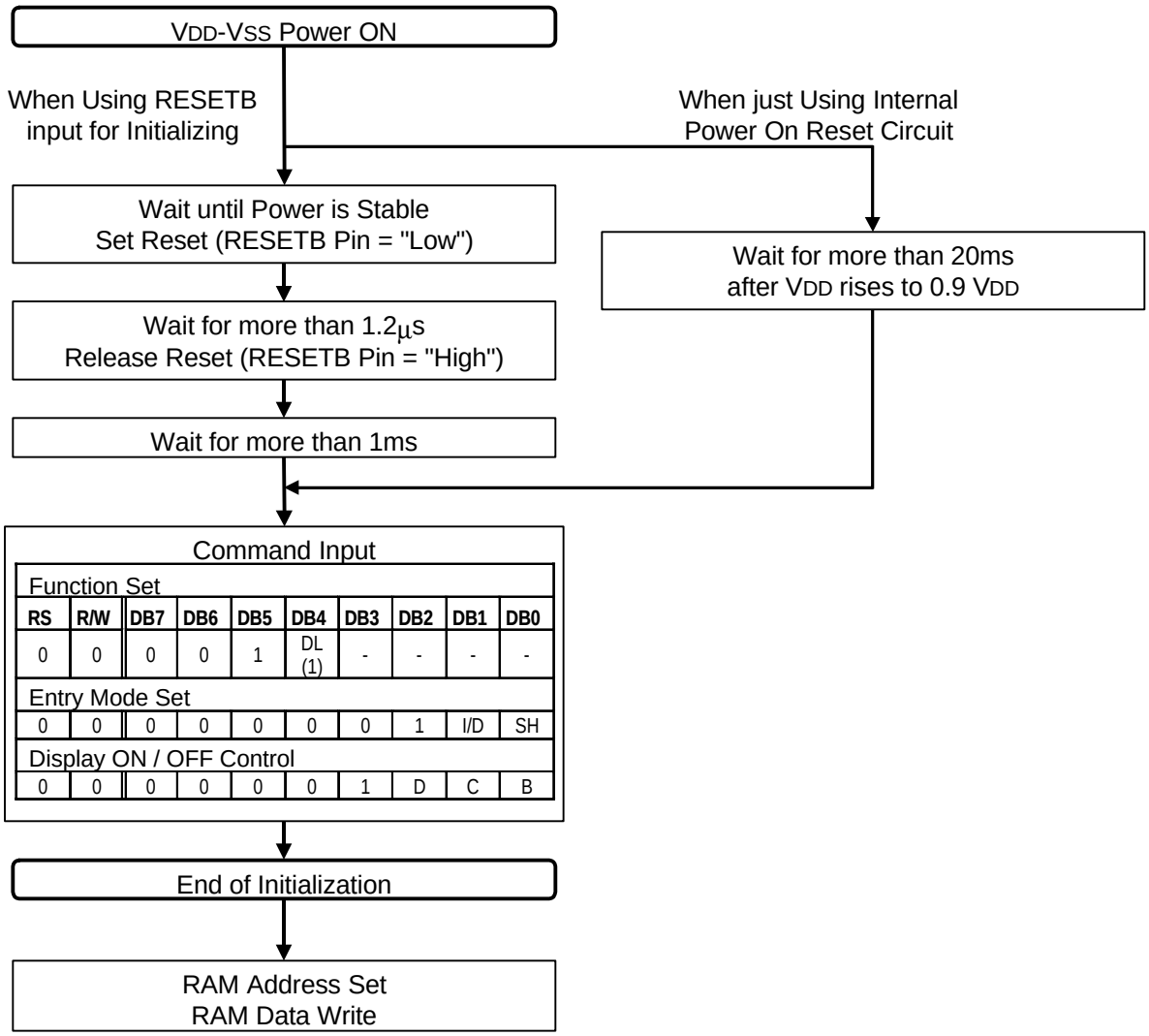
Reset Pulse Width	t_{RW}	1.2 µs
Reset Time	t_R	850 µs

Note: t_{RW} indicates the minimum RESETB duration for activate internal reset signal
t_R indicates reset completion time of internal circuit from the start of the internal reset signal (when fosc = 40.0kHz).

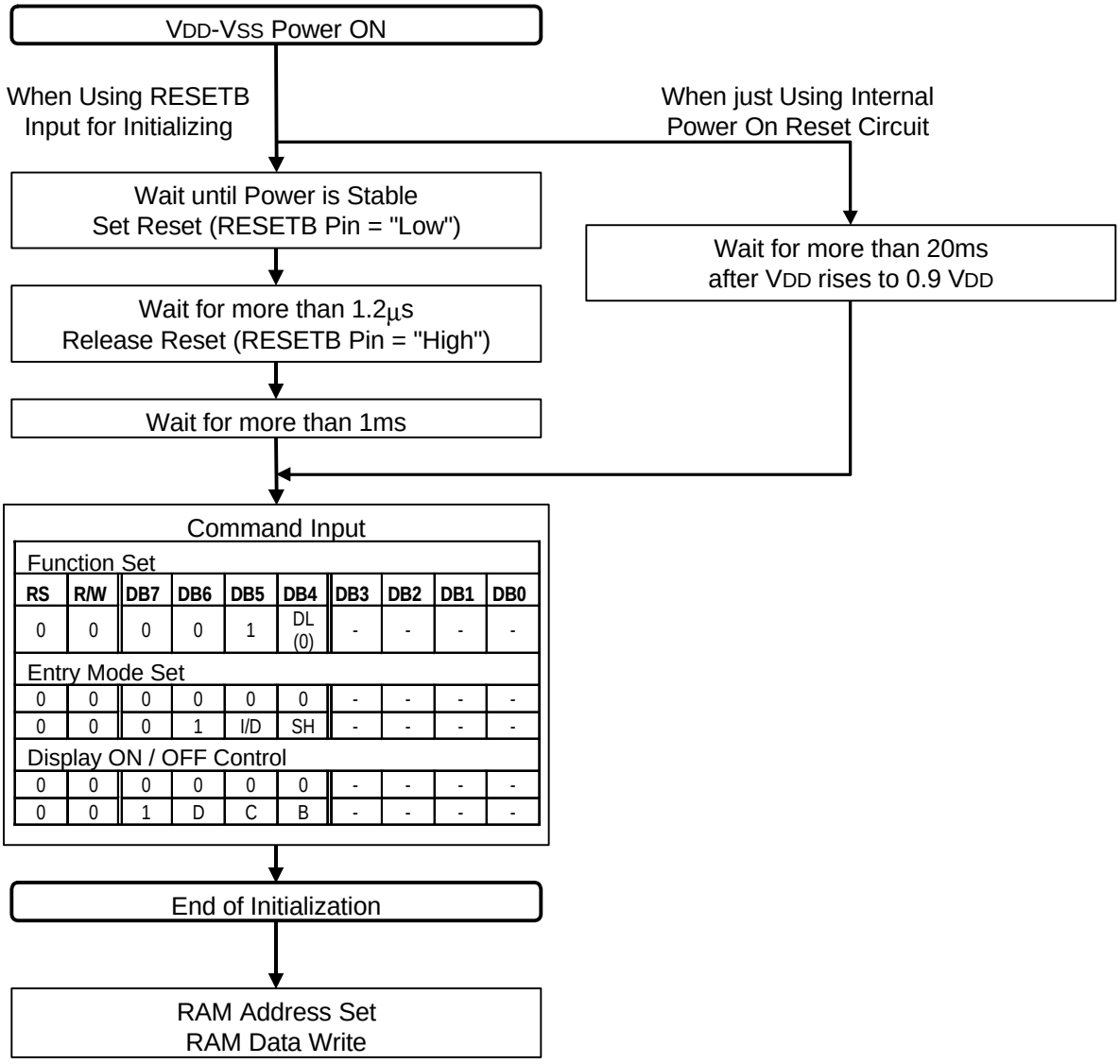
Figure 9. RESET Timing

INSTRUCTION INITIALIZING WITH RESET

8-bit Interface Mode (fosc = 40.0kHz)

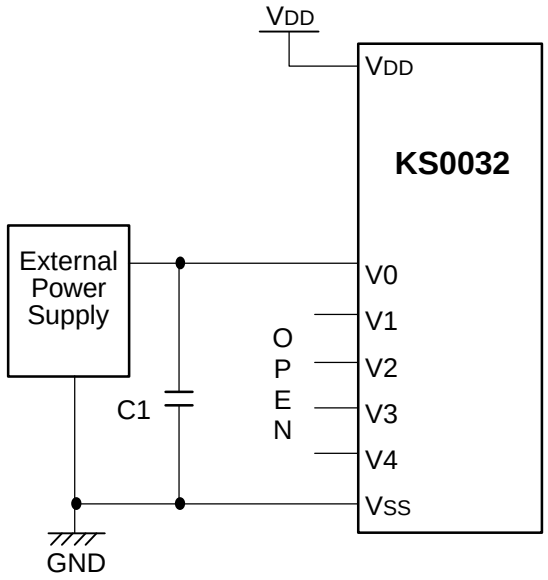


4-bit Interface Mode (fosc = 40.0kHz)



LCD DRIVING POWER SUPPLY CIRCUIT

The Power Supply circuit produces LCD panel driving voltage at low power consumption. The LCD driving Power Supply circuit consists of external voltage input and voltage follower.



* Recommended Capacitance value is 0.1 to 4.7μF

Figure 10. LCD Driving Power Connection

MPU INTERFACE

INTERFACING WITH 8080-SERIES MICROPROCESSORS

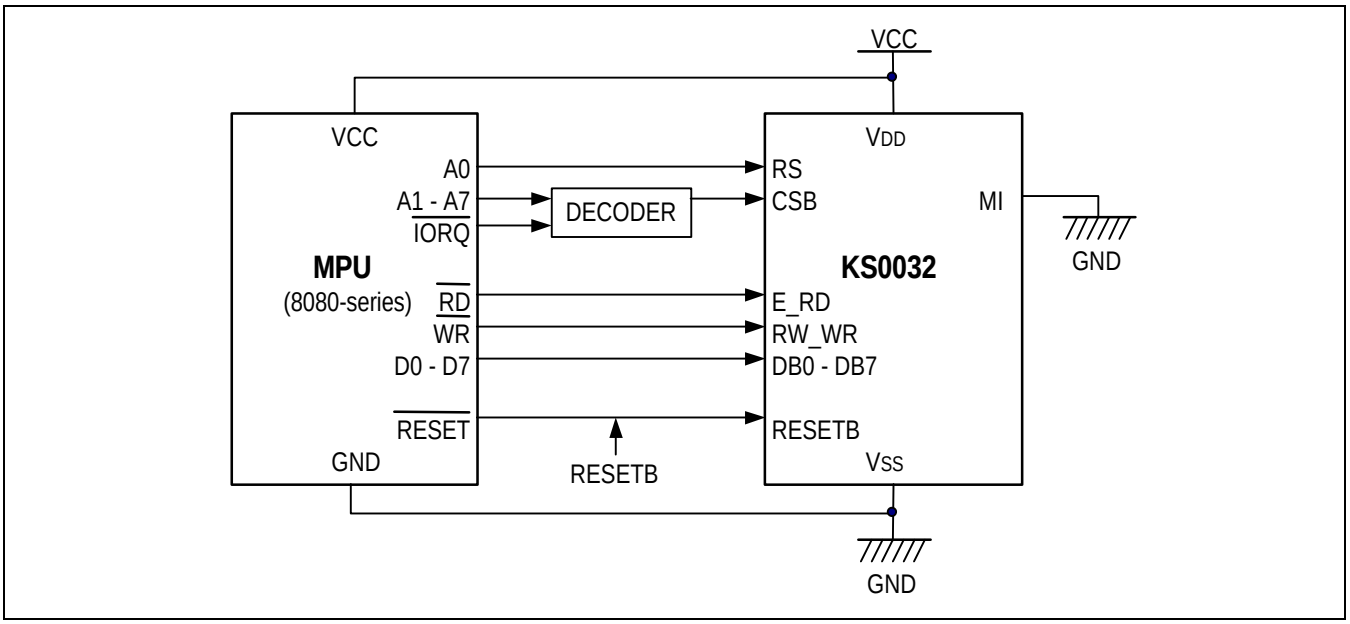


Figure 11. Interfacing with 8080-series MPU

INTERFACING WITH 6800-SERIES MICROPROCESSORS

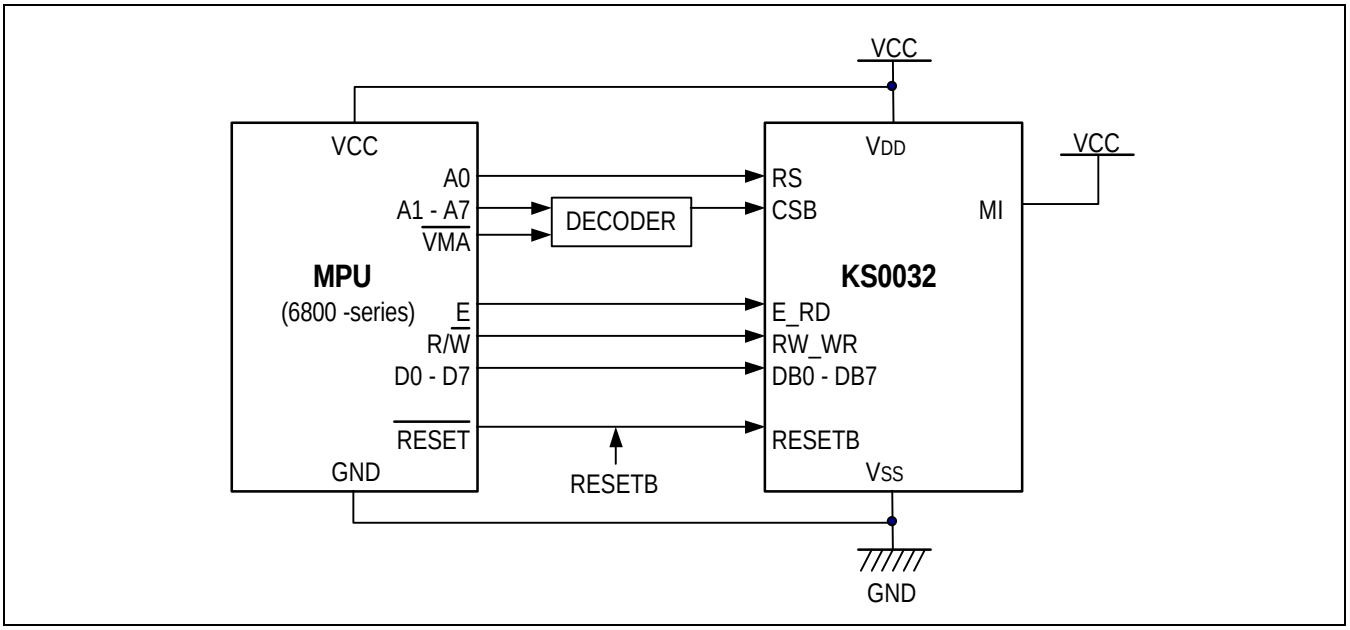


Figure 12. Interfacing with 6800-series MPU

APPLICATION INFORMATION FOR LCD PANEL

Chip Bottom & Lower View (DIRC = "0", DIRS = "0")

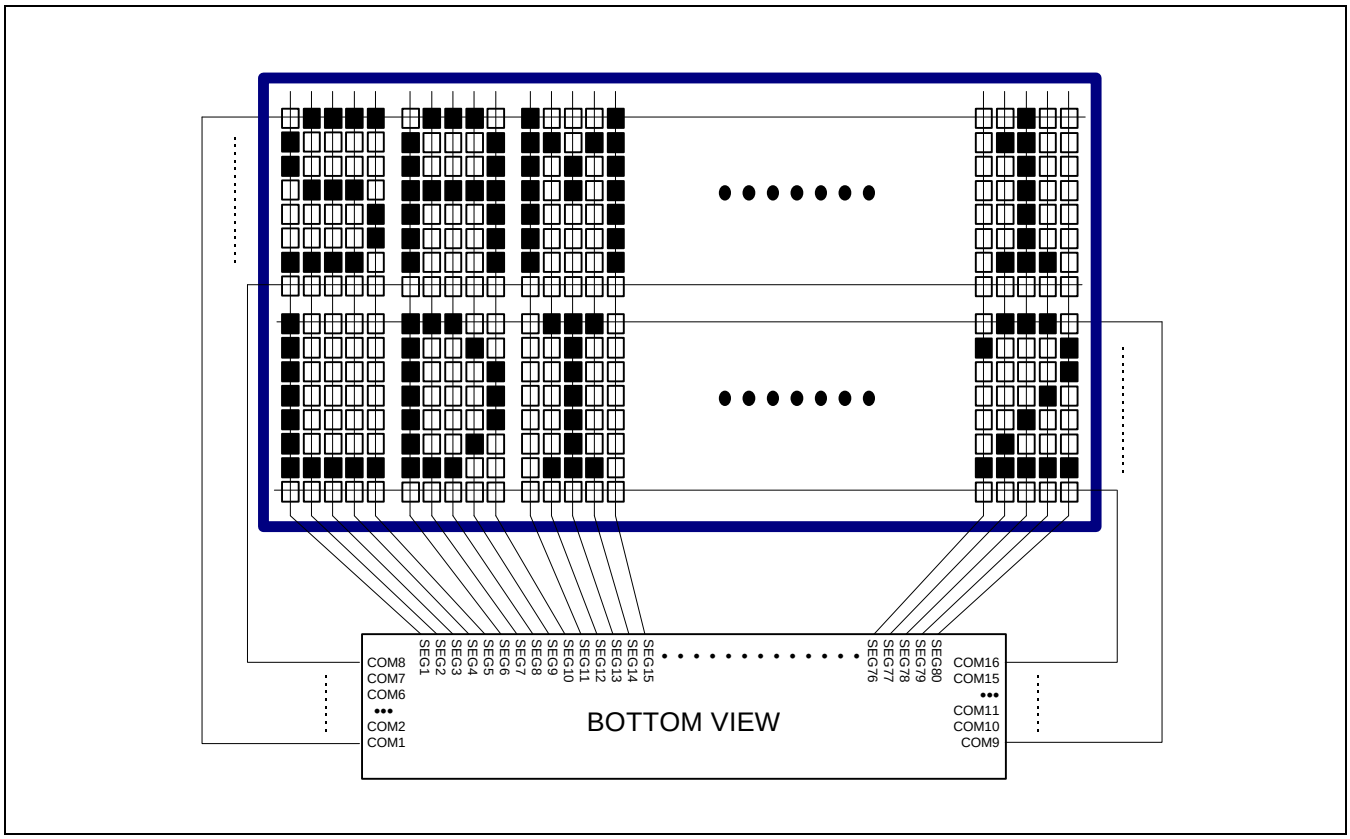


Figure 13. Chip Bottom & Lower View Interfacing with LCD Panel

Chip Bottom & Upper View (DIRC = "1", DIRS = "1")

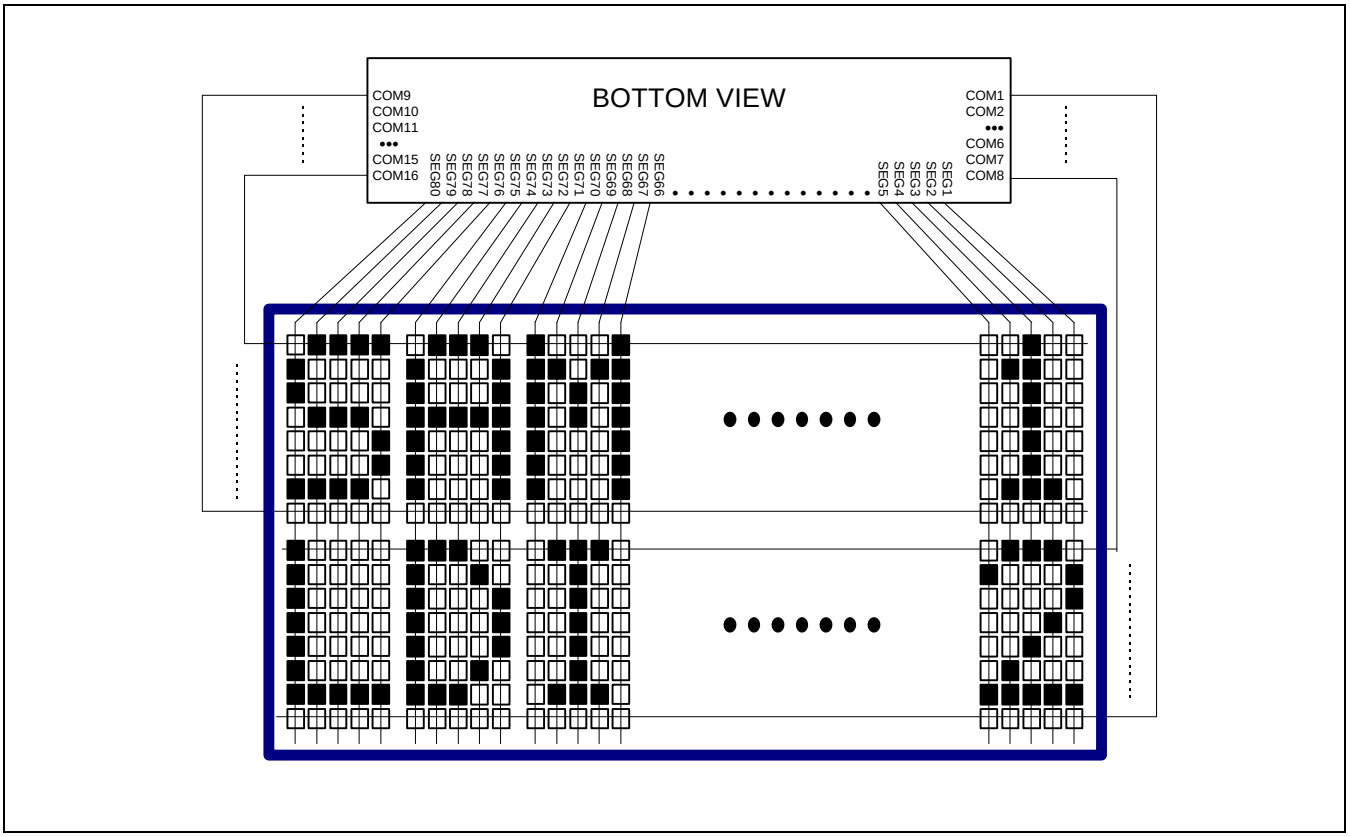


Figure 14. Chip Bottom & Upper View Interfacing with LCD Panel

Chip Top & Lower View (DIRC = "0", DIRS = "1")

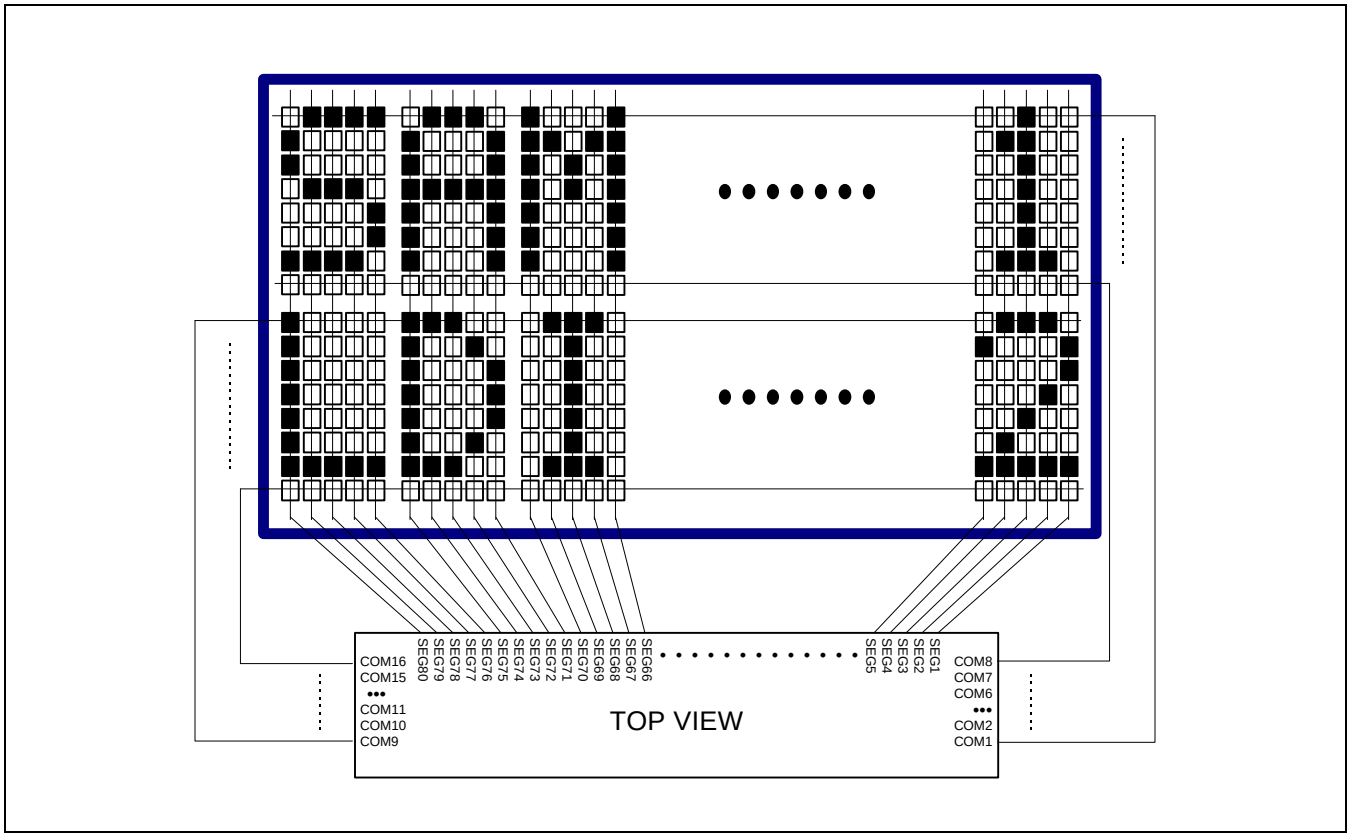


Figure 15. Chip Top & Lower View Interfacing with LCD Panel

Chip Top & Upper View (DIRC = "1", DIRS = "0")

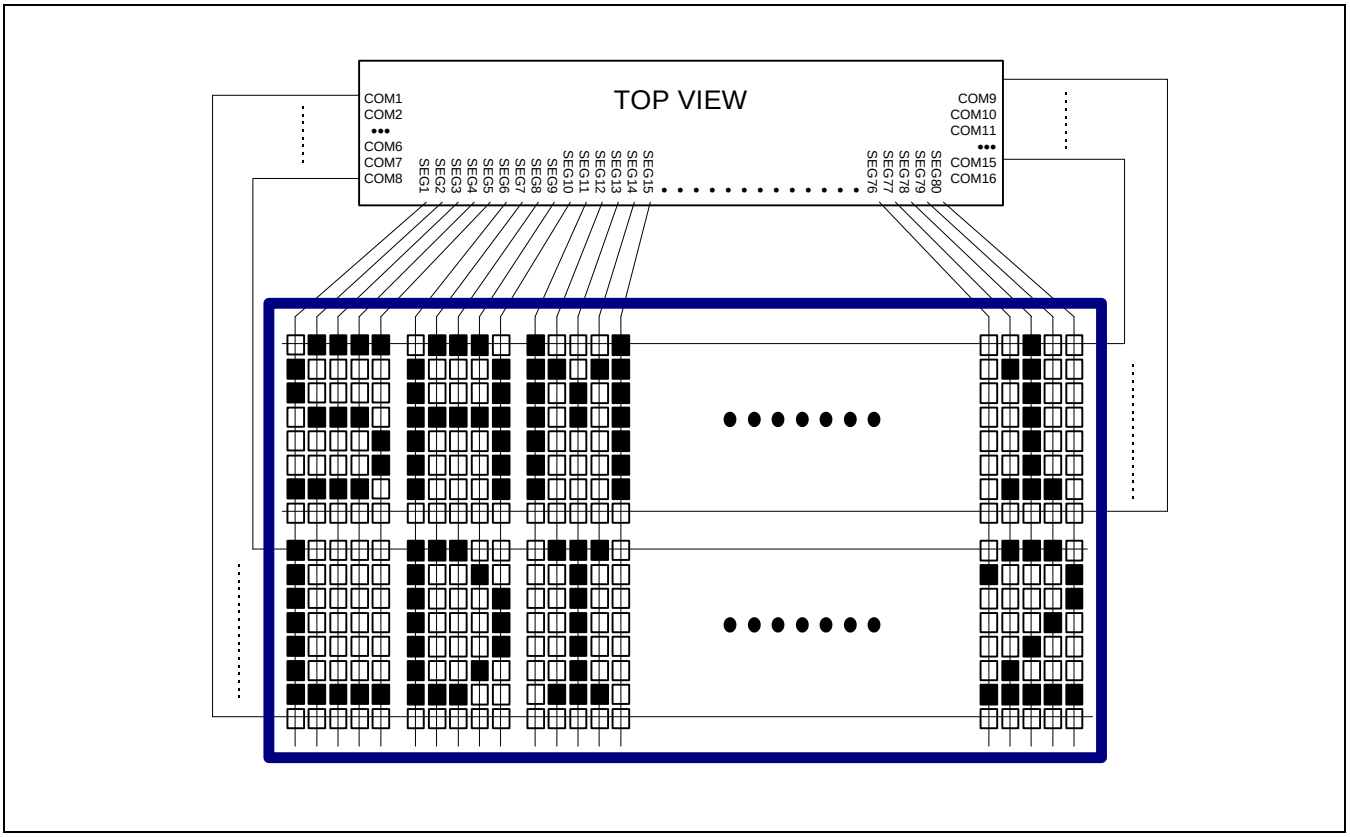
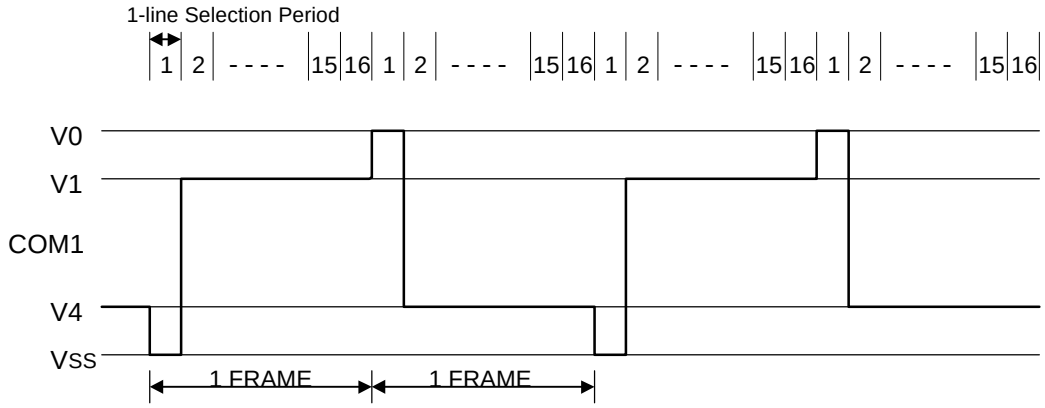


Figure 16. Chip Top & Upper View Interfacing with LCD Panel

FRAME FREQUENCY



1-line Selection Period = 16 Clock Pulses x 2 Division
One Frame = 32 x 16 x 25.0μs = 12.8ms (1 Clock = 25.0μs at fosc = 40.0kHz)
Frame Frequency = 1 / 12.8ms = 78Hz

Figure 17. Frame Frequency

MAXIMUM ABSOLUTE RATE

Table 11. Maximum Absolute Rate

Characteristics	Symbol	Value	Unit
Power supply voltage (1)	V_{DD}	-0.3 to +7.0	V
Power supply voltage (2)	V0	-0.3 to + 8.0	V
Input voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Operating temperature	T_{OPR}	-30 to +85	°C
Storage temperature	T_{STG}	-55 to +125	°C

NOTE1: All the voltage levels are based on V_{SS} = 0V.

NOTE2: Voltage greater than above may damage the circuit.

Voltage level: $V0 \geq V_{DD} \geq V_{SS}$

Voltage level: $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V_{SS}$

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Table 12. DC Characteristics

(V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	-	2.4	-	3.6	V
Supply current (V_{DD} = 3V, Ta = 25 °C)	I_{DD1}	Display operation V0 = 6V without load No access from MPU	-	-	50	µA
	I_{DD2}	Access operation from MPU fcyc = 200kHz	-	-	500	
Input voltage	V_{IH}	-	0.7V_{DD}	-	V_{DD}	V
	V_{IL}	-	V_{SS}	-	0.3V_{DD}	
Input leakage current	I_{LEAK}	V_{IN} = 0V to V_{DD}	-1	-	1	µA
R_{ON} resistance	R_{COM}	Io = ± 50µA	-	-	5	kΩ
	R_{SEG}	Io = ± 50µA	-	-	10	
Frame frequency	f_{FR}	V_{DD} = 3V, Ta = 25 °C	55	78	101	Hz
External clock frequency	f_{CK}	-	-	40.0	-	kHz
LCD driving voltage	V_{LCD}	V_{LCD} = V0 – V_{SS}	3.0	-	6.0	V

Table 12. DC Characteristics (Continued)

(V_{DD} = 3.6V to 5.5V, Ta = -30 to +85 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	-	3.6	-	5.5	V
Supply current (V_{DD} = 5V, Ta = 25 °C)	I_{DD1}	Display operation V0 = 6V without load No access from MPU	-	-	80	µA
	I_{DD2}	Access operation from MPU fcyc = 200kHz	-	-	1000	
Input voltage	V_{IH}	-	0.7V_{DD}	-	V_{DD}	V
	V_{IL}	-	V_{SS}	-	0.3V_{DD}	
Input leakage current	I_{LEAK}	V_{IN} = 0V to V_{DD}	-1	-	1	µA
R_{ON} resistance	R_{COM}	Io = ± 50µA	-	-	5	kΩ
	R_{SEG}	Io = ± 50µA	-	-	10	
Frame frequency	f_{FR}	V_{DD} = 3V, Ta = 25 °C	55	78	101	Hz
External clock frequency	f_{CK}	-	-	40.0	-	kHz
LCD driving voltage	V_{LCD}	V_{LCD} = V0 – V_{SS}	3.6	-	6.0	V

AC CHARACTERISTICS

6800-series MPU Interface & Write Instruction

Table 13. AC Characteristics (6800-series Write Instruction)

Condition	Characteristic	Symbol	Min.	Typ.	Max.	Unit
V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C	E cycle time	t_C	650		-	ns
	Pulse rise / fall time	t_R, t_F	-	-	25	
	E pulse width high	t_{WH}	450	-	-	
	E pulse width low	t_{WL}	150	-	-	
	RS and CSB setup time	t_{SU1}	60	-	-	
	RS and CSB hold time	t_{H1}	30	-	-	
	DB setup time	t_{SU2}	100	-	-	
	DB hold time	t_{H2}	50	-	-	
V_{DD} = 3.6V to 5.5V, Ta = -30 to +85 °C	E cycle time	t_C	350		-	ns
	Pulse rise / fall time	t_R, t_F	-	-	25	
	E pulse width high	t_{WH}	250	-	-	
	E pulse width low	t_{WL}	100	-	-	
	RS and CSB setup time	t_{SU1}	40	-	-	
	RS and CSB hold time	t_{H1}	10	-	-	
	DB setup time	t_{SU2}	40	-	-	
	DB hold time	t_{H2}	10	-	-	

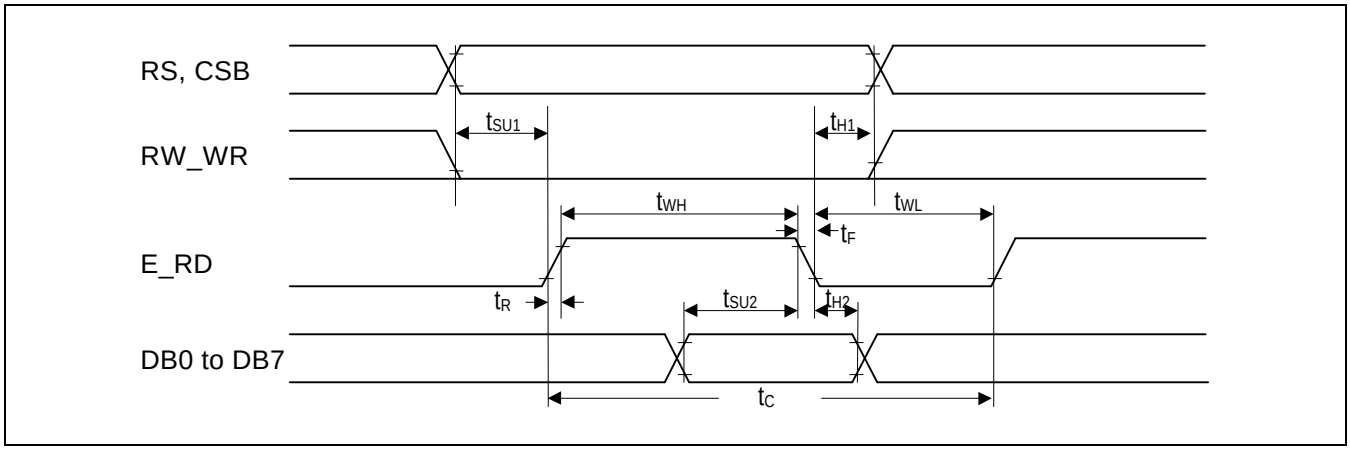


Figure 18. Write Bus Mode Timing (6800-series MPU Interface)

8080-series MPU Interface & Write Instruction

Table 14. AC Characteristics (8080-series Write Instruction)

Condition	Characteristic	Symbol	Min.	Typ.	Max.	Unit
V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C	WR cycle time	t_C	650		-	ns
	Pulse rise / fall time	t_R, t_F	-	-	25	
	WR pulse width high	t_{WH}	150	-	-	
	WR pulse width low	t_{WL}	450	-	-	
	RS and CSB setup time	t_{SU1}	60	-	-	
	RS and CSB hold time	t_{H1}	30	-	-	
	DB setup time	t_{SU2}	100	-	-	
	DB hold time	t_{H2}	50	-	-	
V_{DD} = 3.6V to 5.5V, Ta = -30 to +85 °C	WR cycle time	t_C	350		-	ns
	Pulse rise / fall time	t_R, t_F	-	-	25	
	WR pulse width high	t_{WH}	100	-	-	
	WR pulse width low	t_{WL}	250	-	-	
	RS and CSB setup time	t_{SU1}	40	-	-	
	RS and CSB hold time	t_{H1}	10	-	-	
	DB setup time	t_{SU2}	40	-	-	
	DB hold time	t_{H2}	10	-	-	

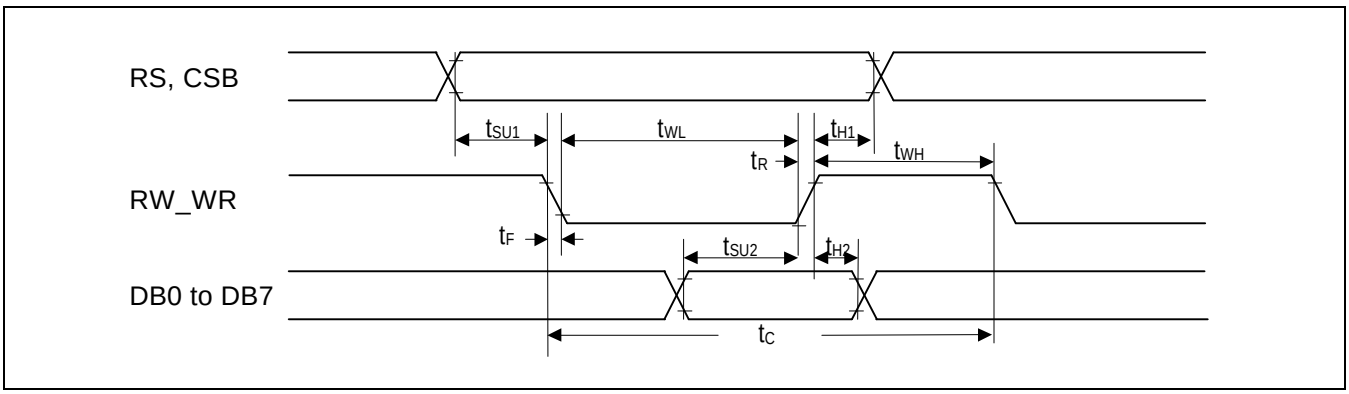


Figure 19. Write Bus Mode Timing (8080-series MPU Interface)

6800-series MPU Interface & Read Instruction

Table 15. AC Characteristics (6800-series Read Instruction)

Condition	Characteristic	Symbol	Min.	Typ.	Max.	Unit
V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C	E cycle time	t_C	650		-	ns
	Pulse rise / fall time	t_R,t_F	-	-	25	
	E pulse width high	t_{WH}	450	-	-	
	E pulse width low	t_{WL}	150	-	-	
	RS and CSB setup time	t_{SU}	60	-	-	
	RS and CSB hold time	t_H	30	-	-	
	DB output delay time	t_D	-	-	360	
	DB output hold time	t_{DH}	20	-	-	
V_{DD} = 3.6V to 5.5V, Ta = -30 to +85 °C	E cycle time	t_C	350		-	ns
	Pulse rise / fall time	t_R,t_F	-	-	25	
	E pulse width high	t_{WH}	250	-	-	
	E pulse width low	t_{WL}	100	-	-	
	RS and CSB setup time	t_{SU}	40	-	-	
	RS and CSB hold time	t_H	10	-	-	
	DB output delay time	t_D	-	-	120	
	DB output hold time	t_{DH}	10	-	-	

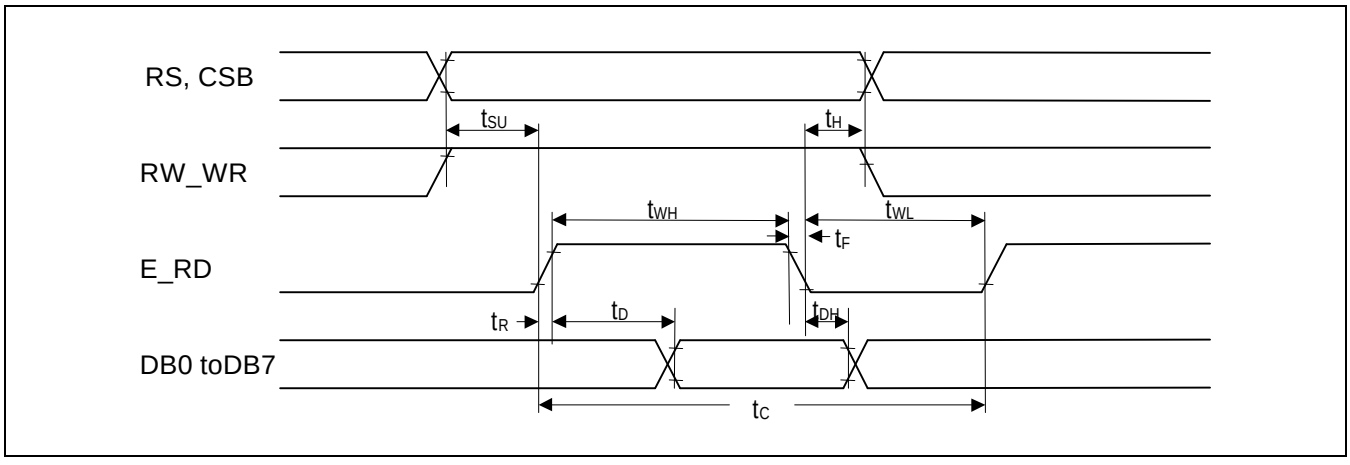


Figure 20. Read Bus Mode Timing (6800-series MPU Interface)

8080-series MPU Interface & Read Instruction

Table 16. AC Characteristics (8080-series Read Instruction)

Condition	Characteristic	Symbol	Min.	Typ.	Max.	Unit
V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C	RD cycle time	t_C	650		-	ns
	Pulse rise / fall time	t_R,t_F	-	-	25	
	RD pulse width high	t_{WH}	150	-	-	
	RD pulse width low	t_{WL}	450	-	-	
	RS and CSB setup time	t_{SU}	60	-	-	
	RS and CSB hold time	t_H	30	-	-	
	DB output delay time	t_D		-	360	
	DB output hold time	t_{DH}	20	-	-	
V_{DD} = 3.6V to 5.5V, Ta = -30 to +85 °C	RD cycle time	t_C	350		-	ns
	Pulse rise / fall time	t_R,t_F	-	-	25	
	RD pulse width high	t_{WH}	100	-	-	
	RD pulse width low	t_{WL}	250	-	-	
	RS and CSB setup time	t_{SU}	40	-	-	
	RS and CSB hold time	t_H	10	-	-	
	DB output delay time	t_D	-	-	120	
	DB output hold time	t_{DH}	10	-	-	

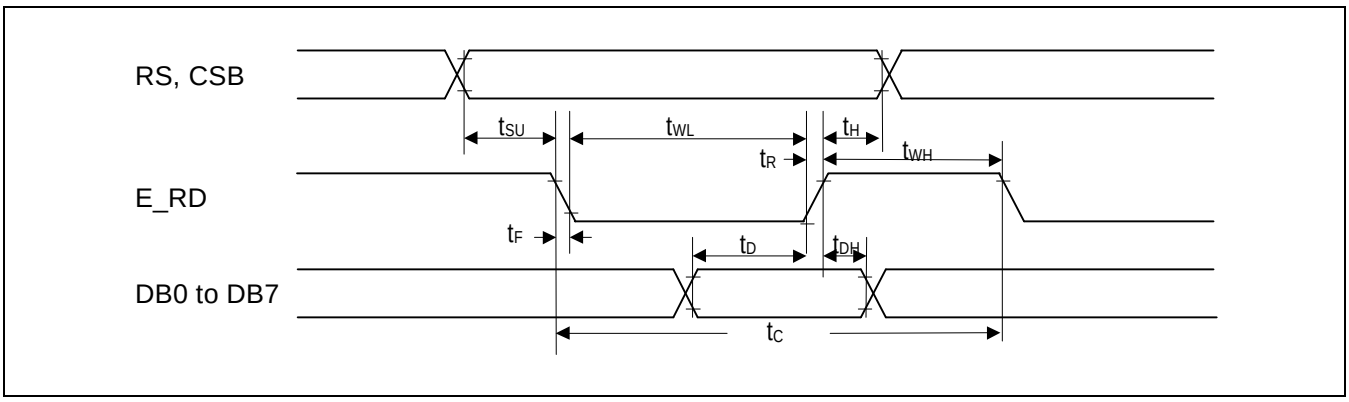


Figure 21. Read Bus Mode Timing (8080-series MPU Interface)