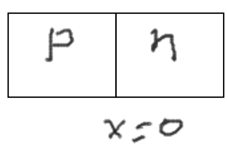
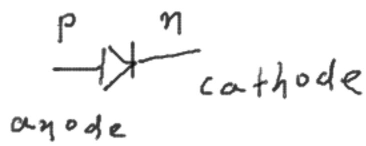
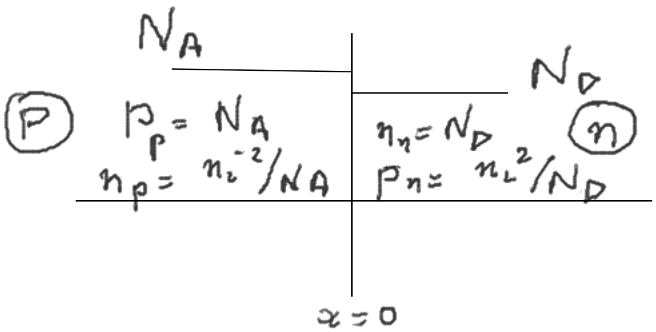
pn Junction Diode

It is formed by bringing a p-type semiconductor in contact with an n-type semiconductor.





x=0 interface called metallurgical junction



p-type side: $p_p = N_A = 10^{17}$ holes/cm^3

$n_p = 10^3$ electrons/cm^3

n-type material:

$n_n = N_D = 10^{16}$ electrons/cm^3

$p_n = 10^4$ holes/cm^3

Now we have to explain the pn junction electrostatics, which contributes to the pn junction formation.

Two mechanisms take place:

a) Diffusion currents → from high to low carrier concentration areas

b) Drift Currents → due to space-charge electric field

Both mechanisms are needed to explain pn junction formation.

Now, lets think about the physics:

Brinking 2 pieces together a p-type material with an n-type material.

We anticipate a diffusion of the holes from the p-type medium to n-type, and a diffusion of electrons from n-type material to p-type material.

If diffusion continues for a while the p-n junction will cease to exist.

However, this is not the case.

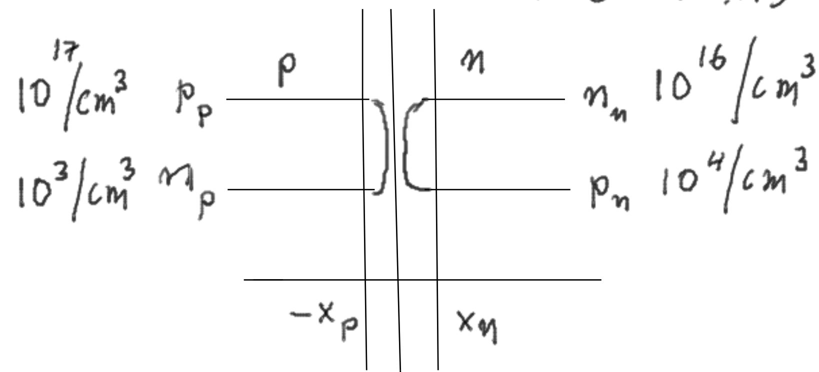
There is a second process that take place, the space charge region, which exhibits a local space-charge electric field.

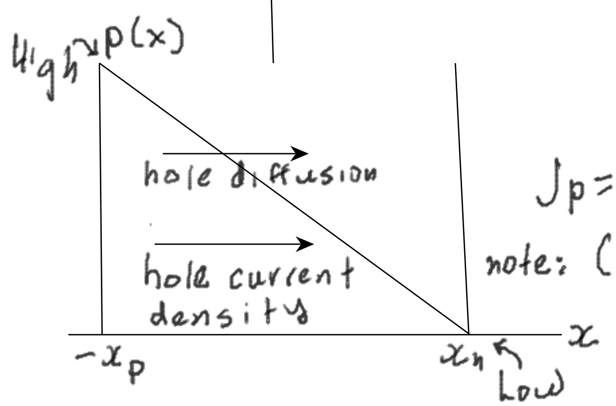
This field, generates drift currents, so that compensates the diffusion currents, therefore, the pn junction formation take place.

At this point, lets explain the two processess:

(a) Diffusion

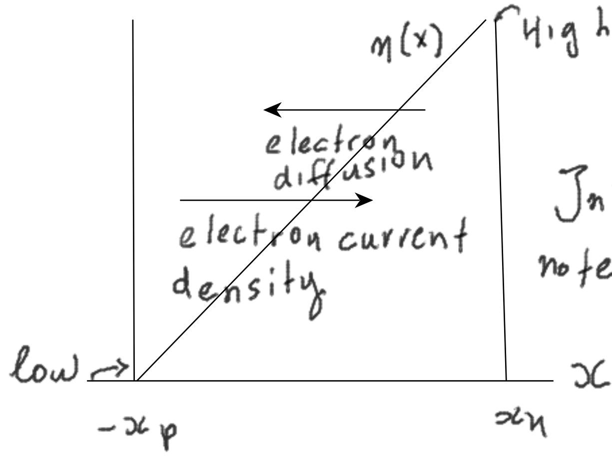
(a) Diffusion Currents





$$J_p = -q D_p \frac{dp}{dx}$$

note: $\left(\frac{dp}{dx}\right) < 0$



$$J_n = q D_n \frac{dn}{dx}$$

note: $\left(\frac{dn}{dx}\right) > 0$

Diffusion of charges leaves:

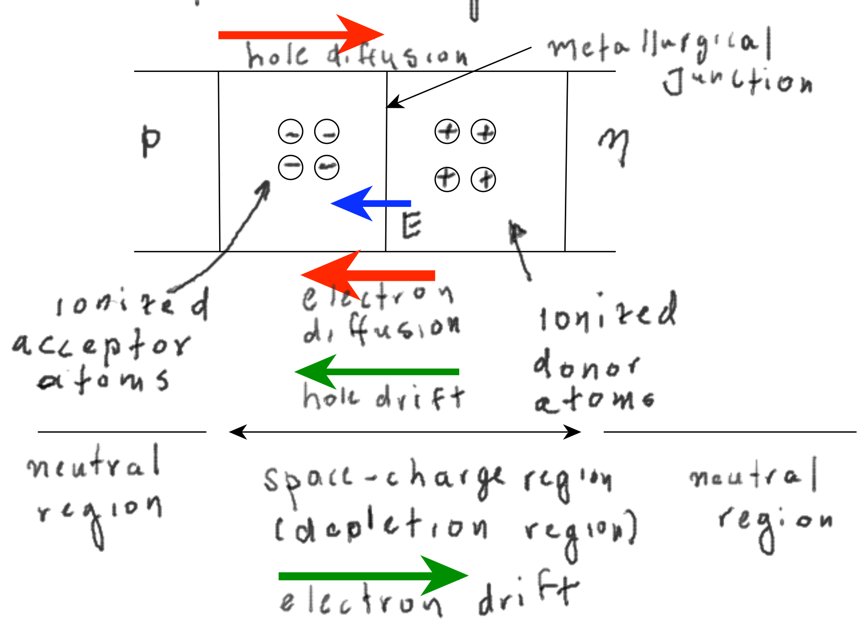
- immobilized negative acceptors on p-type material
- immobilized positive donors on n-type material

⇒ a space-charge region or depletion zone is formed. ⇨

(b) Space-Charge Region - Drift Currents

This is very important section. The concept of

- space-charge region (depletion zone)
- Junction potential φ_j
- depletion layer width.



A region of space-charge exhibits a local electric field

$$E(x) = \frac{1}{\varepsilon_s}\int \rho(x)\,dx \qquad (1)$$

ε_s = electric permittivity (F/cm) of the medium

& φ_j = junction potential

$$= -\int E(x)\,dx \qquad V \qquad (2)$$

(across the space-charge region) it expresses the difference between n - p regions

$$\& \quad \varphi_j = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right) \qquad (3)$$

$$\& \quad W_{do} = (x_n + x_p) = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\varphi_j} \qquad (4)$$

W_{do} = depletion layer width

Example

Calculate the junction potential φ_j & depletion zone width w_{do}

for the silicon diode given.

$N_A = 10^{17} cm^3$ on the p-side

$N_D = 10^{20} cm^3$ on the n-side

Solution

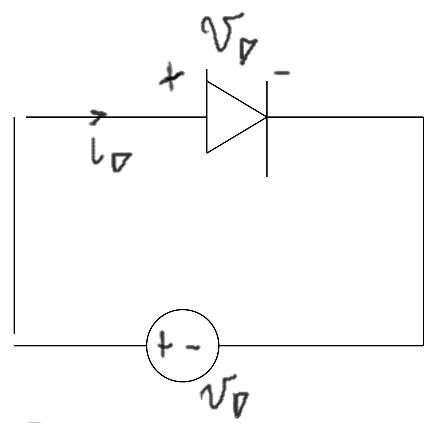
$$\varphi_i = V_T \, e_n \left(\frac{N_A N_D}{n_i^2} \right)$$

$$= (0.025\ V) \, e_n \left[\frac{(10^{17}/cm^3)(10^{20}/cm^3)}{\underbrace{10^{20}/cm^6}_{n_i^2}} \right] = 0.979\ V$$

$$w_{do} = \sqrt{\frac{2\varepsilon_s}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) \varphi_j} = 0.113\ \mu m$$

$\varepsilon_s = 11.7\,\varepsilon_0$, $\varepsilon_0 = 8.85 \times 10^{-14}\ F/cm$

how can we model the I-V characteristics?



$$i_D = I_S\left[\exp\left(\frac{q v_D}{nkT}\right) - 1\right]$$

$$= I_S\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right]$$

$$n_i^2 = BT^3 \exp\left(-\frac{E_G}{kT}\right) \quad [cm^{-6}]$$

Eq. 2.1

I_S = reverse saturation current [A]
$\propto n_i^2$, strongly temperature dependent (see Eq. 2.1)

v_D = voltage applied to diode [V]

q = electric charge (1.6×10^{-19} C)

k = Boltzmann's constant (1.38×10^{-23} J/K)

T = absolute temperature [K]

n = nonideality factor

V_T = kT/q = thermal voltage [V]
= 0.025 V (found earlier), at room temperature.

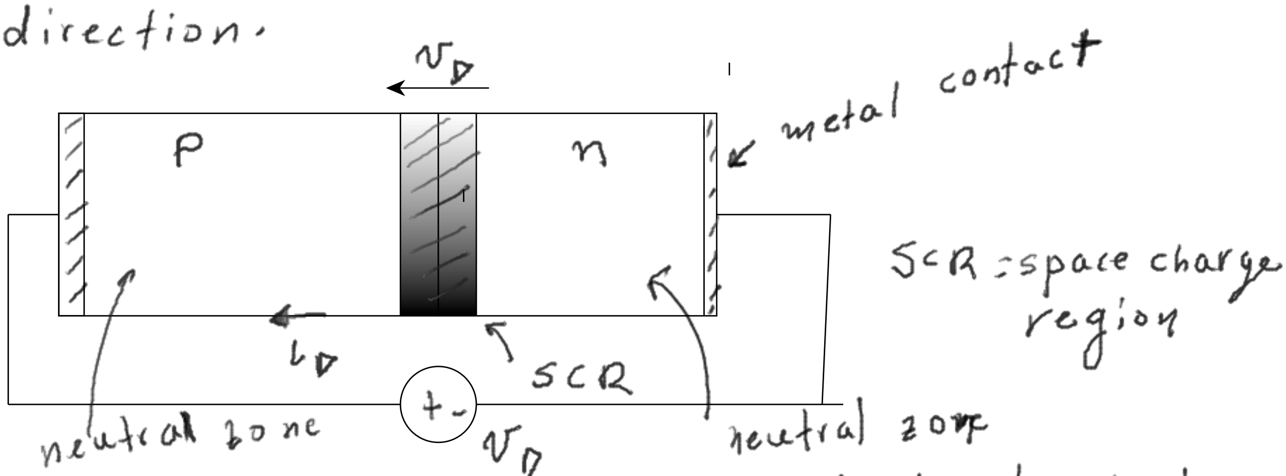
$10^{-18}\,A \leq I_S \leq 10^{-9}\,A$

n = nonideality factor.

typically $1 \leq n \leq 1.1$
(assume in our treatment, $n = 1$)

I-V Characteristics of a Diode

Diode allows current to flow in one direction, prevents current in the opposite direction.

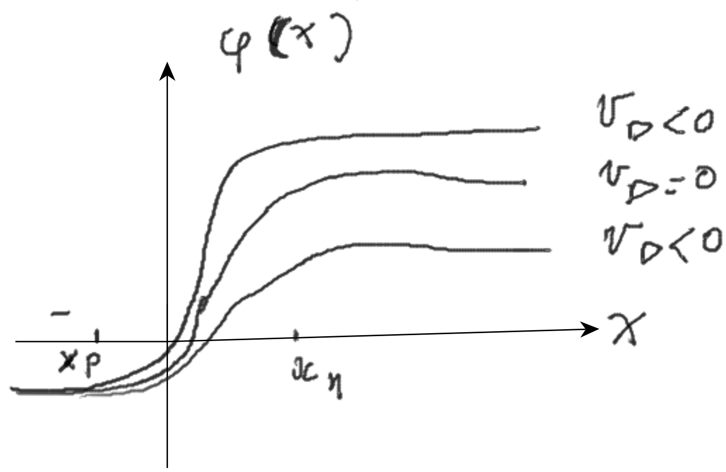


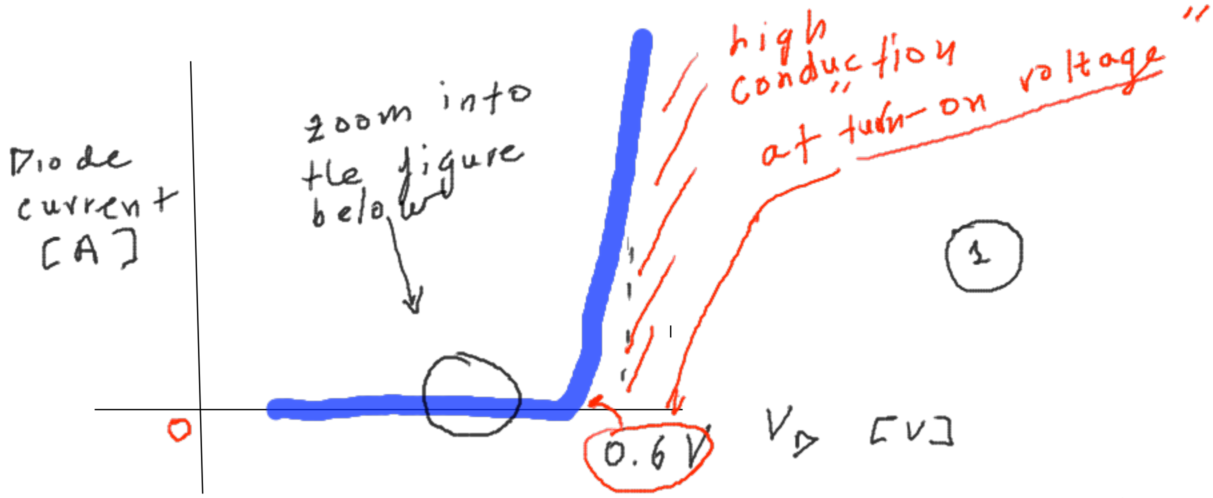
v_D = voltage applied to diode terminal.

i_D = current through the diode

$v_D > 0$ reduces potential barrier to e^-, e^+

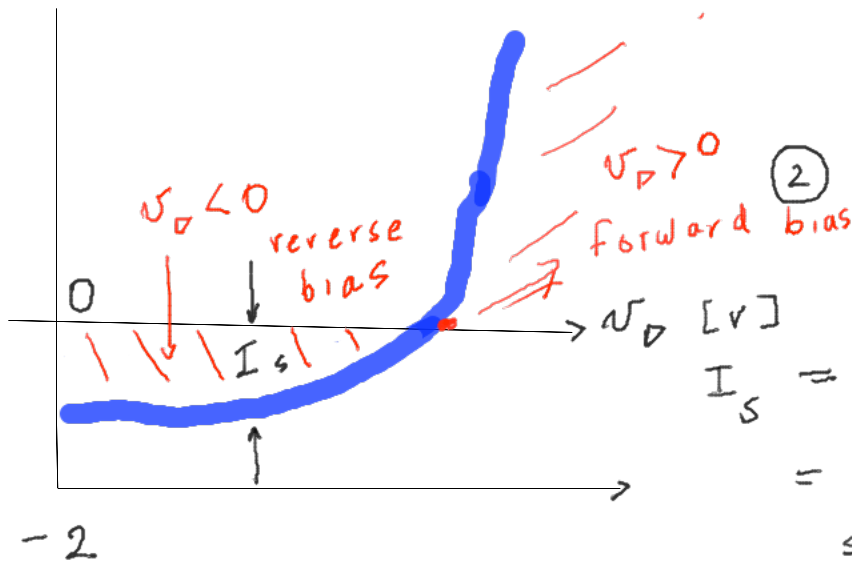
$v_D < 0$ increases potentia barrier to e^-, e^+





diode current increases rapidly between *0.5–0.7V V_D (applied diode voltage)

*(voltage across the diode, almost independent of current).



$I_S \approx 10^{-15}$

= reverse saturation

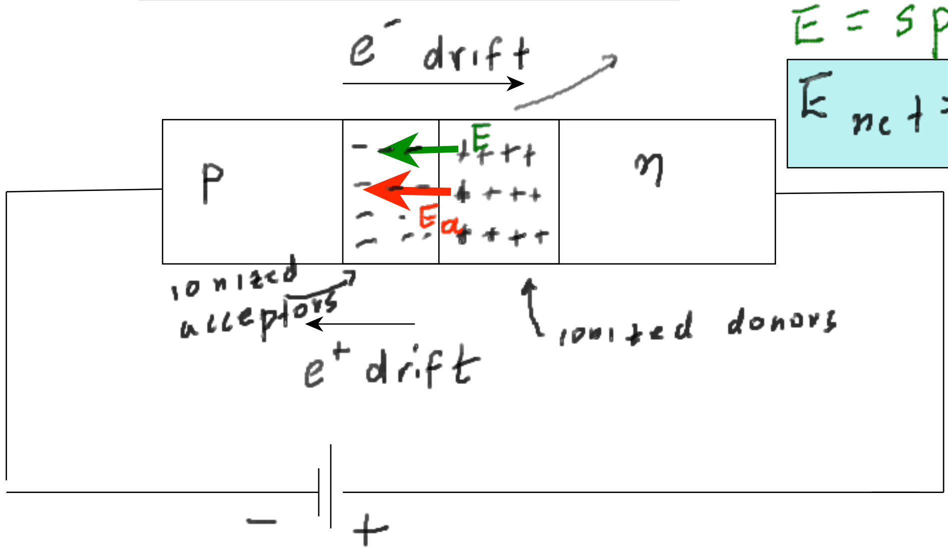
or

saturation current

Reverse Bias

E_a = applied electric field
E = space-charge field

$$\boxed{E_{net} = E + E_s}$$



e^+ are held back in the p-region
e^- −ll− −ll− −ll− n-region

$\Rightarrow$ NO CURRENT ACROSS THE PN JUNCTION
(depletion zone increases)
or
space-charge width

In this case, a capacitance associated with pn junction under reverse bias conditions exist.

$$i_D = I_S \left[\exp\left(\frac{v_D}{V_T}\right) - 1 \right]$$

$$= I_S \left[\exp(-4) - 1 \right] \simeq$$

negligible

$$\simeq -I_S$$

where $v_D = -0.1\,V$ (just an assumption)
$V_T = 0.025\ V$ (found earlier)
& $\exp(-4) = 0.018$

Lets summarize the reverse bias condition:

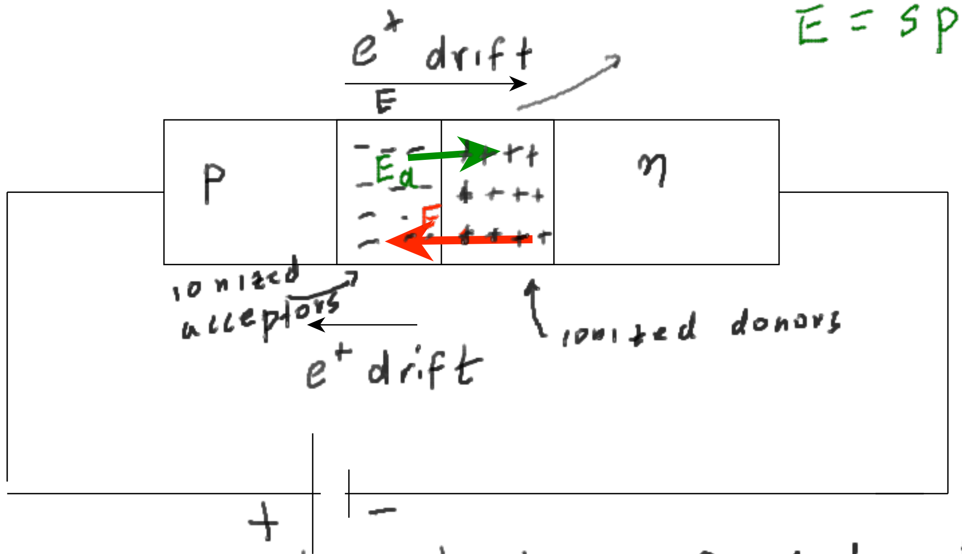
It occurs because:

the <u>thermal</u> breakdown of the covalent bonds generates a leakage current directly proportional to the temperature of the pn junction

(Thermal generation of e^+-e^- pairs in the depletion zone that surrounds the pn junction).

FORWARD BIAS

E_a = applied electric field
E = space-charge field



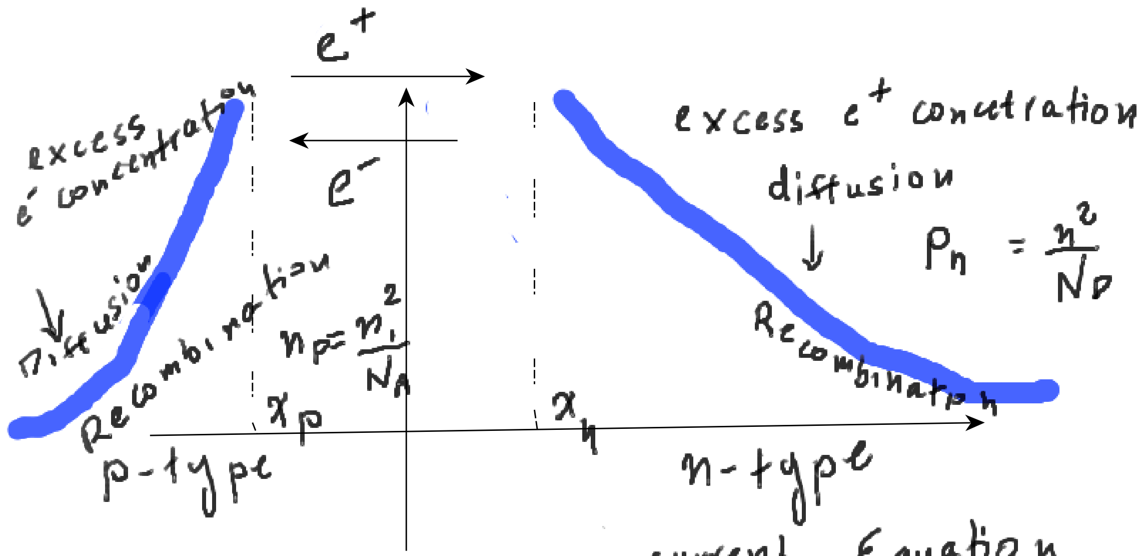
The net electric field E_{net} is lower than the thermal equilibrium value ⇒ $\boxed{E_{net} = E_a - E}$

- majority carriers (e^+) moves from p-region to n-region
- majority carriers (e^-) moves the n-region to p-region

⇒ current across pn junction, I_D

As majority carriers cross in the opposite region they become minority carriers, causing carrier concentration to increase

⇒ DIFFUSION and then RECOMBINATION with the majority carriers



Forward Bias current Equation

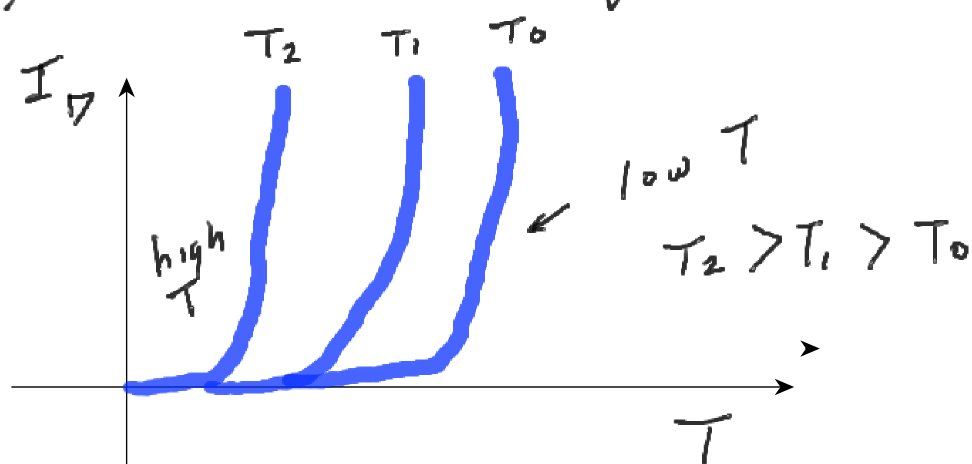
$$i_D = I_S \left[\exp\left(\frac{v_D}{KT} \right) \right]$$

for $v_D > 0$

TEMPERATURE EFFECTS

I_S, V_T are function of temperature

$\Rightarrow$



Diode characteristics vary with Temperature

In Germanium (Ge) reverse current increases with temperature $\Rightarrow$ Impractical for most circuit applications

DIODE BREAKDOWN

Reverse Breakdown → avalanche breakdown
→ Zener Breakdown

$2V \leq V_z \leq 2000V$

V_z: voltage where breakdown occurs

Parameters affecting breakdown:

doping level on the lightest doped side of the pn junction.

Havier the doping, the smaller the breakdown

this can be seen from the depletion layer width under reverse bias conditions; where:

$w_d = (x_n + x_p) =$

junction potential → large internal $\vec{E}$ → charge to the depletion zone

$$\sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)\underbrace{(\varphi_j + V_R)}_{v_j = \text{net voltage}}}$$

reverse bias voltage

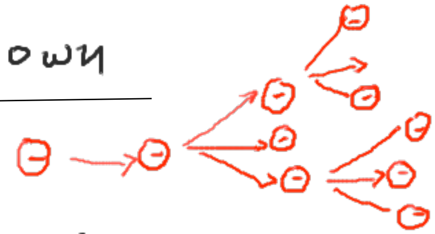
e^+, e^- generated thermaly in the depletion zone $\propto$ to the volume of the depletion region ⇒ larger the reverse bias voltage

large the depletion region ⇒ more charges

But if doping heavy ⇒ it reduces the w_D.

a. Avalanche Breakdown

$V_z > 5.6\ V$



width of depletion zone increases
$\Rightarrow$ electric field increases.

Free carries are accelerated under the influence of the electric field, in the depletion zone
$\Rightarrow$ collision with fixed atoms.

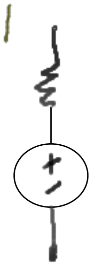
As electric field increases, they break covalent bonds generating $e^- - e^+$ pairs (impact - ionization process)

b. Zener Breakdown, $V_z < 5.6\ V$

It occurs on heavily doped diodes

heavily doping $\rightarrow$ narrow depletion zone.
$\Rightarrow$ reverse bias $\longrightarrow$ Carier TUNNELING between conduction & valence band

model



symbol

Zener Diode

Reverse Breakdown of a diode (modeling)

PN Junction Capacitance.

Both forward & reverse-biased diodes have capacitance associated with pn Junction.

Reverse Bias

$v_d < 0 \Rightarrow w_D$ increases $\Rightarrow$ charge in w_d space charge on the n-side increases

strong dependence from dopants

$$Q_n = q\left(\frac{N_A N_D}{N_A + N_D}\right) w_D A$$

$$C_j = \frac{dQ_n}{dv_R} = \frac{C_{jo} A}{\sqrt{1 + \frac{v_R}{\phi_J}}}$$

cross sectional area of the diode

space charge

applied field

junction potential

where $C_{jo} = \frac{\varepsilon_s}{w_{do}}$

dielectric constant

depletion layer-width (zero bias depletion width)

C_{jo} = zero bias Junction capacitance

If v_R increases $\Rightarrow C_j$ decreases

$\Rightarrow$ variable-controlled capacitance diode

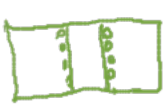
design of diodes with impurity profiles, "hyper-abrupt profiles"

Forward Bias / Diffusion Capacitance

diode operating under forward bias:

Q_D = amount of charge stored in the diode

$Q_D \propto i_D$



$$Q_D = i_D \tau_T \quad [C]$$

diode transit time

$10^{-15} < \tau_T < 10^{-6}$ or more

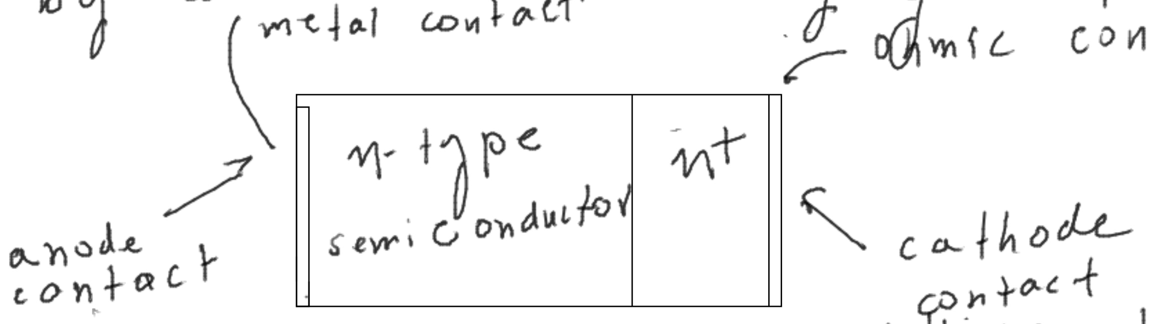
& $$C_D = \frac{dQ_D}{dv_D} = \frac{(i_D + I_S)\tau_T}{V_T} \cong \frac{i_D \tau_T}{V_T}$$

$C_D \propto i_D$

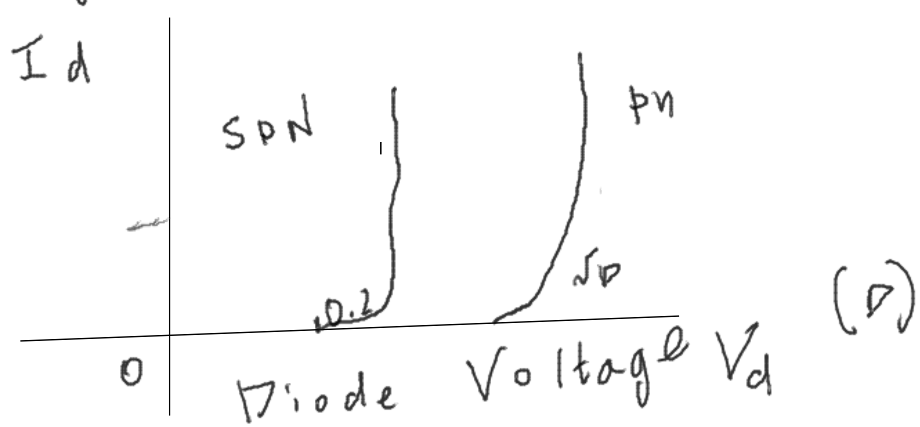
= Diffusion capacitance

SCHOTTKY BARIER DIODE

One of the semiconductor regions is replaced by a non-Ohmic rectifying metal contact.



- It operates on a lower voltage than the PN junction.
- Reduced internal charge Q_D under forwards bias.



Diode circuit Analysis

Goal of Studies:

- Analysis of Circuits containing diodes

Introduce simplified circuit model for the diode.

We'll study the following circuit applying the following techniques:

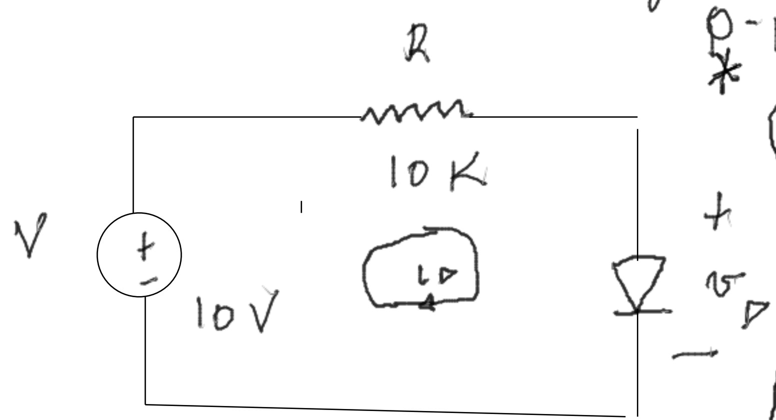
a) Graphical analysis using the LOAD LINE TECHNIQUE

b) Simplified Analysis using an IDEAL DIODE MODEL (PIECEWISE)

c) Simplified Analysis using the Constant Drop Model

4) Numerical Solution of Diode Equation

Q-point (i_D, v_D)
*



* Across the diode there is a small voltage drop, that must be overcomed by the external voltage source

Silicon, $v_D \simeq 0.6 - 0.7V$

Ge, Schottky $\simeq 0.2V$

LED ≈ 2.5V - 3V

$\downarrow$

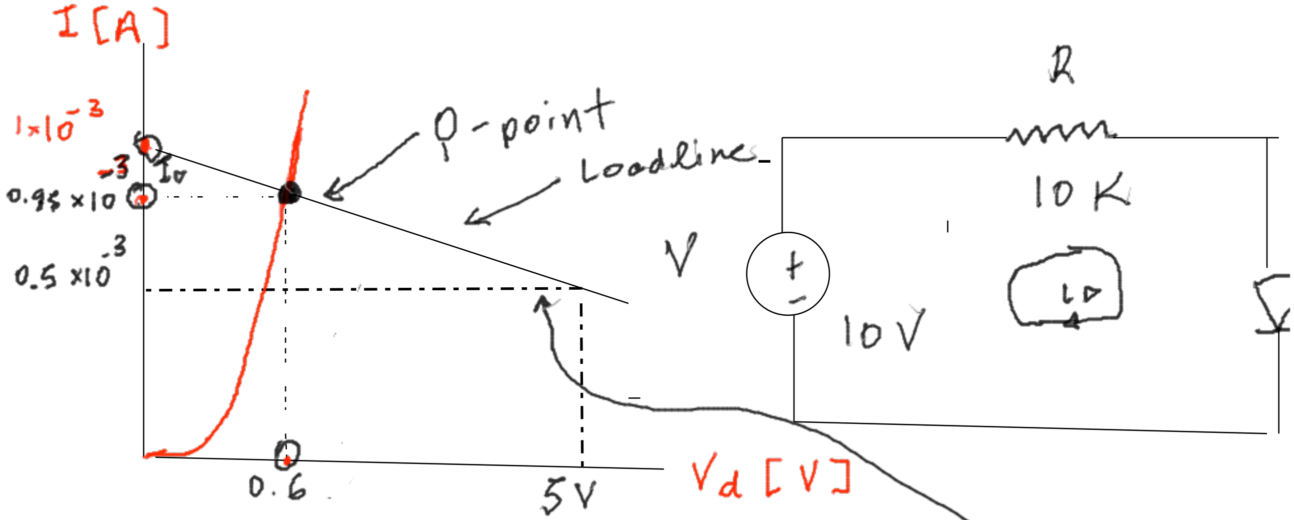
$v_D = v_{ON}$

Q-point or quiescent point, is the point that defines the operation of the diode in terms of I_D, v_D.

We start from: $V = I_D R + V_D$

(Q-point operation of the diode with stability)

a) Graphical analysis using the LOADLINE TECHNIQUE



$$V = I_D R + V_D \qquad (1)$$

$$10 = I_D 10^4 + V_D \qquad (2)$$

we need two points to define a line:

For $V_D = 0$

$$I_D = \frac{V}{R} = \frac{10V}{10K\Omega} = 1mA$$

For $I_D = 0$

$V_D = 10V \longrightarrow$ this point is not on the diode characteristic of the above diagram

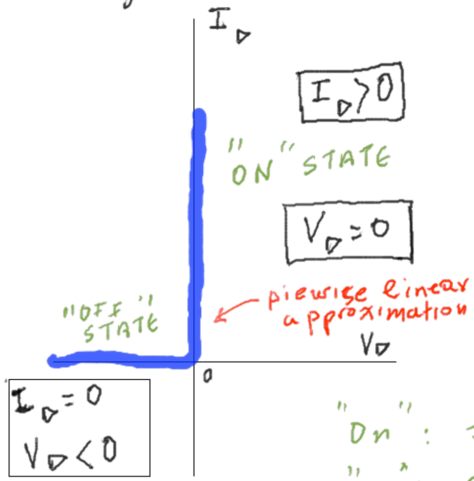
let's pick $V_D = 5V$, then

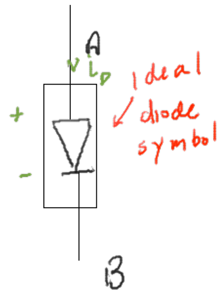
$$I_D = \frac{10V - 5V}{10^4\Omega} = 0.5mA$$

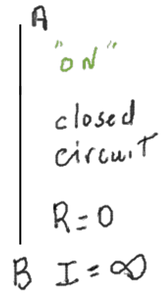
Q-point: intersection of loadline with diode characteristics

$= (0.95mA, 0.6)$

b) IDEAL DIODE





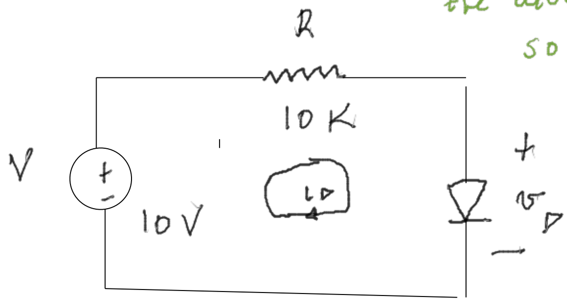


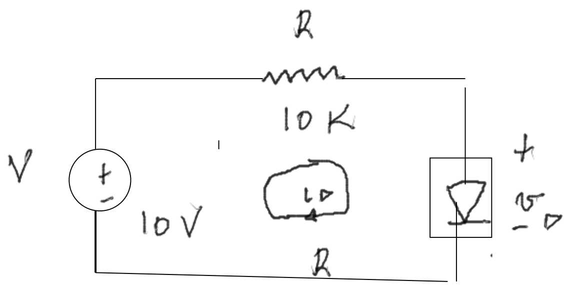
"On": forward bias, voltage across diode is zero

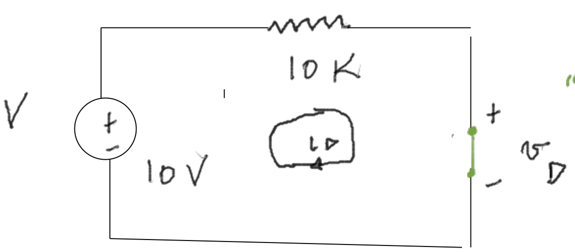
"Off": reverse bias, $v_D < 0$, current through the diode is zero

so: $v_D = 0$ for $i_D > 0$

$i_D = 0$ for $v_D \leq 0$







MODEL OF The Ideal Diode on the "ON" STATE

$$V = I_D R + V_D$$

$$10\ V = I_D \times 10^4\ \Omega + 0\ V$$

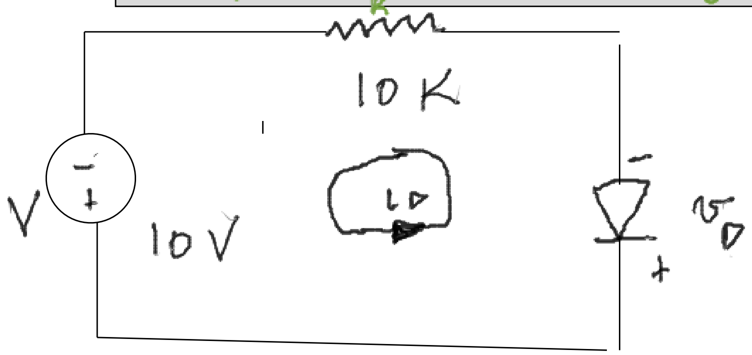
$$\Rightarrow I_D = \frac{(10-0)\ V}{10\ K\Omega} = 1\ mA \geq 0$$ forward bias (ON-STATE)

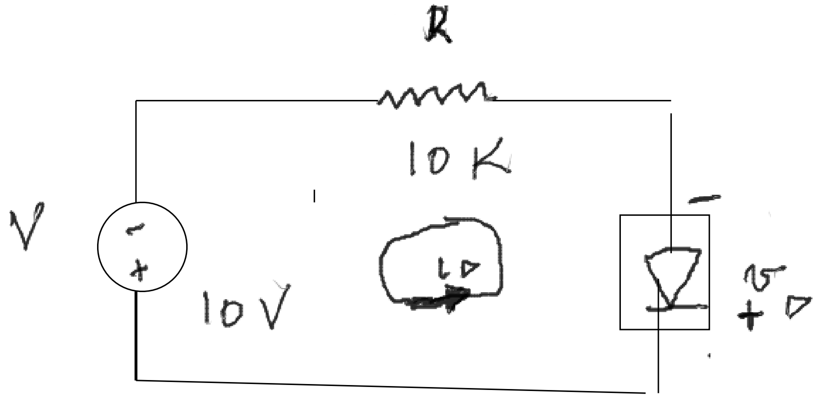
Q - point (1mA, 0 V)

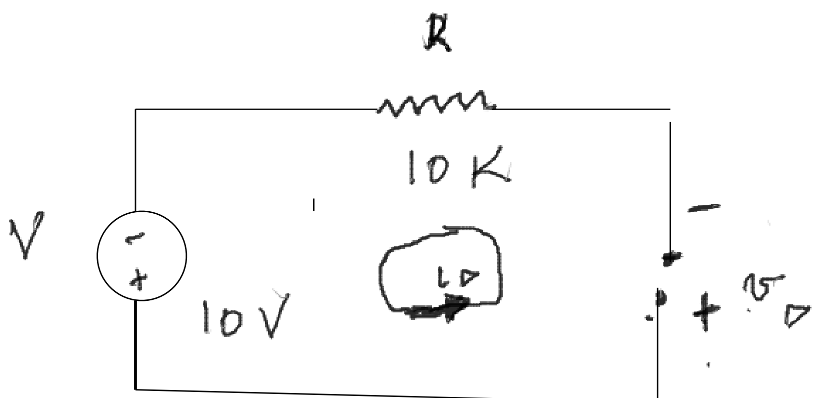
Now, next let's see the case of a reversed bias diode.

Analysis of an Ideal Diode operating under Reverse Bias

(off region)







Ideal diode replaced with its model for the off region

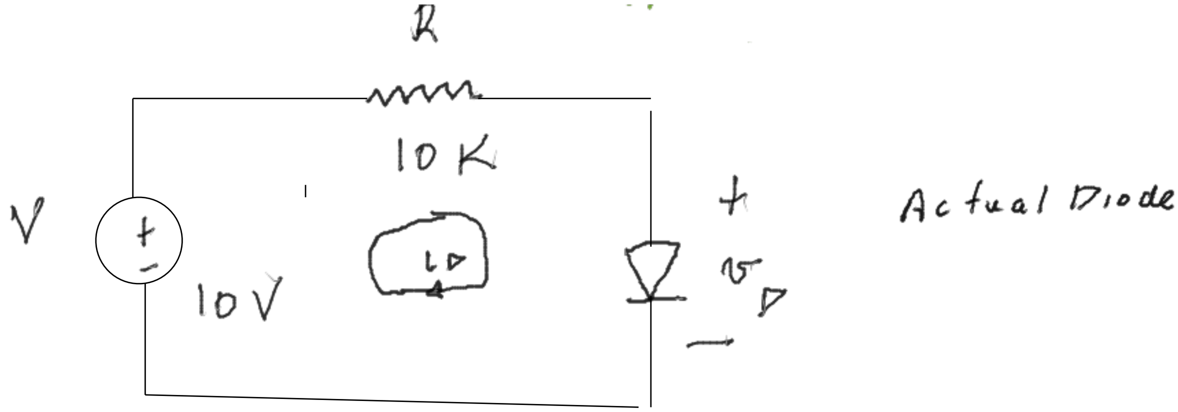
Start again from:

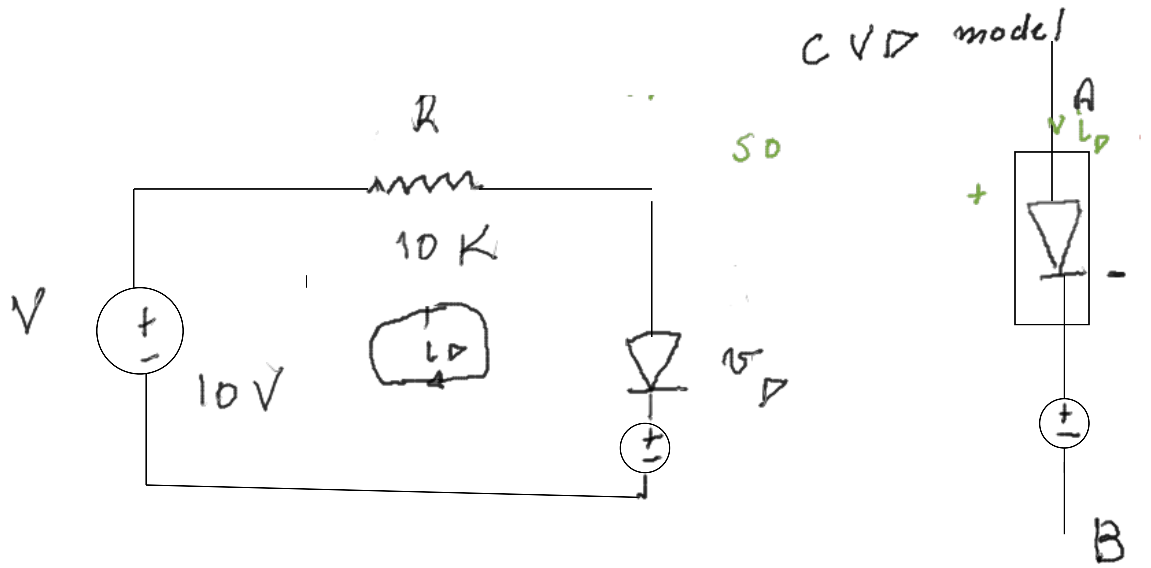
$V = I_D R + V_D$

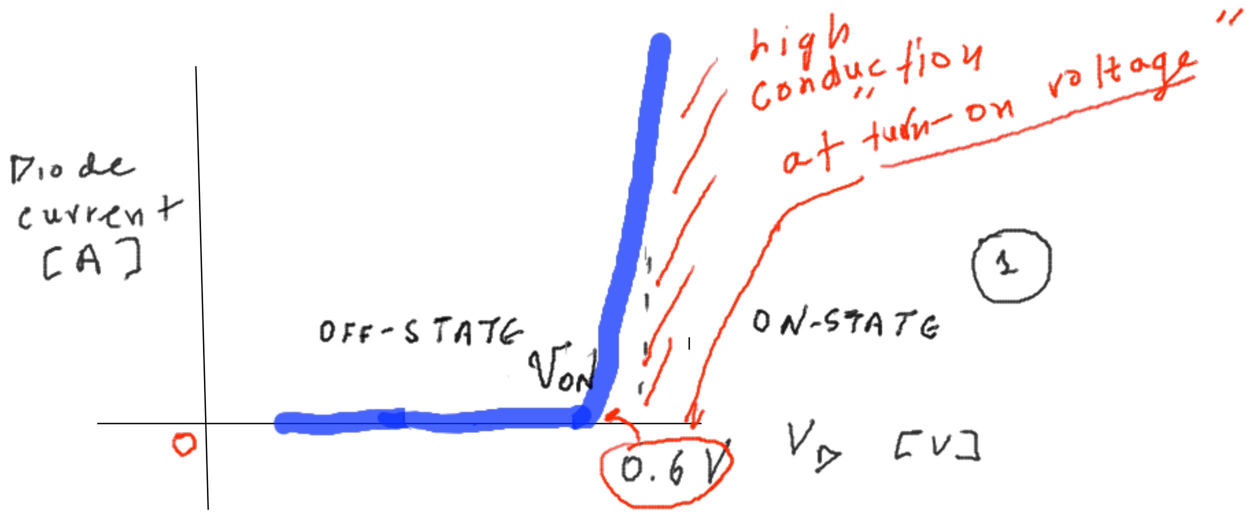
but $I_D = 0$ | $\Rightarrow$ reverse bias diode

$\Rightarrow V_D = -10\,V$ | Q-point $(0, -10\,V)$

3 Constant Voltage Drop Voltage (CVD) Voltage
(It includes 0.6 V, which is the "turn-on" Voltage







$v_D = V_{ON}$ for $i_D > 0$
$i_D = 0$ for $v_D \le V_{ON}$

$$v_D = i_D R + V_{ON}$$

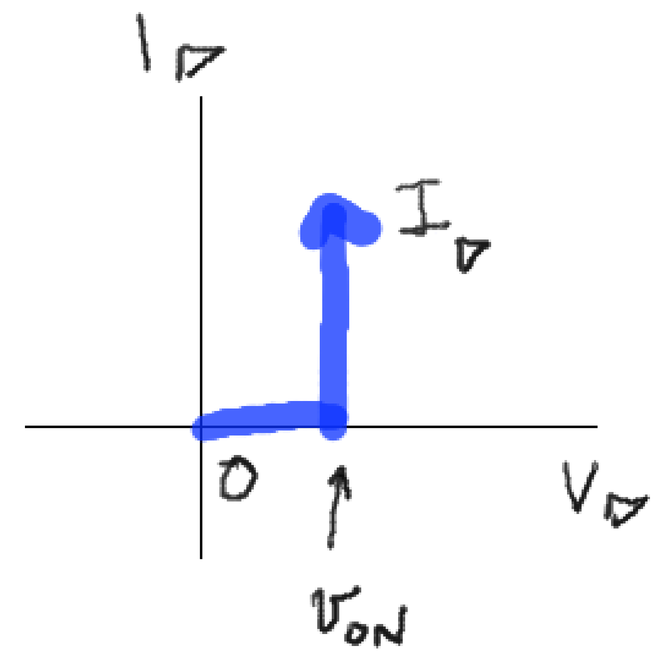
$$V_{ON} = 0.6V$$

$$i_D R = v_D - v_{ON}$$

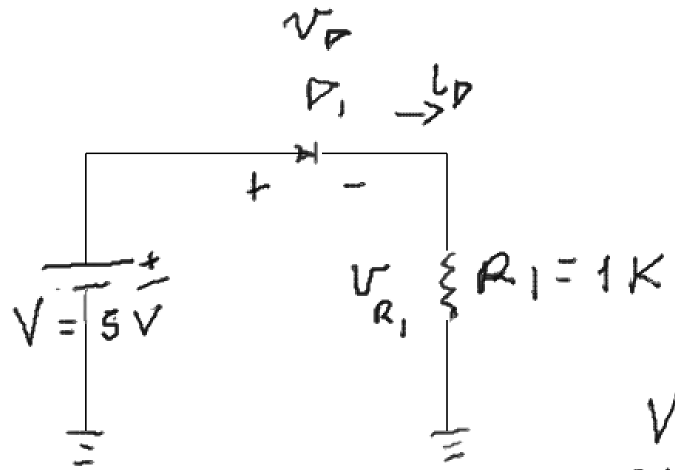
$$i_D = \frac{v_D - v_{ON}}{R}$$

$$= \frac{10V - 0.6V}{10K\Omega}$$

$$= 0.940\,mA$$



Example 1



$V = 5V$

$R_1 = 1K$

$V_D = 0.7V$

$$V = \underset{\overset{\shortparallel}{0}}{V_D} + \overbrace{i_D R_1}^{V_{R_1}}$$

Ideal Diode

$$i_D = \frac{5V - 0}{1K} = 5mA \quad \text{(ideal diode)}$$

CVD Diode (Practical Case)

$$i_D = \frac{V - 0.7V}{R_1}$$

$$= \frac{5V - 0.7V}{1K} = 4.3\ mA \quad \text{(CVD diode)}$$

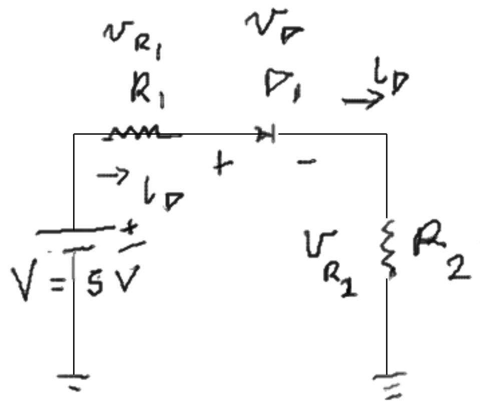
Percentage Error

$$\%\ \text{error} = \frac{|4.3mA - 5mA|}{4.3\ mA} \times 100$$

$$= 16.28\%$$

Example 2

We apply the CVD method



$V = 5V$
$R_1 = 1.2K$
$R_2 = 2.1K$
$v_D = 0.7V$

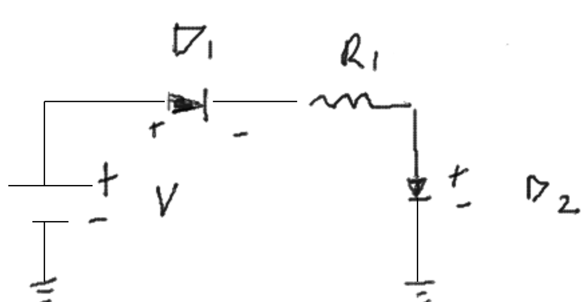
$$V = \underbrace{i_D R_1}_{v_{R_1}} + v_D + \underbrace{i_D R_2}_{v_{R_2}}$$

$$\Rightarrow V - v_D = i_D (R_1 + R_2)$$

$$I_D = \frac{V - v_D}{R_1 + R_2}$$

$$= \frac{5V - 0.7V}{3.3K} = 1.3mA$$

Example 3



$V = 4V$
$R_1 = 5.1V$

$v_{D_1} = v_{D_2} = 0.7V$

$$V = V_{D_1} + \underbrace{i_D R_1}_{V_{R_1}} + v_{D_2}$$

$$i_D R_1 = v_{R_1} = V - v_{D1} - v_{D_2}$$
$$= 4V - (0.7V + 0.7V)$$
$$= 4V - 1.4V = 2.6V \Rightarrow i_D = \frac{v_{R_1}}{R_1} = 5098\ \mu A$$

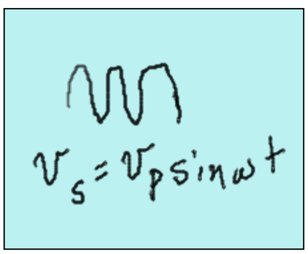
Half-Wave Rectifier Circuits

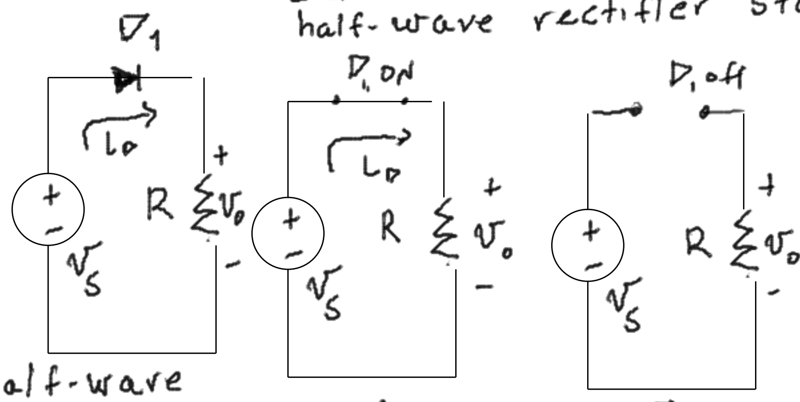
It converts an ac voltage to a pulsating DC voltage

By adding a filter*, the ac components are eliminated. As a result a dc constant voltage, results.

(* typical a capacitor)

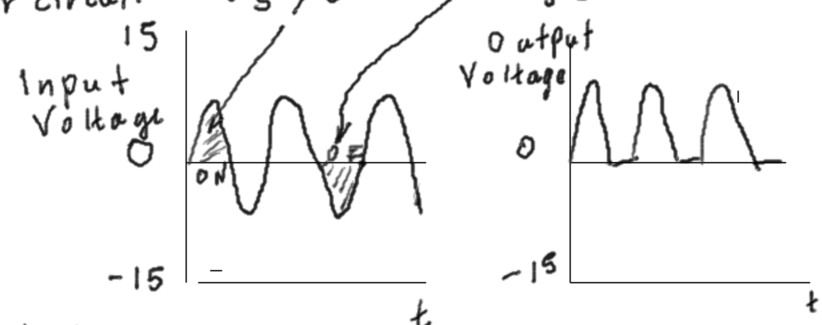
Ideal Diode Model for two half-wave rectifier states





Half-wave rectifier circuit

$v_s > 0$ $\quad$ $v_s < 0$



ON-state $V_o = V_s$ $\quad$ OFF-state $V_o = 0$ $\Big\}$ Circuit 50% conductive

$\Downarrow$

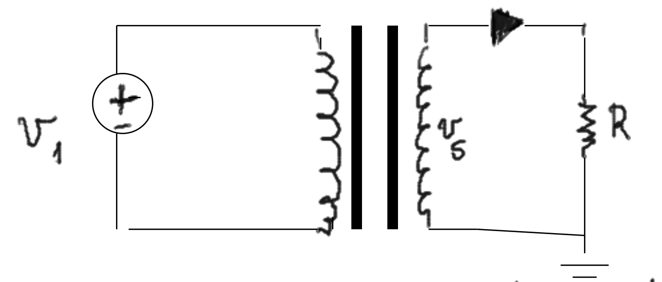
Pulsating DC current

Using the CVD model:

$$V_{out} = (V_p \sin\omega t) - V_{on}$$

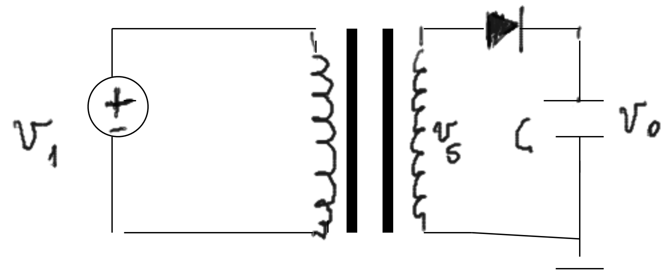
V_{on} = 0.7 V for Si

In order to convert from 120 V-ac, 60 Hz to desired ac voltage level, the following circuit can be used as step the voltage up or down.

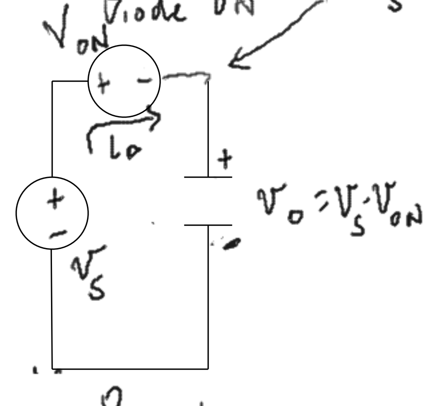


$v_S = V_p \sin \omega t$

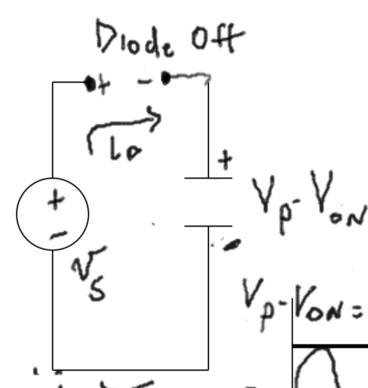
The same ciruit with a filter capacitor to remove time-varying components from the signal



$v_S = V_p \sin \omega t$

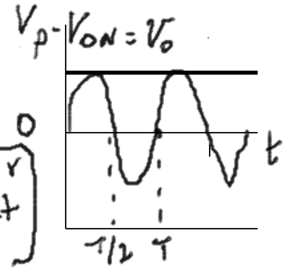


$0 \le t \le T/2$

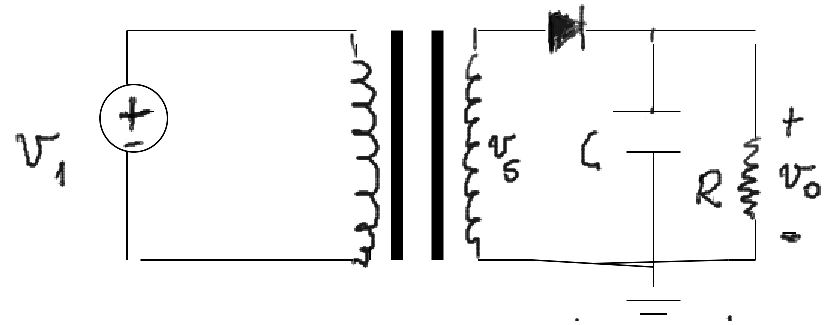


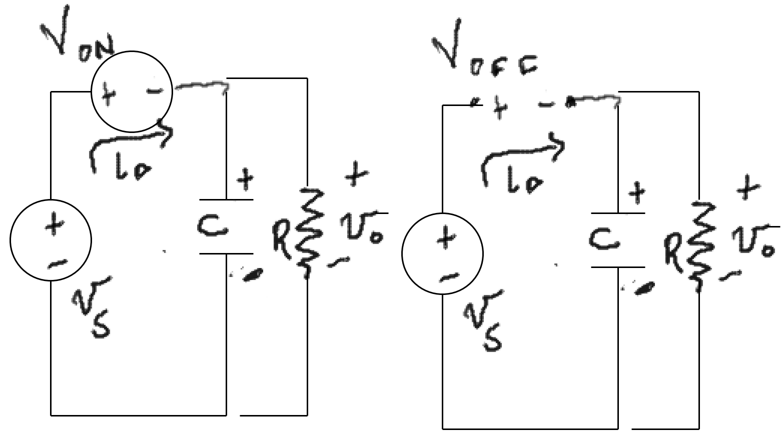
$t > T/2$

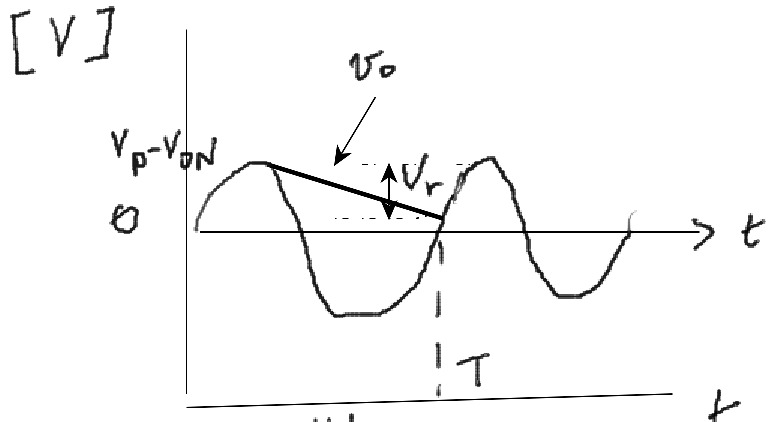
the capacitor is charged but disconnected



However, if we connected a load to the circuit, the capacitor can be discharged. This can be achieved using the half-wave rectifier with RC load.







discharge until,

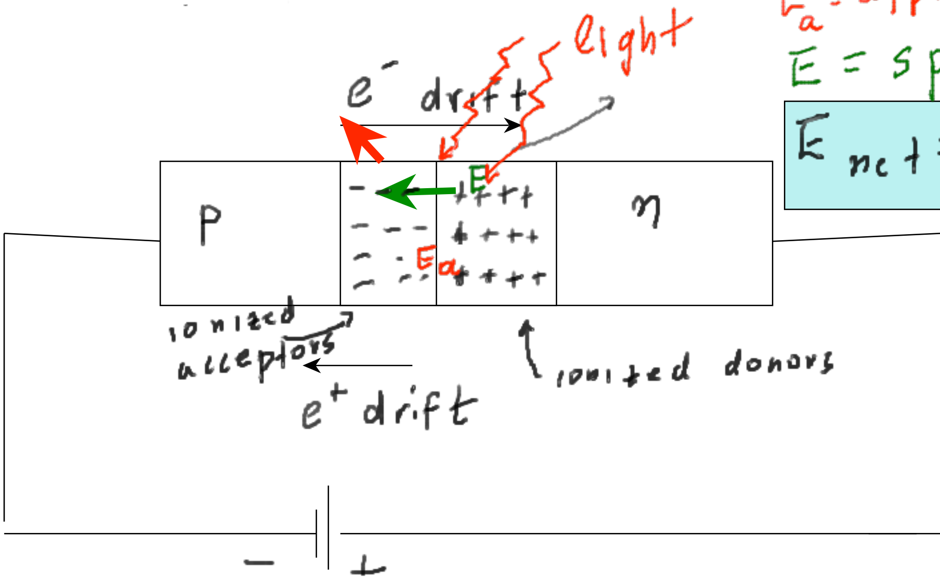
input voltage $> v_o$

=> process repeated once every cycle

Photodiodes

E_a = applied electric field
E = space-charge field

$\boxed{E_{net} = E + E_s}$



Illumination of the depletion zone by light leads to electrons, which acquire energy & jump the semiconductor band gap.

The quantum efficiency (QE) is the term that quantifies the interaction of light with the e^- on the depletion region is $\propto$ to the depletion region width

$\Rightarrow$ reverse bias diode operation

The energy of the incident photon must be $> E_G$

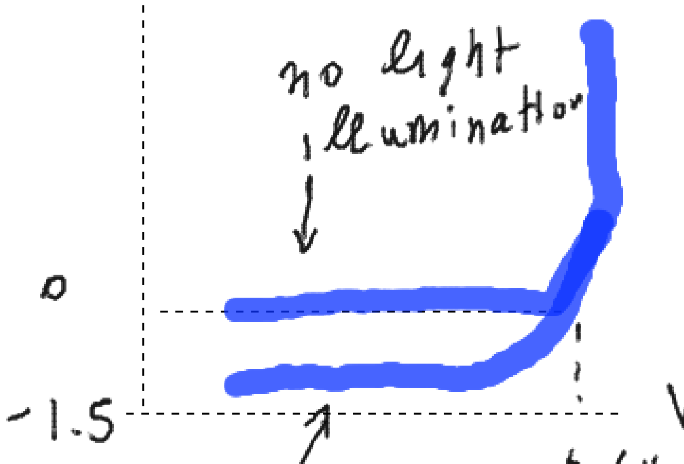
$$E_{photon} = h\nu = \frac{hc}{\lambda} \geq E_G$$

where E = Planks' constant (6.6×10^{-34} J·s)

ν = frequency of incident light

λ = wavelength of light

c = velocity of light $\approx 3 \times 10^8$ m/s



light illumination introduces a photocurrent.

$$v_o = i_{PH} R$$

i_{ph} = photo current