Lecture : 14-16 Applications for Carbon Nanotubes: Transistors

Lecture subset- Handouts

Potential Applications for Carbon Nanotubes

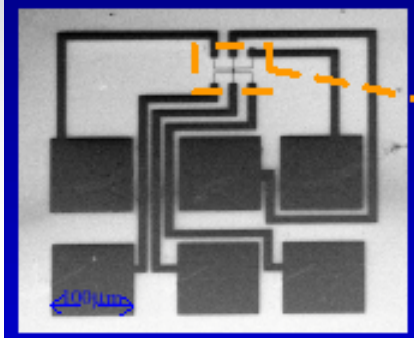
- Interconnect
- Field emission
- STM/AFM tip
- Memory
- Sensors
- Transistor

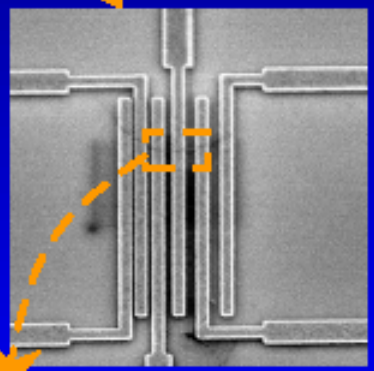
Nanotube Technology ?

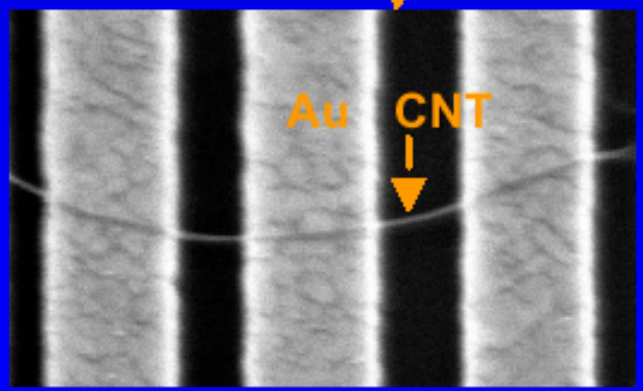
Plenty of room for improvement !

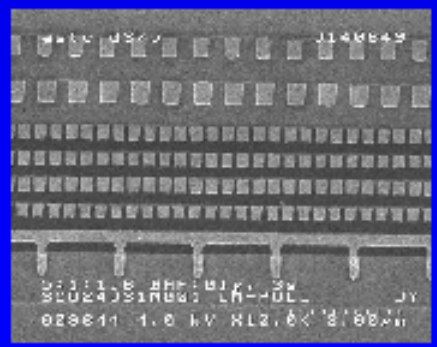
No new architecture !

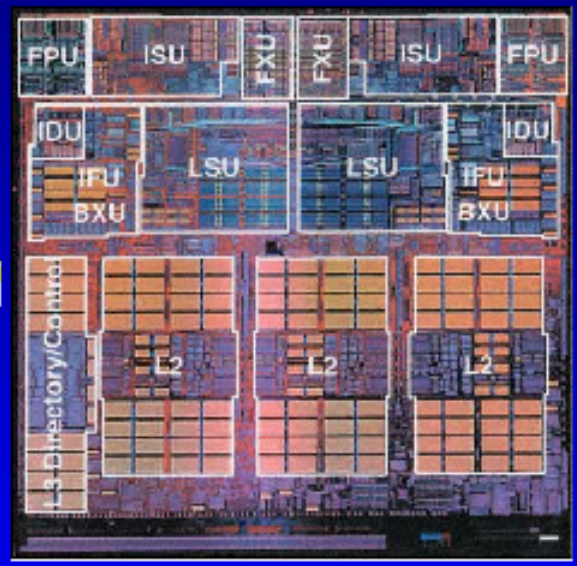
How do you get from here to there?

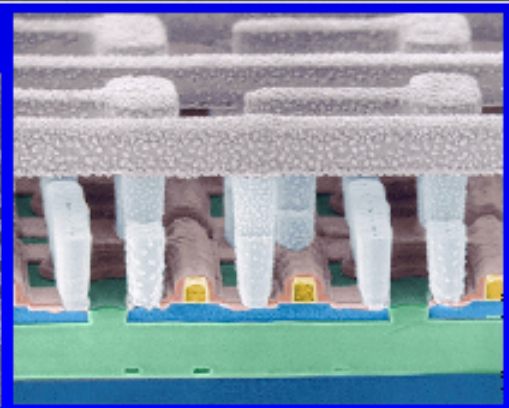






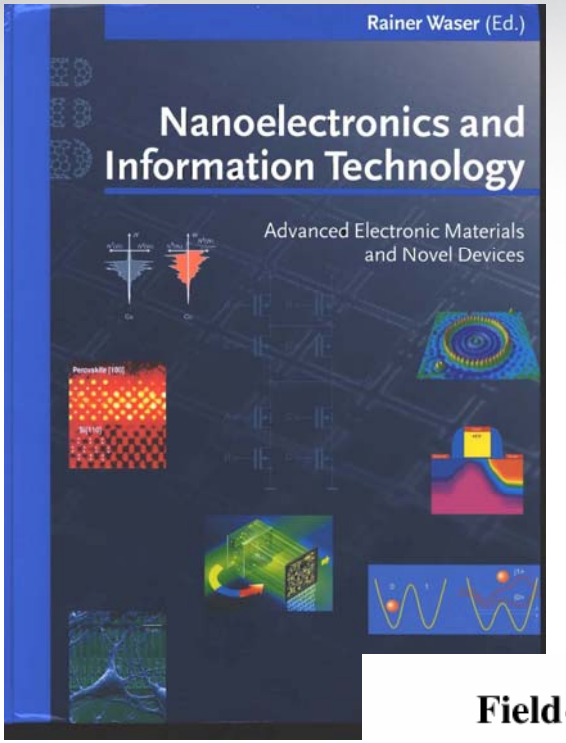






Ref. P. Wong, IBM

References



Logic Circuits with Carbon Nanotube Transistors

Adrian Bachtold,* Peter Hadley, Takeshi Nakanishi, Cees Dekker†

We demonstrate logic circuits with field-effect transistors based on single carbon nanotubes. Our device layout features local gates that provide excellent capacitive coupling between the gate and nanotube, enabling strong electrostatic doping of the nanotube from *p*-doping to *n*-doping and the study of the nonconventional long-range screening of charge along the one-dimensional nanotubes. The transistors show favorable device characteristics such as high gain (>10), large on-off ratio ($>10^5$), and room-temperature operation. Importantly, the local-gate layout allows for integration of multiple devices on a single chip. Indeed, we demonstrate one-, two-, and three-transistor circuits that exhibit a range of digital logic operations, such as an inverter, a logic NOR, a static random-access memory cell, and an ac ring oscillator.

Field-Modulated Carrier Transport in Carbon Nanotube Transistors

J. Appenzeller,[1] J. Knoch,[2] V. Derycke,[1] R. Martel,[1] S. Wind,[1] and Ph. Avouris[1]
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(Received 2 April 2002; published 29 August 2002)

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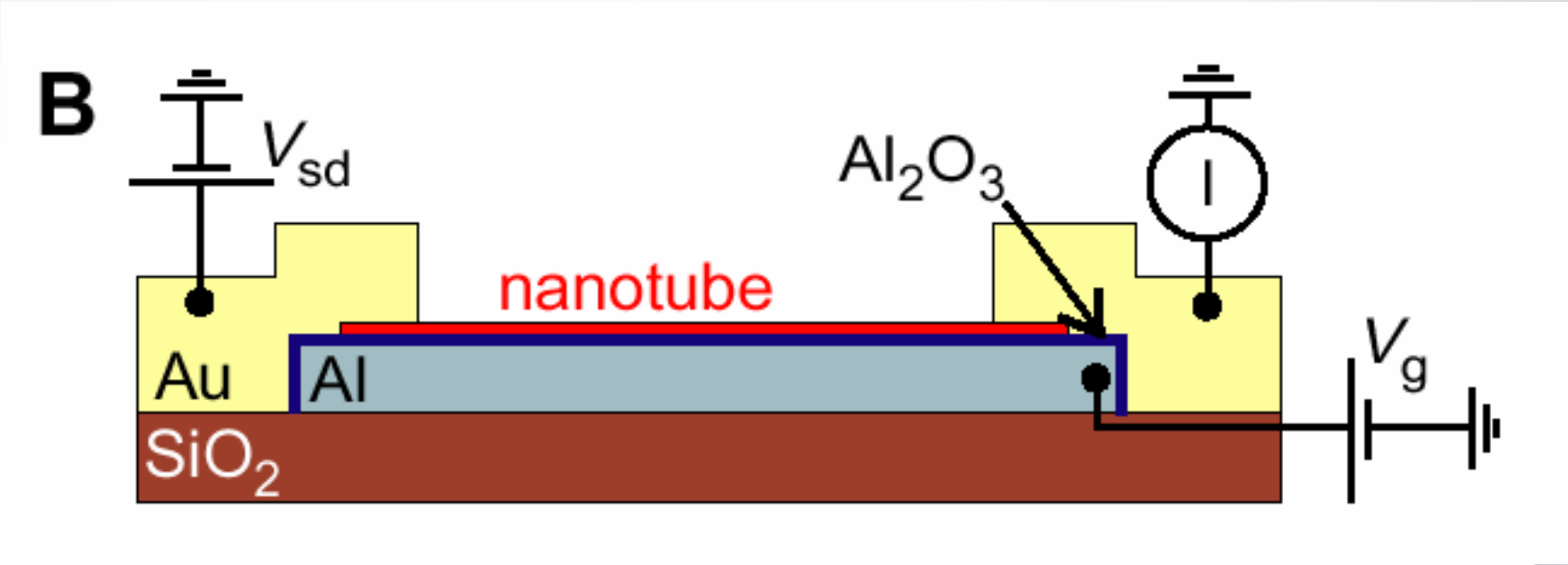
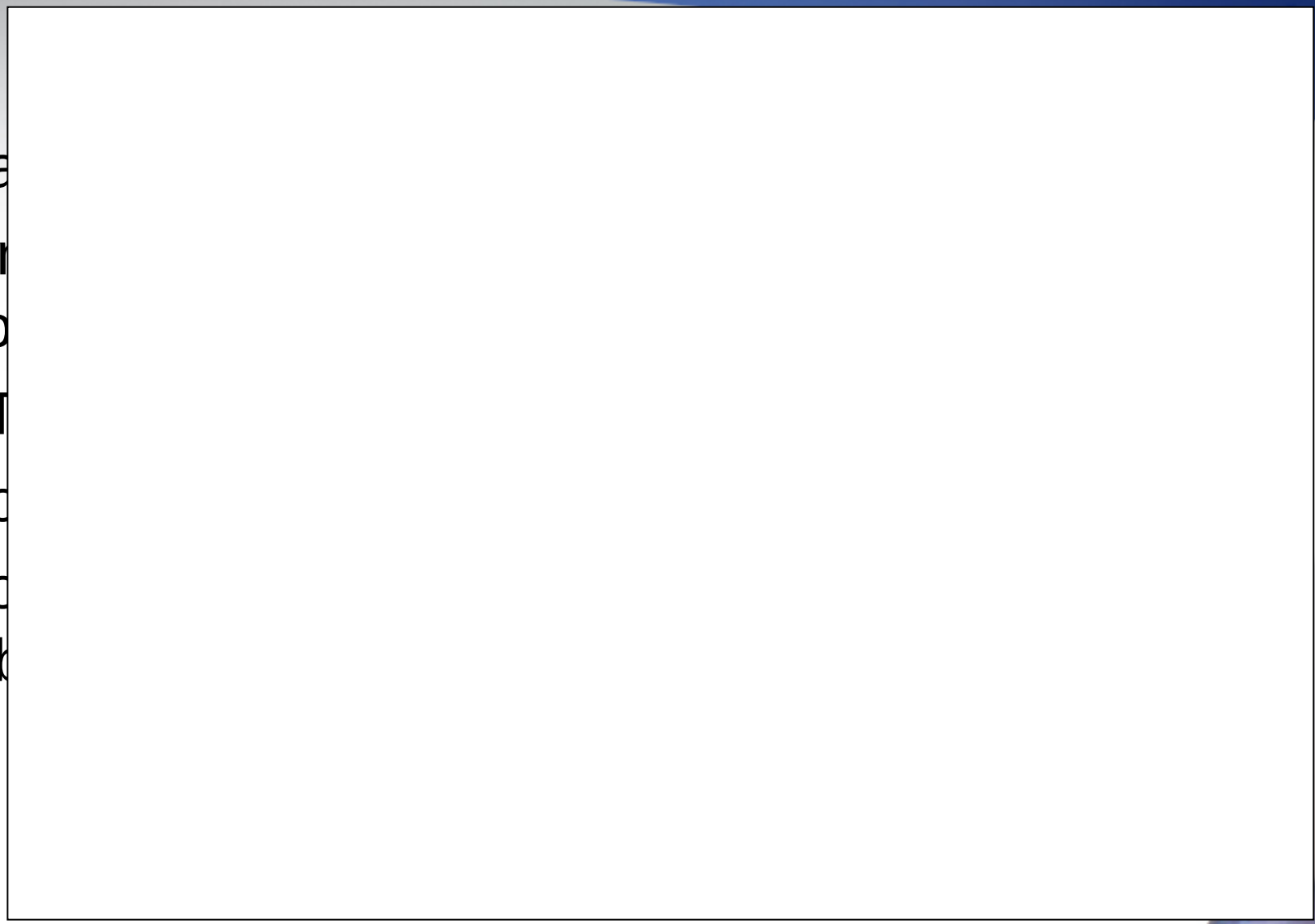
Carbon Nanotube: With Independent Gate

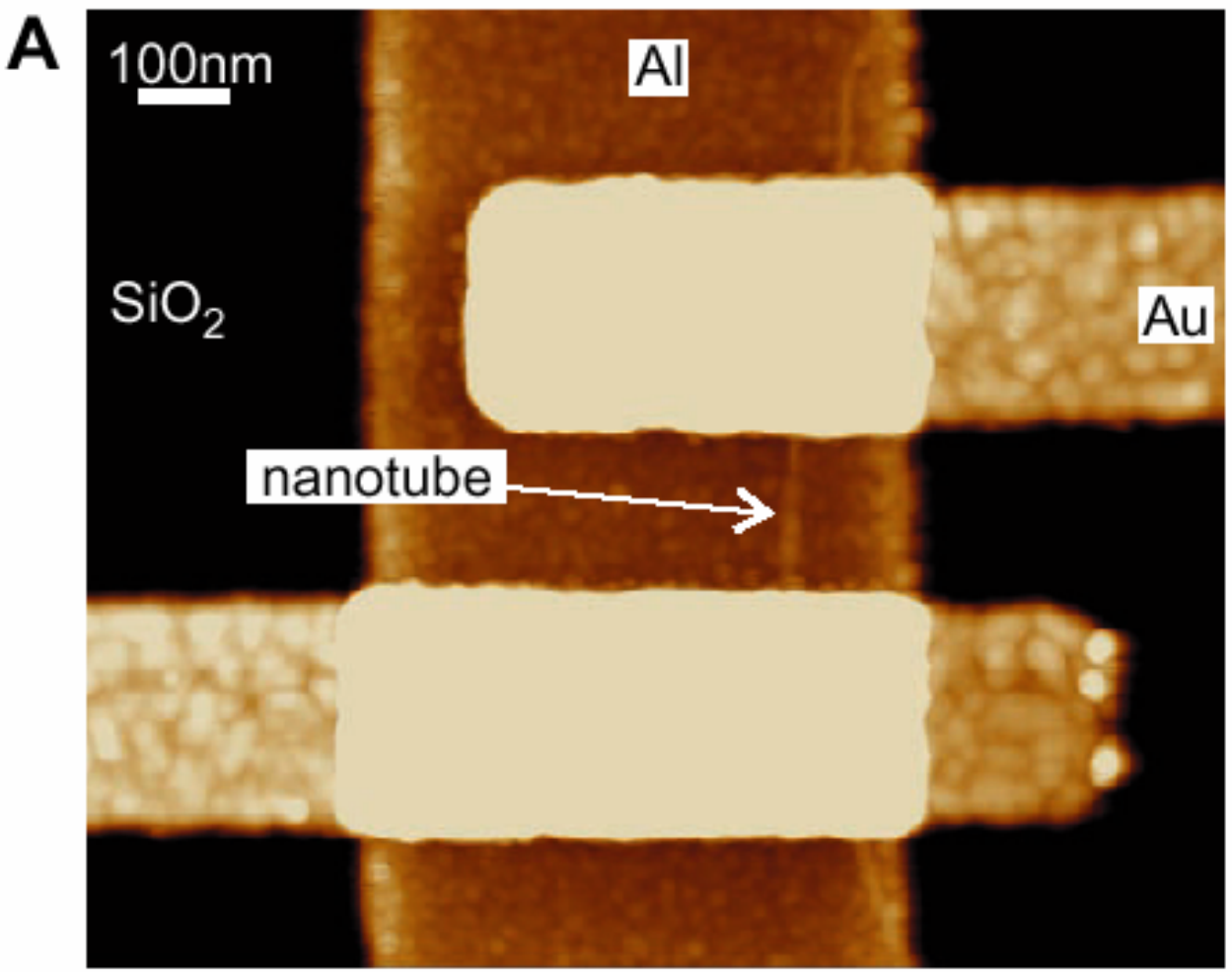


Process Flow

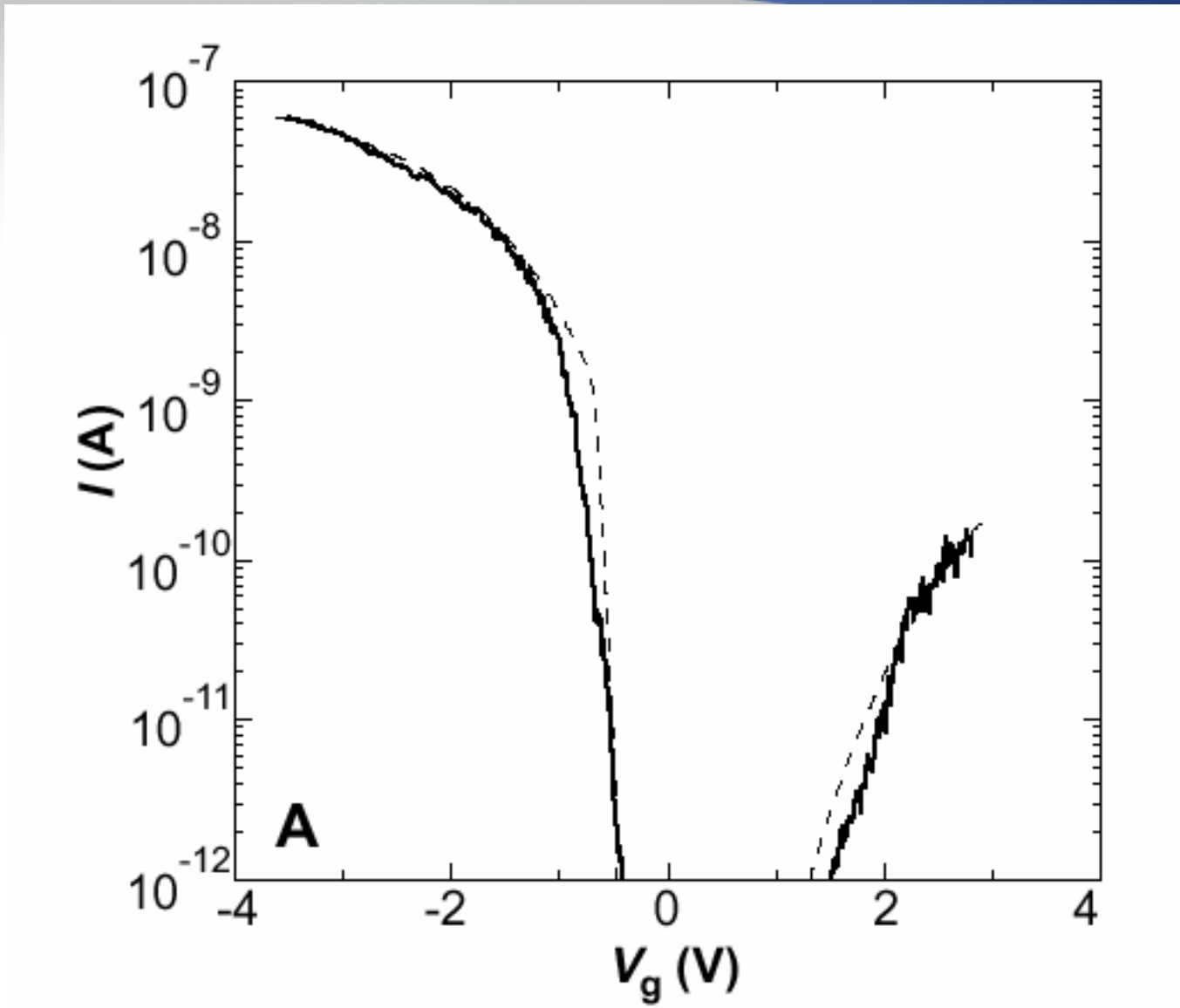
- Al
- Na
- Si
  fro
- AT
- Co
- Co
  fab



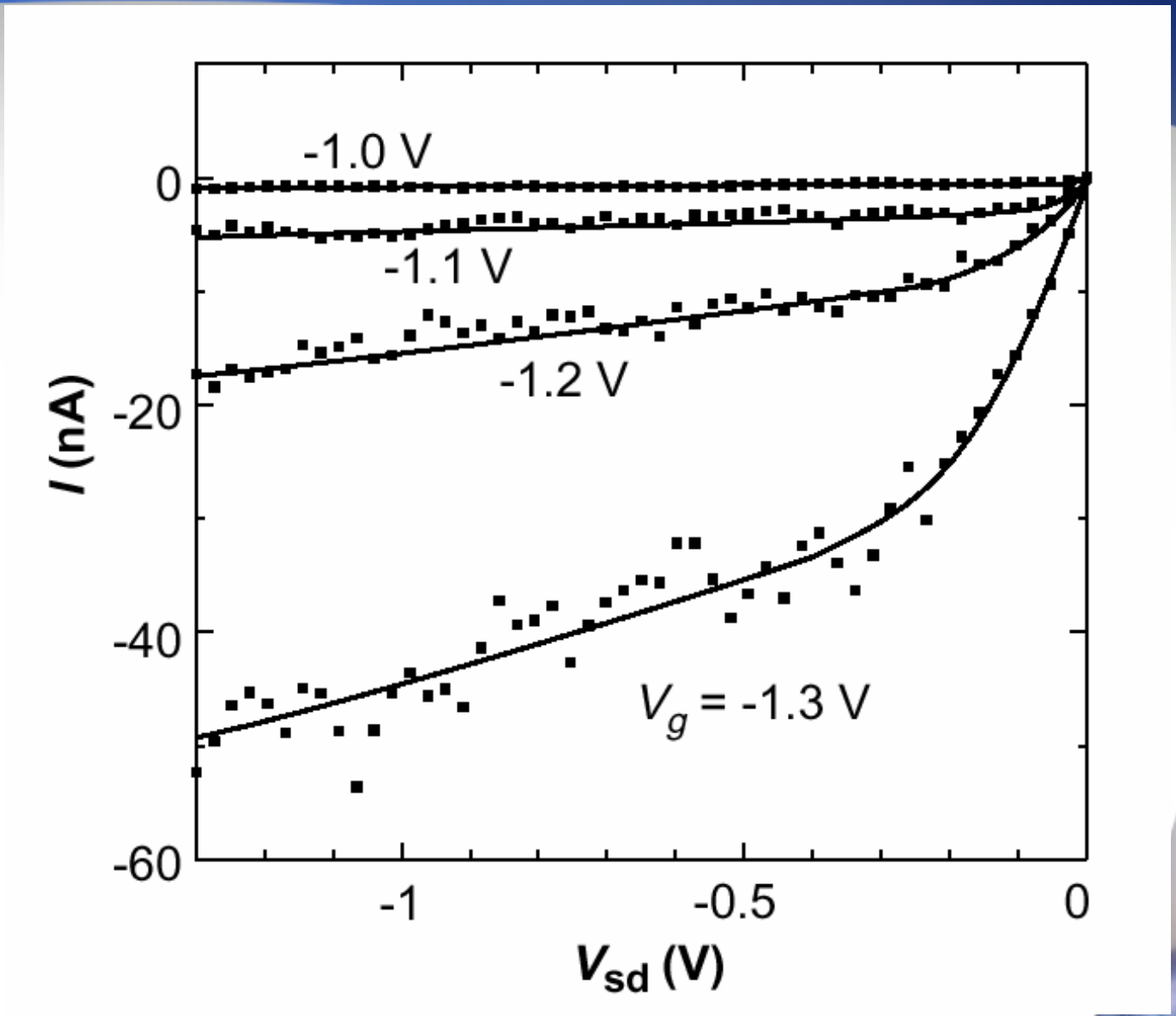
CNT



Log I-V 10^5 I_{ON}/ I_{OFF}



Linear V-I



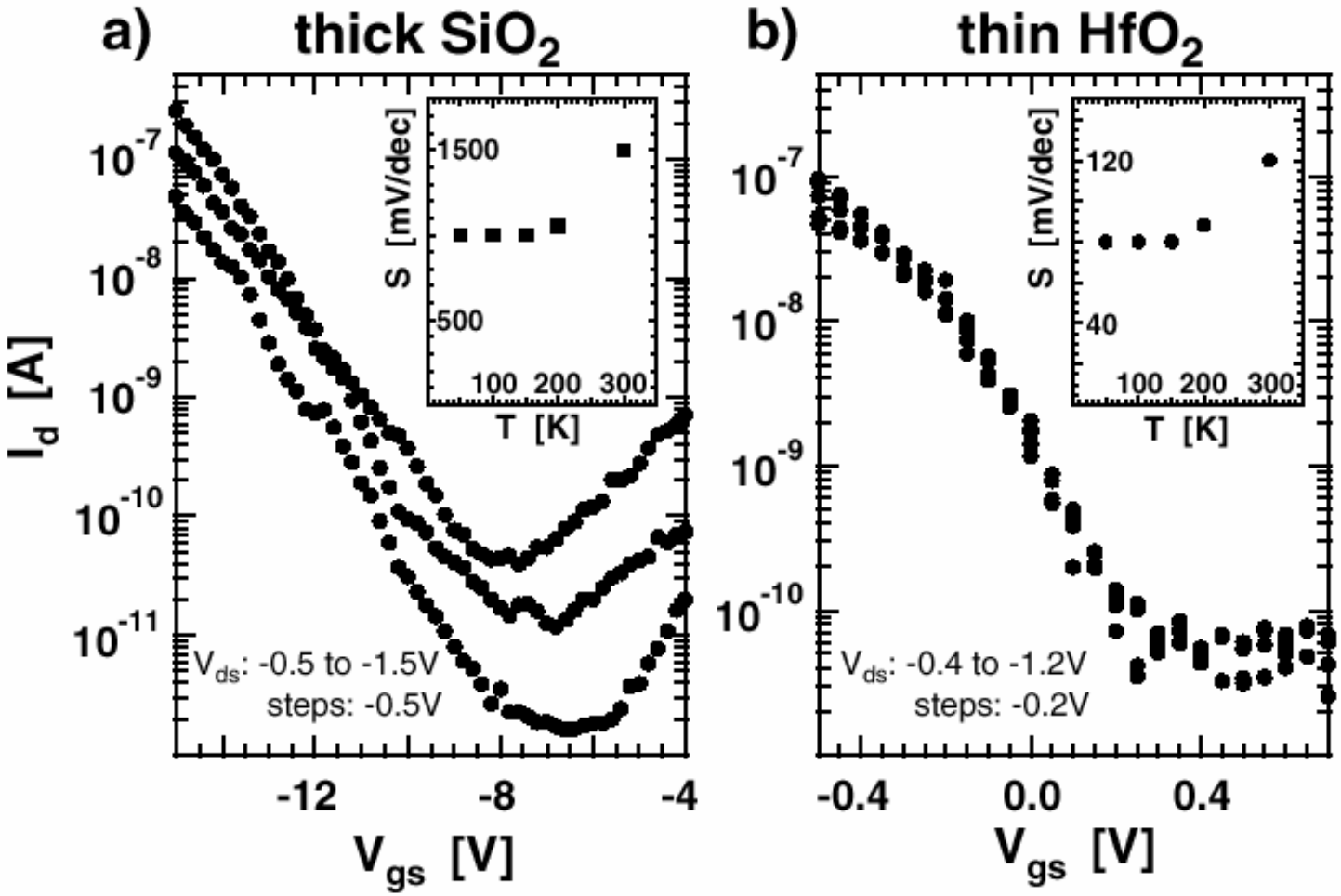
Transistors Metrics: How does CNT compare?

- Leakage
- Drive Current
- Overlap capacitance
- External resistance

Ambipolar Conduction

- So
  He
- Ex
  thi
- Fo
  un
  M
- La

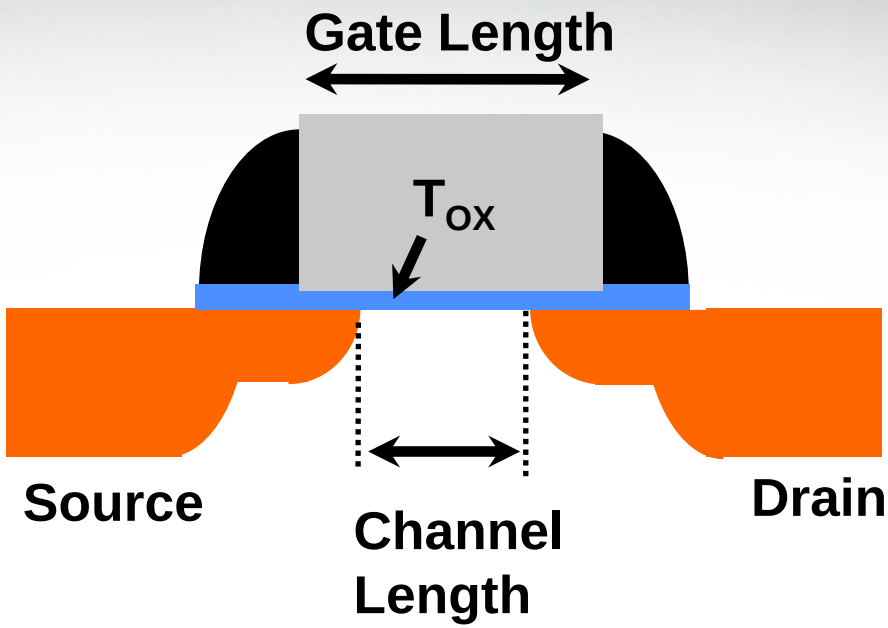
Unexpected Scaling Behavior



Higher ?

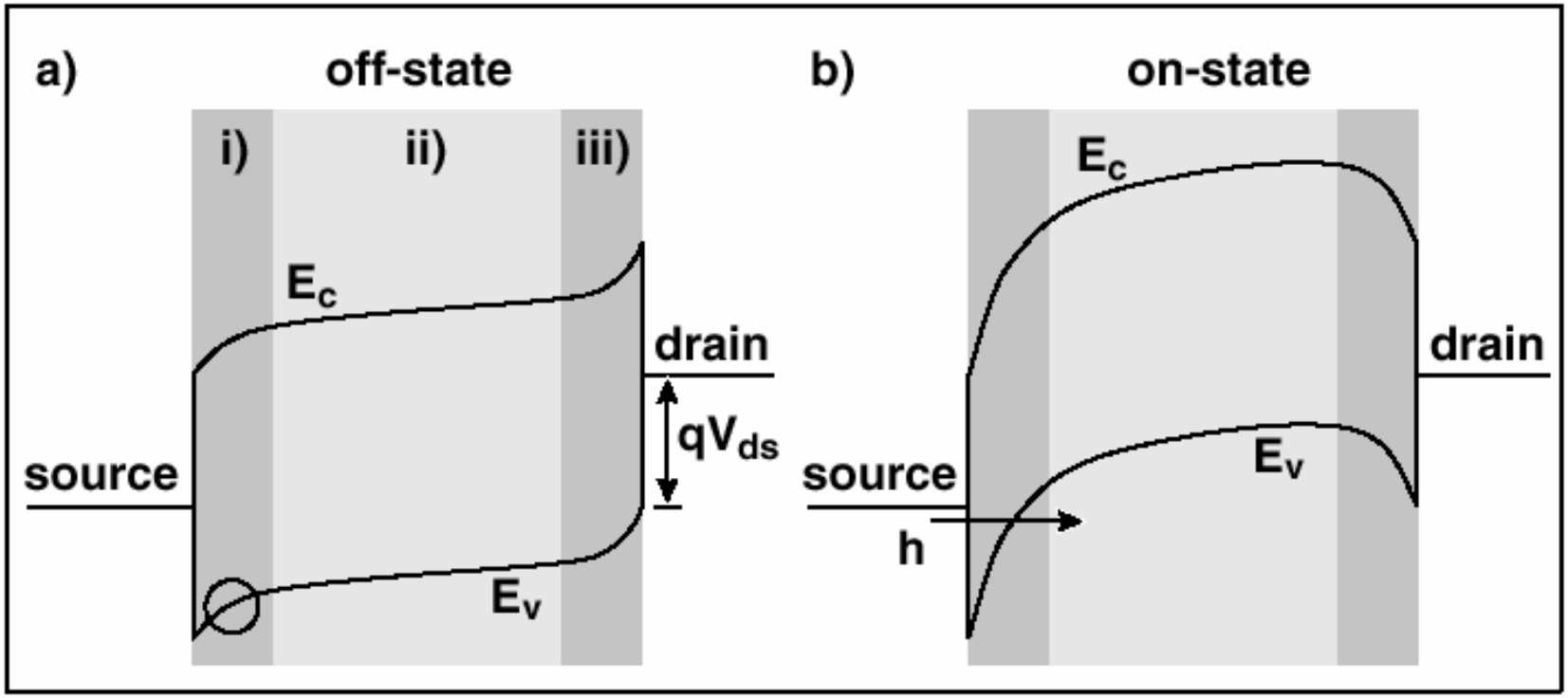
J. Appenzeller, PRL, 2002

Does Contacts to a MOSFET Pass Both Holes and Electrons



Draw Band Diagram nMOSFET + V_G and -V_G

Qualitative Transport Description

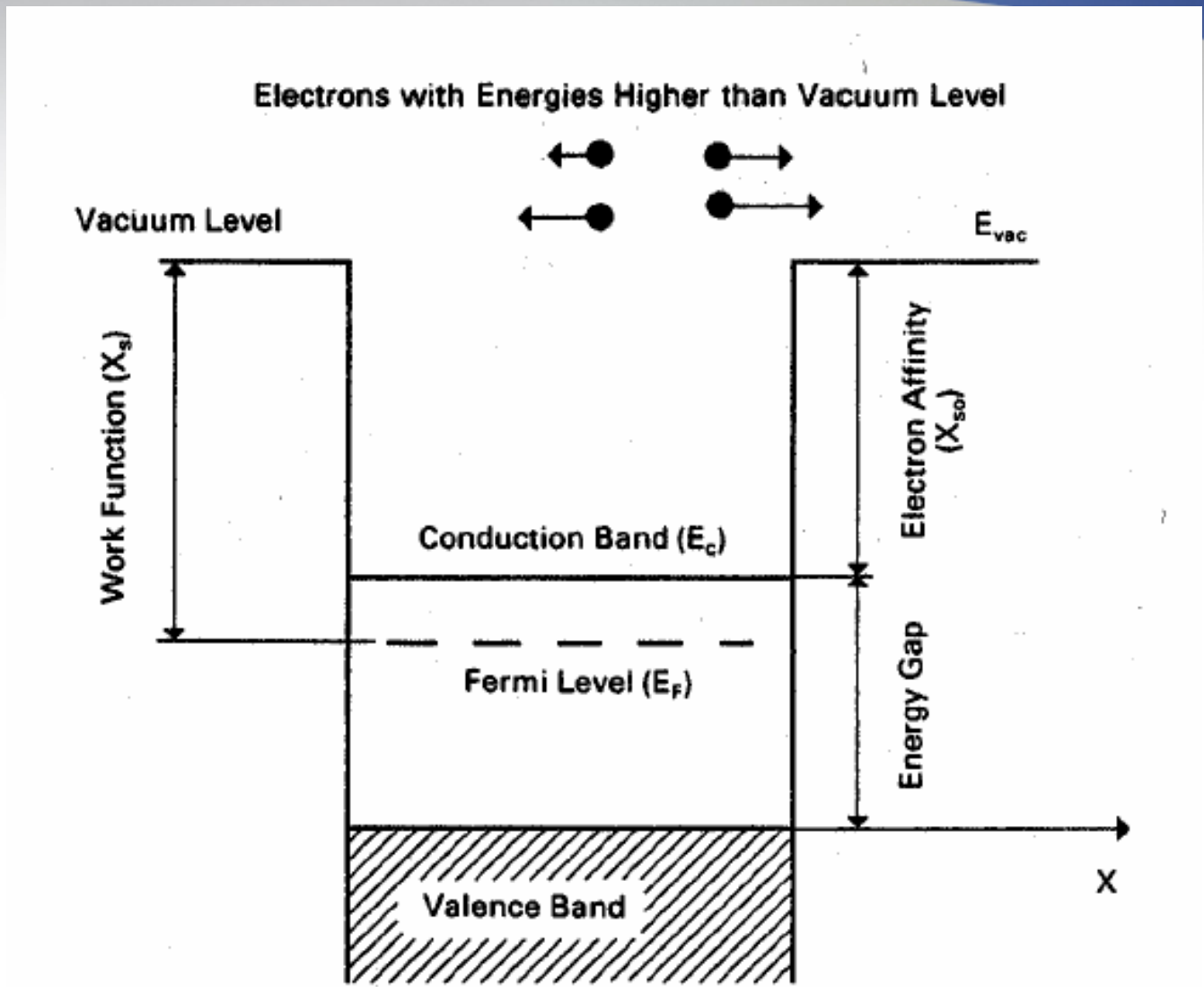


J. Appenzeller, PRL, 2002

Key Takeaways

- Si MOSFET
  - Ohmic metal contacts to source/drain of Si-MOSFET
  - Heavy doping creates very thin tunneling barrier
  - Source/drain only pass one carrier type (hole in P+ or electrons in N+)
  - I_{DS} saturates for Si MOSFET due to pinch-off (CNT-FET saturation attributed to same effect). WRONG
- CNT-FET
  - Difficult to create an ideal Ohmic CN metal contact
  - Intrinsic tube properties DO NOT limit device characteristics
  - Extraction of bulk nanotube related parameters e.g. mobility from I-V not justified
  - I-V controlled by existence of Schottky barriers at nanotube
  - Schottky barriers respond to applied electric field
  - Transmission probability for tunneling through the source Schottky barrier increases with decreasing barier thickness
  - Leads to exponential “turn on” with gate voltage like MOSFET
  - CNT FET current modulated by both gate and S/D voltage

Define: Work Function, Electron Affinity



Shur, Physics of Semiconductor Devices

Energy Band Diagram of Schottky Barrrier

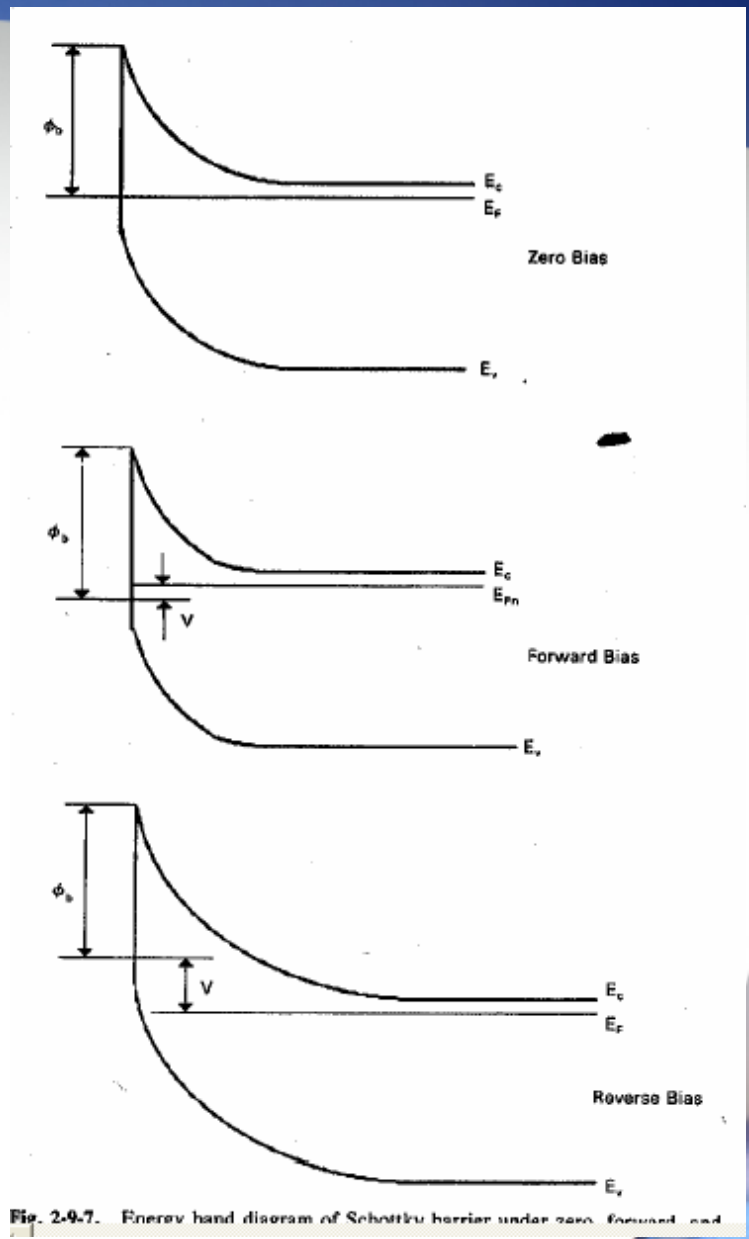
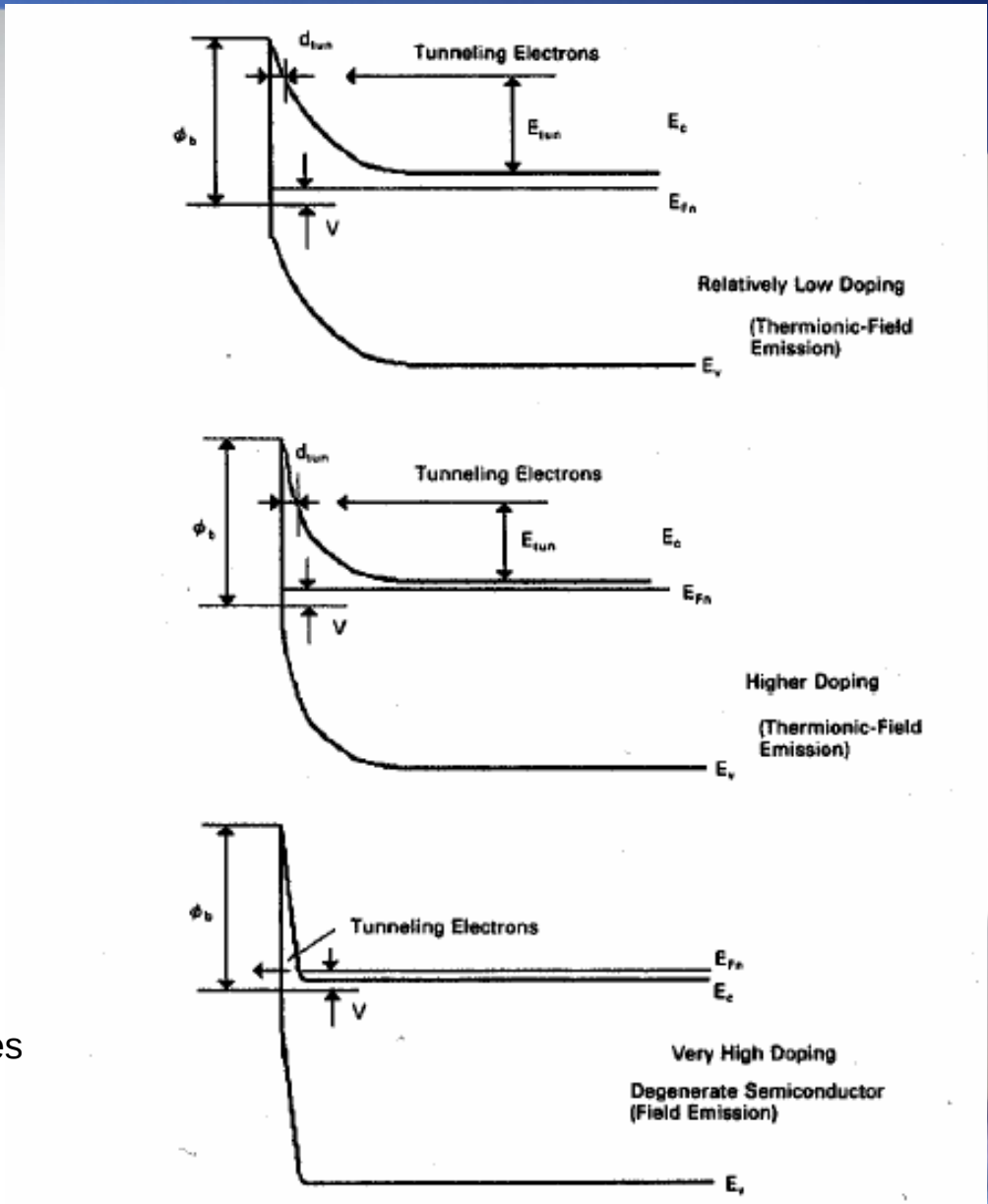


Fig. 2-9-7. Energy band diagram of Schottky barrier under zero, forward, and

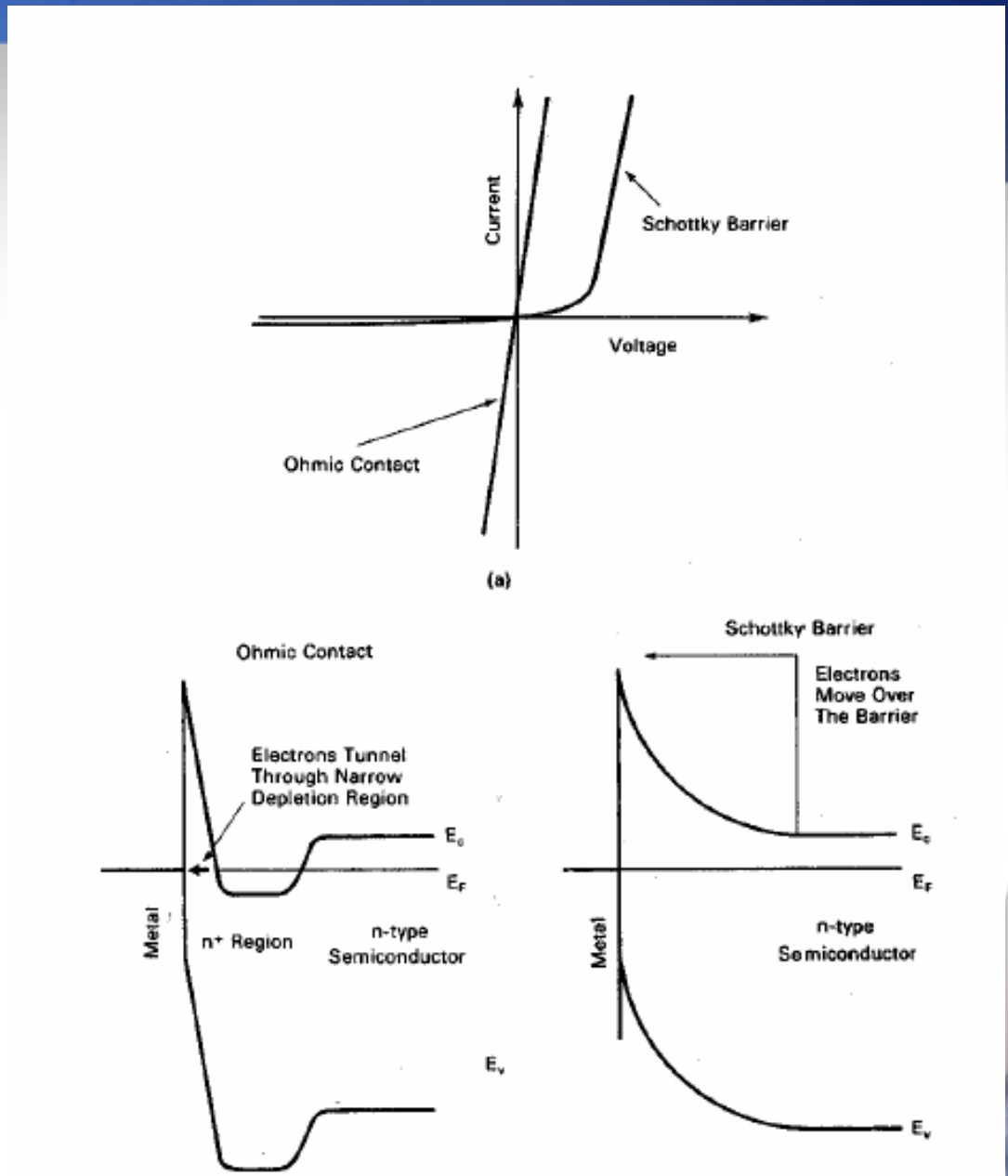
Shur, Physics of Semiconductor Devices

Energy Band Diagram of Schottky Barrrier

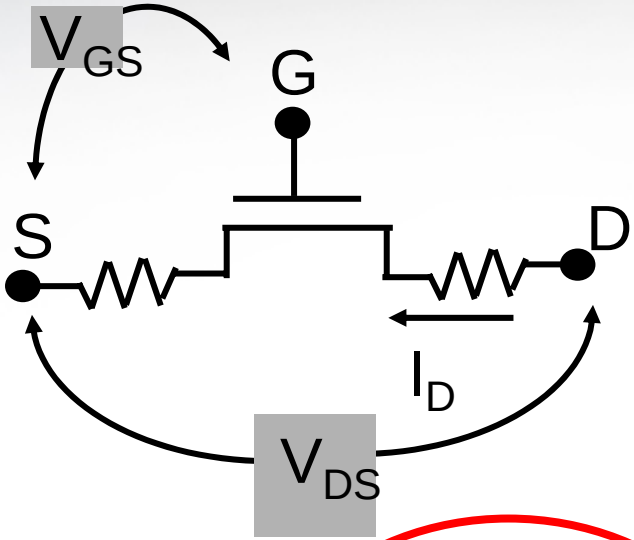


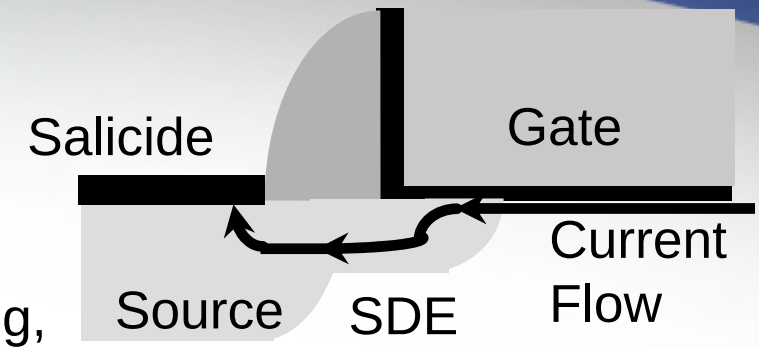
Shur, Physics of Semiconductor Devices

I-V Curves

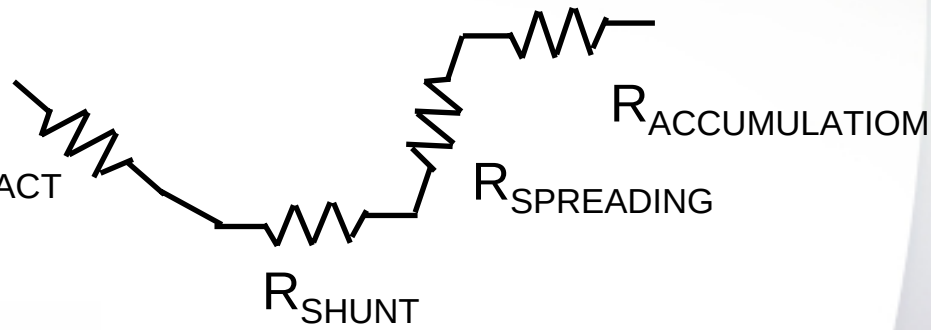

Current
Schottky Barrier
Voltage
Ohmic Contact
(a)
Ohmic Contact
Electrons Tunnel
Through Narrow
Depletion Region
E_c
E_F
Metal
n^+ Region
n-type
Semiconductor
E_v
Schottky Barrier
Electrons
Move Over
The Barrier
E_c
E_F
Metal
n-type
Semiconductor
E_v

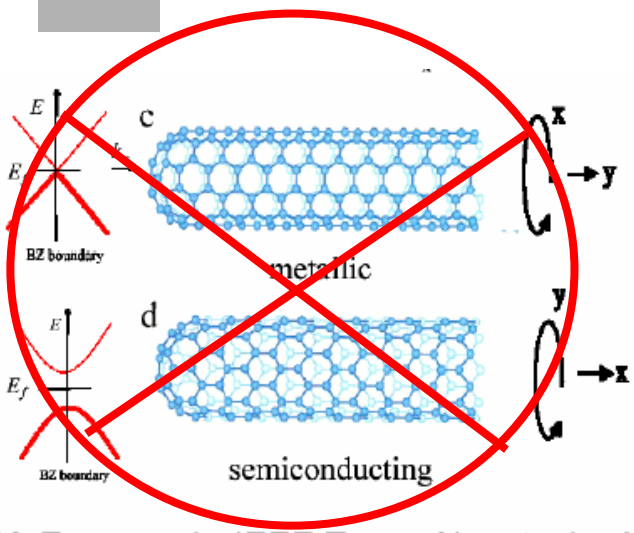
R_{EXT} In A MOSFET





K. K. Ng, 1986.





McEuen et al., *IEEE Trans. Nanotech.*, **1** ,

Is a better switch (i.e. carbon nanotude) is the issue for microelectronics?

R_{EXT}

DRAM ½ PITCH (nm)	130	100	80	65	45	32	22
MPU / ASIC ½ PITCH (nm)	150	107	80	65	50	35	25
MPU PRINTED GATE LENGTH (nm)	90	65	45	35	25	18	13
Physical gate length high-performance (HP) (nm)	65	45	32	25	18	13	9
Equivalent physical oxide thickness for high-performance t_{eq} (EOT) (nm)	1.3-1.6	1.1-1.6	0.8-1.3	0.6-1.1	0.5-0.8	0.4-0.6	0.4-0.5
Gate depletion and inversion layer quantum effects electrical thickness adjustment factor (nm)	0.8	0.8	0.8	0.5	0.5	0.5	0.5
t_{ox} electrical equivalent (nm)	2.3	2.0	1.9	1.4	1.2	1.0	0.9
Nominal power supply voltage (V_{dd}) (V)	1.2	1.0	0.9	0.7	0.6	0.5	0.4
Nominal high-performance NMOS sub-threshold leakage current, $I_{sd,leak}$ (at 25°C) (μA/μm)	0.01	0.07	0.3	1	3	7	10
Nominal high-performance NMOS saturation drive current I_D (at V_D, at 25°C) (μA/μm)	900	900	900	900	1200	1500	1500
Drain extension x_j (nm)	27-45	19-31	13-22	10-17	7-12	5-9	4-6
Maximum drain extension sheet resistance (PMOS)(Ω/sq)	400.0	550.0	770.0	760.0	830.0	940.0	1210.0
Contact (nm)	48-95	33-66	24-47	18-37	13-26	10-19	7-13
Silicide thickness (nm)	35.8	24.8	17.6	13.8	9.9	7.2	5.0
Contact silicide sheet $R_{contact}$ (Ω/sq)	4.2	6.1	8.5	10.9	15.2	21.0	30.3
Contact maximum resistivity (Ω/sq^2)	4.10E-07	2.70E-07	1.80E-07	1.10E-07	6.40E-08	3.80E-08	2.40E-08
Parasitic source/drain resistance (R_{SD}) (Ω-μm)	190	180	180	140	110	90	80
Parasitic source/drain resistance (R_{SD}) percent of ideal channel resistance (V_D/I_D)	16 %	17 %	19 %	20 %	25 %	30 %	35 %
High-performance NMOS device delay time τ (ps)	1.6	1.1	0.83	0.68	0.39	0.22	0.15
Energy per (w/L = 3) device switching transition (fJ)	0.347	0.137	0.065	0.032	0.015	0.007	0.002
Static power dissipation per (w/L = 3) device (W/device)	5.6E-09	1.0E-08	2.6E-08	5.3E-08	9.7E-08	1.4E-07	1.1E-07

Manufacturable solutions exist, and are being optimized

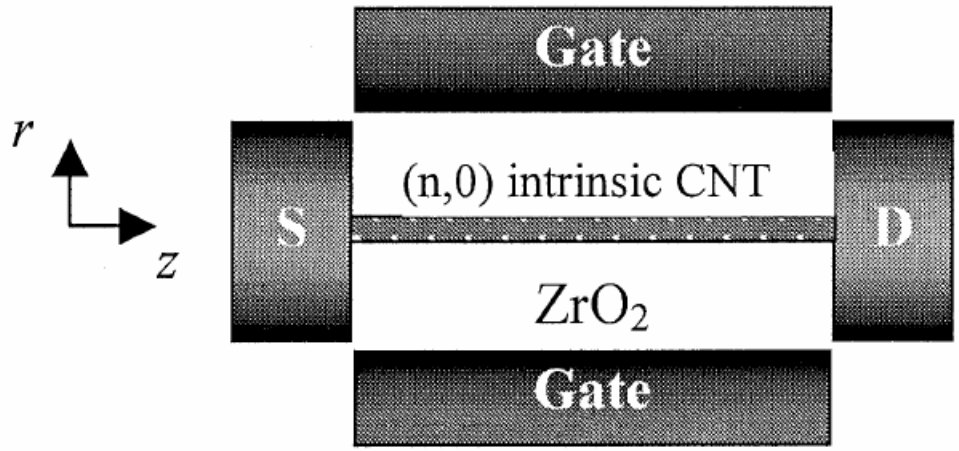
Manufacturable solutions are known

Manufacturable solutions are NOT known

Table 2: Requirements for high performance logic (MPU, ASIC) and for memory (DRAM) applications taken from the International Technology Roadmap for Semiconductors 2001 [9]. MPU is the Micro Processor Unit and ASIC is a Application Specific Integrated Circuit. The pitch size denotes the closest distance of metal lines in the first metal layer and EOT the equivalent oxide thickness

In order to increase the IC package density, the CMOS transistor is shrinking in all dimensions. According to Tab. 2 the half pitch size also known as the "technology node" is shrinking as well as the gate length, the dielectric thickness and the junction depth.

Simulation CNT-FET



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CNT-FET For Different Metal X_M

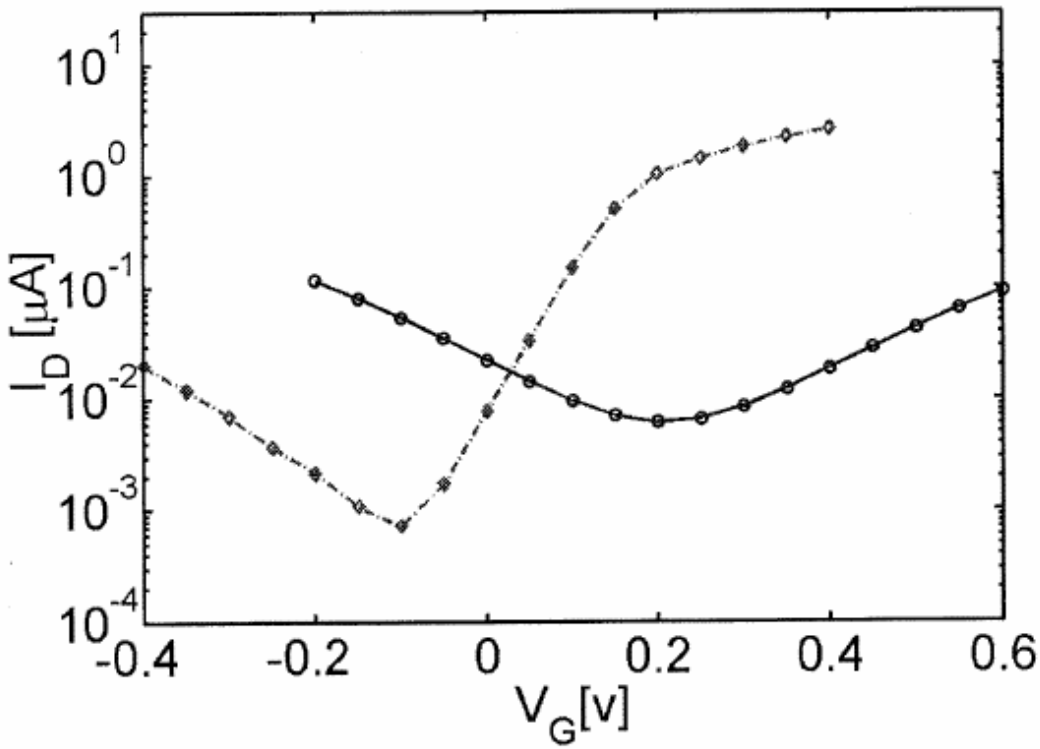

Fig. 4. I_D versus V_G for thick gate oxide (the oxide thickness $t_{ox} = 40$ nm and dielectric constant $\varepsilon = 25$). The channel length is 100 nm. The SB height for electrons is $\phi_{bn} = 0$ (the solid-dash lines) and $\phi_{bn} = E_g/2$ (the solid lines). A (25,0) nanotube (with a diameter $d \_ 2.0$ nm and $E_g \_ 0.43$ eV) is used as channel.

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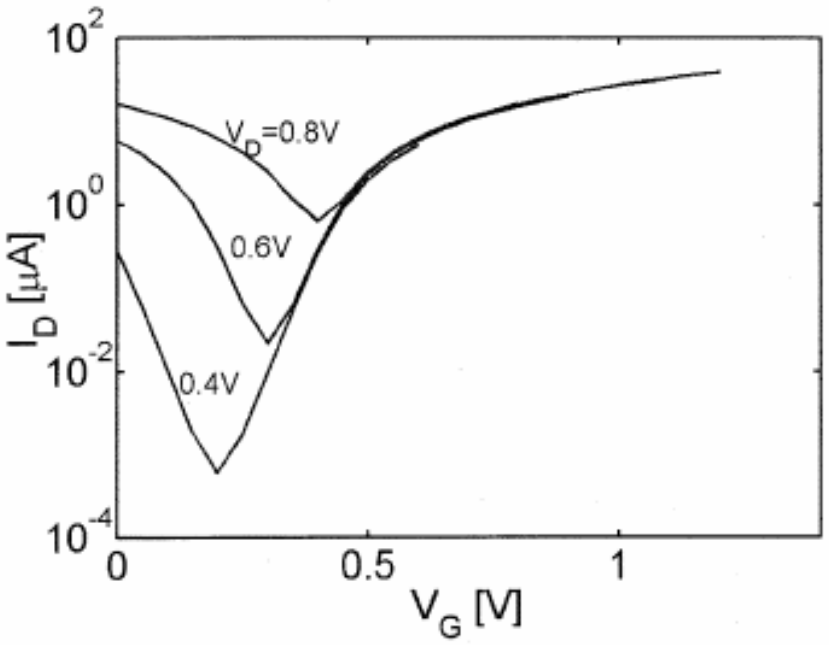
10^2
10^0
10^{-2}
10^{-4}
I_D [μA]
V_D=0.8V
0.6V
0.4V
0
0.5
1
V_G [V]

(a)

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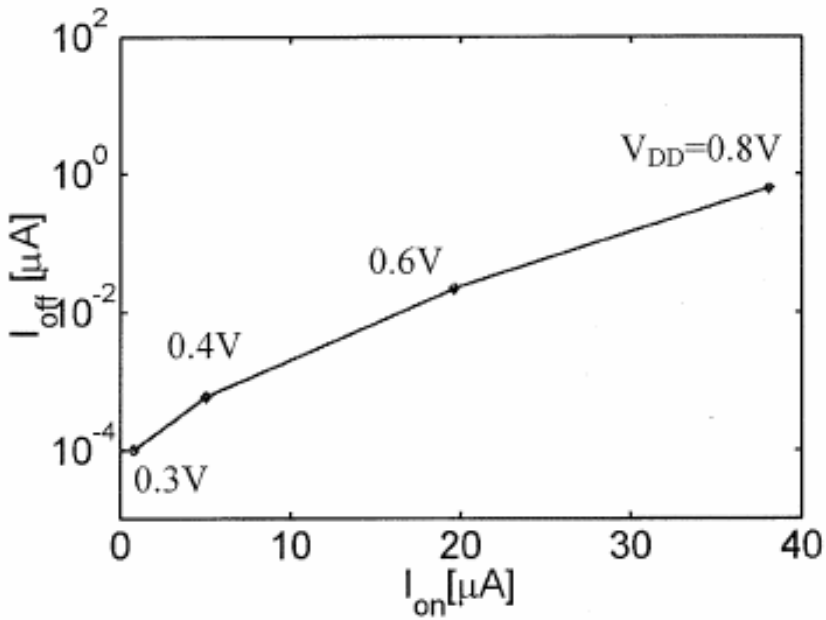
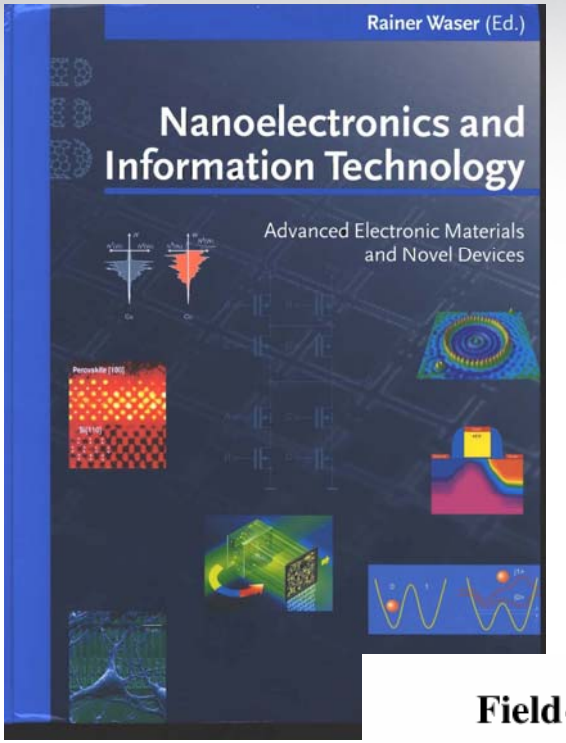

10^2
10^0
10^{-2}
10^{-4}
I_{off} [μA]
V_{DD}=0.8V
0.6V
0.4V
0.3V
0
10
20
30
40
I_{on}[μA]

(b)

Lecture 16: References



Chapter 19 book

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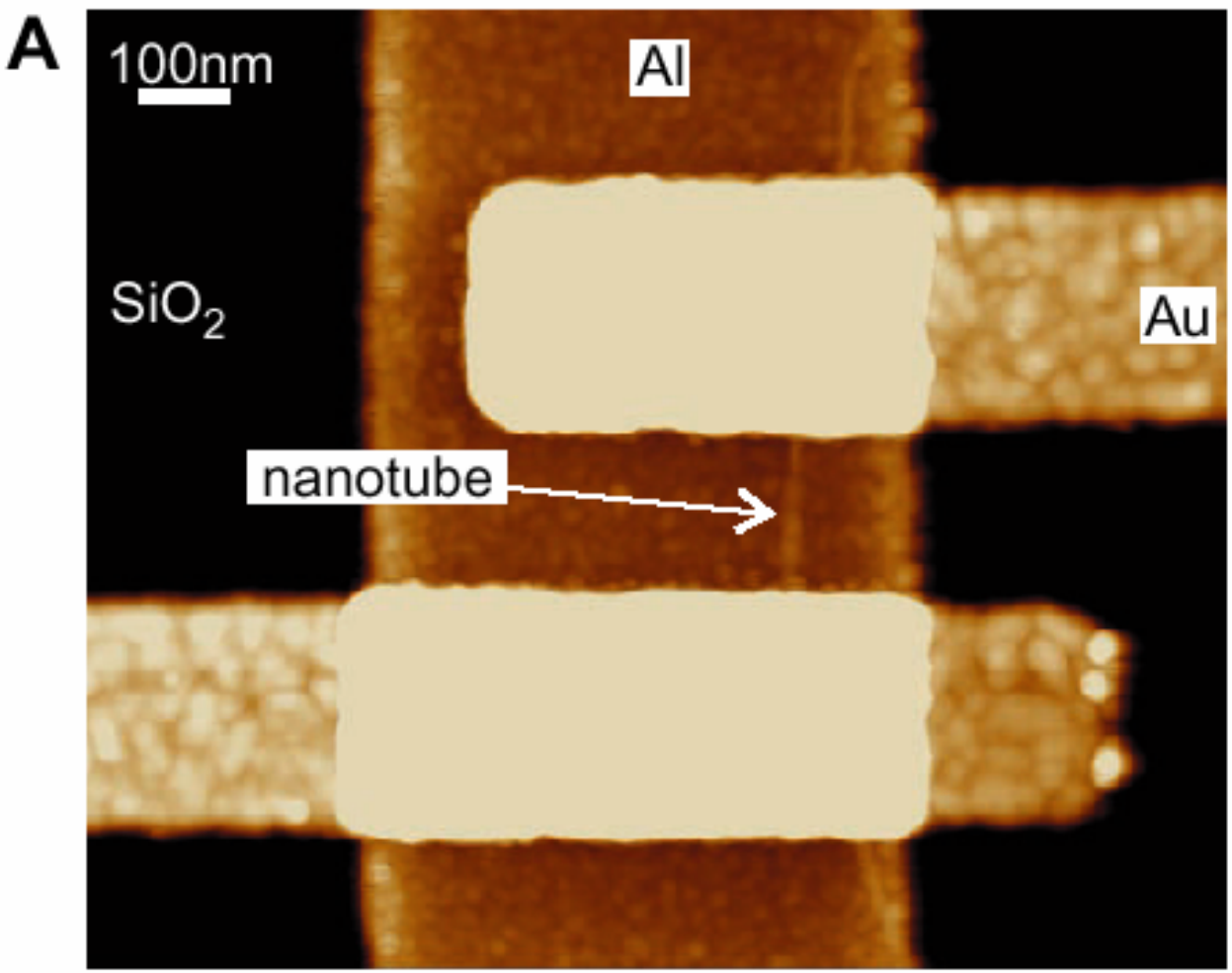
Papers Contributions

Logic Circuits with Carbon Nanotube Transistors

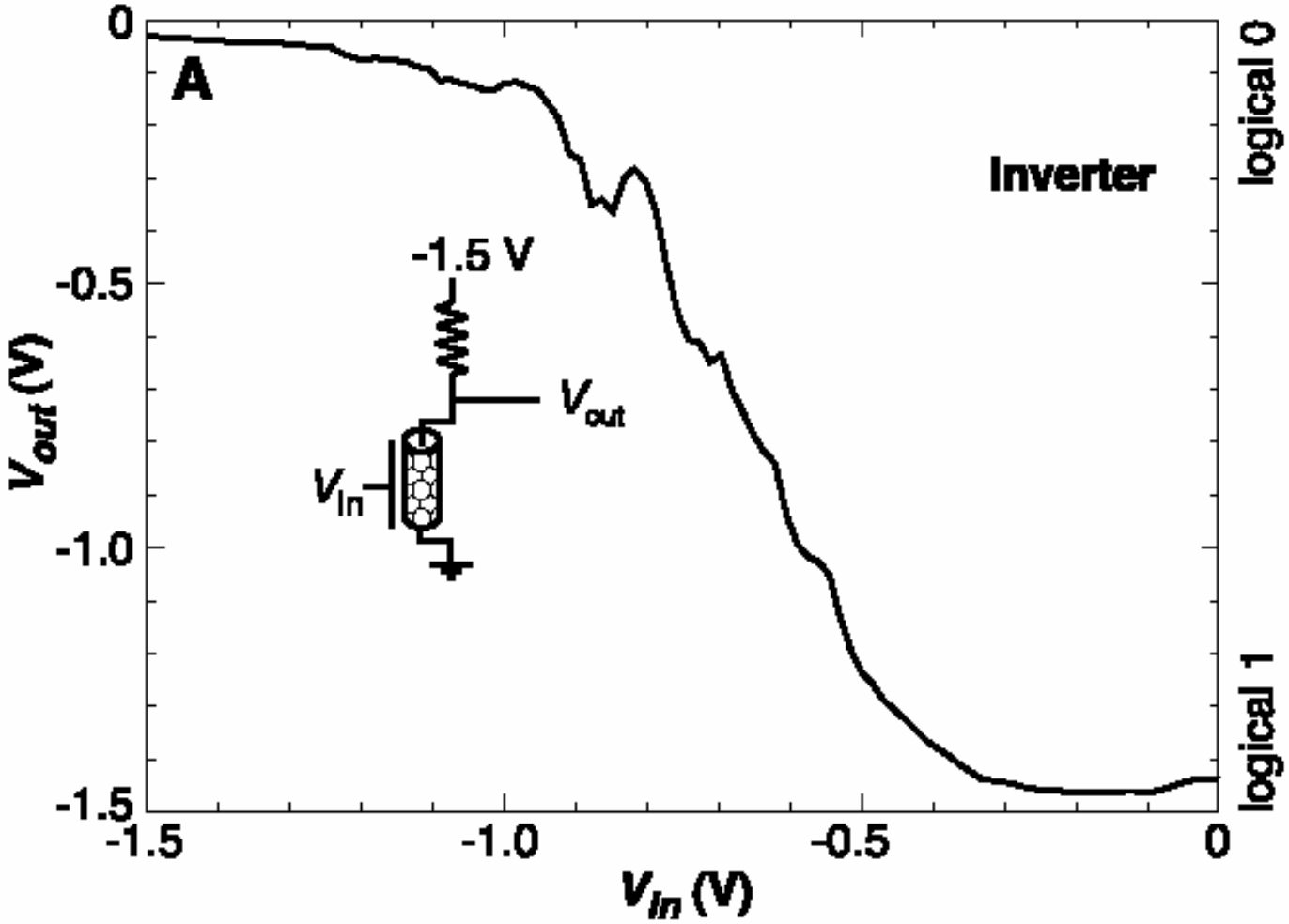
Adrian Bachtold,* Peter Hadley, Takeshi Nakanishi, Cees Dekker†

- Integration of molecule components
- Local gate layout: independent control of gates
- 3 transistor circuit demonstrated
- Demonstrated invertor, NOR, SRAM
  - AND,OR, NAND, XOR could also be demonstrated
- Use Resistor-Transistor Logic:
  - 0 to -1.5V
  - Off chip 100M ohms resistor

CNT



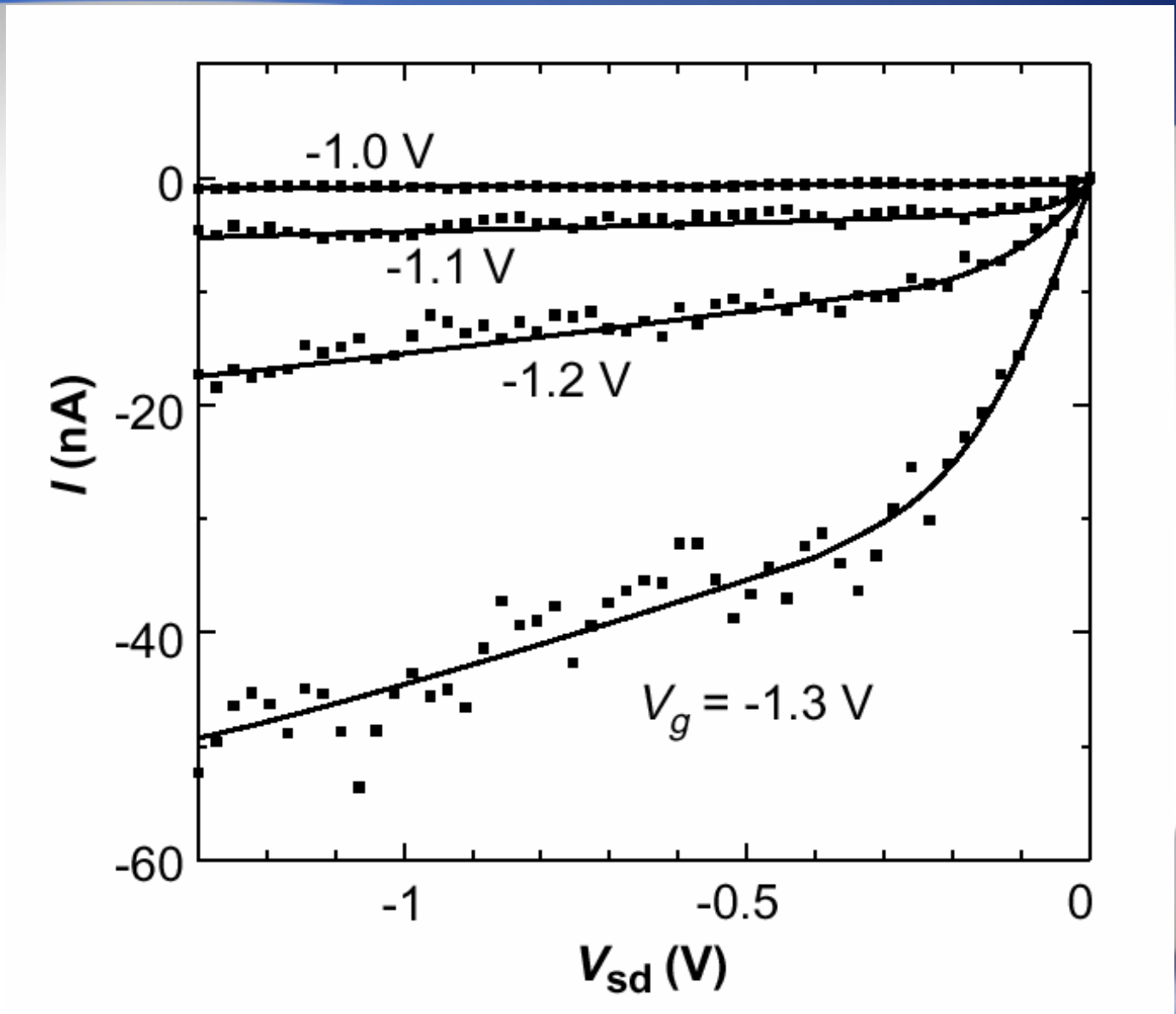
1st Inverter



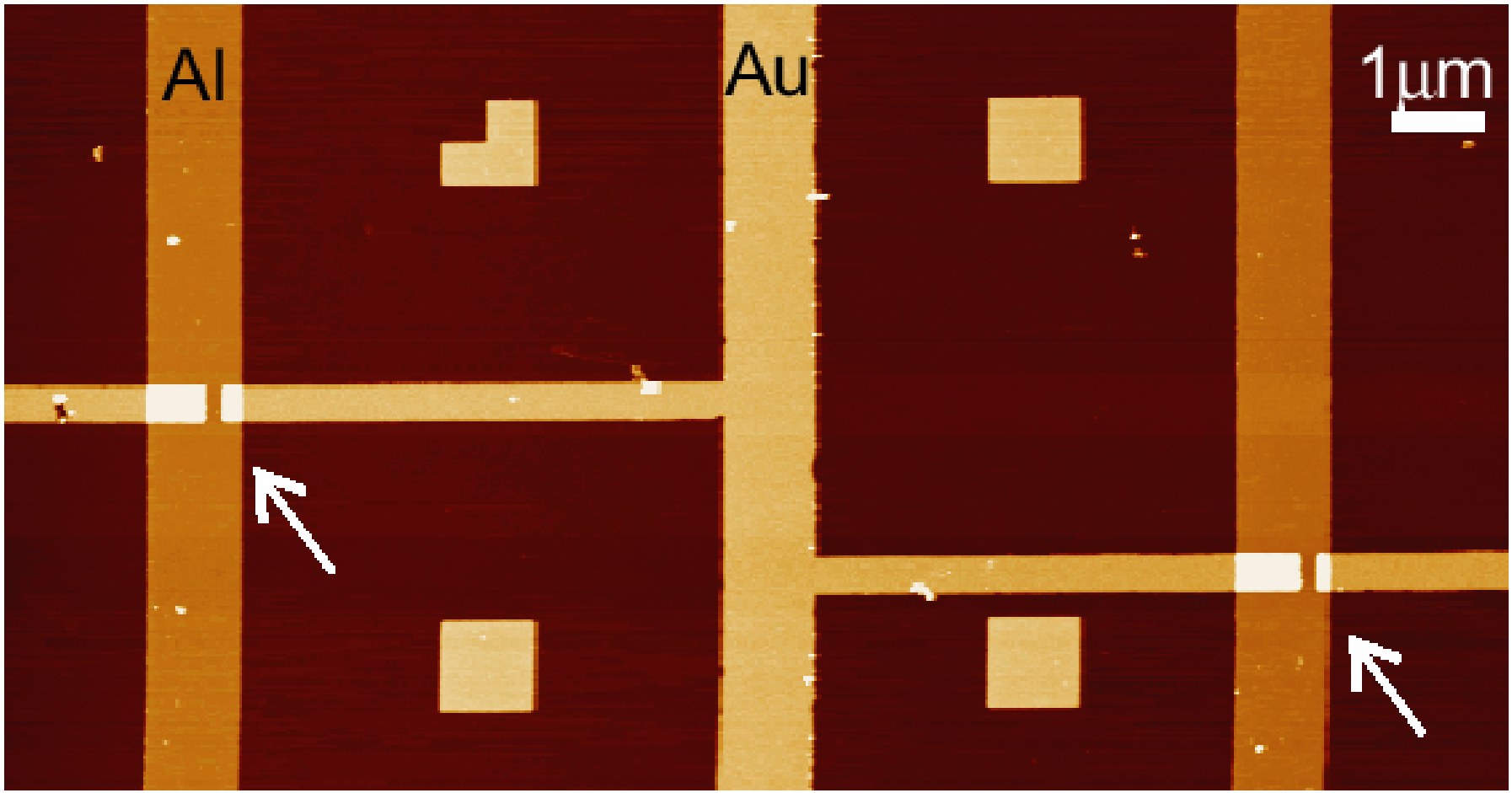
Logic Circuits with Carbon Nanotube Transistors

What is the Gain?

Resistance of CNT (when "ON)?

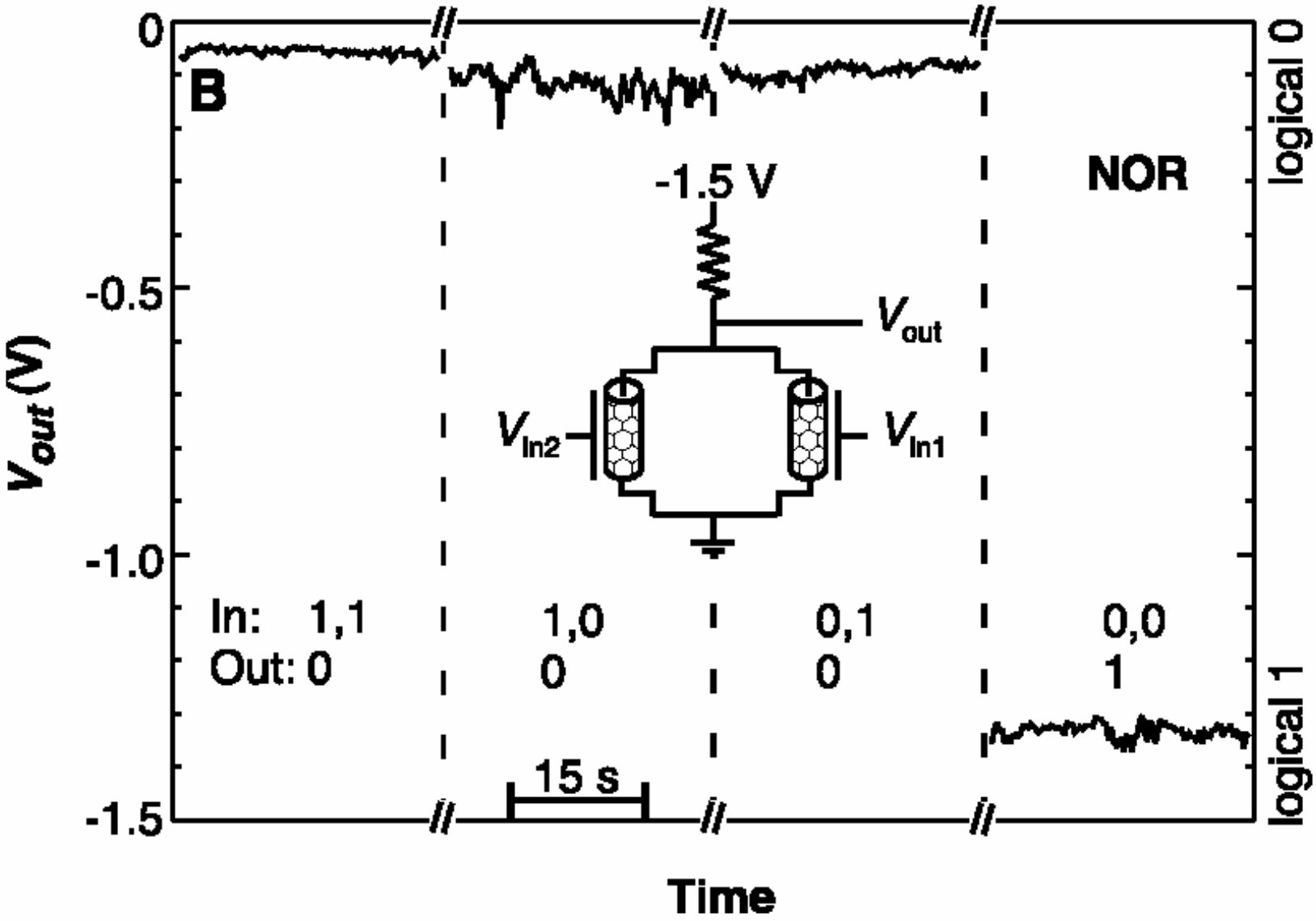


Two CNT-FET Connected Together

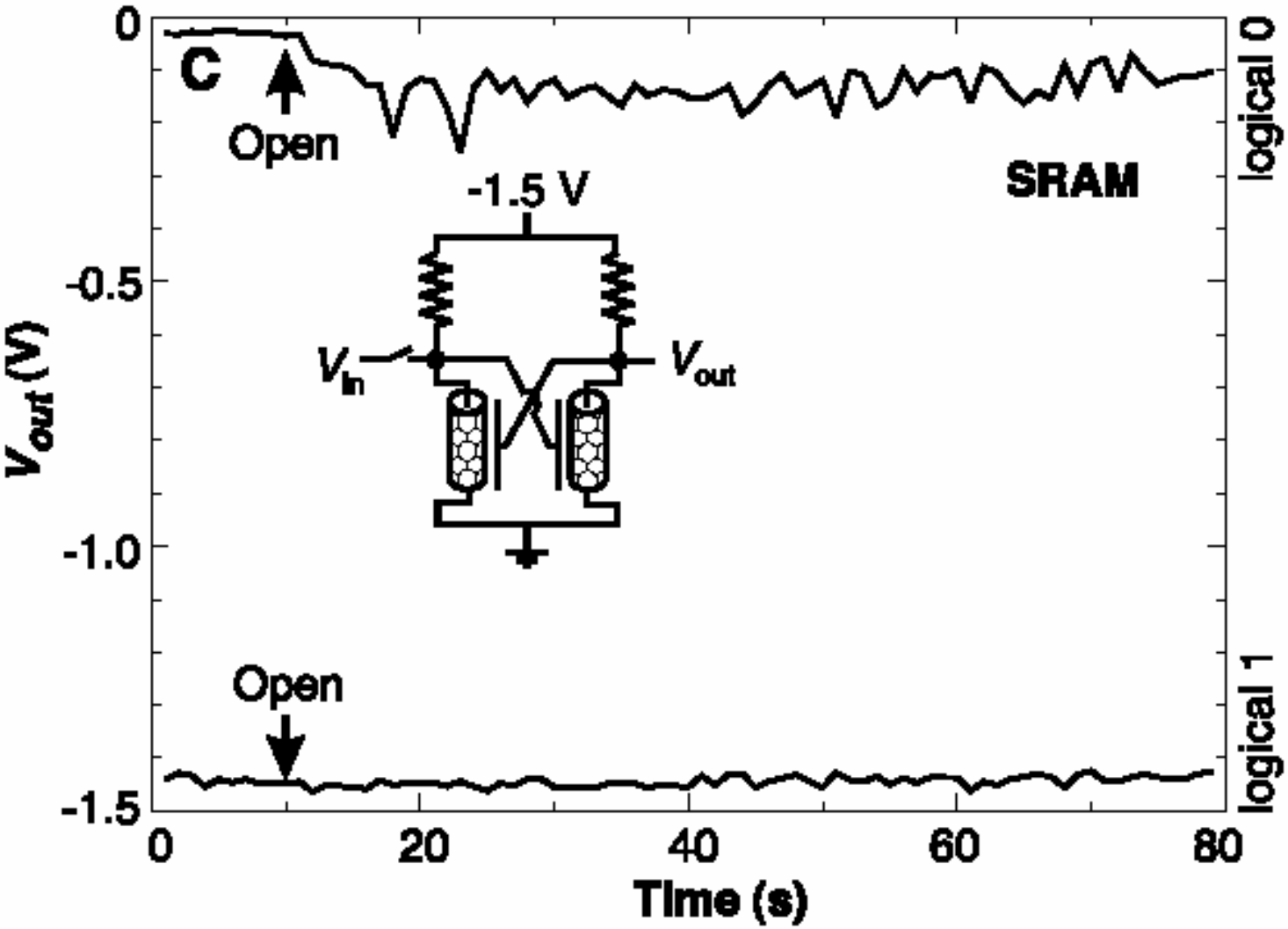


Logic Circuits with Carbon Nanotube Transistors

NOR


B
0
-0.5
-1.0
-1.5
V_{out} (V)
-1.5 V
V_{out}
V_{In2}
V_{In1}
NOR
logical 0
logical 1
In: 1,1 1,0 0,1 0,0
Out: 0 0 0 1
15 s
Time

SRAM


0
-0.5
-1.0
-1.5
V_{out} (V)
C
Open
-1.5 V
SRAM
V_{in}
V_{out}
logical 0
Open
logical 1
0
20
40
60
80
Time (s)

Statements From Book

- “The realization of simple logic circuits represents a giant step towards the integration of carbon nanotubes”
- “This proof of their operation further enhances the thrust in driving CNT technology forward”
- “Noted only build out of P-type transistors”

Text book p494

N and P FET Inverter Demonstrated

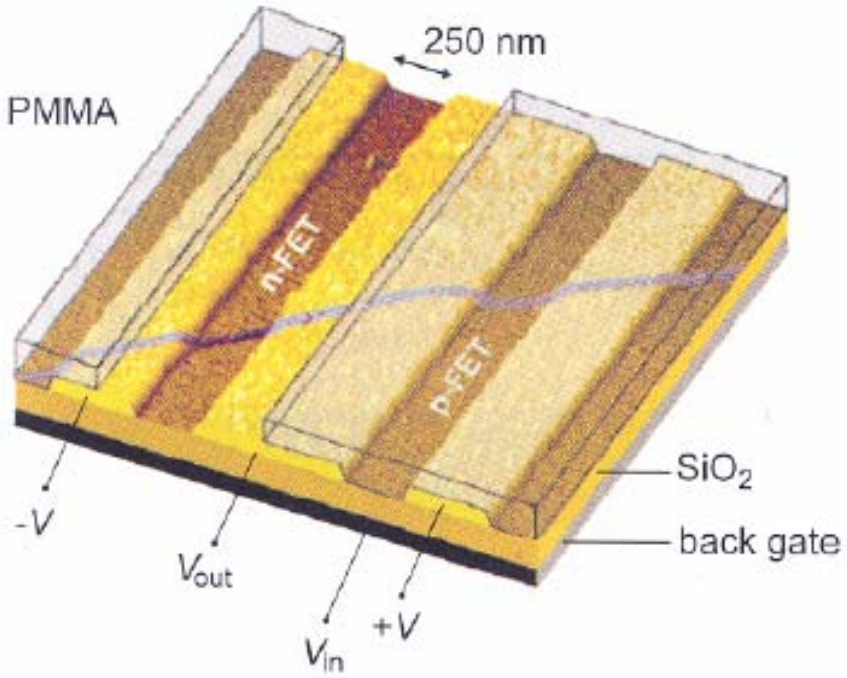


Figure 32: Intramolecular complementary CNTFET gate made by an n-type and p-type CNTFET in series, operated by a common back-gate. Complementary transistors are produced from one single nanotube by doping the section which is not covered by the PMMA resist with potassium (after [63]).

Avouris, Nano Letters 2001

CNT P-FET Converted to N-FET

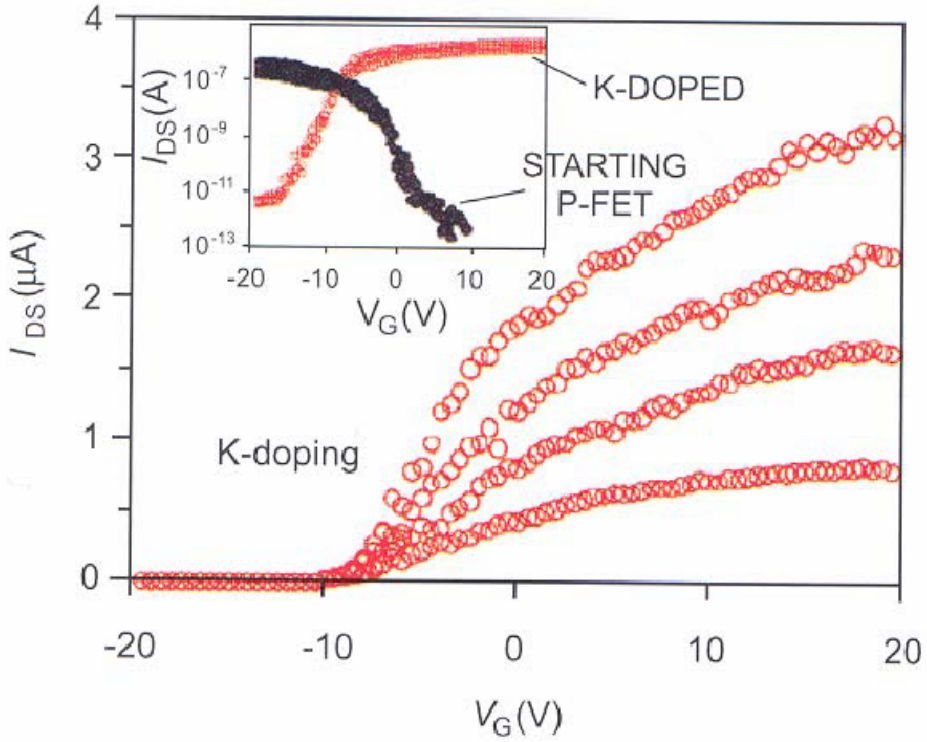
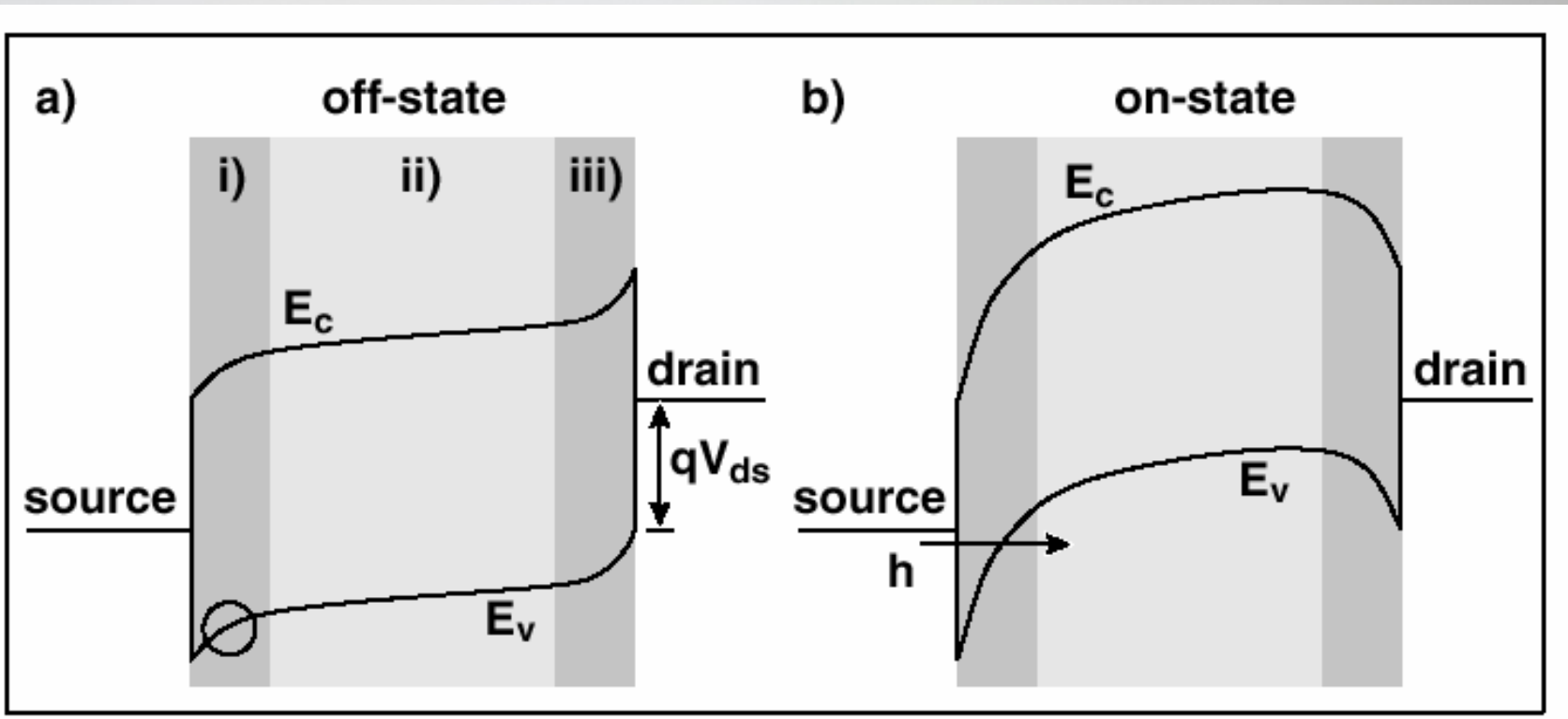


Figure 27: Inversion of the conductivity type of a semiconducting carbon nanotube. As displayed by the insert the starting device was a p-type CNT-FET. After exposure to potassium vapor, the conductivity type was reversed with current flowing for positive gate voltages (after [63]).

Consistent with Schottky Barriers Transport Description?



J. Appenzeller, PRL, 2002

CNT-IV

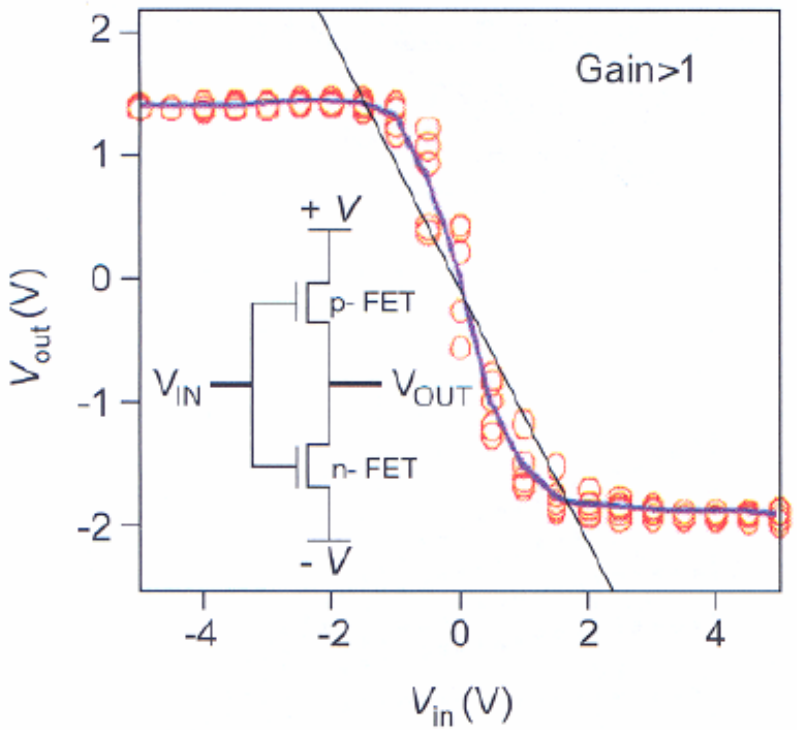


Figure 33: Input-output characteristic of a complementary CNTFET gate. The output voltage switches from logical 1 to 0 as the input voltage changes from negative to positive values. Red circles represent the data of five measurements on the same device. The blue line is the average of this measurements indicating a voltage gain > 1 (straight line).

Benchmark CNT-FET to Si-MOSFET

APPLIED PHYSICS LETTERS VOLUME 80, NUMBER 20

Vertical scaling of carbon nanotube field-effect transistors using top gate electrodes

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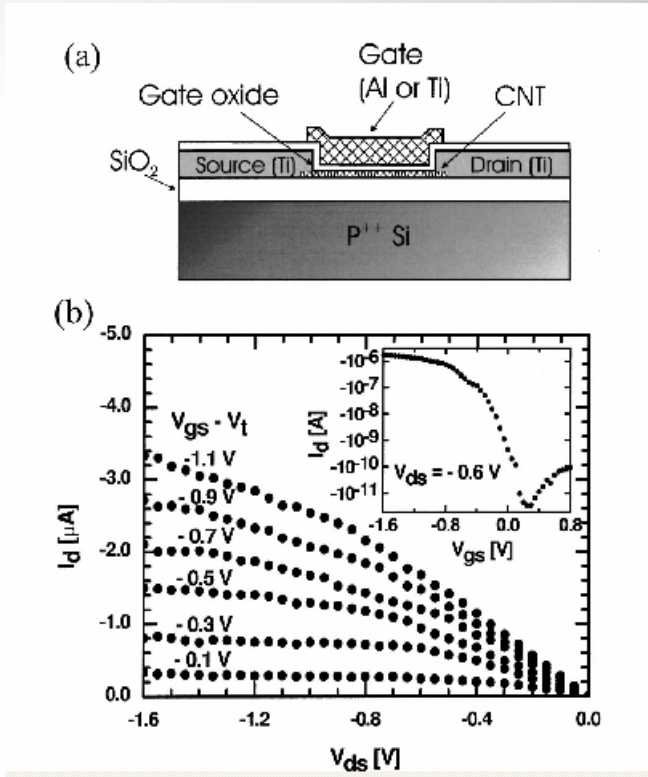
(Received 24 January 2002; accepted for publication 3 April 2002)

We have fabricated single-wall carbon nanotube field-effect transistors (CNFETs) in a conventional metal–oxide–semiconductor field-effect transistor (MOSFET) structure, with gate electrodes above the conduction channel separated from the channel by a thin dielectric. These top gate devices exhibit excellent electrical characteristics, including steep subthreshold slope and high transconductance, at gate voltages close to 1 V—a significant improvement relative to previously reported CNFETs which used the substrate as a gate and a thicker gate dielectric. Our measured device performance also compares very well to state-of-the-art silicon devices. These results are observed for both *p*- and *n*-type devices, and they suggest that CNFETs may be competitive with Si MOSFETs for future nanoelectronic applications.
[DOI: 10.1063/1.1480877]



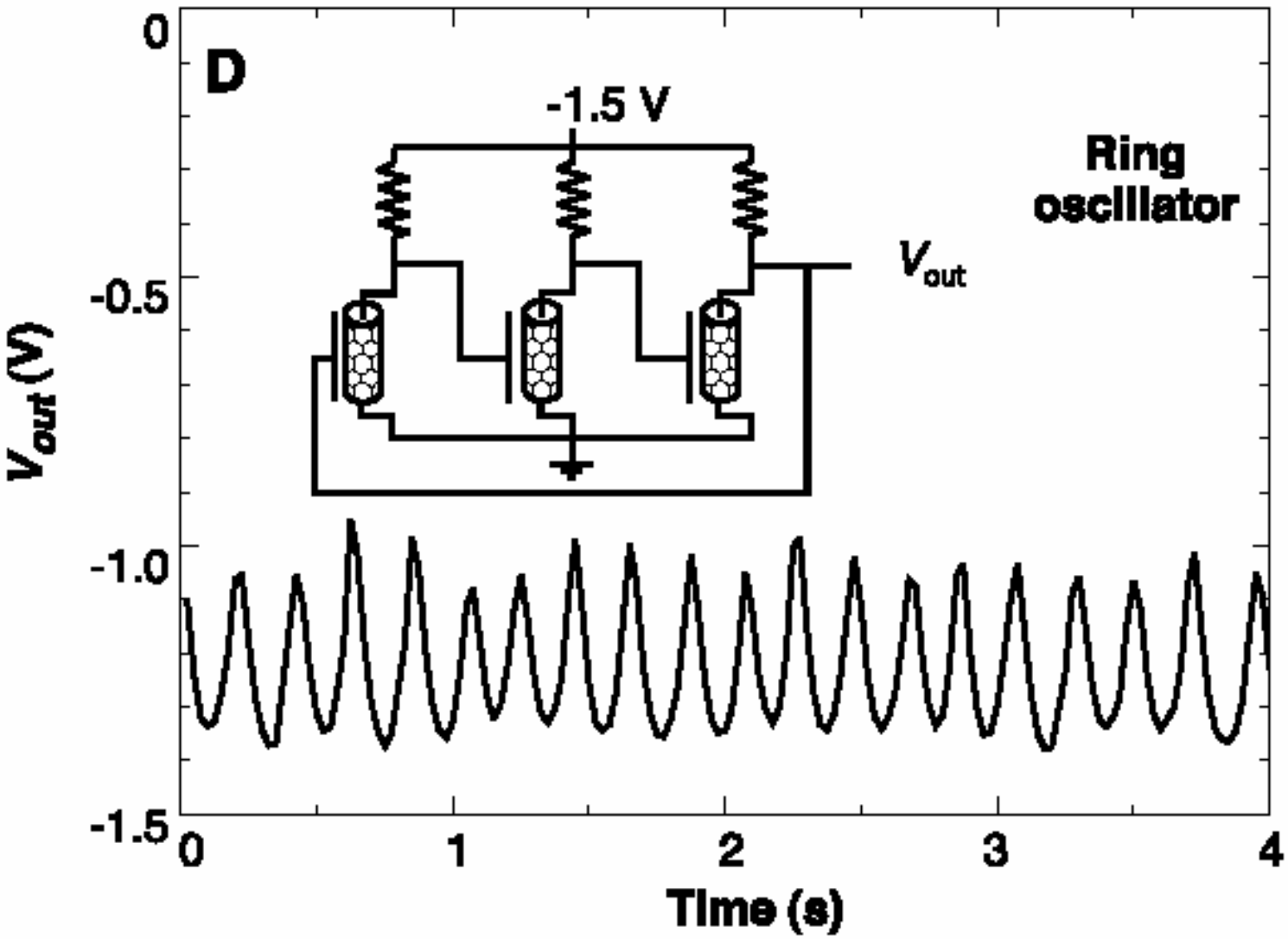
Benchmark CNT to Si MOSFET

	p-type CNFET	Ref. 59	Ref. 60
Gate length (nm)	260	15	50
Gate oxide thickness (nm)	15	1.4	1.5
V_t (V)	–0.5	~ –0.1	~ –0.2
I_{ON} (μA/μm) ($V_{ds} = V_{gs} - V_t \approx -1$ V)	2100	265	650
I_{OFF} (nA/μm)	150	< 500	9
Subthreshold slope (mV/dec)	130	~ 100	70
Transconductance (μS/μm)	2321	975	650

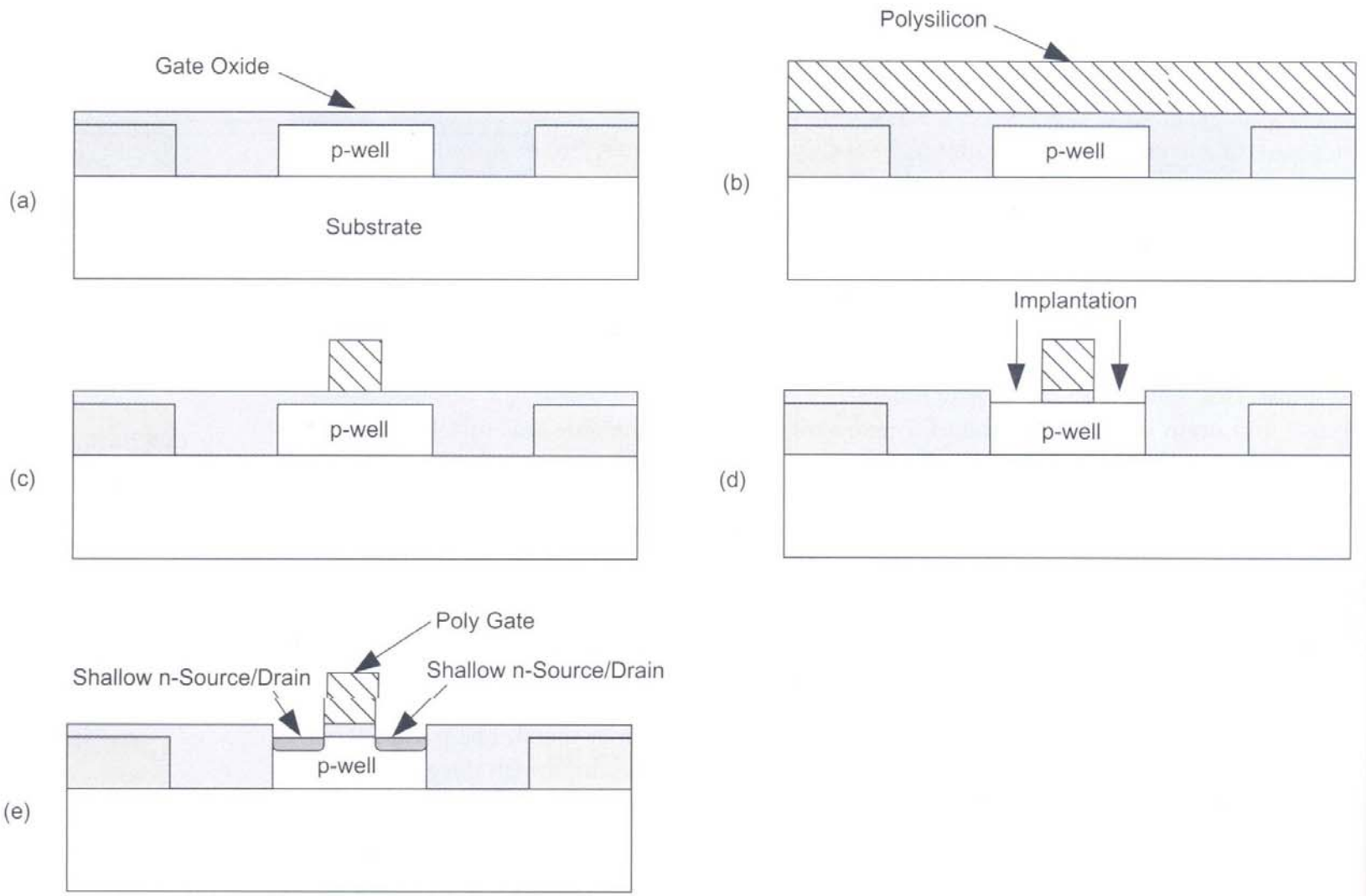
Table 1: Comparison of most important transistor data for a p-type CNTFET and two advanced Si-MOSFETs (reproduced from [65]).

(59) AMD IEDM 2001, (60) Intel 2001

Ring Oscillator: Benchmark?

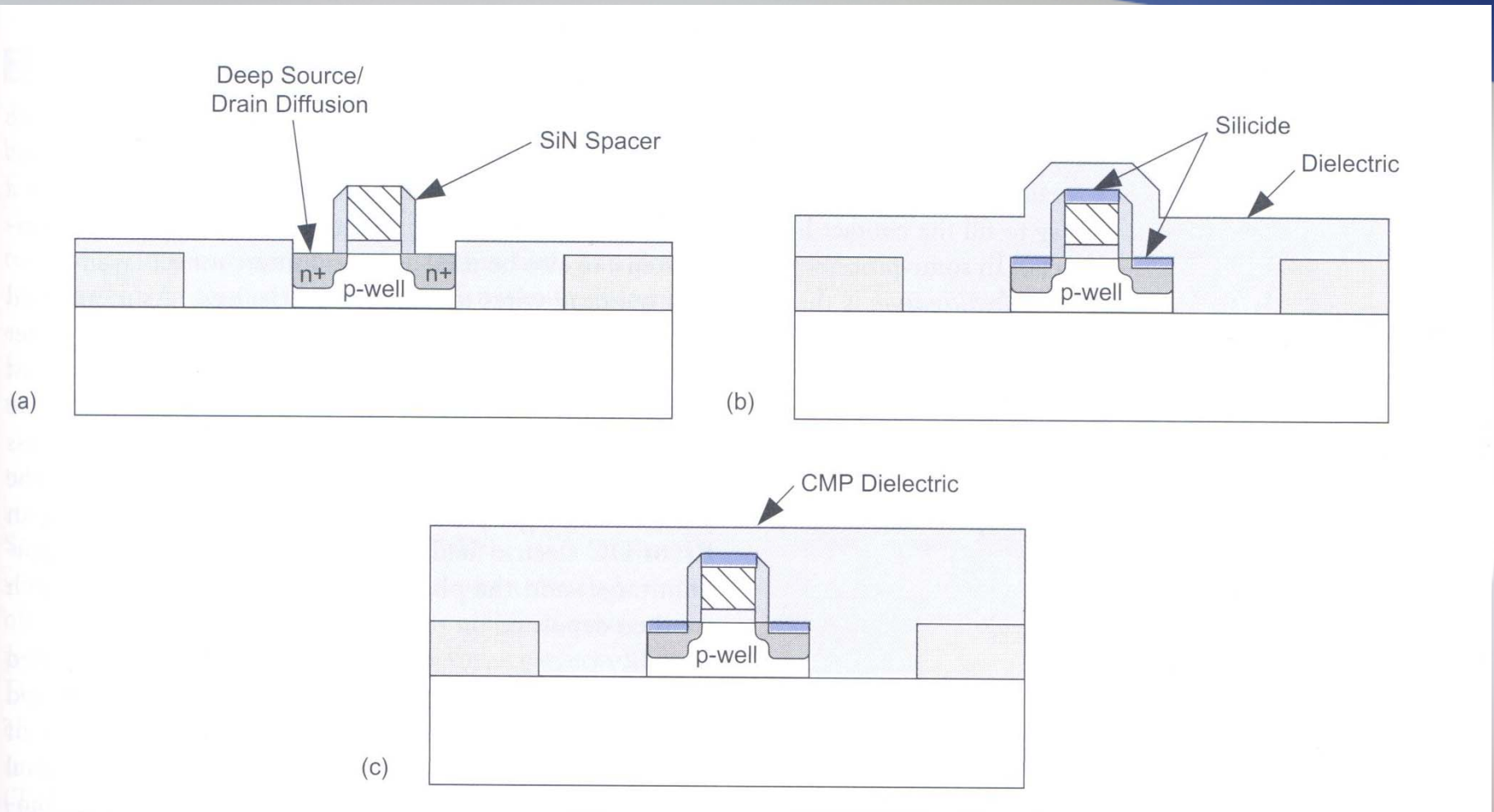


Compare CNT to Si MOSFET



Source: CMOS VLSI Design Weste/Harrris

Compare CNT to Si MOSFET



Source: CMOS VLSI Design Weste/Harrris

Overlap Capacitance

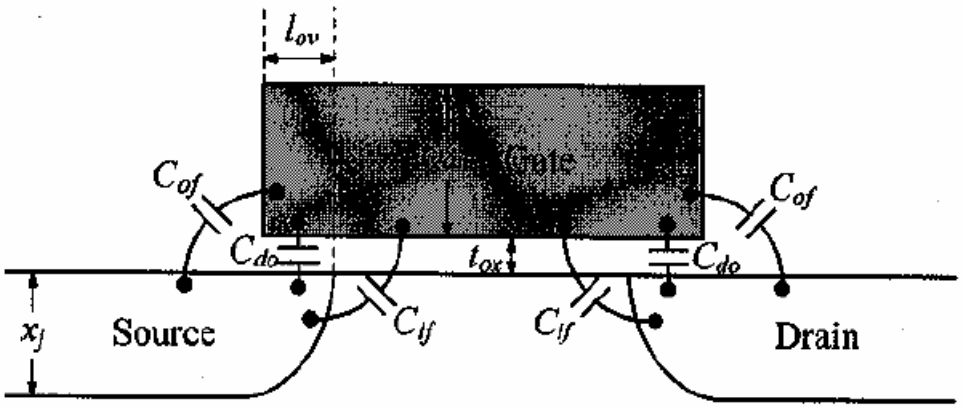


FIGURE 5.17. Schematic diagram showing the three components of the gate-to-diffusion overlap capacitance.

Taur, Ning, Modern VLSI Devices

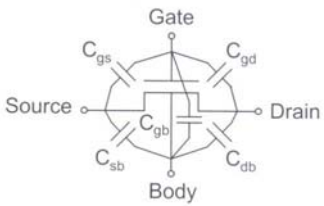


FIG 2.14 Capacitances of an MOS transistor

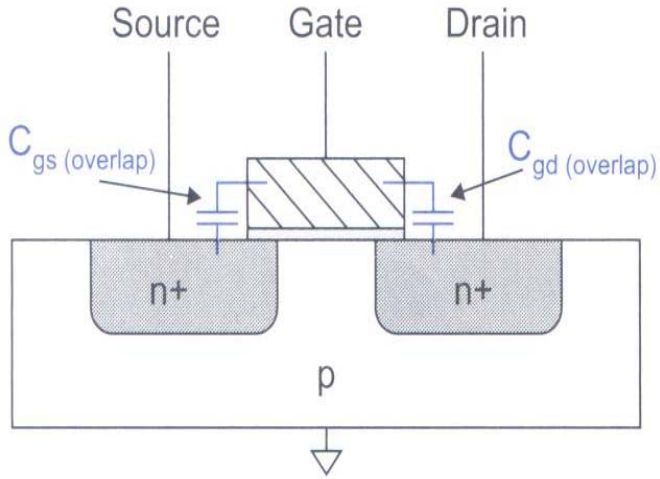
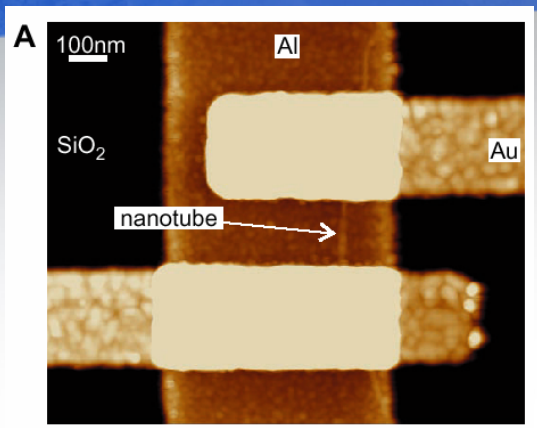


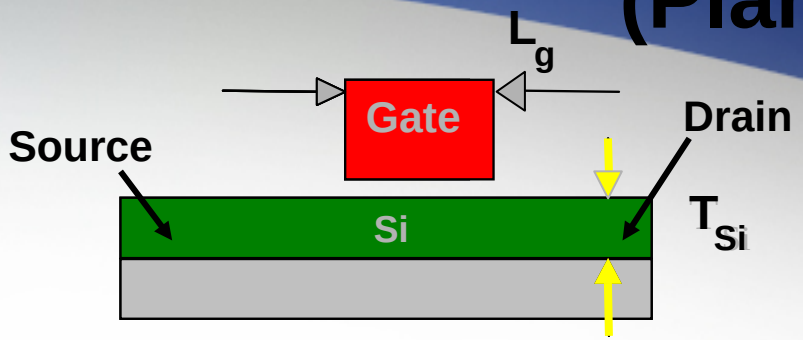
FIG 2.10 Overlap capacitance

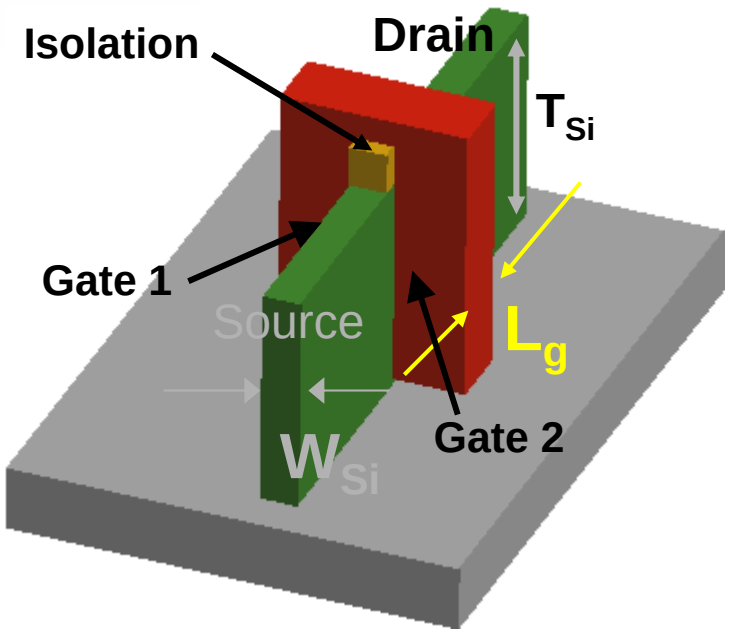
Source: CMOS VLSI Design Weste/Harrris

Miller Capacitance Difference

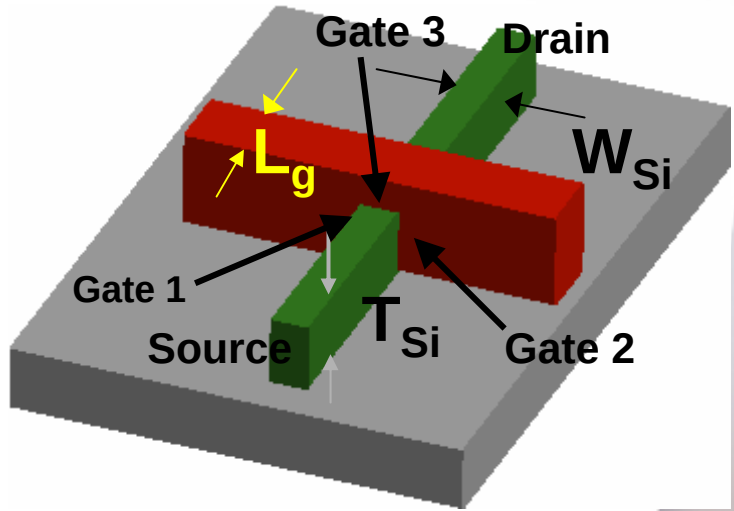


(Planar)





Double-gate (e.g. FINFET)

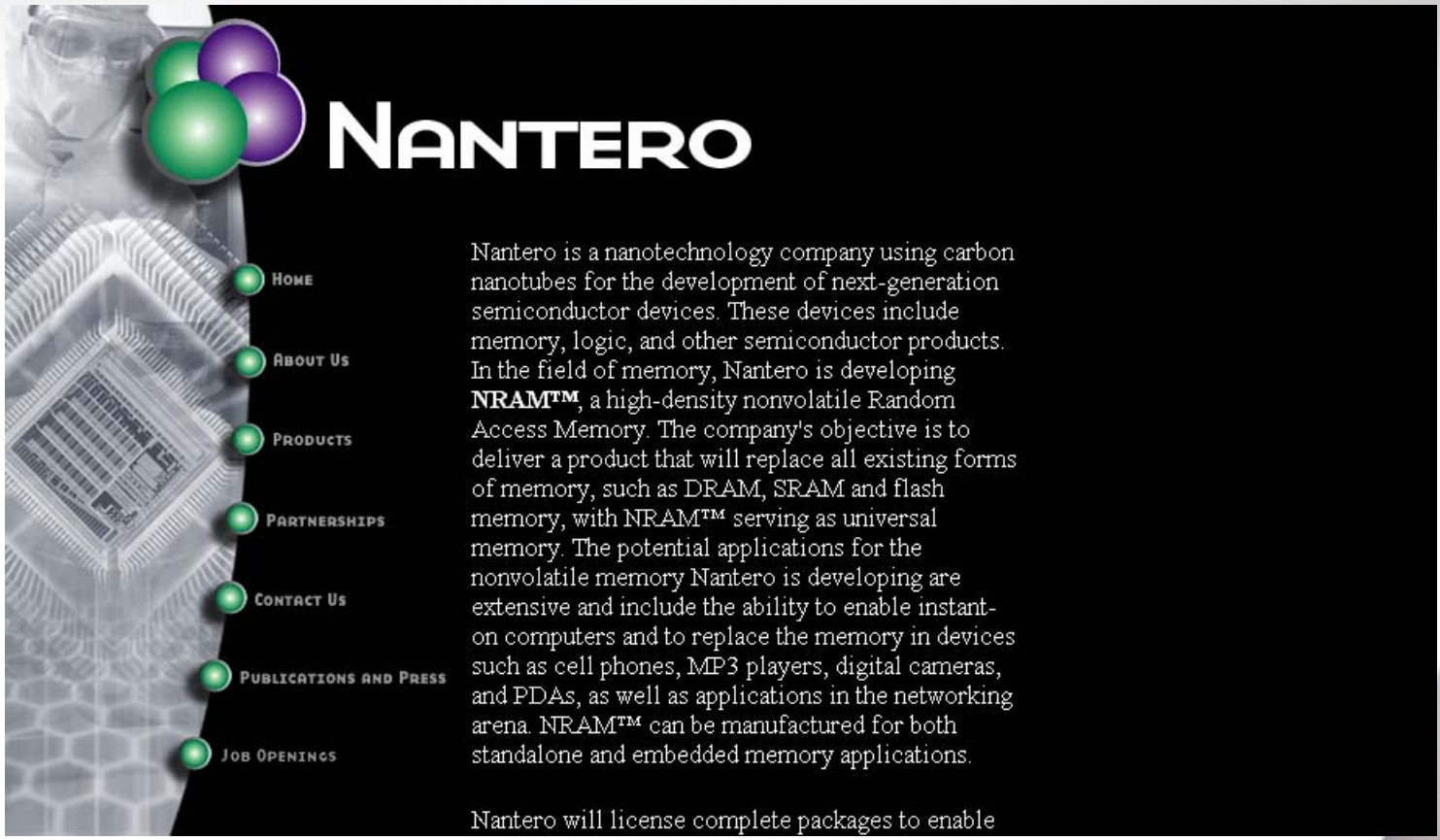


Tri-gate

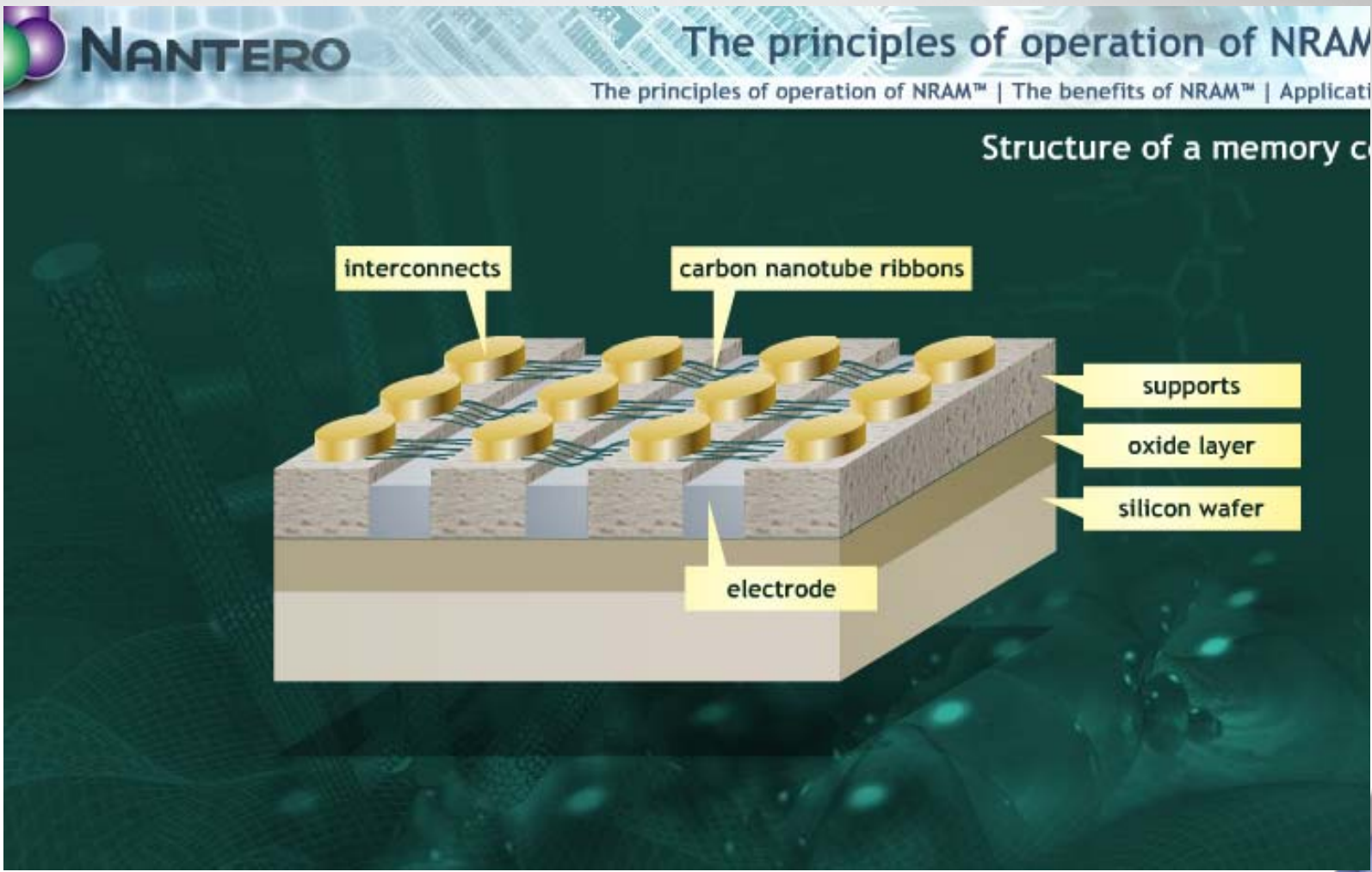
Source: Intel

Next Time: CNT as Memory Applications

- 1st semiconductor applications



Operation


NANTERO
The principles of operation of NRAM
The principles of operation of NRAM™ | The benefits of NRAM™ | Applicati
Structure of a memory c
interconnects
carbon nanotube ribbons
supports
oxide layer
silicon wafer
electrode