FIELD EFFECT TRANSISTORS (FET's)

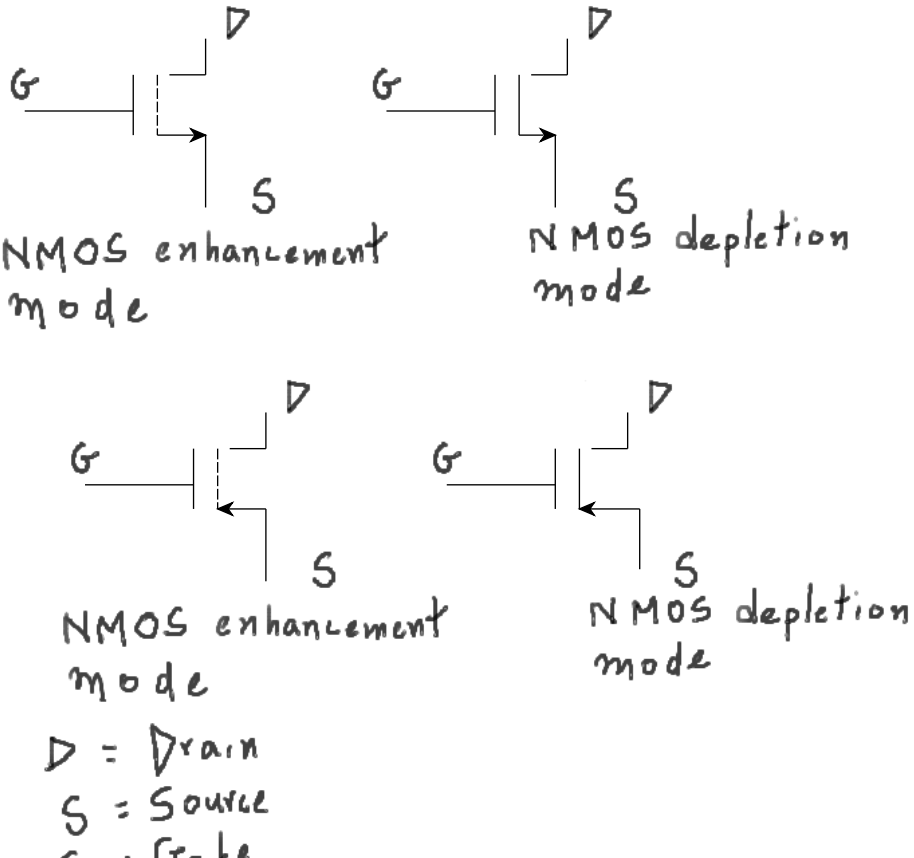
1. Metal-Oxide FETs (MOSFET's)

most successful transistors, (NMOS, PMOS)

Applications: high density VLSI chips
microprocessors
memories

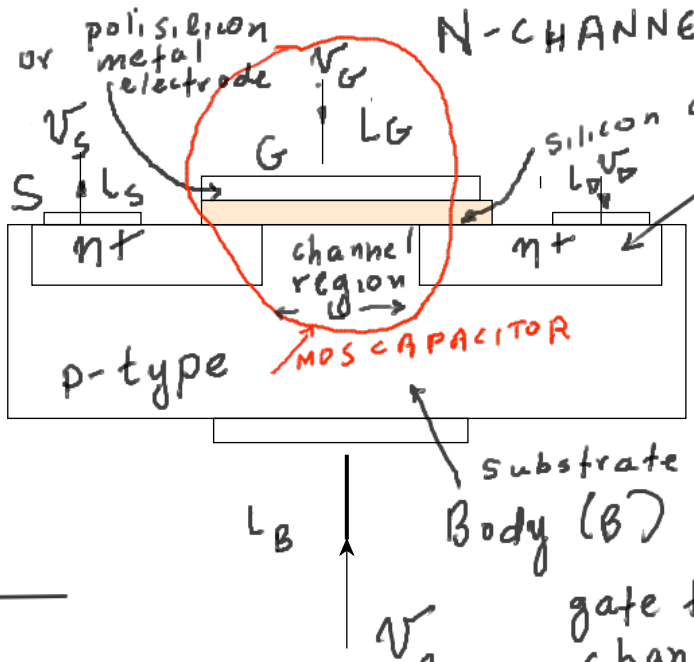
p-channel MOS (PMOS) → first devices for fabrication of LSI

n-channel MOS (NMOS) → greater performance

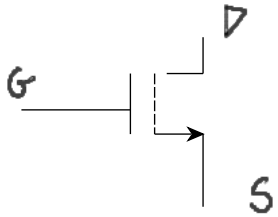


D = Drain
S = Source
G = Gate

2. JFETs: based on pn junction structure



gate terminal insulated from the channel $\Rightarrow$ $L_G = 0$, $L_B = 0$ $\Rightarrow L_s = L_d$



Important terminal voltages

$$V_{GS} = V_G - V_S$$
$$V_{DS} = V_D - V_S$$
$$V_{SB} = V_S - V_B$$

} All ≥ 0 for NMOS

Source & Drain regions form pn junction with p-type material.

pn junction reversed biased all time to keep isolation between the junctions of adjacent MOS transistors -

$\Rightarrow V_B \leq V_S, V_D$ to ensure reverse bias

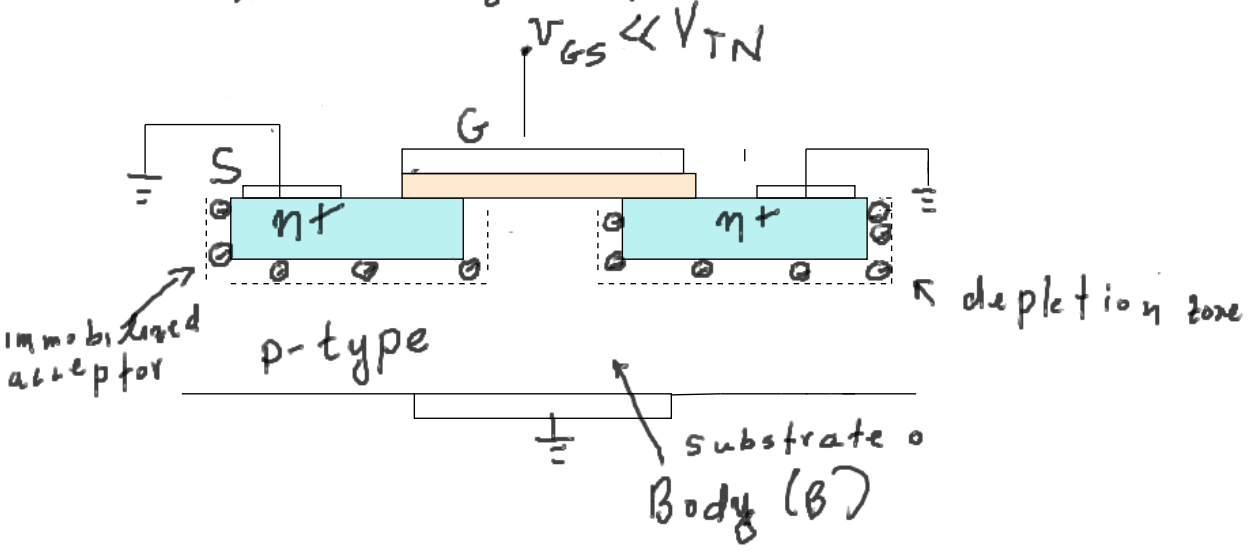
Length of channel region $< 1\mu m$

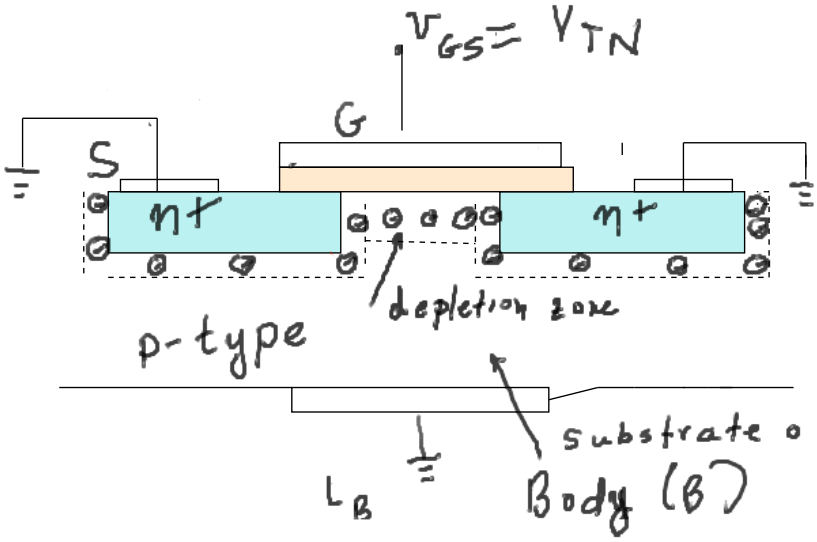
t_{ox} = oxide thickness $\leq 400\ A^\circ$

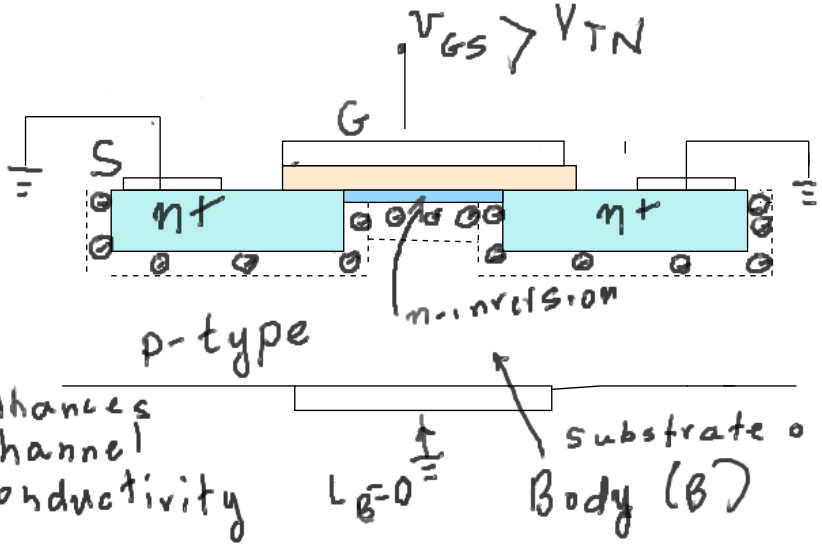
w = width of channel

I-V Behavior of the NMOS Transistor

V_{TN} = threshold voltage, the voltage where a p-type substrate is inverted to n-type inversion layer (important for MOS operation)







V_{GS} = enhances channel conductivity

TRIODE REGION CHARACTERISTICS

fixed for given technology

$$I_D = \mu_n C''_{ox} \frac{W}{L} \left(v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS} \quad (1)$$

where:

μ_n = e⁻ mobility $[cm^2/V.s]$

$C''_{ox} = \epsilon_{ox} / T_{ox}$ = oxide capacitance per unit area $[F/cm^2]$

ϵ_{ox} = oxide permitivity

T_{ox} = oxide thickness $[cm]$

W = channel width $[cm]$

Eq (1) holds under:

$$v_{GS} - V_{TN} \gg v_{DS} > 0$$

important criterion

For silicon dioxide, $\epsilon_{ox} = 3.9\epsilon_0$

where $\epsilon_{ox} = 8.854 \times 10^{-14}$ F/cm

Eq 1 can be re-written:

$$I_D = K_n \left(v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS} \quad (2)$$

where $K_n = K'_n \frac{W}{L}$

& $K'_n = \mu_n C''_{ox}$

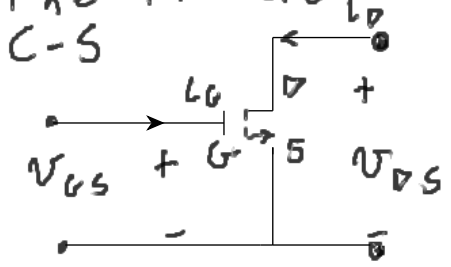
$K_n = K'_n$ = tranconductance parameters (A/V^2)

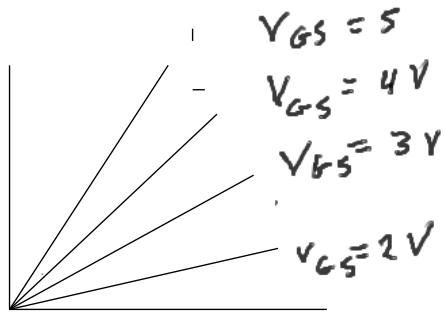
Eq (2) can be re-written as:

$$I_D = K'_n \frac{W}{L} \left(v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS} \quad (3)$$

ON RESISTANCE (in the triode zone of operation)

Based on Eq 3, the i-v characteristics in the triode region are:





Assume: $V_{TN} = 1V$

$k_n = 250 \mu A/V^2$

linear region of operation (triode mode)

for small v_{DS} voltages where

$$v_{DS}/2 \ll v_{GS} - V_{TN}$$

Eq 3 is re-written:

$$i_D \cong \underbrace{\mu_n C_{ox}}_{k_n''} \frac{W}{L} (v_{GS} - V_{TN}) v_{DS} \quad (4)$$

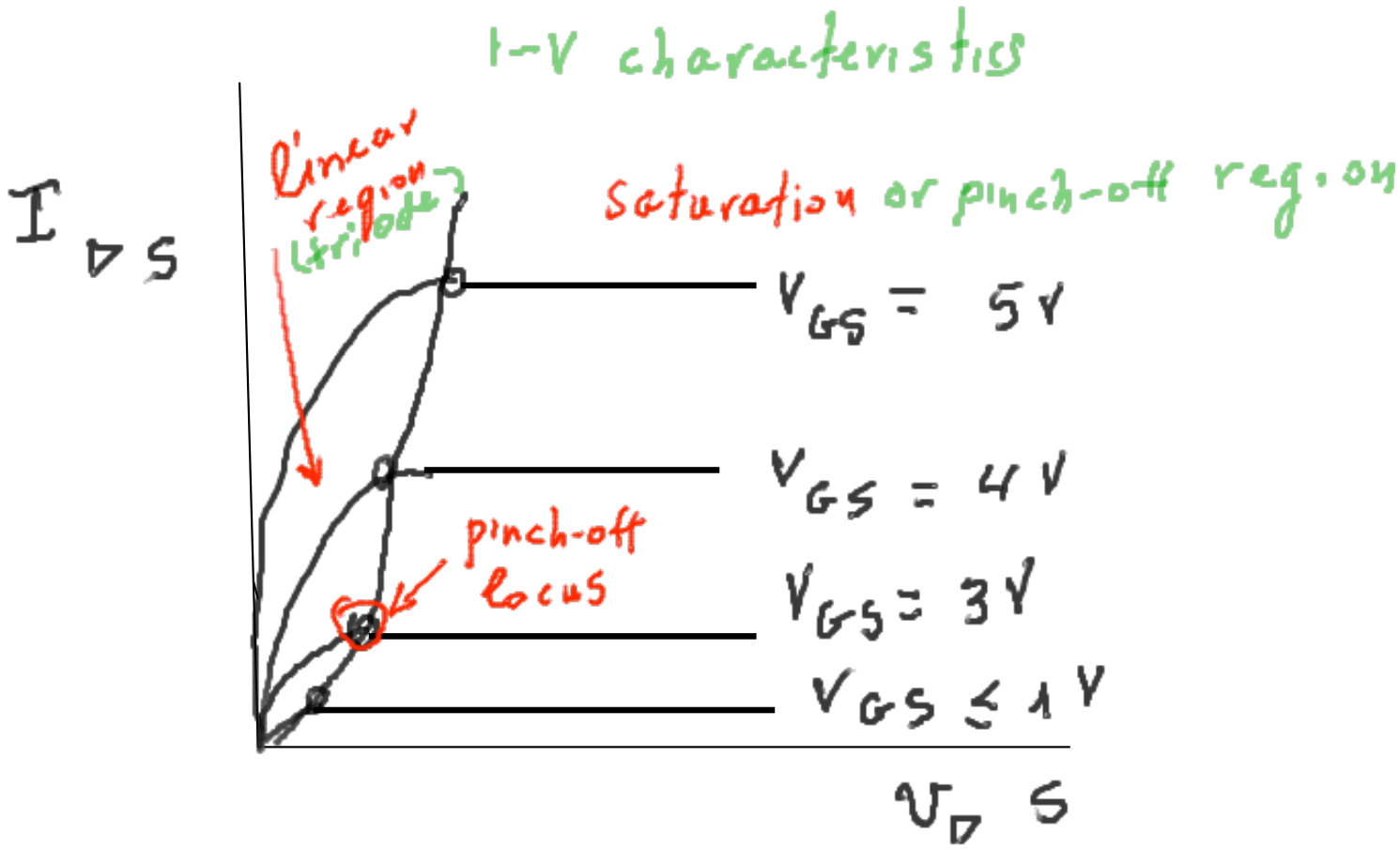
$$\Rightarrow i_D \propto v_{DS}$$

The resistance of the FET in the triode zone is:

$$R_{ON} = \left[\frac{\partial i_D}{\partial v_{DS}} \Big|_{v_{DS} \to 0} \right]^{-1}_{Q\text{-point}}$$

$$= \frac{1}{k_n' \frac{W}{L} (v_{GS} - V_{TN})} \quad (5)$$

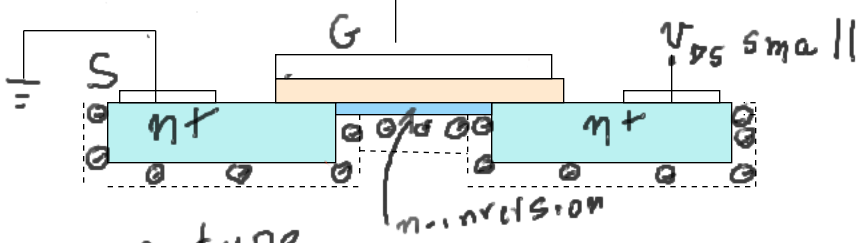
Saturation of the i-v characteristics



when V_{DS} increases above triode region limit

$\Rightarrow$ saturation

PINCH-OFF REGION
(linear region) $v_{GS} > V_{TN}$



p-type

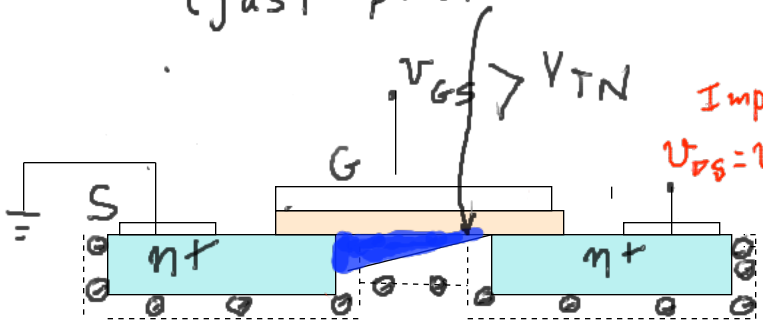
v_{GS} = enhances channel conductivity

$I_B = 0$

substrate o

Body (B)

(just pinch-off). Saturation



p-type

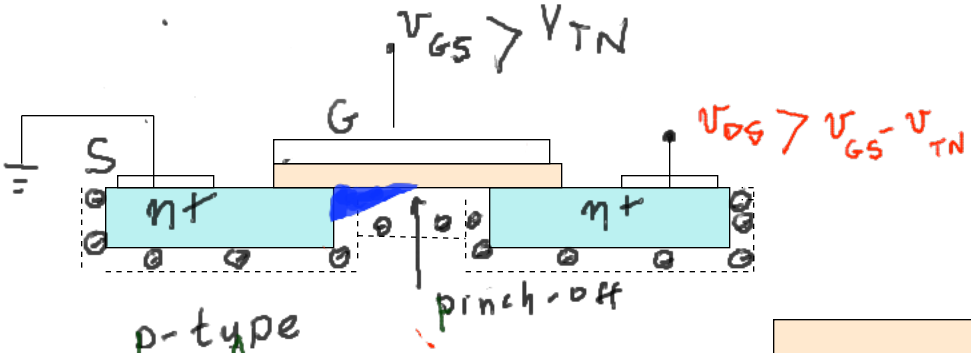
v_{GS} = enhances channel conductivity

$I_B = 0$

substrate o

Body (B)

pinch-off for $v_{DS} > v_{GS} - v_{TN}$



p-type

Therefore, pinch-off occurs at $v_{DS} > v_{GS} - v_{TN}$ (6)

Substituting (6) → (3):

$$i_D = \frac{K'_n}{2}\frac{W}{L}(v_{GS}-v_{TN})^2 \qquad (7)$$

for $v_{DS} \geq (v_{GS}-v_{TN}) \geq 0$

Square-law Expression for the i_D-v current for the NMOS operation in the pinch-off region.

$$v_{DSAT} = v_{GS} - v_{TN}$$

TRANSCONDUCTANCE

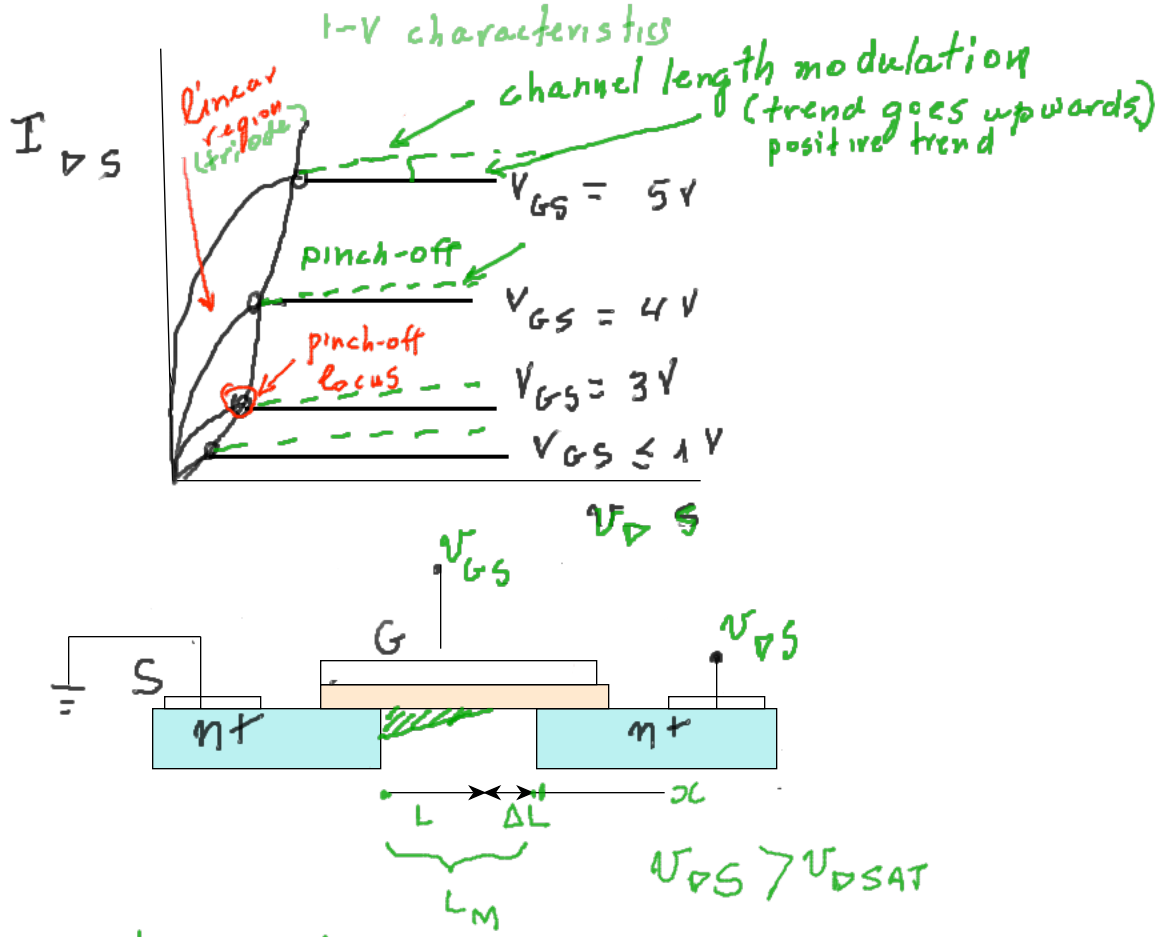
$$g_m = \left.\frac{di_D}{dv_{GS}}\right|_{Q\text{-point}} \qquad (8)$$

where i_D is given in Eq. 7.

$$g_m = K'_n \frac{W}{L}(V_{GS}-V_{TN})$$

$$= \frac{2I_D}{V_{GS}-V_{TN}} \qquad (9)$$

CHANNEL-LENGTH MODULATION



$L_M = L + \Delta L$

$L = L_M - \Delta L$

As V_{DS} increases above V_{DSAT}:

$\Delta L \rightarrow$ increases

$L \rightarrow$ decreases

Eq 7 can be re-written

$$I_D = \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_{TN})^2(1 + \lambda V_{DS}) \quad (8)$$

λ = channel-length modulation parameter

$0.001V^{-1} \leq \lambda \leq 0.10V^{-1}$

It expresses how the drain current increases for increasing V_{DS} voltage.

Transfer Characteristics

Besides the I-V characteristics (I_{DS} vs V_{DS}), we have the transfer characteristic curve. In this case, we plot I_{DS} v.s V_{GS}.

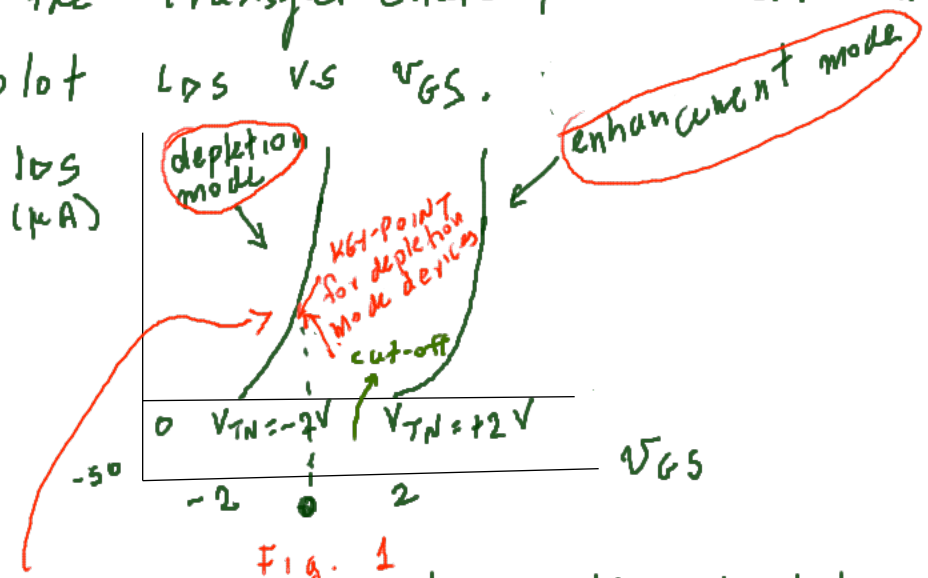
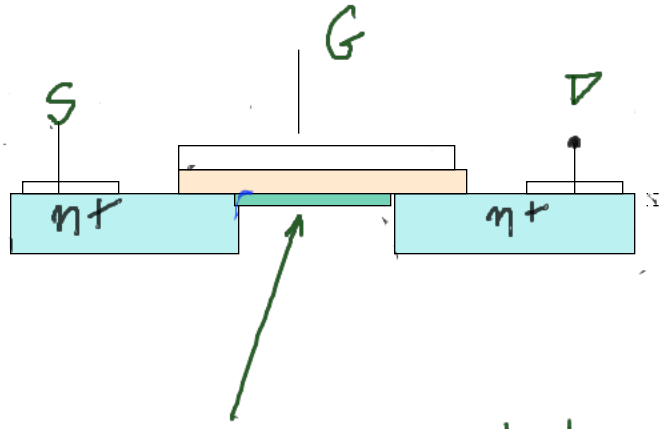


Fig. 1

non-zero drain exists in the depletion region



we use ion implantation to build the n-channel. Then, we apply a negative voltage to the gate (G) to deplete the n-channel. (still conductive) see fig 1.

Applications: MOS LOGIC CIRCUITS

PROBLEM SOLVING

ALGORITHM FOR Q-POINT

1. Assume a region of operation (mostly saturation region)

   $V_{DS} \geq V_{GS} - V_{TN}$

2. Find V_{GS} through circuit analysis

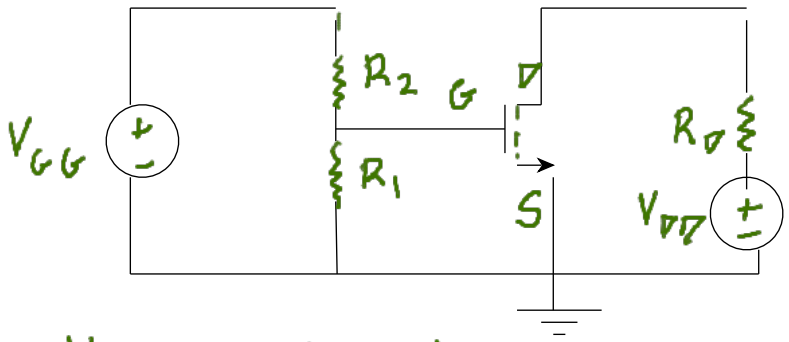
3. Use V_{GS} to calculate I_D through:

   $$I_D = \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2$$

4. Use I_D to estimate V_{DS} through circuit analysis
5. Check the validity of the operating region assumptions

Problems on MOSFETS

1) Constant Gate-Source Voltage Bias



V_{GG} = 10V = establish a fixed gate-source bias

R_1 = 30K

R_2 = 70K

R_D = 100K (its value determines I_D)

V_{DD} = 10V = supplies current through R_D.

V_{TN} = 1V

K_n = 25 μA / V^2

GOAL

Find the Q-point (I_{DS}, V_{DS})

Approach

1. Draw the Thevenin Equivalent Circuit
2. Follow the algorithm of the previous section

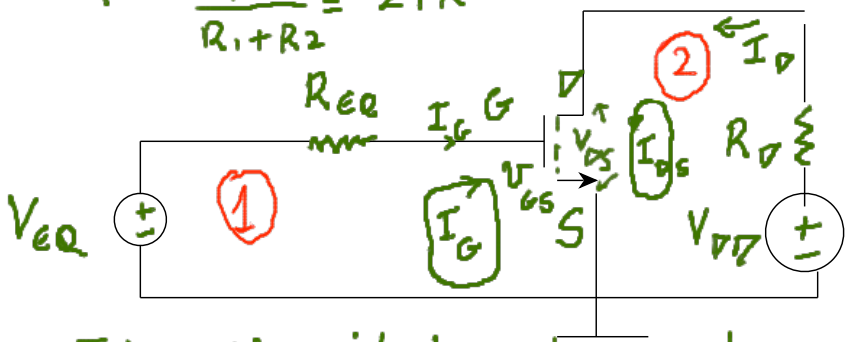
Again, make our assumptions:

The NMOS operates in the Saturation regime, so that

$V_{DS} \geq V_{GS} - V_{TN}$

$$V_{EQ} = \left(\frac{R_1}{R_1 + R_2}\right) V_{GG} = 3V$$

$$R_{EQ} = \frac{R_1 R_2}{R_1 + R_2} = 21K$$



Note: The circuit has been broken into two loops:
The circuit (1) will be provide V_{DS}.
Then, circuit (2) will be provide I_{DS}

loop 1

$$V_{EQ} = I_G R_{EQ} + V_{GS} \qquad (1)$$

But $I_G = 0 \Rightarrow$

$$V_{EQ} = V_{GS} = 3V \qquad (2)$$

plug

Again: $I_{DS} = \frac{K_n}{2}(V_{GS} - V_{TN})^2$ (assume saturation

$$= \frac{25 \times 10^{-6}}{2} \frac{\mu A}{V^2} (3-1)^2$$

$$= 50\ \mu A \qquad (3)$$

Loop 2

$$V_{DD} = I_{DS} R_D + V_{DS} \qquad (4)$$

$$\Rightarrow$$

$$V_{DS} = V_{DD} - I_{DS} R_D \qquad (5)$$

(now, plug I_{DS} from Eq 3. → (5)

$$\Rightarrow V_{DS} = 10V - (50 \times 10^{-6}) A \; (10^5 \Omega)$$

$$= 5V$$

Therefore, the Q-point is:

$$(I_{DS}, V_{DS} = 50\mu A, 5V)$$

Now, let's check if our assumption on saturation region operation, is correct or not.

$$V_{GS} - V_{TN} = 3V - 1V = 2V$$

$$\Rightarrow V_{GS} > V_{TN}$$

Also: $V_{DS} = 5V > V_{GS} - V_{TN} > 2V$ $\Rightarrow$ saturation assumption correct

PROBLEM 2

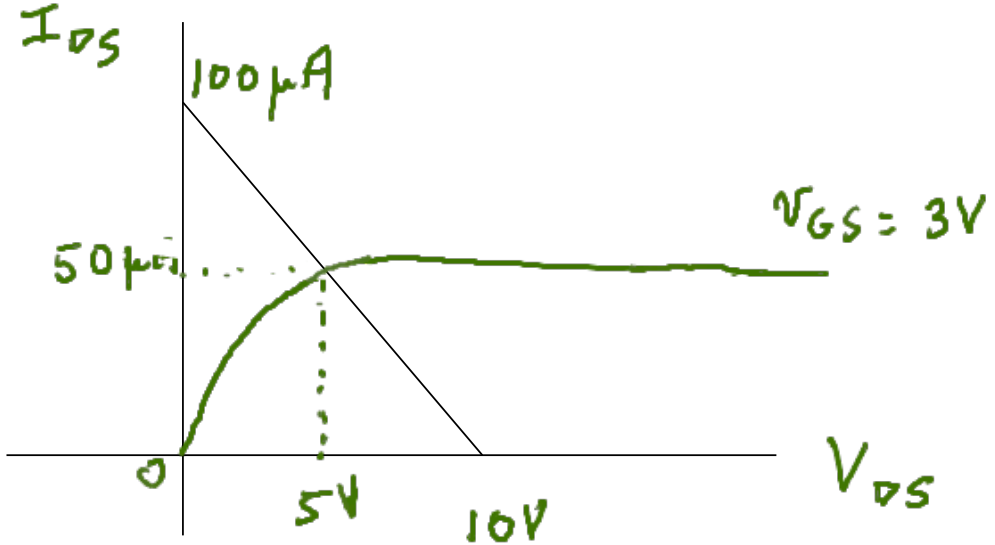
Solve Problem 1 using a load-line technique

$$V_{DD} = I_{DS} R_D + V_{DS} \qquad (4)$$

$$10V = 10^5 I_{DS} + V_{DS}$$

for $V_{DS} = 0 \Rightarrow I_{DS} = 100\mu A$

for $I_{DS} = 0 \Rightarrow V_{DS} = 10V$



Problem 3

FOUR RESISTOR BIASING: FIND THE Q-POINT

It provides enhanced stability.

The reason is that K_n, V_{TN}, λ are not known with precision.

Also, resistor and power supply tolerances, & temperature & timing drifts of the components.

Idea: Use a single voltage source, V_{DD}

$V_{DD} = 10V$

$R_1 = 100K$

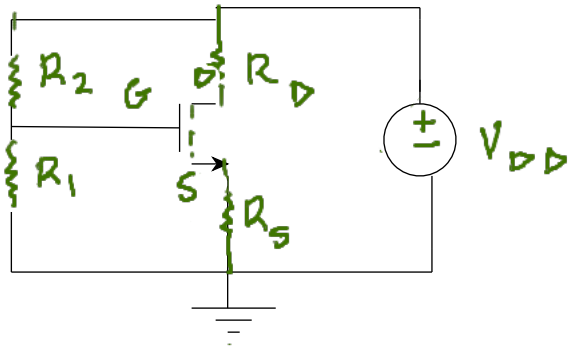
$R_2 = 150K$

$R_D = 75K$

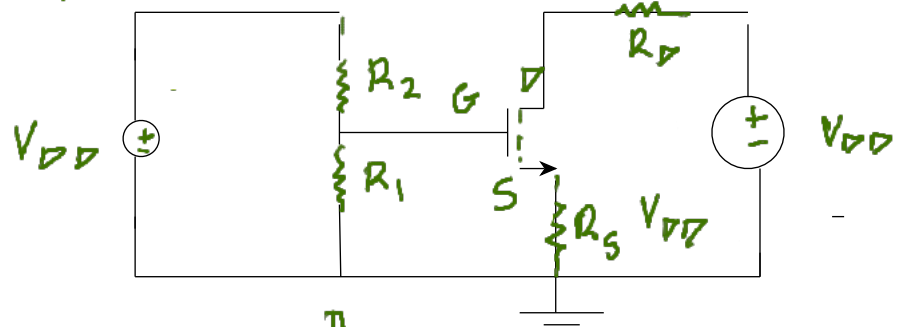
$R_S = 39K$

$V_{TN} = 1V$

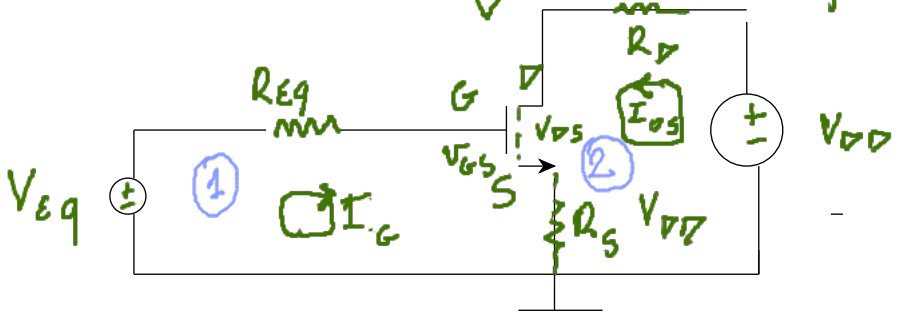
$K_n = 25\mu A/V^2$



SPLIT VOLTAGE SOURCE TO TWO EQUNALENT SOURCES V_{DD}'s



Therevin Equivalent Circuit



check assumption about saturation:

$$V_{DS} = 6.08\ V > (V_{GS} - V_{TN}) = 1.66\ V$$

$\Rightarrow$ assumption correct

$$Q\text{-point} = (34.4\ \mu A,\ 6.08\ V)$$

with $V_{GS} = 2.66\ V$

$$V_{EQ} = \left(\frac{R_1}{R_1+R_2}\right)(V_{DD})$$

$$= \frac{100K}{100K+150K}$$

$$= 4V$$

$$R_{EQ} = R_1 // R_2 = \frac{R_1 R_2}{R_1+R_2}$$

$$= \frac{100K \times 150K}{100K+150K}$$

$$= 60K$$

Loop 1

$$V_{EQ} = I_G R_{EQ} + V_{GS} + (I_G + I_D) R_S \qquad (1)$$

Loop 2

$$V_{DD} = I_D R_D + V_{DS} + (I_G + I_D) R_S \qquad (2)$$

But $I_G = 0$ (3)

$$V_{EQ} = V_{GS} + I_D R_S \qquad (4)$$

$$V_{DD} = I_D (R_D + R_S) + V_{DS} \qquad (5)$$

Again, the assume that the transistor operates in saturation region

Find V_{GS}

$$V_{EQ} = V_{GS} + I_D R_S \qquad (4)$$

It can be re-written as:

$$V_{EQ} = V_{GS} + \frac{K_n R_S}{2}(V_{GS} - V_{TN})^2 \qquad (5)$$

and

$$V_{GS}^2 + 0.05 V_{GS} - 7.21 = 0$$

$$V_{GS} = \pm 2.66 \text{ V}$$

$-2.66 \leq V_{TN} < 1\text{V} \Rightarrow$ cut-off region $\Rightarrow$ rejected

so $V_{GS} = 2.66\text{V}$ is accepted

Therefore, $I_{DS} = \frac{K_n}{2}(V_{GS} - V_{TN})^2$

$= 34.4\,\mu\text{A}$

from Circuit 2

Find V_{DS}

$$V_{DD} = 10\text{V} = I_D R_D + V_{DS} + I_D R_S + \cancel{I_G R_G}^{\,0}$$

$$= I_D(R_D + R_S) + V_{DS}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

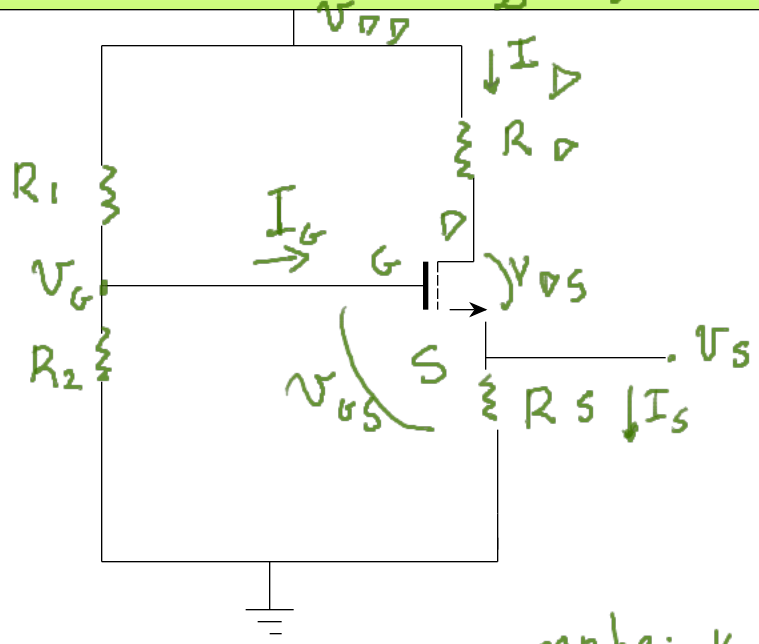
$$= 10\text{V} - (34.4\,\mu\text{A})(75\text{K} + 39\text{K})$$

$$= 6.08\text{V}$$

Problem 4

Design the dc bias of a MOSFET circuit to produce a specific drain voltage V_{DS}, under the following conditions:

Choose R_1 & R_2 such that the current in the in the bias resistors is $\frac{1}{2}$ of I_D ($I_D = 0.5\,mA$).



$V_{DD} = 10V$

$R_D = 10K$

$R_S = 2K$

$V_{TN} = 2V$

$K_n' = 80\,\mu A/V^2$

$\frac{W}{L} = 4$

note: $K_n = K_n' \frac{W}{L}$

$$I_D = \frac{K_n}{2}(V_{GS} - V_{TN})^2$$

$$= \frac{K_n'}{2}\frac{W}{L}(V_{GS} - V_{TN})^2$$

$$0.5\,mA = \frac{0.080\,mA}{2} \times 4 \times (V_{GS} - 2)^2$$

which yields

$$V_{GS} = 3.77V$$

Now we must find R_1, R_2.

$\frac{1}{10}$ 0.5 mA

$$R_1 + R_2 = \frac{10V}{0.05\,mA} = 200\,K\Omega$$

Now, lets calculate V_{GS}

$$V_{GS} = V_G - V_S$$

$$= \left(\frac{R_2}{R_1+R_2}\right) \underbrace{10V}_{V_{DD}} - I_D R_S$$

$$\Rightarrow$$

$$3.77\ V = \left(\frac{R_2}{200K}\right)(10V) - (0.5mA)\ (2K)$$

So $R_2 = 95.4\ K$

$$R_1 = \underbrace{200K}_{R_1+R_2} - 95.4\ K = 104.6\ K$$

Now, let's find V_{DS}:

$$V_{DD} = I_D R_D + V_{DS} + R_S I_D$$

$$\Rightarrow V_{DS} = V_{DD} - I_D R_D - R_S I_D$$

$$= 10V - \underbrace{5V}_{0.5mA \times 5K} - 1V$$

$$= 4V$$

Verification:

$$V_{DS} > V_{GS} - V_{TN}$$

$$4\ V > 3.77 - 2 = 1.77\ V$$

$\Rightarrow$ saturation regime

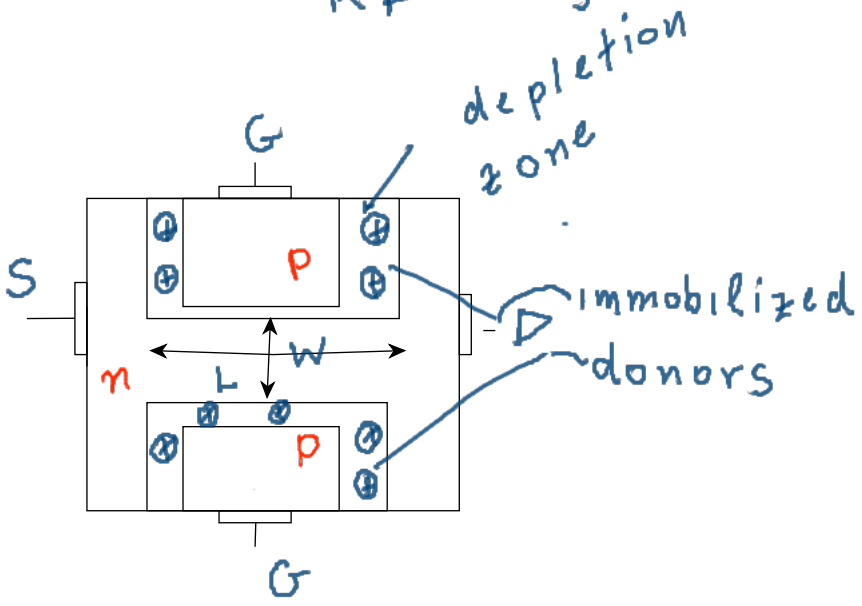
JFET'S (Junction Field-Effect Transistor)

No need for insulating oxide.

It utilizes pn-junctions

Applications: integrated, discrete } circuit design

Analog, RF } Applications



No applied bias:
resistive channel between Source & Drain

Application of a reverse bias:
Depletion zone increases (channel resistance increases)
$\Rightarrow$ $I_G \simeq 0$ = saturation current

Principles of Operation

Change the resistance of the channel region by changing the physical width of the channel through modulation of the depletion zone.

When operated in the linear zone, JFET is a voltage controlled resistor.

$$R_{CH} = \frac{\rho}{t}\frac{L}{W}$$

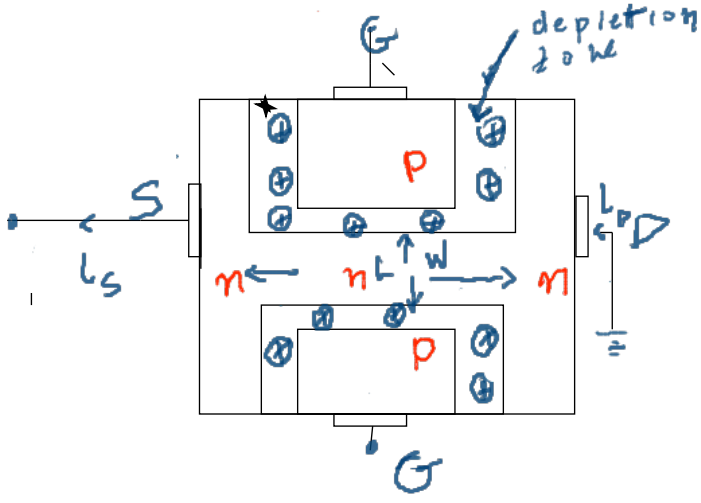
where ρ = resistivity of channel (Ω-cm)

L = channel length

W = channed width between the pn junction depletion regions

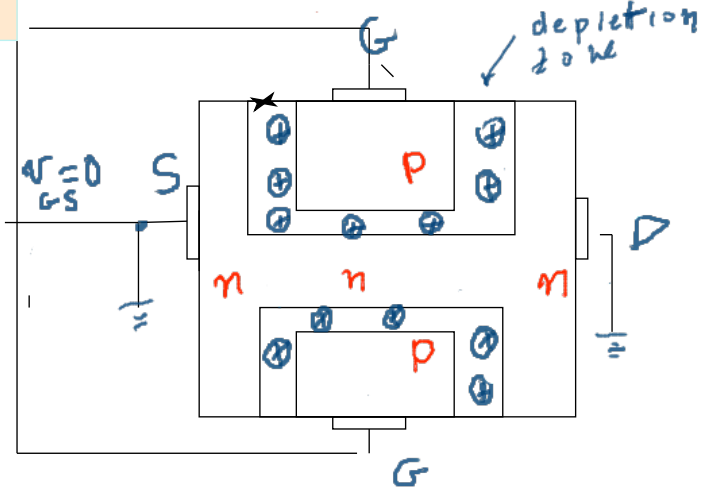
t = depth of channel into the paper.

in general, $I_{DS} = \frac{V_{DS}}{R_{ch}}$

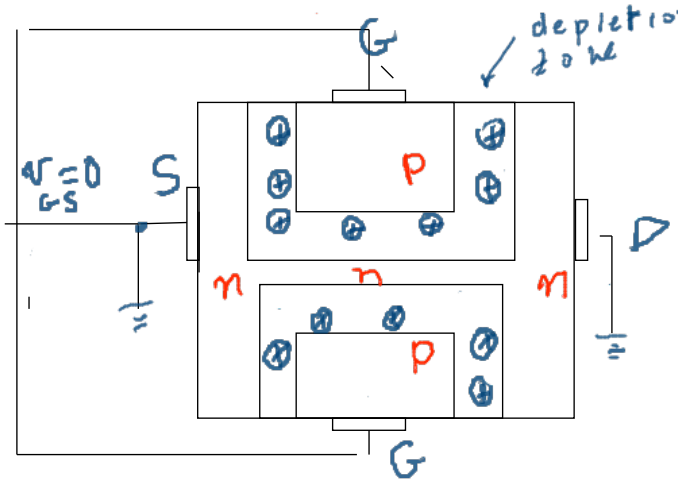


JFET with Bias Applied

$V_{GS} = 0$

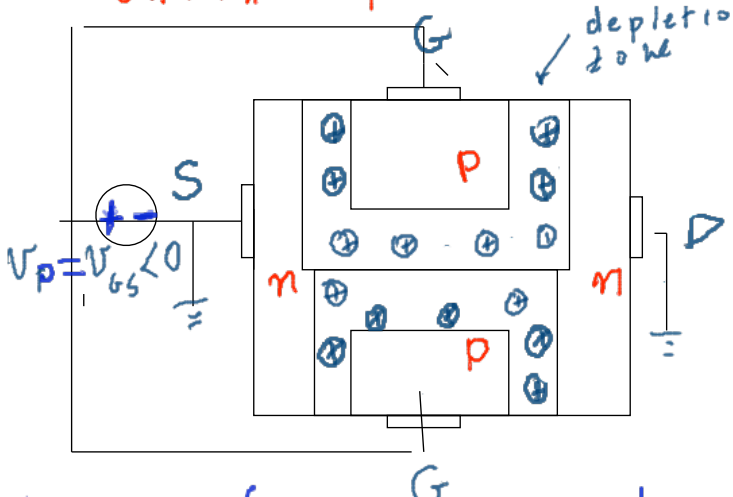


$V_p < V_{GS} < 0$



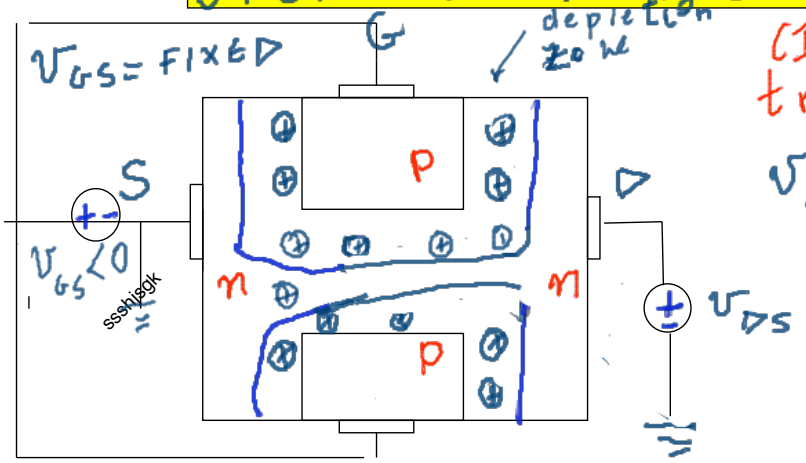
$V_{GS} = V_p < 0$ (more negative values of V_{GS})

channel pinch-off



$R \to \infty$ (conductive channel completely dissapears)

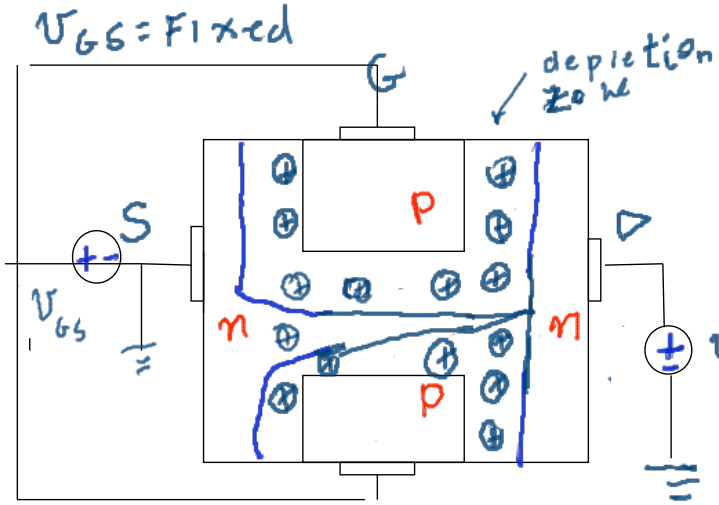
JFET with DRAIN-SOURCE BIAS



(I_D depends from v_{DS})
triode zone of operation
v_{DS} = small

v_{DS} increasing

saturation

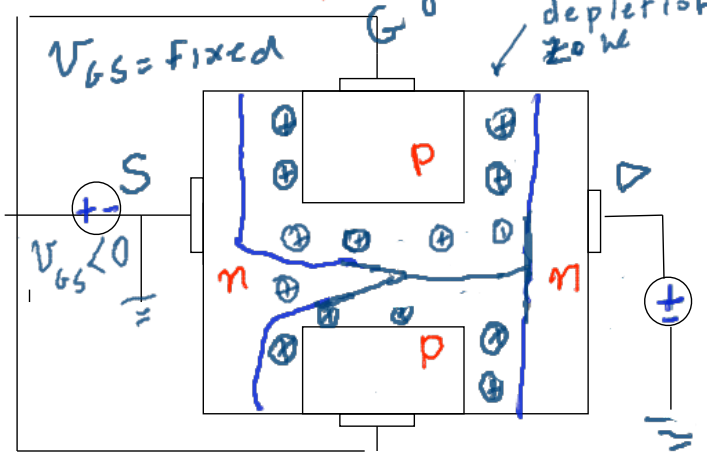


$v_{GS} - v_{DSP} = V_P$

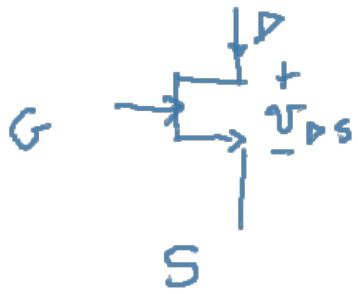
$v_{DSP} = V_P - v_{GS}$

v_{DSP} = voltage required to pinch-off the channel

channel-length modulation



channel length modulation



n-channel

$i_G \simeq 0$ for $v_{GS} \leq 0$ (this hold for any reason)

cut off region

$i_{DS} = 0$ for $v_{GS} \leq v_p$ $(v_p < 0)$

Linear Region

$$i_{DS} = \frac{2I_{DSS}}{V_p^2}\left(v_{GS} - V_p - \frac{v_{DS}}{2}\right)v_{DS}$$

for $v_{GS} - v_p \geq v_{DS} \geq 0$

Saturation Region

$$i_{DS} = i_{DSS}\left(1 - \frac{v_{GS}}{V_p}\right)^2\left(1 + \lambda v_{DS}\right)$$

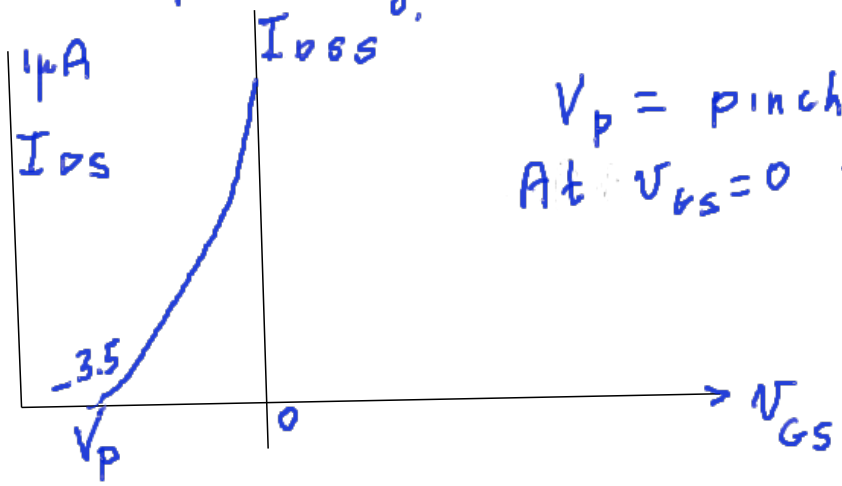
for $v_{DS} \geq v_{GS} - v_p \geq 0$

where:

$$I_{DSS} = \frac{K_n}{2} V_p^2$$

By refering to the saturation region (Pinch-off)

transfer characterics for JFET operating in Pinch-off



V_p = pinch-off voltage

At $V_{GS}=0$ $I_{DSS}=1\mu A$

$I_{DSS}=1\mu A$ (max current, under normal operating conditions, because gate diode reverse bias for $V_{GS} \leq 0$.

I-V characteristics