Integrated Matrix Extension (IME)

Task Group Meeting

Guido Araujo
Jose Moreira

07/15/24

Agenda

- Update on working groups and TG schedule

- Revisiting options

- [Abel] Updates on Option D

- [Jose] Updates on Option C*

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Working groups

Group	Coordinator	Members
Option A and A*	Marc Casas	Huayue Liang, Erich Focht
~~Option B~~		
Option C and C*	Jose Moreira	
Option D	Abel Bernabeu	
Option E	Jim (CN.Ke)	Yi-Xuan.Huang
Workloads and benchmarking	Guido Araujo	

Update on TG schedule (Previous)

Task	Del.	Task Description	1	2	3	4	5	6	7	8	9	10	11	12
1		Architectural features												
3		a. uArch: Overall analysis	Delivery											
6		b. uArch: Memory access analysis	Delivery											
2		c. ISA: Matrix data encoding	Delayed	Delayed	Delayed	Delayed								
4		d. ISA: Register usage and mapping	Discuss	Discuss	Delayed	Delayed								
6		e. ISA: Data type and geometry configuration		Discuss	Discuss	Delayed								
5		f. ISA: Binary compatibility			Not touched	Delayed								
6		g. ISA: Computation operations definition			Not touched	Not touched	Delivery							
7		h. ISA: Instruction encoding					Not touched	Delivery						
8		Workloads and bechmarking												
9		a. ML: T-Head profiling and ConvBench	Delivery											
10		b. HPC: Polybench	Discuss	Discuss	Delivery									
11		c. ML: POWER10 MMA transfers		Delivery										
12		d. Workload analysis		Discuss	Discuss	Discuss	Discuss	Discuss	Delivery					
13		Quantitative analysis												
14		a. QEMU modelling						Not touched	Not touched	Delivery				
15		b. Performace evaluation							Not touched	Not touched	Delivery			
16		Definition of the final architecture												
17		a. RVM ISA v0							Not touched	Not touched	Delivery			
18		b. RVM ISA v1								Not touched	Not touched	Delivery		
19		RVM Spec writing									Not touched	Not touched	Not touched	Delivery

Legend:
- Green — Delivery date
- Yellow — Still discussing
- Blue — Not touched
- N — Past meeting
- Red — Delayed

Update on TG schedule (Current)

Task	Del.	Task Description	Meetings											
			1	**2**	**3**	**4**	**5**	**6**	**7**	8	9	10	11	12
1		Architectural features												
2		a. uArch: Overall analysis	✓											
3		b. uArch: Memory access analysis	✓											
4		c. ISA: Matrix data encoding							⚠					
5		d. ISA: Register usage and mapping												
6		e. ISA: Data type and geometry configuration												
7		f. ISA: Binary compatibility												
8		g. ISA: Computation operations definition												
9		h. ISA: Instruction encoding												
10		Workloads and bechmarking												
11		a. ML: T-Head profiling and ConvBench	✓											
12		b. HPC: Polybench			✓									
13		c. ML: POWER10 MMA transfers		✓										
14		d. Workload analysis												
15		Quantitative analysis												
16		a. QEMU modelling												
17		b. Performace evaluation												
18		Definition of the final architecture												
19		a. RVM ISA v0												
20		b. RVM ISA v1												
21		RVM Spec writing												

Legend:
- 🟩 Delivery date
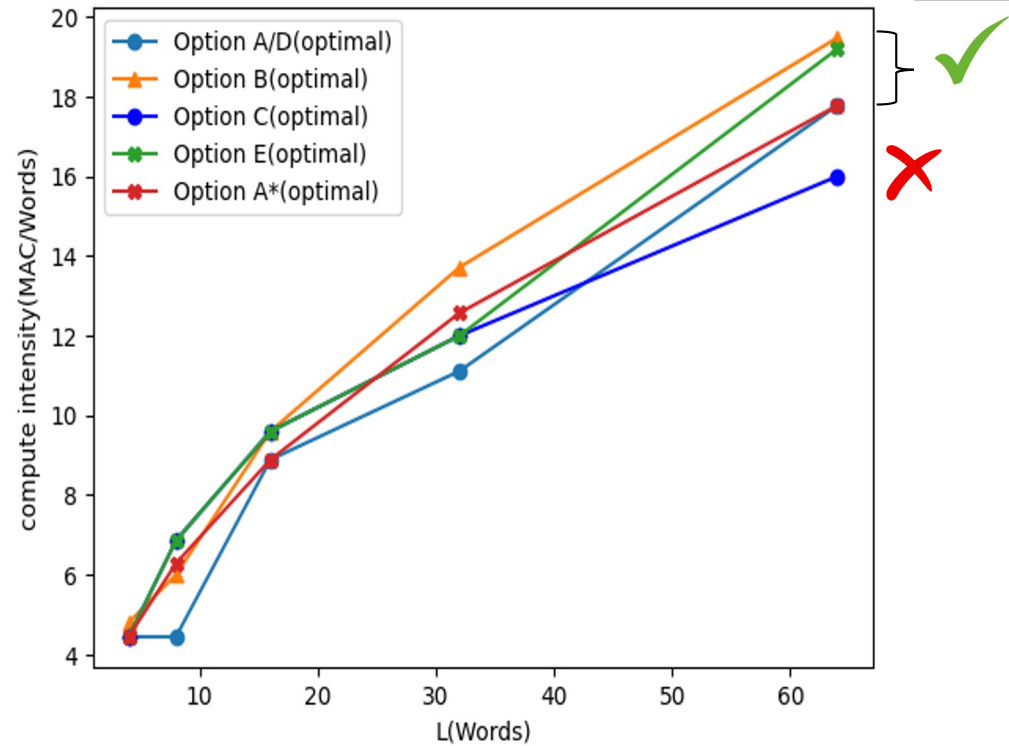- 🟨 Still discussing
- 🟦 Not touched
- N Past meeting
- 🟥 Delayed

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- Update on working groups and TG schedule

- Revisiting options

- [Abel] Updates on Option D
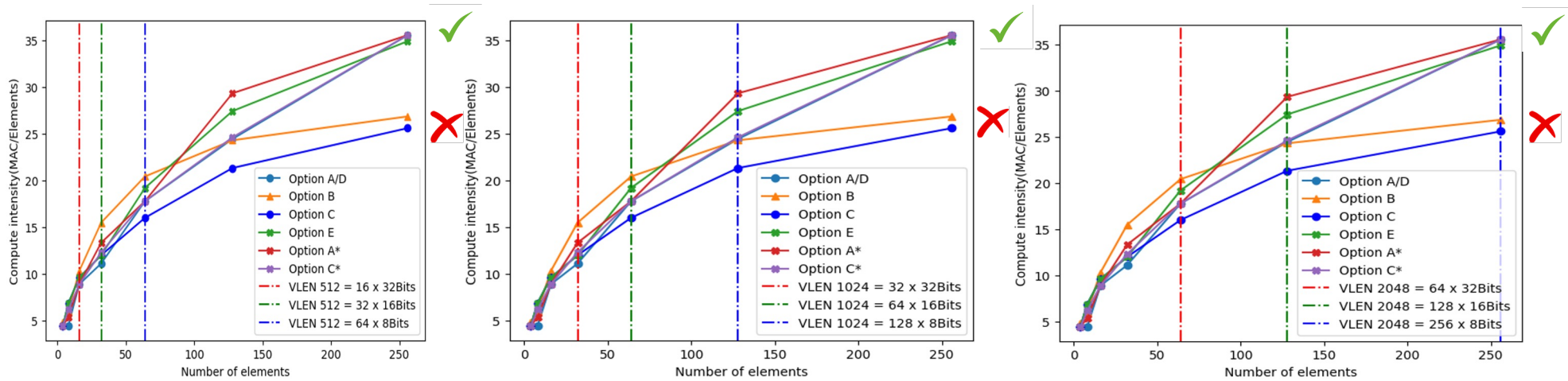
- [Jose] Updates on Option C*

CI Analysis

✔ All but C

✘ Options C

CI Analysis considering datatypes

VLEN = 512   VLEN = 1024   VLEN = 2048

✓ Options A*, C*, D and E

✗ Options B and C

Conclusions

- Rule out: A, B and C ✗

- Candidates: A*, C*, D and E ✓

- Waiting for selected chairs….

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