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CENG 303: LINEAR ELECTRONIC CIRCUITS

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BY:

NANA Dr. K. DIAWUO

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CHAPTER ONE: INTEGRATED CIRCUIT FABRICATION PROCESSES

1.1 Introduction

An integrated circuit consists of a single-crystal chip of silicon, typically 50 by 50 mils in cross section, containing both active and passive elements and their interconnections. Such circuits are produced by the same processes used to fabricate individual transistors and diodes. These processes include epitaxial growth, masked impurity diffusion, oxide growth, and oxide etching, using photolithography for pattern definition. A method of batch processing is employed which offers excellent repeatability and is adaptable to the production of large numbers of integrated circuits at low cost. In this chapter we describe the basic processes involved in fabricating an integrated circuit.

1.1.1 Wafer Preparation: Electronic - Grade Silicon: (EGS)

To obtain EGS requires a multistep process. First, metallurgical-grade silicon is produced in a submerged – electrode arc furnace. The furnace is charged with quartzite, a relatively pure form of SiO_2 and carbon in the form of coal, coke, and wood chips. The reaction is as follows:

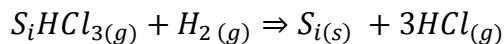


The result, the MGS is further purified since EGS requires that doping elements be in the parts per billion (ppb) range, and carbon be less than 2 parts per million (ppm). Some of the impurities found in the MGS are Al, Fe, Cr, Ti, B.

The next process step is to mechanically pulverize the silicon and react it with anhydrous hydrogen chloride to form trichlorosilane ($SiHCl_3$) according to the reaction:



EGS is prepared from purified $SiHCl_3$ in a chemical vapour deposition (CVD). The reaction is as follows:



The process that follows is the crystal growth. This involves a phase change from solid, liquid or gas phases to a crystalline phase. The process known as Czochralski growth is mostly used to grow crystals from which wafers are produced. The ingot is then prepared by shaping - surface and diameter grinding; polishing etc.

Fabrication of monolithic ICs involves a number of steps. These steps may be grouped under the planar process technology.

The planar process tech is composed of five independent processes: epitaxy, oxidation, photolithography, diffusion (ion implant) and thin-film deposition.

1.2. Integrated-Circuit (Microelectronic) Technology

The fabrication of integrated circuits is based on materials, processes, and design principles which constitute a highly developed semiconductor (planar- diffusion) technology. The basic structure of an integrated circuit is shown in Fig. 1.1. Fig 1.1b consists of four distinct layers of material. The bottom layer (1) (6 mils thick) is p-type silicon and serves as a substrate or body upon which the integrated circuit is to be built. The second layer (2) is thin (typically 5 to 25 μm) n-type material which is grown as a single-crystal extension of the substrate. All active and passive components are built within the thin n-type layer using a series of diffusion steps. These components are transistors, diodes, capacitors, and resistors, and they are made by diffusing p-type and n-type impurities. The most complicated component fabricated is the transistor, and all other elements are constructed with one or more of the processes required in making a transistor.

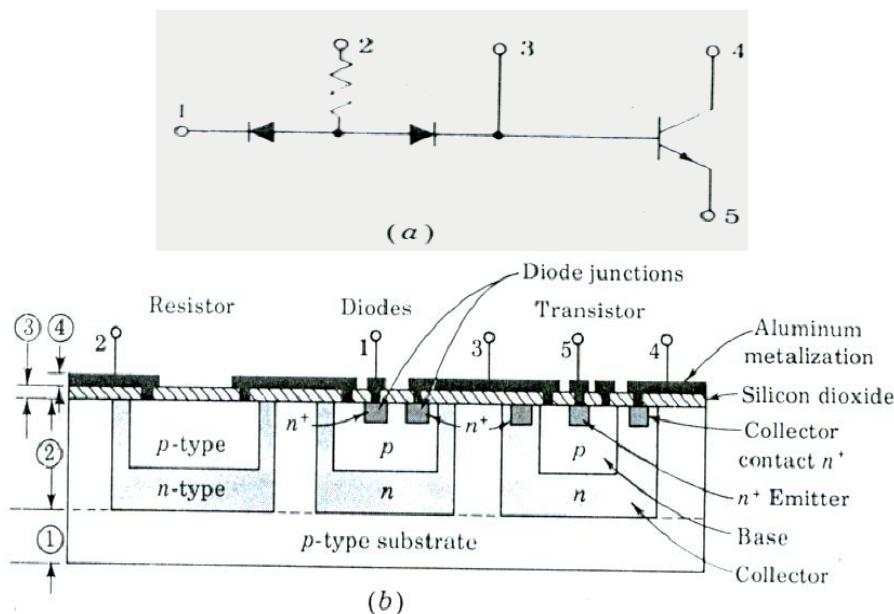


Figure 1.1 (a) A circuit containing a resistor, two diodes, and a transistor, (b) Cross-sectional view of the circuit in (a) when transformed into a monolithic form (not drawn to scale). The four layers are (1) substrate, (2) n-type crystal containing the integrated circuit, (3) silicon dioxide, and (4) aluminum metallization. (After Phillips¹)

In the fabrication of all the above elements it is necessary to distribute impurities in certain precisely defined regions within the second (n--type) layer. The selective diffusion of impurities is accomplished by using SiO_2 as a barrier which protects portions of the wafer against impurity penetration. Thus the third layer of material (3) is silicon dioxide, and it also provides protection of the semiconductor surface against

contamination. In the regions where diffusion is to take place, the SiO_2 layer is etched away, leaving the rest of the wafer protected against diffusion. **To permit selective etching, the SiO_2 layer must be subjected to a photolithographic process**. Finally, a fourth metallic (aluminum) layer (4) is added to supply the necessary interconnections between components.

We are now in a position to appreciate some of the significant advantages of microelectronic technology. Let us consider a 2 by 2 inch wafer divided into 1,600 chips of surface area 50 by 50 mils. We demonstrate in this chapter that a reasonable area under which a component (say, a transistor) is fabricated is 50 mils². Hence each chip (each integrated circuit) contains 50 separate components, and there are $50 \times 1,600 == 80,000$ components on each wafer.

If we process 20 wafers in a batch, we can manufacture 32,000 integrated circuits simultaneously, and these contain 1,600,000 components. Some of the chips will contain faults due to imperfections in the manufacturing process, but if the yield (the percentage of fault-free chips per wafer) is only 20 percent, then 6,400 good chips containing 320,000 circuit components are mass-produced in a single batch! The following advantages are offered by integrated-circuit technology as compared with discrete components interconnected by conventional techniques:

1. Low cost (due to the large quantities processed).
2. Small size.
3. High reliability. (All components are fabricated simultaneously, and there are no soldered joints.)
4. Improved performance. (Because of the low cost, more complex circuitry may be used to obtain better functional characteristics.)
5. Matched devices. Since all transistors are manufactured simultaneously by the same processes, the corresponding parameters of these devices as well as the temperature variation of their characteristics have essentially the same magnitudes (the parameters track well with temperature).

In the next sections we examine the processes required to fabricate an integrated circuit.

1.2.1 Basic Monolithic Integrated Circuits

We now examine in some detail the various techniques and processes required to obtain the circuit of Fig. 1.1a in an integrated form, as shown in Fig. 1.1b. This configuration is called a monolithic integrated circuit because it is formed on a single silicon chip. The word "monolithic" is derived from the Greek monos, meaning "single," and lithos, meaning "stone." Thus a monolithic circuit is built into a single stone, or single crystal.

In this section we describe qualitatively a complete epitaxial-diffused fabrication process for integrated circuits. In subsequent sections we examine in more detail the epitaxial, photographic, and diffusion processes involved. The circuit of Fig. 1.1 is chosen for discussion because it contains typical components: a resistor, diodes, and a transistor. These elements (and also capacitors with small

values of capacitances) are the components encountered in integrated circuits. The monolithic circuit is formed by the steps described below.

Step 1. Crystal Growth of the Substrate

A tiny crystal of silicon is attached to a rod and lowered into a crucible molten silicon to which acceptor impurities have been added. As the rod is very slowly pulled out of the melt under carefully controlled conditions, a single *p*-type crystal ingot of the order of 3 in (7.5 cm) in diameter and 20 in (50 cm) long is grown. The ingot is subsequently sliced into round wafers approximately 6 mils thick to form the substrate upon which all integrated components will be fabricated. One side of each wafer is lapped and polished to eliminate surface imperfections before proceeding with the next process.

Step 2. Epitaxial Growth

An n-type epitaxial layer, typically 5 to 25 μm thick, is grown into a p-type substrate which has a resistivity of approximately $10\Omega \cdot \text{cm}$, corresponding to $N_A = 1.4 \times 10^{15} \text{ atoms/cm}^3$. The epitaxial process described in Sec. 1.3 indicates that the resistivity of the n-type epitaxial layer can be chosen independently of that of the substrate. Values of 0.1 to 0.5 $\Omega \cdot \text{cm}$ are chosen for the n-type layer. After polishing and cleaning, a thin layer ($0.5 \mu\text{m} = 5,000 \text{ \AA}$) of oxide, SiO_2 , is formed over the entire wafer, as shown in Fig. 1.2a. The SiO_2 is grown by exposing the epitaxial layer to an oxygen or steam atmosphere while being heated to about 1000°C . Silicon dioxide has the fundamental property of preventing the diffusion of impurities through it. Use of this property is made in the following steps.

Step 3. Isolation Diffusion

In Fig. 1.2b the wafer is shown with the oxide removed in four different places on the surface. This removal is accomplished by means of a photolithographic etching process described in Sec. 1.4. The remaining SiO_2 serves as a mask for the diffusion of acceptor impurities (in this case, boron). The wafer is now subjected to the so-called *isolation diffusion*, which takes place at the temperature and for the time interval required for the p-type impurities to penetrate the n-type epitaxial layer and reach the n-type substrate. We thus leave the shaded n-type regions in Fig. 1.2b. These sections are called *isolation islands*, or *isolated regions*, because they are separated by two back-to-back p-n junctions. Their purpose is to allow electrical isolation between different circuit components. For example, it will become apparent later in this section that a different isolation region must be used for the collector of each separate transistor. The p-type substrate must always be held at a negative potential with respect to the isolation islands in order that the p-n junctions be reverse-biased. If these diodes were to become forward-biased in an operating circuit, then, of course, the isolation would be lost. It should be noted that the concentration of acceptor atoms ($N_A \approx 5 \times 10^{20} \text{ cm}^{-3}$) in the region between isolation islands will generally be much higher (and hence indicated as p^+) than in the p-type substrate. The reason for this higher density is to prevent the depletion region of the reverse-biased isolation-to-substrate junction from extending into p^+ -type material (Sec. 1.6) and possibly connecting two isolation islands.

Parasitic Capacitance. It is now important to consider that these isolation regions, or junctions, are connected by a significant barrier, or transition capacitance C_{Ts} , to the p-type substrate, which

capacitance can affect the operation of the circuit. Since C_{Ts} is an undesirable by-product of the isolation process, it is called the *parasitic capacitance*.

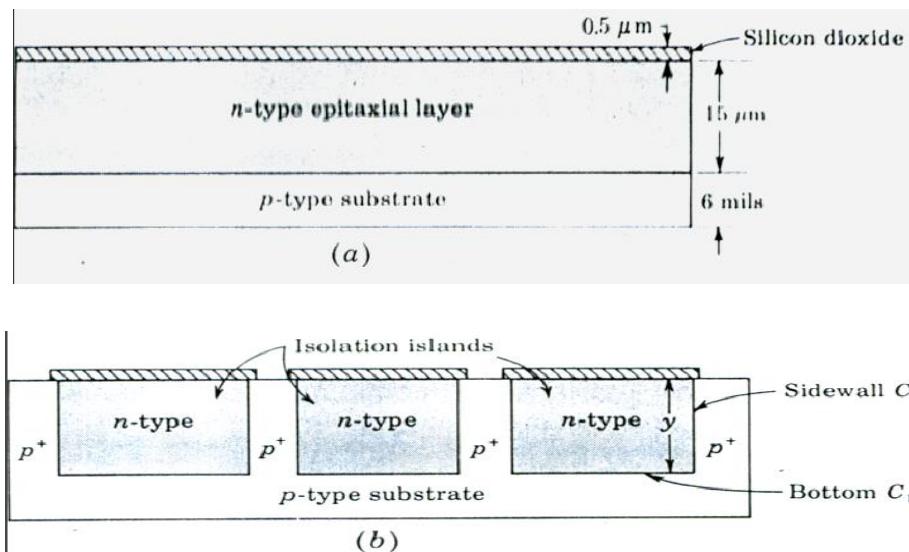
Step 4. Base Diffusion

During this process a new layer of oxide is formed over the wafer, and the photolithographic process is used again to create the pattern of openings shown in Fig. 1.2c. The p-type impurities (boron) are diffused through these openings. In this way are formed the transistor base regions as well as resistors, the anode of diodes, and junction capacitors (if any). It is important to control the depth of this diffusion so that it is shallow and does not penetrate to the substrate. The resistivity of the base layer will generally be much higher than that of the isolation regions.

Step 5. Emitter Diffusion

A layer of oxide is again formed over the entire surface, and the masking and etching processes are used again to open windows in the p-type regions, as shown in Fig. 1.2d. Through these openings are diffused n-type impurities (phosphorus) for the formation of transistor emitters, the cathode regions for diodes, and Junction capacitors.

Additional windows (such as W_1 and W_2 in Fig. 1.2d) are often made into the regions to which a lead is to be connected, using aluminum as the ohmic contact, or interconnecting metal. During the diffusion of phosphorus a heavy concentration (called n^+) is formed at the point where contact with aluminum is to be made. Aluminum is a p-type impurity in silicon, and a large concentration of phosphorus prevents the formation of a $p-n$ junction when the aluminum is alloyed to form an ohmic contact.



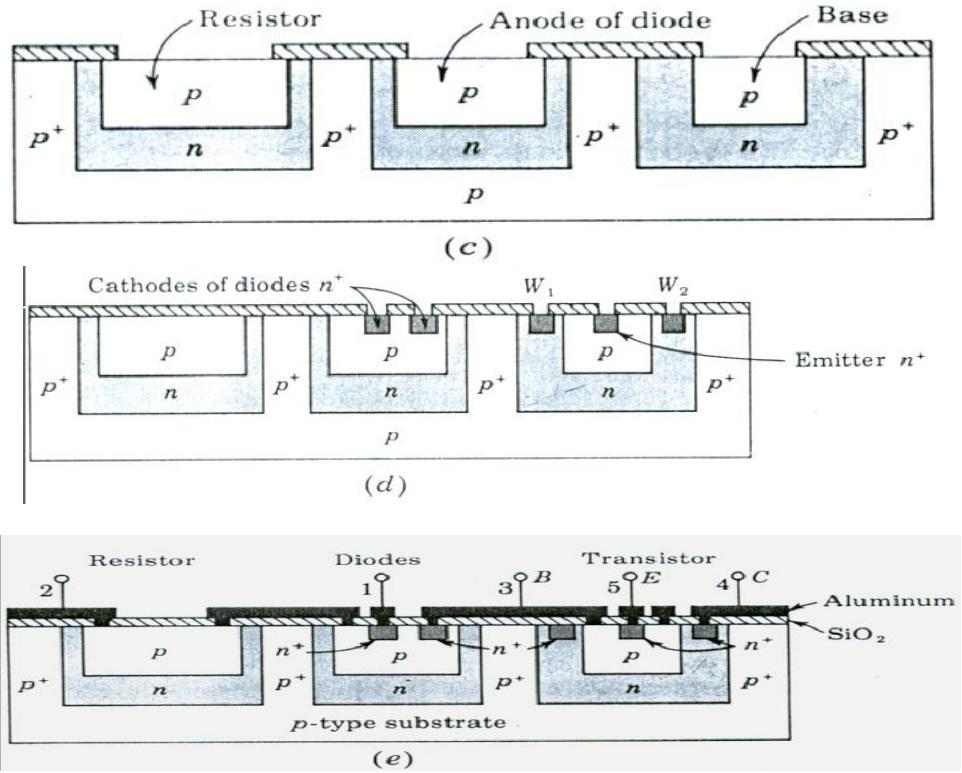


Fig. 1.2 The steps involved in fabricating a monolithic circuit (not drawn to scale). (a) Epitaxial growth; (b) isolation diffusion; (c) base diffusion; (d) emitter diffusion; (e) aluminum metallization.

Step 6. Aluminum Metallization

All p-n junctions and resistors for the circuit of Fig. 1.1a have been formed in the preceding steps. It is now necessary to interconnect the various components of the integrated circuit as dictated by the desired circuit. To make these connections, a fourth set of windows is opened into a newly formed SiO_2 layer as shown in Fig. 1.2e, at the points where contact is to be made. The interconnections are made first, using vacuum deposition of thin even coating of aluminum over the entire wafer. The photoresist technique is now applied to etch away all undesired aluminum areas, leaving the desired pattern of interconnections shown in Fig. 1.2e between resistors, diodes, and transistors. In production, a large number (several hundred) of identical circuits are manufactured simultaneously on a single wafer (Fig. 1.3). After the metallization process has been completed, the wafer is scribed with a diamond tip tool and separated into individual chips. Each chip is then mounted on a ceramic wafer and attached to a suitable header. The package leads are then connected to the integrated circuit by stitch bonding of a 1-mil aluminum or gold wire from the terminal pad on the circuit to the package lead. Most of the labour cost of an IC is in the packaging and testing (which cannot be done in a batch process).

Summary

In this section the epitaxial-diffused method of fabricating microcircuits is described. We have encountered the following processes:

1. Crystal growth of a substrate
2. Epitaxial layer growth
3. Silicon dioxide growth
4. Photoetching
5. Diffusion
6. Vacuum evaporation of aluminum

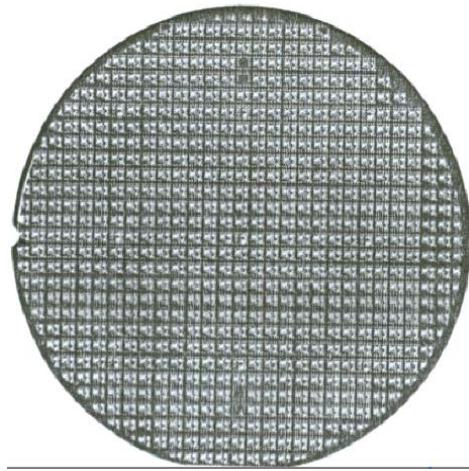


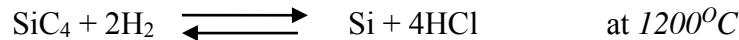
Figure 4-3 A semiconductor wafer about 2 inches in diameter which includes almost 600 monolithic IC chips. (Courtesy of IBM, Inc.)

Using these techniques, it is possible to produce the following elements on the same chip: transistors, diodes, resistors, capacitors, and aluminum interconnections. Processes 3, 4, and 5 enumerated in the foregoing are repeated several times. For example, to fabricate a transistor, five masks are required: the first for the isolation diffusion, the second for the base diffusion, the third for the emitter diffusion, the fourth for location of ohmic contacts through the SiO₂, and the fifth for removing the undesired aluminum areas, so as to leave only the necessary interconnections.

1.3. EPITAXIAL GROWTH

Epitaxy, a term applied to processes used to grow a thin crystalline silicon from the gas phase as a continuation of an existing crystal wafer of the same material. This was developed to enhance the performance of discrete bipolar transistor. Bipolar integrated circuits utilize epitaxial structures in much the same way as discrete transistors. The substrate and epitaxial layer have opposite doping types to provide isolation and a heavily doped diffusion layer serves as a low - resistance collector contact. Unipolar devices such as the junction field-effect transistor (JFET) employ an epitaxial wafer as does the VMOS technology. Epitaxial structures have also been used to improve the

performance of RAMS and CMOS ICs. The basic chemical reaction used to describe the epitaxial growth of pure silicon is the hydrogen reduction of silicon tetrachloride:



Since it is required to produce epitaxial films of specific impurity concentrations, it is necessary to introduce impurities such as phosphine (PH_3) for *n-type* doping or diborane (B_2H_6) for *p-type* doping into the silicon tetrachloride-hydrogen gas stream. An apparatus (which allows simple and precise impurity control) for the production of an epitaxial layer consists of a long cylindrical quartz tube encircled by a radio-frequency induction coil. The silicon wafers are placed on a rectangular graphite rod called a *boat*. The boat is inserted in the reaction chamber, and the graphite is heated inductively to about 1200°C . A control console permits the introduction and removal of various gases required for the growth of appropriate epitaxial layers.

1.4 MASKING AND ETCHING

The monolithic technique described in Section 1.2 requires the selective removal of the SiO_2 to form openings through which impurities may be diffused. The photoetching method used for this removal is illustrated in Fig. 1.4. During the photolithographic process the wafer is coated with a uniform film of a photosensitive emulsion (such as the Kodak *photoresist* KPR). A large black-and-white layout of the desired pattern of openings is made and then reduced photographically. This negative, or stencil, of the required dimensions is placed as a mask over the photoresist, as shown in Fig. 1.4. By exposing the KPR to ultraviolet light through the mask, the photoresist becomes polymerized under the transparent regions of the stencil. The mask is now removed, and the wafer is "developed" by using a chemical (such as trichloroethylene) which dissolves the unexposed (unpolymerized) portions of the photoresist film and leaves the surface pattern as shown in Fig. 1.4b. The emulsion which was not removed in development is *now fixed*, or *cured*, so that it becomes resistant to the corrosive etches used next. The chip is immersed in an etching solution of hydrofluoric acid, which removes the oxide from the areas through which dopants are to be diffused. Those portions of the SiO_2 which are protected by the photoresist are unaffected by the acid (Fig. 1.4c). After diffusion of impurities, the resist mask is removed (stripped) with a chemical solvent (hot H_2SO_4) coupled with a mechanical abrasion process.

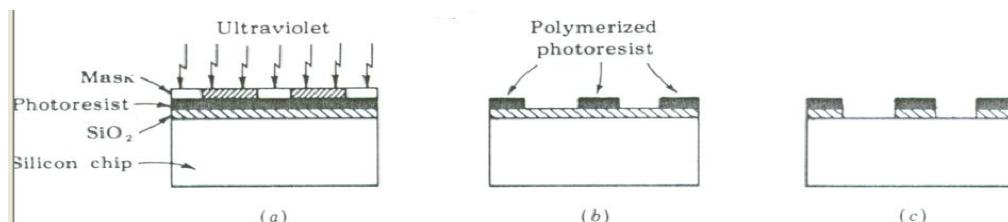


Fig. 1.4. Photoetching technique, (a) Masking and exposure to ultraviolet radiation, (b) The photoresist after development, (c) After etching.

Depending on the type of polymer used either exposed or non-protected areas of film are removed in the developing process. The wafer is then etched to remove the non-protected area. Because the polymer material resists the etching process, they are called resists: [photo resists optical resist;

Electron resist, X-ray resist, ion beam resist etc] depending on type of exposure method. There are two types of resist namely positive and negative resist whose properties are listed below.

Property	Negative	Positive
Solubility in developer after exposure	less	more
Exposure time	less	more
Over exposure-image size	decreases	increases
Resolution	limited	high
Amount of energy	less	high

Summary of Photo masking procedure

- (1) Growth of oxide layer (2) Photo resist layer – applying a thin coat of photo resist on oxidized water surface. (3) Mask plate to exposure – exposing photo resist through a mask plate. (4) Develop etch: - developing and etching photo resist Etch diffusion windows – etching the exposed SiO_2 layer and stripping the photo resist to end up with diffusion window in the SiO_2 layer.

The making of a photographic mask involves complicated and expensive processes. After the circuit layout has been determined, a large-scale drawing is made showing the locations of the openings to be etched in the SiO_2 for a particular process step (say, for the isolation diffusion). The layout may be carried out by use of computer-aided graphics to produce the photographic masking plate. This glass plate is (Fig. 1.4) used for photoresist operation.

The smallest features that can be formed by the photolithographic process described in the foregoing is limited by the wavelength of light, because of diffraction. Electron beams have much smaller wavelengths than radiation and are capable of defining much smaller areas. Hence, electron-beam lithography is now used in the production of masks. A narrow electron beam scans a mask covered with an electron-sensitive resist. In this manner the pattern is written on the mask, the scanning being controlled by a computer. The advantages of this method of mask preparation are higher resolution, the elimination of two photographic reduction steps, and shorter production time. The disadvantage is the high cost of the equipment.

1.5. DIFFUSION OF IMPURITIES

The most important process in the fabrication of integrated circuits is the diffusion of impurities into the silicon chip. Reasonable diffusion times (2 hours) require high diffusion temperatures ($\sim 1000^\circ\text{C}$). Therefore a high-temperature diffusion furnace, having a closely controlled temperature over the length of the hot zone of the furnace, is standard equipment in a facility for the fabrication of integrated circuits. About 20 wafers are placed on a quartz carrier inside the quartz tube of the furnace. Impurity sources in connection with diffusion ovens can be gases, liquids, or solids. For example, the impurity gas for boron diffusion is B_2H_6 , for phosphorous it is

PH_3 and for arsenic it is AsH_3 . An inert carrier gas (such as nitrogen) brings the impurity atoms to the surface of the wafers where they can diffuse into the silicon.

1.5.1. Lateral Diffusion.

For the sake of simplicity of drawing, the cross-sectional diagrams in this chapter are all shown with vertical diffusion edges. However, when a hole is opened in the SiO_2 and impurities are introduced, they will diffuse laterally the same distance that they do vertically. Hence, the impurity will spread out under the passivating oxide surface layer and the Junction profiles should be drawn more realistically as shown in Fig. 1.5.

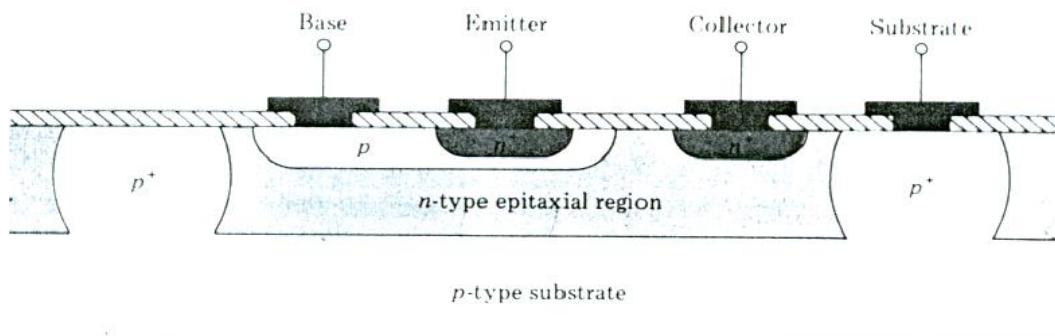


Fig. 1.5 The cross section of an $n-p-n$ transistor indicating curved junction profiles as a result of lateral diffusion

1.6 TRANSISTORS FOR MONOLITHIC CIRCUITS

A planar transistor made for monolithic integrated circuits, using epitaxy and diffusion, is shown in Fig. 1.6a. Here the collector is electrically separated from the substrate by the reverse-biased isolation diodes. Since the anode of the isolation diode covers the back of the entire wafer, it is necessary to make the collector contact on the top, as shown in Fig. 1.6a. It is now clear that the isolation diode of the integrated transistor has two undesirable effects: it adds a parasitic shunt capacitance to the collector and a leakage current path. In addition, the necessity for a top connection for the collector increases the collector-current path and thus increases the collector resistance and $V_{CE}(\text{sat})$ these undesirable effects are absent from the discrete epitaxial transistor shown in Fig. 1.6b. A significant improvement in performance arises from the fact that integrated transistors are located physically close together and their electrical characteristics are closely matched. These matched transistors make excellent difference amplifiers.

The electrical characteristics of a transistor depend on the size and geometry of the transistor, doping levels, diffusion schedules, and the basic silicon material. Of all these factors the size and geometry offer the greatest flexibility for design. The doping levels and diffusion schedules are determined by the standard processing schedule used for the desired transistors in the integrated circuit.

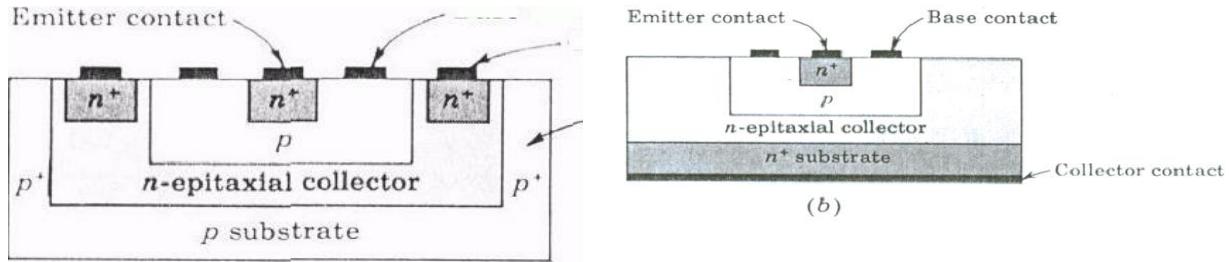


Figure 4-6 Comparison of cross sections of (a) a monolithic integrated circuit transistor with (b) a discrete planar epitaxial transistor. (For a top view of the transistor in *a* see Fig. 1.8.)

1.6.1. Monolithic Transistor Layout

The physical size of a transistor determines the parasitic isolation capacitance as well as the junction capacitance. It is therefore necessary to use small-geometry transistors if the integrated circuit is designed to operate at high frequencies or high switching speeds. The geometry of a typical monolithic transistor is shown in Fig. 1.7. The emitter rectangle is diffused into a base region. Contact to the base is made through two metalized stripes on either side of the emitter. The rectangular metalized area forms the ohmic contact to the collector region. The rectangular collector contact of this transistor reduces the saturation resistance. Since diffusion proceeds in three dimensions, it is clear that the *lateral-diffusion* (Fig. 1.5) will take place. The dashed rectangle in Fig. 1.7 represents the substrate area.

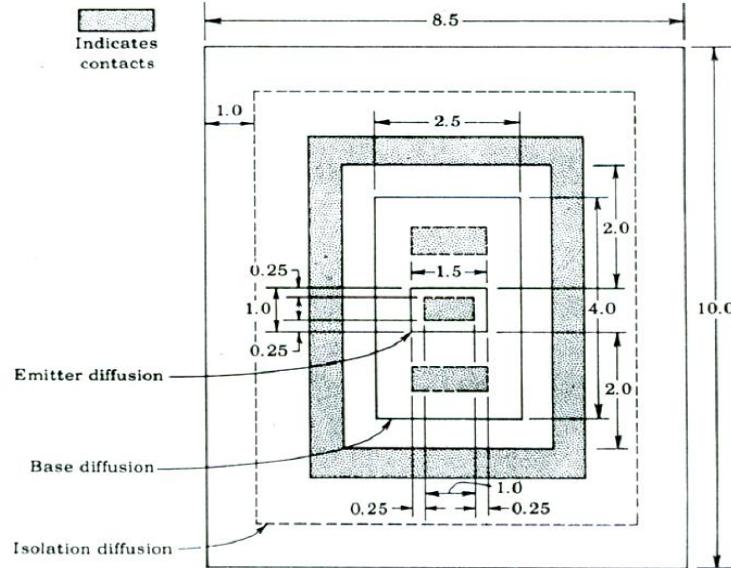


Fig. 1.7. A typical double-base stripe geometry of an integrated-circuit transistor. Dimensions are in mils. (For a side view of the transistor see Fig. 1.6.) (Courtesy of Motorola Monitor.)

1.6.2. Buried Layer

We noted above that the integrated transistor, because of the top collector contact, has a higher collector series resistance than a similar discrete-type transistor. One common method of reducing the collector series resistance is by means of a heavily doped n^+ "buried" layer sandwiched between the p-type substrate and the n-type epitaxial collector, as shown in Fig. 1.8. The buried-layer structure can be obtained by diffusing the n^+ layer into the substrate before the n-type epitaxial collector is grown or by selectively growing the n^+ -type layer, using masked epitaxial techniques. Six masks are required to fabricate this transistor; the five enumerated in Sec. 1.2 and a sixth needed for the buried layer.

We are now in a position to appreciate one of the reasons why the integrated transistor is usually of the $n-p-n$ type. Since the collector region is subjected to heating during the base and emitter diffusions, it is necessary that the diffusion coefficient of the collector impurities be as small as possible, to avoid movement of the collector junction. Since n-type impurities have smaller values of the diffusion constant D than p-type impurities, the collector is usually n-type. In addition, the solid solubility of some n-type impurities is lighter than that of any p-type impurity, thus allowing heavier doping of the n^+ -type emitter and other n^+ regions.

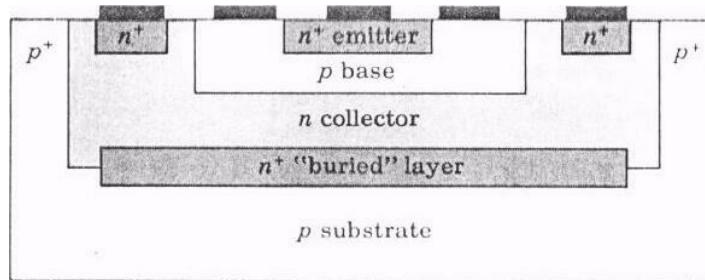


Fig. 1.8 Utilization of "buried" n^+ layer to reduce collector series resistance.

1.6.3. Lateral p-n-p Transistor

The standard integrated-circuit transistor is an $n-p-n$ type, as we have already emphasized. In some applications it is required to have both $n-p-n$ and $p-n-p$ transistors on the same chip. The *lateral p-n-p* structure shown in Fig. 1.9 is the most common form of the integrated $p-n-p$ transistor. This $p-n-p$ uses the standard diffusion techniques as the $n-p-n$, but the last n diffusion (used for the $n-p-n$ transistor) is eliminated. While the p base for the $n-p-n$ transistor is made, the two adjacent p regions are diffused for the emitter and collector of the $p-n-p$ transistor shown in Fig. 1.9. Note that the current flows *laterally* from emitter to collector.

The $p-n-p$ transistor has inferior characteristics compared with those of the $n-p-n$ device. The tolerance of the base thickness (width) in Fig. 1.9 is determined by the lateral diffusion of the p-type impurities as well as by photographic limitations during mask making and alignment.

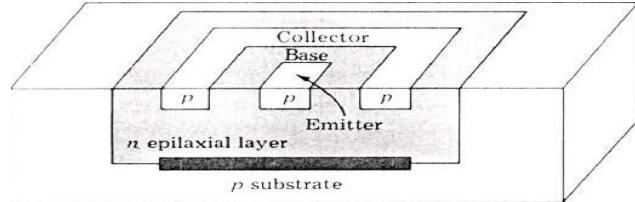


Fig. 1.9. A *p-n-p* lateral transistor.

Consequently, the base width is much larger than that of an *n-p-n* transistor, and the current gain of the *p-n-p* transistor is usually very low (0.5 to 5) instead of 50 to 300 for the *n-p-n* device. However, with improved processing control it is possible to obtain a gain as high as 100 for the lateral *p-n-p* transistor. Since the resistivity of the base region of the *n-p-n* resistor is relatively high, the collector and emitter resistances are large. Because of the long thickness of the base, these transistors have poor high-frequency response.

1.6.4. Vertical *p-n-p* Transistor

This transistor uses the substrate for the *p* collector; the *p* epitaxial layer for the base; and the *p* base of the standard *n-p-n* transistor as the emitter of this *p-n-p* device. We have already emphasized that the substrate must be connected to the most negative potential in the circuit. Hence a vertical *p-n-p* transistor can be only if its collector is at a fixed negative voltage. Such a configuration is called an *emitter follower*.

The vertical *p-n-p* transistor is a poor match for the *n-p-n* transistor. From Figs. 1.2 and 1.7 the base width is $15 - 2.7 = 12.3\mu\text{m}$ compared with $0.7\mu\text{m}$ for the *n-p-n* transistor. However, if the epitaxial layer is made much thinner than the $15\mu\text{m}$ indicated in Fig. 1.2, it is possible to obtain values of current gain as large as 100 for the vertical *p-n-p* device.

1.6.5. Triple-diffused *p-n-p* Transistor

If an extra *p*-type diffusion is added (after the *n*-type diffusion) to the processes described in Fig. 1.2, it is possible to obtain a *p-n-p* transistor. Besides the additional fabrication step required, there are serious design considerations which limit the usefulness of the triple-diffused *p-n-p* transistor.

1.7 Monolith1c Diodes

The diodes utilized in integrated circuits are made by using transistor structures in one of five possible connections. The three most popular diode structures are shown in Fig. 1.10. They are obtained from a transistor structure by using the emitter-base diode, with the collector short-

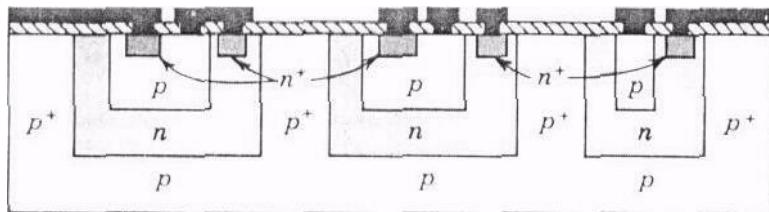


Fig. 1.10. Cross section of various diode structures, (a) Emitter-base diode with collector shorted to base; (b) emitter-base diode with collector open;(c) collector-base diode (no emitter diffusion).

circuted to the base (a); the emitter base diode, with the collector open (b); and the collector-base diode, with the emitter open circuited (or not fabricated at all) (c). The choice of the diode type used depends upon the application and circuit performance desired. Collector-base diodes have the higher collector base voltage-breakdown rating of the collector junction (~ 12 V minimum), and they are suitable for common-cathode diode arrays diffused within a single isolation island, as shown in Fig. 1.11a. Common-anode arrays can also be made with the collector-base diffusion, as shown in Fig. 1.11b. A separate isolation is required for each diode, and the anodes are connected by metallization.

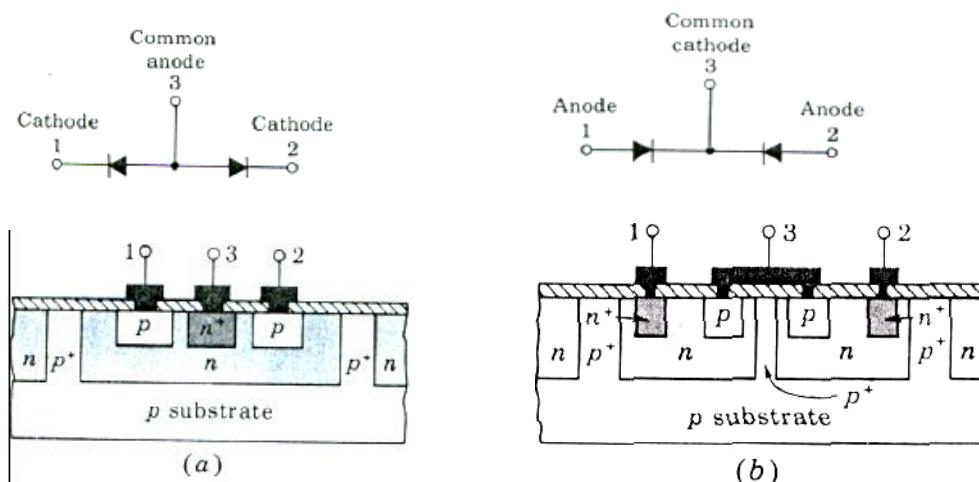


Figure 1.11. Diode pairs, (a) Common-cathode pair and (b) common-anode pair, using collector-base diodes.

1.8 THE METAL-SEMICONDUCTOR CONTACT

Two types of metal-semiconductor junctions are possible, *ohmic* and *rectifying*. The former is the type of contact desired when a lead is to be attached to a semiconductor. On the other hand, the rectifying contact results in a metal-semi-conductor diode (called a *Schottky barrier*), with volt-ampere characteristics very similar to those of a *p-n* diode.

As mentioned in Sec. 1.2 (step 5), aluminum acts as a p-type impurity when in contact with silicon. If Al is to be attached as a lead to *n*-type Si, an ohmic contact is desired and the formation of a *p-n* junction must be prevented. It is for this reason that *n*⁺ diffusions are made in the n regions near the surface where the Al is deposited (Fig. 1.2d). On the other hand, if the *n*⁺ diffusion is omitted and the Al is deposited directly upon the n-type Si, an equivalent *p-n* structure is formed, resulting in an excellent metal-semiconductor diode. In Fig. 1.12 contact 1 is a Schottky barrier, whereas contact 2 is an ohmic (non-rectifying) contact, and a metal-semiconductor diode exists between these two terminals, with the anode at contact 1. Note that the fabrication of a Schottky diode is actually simpler than that of a *p-n* diode, which requires extra (p-type) diffusion.

It should be mentioned that the voltage drop across a Schottky diode is much less than that of a *p-n* diode for the same forward current. Thus, a cutin voltage of about 0.3 V is reasonable for a metal-semiconductor diode as against 0.6 V for a *p-n* barrier. Hence the former is closer to the ideal diode clamp than the latter.

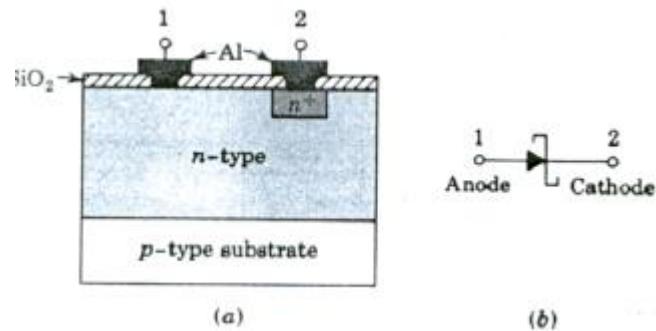


Fig. 1.1.2 (a) A Schottky diode formed by IC techniques. The aluminum and the lightly doped n region form a rectifying contact 1, whereas the metal and the heavily doped n⁺ region form an ohmic contact 2, (b) The symbol for this metal-semiconductor diode.

1.9. INTEGRATED RESISTORS

A resistor in a monolithic integrated circuit is very often obtained by utilizing the bulk resistivity of one of the diffused areas. The p-type base diffusion is most commonly used, although the n-type emitter diffusion is also employed. Since these diffusion layers are very thin, it is convenient to define a quantity known as the *sheet resistance* R_S .

1.9.1. Sheet Resistance

If, in Fig. 1.13, the width w equals the length l , we have a square l by l of material with resistivity ρ , thickness y , and cross-sectional area $A = ly$. The resistance of this conductor (in ohms per square) is

$$R_S = \frac{\rho l}{ly} = \frac{\rho}{y}$$

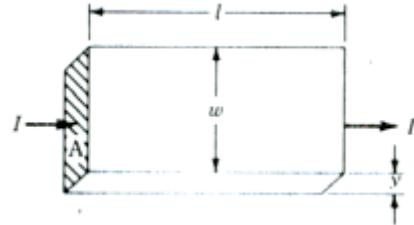


Fig. 1.14 Pertaining to sheet resistance, ohms per square

Note that R_S is independent of the size of the square. Typically, the sheet resistance of the base and emitter diffusions whose profiles are given in Fig. 1.7 is $200 \Omega/\text{square}$ and $2.2 \Omega/\text{square}$, respectively.

The construction of a base-diffused resistor is shown in Fig. 1.1 and is repeated in Fig. 1.15a. A top view of this resistor is shown in Fig. 4-18b. The resistance value may be computed from

$$R = \frac{\rho l}{yw} = R_S \frac{l}{w}$$

where l and w are the length and width of the diffused area, as shown in the top view. For example, a base-diffused-resistor stripe 1 mil wide and 10 mils long contains 10 (1 by 1 mil) squares, and its value is $10 \times 200 = 2,000 \Omega$. Empirical corrections for the end contacts are usually included in calculations of R .

1.9.2. Resistance Values

Since the sheet resistance of the base and emitter diffusions is fixed, the only variables available for diffused-resistor design are stripe length and stripe width. Stripe widths of less than 1 mil (0.001 in) are not normally used because a line-width variation of 0.0001 resulting from mask drawing error or mask misalignment or photographic-resolution error can result in 10 percent resistor-tolerance error.

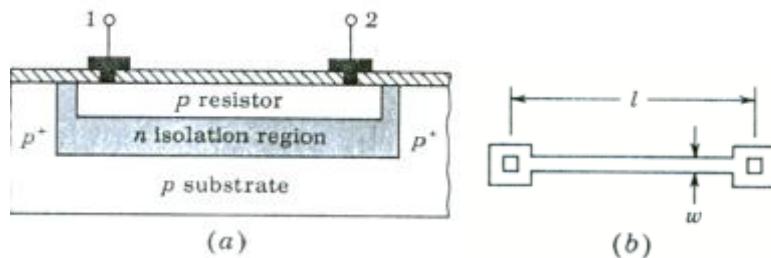


Fig. 1.15 monolithic resistor. (a) Cross-sectional view; (b) top view.

1.10. INTEGRATED CAPACITORS

Capacitors in integrated circuits may be obtained by utilizing the transition capacitance or a reverse-biased p-n junction or thin film or MOS techniques.

A capacitance associated with a p-n junction increases with a reverse-biased potential across the junction and this when properly tailored can be used in Monolithic IC design. The MOS type non-polarized capacitor has a structure of a parallel-plate capacitor. The capacitor can be formed at the same time an npn transistor is being made which therefore require no extra masking level. The process is as indicated below.

1. Bottom plate is n^+ diffusion (same time as emitter is done)
2. Oxide grown then etched (dielectric)
3. Metal used for upper plate.

The value of the capacitor can then be calculated using the formula below.

$$C = \frac{K_o \epsilon_o A}{d}$$

Where d is oxide thickness, A is area of upper plate. K_o is the relative dielectric constant and ϵ_o is the permittivity of free space.

CHAPTER TWO: Bipolar Junction Transistors

2.0 INTRODUCTION

Bipolar Junction Transistors (BJT's) are three terminal devices in which **voltage applied across the two terminals control the current flowing in the third terminal**. The BJT can be used as both a voltage-controlled current source (analog device) and a voltage-controlled switch (digital device). The Bipolar Junction Transistor three terminals are labeled Emitter (E), Base (B), and Collector (C), and are connected to the three regions within a monolithic (single-piece) structure. The name Bipolar implies, namely both mobile carriers, electron and holes, are contributing to the charge transport, hence current. The Bipolar Junction Transistor is called an npn transistor if the transistor's emitter region n-type, base region p-type, and collector region are n-type semiconductors. Likewise, the transistor is pnp transistor if the transistor's emitter region p-type, base region, n-type, and collector region, p-type semiconductor materials. Silicon is the dominant material in transistor fabrication because of temperature and breakdown voltage advantages over other semiconductor materials.

The Bipolar Junction transistors can be viewed as two pn junction diodes connected, back-to-back, in series, namely the emitter-base junction diode and the collector-base junction diode. The different modes of operation of bipolar junction transistor are possible by forward or reverse biasing the two junctions as shown in table 2-1.

Table 2.1 Bipolar junction modes of operation and their junctions biasing

Mode of operation	E-B junction	C-B junction
Saturation	Forward bias	Forward bias
Active	Forward bias	Reverse bias
Reverse active	Reverse bias	Forward bias
Cutoff	Reverse bias	Reverse bias

The combination of the bipolar junction transistor emitter-base junction and collector-base junction voltages for the four modes of operations are given in Fig. 2.1. The junction voltage polarities are given for both *pnp* and *npn* transistors.

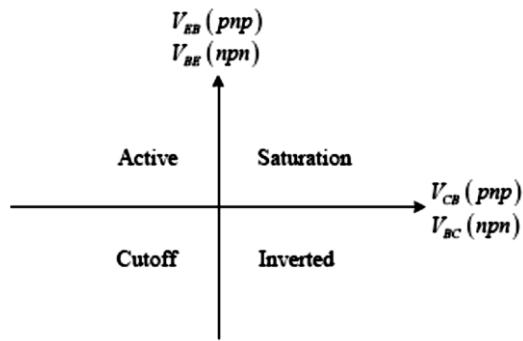


Fig. 2.1 *pnp* and *npn* BJT mode of operations and their junction biases

The output $I-V$ characteristics for bipolar junction transistor in common-emitter configuration for all mode of operation is given in Fig 2.2. Where I_C is collector current flowing out of the transistor for pnp and flowing into the transistor for npn . The output voltage is V_{EC} for pnp and V_{CE} for npn .

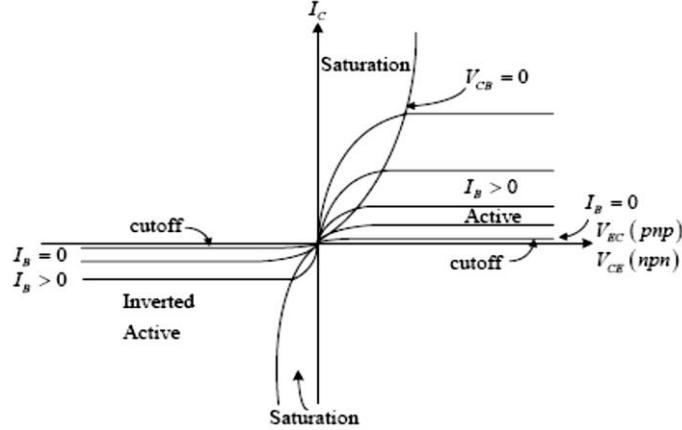


Fig. 2.2 pnp and npn BJT $I-V$ characteristic for the different mode of operations

The 2-port device has four terminals, two input terminals and 2 output terminals. The bipolar junction transistor is a 3-terminal device. In order for the bipolar junction transistors to be employed as a 2-port device, one of the bipolar junction terminals should be in common between input and output of the device. The *Common-Base (CB) configuration*, *Common-Emitter (CE) configuration* and *Common-Collector (CC) configuration* are three configuration possibilities.

The Common Base configuration has an input; emitter-base voltage V_{EB} and emitter current of I_E . Its output is a collector-base voltage V_{CB} and collector current I_C as shown in Fig. 2.3

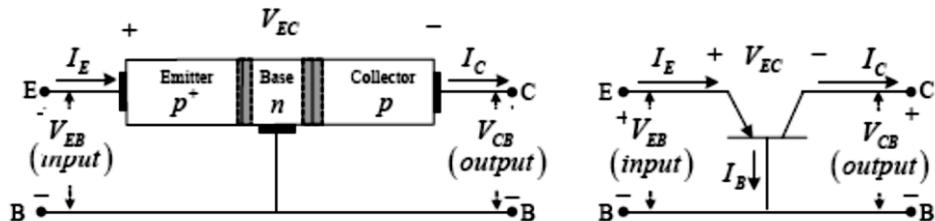


Fig. 2.13 Common Base configuration

A typical input-output $I-V$ characteristic of common-base two port device is given in Fig. 2.4

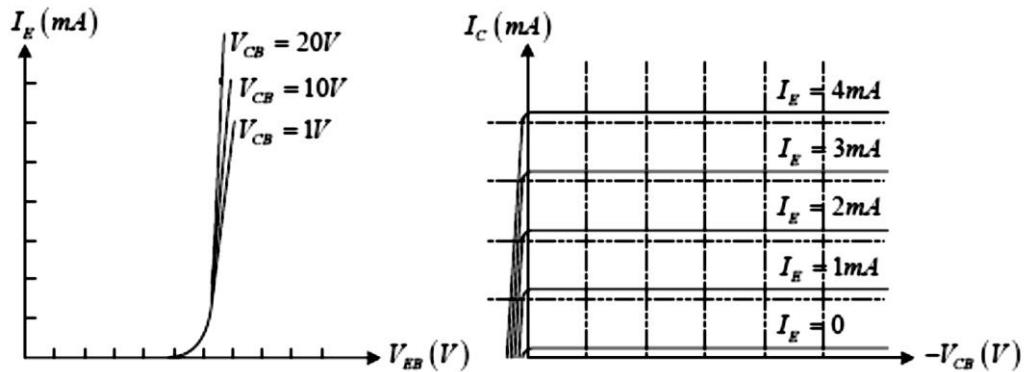


Fig. 2.4 $I-V$ Characteristics of input and output of the Common base configuration

The Common Emitter configuration has an input; emitter-base voltage V_{EB} and base current of I_B . Its output is a collector-base voltage V_{CB} and collector current I_C as shown in Fig. 2.5.

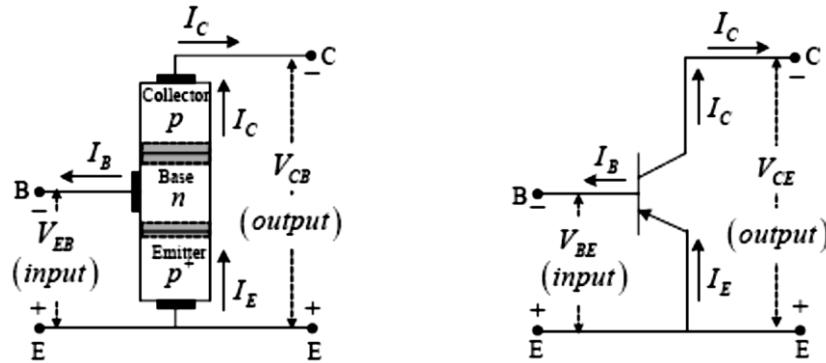


Fig. 2.5 Common Emitter configuration

A typical input-output $I-V$ characteristic of common-emitter two port device is given in Fig. 2.6

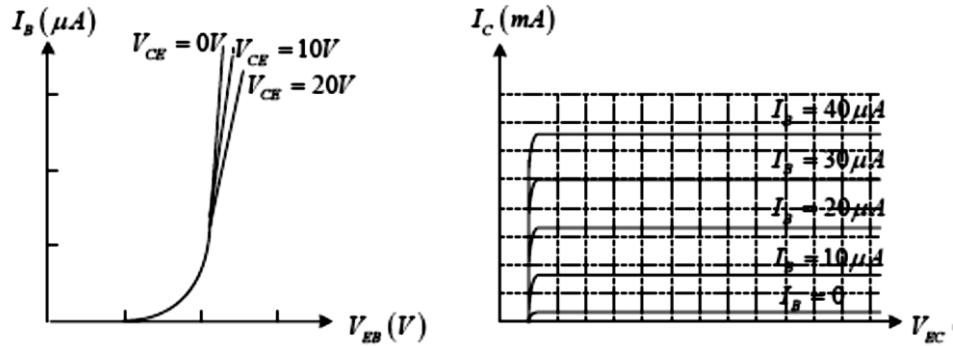


Fig. 2.6 $I-V$ Characteristics of input and output of the Common base configuration

The Common Collector configuration has an input; collector-base voltage V_{CB} and base-current of I_B . Its output is a emitter-collector voltage V_{EC} and emitter current I_E as shown in Fig. 2.7.

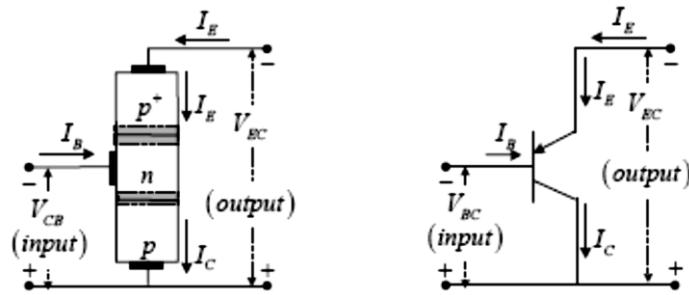


Fig. 2.7 Common Collector configuration

2.1.1 Operation of the pnp transistor in the active mode

In the active mode of operation, the emitter-base junction is forward biased with voltage V_{BE} , which causes the p-type emitter region to be higher in potential than the n-type base region. The collector base junction is reverse biased by voltage, V_{CB} , which cause the p-type collector region to be lower in potential than the n-type collector region (Fig. 2.8)

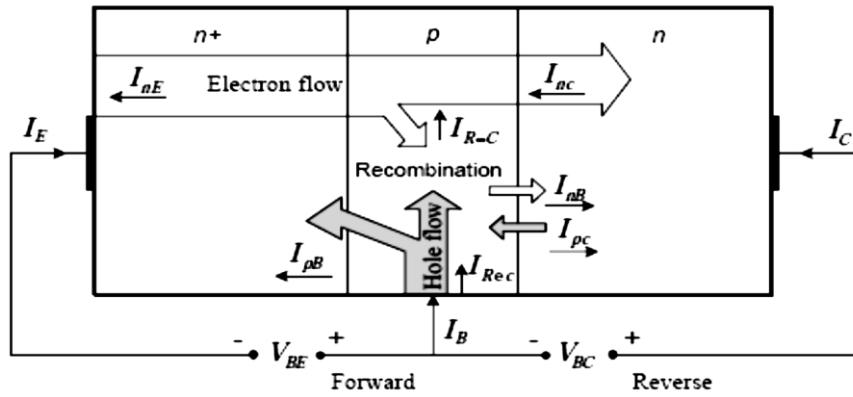


Fig. 2.8 Bipolar Junction Transistor in active mode of operation

The emitter current is made up of majority carriers from the base (holes) I_{pB} and majority carriers from the emitters (electrons) I_{nE} injected across the forward-biased emitter-base junction. Emitter is more heavily doped than the base, resulting in more electrons injected from the emitter than holes injected from the base. The base width W is typically very thin. The collector current almost equals the electron current flowing from the emitter to the base. (Recombination with holes in the base is minimal).

Collector Current

$$I_c = I_s e^{\frac{V_{FB}}{V_T}}$$

where I_s is scale current of saturation current given by

$$I_s = \frac{qAD_n n_i^2}{N_A W}$$

N_A = Doping concentration in the base typical values of I_S are 10^{-14} to $10^{-16} A$

Base Current

i is also proportional to V_{BE} .

$$i_B = \frac{i_C}{\beta}$$

For high β , W should be small, N_A should be low and the emitter should be heavily doped.

2.1.3 Modes of Operation

Consider the simple DC Bias of a BJT in CE configuration shown in Fig. 2.9

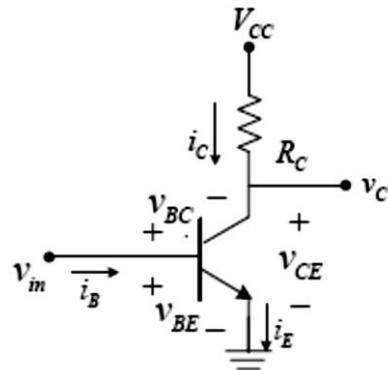


Fig. 2.9 Common Emitter configuration

$I-V$ output characteristics related output variable i_C and V_{CE} , with input current i_E held constant is as in Fig. 2.10

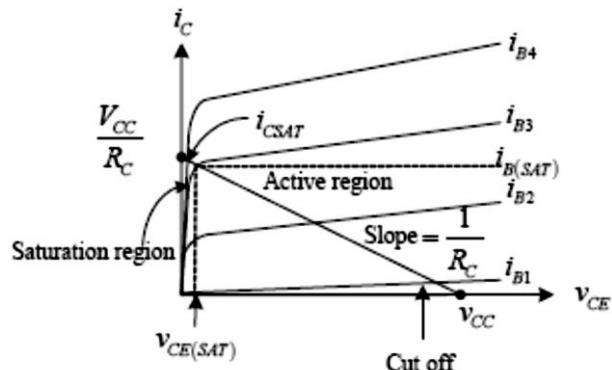


Fig. 2.10 Common Emitter configuration

$$i_E = i_B + i_C$$

$$V_{CE} = V_{BE} - V_{BC}$$

k = overdrive factor $I_{B(EOS)}$ is I_B at the age of saturation.

Table 2-2 Various modes of CE operation

Mode	EBJ	CBJ	V_{BE}	V_{BC}	V_{CE}	i_B	i_C	i_E
Active	Forward	Reverse	≥ 0.7	≤ 0.5	≥ 0.2	i_B	βi_B	$(\beta+1)i_B$
Saturation	Forward	Forward	$= 0.7$	≥ 0.5	≤ 0.2	i_B	$\beta_{forced} i_B$	$i_B + i_C$
Cut-off	Reverse	Reverse	< 0.7	< 0.5	V_{CC}	0	0	0

Example 2.1:

Find the terminal voltages and nodal currents of circuit in Fig. 2.11 for $V_{BE(ON)} = 0.7 = V$, $V_{CC} = 5\text{volts}$, $V_B = 2\text{volts}$ and $\beta = 100$

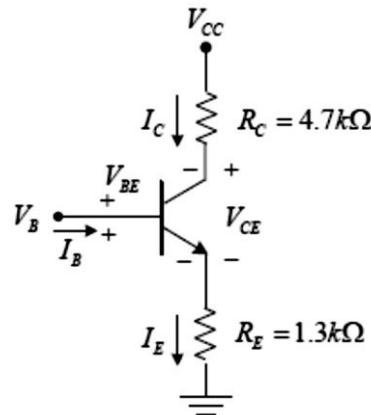


Figure 2-11 Common Emitter configuration

Solution:

Find all currents and voltages. Assume transistor in active mode.

$$V_E = 2V - V_{BE} = 2V - 0.7V = 1.3V$$

$$I_E = \frac{1.3V}{1.3k\Omega} = 1mA$$

$$\alpha = \frac{\beta}{\beta+1} = \frac{100}{100+1} = 0.99$$

$$I_C = \alpha I_E = 0.99(1mA) = 0.99mA$$

$$I_B = \frac{I_E}{\beta+1} = 0.01mA$$

$$V_C = 5V - 0.99mA(1.72k\Omega) = 3.3V$$

$$V_{CE} = V_C - V_E = 3.3 - 1.3 = 2.0V$$

$$V_{BC} = 2V - 3.3V = -1.3V$$

CB Junction reverse biased by 1.3V, Active mode confirmed

Example 2.2

Find the terminal voltages and nodal currents of circuit in Fig. 2.33 for $V_{BE\ (ON)} = 0.7V$, $V_{CC} = 5V$, $V_B = 3V$ and $\beta = 100$.

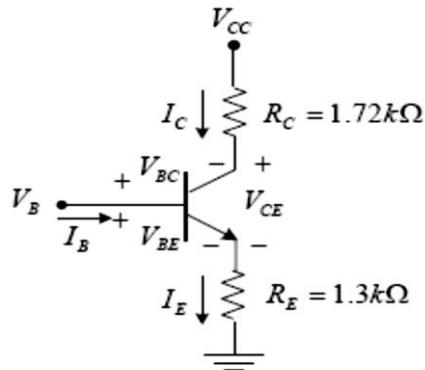


Fig. 2.33 Common Emitter configuration

Solution:

Assume transistor in active mode.

$$V_E = 3V - 0.7V = 2.3V$$

$$I_E = \frac{2.3V}{1.3V} = 1.77mA$$

$$I_C = \alpha I_E = 0.99(1.77mA) = 1.75mA$$

$$V_C = 5V - 1.75mA(1.72k\Omega) = 2V$$

$$V_{BC} = 3V - 2V = 1V$$

CB Junction forward biased saturation mode original assumption is incorrect. Since the transistor is in saturation mode.

$$V_{CE} \approx 0.2V = V_{CE(SAT)}$$

$$V_C = V_E + V_{CE(SAT)} = 2.3V + 0.2V = 2.5volts$$

$$I_C = I_{C(SAT)} = \frac{(5V - 2.5V)}{1.72k\Omega} = 1.45mA$$

$$I_B = I_E - I_C = 1.77mA - 1.45mA = 0.32mA$$

$$\beta_{Forced} = \frac{I_{C(SAT)}}{I_B} = \frac{1.45mA}{0.32mA} = 4.5 < \beta$$

The Transistor is indeed saturated.

Example 2-7

Find the terminal voltages and nodal currents of circuit in Fig. 2.35 for $V_{BE(ON)} = 0.7V$, $V_{CC} = 5volts$, $-V_{EE} = -5volts$ and $\beta = 100$

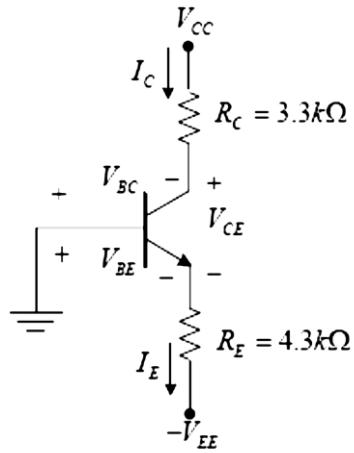


Fig. 2.35 Common Emitter configuration

Solution:

Assume active mode

$$V_E = -0.7V$$

$$I_E = \frac{V_E - (-V_{EE})}{R_E} = \frac{-0.7V - (-5V)}{4.3k\Omega} = 1mA$$

$$I_C = \alpha I_E = 0.99mA$$

$$V_C = 5V - 0.99mA(3.3k\Omega) = 3.27V$$

$$V_{BC} = V_B - V_C = 0 - 3.27 = -3.27V$$

Collector base junction is reversed biased and assumption is correct.

Example 2.8

Find the terminal voltages and nodal currents of circuit in Fig. 2.36 for $V_{BE(ON)} = 0.7V$, $-V_{CC} = -5V$, $V_{EE} = 5V$ and $\beta = 100$

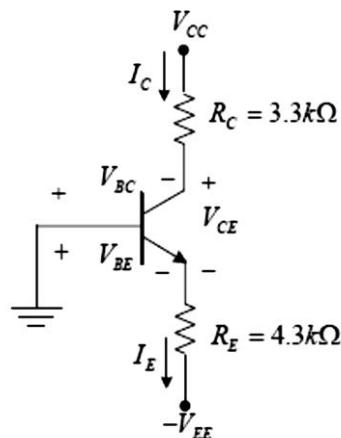


Fig. 2.36 Common Emitter configuration

Solution:

Assume active mode of operation

$$V_E = 0.7V$$

$$I_E = \frac{(5V - 0.7V)}{2k\Omega} = 2.15mA$$

$$I_C = \alpha I_E = 0.99 \times 2.15mA = 2.13mA$$

$$V_C = -5V + I_C R_C = -2.87V$$

$$V_{EC} = 3.57V$$

$$V_{CB} = -2.87V$$

Reverse Bias assumption is correct.

Example 2.9

Find the value of resistance R_B for the transistor to saturate with an overdrive factor of 5, ($K=5$) in circuit in Fig. 2.37 for $20 < \beta < 100$ and $V_{BE(ON)} = 0.7V$, $V_{CC} = 5volts$, $V_B = 3volts$

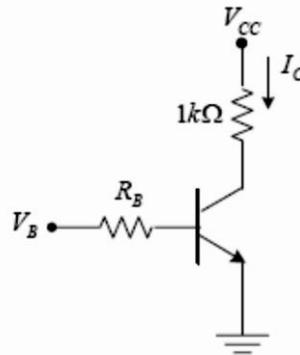


Fig. 2.37 Common Emitter configuration

Solution:

$$I_{C(SAT)} = \frac{5 - V_{CE(SAT)}}{1k\Omega} = \frac{(5 - 0.2)V}{1k\Omega} = 4.8mA$$

$$I_{B(EOS)} = \frac{I_{C(SAT)}}{\beta_{MIN}} = \frac{4.8mA}{20} \cong 0.24mA$$

$$k = 5 = \frac{I_B}{I_{B(EOS)}}$$

$$I_B = 5 \times 0.24mA = 1.2mA$$

$$\frac{3V - 0.7V}{R_B} = 1.2mA$$

$$R_B = 1.91k\Omega$$

Example 2.10

Find I_{C1} , I_{C2} , V_{CE1} , and V_{CE2} in Fig. 2.38, circuit where $V_{BE(ON)} = 0.7V$ and β is large.

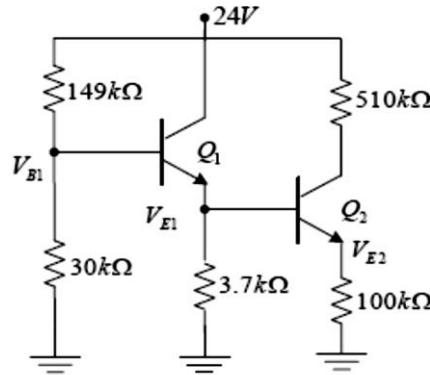


Fig. 2.38 Common Emitter configuration

Solution:

$$V_{B1} = \left(\frac{30k\Omega}{30k\Omega + 149k\Omega} \right) 24V = 4V$$

$$V_{E1} = 4V - 0.7V = 3.7V$$

$$I_{E1} = I_{C1} = \frac{3.7}{3.7k\Omega} = 1mA$$

$$V_{CE1} = 24V - 3.7V = 20.3V$$

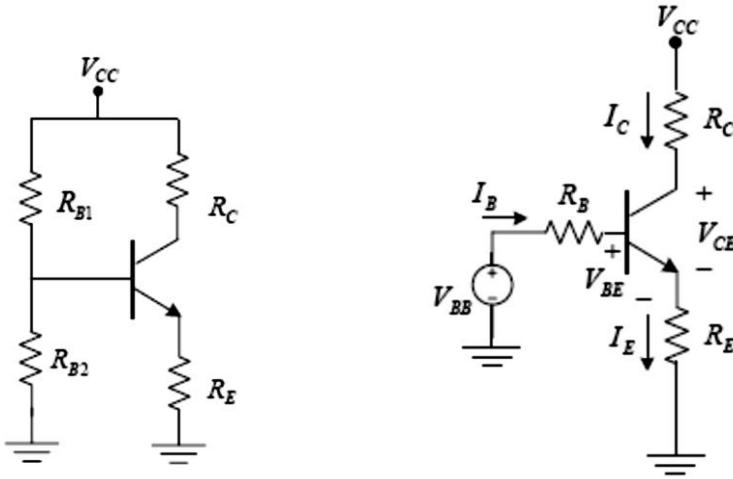
$$V_{E2} = V_{E1} - V_{BE(ON)} = 3.7V - 0.7V = 3V$$

$$I_{E2} = I_{C2} = \frac{3V}{100\Omega} = 30mA$$

$$V_{C2} = 24V - (30mA)(510\Omega) = 8.7V$$

$$V_{CE2} = 8.7 - 3 = 5.7V$$

β - Independent biasing



Figs. 2.39 and 2.40 Common Emitter configuration

$$V_{BB} = I_B R_B + V_{BE} = I_E R_E$$

$$I_B = \frac{I_E}{(\beta+1)}$$

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + \frac{R_B}{(\beta+1)}}$$

$$R_E \gg \frac{R_B}{(\beta+1)}$$

$$I_E \cong \frac{V_{BB} - V_{BE}}{R_E}$$

Independent of β

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$V_{CC} - I_E (\alpha R_C + R_E)$$

Typically we design $V_{CE} \approx \frac{V_{CC}}{3}$, $I_C R_C \approx \frac{V_{CC}}{3}$

Example 2.12

Calculate the DC bias voltages and currents in Fig. 2.45. Given: $V_{CC}=20V$, $R_{B1}=40 k\Omega$, $R_{B2}=4 k\Omega$, $R_C=10 k\Omega$ and $R_E=2 k\Omega$.

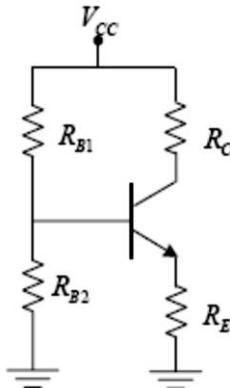


Fig. 2.45 Common Emitter configuration

Solution:

Assume the voltage divider network is not “LOADED” by the transistor (Approximate analysis).

$$V_B = \left(\frac{4}{4+40} \right) 20V = 1.818V$$

$$V_E = V_B - 0.7V = 1.118V$$

$$I_E = \frac{V_E}{R_E} = 0.559mA$$

$$V_C = 20V - (0.559mA)(10k\Omega) = 14.4V (I_C \approx I_E)$$

$$V_{CE} = V_C - V_E = 13.28V$$

Exact analysis (Thevenin the divider network)

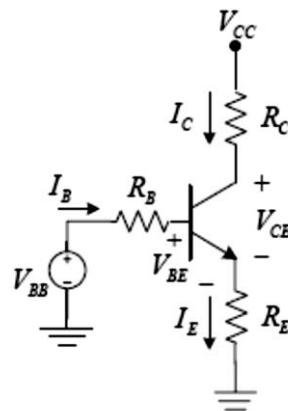


Fig. 2.46 Common Emitter configuration

$$V_{BB} = \left(\frac{4}{40+4} \right) 20V = 1.818V$$

$$R_B = 40k\Omega \parallel 4k\Omega = 3.6k\Omega$$

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + \frac{R_B}{(\beta+1)}} = 0.549mA$$

$$V_E = I_E R_E = 1.098V$$

$$V_B = V_E + 0.7V = 1.798V$$

$$V_C = 20V - (0.549mA)(10k\Omega) = 14.51V$$

$$V_{CE} = V_C - V_E = 13.41V$$

2.2 THE TRANSISTOR AS AN AMPLIFIER

A transistor is biased in active mode of operation in order to be employed as an amplifier.

2.2.1. DC biasing

In order that the transistor operate in active mode, the base-emitter junction is forward biased by a DC voltage of V_{BE} and collector-base junction is reversed biased by DC power supply V_{BE} through resistor R_C . The signal V_{BE} is set to zero.

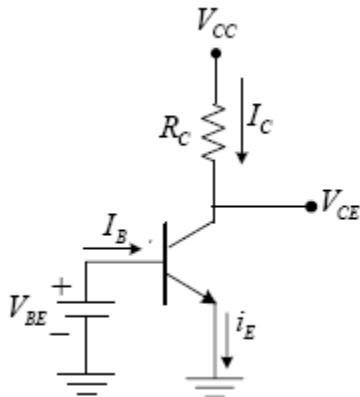


Fig. 2.47 DC biasing of transistor for an amplifier

For active mode of operation voltage at node V_C given should be higher than voltage at node V_B to allow a signal swing at the collector node.

$$V_C = V_{CE} = V_{CC} - R_C I_C$$

2.4 THE T-MODEL

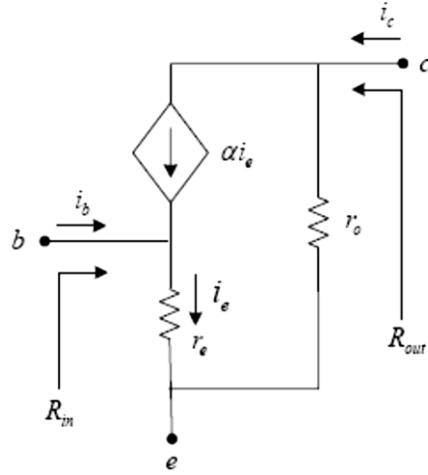


Fig. 2.52. The T-model equivalent circuit Common Emitter configuration

Since i_b is lower than i_e by a factor of $(1 + \beta)$. Looking into the base, we see an impedance $(1 + \beta)$ times higher than r_e . Similarly

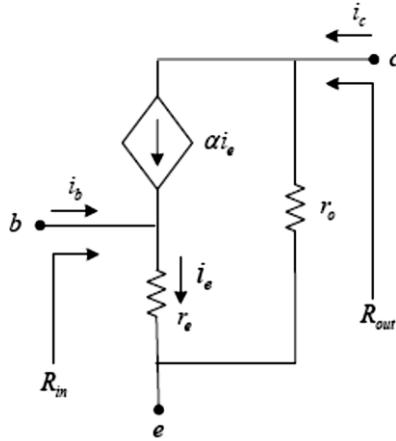


Fig. 2.53 Common Emitter configuration

Looking into the emitter, we see r_e in series with the “reflected” base resistance, which is equal to

$$\frac{R_B}{(1 + \beta)}$$

2.4.1 Common-Emitter Amplifier:

The common-emitter bipolar junction transistor is biased with the two power supply V_{CC} and $-V_{EE}$.

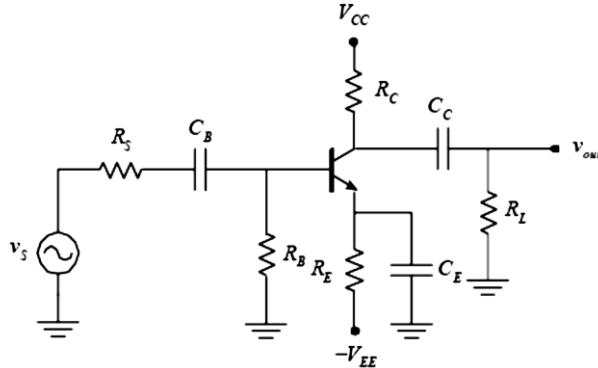


Fig. 2.54 Common Emitter configuration

The reactance of a capacitor X_C is given by

$$X_C = \frac{1}{\omega C} \text{ (Ohms)}$$

All capacitors are specified to have very large values (∞) values then

$$X_C = \frac{1}{\omega(\infty)} = 0 \text{ (Ohms)}$$

Capacitors for any input frequencies are short-circuit except for DC, which are then an open circuit.

The input signal source v_s has a resistance R_s , which through a large bypass capacitor C_B is connected to the transistor base. The output signal V_{out} is taken across the collector to ground.

2.4.2 Small signal equivalent circuit.

To obtain small signal equivalent circuit, short all capacitors and connect all power supplies to AC ground as shown in Figure

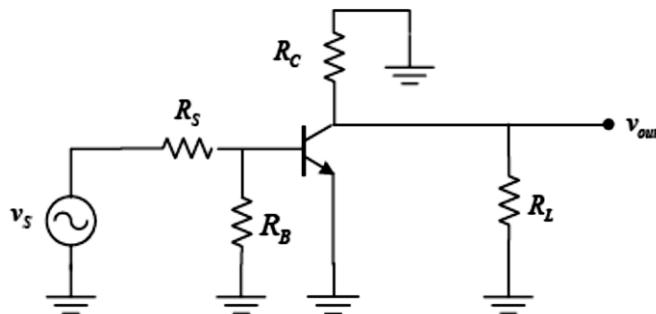


Fig. 2.54 Common Emitter configuration

Replace the transistor by its T-model

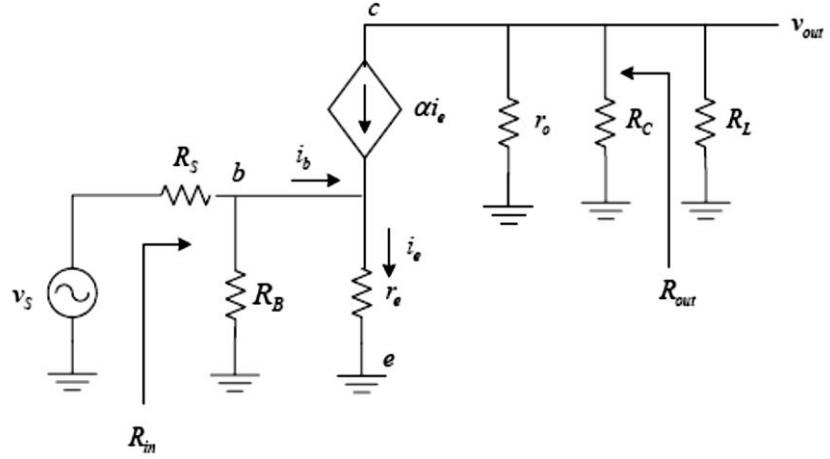


Fig. 2.56 Equivalent T-model for Common Emitter configuration

$$R_{in} = R_B \parallel r_\pi$$

$$R_{out} = R_C \parallel r_o$$

Voltage gain

$$\frac{v_{out}}{v_{in}} = \left(\frac{v_b}{v_{in}} \right) \left(\frac{v_{out}}{v_b} \right)$$

Chain rule

$$\frac{v_b}{v_{in}} = \frac{R_{in}}{R_{in} + R_z}$$

$$v_b = i_e r_e$$

$$v_{out} = -\alpha i_e (r_o \parallel R_C \parallel R_L)$$

$$\frac{v_{out}}{v_b} = \frac{-\alpha (r_o \parallel R_C \parallel R_L)}{r_e}$$

$$\frac{v_{out}}{v_{in}} = -\left(\frac{R_i}{R_i + R_t}\right) \left[\frac{\alpha(r_o \parallel R_c \parallel R_L)}{r_e} \right]$$

Note that

$$g_m = \frac{\alpha}{r_e}$$

The important issues:

The voltage gain from the base to the collector

$$\frac{v_c}{v_b} = (-g_m)$$

The voltage gain from the base to the collector

$$\frac{v_c}{v_b} = -\alpha$$

2.4.3 Current gain of the common emitter amplifier

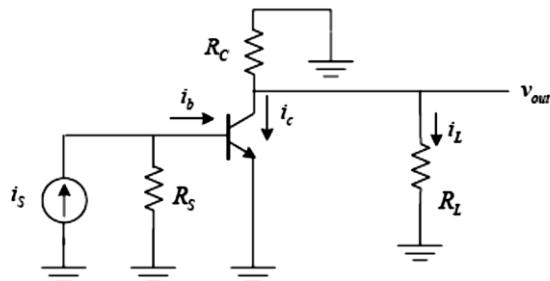


Fig. 2.57 Bipolar

$$\frac{i_L}{i_s} = \left(\frac{i_b}{i_s} \right) \left(\frac{i_c}{i_b} \right) \left(\frac{i_L}{i_c} \right)$$

$$\frac{i_b}{i_s} = \frac{R_s}{R_s + r_\pi}$$

$$\frac{i_c}{i_b} = \beta$$

$$\frac{i_L}{i_c} = \frac{-R_c}{R_c + R_L}$$

Assume $r_o = \infty$

$$\frac{i_L}{i_s} = -\left(\frac{R_s}{R_s + r_\pi}\right) \beta \left(\frac{R_c}{R_c + R_L}\right)$$

$$R_{ib} = (\beta + 1)(r_e + R_{E1}) = r_\pi + (\beta + 1)R_{E1}$$

$$R_m = R_B \parallel R_{ib}$$

$$R_{out} = r_0 (1 + g_m R_{E1}) \parallel R_C \simeq R_C$$

$$\frac{v_{out}}{v_s} = \left(\frac{v_b}{v_s}\right) \left(\frac{v_{out}}{v_b}\right)$$

$$\frac{v_b}{v_s} = \frac{R_m}{R_m + R_s}$$

$$\frac{v_{out}}{v_b} = \frac{-\alpha(R_C \parallel R_L)}{r_e + R_{E1}}$$

Assuming

$$R_{out} \gg R_c \quad \text{and} \quad R_{out} \gg R_L$$

$$\frac{v_{out}}{v_s} = -\left(\frac{R_m}{R_m + R_s}\right) \left[\frac{\alpha(R_C \parallel R_L)}{r_e + R_{E1}} \right]$$

Example:

$$\begin{aligned}
 \beta &= 100 \\
 r_o &= \infty \\
 V_T &= 25mV \\
 V_{BE(ON)} &= 0.7V
 \end{aligned}$$

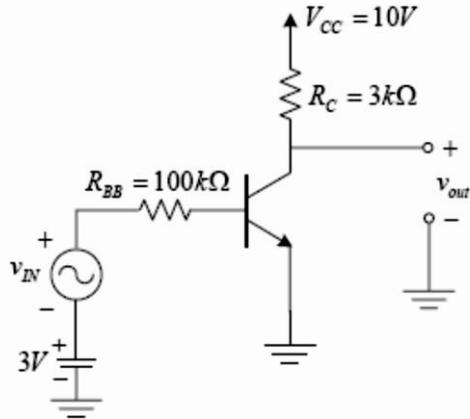


Fig. 2.58 Bipolar

Solution

DC Analysis:

$$I_B = \frac{(3V - 0.7V)}{100k\Omega} = 0.023mA$$

$$I_C = \beta I_B = 2.3mA$$

$$I_E = \frac{I_C}{\alpha} = \frac{2.3mA}{0.99} = 2.323mA$$

$$V_c = V_{cc} - I_C R_C = 3.1V$$

$$V_{CB} = (0.7 - 3.1)V = -2.4V$$

AC Analysis:

$$r_e = \frac{V_T}{I_E} = \frac{25mV}{2.323mA} = 10.8\Omega$$

$$g_m = \frac{I_C}{V_T} = 92mA/V$$

$$r_\pi = \frac{\beta}{g_m} = 1.09k\Omega$$

Small signal model = T model

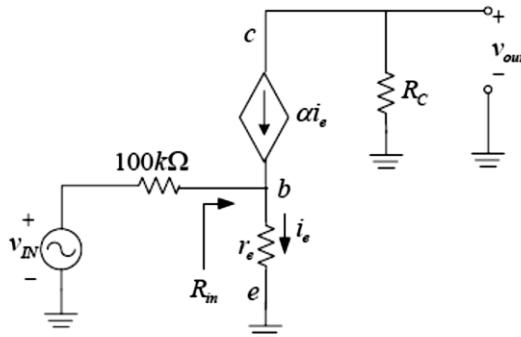


Fig. 2.60

$$\frac{v_{out}}{v_{in}} = \left(\frac{v_b}{v_{in}} \right) \left(\frac{v_{out}}{v_b} \right)$$

$$\frac{v_b}{v_{in}} = \frac{(1+\beta)r_e}{R_{BB} + (1+\beta)r_e} = 0.0108$$

$$v_b = i_e r_e$$

$$v_{out} = -\alpha i_e R_c$$

$$\frac{v_{out}}{v_b} = \frac{-\alpha R_c}{r_e}$$

$$\frac{v_{out}}{v_{in}} = \left[\frac{(1+\beta)r_e}{R_{BB} + (1+\beta)r_e} \right] \left(\frac{-\alpha R_c}{r_e} \right) = \frac{-\alpha(1+\beta)R_c}{R_{BB} + (1+\beta)r_e} = -2.98 V/V$$

Directly on the schematic

$$v_{in} = R_{BB} \left(\frac{i_e}{1+\beta} \right) + i_e r_e$$

$$v_{out} = -\alpha i_e R_c$$

$$\frac{v_{out}}{v_{in}} = \frac{-\alpha i_e R_c}{R_{BB} \left(\frac{i_e}{1+\beta} \right) + i_e r_e} = \frac{-\alpha(1+\beta)R_c}{R_{BB} + (1+\beta)r_e} = -2.98 V/V$$

Example:

- Draw the AC schematic
- Find the small-signal voltage gain v_{out}/v_{in}

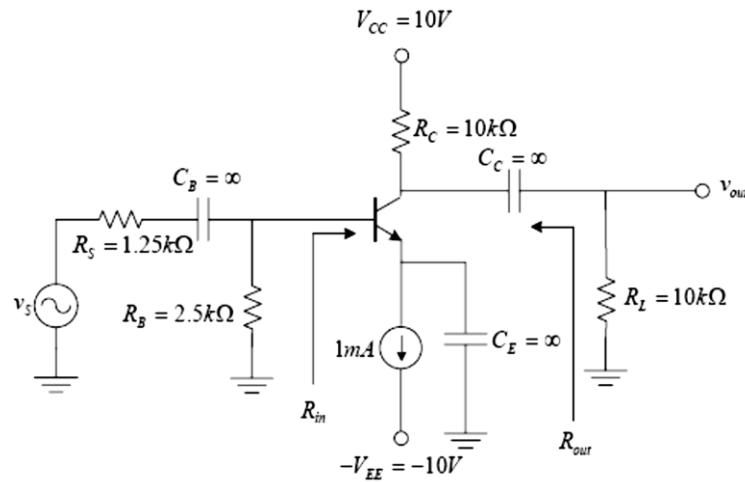


Fig. 2.61

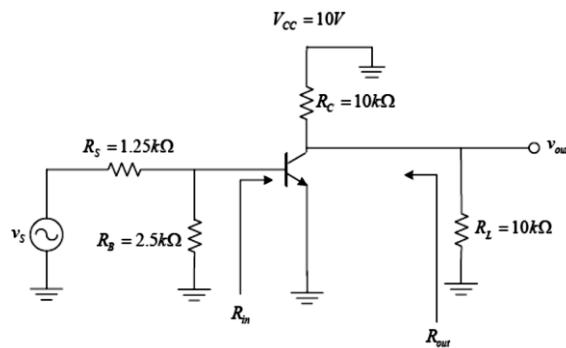


Fig. 2.62

$$r_e = \frac{V_T}{I_E} = 25\Omega$$

$$R_{IN} = r_\pi = (1 + \beta)r_e = 2.5k\Omega$$

$$r_o = \frac{V_A}{I_C} = 10k\Omega$$

$$\frac{v_o}{v_i} = \frac{2.5k\Omega || R_{IN}}{2.5k\Omega || R_{IN} + 1.25k\Omega} = 0.5 \text{ V/V}$$

$$\frac{v_{out}}{v_i} = \frac{-\alpha(10k\Omega || 10k\Omega || r_o)}{r_e} \cong -133.3 \text{ V/V}$$

$$\frac{V_{out}}{V_{in}} = \left(\frac{V_b}{V_{in}} \right) \left(\frac{V_{out}}{V_b} \right) = -66.6 V/V$$

Example:

$$V_T = 25mV \\ V_A = 50V \\ I_E = 1mA \\ \beta = 99 \\ \text{Find } R_{IN}, R_{out}, \frac{V_b}{V_{in}}, \frac{V_{out}}{V_b}, \frac{V_{out}}{V_{in}}$$

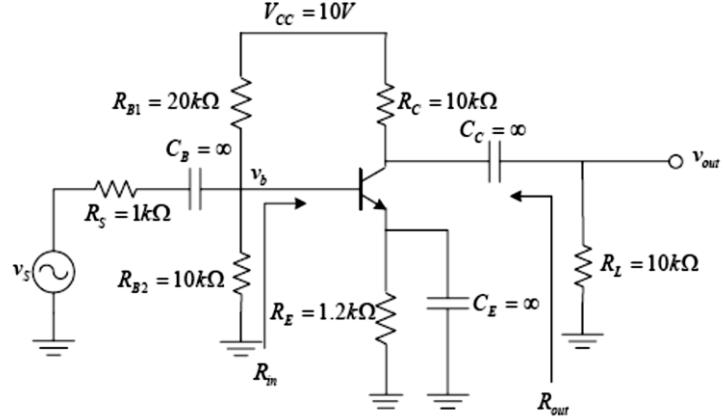


Fig. 2.63

$$r_e = \frac{V_T}{I_E} = 25\Omega$$

$$r_o = \frac{V_A}{I_C} \cong 50k\Omega$$

$$r_\pi = (1 + \beta)r_e = 2.5k\Omega$$

$$R_{IN} = 20k\Omega \parallel 10k\Omega \parallel r_\pi = 1.82k\Omega$$

$$R_{out} = r_o \parallel R_C = 50k\Omega \parallel 10k\Omega = 8.33k\Omega$$

$$\frac{V_b}{V_{in}} = \frac{R_{IN}}{R_i + R_{IN}} = \frac{1.82k\Omega}{1k\Omega + 1.82k\Omega} = 0.645 V/V$$

$$\frac{V_{out}}{V_b} = \frac{-\alpha(R_C \parallel r_o \parallel R_L)}{r_e} \text{ or } -g_m(R_C \parallel r_o \parallel R_L)$$

$$= \frac{-0.99(10k\Omega \parallel 50k\Omega \parallel 10k\Omega)}{25\Omega}$$

$$= -180 V/V$$

$$\frac{V_{out}}{V_{in}} = \left(\frac{V_b}{V_{in}} \right) \left(\frac{V_{out}}{V_b} \right)$$

$$= (0.645 \text{ V/V}) (-180 \text{ V/V}) = -116 \text{ V/V}$$

2.4.4 Common-Emitter Amplifier with Emitter Resistor

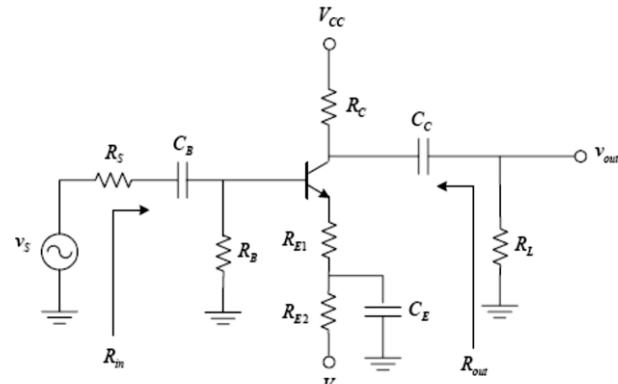


Figure 2.64

Small signal equivalent circuit

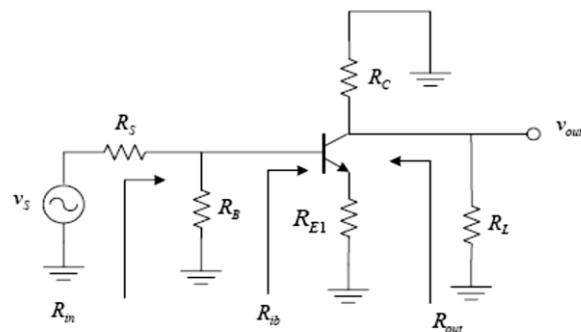


Fig. 2.64

$$R_{out} = r_o (1 + g_m R_{E1}) \parallel R_C \cong R_C$$

Replace the transistor by its T-model

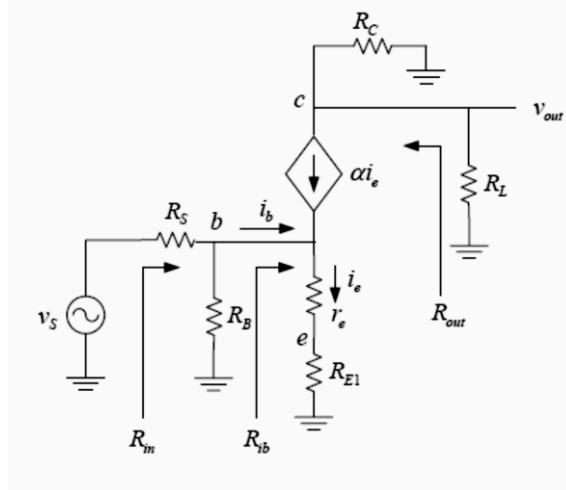


Fig. 2.65 Bipolar

$$R_{ib} = (1 + \beta)(r_e + R_{E1})$$

$$= r_\pi + (1 + \beta)R_{E1}$$

$$R_i = R_B \parallel R_{ib}$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{v_b}{v_{in}} \right) \left(\frac{v_{out}}{v_b} \right)$$

$$\frac{v_b}{v_{in}} = \frac{R_i}{R_i + R_z}$$

$$\frac{v_{out}}{v_b} \cong \frac{-\alpha(R_C \parallel R_L)}{r_e + R_{E1}}$$

Assuming $R_{out} \gg R_C$ and $R_{out} \gg R_L$

$$\frac{v_{out}}{v_{in}} \cong - \left(\frac{R_i}{R_i + R_z} \right) \left[\frac{\alpha(R_C \parallel R_L)}{r_e + R_{E1}} \right]$$

Note that v_{out}/v_b is the ratio of AC resistances again.

We can now derive an expression of v_{out}/v_b in terms g_m

$$g_m \triangleq \frac{i_C}{v_{be}}$$

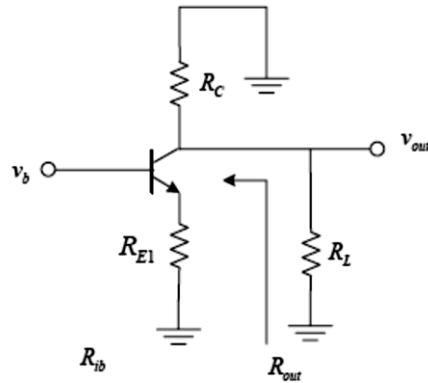


Fig. 2.67

Define

$$g_{m\text{eff}} \triangleq \frac{i_C}{v_b}$$

note that $v_b \neq v_{be}$, then,

$$\frac{v_{out}}{v_b} = -g_{m\text{eff}} (R_C \parallel R_L)$$

$$v_b = i_e r_e + i_e R_{E1}$$

$$i_C = \alpha i_e$$

$$g_{m\text{eff}} = \frac{i_C}{v_b} = \frac{\alpha}{r_e + R_{E1}}$$

$$= \frac{\alpha}{\frac{r_e}{1 + \frac{R_{E1}}{r_e}}}$$

$$\cong \frac{g_m}{1 + g_m R_{E1}}$$

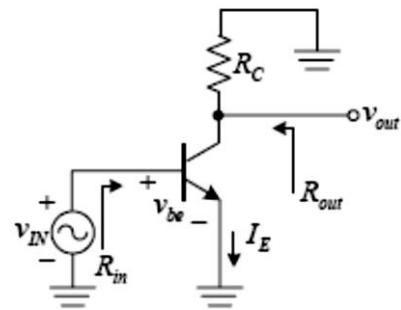


Fig. 2.69

$$\frac{v_{out}}{v_{in}} = \frac{-\alpha(r_o \parallel \infty)}{r_e} = -\frac{\alpha r_o}{r_e}$$

$$r_o = \frac{V_A}{I_C} = \frac{V_A}{\alpha I_E}$$

$$r_e = \frac{V_T}{I_E}$$

$$\frac{v_{out}}{v_{in}} = -\alpha \left(\frac{V_A}{\alpha I_E} \right) \left(-\frac{I_E}{V_T} \right) = \frac{-V_A}{V_T}$$

Intrinsic gain is the maximum possible gain

Example

$$r_e = 25\Omega, \beta = 99, r_o = \infty$$

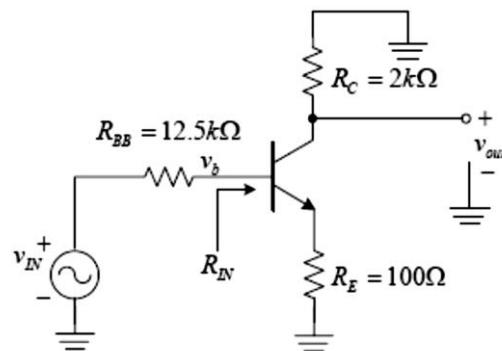


Fig. 2.70

AC schematic

$$R_{in} = (1 + \beta)(r_e + R_E) = (1 + 99)(25\Omega + 100\Omega) = 12.5k\Omega$$

$$g_m = \frac{\beta}{r_e} = \frac{99}{(1 + \beta)r_e} = \frac{\alpha}{r_e} = 39.6 \text{ mA/V}$$

$$g_{m\text{eff}} \cong \frac{g_m}{1 + g_m R_E} \cong \frac{39.6}{1 + 39.6(0.1)} \cong 7.98 \text{ mA/V}$$

$$\frac{v_b}{v_{in}} = \frac{R_{IN}}{R_{BB} + R_{IN}} = 0.5 \text{ V/V}$$

$$\frac{v_{out}}{v_b} = -g_{m\text{eff}} R_C = \left(-7.89 \frac{\text{mA}}{\text{V}} \right) (2k\Omega) = -15.96 \text{ V/V}$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{v_b}{v_{in}} \right) \left(\frac{v_{out}}{v_b} \right) \cong -7.98 \text{ V/V}$$

Second method (T-Model)

$$\frac{v_b}{v_{in}} = 0.5 \text{ V/V}$$

Same above

$$\frac{v_{out}}{v_b} = \frac{-\alpha R_C}{(r_e + R_E)}$$

Ratio of resistances

$$= \frac{-(0.99)2k\Omega}{25\Omega + 100\Omega}$$

$$= -15.84 \text{ V/V}$$

$$\frac{v_{out}}{v_{in}} = (0.5)(-15.84) \text{ V/V} = -7.92 \text{ V/V}$$

Example:

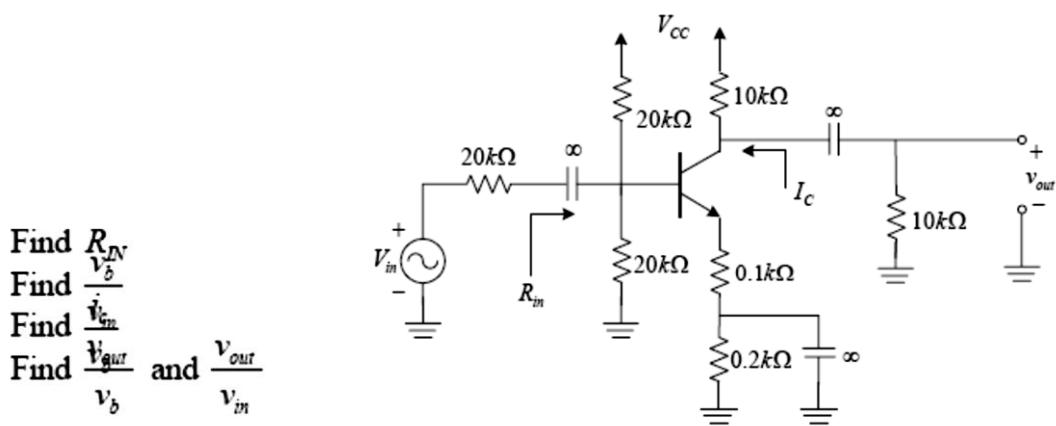


Fig. 2.71 Bipolar

Estimate the peak-to-peak value of v_{in} when you start seeing distortion at the output v_{out}

Solution:

(a)

$$R_{IN} = 20k\Omega \parallel 20k\Omega \parallel r_i$$

$$r_i = (1 + \beta)(r_e + 100\Omega) = 12.5k\Omega$$

$$R_{IN} = 5.56k\Omega$$

(b)

$$\frac{V_b}{v_{in}} = \frac{R_{IN}}{(2k\Omega + R_{IN})} = 0.73/V$$

(c)

$$\frac{i_c}{V_b} \triangleq g_{m\text{eff}} \cong \frac{g_m}{(1 + g_m R_E)}$$

$$g_m = \frac{I_c}{V_T} \cong 40mA/V$$

$$\frac{i_c}{V_b} = \frac{40mA/V}{1 + (40mA/V)(0.1k\Omega)} = 8mA/V$$

(d)

$$\frac{V_{out}}{V_b} = -g_{m\text{eff}} (10k\Omega \parallel 10k\Omega) = -40V/V$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{v_b}{v_{in}} \right) \left(\frac{v_{out}}{v_b} \right) = (0.73)(-40) = -29.2 V/V$$

(e)

$$v_{b(p-p)} \cong (1 + g_m R_E) v_{be(p-p)} \cong (1 + 40 \times 0.1) (10mV_{p-p}) = 50mV_{p-p}$$

$$v_{in(p-p)} = \frac{50mV_{p-p}}{0.73} = 68.5mV_{p-p}$$

Example:5-20

Find R_{IN} , R_{out} and transfer function $\frac{v_{out}}{v_{in}}$ where $V_T = 25mV$, $V_A = \infty$, $\beta = 99$, $I_{E1} = 1mA$.

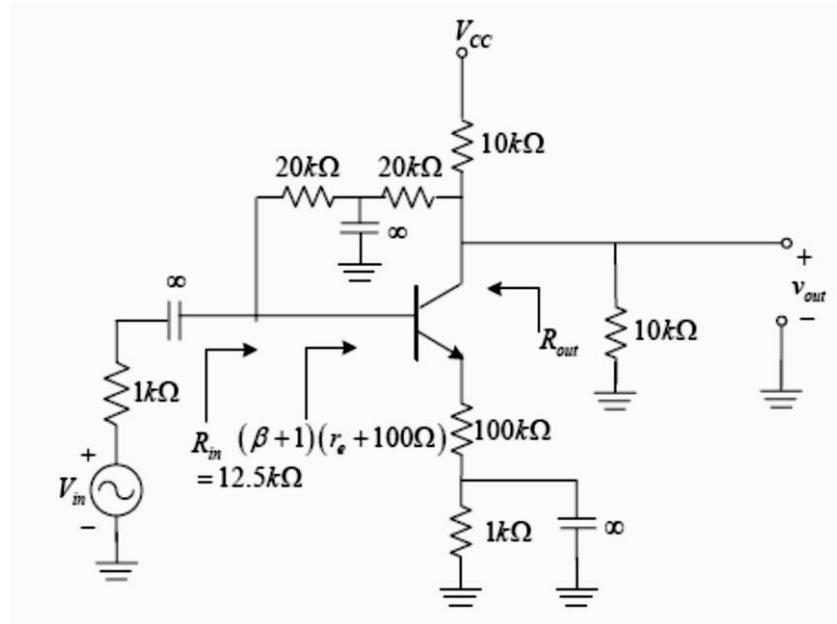


Fig. 2.71 Bipolar

Solution:

$$R_{IN} = 20k\Omega \parallel 12.5k\Omega = 7.7k\Omega$$

$$R_{out} = 10k\Omega \parallel 20k\Omega = 6.7k\Omega$$

$$\frac{v_b}{v_{in}} = \frac{R_{IN}}{1k\Omega + R_{IN}} = \frac{7.7k\Omega}{8.7k\Omega} = 0.89 V/V$$

$$\begin{aligned}
 \frac{v_{out}}{v_b} &= \frac{-\alpha(10k\Omega \parallel 20k\Omega \parallel 10k\Omega)}{r_{e1} + 100\Omega} \\
 &= \frac{-0.99(4k\Omega)}{125\Omega} \\
 &= -31.68 \text{V/V}
 \end{aligned}$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{v_b}{v_{in}} \right) \left(\frac{v_{out}}{v_b} \right) = (0.89 \text{V/V}) (-31.68 \text{V/V}) = -28.2 \text{V/V}$$

2.4.5 Common-Base amplifier:

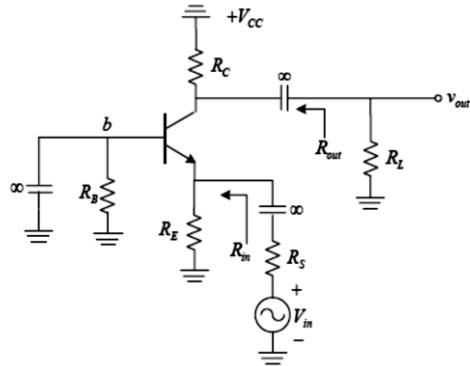


Fig. 2.72 Bipolar

Small signal equivalent circuit

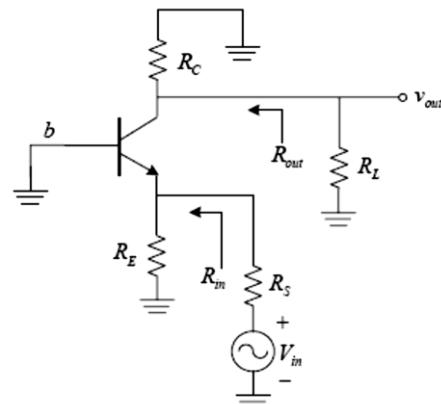


Fig. 2.73 Bipolar

Replace the transistor by its T-Model

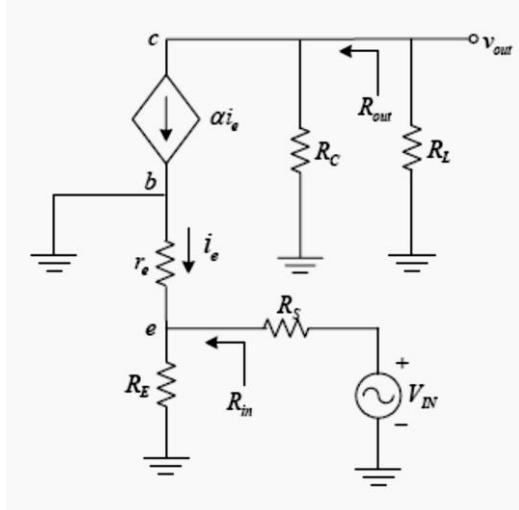


Fig. 2.74 Bipolar

$$R_m = r_e \parallel R_E \cong r_e$$

If $R_E \gg r_e$

$$R_{out} \cong R_C$$

To be more exact

$$R_{out} \cong R_C \parallel \left\{ r_o \left[1 + g_m (R_E \parallel R_s) \right] \right\}$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{r_o}{r_m} \right) \left(\frac{R_C}{r_o} \right)$$

$$\frac{v_o}{v_m} = \frac{R_i}{R_i + R_s} = \frac{r_e \parallel R_E}{r_e \parallel R_E + R_s}$$

$$v_o = -i_e r_e$$

$$v_{out} = -\alpha i_e (R_C \parallel R_L)$$

$$\frac{v_{out}}{v_o} = \frac{\alpha (R_C \parallel R_L)}{r_e}$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{r_e \parallel R_E}{r_e \parallel R_E + R_s} \right) \left[\frac{\alpha (R_C \parallel R_L)}{r_e} \right]$$

Example:

$$V_T = 25mV, \beta = 99, r_o = \infty$$

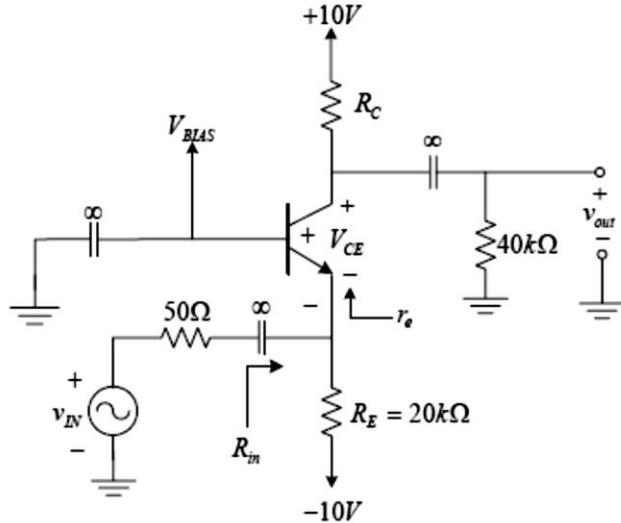


Fig. 2.75 Bipolar

Solution:

- a) Find I_C required setting R_{IN} approximately equal to 100Ω

$$R_{IN} = r_e \parallel 20k\Omega \approx r_e$$

If $r_e \ll 20k\Omega$

$$r_e = 100\Omega = \frac{V_T}{I_E}$$

$$I_C \approx I_E = 0.25mA$$

- b) Find R_C that will set V_{CE} to 5V at the value of I_C found in part (a)

$$V_E = -10V + 0.25mA(20k\Omega) = -5V$$

$$V_C = V_E + V_{CE} = -5V + 5V = 0V$$

$$R_C = \frac{10V}{0.25mA} = 40k\Omega$$

c) Find $\frac{v_{out}}{v_m}$

$$\begin{aligned}\frac{v_{out}}{v_m} &= \left(\frac{R_{IN}}{50\Omega + R_{IN}} \right) \left[\frac{\alpha(R_C \parallel 40k\Omega)}{r_e} \right] \\ &= \left(\frac{100\Omega}{50\Omega + 100\Omega} \right) \left[\frac{0.99(40k\Omega \parallel 40k\Omega)}{100\Omega} \right]\end{aligned}$$

$$= 132 V/V$$

2.4.6 Common Collector Amplifier (Emitter Follower)

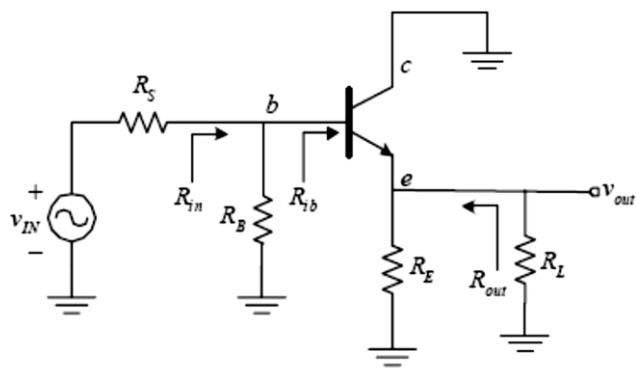


Fig. 2.76 Bipolar

Replace the transistor by its T-Model

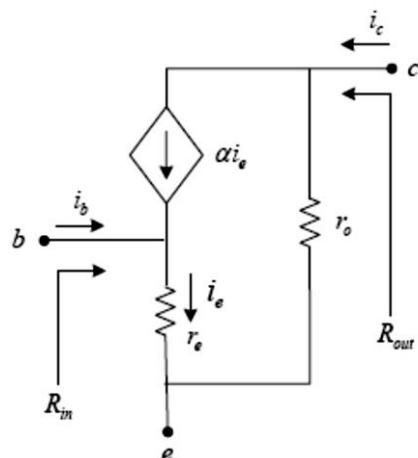


Fig. 2.77 Bipolar

$$R_{ib} = (1 + \beta) [r_o + (R_E \parallel r_o \parallel R_L)]$$

$$R_i = R_B \parallel R_{ib}$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{v_b}{v_{in}} \right) \left(\frac{v_{out}}{v_b} \right)$$

$$\frac{v_b}{v_{in}} = \frac{R_i}{R_i + R_s}$$

$$\frac{v_{out}}{v_b} = \frac{R_E \parallel r_o \parallel R_L}{r_e + R_E \parallel r_o \parallel R_L}$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{R_i}{R_i + R_s} \right) \left(\frac{R_E \parallel r_o \parallel R_L}{r_e + R_E \parallel r_o \parallel R_L} \right)$$

To find R_{out} :

$$R_{out} = r_o \parallel R_E \parallel (r_e + r_R)$$

To find r_R

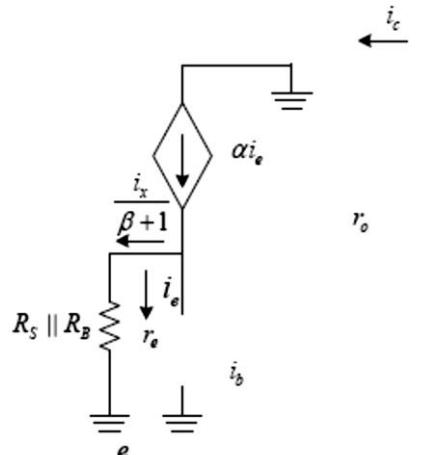


Fig. 2.78 Bipolar

$$r_R = \frac{V_x}{i_x}$$

$$V_x = (R_s \parallel R_B) \frac{i_x}{(1 + \beta)}$$

$$r_R = \frac{R_s \parallel R_B}{(1+\beta)}$$

$$R_{out} = \left[\frac{R_s \parallel R_B}{(1+\beta)} + r_e \right] \parallel r_o \parallel R_E$$

$$\cong r_o$$

If, β , r_o and R_E are large.

2.5 MULTIPLE-TRANSISTOR AMPLIFIERS:

Voltage divider and the effect of loading

$$\frac{v_{out}}{v_{in}} = \frac{2k\Omega}{2k\Omega + 2k\Omega} = \frac{1}{2}$$

V_A is loaded by another 2K resistor

$$\frac{v_{out}}{v_{in}} = \left(\frac{V_A}{v_{in}} \right) \left(\frac{v_{out}}{V_A} \right)$$

$$\frac{v_{out}}{v_{in}} \neq \left(\frac{2k\Omega}{2k\Omega + 2k\Omega} \right) \left(\frac{1k\Omega}{1k\Omega + 1k\Omega} \right) \neq \frac{1}{4}$$

Should be

$$\frac{v_{out}}{v_{in}} = \left(\frac{2k\Omega}{2k\Omega + 2k\Omega \parallel 2k\Omega} \right) \left(\frac{1k\Omega}{1k\Omega + 1k\Omega} \right) = \frac{1}{6}$$

If a buffer is added

$$\frac{v_{out}}{v_{in}} = \left(\frac{2k\Omega}{2k\Omega + 2k\Omega} \right) \left(\frac{1k\Omega}{1k\Omega + 1k\Omega} \right) = \frac{1}{4}$$

Note: Need to determine the "TOTAL" loading at a node before doing voltage division.

Example:

$$I_{E1} = I_{E2} = 1mA$$

$$V_T = 25mV$$

$$\beta = 119$$

$$V_A = 40V$$

Find $\frac{V_{out}}{V_{in}}$ and R_{out}

$$r_{o1} = r_{o2} \cong \frac{V_A}{1mA} = 40k\Omega$$

$$r_{e1} = r_{e2} = \frac{V_T}{1mA} = 25\Omega$$

$$R_{IN1} = (1 + \beta) r_{e1} = 3k\Omega$$

$$R_{IN2} = (1 + \beta)(r_{e2} + 10k\Omega \parallel 10k\Omega \parallel 40k\Omega) \cong 534k\Omega$$

$$\frac{v_{b1}}{v_{in}} = \frac{R_{IN1}}{10k\Omega + R_{IN1}} = 0.231 V/V$$

$$\begin{aligned} \frac{v_{c1}}{v_{b1}} &= \frac{-\alpha(10k\Omega \parallel R_{IN2} \parallel r_{o1})}{r_{e1}} = \frac{-0.992(10k\Omega \parallel 534k\Omega \parallel 40k\Omega)}{25\Omega} \\ &= -315 V/V \end{aligned}$$

$$\frac{v_{out}}{v_{c1}} = \frac{10k\Omega \parallel 10k\Omega \parallel r_{o2}}{r_{e2} + 10k\Omega \parallel 10k\Omega \parallel r_{o2}} = 0.995 V/V$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{v_{b1}}{v_{in}} \right) \left(\frac{v_{c1}}{v_{b1}} \right) \left(\frac{v_{out}}{v_{c1}} \right) = -72 V/V$$

$$R_{out} = \left[\left(\frac{10k\Omega \parallel r_{o1}}{1 + \beta} \right) + r_{e2} \right] \parallel 10k\Omega \parallel 10k\Omega \parallel 40k\Omega$$

$$= (67\Omega + 25\Omega) \parallel 10k\Omega \parallel 10k\Omega \parallel 40k\Omega$$

$$\cong 90\Omega$$

Example:

$$I_{E1} = I_{E2} = 0.1mA$$

$$\beta = 99$$

$$r_o = \infty$$

$$V_T = 25mV$$

Solution

$$r_{e1} = r_{e2} = \frac{25mV}{0.1mA} = 250$$

$$R_{IN1} = (1 + 99)(r_{e1} + 500\Omega \parallel 500\Omega) = 50k\Omega$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{v_{b1}}{v_{in}} \right) \left(\frac{v_{e1}}{v_{b1}} \right) \left(\frac{v_{e2}}{v_{e1}} \right) \left(\frac{v_{out}}{v_{e2}} \right)$$

$$\frac{v_{b1}}{v_{in}} = \frac{R_{IN1}}{10k\Omega + R_{IN1}} = \frac{50k\Omega}{10k\Omega + 50k\Omega} = 0.833$$

$$\frac{v_{e1}}{v_{b1}} = \frac{500\Omega \parallel 500\Omega}{r_{e1} + 500\Omega \parallel 500\Omega} = 0.5$$

$$\frac{v_{e2}}{v_{e1}} = \frac{250\Omega}{250\Omega + 250\Omega} = 0.5$$

$$\frac{v_{out}}{v_{e2}} = \frac{\alpha(20k\Omega)}{r_{e2}} = \frac{(0.99)(20k\Omega)}{250\Omega} = 79.2$$

$$\frac{v_{out}}{v_{in}} = (0.833)(0.5)(0.5)(79.2) = 16.5$$

Example:

$$r_{e1} = r_{e2} = 25\Omega$$

$$\beta = 49$$

$$V_A = \infty$$

Find R_{IN} , R_{out} and $\frac{v_{out}}{v_{in}}$

$$r_{in2} = (1+49)(r_{e2} + 1k\Omega \parallel 50\Omega) = 3.63k\Omega$$

$$R_{IN} = (1+49)(r_{e1} + 1k\Omega \parallel r_{in2}) = 40.45k\Omega$$

$$R_{out} = \left\{ \frac{\left[\frac{10k\Omega}{(1+49)} + r_{e1} \right] \parallel 1k\Omega}{(1+49)} + r_{e2} \right\} \parallel 1k\Omega = 28\Omega$$

$$\frac{v_{b1}}{v_{in}} = \frac{R_{IN}}{10k\Omega + R_{IN}} = 0.80V/V$$

$$\frac{v_{e1}}{v_{b1}} = \frac{1k\Omega \parallel r_{in2}}{r_{e2} + 1k\Omega \parallel r_{in2}} = 0.97V/V$$

$$\frac{v_{out}}{v_{e1}} = \frac{1k\Omega \parallel 50\Omega}{r_{e2} + 1k\Omega \parallel 50\Omega} = 0.66V/V$$

$$\frac{v_{out}}{v_{in}} = (0.80V/V)(0.97V/V)(0.66V/V) = 0.51V/V$$

Example:

$$V_{EE} = V_{EB} = 0.7V$$

$$\beta_{npn} = 99$$

$$\beta_{pnp} = 49$$

$$r_{o1} = r_{o2} = \infty$$

$$\alpha_1 = 0.99$$

$$\alpha_2 = 0.98$$

Find V_{out} and $\frac{v_{out}}{v_{in}}$

DC Analysis:

$$I_E = \frac{-0.7 - (-10)}{9.3k\Omega} = 1mA$$

$$I_C = \alpha I_E = 0.99mA$$

$$V_{C1} \approx 20V - (10k\Omega)(0.99mA) \approx 10.1V$$

Assume $I_B \cong 0$

$$V_{E2} = 10.1V + 0.7V = 10.8V$$

$$I_{E2} = \frac{(20 - 10.8)V}{9.3k\Omega} = 0.989mA$$

$$I_{C2} = \alpha_2 I_{E2} = 0.969mA$$

$$V_{out} = 9.69V$$

AC analysis:

$$r_{e1} = 25\Omega \text{ And } r_{e2} = 25.3\Omega$$

$$\frac{v_{c1}}{v_{in}} \cong \frac{-10k\Omega || (1 + \beta_{pnp}) r_{e2}}{r_{e1}} \cong -44.9 \frac{V}{V}$$

$$\frac{v_{out}}{v_{c1}} \cong \frac{-10k\Omega}{r_{e2}} \cong -395.3$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{v_{c1}}{v_{in}} \right) \left(\frac{v_{out}}{v_{c1}} \right) = (-44.9)(-395.3) = 1.78 \times 10^4 \frac{V}{V}$$

Example:

$$V_{CE(sat)} = 0V \quad \beta = 99$$

- a) Find R_1 and R_2 for maximum symmetrical output voltage swings
- b) Sketch the DC and the AC load lines.

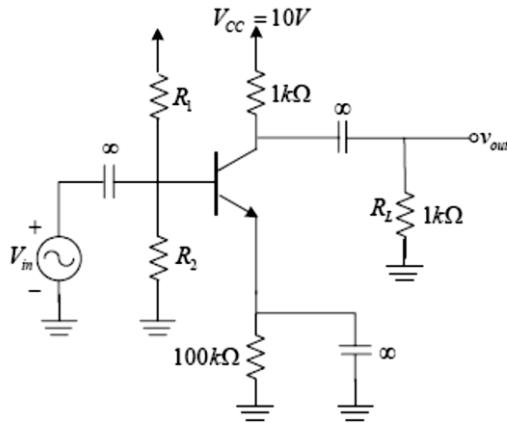


Fig. 2.79 Bipolar

Solution:

(a)

$$R_{AC} = R_C \parallel R_L = 1k\Omega \parallel 1k\Omega = 0.5k\Omega$$

$$R_{DC} = R_C + R_E = 1k\Omega + 100\Omega = 1.1k\Omega$$

$$I_{CQ} = \frac{V_{CC}}{R_{AC} + R_{DC}} = \frac{10V}{0.5k\Omega + 1.1k\Omega} = 6.25mA$$

$$R_B = R_1 \parallel R_2 = \frac{(1+\beta)R_E}{10} = 1k\Omega$$

$$V_{BB} = V_{BE} + I_{CQ} \left(R_E + \frac{R_B}{1+\beta} \right) = 0.7V + 6.25mA \left(0.1k\Omega + \frac{1k\Omega}{1+99} \right) = 1.39V$$

$$V_{CEQ} = I_{CQ} R_{AC} = 3.13V$$

$$R_1 = R_B \left(\frac{V_{CC}}{V_{BB}} \right) = 7.19k\Omega$$

$$R_2 = \frac{R_B}{1 - \frac{V_{BB}}{V_{CC}}} = 1.16k\Omega$$

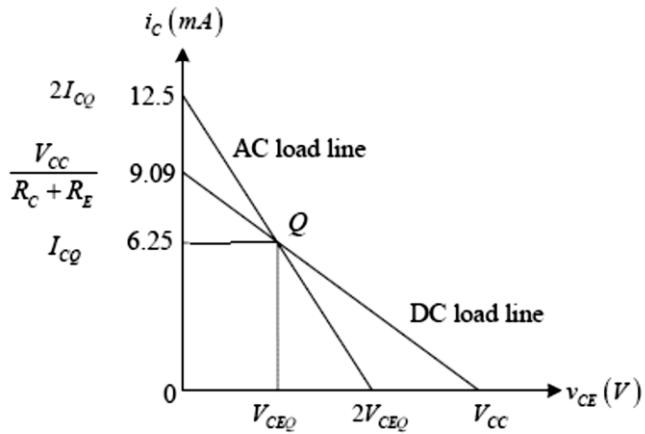


Fig. 2.80

Example:

$$V_{CE(sat)} = 0V \quad \beta = 99$$

- a) Find R_1 and R_2 for maximum symmetrical output voltage swings
- b) Sketch the DC and the AC load lines.

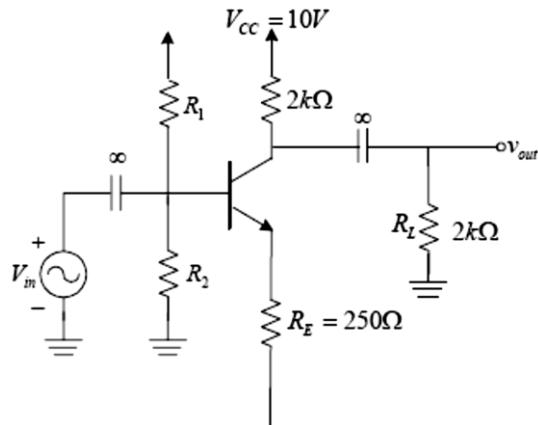


Fig. 2.81

Solution:

$$R_{AC} = R_C \parallel R_L + R_E = 2k\Omega \parallel 2k\Omega + 250\Omega = 1.25k\Omega$$

$$R_{DC} = R_C + R_E = 2k\Omega + 250\Omega = 2.25k\Omega$$

$$I_{CQ} = \frac{V_{CC}}{R_{AC} + R_{DC}} = \frac{10V}{1.25k\Omega + 2.25k\Omega} = 2.86mA$$

$$V_{CEQ} = I_{CQ} R_{AC} = 3.57V$$

$$R_B = \frac{(1+\beta)R_E}{10} = 2.5k\Omega$$

$$V_{BB} = V_{BE} + I_{CQ} \left(R_E + \frac{R_B}{1+\beta} \right) = 1.49V$$

$$R_1 = R_B \left(\frac{V_{CC}}{V_{BB}} \right) = 16.78k\Omega$$

$$R_2 = \frac{R_B}{1 - \frac{V_{BB}}{V_{CC}}} = 2.94k\Omega$$

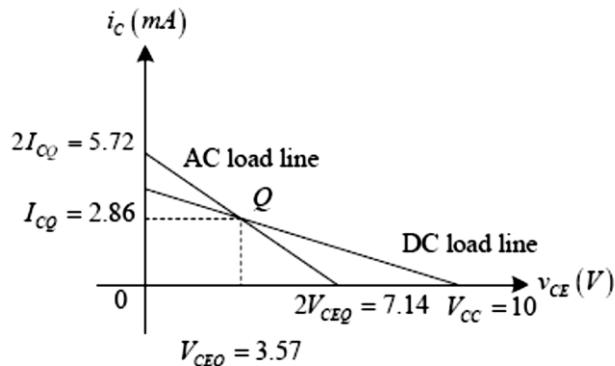


Fig. 2.82

Maximum symmetrical output voltage swing

$$= 2I_{CQ} (2k\Omega \parallel 2k\Omega) = 5.72V_{P-P}$$

CHAPTER THREE: The Field Effect Transistor (FET)

3.1 Introduction.

The FET is a three terminal device like the BJT, but operates by a different principle. The three terminals are called the source, drain, and gate. The voltage applied to the gate controls the current flowing in the source-drain channel. No current flows through the gate electrode, thus the gate is essentially insulated from the source-drain channel. Because no current flows through the gate, the input impedance of the FET is extremely large (in the range of 10^{10} – $10^{15} \Omega$). The large input impedance of the FET makes them an excellent choice for amplifier inputs.

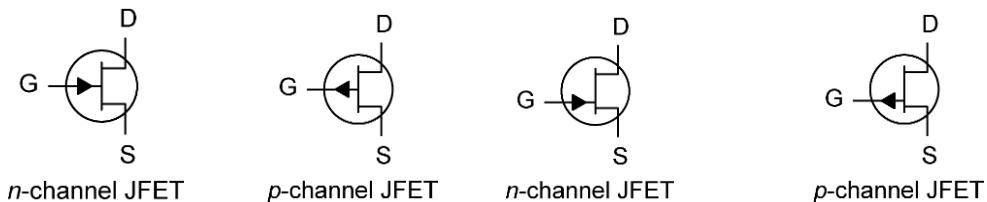
The two common families of FETs, the junction FET (JFET) and the metal oxide semiconductor FET (MOSFET) differ in the way the gate contact is made on the source-drain channel.

In the JFET the gate-channel contact is a reverse biased *pn* junction. The gate-channel junction of the JFET must always be reverse biased otherwise it may behave as a diode. All JFETs are depletion mode devices—they are *on* when the gate bias is zero ($V_{GS} = 0$).

In the MOSFET the gate-channel contact is a metal electrode separated from the channel by a thin layer of insulating oxide. MOSFETs have very good isolation between the gate and the channel, but the thin oxide is easily damaged (punctured!) by static discharge through careless handling. MOSFETs are made in both depletion mode (*on* with zero biased gate, $V_{GS} = 0$) and in enhancement mode (*off* with zero biased gate).

Schematic symbols. Two versions of the symbols are in common use (Fig.3.1). The first two symbols depict the source and drain as being symmetric. This is not generally true. Slight asymmetries are built into the channel during manufacturing which optimize the performance of the FET. Thus it is necessary to distinguish the source from the drain. The third and forth symbols show the differences between the drain and the source which depict the gate close to the source. The designation *n*-channel means that the channel is *n* doped and the gate is *p* doped. The *p*-channel is complement of *n*-channel.

Fig. 3.1



3.2 REGIONS OF JFET OPERATION:

Like the BJT, the FET can be operated in three regions:

Cut-off region: The transistor is off. There is no conduction between the drain and the source when the gate-source voltage is greater than the cut-off voltage. ($I_D = 0$ for $V_{GS} > V_{GS,off} = V_p$), V_p is the pinch-off voltage.

Active region (also called the Saturation region): The transistor is on. The drain current is controlled by the gate-source voltage (V_{GS}) and relatively insensitive to V_{DS} . In this region the transistor can be an amplifier.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS,off}} \right)^2$$

In the active region:

Ohmic region: The transistor is on, but behaves as a voltage controlled resistor. When V_{DS} is less than in the active region, the drain current is roughly proportional to the source-drain voltage and is controlled by the gate voltage.

$$I_D = I_{DSS} \left[2 \left(1 - \frac{V_{GS}}{V_{GS,off}} \right) \frac{V_{DS}}{V_{GS,off}} - \left(\frac{V_{DS}}{V_{GS,off}} \right)^2 \right]$$

$$R_{DS} \approx \frac{V_{GS,off}}{2I_{DSS}(V_{GS} - V_{GS,off})} = \frac{1}{g_m}$$

In the ohmic region:

3.2.1 Common Specifications.

I_{DSS} is the drain current in the active region for $V_{GS} = 0$. (I_D source shorted to gate)

$V_{GS,off}$ is the minimum V_{GS} where $I_D = 0$. $V_{GS,off}$ is negative for *n*-channel and positive for *p*-channel. g_m is the transconductance, the change in I_D with V_{GS} and constant V_{DS} .

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \Big|_{V_{DS}} = \frac{2I_{DSS}}{V_{GS,off}} (V_{GS} - V_{GS,off})$$

3.3 DC Bias

The general relationships that can be applied to the dc analysis of all FET amplifiers are that there is no gate current and Drain and Source current are the same. Thus:

$$I_G = 0 \text{ and } I_D = I_S$$

For JFETs and depletion-type MOSFETs and MESFETs, Shockley's equation is applied to relate the input and output quantities:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

For enhancement-type MOSFETs and MESFETs, the following equation is applicable

$$I_D = k(V_{GS} - V_T)^2$$

These equations do not change with each network configuration so long as the device is in the active region. The network simply defines the level of current and voltage associated with the operating point through its own set of equations. In reality, the dc solution of BJT and FET networks is the solution of simultaneous equations established by the device and the network. The solution can be determined using a mathematical or graphical approach. However, as noted earlier, the graphical approach is the most popular for FET networks and is employed here.

3.3 Fixed-Bias Configuration

The simplest of biasing arrangements for the n -channel JFET is shown in Fig. 3.2. This simple type of configuration can be solved directly using either a mathematical or a graphical approach. Both methods are included in this section to demonstrate the difference between the two methods and also to establish the fact that the same solution can be obtained using either approach.

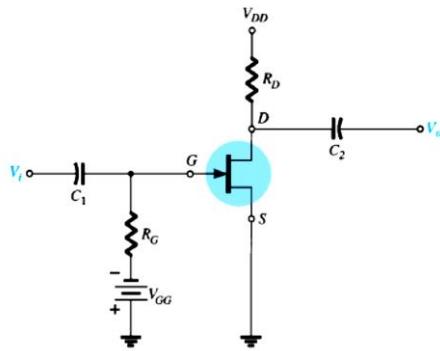


Fig 3.2 Fixed-Bias configuration

Since no current flows through the gate, it implies that $V_{GG}=V_{GS}$, and the writing KVL around the output, we have $V_{DD} = I_D R_D = V_{DS}$

3.4 Self-Bias Configuration

The self-bias configuration eliminates the need for two dc supplies. The controller gate-to-source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration as shown in Fig. 3.3

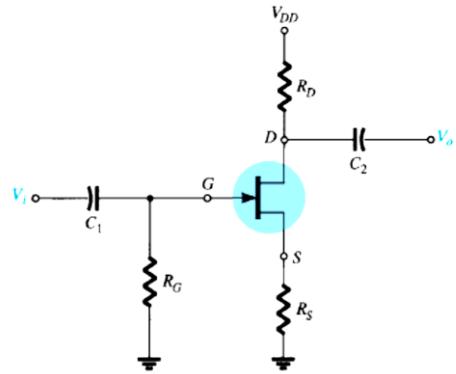


Fig. 3.3 JFET self-bias configuration

For the dc analysis, the capacitors can again be replaced by "open circuits" and the resistor R_G replaced by a short-circuit equivalent since $I_G = 0$ A. The result is the network of Fig. 3.4 for the important dc analysis.

The current through R_S is the source current I_S , but $I_S = I_D$ and

$$V_{RS} = I_D R_S$$

For the indicated closed loop of Fig. 6.9, we find that

$$-V_{GS} - V_{RS} = 0$$

And

$$V_{GS} = -V_{RS}$$

Or

$$V_{GS} = -I_D R_S$$

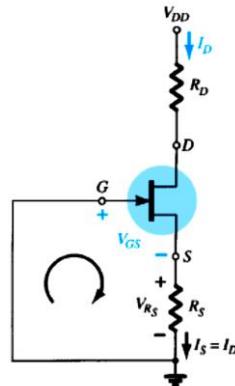


Fig. 3.4 DC analysis of the self-bias configuration

Note in this case that V_{GS} is a function of the output current I_D and not fixed in magnitude as occurred for the fixed-bias configuration.

A mathematical solution could be obtained from the equation as shown below:

$$\begin{aligned} I_D &= I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \\ &= I_{DSS} \left(1 - \frac{-I_D R_S}{V_P}\right)^2 \\ I_D &= I_{DSS} \left(1 + \frac{I_D R_S}{V_P}\right)^2 \end{aligned}$$

By performing the squaring process indicated and rearranging terms, an equation of the following form can be obtained:

$$I_D^2 + K_1 I_D + K_2 = 0$$

The quadratic equation can then be solved for the appropriate solution for I_D .

The sequence above defines the mathematical approach. The graphical approach requires that we first establish the device transfer characteristics as shown in Fig. 3.5. The relation defines a straight line on the same graph, let us now identify two points on the graph that are on the line and simply draw a straight line between the two points. The most obvious condition to apply is $I_D = 0$ A since it results in $V_{GS} = -I_D R_S = (0 \text{ A}) R_S = 0 \text{ V}$ (Fig. 3.10).

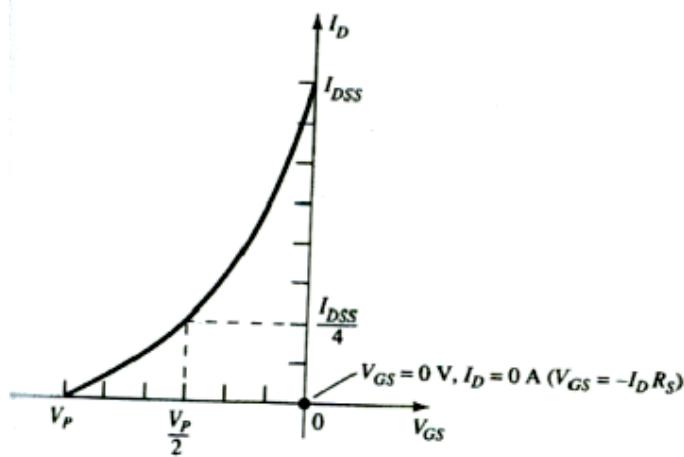


Fig. 3.5

Secondly it is required that a level of V_{GS} or I_D be chosen and the corresponding level of the other quantity be determined. The resulting levels of I_D and V_{GS} will then define another point on the

straight line and permit an actual drawing of the straight line. Suppose, for example, that we choose a level of I_D equal to one-half the saturation level. That is,

$$I_D = \frac{I_{DSS}}{2} \text{ and } V_{GS} = I_D R_S = -\frac{I_{DSS} R_S}{2}$$

The result is a second point for the straight-line plot as shown in Fig. 3.6. The straight line as shown is then drawn and the quiescent point obtained at the intersection of the straight line plot and the device characteristic curve. The quiescent values of I_D and V_{GS} can then be determined and used to find the other quantities of interest.

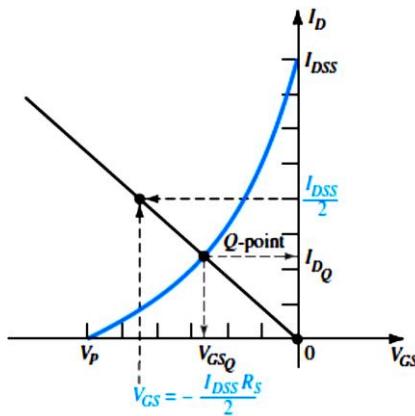


Fig. 3.6 V_{GS} vrs I_D

The level of V_{DS} can be determined by applying Kirchoff's voltage law to the output circuit, with the result that

$$\begin{aligned} V_{RS} + V_{DS} + V_{RD} - V_{DD} &= 0 \\ V_{DS} &= V_{DD} - V_{RS} - V_{RD} = V_{DD} - I_S R_S - I_D R_D \\ I_D &= I_S \\ V_{DS} &= V_{DD} - I_D (R_S + R_D) \\ V_S &= I_D R_S \\ V_G &= 0 V \\ V_D &= V_{DS} + V_S = V_{DD} - V_{RD} \end{aligned}$$

3.5 Voltage-Divider Biasing

The voltage-divider bias arrangement applied to BJT transistor amplifier is also applied to FET amplifiers as demonstrated by Fig. 3.7. The basic construction is exactly the same, but the dc analysis of each is quite different. $I_G = 0$ A for FET amplifiers, but the magnitude of I_B for common-emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits. Recall that I_B provided the link between input and output circuits for the BJT

voltage-divider configuration while V_{GS} will do the same for the FET configuration. Note that all the capacitors, including the bypass capacitor C_s , have been replaced by an "open-circuit" equivalent.

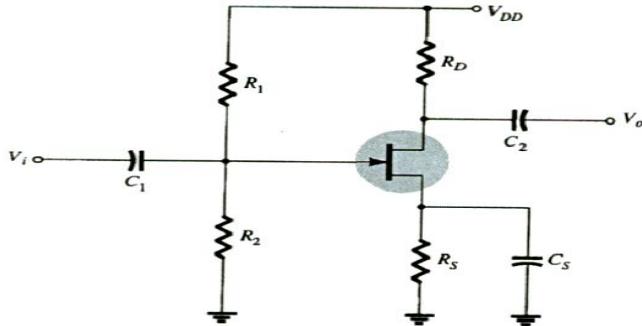


Fig. 3.7 Voltage-divider bias arrangement

Since $i_G = 0$, Kirchhoff's current law requires that $I_{R1} = I_{R2}$ and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G . The voltage V_G , equal to the voltage across R_2 , can be found using the voltage-divider rule as follows:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Applying Kirchhoff's voltage law in the clockwise direction to the indicated loop of Fig. 3.13 will result in

$$V_G - V_{GS} - V_{R_S} = 0$$

$$V_{GS} = V_G - V_{R_S}$$

By substitution

$$V_{R_S} = I_S R_S = I_D R_S$$

We have: $V_{GS} = V_G - I_D R_S$

The quantities V_G and R_S are fixed by the network construction. The procedure for plotting the load line is not a difficult one and will proceed as follows. Since any straight line requires two points to be defined, let us first use the fact that *anywhere on the horizontal axis* of Fig. 3.8 the current $I_D = 0$ mA. If we therefore select I_D to be 0 mA, we are in essence stating that we are somewhere on the horizontal axis. The exact location can be determined simply by substituting $I_D = 0$ mA into the equation below and finding the resulting value of V_{GS} as follows:

$$V_{GS} = V_G - I_D R_S$$

$$= V_G - (0 \text{ mA})R_S$$

$$V_{GS} = V_G|_{I_D=0 \text{ mA}}$$

The result specifies that whenever we plot the equation, if we choose $i_d = 0 \text{ mA}$, the value of V_{GS} for the plot will be v_g volts. The point just determined appears in Fig. 3.8.

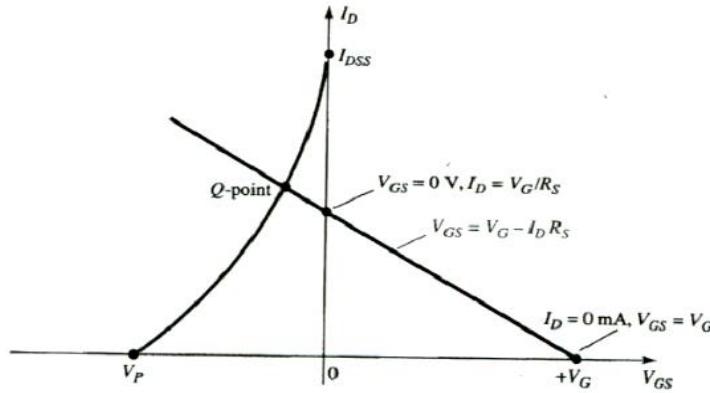


Fig. 3.8 Plot of I_D vrs V_{GS}

For the other point, let us now employ the fact that at any point on the vertical axis $V_{GS} = 0 \text{ V}$ and solve for the resulting value of I_D .

$$V_{GS} = V_G - I_D R_S$$

$$0 \text{ V} = V_G - I_D R_S$$

$$I_D = \frac{V_G}{R_S} \Big|_{V_{GS}=0 \text{ V}}$$

The result specifies that whenever we plot I_D and V_{GS} relation, if $V_{GS} = 0 \text{ V}$, the value of I_D can be determined from the intersection. The intersection of the straight line with the transfer curve in the region to the left of the vertical axis will define the operating point and the corresponding levels of I_D and V_{GS} .

Since the intersection on the vertical axis is determined by $i_d = V_G/R_s$ and v_g is fixed by the input network, increasing values of R_s will reduce the level of the I_D intersection as shown in Fig. 3.9. It is fairly obvious from Fig. 3.9 that:

Increasing values of R_s result in lower quiescent values of I_D and more negative values of V_{GS} .

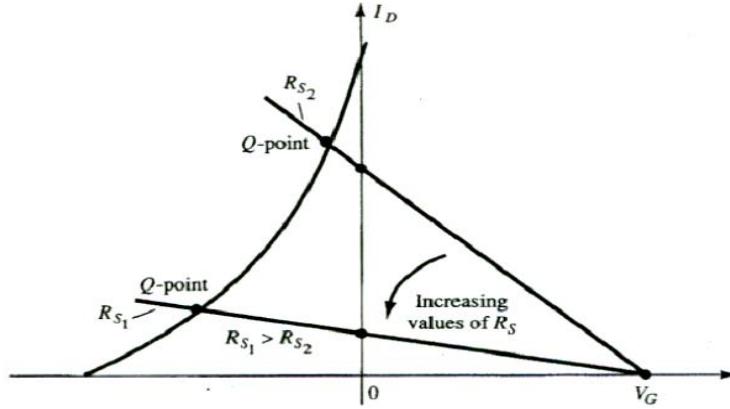


Fig. 3.9 Effect of R_S on the resulting Q -point

Once the quiescent values of I_{DQ} and V_{GSQ} are determined, the remaining network analysis can be performed in the usual manner. That is,

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = I_D R_S$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$$

Example 3.1 For the voltage-divider bias configuration of Fig. Q3.1, if $V_D = 12$ V and $V_{GSQ} = -2$ V, determine the value of R_S

Solution: V_G is determined as follows:

$$V_G = \frac{47 \text{ k}\Omega(16 \text{ V})}{47 \text{ k}\Omega + 91 \text{ k}\Omega} = 5.44 \text{ V}$$

$$I_D = \frac{V_{DD} - V_D}{R_D}$$

$$= \frac{16 \text{ V} - 12 \text{ V}}{1.8 \text{ k}\Omega} = 2.22 \text{ mA}$$

$$V_{GS} = V_G - I_D R_S$$

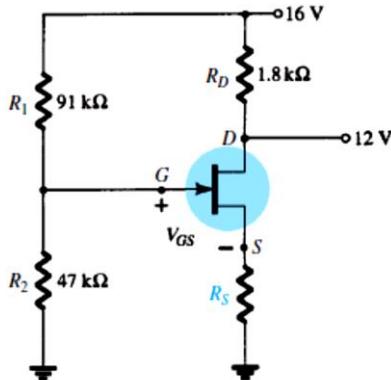


Fig. Q3.1

$$-2 \text{ V} = 5.44 \text{ V} - (2.22 \text{ mA})R_S$$

$$-7.44 \text{ V} = -(2.22 \text{ mA})R_S$$

$$R_S = \frac{7.44 \text{ V}}{2.22 \text{ mA}} = 3.35 \text{ k}\Omega$$

3.6 FET Small-Signal Model

The ac analysis of a FET configuration requires that a small-signal ac model for the FET be developed. A major component of the ac model will reflect the fact that an ac voltage applied to the input gate-to-source terminals will control the level of current from drain to source. Recall from previous discussions that a dc gate-to-source voltage controlled the level of dc drain current through a relationship known as Shockley's equation: $I_D = I_{DSS}(1-V_{GS}/V_P)^2$. The *change* in collector current that will result from a *change* in gate-to-source voltage can be determined using the transconductance factor g_m in the following manner:

$$\Delta I_D = g_m \Delta V_{GS}$$

where g_m is given as:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

If we therefore take the derivative of I_D with respect to V_{GS} (differential calculus) using Shockley's equation, we can derive an equation for g_m as follows:

$$\begin{aligned} g_m &= \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} \left[I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \right] \\ &= I_{DSS} \frac{d}{dV_{GS}} \left(1 - \frac{V_{GS}}{V_P} \right)^2 = 2I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right] \frac{d}{dV_{GS}} \left(1 - \frac{V_{GS}}{V_P} \right) \end{aligned}$$

$$= 2I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right] \left[\frac{d}{V_{GS}}(1) - \frac{1}{V_P} \frac{dV_{GS}}{dV_{GS}} \right] = 2I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right] \left[0 - \frac{1}{V_P} \right]$$

and

$$g_m = \frac{2I_{DSS}}{|V_P|} \left[1 - \frac{V_{GS}}{V_P} \right]$$

where $|V_P|$ denotes magnitude only, to ensure a positive value for g_m . It was mentioned earlier that the slope of the transfer curve is a maximum at $V_{GS} = 0$ V. Plugging in $V_{GS} = 0$ V into the equation above results in the following equation for the maximum value of g_m for a JFET in which I_{DSS} and V_P have been specified:

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

and hence g_m becomes:

$$g_m = g_{m0} \frac{2I_{DSS}}{|V_P|}$$

3.6.1 FET AC Equivalent Circuit

Now that the important parameters of an ac equivalent circuit have been introduced and discussed, a model for the FET transistor in the ac domain can be constructed. The control of I_d by V_{gs} is included as a current source $g_m V_{gs}$ connected from drain to source as shown in Fig. 3.10. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation.

$$i_d = g_m V_{gs} + \frac{V_{ds}}{r_d}$$

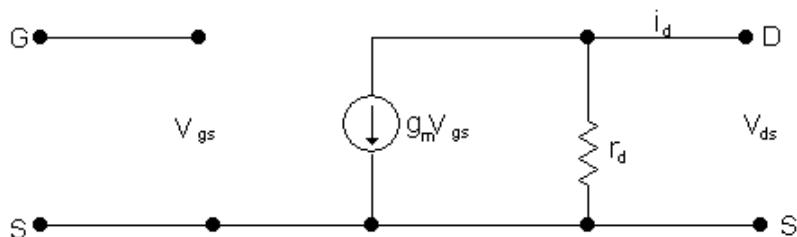


Fig. 3.10 FET AC equivalent circuit

The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor r_d from drain to source. Note that the gate to source voltage is now represented by V_{gs} (lower-case subscripts) to distinguish it from dc levels. In addition, take note of the fact that the source is common to both input and output circuits while the gate and drain terminals are only in "touch" through the controlled current source $g_m V_{gs}$.

In situations where r_d is ignored (assumed sufficiently large to other elements of the network to be approximated by an open circuit), the equivalent circuit is simply current source whose magnitude is controlled by the signal V_{gs} and parameter g_m . clearly a voltage-controlled device.

3.6.2 Fixed-Bias Configuration

Now that the JFET equivalent circuit has been defined, a number of fundamental JFET small-signal configurations are investigated. The approach parallels the ac analysis of BJT amplifiers with a determination of the important parameters of Z_i , Z_o , and A_v for each configuration.

The *fixed-bias* configuration of Fig. 3.11(a) includes the coupling capacitors C_1 and C_2 , which isolate the dc biasing arrangement from the applied signal and load; they act as short circuit equivalents for the ac analysis. The network of Fig. 3.11(b) is the ac small signal equivalent of the that of Fig. 3.11 Note the defined polarity of V_{gs} , which defines the direction of $g_m V_{gs}$. If V_{gs} is negative, the direction of the current source reverses. The applied signal is represented by V_i and the output signal across $R_D//r_d$ by V_o .

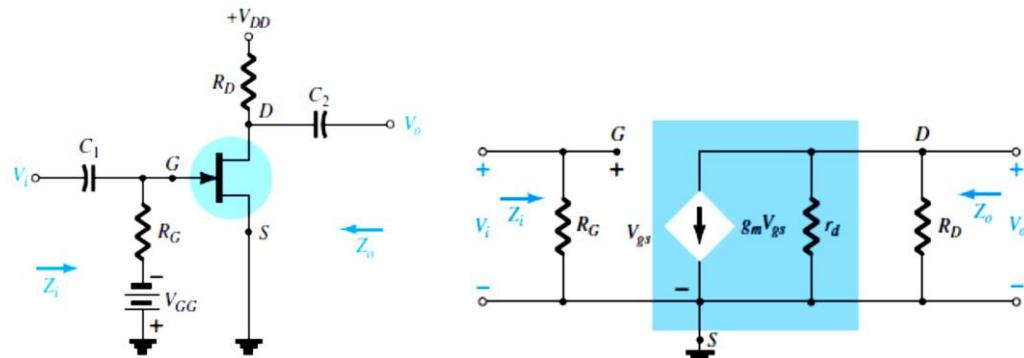


Fig. 3.11 (a) fixed-bias configuration (b) ac small signal equivalent

Input Impedance: Z_i

The input impedance is equal R_G to because of the infinite input impedance at the input terminals of the JFET thus: $Z_i = R_G$

Output Impedance: Z_o

Setting $V_i = 0$ V as required by the definition of Z_o will establish V_{gs} as 0 V also. The result is $g_m V_{gs} = 0$ mA, (short-circuited) and hence r_d and R_D will be in parallel. The output impedance is then: $Z_o = R_D // r_d$. If $r_d >> R_D$, thus about 10x greater, the $Z_o = R_D$

Voltage gain: A_v

Solving for V_o , we find,

$$V_o = -g_m V_{gs} (r_d \| R_D)$$

but

$$V_{gs} = V_i$$

and

$$V_o = -g_m V_i (r_d \| R_D)$$

so that

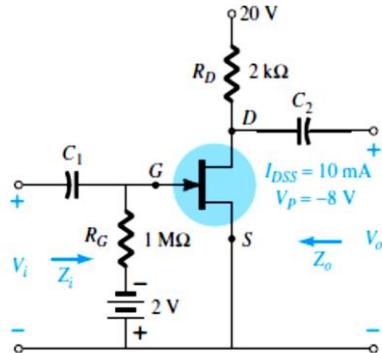
$$A_v = \frac{V_o}{V_i} = -g_m (r_d \| R_D)$$

If $r_d \geq 10R_D$

$$A_v = -g_m R_D$$

Example 3.2 The fixed-bias configuration of Fig. Q3.2 has an operating point defined by $V_{GSQ} = -2$ V and $I_{DQ} = 5.625$ mA, with $I_{DSS} = 10$ mA and $V_P = -8$ V. The value of y_{os} is provided as 40 mS.

- Determine g_m .
- Find r_d .
- Determine Z_i .
- Calculate Z_o .
- Determine the voltage gain A_v .
- Determine A_v ignoring the effects of r_d .



Solution

- a. $g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10 \text{ mA})}{8 \text{ V}} = 2.5 \text{ mS}$
 $g_m = g_{m0} \left(1 - \frac{V_{GSQ}}{V_P} \right) = 2.5 \text{ mS} \left(1 - \frac{(-2 \text{ V})}{(-8 \text{ V})} \right) = 1.88 \text{ mS}$
- b. $r_d = \frac{1}{y_{os}} = \frac{1}{40 \mu\text{S}} = 25 \text{ k}\Omega$
- c. $Z_i = R_G = 1 \text{ M}\Omega$
- d. $Z_o = R_D \parallel r_d = 2 \text{ k}\Omega \parallel 25 \text{ k}\Omega = 1.85 \text{ k}\Omega$
- e. $A_v = -g_m(R_D \parallel r_d) = -(1.88 \text{ mS})(1.85 \text{ k}\Omega)$
 $= -3.48$
- f. $A_v = -g_m R_D = -(1.88 \text{ mS})(2 \text{ k}\Omega) = -3.76$

3.6.3 Self-bias Configuration

Bypassed R_S

The fixed-bias configuration has the distinct disadvantage of requiring two dc voltage sources. The *self-bias* configuration of Fig. 3.12 requires only one dc supply to establish the desired operating point and A_v will be the same.

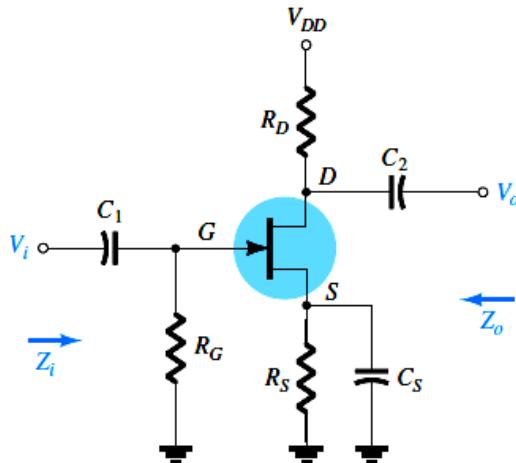


Fig. 3.12 Self-bias JFET configuration

The capacitor C_S across the source resistance assumes its open-circuit equivalence for dc, allowing R_S to define the operating point. Under ac conditions, the capacitor assumes the short-circuit state and “short circuits” the effects of R_S . The JFET equivalent circuit is as shown in Fig. 3.13. Since the resulting configuration is the same as appearing in Fig. 3.11, the resulting equations for Z_i , Z_o , and A_v will be the same.

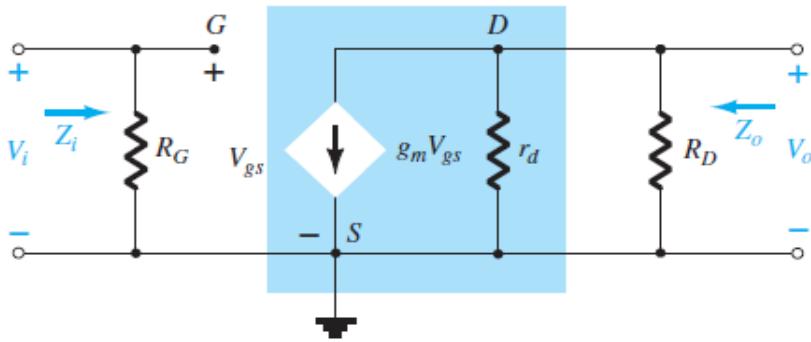


Fig 3.13 JFET ac equivalent circuit

The input impedance Z_i

$$Z_i = R_G$$

$$Z_0 = r_d || R_D$$

If $r_d \geq 10R_D$

$$Z_0 \cong R_D$$

$$A_V = -g_m(r_d || R_D)$$

$$\text{If } r_d \geq 10R_D, \quad A_V = -g_m R_D$$

Phase Relationship The negative sign in the solutions for A_V again indicates a phase shift of 180° between V_i and V_o .

Unbypassed R_S

If C_S is removed from Fig 3.12, the resistor R_S will be part of the ac equivalent circuit as shown in Fig. 8.18. In this case, there is no obvious way to reduce the network to lower its level of complexity. In determining the levels of Z_i , Z_o , and A_V , one must be very careful with notation and defined polarities and direction. Initially, the resistance r_d will be left out of the analysis to form a basis for comparison.

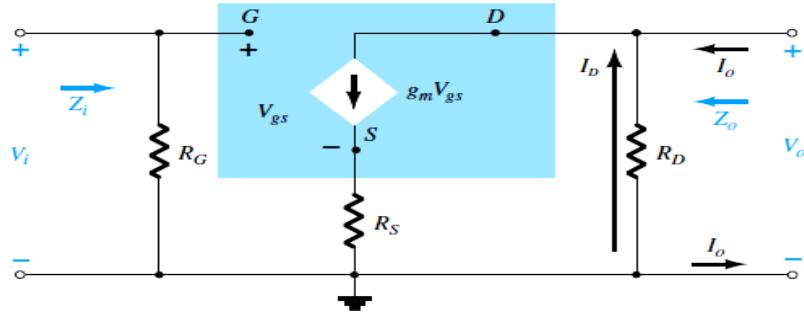


Fig. 3.14 Self-bias JFET configuration including the effects of R_S with

$$r_d = \infty \Omega$$

Input Impedance Z_i

Due to the open-circuit condition between the gate and the output network, the input remains the following:

$$Z_i = R_G$$

Output Impedance Z_o

The output impedance is defined by

$$Z_o = \left. \frac{V_o}{I_o} \right|_{V_i=0}$$

Setting $V_i = 0$ V in Fig. 3.14 results in the gate terminal being at ground potential (0 V). The voltage across R_G is then 0 V, and R_G has been effectively “shorted out” of the picture. Applying Kirchhoff's current law results in

$$I_o + I_D = g_m V_{gs}$$

$$\text{with, } V_{gs} = -(I_o + I_D)R_S$$

$$\text{So that } I_o + I_D = -g_m(I_o + I_D)R_S = -g_m I_o R_S - g_m I_D R_S$$

$$\text{or } I_o[1 + g_m R_S] = I_D[1 + g_m R_S]$$

$$\text{and } I_o = -I_D \quad (\text{the controlled current source } g_m V_{gs} = 0 \text{ A for applied conditions})$$

$$\text{since } V_o = -I_D R_D$$

$$\text{then } V_o = -(-I_o)R_D = I_o R_D$$

$$\text{and } Z_o = \left. \frac{V_o}{I_o} \right|_{r_d=\infty \Omega} = R_D$$

If r_d is included in the network, the equivalent will appear as shown in Fig. 3.15.

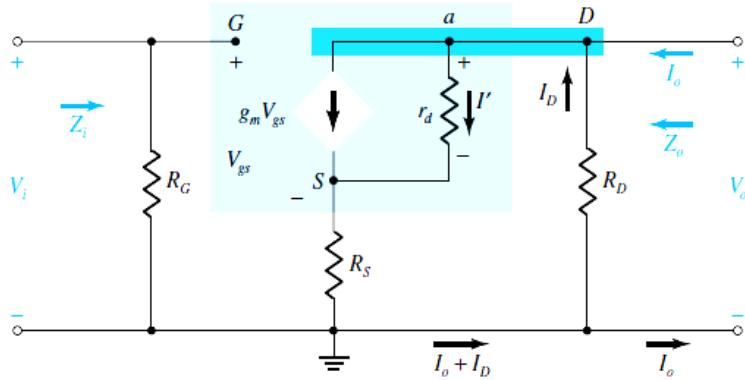


Fig. 3.15 Including the effects of r_d in the self-bias JFET configuration.

$$\text{since } Z_o = \left. \frac{V_o}{I_o} \right|_{V_i=0V} = -\frac{I_D R_D}{I_o}$$

We should try to find an expression for I_o in terms of I_D . Applying Kirchhoff's current law, we have

$$I_o = g_m V_{gs} + I_{rd} - I_D$$

$$\text{but } V_{rd} = V_o + V_{gs}$$

$$\text{and } I_o = g_m V_{gs} + \frac{V_o + V_{gs}}{r_d} - I_D$$

$$\text{or } I_o = \left(g_m + \frac{1}{r_d} \right) V_{gs} - \frac{I_D R_D}{r_d} - I_D \text{ using } V_o = -I_D R_D$$

$$\text{Now } V_{gs} = -(I_D + I_o)R_s$$

$$\text{so that } I_o = -\left(g_m + \frac{1}{r_d} \right) (I_D + I_o)R_s - \frac{I_D R_D}{r_d} - I_D$$

$$\text{with that result that } I_o \left(1 + g_m R_s + \frac{R_s}{r_d} \right) = -I_D \left(1 + g_m R_s + \frac{R_s}{r_d} + \frac{R_D}{r_d} \right)$$

$$\text{or } I_o = \frac{-I_D \left(1 + g_m R_s + \frac{R_s}{r_d} + \frac{R_D}{r_d} \right)}{\left(1 + g_m R_s + \frac{R_s}{r_d} \right)}$$

$$\text{and } Z_O = \frac{V_O}{I_O} = \frac{-I_D R_D}{\frac{-I_D \left(1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right)}{\left(1 + g_m R_S + \frac{R_S}{r_d}\right)}}$$

$$\text{and finally, } Z_O = \frac{\left(1 + g_m R_S + \frac{R_S}{r_d}\right)}{\left(1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right)} R_D$$

for $r_d \geq 10R_D$,

$$\left(1 + g_m R_S + \frac{R_S}{r_d}\right) \gg \frac{R_D}{r_d}$$

$$\text{and } 1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d} \cong 1 + g_m R_S + \frac{R_S}{r_d}$$

$$Z_O \cong R_D \quad r_d \geq 10R_D$$

Voltage Gain, A_v

For the network of Fig. 8.19, application of Kirchhoff's voltage law to the input circuit results in

$$V_i - V_{gs} - V_{RS} = 0$$

$$V_{gs} = V_i - I_D R_S$$

The voltage across r_d using Kirchhoff's voltage law is

$$V_{rd} = V_O - V_{RS}$$

$$\text{and } I' = \frac{V_{rd}}{r_d} - \frac{V_O - V_{RS}}{r_d}$$

so that application of Kirchhoff's current law results in

$$I_D = g_m V_{gs} + \frac{V_O - V_{RS}}{r_d}$$

Substituting for V_{gs} from above and substituting for V_O and V_{RS} , we have

$$I_D = g_m (V_i - I_D R_S) + \frac{(-I_D R_D) - (I_D R_S)}{r_d}$$

$$\text{so that } I_D \left[1 + g_m R_S + \frac{R_D + R_S}{r_d} \right] = g_m V_i$$

$$\text{or } I_D = \frac{g_m V_i}{\left[1 + g_m R_S + \frac{R_D + R_S}{r_d} \right]}$$

$$\text{The output voltage is then } V_o = -R_D I_D = -\frac{g_m R_D V_i}{\left[1 + g_m R_S + \frac{R_D + R_S}{r_d} \right]}$$

$$\text{and } A_V = \frac{V_o}{V_i} = -\frac{g_m R_D}{\left[1 + g_m R_S + \frac{R_D + R_S}{r_d} \right]}$$

$$\text{Again, } r_d \geq 10(R_D + R_S),$$

$$\text{and } A_V = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S} \Big|_{r_d \geq 10(R_D + R_S)}$$

Phase Relationship

The negative sign in reveals that a 180° phase shift will exist between V_i and V_o .

Example 3.3. The self-bias configuration of Example 3.2 has an operating point defined by $V_{GSQ} = -2.6$ V and $I_{DQ} = 2.6$ mA, with $I_{DSS} = 8$ mA and $V_P = -6$ V. The network is redrawn as Fig. 3.3 with an applied signal V_i . The value of g_{os} is given as 20 mS.

- Determine g_m .
- Find r_d .
- Find Z_i .
- Calculate Z_o with and without the effects of r_d . Compare the results.
- Calculate A_V with and without the effects of r_d . Compare the results.

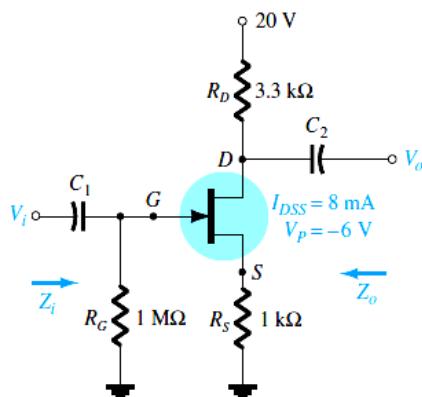


Fig. Q3.3

Solution:

$$\text{a. } g_{mo} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8mA)}{6V} = 2.67mS$$

$$g_m = g_{mo} \left(1 - \frac{V_{GSQ}}{|V_P|}\right) = 2.67mS \left(1 - \frac{(-2.6V)}{(-6V)}\right) = 1.51mS$$

$$\text{b. } r_d = \frac{1}{y_{os}} = \frac{1}{20\mu S} = 50k\Omega$$

$$\text{c. } Z_i = R_G = 1M\Omega$$

$$\text{d. With } r_d, \quad r_d = 50k\Omega > 10R_D = 33k\Omega$$

$$\text{therefore } Z_o = R_D = 3.3k\Omega$$

$$\text{if } r_d = \infty\Omega, \quad Z_o = R_D = 3.3k\Omega$$

$$\text{e. With } r_d,$$

$$\begin{aligned} A_V &= -\frac{g_m R_D}{\left[1 + g_m R_S + \frac{R_D + R_S}{r_d}\right]} = \frac{-(1.51mS)(3.3k\Omega)}{1 + (1.51mS)(1k\Omega) + \frac{3.3k\Omega + 1k\Omega}{50k\Omega}} \\ &= -1.92 \end{aligned}$$

With $r_d = \infty\Omega$ (open-circuit equivalence),

$$A_V = -\frac{g_m R_D}{1 + g_m R_S} = \frac{-(1.51mS)(3.3k\Omega)}{1 + (1.51mS)(1k\Omega)} = -1.98$$

3.6.4 Voltage-Divider Configuration

The popular voltage-divider configuration for BJTs can also be applied to JFETs as demonstrated in Fig. 3.16.

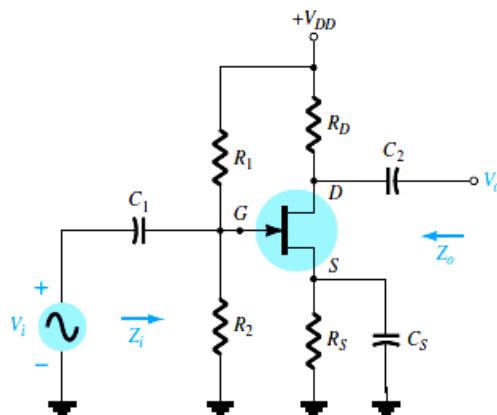


Fig. 3.16 JFET voltage-divider

Substitute the ac equivalent model for the JFET results in the configuration of Fig. 3.16. Replacing the dc supply V_{DD} by a short-circuit equivalent has grounded one end of R_1 and R_D . Since each network has a common ground, R_1 can be brought down in parallel with R_2 as shown in Fig. 3.17. R_D can also be brought down to ground, but in the output circuit across r_d . The resulting ac equivalent network now has the basic format of some of the networks already analyzed.

Input Impedance Z_i

R_1 and R_2 are in parallel with the open-circuit equivalence of the JFET, resulting in

$$Z_i = R_1 \parallel R_2$$

Output Impedance Z_o

Setting $V_i = 0$ V sets V_{GS} and $g_m V_{GS}$ to zero, and

$$Z_o = r_d \parallel R_D$$

for $r_d \geq 10R_D$

$$Z_o \cong R_D$$

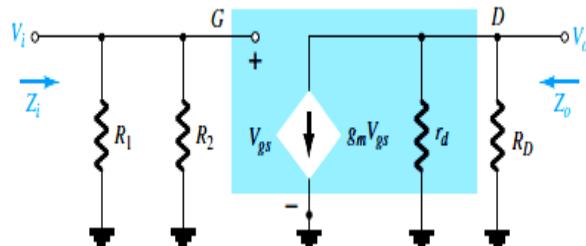


Fig. 3.17 ac equivalent circuit of Fig. 3.16

Calculating Av;

$$V_{GS} = V_i$$

$$V_o = -g_m V_{GS} (r_d \parallel R_D)$$

$$A_V = \frac{V_o}{V_i} = \frac{-g_m V_{GS} (r_d \parallel R_D)}{V_{GS}}$$

$$\text{and } A_V = \frac{V_o}{V_i} = -g_m (r_d \parallel R_D)$$

for $r_d \geq 10R_D$

$$A_V = \frac{V_o}{V_i} \cong -g_m R_D$$

Note that the equations for Z_o and A_v are the same as obtained for the fixed-bias and self-bias (with bypassed R_S) configurations. The only difference is the equation for Z_i , which is now sensitive to the parallel combination of R_I and R_2 .

CHAPTER 4: OP-AMP BASICS AND APPLICATIONS

4.0 Introduction

The operational amplifier is one of the most useful and important components of analog electronics. They are widely used in popular electronics. Their primary limitation is that they are not especially fast: The typical performance degrades rapidly for frequencies greater than about 1 MHz, although some models are designed specifically to handle higher frequencies.

The primary use of op-amps in amplifier and related circuits is closely connected to the concept of negative feedback. Feedback represents a vast and interesting topic in itself. We will discuss it in rudimentary terms a bit later. However, it is possible to get a feeling for the two primary types of amplifier circuits, inverting and non-inverting amplifiers, by simply postulating a few simple rules (the “golden rules”). We will start in this way, and then go back to understand their origin in terms of feedback.

4.1 The Ideal Op-Amp

The ideal op-amp Fig.4.1 aspires to have the following properties:

- ***Infinite power:*** Infinite power is unrealistic, but there are hi-powered amplifiers with more power than is actually required. Therefore, power is not limitation. In a past era when only valve amplifiers existed, power was a limitation.
- ***Infinite gain:*** this is not necessary for any audio application. The maximum gain normally required may be 100. Cheap op-amps are capable of a gain of 1 million. Special op-amps can be much higher.
- ***Infinite bandwidth:*** this is also un-necessary for applications such as audio, since the audio frequency spectrum is from 20Hz to 20 kHz. The cheapest op-amp is capable of 1MHz. special op-amps however can go higher than 100MHz.
- ***Infinitely high input impedance:*** in common applications such as audio, a high input impedance of 1M Ohm is sometimes required. Special op-amps can however achieve input impedance 100M Ohm and higher.
- ***Infinitely low output impedance:*** this is achievable, but is rarely required in applications such as audio. It is even possible to make an op-amp achieve negative output impedance
- ***Infinitely low distortion:*** op-amps can attain distortion figures that are magnitudes below what is audibly detectable.

- **Infinitely low noise:** the lowest noise is thermionic electron noise of the components limited by the laws of physics.
- **Zero output Impedance:** The output impedance appreciable very low and thus can be approximated as zero.

These ideals can be summarized as;

- I. The output attempts to minimize the differential input.
- II. The inputs draw no current. Thus;

$$I_p = I_n = 0$$

$$R_i = \infty$$

$$R_o = 0$$

$$V_n = V_p$$

$$A \rightarrow \infty$$

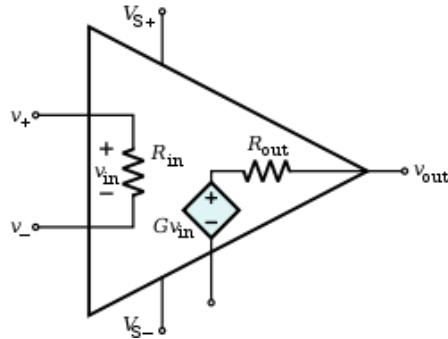


Fig. 4.1: Operational Amplifiers

The operational amp consists of among others three main amplifier stages; the differential, buffer and an output stage. The differential amplifier stage is shown in Fig. 4.2.

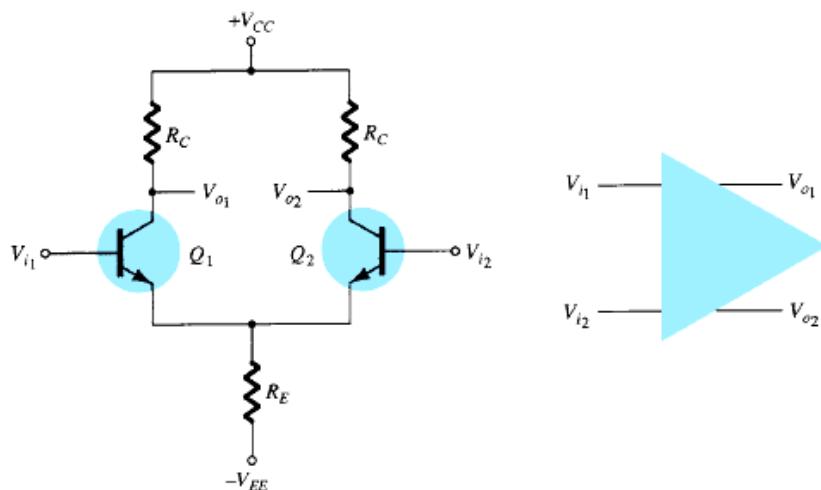


Fig. 4.2: Basic differential amplifier circuit.

The two transistors making up of the differential amplifier must be well matched; thus

$$\beta_1 = \beta_2, \quad I_{b1} = I_{b2} \text{ and } V_{BE1} = V_{BE2}$$

If an input signal is applied to either input with the other input connected to ground, the operation is referred to as “single-ended.”

If two opposite-polarity input signals are applied, the operation is referred to as “double-ended.”

If the same input is applied to both inputs, the operation is called “common-mode.”

The modes of operation

- Differential mode $V_d = V_1 - V_2$
- Common mode $V_{cm} = \frac{1}{2}(V_1 + V_2)$
- Single mode $V_1 = 0 \text{ or } V_2 = 0$

In single-ended operation, a single input signal is applied. However, due to the common emitter connection, the input signal operates both transistors, resulting in output from *both* collectors.

In double-ended operation, two input signals are applied, the difference of the inputs resulting in outputs from both collectors due to the difference of the signals applied to both inputs.

In common-mode operation, the common input signal results in opposite signals at each collector, these signals canceling, so that the resulting output signal is zero. As a practical matter, the opposite signals do not completely cancel, and a small signal results.

The main feature of the differential amplifier is the very large gain when opposite signals are applied to the inputs as compared to the very small gain resulting from common inputs. The ratio of this difference gain to the common gain is called *common-mode rejection*

4.1.1 Double-Ended (Differential) Input

In addition to using only one input, it is possible to apply signals at each input: this being a double-ended operation. Fig. 4.3 shows an input, V_d , ($V_{i1} - V_{i2}$) applied between the two input terminals (recall that neither input is at ground), with the resulting amplified output in phase with that applied between the plus and minus inputs.

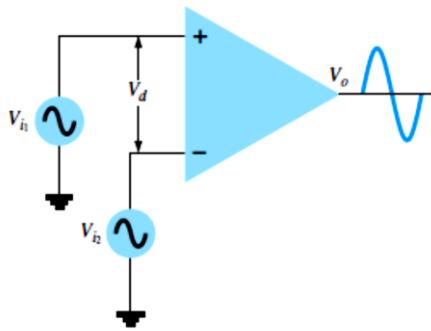


Fig. 4.3: Double-ended (differential) operation

4.1.2 Common-Mode Operation

When the same input signals are applied to both inputs, common-mode operation results, as shown in Fig. 4.4. Ideally, the two inputs are equally amplified, and since they result in opposite-polarity signals at the output, these signals cancel, resulting in 0-V output. Practically, a small output signal will result.

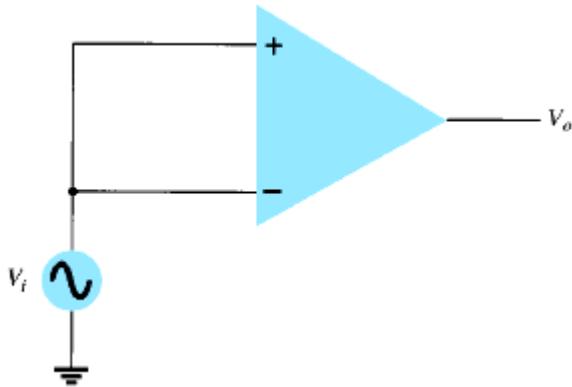


Fig. 4.4: Common-mode operation.

4.1.3 Single-ended operation

Single-ended input operation results when input signal is connected to one input with the other input connected to ground (Fig. 4.5). Any of the input can be grounded resulting in the output having the same polarity as the input or opposite depending on which input is used.

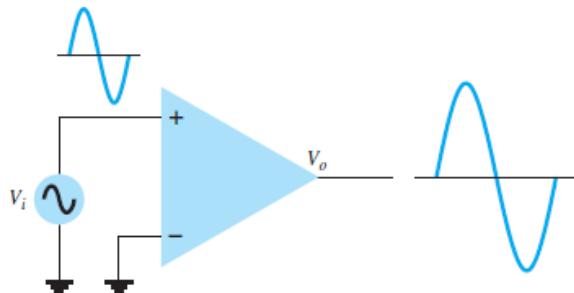


Fig. 4.5: Single-ended operation

4.2 DC operation and Small signal analysis:

In this analysis the T-model of what is usually referred to as the re-model is used. We consider first the differential mode, the common mode and then the single-ended mode.

4.2.1: Differential mode

DC Bias

Let's first consider the dc bias operation of the circuit of Fig. 4.6 . With ac inputs obtained from voltage sources, the dc voltage at each input is essentially connected to 0 V, as shown

$$V_E = 0 \text{ V} - V_{BE} = -0.7 \text{ V}$$

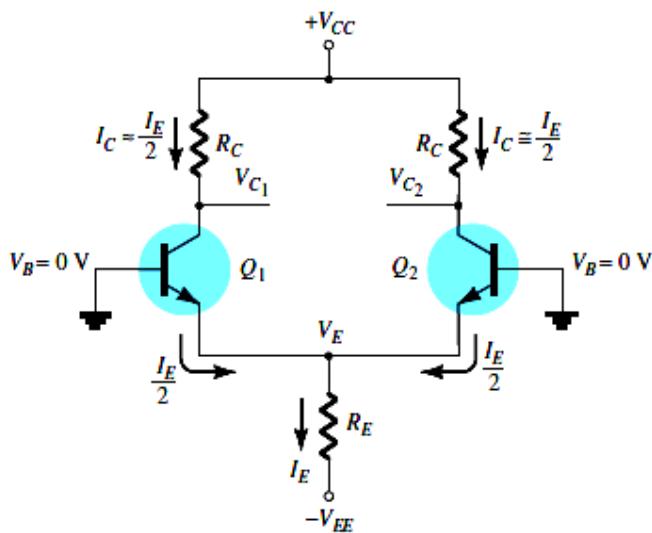


Fig. 4.6: DC bias of differential amplifier circuit.

The emitter dc bias current is then

$$I_E = \frac{V_E - (-V_{EE})}{R_E} \approx \frac{V_{EE} - 0.7V}{R_E}$$

Assuming that the transistors are well matched (as would occur in an IC unit), we obtain

$$I_{C1} = I_{C2} = \frac{I_E}{2}$$

resulting in a collector voltage of

$$V_{C1} = V_{C2} = V_{CC} - I_C R_C \frac{I_E}{2} R_c$$

EXAMPLE 4.1 Calculate the dc voltages and currents in the circuit of Fig. 4.7

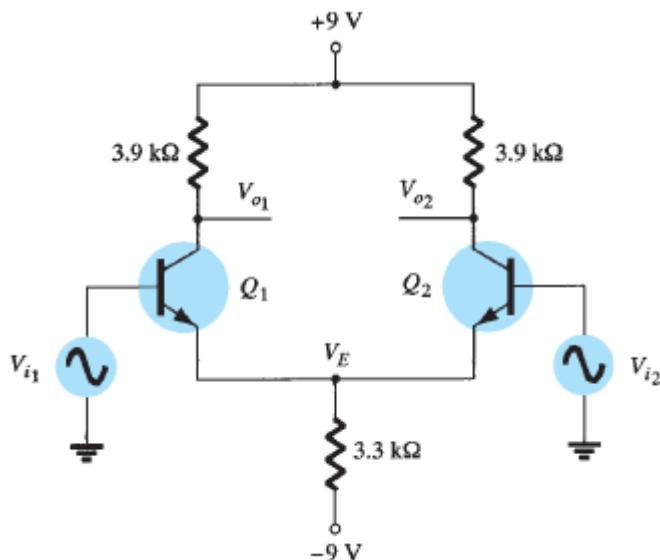


Fig. 4.7: Differential amplifier circuit for Example 4.1

Solution:

$$I_E = \frac{V_{EE} - 0.7V}{R_E} = \frac{9V - 0.7V}{3.3k\Omega} \approx 2.5 \text{ mA}$$

The collector current is then

$$I_C = \frac{I_E}{2} = \frac{2.5 \text{ mA}}{2} = 1.25 \text{ mA}$$

resulting in a collector voltage of

$$V_C = V_{CC} - I_C R_C = 9V - (1.25mA)(3.9k\Omega)$$

The common-emitter voltage is thus -0.7 V, whereas the collector bias voltage is near 4.1 V for both outputs.

Small Signal Analysis (AC Operation of Circuit)

An ac connection of a differential amplifier is shown in Fig. 4.8. Separate input signals are applied as V_{i1} and V_{i2} , with separate outputs resulting as V_{o1} and V_{o2} . To carry out ac analysis, we redraw the circuit in Fig. 4.9. Each transistor is replaced by its ac equivalent.

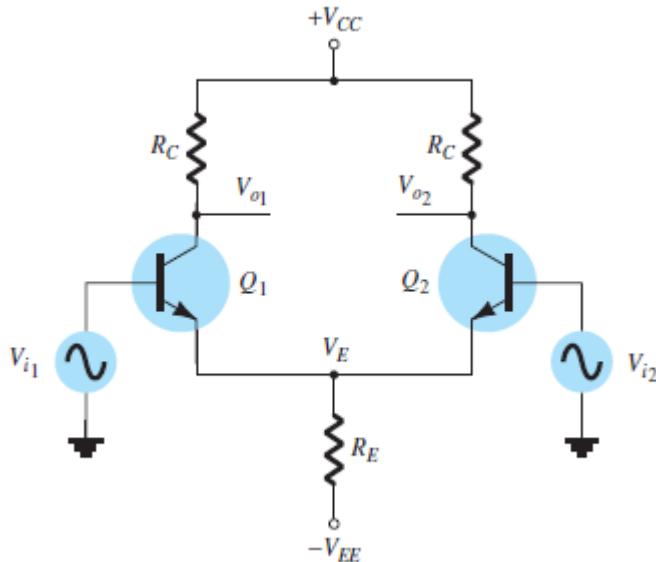


Fig. 4.8: AC connection of differential amplifier.

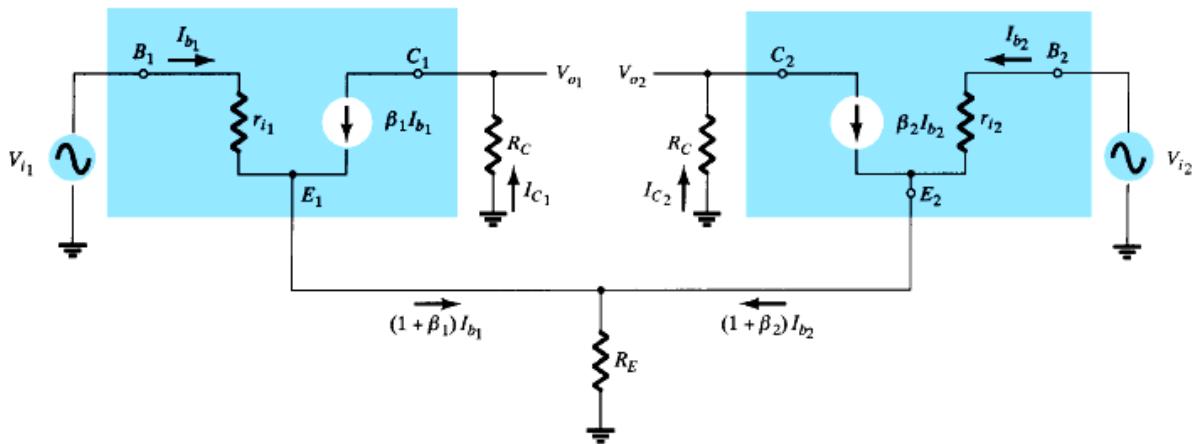


Fig. 4.9: AC equivalent of differential amplifier circuit.

In this particular circuit the output can be taken from any of the two outputs. Here we show that for the condition of signals applied to both inputs, the differential voltage gain magnitude is

$$A_d = \frac{V_o}{V_i} = \frac{R_c}{r_e}$$

$$\text{where } V_d = V_{i1} - V_{i2}$$

Consider the loop from V_{i1} through $B_1E_1E_2B_2$ to V_{i2} , we can write

$$V_{i1} = \beta r_{e1} I_{b1} + \beta r_{e2} (I_{b1} - I_{b2}) + V_{i2}$$

$$V_{i1} - V_{i2} = \beta r_{e1} I_{b1} + \beta r_{e2} (I_{b1} - I_{b2})$$

Since $I_{b1} = I_{b2} = I_b$ and $r_{e1} = r_{e2} = r_e$

$$\text{Therefore } V_{i1} - V_{i2} = \beta r_{e1} I_b$$

$$V_o = I_C R_C \quad ; \quad I_C = \beta I_b$$

$$V_o = \beta I_b R_C$$

Then

$$A_d = \frac{V_o}{V_d} = \frac{\beta I_b R_C}{\beta r_{e1} I_b} = \frac{R_C}{r_e}$$

4.2.2: Common-Mode Operation of Circuit

Whereas a differential amplifier provides large amplification of the difference signal applied to both inputs, it should also provide as small an amplification of the signal common to both inputs. An ac connection showing common input to both transistors is shown in Fig. 4.10. The ac equivalent circuit is drawn in Fig. 4.11, from which we can write

$$V_i = I_b \beta r_e + R_E I_E$$

$$I_E = (\beta + 1) I_b + (\beta + 1) I_b$$

$$I_E = 2(\beta + 1) I_b$$

$$V_i = I_b \beta r_e + R_E [2(\beta + 1) I_b]$$

Since β is large, $\beta + 1 \approx \beta$

$$V_i = I_b \beta r_e + R_E [2\beta I_b] \quad ; \quad V_i = I_b \beta r_e + 2I_b R_E$$

$$V_o = I_C R_C \quad ; \quad I_C = \beta I_b$$

$$V_o = \beta I_b R_C$$

$$A_d = \frac{V_o}{V_i} = \frac{\beta I_b R_C}{I_b \beta r_e + 2 I_b R_E} = \frac{R_C}{r_e + 2 R_E}$$

OR

$$I_b = \frac{V_i - 2(\beta + 1)I_b R_E}{r_i}$$

Which can be rewritten as

$$I_b = \frac{V_i}{r_i + 2(\beta + 1)R_E}$$

The output voltage is then

$$V_o = I_C R_C = \beta I_b R_C = \frac{\beta V_i R_C}{r_i + 2(\beta + 1)R_E}$$

providing a voltage gain of

$$A_d = \frac{V_o}{V_i} = \frac{\beta R_C}{r_i + 2(\beta + 1)R_E}$$

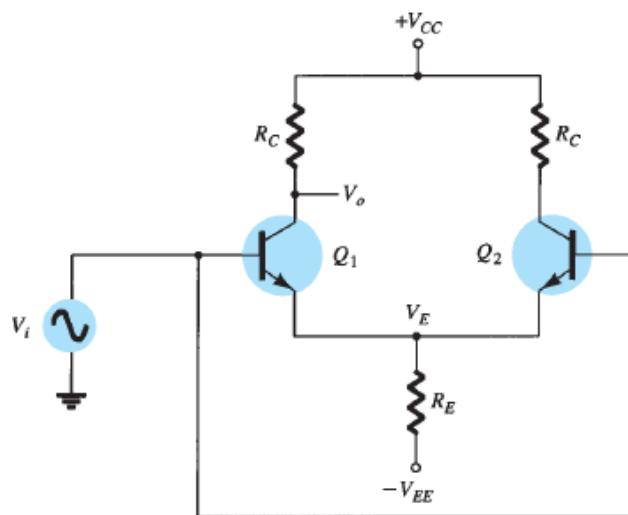


Fig. 4.10: Common-mode connection.

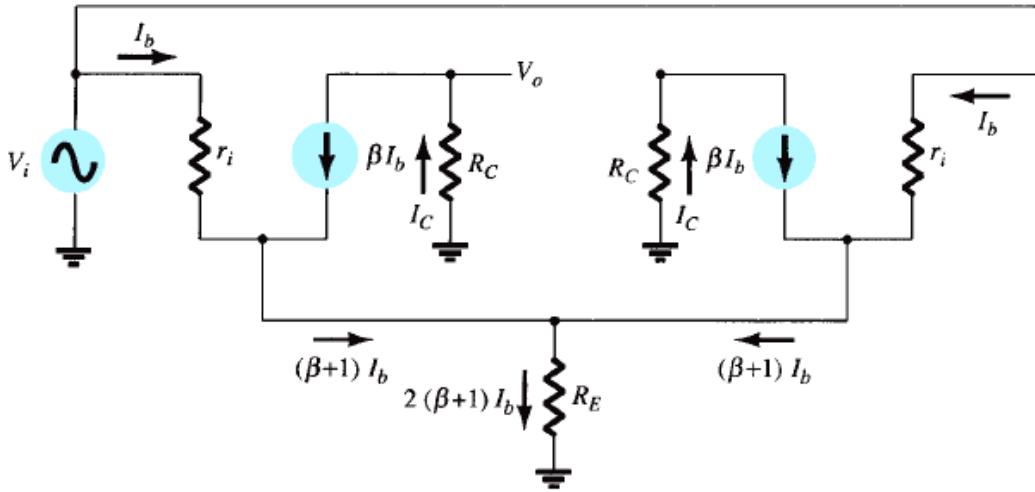


Fig. 4.11: AC circuit in common-mode connection.

4.2.3 Single-ended mode of operation

To calculate the single-ended ac voltage gain, $V_o > V_i$, apply signal to one input with the other connected to ground, as shown in Fig. 4.12. The ac equivalent of this connection is drawn in Fig. 4.13.

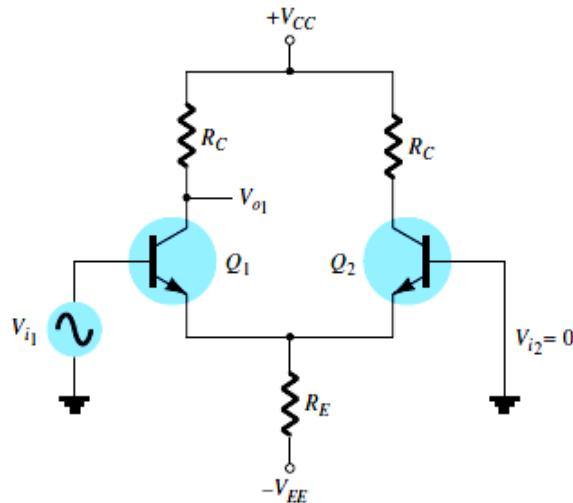


Fig. 4.12 Single-ended operation

The ac base current can be calculated using the base 1 input Kirchhoff voltage loop (KVL) equation.

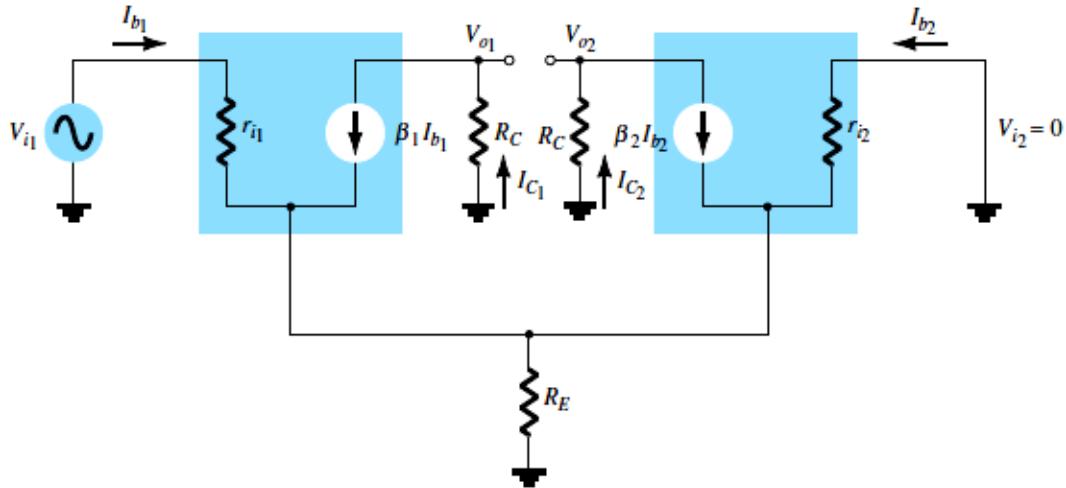


Fig 4.13. AC equivalent of circuit in Fig. 10.14

If one assumes that the two transistors are well matched, then

$$I_{b1} = I_{b2} = I_b \text{ and } r_{i1} = r_{i2} = r_i = \beta r_e$$

With R_E very large (ideally infinite), the circuit for obtaining the KVL equation simplifies to that of Fig. 4.15, from which we can write

$$V_{i1} - I_b r_i - I_b r_i = 0$$

so that

$$I_b = \frac{V_{i1}}{2r_i} = \frac{V_i}{2\beta r_e}$$

If we also assume that

$$\beta_1 = \beta_2 = \beta$$

then

$$I_C = \beta I_b = \beta \frac{V_i}{2\beta r_e} = \frac{V_i}{2r_e}$$

And the output voltage at either collector is

$$V_o = I_C R_C = \frac{V_i}{2r_e} R_C = \frac{R_C}{2r_e} V_i$$

For which the single-ended voltage gain A_v at either collector is

$$A_v = V_o / V_i = \frac{R_C}{2r_e}$$

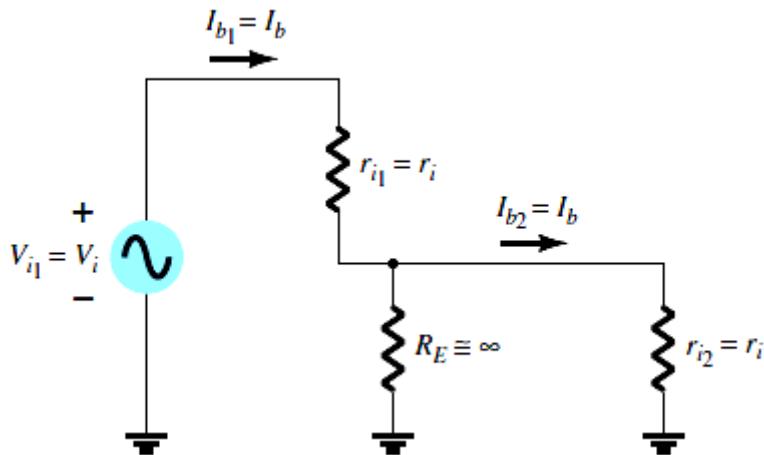


Fig. 4.15 Partial circuit for calculating I_b

4.3 The Golden Rules

The op-amp is in essence a differential amplifier of the type we discussed in above with other refinements (buffer stage, current source load, follower output stage), plus more, all nicely debugged, characterized, and packaged for use. Examples are the 741 and 411 models. These two differ most significantly in that the 411 uses JFET transistors at the inputs in order to achieve a very large input impedance ($Z_{in} \sim 10^9$), whereas the 741 is an all-bipolar design ($Z_{in} \sim 10^6$).

The other important fact about op-amps is that their *open-loop gain* is huge. This is the gain that would be measured from a configuration like Fig. 4.16, in which there is no feedback loop from output back to input. A typical open-loop voltage gain is $\sim 10^4\text{-}10^5$. By using negative feedback, we throw most of that away! We will soon discuss why, however, this might actually be a smart thing to do.

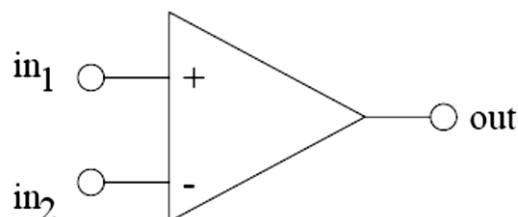


Fig. 4.16: Operational Amplifiers

The golden rules are idealizations of op-amp behavior, but are nevertheless very useful for describing overall performance. They are applicable whenever op-amps are configured with

negative feedback, as in the two amplifier circuits discussed below. These rules consist of the following two statements:

1. The voltage difference between the inputs, V_+ and $V_-(X)$, is zero.

(Negative feedback will ensure that this is the case.)

2. The inputs draw no current.

(This is true in the approximation that the Z_{in} of the op-amp is much larger than any other current path available to the inputs.) When we assume ideal op-amp behavior, it means that we consider the golden rules to be exact. We now use these rules to analyze the two most common op-amp configurations.

How to solve Op-amp circuits:

1) Replace the Op-amp with its circuit model.

2) Check for negative feedback (connection from output to the inverting terminal), if so, write down $V_p \approx V_n$.

3) Solve. Best method is usually node-voltage method. You can solve simple circuits with KVL and KCLs. Do not use mesh-current method.

4.4 Op amp inverting amplifier

The basic circuit for an inverting amplifier is shown in Fig. 4.17 where the input voltage V_o , (a.c or d.c) to be amplified is applied via resistor R_i to the inverting (-) terminal; the output voltage V_o is therefore in anti-phase with the input. The non-inverting (+) terminal is held at 0V. Negative feedback is provided by the feedback resistor R_f , feeding back a certain fraction of the output voltage to the inverting terminal.

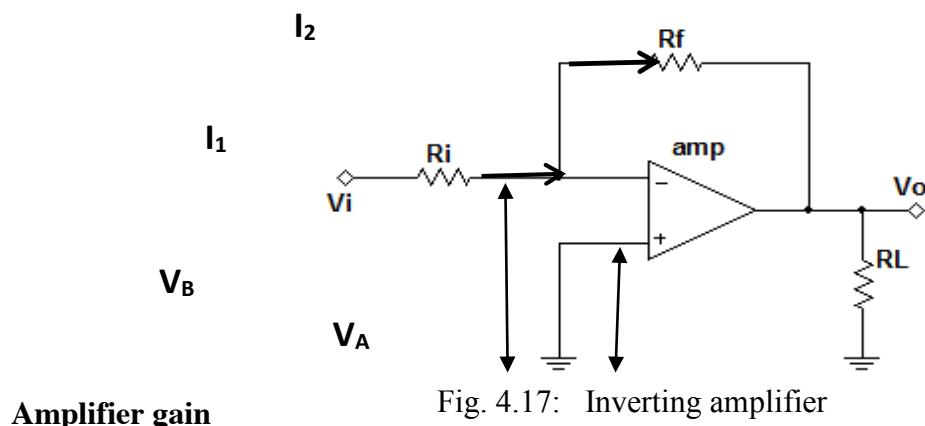


Fig. 4.17: Inverting amplifier

In an **ideal op amp** two assumptions are made, these being that:

- (i) Each input draws zero current from the signal source, i.e. their input impedance's are infinite, and
- (ii) The inputs are both at the same potential if the op amp is not saturated, i.e. $V_A = V_B$ in Fig. 4.17

In Fig. 4.17, $V_+ = 0$, hence $V_- = 0$ and point (V_+ to V_-) is called a **virtual earth**. Thus,

$$I_1 = \frac{V_i - 0}{R_i}$$

And

$$I_1 = \frac{0 - V_o}{R_f}$$

However, $I_1 = I_2$ (from the ideal amplifier assumptions).

$$\text{Hence } \frac{V_i}{R_i} = -\frac{V_o}{R_f}$$

The negative sign showing that V_o is negative when V_i is positive, and vice versa. The **closed-loop gain A** is given by:

$$A = \frac{V_o}{V_i} = -\frac{R_f}{R_i}; \quad V_o = -\frac{R_f}{R_i} V_i$$

This shows that the gain of the amplifier depends only on the two resistors, which can be made with precise values, and not on the characteristics of the op amp, which may vary from sample to sample. For example, if $R_i = 10k\Omega$ and $R_f = 1000k\Omega$ then the closed-loop gain,

$$A = -\frac{R_f}{R_i} = \frac{1000 \times 10^3}{10 \times 10^3} = -100$$

Thus an input of 10mV will cause an output change of 1V.

Example 4.3: In the inverting amplifier of Fig. 4.17, $R_i = 1 k\Omega$ and $R_f = 5 k\Omega$. Determine the output voltage when the input voltage is:

- (a) +0.4V
- (b) -1.2V.

Solution

From equation above,

$$\frac{V_o}{V_i} = -\frac{R_f}{R_i}; \quad V_o = -\frac{R_f}{R_i} V_i$$

(a) When $V_i = +0.4V$,

$$V_o = -\frac{5000}{1000} * (+0.5) = -2.5$$

Example 4.4: The op amp shown in Fig. Q4.4 has an input bias current of 100 nA at 20 °C. Calculate

(a) The voltage gain, and (b) the output offset voltage due to the input bias current. (c) How can the effect of input bias current be minimised?

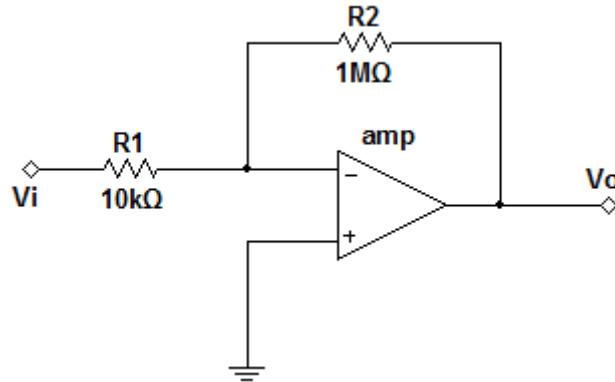


Fig. Q4.4

Fig. 3.16

Comparing Fig. 4.17 with Fig. Q4.4, gives $R_i = 10k\Omega$ and $R_f = 1M\Omega$

(a) **Voltage gain,**

$$A = -\frac{R_f}{R_i}$$

$$= -\frac{1 \times 10^6}{10 \times 10^3} = -100$$

(b) The input bias current, I_B causes a volt drop across the equivalent source impedance seen by the op amp input, in this case, R_i and R_f in parallel. Hence, the offset voltage, V_{OS} at the input due to the 100nA input bias current, I_B is given by:

$$V_{OS} = I_B$$

$$\begin{aligned} V_{OS} &= I_B \left(\frac{R_i R_f}{R_i + R_f} \right) \\ &= (100 \times 10^{-9}) \left(\frac{10 \times 10^3 \times 1 \times 10^6}{(10 \times 10^3) + (1 \times 10^6)} \right) \\ &= (10^{-7})(9.9 \times 10^3) = 9.9 \times 10^{-4} \\ &= \mathbf{0.99 \text{ mV}} \end{aligned}$$

(c) The effect of input bias current can be minimised by ensuring that both inputs ‘see’ the same driving resistance. This means that a resistance of value of $9.9\text{ k}\Omega$ (from part (b)) should be placed between the non-inverting (+) terminal and earth in Fig. Q4.4

Example 4.5. Design an inverting amplifier to have a voltage gain of 40 dB, a closed-loop bandwidth of 5 kHz and an input resistance of $10\text{ k}\Omega$.

The voltage gain of an op amp, in decibels, is given by:

$$\text{Gain in decibels} = 20 \log 10 (\text{voltage gain})$$

$$\text{Hence } 40 = 20 \log 10 A$$

$$\text{From which, } 2 = \log 10 A$$

$$\text{and } A = 10^2 = 100$$

$$A = -\frac{R_f}{R_i}, \Rightarrow 100 = -\frac{R_f}{10 \times 10^3}$$

$$\text{Hence } R_f = 100 \times 10 \times 10^3$$

$$\text{Frequency} = \text{gain} \times \text{bandwidth}$$

$$= 100 \times 5 \times 10^3$$

$$= 0.5\text{MHz or } 500\text{kHz}$$

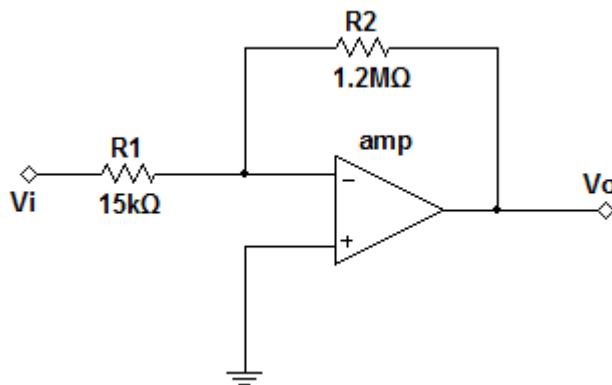


Fig. 3.17

6. Determine (a) the value of the feedback resistor, and (b) the frequency for an inverting amplifier to have a voltage gain of 45 dB, a closed-loop bandwidth of 10 kHz and an input resistance of $20\text{ k}\Omega$.

[(a) $3.56\text{M}\Omega$ (b) 1.78 MHz]

4.5 Non-inverting Amplifier

The basic circuit for a non-inverting amplifier is shown in Fig. 4.18 where the input voltage V_i (*a.c and d.c*) is applied to the non-inverting (+) terminal of the op amp. This produces an output V_o that is in phase with the input. Negative feedback is obtained by feeding back to the inverting (-) terminal, the fraction of V_o developed across R_i in the voltage divider formed by R_f and R_i across V_o .

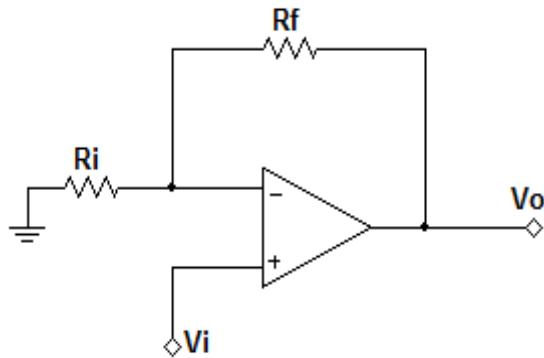


Fig 4.18: Non-inverting Amplifier

Amplifier gain

Let

$$\frac{0 - V_n}{R_i} = \frac{V_n - V_o}{R_f}$$

$$\frac{V_o}{R_f} = \frac{V_n}{R_f} + \frac{V_n}{R_i}$$

$$V_o = R_f V_n \left(\frac{1}{R_f} + \frac{1}{R_i} \right)$$

$$V_n = V_p = V_i$$

$$\frac{V_o}{V_i} = \left(1 + \frac{R_f}{R_i} \right)$$

$$A_V = \frac{V_o}{V_i} = \left(1 + \frac{R_f}{R_i} \right)$$

For example, if $R_i = 10 \text{ k}\Omega$ and $R_f = 100 \text{ k}\Omega$, then

$$A = 1 + \frac{100 \times 10^3}{10 \times 10^3} = 11$$

Again, the gain depends only on the values of R_i and R_f and is independent of the open-loop gain A_o .

Note that for the non-inverting amplifier the closed loop gain is greater than unity.

Example 4.5. For the op amp shown in Fig. 4.18, $R_1 = 4.7 \text{ k}\Omega$ and $R_f = 10 \text{ k}\Omega$. If the input voltage is -0.4 , determine (a) the voltage gain (b) the output voltage.

Solution;

The op amp shown in Fig. 4.18 is a non-inverting amplifier

(a) From equation above,

$$\begin{aligned} A &= 1 + \frac{R_f}{R_i} \\ &= 1 + \frac{10 \times 10^3}{4.7 \times 10^3} \\ &= 1 + 2.13 = 3.13 \end{aligned}$$

(b) Also output voltage,

$$\begin{aligned} V_o &= -\frac{R_f}{R_i} V_i \\ 1(3.13)(-0.4) &= -1.25V \end{aligned}$$

4.6 Voltage Follower

In some cases, we have two-terminal networks which do not match well, i.e., the input impedance of the later stage is not very large, or the output impedance of preceding stage is not low enough. A “buffer” circuit is usually used in between these two circuits to solve the matching problem. These “buffer” circuits typically have a gain of 1 but have very large input impedance and very small output impedance. Because their gains are 1, they are also called “voltage followers.” The non-inverting amplifier above can be turned into a voltage follower (buffer) by adjusting R_1 and R_2 such that the gain is 1. (fig. 4.19)

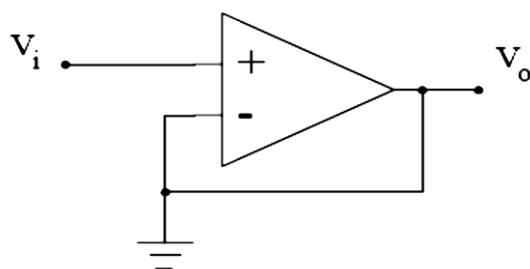


Fig. 4.20 Voltage Follower

$$\frac{V_o}{V_i} = 1 + \frac{R_2}{R_1} = 1 \quad \rightarrow \quad R_2 = 0$$

So by setting $R_2 = 0$, we have $V_o = V_i$ or a gain of unity. We note that this expression is valid for any value of R_1 . As we want to minimize the number of components in a circuit as a rule (cheaper circuits!) we set $R_1 = 0$ and also remove R_1 from the circuit.

4.7 Inverting Summer amplifier

Because of the existence of the virtual earth point, an op amp can be used to add a number of voltages (*a.c and d.c*) when connected as a multi-input inverting amplifier. This, in turn, is a consequence of the high value of the open-loop voltage gain A_o . Such circuits may be used as ‘mixers’ in audio systems to combine the outputs of microphones, electric guitars, pick-ups, etc. They are also used to perform the mathematical process of addition in analogue computing. The circuit of an op amp summing amplifier having three input voltages V_1 , V_2 and V_3 applied via input resistors R_1 , R_2 and R_3 is shown in Fig. 3.21. If it is assumed that the inverting (–) terminal of the op amp draws no input current, all of it passing through R_f , then:

$$I = I_1 + I_2 + I_3$$

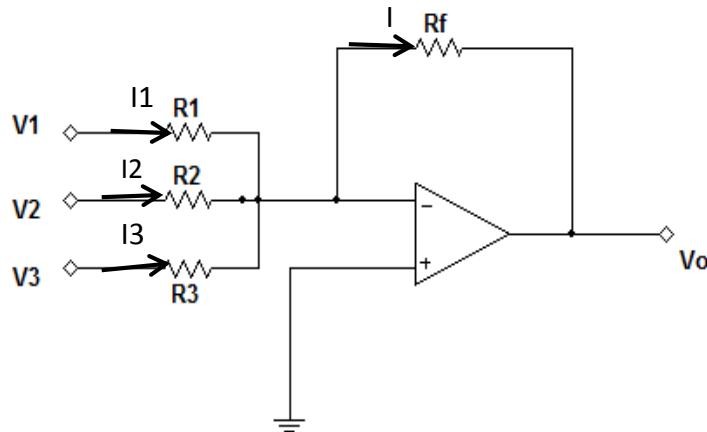


Fig. 4.20 Inverting Summer amplifier

Since (V_+ to V_-) is a virtual earth (*i.e* 0V), it follows that:

$$\frac{V_o}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

$$V_o = \left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right)$$

$$V_o = R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

Summation is said to have occurred. Alternatively, the input voltages are added and attenuated if R_f is less than each input resistor; ‘weighted’ summation is said to have occurred. Alternatively, the input voltages are added and attenuated if R_f is less than each input resistor. For example, if

$$\frac{R_f}{R_1} = 5 \quad \frac{R_f}{R_2} = 4 \text{ and } \frac{R_f}{R_3} = 1$$

And $V_1 = V_2 = V_3 = +1V$, then

$$V_o = \left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right)$$

$$V_o = -(5 + 4 + 1) = -10V$$

If $R_1 = R_2 = R_3 = R$ then the input voltages are amplified or attenuated equally, and

$$V_o = -\frac{R_f}{R}(V_1 + V_2 + V_3)$$

If, also $R = R_f$ then

$$V_o = -(V_1 + V_2 + V_3)$$

The virtual earth is also called the **summing point** of the amplifier. It isolates the inputs from one another so that each behaves as if none of the others existed and none feeds any of the other inputs even though all the resistors are connected at the inverting (–) input.

Example 4.6. For the summing op amp shown in Fig 3.22, determine the output voltage V_o .

Solution

$$V_o = R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

$$V_o = -50 \times 10^3 \left(\frac{0.5}{10 \times 10^3} + \frac{0.8}{20 \times 10^3} + \frac{1.2}{30 \times 10^3} \right)$$

$$V_o = -50 \times 10^3 (5 \times 10^{-5} + 4 \times 10^{-5} + 4 \times 10^{-5})$$

$$V_o = -(50 \times 10^3)(13 \times 10^{-5}) = -6.5V$$

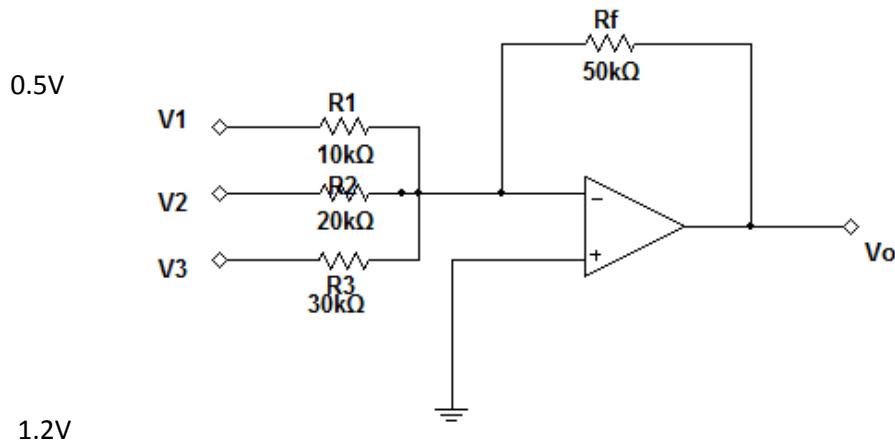
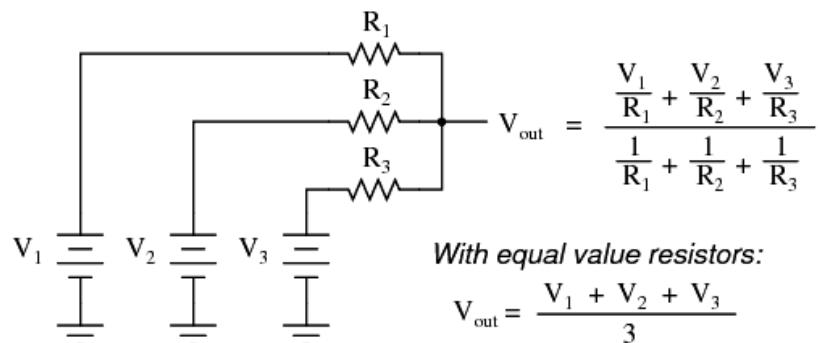


Fig. Q4.6

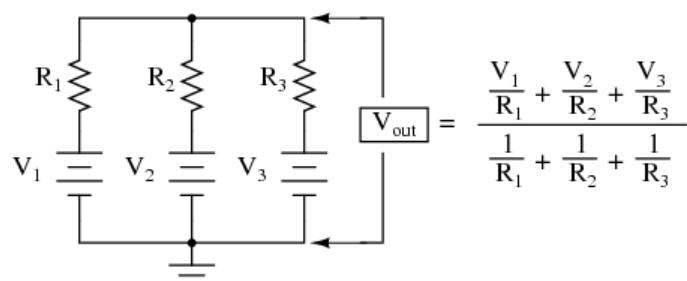
4.8 Averager

If we take three equal resistors and connect one end of each to a common point, then apply three input voltages (one to each of the resistors' free ends), the voltage seen at the common point will be the mathematical *average* of the three, (Fig. 4.21). This circuit is really nothing more than a practical application of Millman's Theorem.

"Passive averager" circuit



(a)



(b)

Fig. 4.21 The circuit diagram of an averager

This circuit is commonly known as a *passive averager*, because it generates an average voltage with non-amplifying components. *Passive* simply means that it is an unamplified circuit. The large equation to the right of the averager circuit comes from Millman's Theorem, which describes the voltage produced by multiple voltage sources connected together through individual resistances. Since the three resistors in the averager circuit are equal to each other, we can simplify Millman's formula by writing R_1 , R_2 , and R_3 simply as R (one, equal resistance instead of three individual resistances):

$$V_{\text{out}} = \frac{\frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R}}{\frac{1}{R} + \frac{1}{R} + \frac{1}{R}}$$

$$V_{\text{out}} = \frac{\frac{V_1 + V_2 + V_3}{R}}{\frac{3}{R}}$$

$$V_{\text{out}} = \frac{V_1 + V_2 + V_3}{3}$$

4.8.1 Active averager

If we take a passive averager and use it to connect three input voltages into an op-amp amplifier circuit with a gain of 3, we can turn this *averaging* function into an *addition* function. The result is called a *non-inverting summer* circuit:

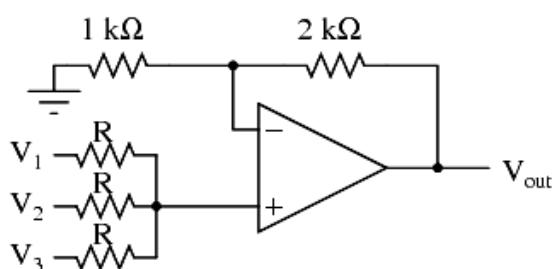


Fig. 4.22 The circuit diagram of an active averager

With a voltage divider composed of a $2\text{k}\Omega / 1\text{k}\Omega$ combination, the non-inverting amplifier circuit will have a voltage gain of 3. By taking the voltage from the passive averager, which the sum is of V_1, V_2 and V_3 divided by 3, and multiplying that average by 3, we arrive at an output voltage equal to the *sum* of V_1, V_2 and V_3 :

$$V_{\text{out}} = 3 \frac{V_1 + V_2 + V_3}{3}$$

$$V_{\text{out}} = V_1 + V_2 + V_3$$

4.9 Op amp integrator

The circuit for the op amp integrator shown in Fig. 4.17 is the same as for the op amp inverting amplifier shown in Fig. 4.23, but feedback occurs via a capacitor C , rather than via a resistor.

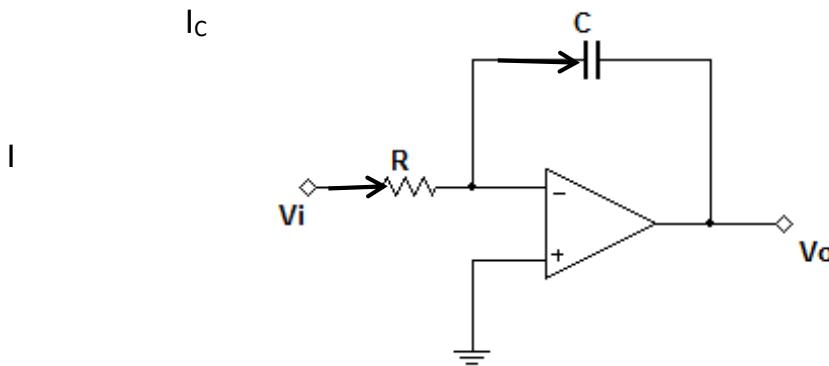


Fig. 4.23 Op amp integrator

The output voltage is given by:

$$V_0 = -\frac{1}{CR} \int V_i dt$$

Since the inverting ($-$) input is used in Fig. 19.15, V_0 is negative if V_i is positive, and vice versa, hence the negative sign in equation (9). Since X is a virtual earth in Fig. 4.23, i.e. at 0V, the voltage across R is V_i and that across C is V_0 . Assuming again that none of the input current I enters the op amp inverting ($-$) input, then all of current I flows through C and charges it up. If V_i is constant, I will be a constant value given by $I = V_i/R$. Capacitor C therefore charges at a constant rate and the potential of the output side of C ($=V_0$, since its input side is zero) changes so that the feedback path absorbs I . If Q is the charge on C at time t and the p.d. across it (i.e. the output voltage) changes from 0 to V_0 in that time then:

$$Q = V_0 C = It$$

For the ideal integrator, the rate of change of the output is given by

$$I = I_C \quad \text{and} \quad I = \frac{V_i}{R}$$

$$i.e - V_0 C = \frac{V_i}{R} t$$

$$i.e V_0 = -\frac{1}{CR} V_i t$$

This result is the same as would be obtained from

$$\begin{aligned} - \int dV_0 &= \int \frac{1}{CR} V_i t dt \\ V_0 &= -\frac{1}{CR} \int V_i dt \end{aligned}$$

$$V_0 = -\frac{1}{CR} \int V_i dt + V_0(0) \text{initial}$$

$m = 2$ and vertical axis intercept $c = 0$). V_0 rises steadily by $+2V/s$ in Fig. 3.25, and if the power supply is, say, $\pm 9V$, then V_0 reaches $+9V$ after 4.5 s when the op amp saturates.

Example 4.7. A steady voltage of $-0.75V$ is applied to an op amp integrator having component values of $R = 200 \text{ k}\Omega$ and $C = 2.5 \mu\text{F}$. Assuming that the initial capacitor charge is zero, determine the value of the output voltage 100ms after application of the input.

$$V_0 = -\frac{1}{CR} V_i t$$

$$V_0 = \frac{1}{(2.5 \times 10^{-6})(200 \times 10^3)} \int (-0.75) dt$$

$$V_0 = \frac{1}{(0.5)} \int (-0.75) dt = 2[-0.75t] = +1.5V$$

$$\begin{aligned} \text{When time } t &= 100\text{ms}, \\ \text{Output voltage, } V_0 &= (1.5)(100 \times 10^{-3}) = 0.15V \end{aligned}$$

4.10 Difference Amplifier

A circuit for an op amp differential amplifier is shown in Fig. 4.24 where voltages V_1 and V_2 are applied to its two input terminals and the difference between these voltages is amplified.

(i) Let V_1 volts be applied to terminal 1 and 0V be applied to terminal 2. The difference in the potentials at the inverting ($-$) and non-inverting ($+$) op amp inputs is practically zero and hence the inverting terminal must be at zero potential. Then $I_1 = V_1 / R_1$. Since the op amp input resistance is high, this current flows through the feedback resistor R_f . The volt drop across R_f which is the output voltage.

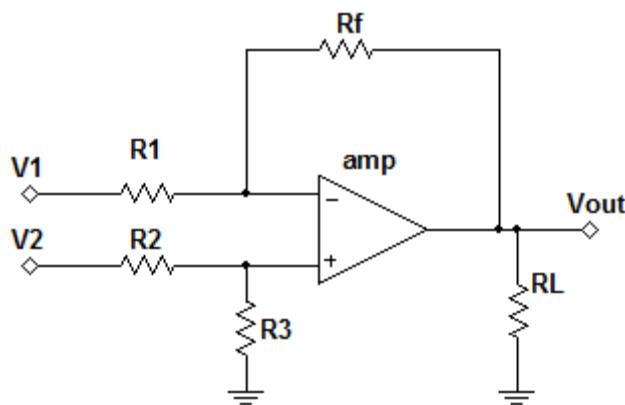


Fig. 4.24 A typical difference amplifier

$$V_o = -\frac{V_1}{R_1} R_f$$

Hence, the closed loop voltage gain A is given by:

$$A = -\frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

(ii) By similar reasoning, if V_2 is applied to terminal 2 and 0V to terminal 1, then the voltage appearing at the non-inverting terminal will be

$$\left(\frac{R_3}{R_2 + R_3} \right) V_2 \text{ volts}$$

This voltage will also appear at the inverting ($-$) terminal and thus the voltage across R_1 is equal to

$$-\left(\frac{R_3}{R_2 + R_3} \right) V_2 \text{ volts}$$

Now the output voltage,

$$V_o = \left(\frac{R_3}{R_2 + R_3} \right) V_2 + \left[-\left(\frac{R_3}{R_2 + R_3} \right) V_2 \right] \left(-\frac{R_f}{R_1} \right)$$

And

the voltage gain,

$$A = \frac{V_o}{V_2} = \left(\frac{R_3}{R_2 + R_3} \right) + \left[-\left(\frac{R_3}{R_2 + R_3} \right) \right] \left(-\frac{R_f}{R_1} \right)$$

$$A = \frac{V_o}{V_2} = \left(\frac{R_3}{R_2 + R_3} \right) + \left[\left(\frac{R_3}{R_2 + R_3} \right) \left(\frac{R_f}{R_1} \right) \right]$$

$$A = \frac{V_o}{V_2} = \left(\frac{R_3}{R_2 + R_3} \right) \left[1 + \frac{R_f}{R_1} \right]$$

(iii) Finally, if the voltages applied to terminals 1 and 2 are V_1 and V_2 respectively, then the difference between the two voltages will be amplified.

If ($V_1 > V_2$), then;

$$V_o = (V_1 - V_2) \left(-\frac{R_f}{R_1} \right)$$

If ($V_2 > V_1$), then;

$$V_o = (V_2 - V_1) \left(\frac{R_3}{R_2 + R_3} \right) \left(-\frac{R_f}{R_1} \right)$$

4.11 Op amp differentiator

The circuit for the op amp Inverting differentiator shown in Fig. 4.25 is the same as for the op amp inverting amplifier shown in Fig. 4.17, but input is through a capacitor C, rather than via a resistor.

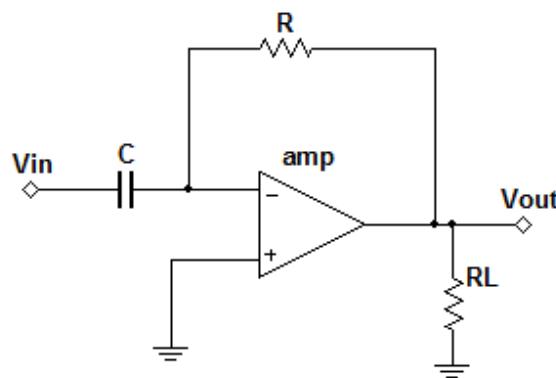


Fig. 4.26 Op amp differentiator

The output voltage is given by:

$$V_{out} = -RC \frac{d V_{in}}{dt} \text{ where } V_{in} \text{ and } V_{out} \text{ are functions of time}$$

This can also be viewed as a high-pass electronic filter. It is a filter with a single zero at DC (i.e., where angular_frequency $\omega = 0$ radians) and gain. The high-pass characteristics of a differentiating amplifier (i.e., the low-frequency zero) can lead to stability challenges when the circuit is used in an analogue servo loop (e.g., in a PID controller with a significant derivative gain).

Since the inverting (-) input is used in Fig. 4.18, V_o is negative if V_{in} is positive, and vice versa, hence the negative sign in equation (9). Since X is a virtual earth in Fig. 4.17, i.e. at 0V, the voltage across R is V_o and that across C is V_{in} . Assuming again that none of the input current I enters the op amp inverting (-) input, then all of current I from input flows through R. I will be a given by $I_C = C \frac{d V_i}{dt}$ Capacitor C therefore charges at a constant rate and the potential of the input side of C is equal to V_{in} , (since its other side is zero potential) charges so that the feedback path absorbs I_C . The input current that charge the capacitor from 0 to V_i for the ideal differentiator in time t is given by;

$$I_C = C \frac{d V_i}{dt}, \quad I = -\frac{V_o}{R}$$

$$-\frac{V_o}{R} = C \frac{d V_i}{dt}$$

$$V_o = -RC \frac{d V_i}{dt}$$

Example 4.8. A 1.0 kHz, 10V_{pp} triangular wave is applied to a practical differentiator as shown. Show the output in relationship to the input.

$$V_{out} = -R_f C \left(\frac{V_c}{t} \right) = \left(\frac{10V}{0.5ms} \right) (2.7k\Omega)(100nF) = -5.4$$

4.12 Current Source

Refer to Fig. 4.27 showing the configuration of a current source.

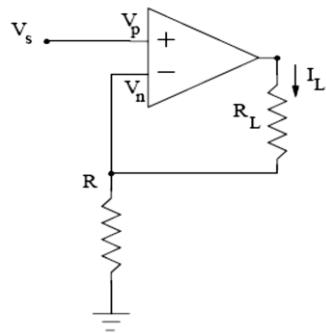


Fig. 4.27 Current Source

Negative Feedback:

$$V_n \cong V_p = V_s$$

$$i_L = \frac{V_n}{R} = \frac{V_s}{R} = \text{constant}$$

Note the current I_L is independent of the value of R_L and, therefore, independent of the voltage V_L . As such this circuit (without resistor R_L) is an independent current source.

The value of the current can be adjusted by changing V_s . Therefore, this circuit is also a “voltage to current” convertor.

4.13 Cascading Op-Amp circuits

An important property of the op-amp circuits discussed above (with the exception of the current source) is that the circuit gain, V_o/V_i is independent of the load. To see that, attach a resistance R_L between the output and ground (voltage V_o appears across this resistor) and solve the circuit. One finds that V_o/V_i is independent of R_L .

This observation means that we can attach any sub-circuit to the op-amp output without affecting V_o/V_i ratio. As such, analysis of cascading op-amp circuit is easy in most cases. Alternatively, a circuit can be designed with the above op-amp building blocks to have a desired value of V_o/V_i . Examples below highlight these two features: (figures 4.9 and 4.10).

Example 4.9: Find V_o/V_i

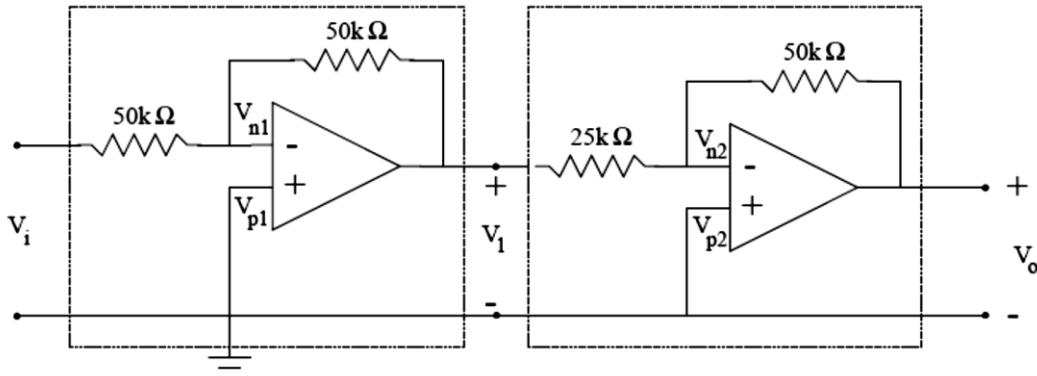


Fig. Q4.9

The circuit is made of two op-amp configured as an inverting amplifiers (see inside each dashed box). Thus,

First stage is an inverting Amp.:

$$\frac{V_1}{V_i} = -\frac{R_2}{R_1} = -\frac{50 \times 10^3}{50 \times 10^3} = -1$$

Second stage is an inverting Amp.:

$$\frac{V_o}{V_1} = -\frac{R_2}{R_1} = -\frac{50 \times 10^3}{25 \times 10^3} = -2$$

System gain:

$$\frac{V_o}{V_i} = \frac{V_1}{V_i} \times \frac{V_o}{V_1} = (-1) \times (-2) = 2$$

This method is much easier than solving the circuit as is shown in Fig. Q4.10 using node-voltage method:

op-amp 1 has negative feedback:

$$V_{n1} \cong V_{p1} = 0$$

op-amp 2 has negative feedback:

$$V_{n2} \cong V_{p2} = 0$$

KCL on node V_{n1} :

$$\frac{V_{n1} - V_i}{50 \times 10^3} + \frac{V_{n1} - V_1}{50 \times 10^3} = 0$$

KCL on node V_{n1}

$$\frac{V_{n2} - V_1}{25 \times 10^3} + \frac{V_{n2} - V_o}{50 \times 10^3} = 0$$

Now substituting for $V_{n1} = V_{n2} = 0$ in the two node equations, we get: $V_I = -V_i$ and $V_o = -2V_I$ and, therefore, $V_o = 2V_i$

Example 4.10:

Design an op-amp circuit such that $V_o = 100V_a - 20V_b$ (V_a and V_b are given inputs). We need first to write the expression for V_o in a form that can be broken into expressions for our 4 op-amp building blocks. Many variations are possible. For example, we can let

From the 1st Stage: $V_1 = -5V_a$

2nd Stage: $V_o = -20(V_1 + V_b)$

System Gain: $V_o = -20(-5V_a + V_b) = 100V_a - 20V_b$

As can be seen, the first stage is an inverting amplifier with a gain of five. The second stage is an inverting summer with a gain of 40. Thus, the circuit will be as shown below

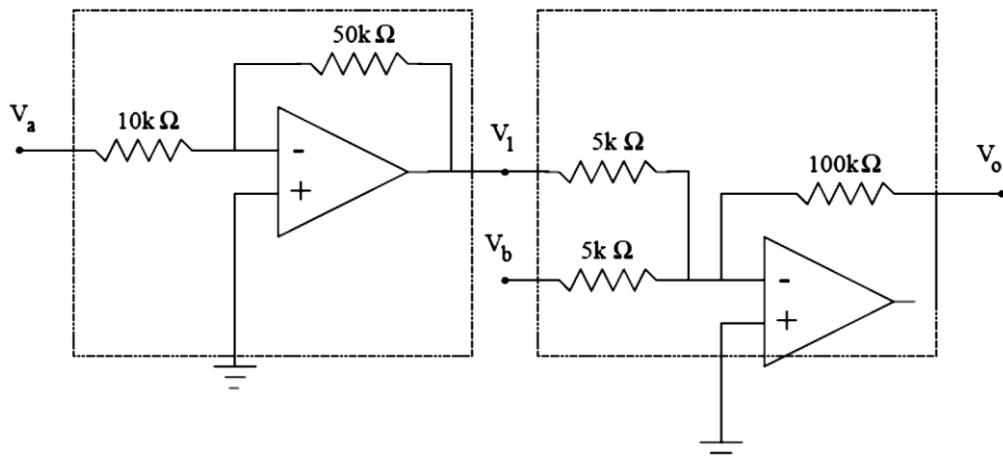


Fig. Q4.10

4.14 Departures from Ideal

The golden rules are not exact. On the other hand, they generally describe most, if not all, observed op-amp behavior. Here are some departures from ideal performance.

- **Offset voltage, V_{os} :** Recall that the input of the op-amp is a differential pair. If the two transistors are not perfectly matched, an offset will show up as a non-zero DC offset at the output. This can be zeroed externally. This offset adjustment amounts to changing the ratio of currents coming from the emitters of the two input transistors.
- **Bias current, I_{bias} :** The transistor inputs actually do draw some current, regardless of golden rule 2. Those which use bipolar input transistors (*e.g.* the 741) draw more current than those which use FETs (*e.g.* the 411). The bias current is defined to be the average of the currents of the two inputs.
- **Offset current, I_{os} :** This is the difference between the input bias currents. Each bias current, after passing through an input resistive network, will effectively offer a voltage to the op-amp input. Therefore, an offset of the two currents will show up as a voltage offset at the output.

The best way to beat these effects, if they ever are a problem for a particular application, is to choose op-amps which have good specifications. For example, I_{os} can be a problem for bi-polar designs, in which case choosing a design with FET inputs will usually solve the problem. However, if one has to deal with this, it is good to know what to do. Fig. 4.28 shows how this might be accomplished. Without the 10 k resistors, this represents a non-inverting amplifier with voltage gain of $1 + (10^5/10^2) \approx 1000$. The modified design in the figure gives a DC path from ground to the op-amp inputs which are approximately equal in resistance (10 k), while maintaining the same gain.

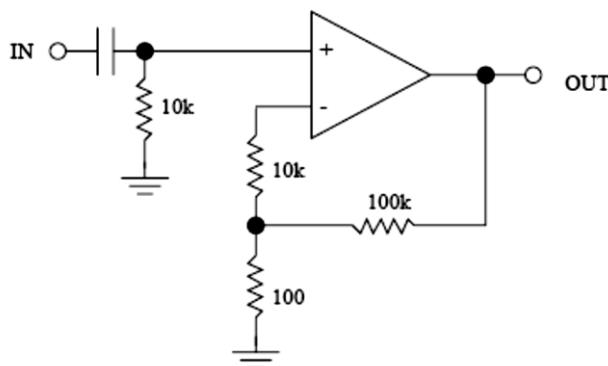


Fig. 4.28: Non-inverting amplifier designed to minimize the effect of I_{os}

Similarly, the inverting amplifier configuration can be modified to mitigate offset currents. In this case one would put a resistance from the $-$ input to ground which is balanced by the R_I and R_f in parallel. It is important to note that, just as we found for transistor circuits, one should always *provide a DC path to ground for op-amp inputs*. Otherwise, charge will build up on the effective capacitance of the inputs and the large gain will convert this voltage ($V = Q/C$) into a large and uncontrolled output voltage offset.

However, our modified designs to fight I_{os} have made our op-amp designs worse in a general sense. For the non-inverting design, we have turned the very large input impedance into a not very spectacular 10 k. In the inverting case, we have made the virtual ground into an approximation. One way around this, if one is concerned only with AC signals, is to place a capacitor in the feedback loop. For the non-inverting amplifier, this would go in series with the resistor R_I to ground. Therefore, as stated before, it is best, where important, to simply choose better op-amps.

4.15 Frequency-dependent Feedback

Below are examples of simple integrator and differentiator circuits which result from making the feedback path have frequency dependence, in these cases single-capacitor RC filters. Again, one would simply modify our derivations of the basic inverting and non-inverting gain formulae by the replacements R with Z , as necessary.

4.16 Negative Feedback

As mentioned above, the first of our Golden Rules for op-amps required the use of negative feedback. We illustrated this with the two basic negative feedback configurations- the inverting and the non-inverting configurations. In this section we will discuss negative feedback in a very general way, followed by some examples illustrating how negative feedback can be used to improve performance.

4.16.1 Gain

Consider the rather abstract schematic of a negative feedback amplifier system shown in Fig. 4.29. The symbol \otimes is meant to indicate that negative feedback is being added to the input. The op-amp device itself has intrinsic gain A . This is called the op-amp's *open-loop gain* since this is the gain the op-amp would have in the absence of the feedback loop. The quantity B is the fraction of the output which is fed back to the input. For example, for the non-inverting amplifier

this is simply given by the feedback voltage divider: $B = R_1 / (R_1 + R_2)$. The gain of the device is, as usual, $G = V_{\text{out}}/V_{\text{in}}$. G is often called the *closed-loop gain*. To complete the terminology, the product AB is called the *loop gain*.

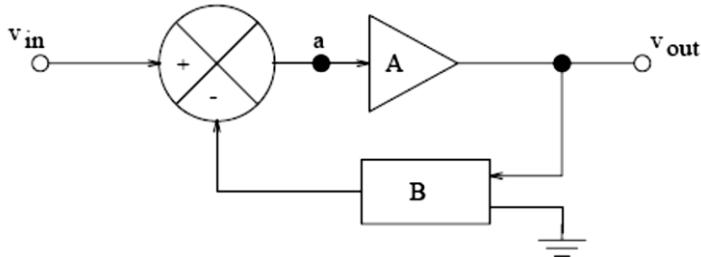


Fig. 4.29: General negative feedback configuration

As a result of the negative feedback, the voltage at the point labeled "a" in the figure is
 $v_a = v_{\text{in}} - Bv_{\text{out}}$

The amplifier then applies its open-loop gain to this voltage to produce v_{out} :

$$v_{\text{out}} = Av_a = Av_{\text{in}} - ABv_{\text{out}}$$

Now we can solve for the closed-loop gain:

$$\frac{V_{\text{out}}}{V_{\text{in}}} \equiv G = \frac{A}{1 + AB}$$

Note that there is nothing in our derivation which precludes having B (or A) be a function of frequency.

4.16.2 Input and Output Impedance

We can now also calculate the effect that the closed-loop configuration has on the input and output impedance. Fig. 4.30 below is meant to clearly show the relationship between the definitions of input and output impedances and the other quantities of the circuit. The quantity R_i represents the open-loop input impedance of the op-amp, that is, the impedance the hardware had in the absence of any negative feedback loop. Similarly, R_o represents the Thevenin source (output) impedance of the open-loop device.

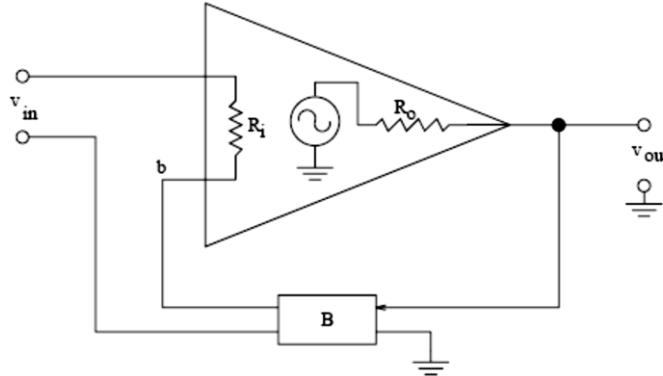


Fig. 4.30: Schematic to illustrate the input and output impedance of a negative feedback configuration

We start the calculation of Z_{in} with the definition $Z_{in} = V_{in}/I_{in}$. Let us calculate the current passing through R_i :

$$i_{in} = \frac{v_{in} - v_b}{R_i} = \frac{v_{in} - Bv_{out}}{R_i}$$

Substituting the result of Eqn. 42 gives

$$i_{in} = \frac{1}{R_i} \left[v_{in} - Bv_{in} \left(\frac{A}{1+AB} \right) \right]$$

Rearranging allows one to obtain

$$Z_{in} = v_{in}/i_{in} = R_i [1 + AB]$$

A similar procedure allows the calculation of $Z_{out} \equiv v_{open}/i_{short}$. We have $v_{open} = v_{out}$ and the shorted current is what we get when the load has zero input impedance. This means that all of the current from the amplifier goes into the load, leaving none for the feedback loop. Hence, $B = 0$ and

$$i_{short} = A(v_{in} - Bv_{out})/R_o = Av_{in}/R_o = \frac{Av_{out}}{R_o G} = \left(\frac{Av_{out}}{R_o} \right) \left(\frac{1+AB}{A} \right) = \frac{v_{out}}{R_o} (1+AB)$$

This gives our result

$$Z_{out} = v_{open}/i_{short} = \frac{R_o}{1+AB}$$

Therefore, the effect of the closed loop circuit is to improve input and output impedances by the identical loop-gain factor $1 + AB \approx AB$. So for a typical op-amp like a 741 with $A = 10^3$, $R_i = 1 M\Omega$, and $R_o = 100\Omega$ then if we have a loop with $B = 0.1$ we get $Z_{in} = 100 M\Omega$ and $Z_{out} = 1\Omega$.

4.16.3 Examples of Negative Feedback Benefits

We just demonstrated that the input and output impedance of a device employing negative feedback are both improved by a factor $1 + AB \approx AB$, the device loop gain. An op-amp may typically have an open-loop gain A which varies by at least an order of magnitude over a useful range of frequency. Let $A_{\max} = 10^4$ and $A_{\min} = 10^3$, and let $B = 0.1$. We then calculate for the corresponding closed-loop gain extremes:

$$G_{\max} = \frac{10^4}{1 + 10^3} \approx 10(1 - 10^{-3})$$

$$G_{\min} = \frac{10^3}{1 + 10^2} \approx 10(1 - 10^{-2})$$

Hence, the factor of 10 open-loop gain variation has been reduced to a 1% variation. This is typical of negative feedback. It attenuates errors which appear within the feedback loop, either internal or external to the op-amp proper.

In general, the benefits of negative feedback go as the loop gain factor AB . For most op-amps, A is very large, starting at $> 10^5$ for $f < 100$ Hz. A large gain G can be achieved with large A and relatively small B , at the expense of somewhat poorer performance relative to a smaller gain, large B choice, which will tend to very good stability and error compensation properties. An extreme example of the latter choice is the “op-amp follower” circuit, consisting of a non-inverting amplifier (see Fig. figure 4.3) with $R_2 = 0$ and R_1 removed. In this case, $B = 1$, giving $G = A/(1 + A) \approx 1$.

There is another interesting feature of negative feedback. The qualitative statement is that any signal irregularity which is put into the feedback loop will, in the limit $B \rightarrow 1$, be taken out of the output. This reasoning is as follows. Imagine small, steady signal v_s which is added within the feedback loop. This is returned to the output with the opposite sign after passing through the feedback loop. In the limit $B = 1$ the output and feedback are identical ($G = 1$) and the cancellation of v_s is complete. An example of this is that of placing a “push-pull” output stage to the op-amp output in order to boost output current. The push-pull circuits, while boosting current, also exhibits “cross-over distortion”. However, when the stage is placed within the op-amp negative feedback loop, this distortion can essentially be removed, at least when the loop gain AB is large.

4.17 Compensation in Op-amps

Recall that an RC filter introduces a phase shift between 0 and $\pi/2$. If one cascades these filters, the phase shifts can accumulate, producing at some frequency ω_π the possibility of a phase shift of $\pm \pi$. This is dangerous for op-amp circuits employing negative feedback, as a phase shift of π converts negative feedback to *positive* feedback. This in turn tends to compound circuit instabilities and can lead to oscillating circuits (as we do on purpose for the RC relaxation oscillator).

So it is perhaps easy to simply not include such phase shifts in the feedback loop. However, at high frequencies ($f \sim 1$ MHz or more), unintended stray capacitances can become significant. In fact, within the op-amp circuits themselves, this is almost impossible to eliminate. Most manufacturers of op-amps confront this issue by intentionally reducing the open-loop gain at high frequency. This is called *compensation*. It is carried out by bypassing one of the internal amplifier stages with a high-pass filter. The effect of this is illustrated in Fig. 4.31. It is a so-called "Bode plot", $\log_{10}(A)$ vs $\log_{10}(f)$, showing how the intrinsic gain of a compensated op-amp (like the 741 or 411) decreases with frequency much sooner than one without compensation. The goal is to achieve $A < 1$ at ω_π which is typically at frequencies of 5 to 10 MHz (One other piece of terminology: The frequency at which the op-amp open-loop gain, A , is unity, is called f_T , and gives a good indication of how fast the op-amp is.

Compensation accounts for why op-amps are not very fast devices: The contribution of the higher frequency Fourier terms are intentionally attenuated. However, for comparators, which we turn to next, negative feedback is not used. Hence, their speed is typically much greater.

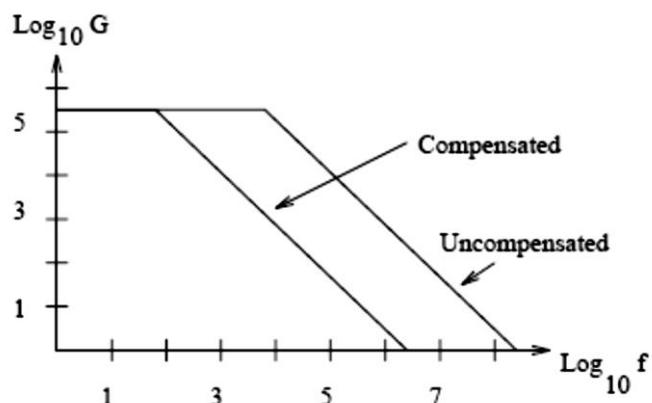


Fig. 4.31: Bode plot showing effect of op-amp compensation.

4.18 Simple Comparator

A comparator can be thought of as a fast, high-gain op-amp which is not used with negative feedback. This basic idea is shown in Fig. 4.32. The comparator has large open-loop gain A . The function of a comparator is to decide which of the two inputs has larger voltage. We have in the limit of very large A

$$v_{\text{out}} = A(v_+ - v_-) = \begin{cases} +V_{\max} & v_+ > v_- \\ -|V_{\min}| & v_+ < v_- \end{cases}$$

where V_{\max} and V_{\min} are approximately the power supply voltages. Therefore, the comparator converts an analog input signal into an output with two possible states. Hence, this can be thought of as a 1-bit analog to digital converter (A/D or ADC). The comparator circuit does not use negative feedback, and so purposefully violates Golden Rule 1. In fact, as we shall see below, comparator circuits often employ *positive* feedback to ensure that nothing intermediate between the two extreme output states is utilized. Finally, without negative feedback, there is no need to do compensation. Thus there is more gain at high frequency, meaning faster response. Also, the amplifier can be optimized for speed at the expense of linearity. Comparators, like op-amps, are readily available as integrated circuit chips, such as the model 311 (LM311 or LF311).

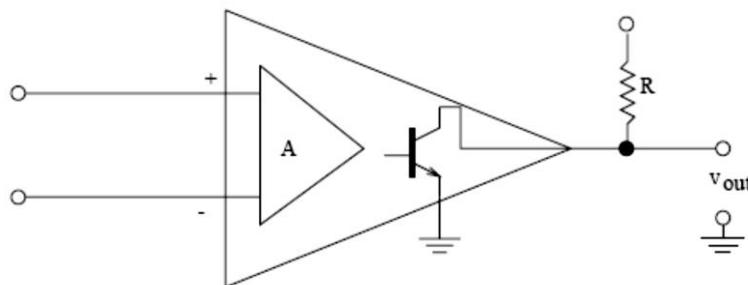


Fig. 4.32: Comparator model

We have shown explicitly in Fig. 4.32 the output stage consisting of a transistor with collector connected to the comparator output. This is the *open collector* output, and is typical. It is used in the 311 comparators we use in lab. We are obliged to complete the circuit by providing a “pull-up” resistor R . The transistor emitter is also available as an external connection. It should be connected to whatever is the lower of the two output voltage states we require. This is chosen to be ground in the figure. The high-gain differential amplifier of the comparator has output connected to the base of this transistor. When that is *low* it will, after passing through an inverter, turn the transistor on. In this case, current will pass through R and to the emitter connection. This current produces a voltage drop across R which pulls the output voltage (very close) to the emitter voltage (ground in our example). Typically $R \approx 1 \text{ k}$. When the comparator inputs are in the complementary inequality, the transistor is switched off and the output voltage goes to the

voltage held by R , which is +5 V in our example. Using outputs of 0 and +5 V are typical, since these voltages correspond (roughly) to the TTL convention of digital electronics.

4.19 Schmitt Trigger

A typical circuit using a comparator is shown in Fig. 4.33. The output goes to one of its two possible states depending upon whether the input v_- is greater than or less than the “threshold” determined by v_+ . Positive feedback is used to help reinforce the chosen output state. In this configuration, called the Schmitt trigger, two thresholds can be set, depending upon which state the output is in. The way this works is illustrated in Fig. 3.34. V_h and V_l refer to threshold voltages which are set up at the comparator + input by the resistor divider chain. As long as $R_3 \gg R_4$, the output states will still be determined by the pull-up resistor R_4 . For the circuit in the figure, these states are 0 and +5 V. The resistor divider, then sets V_+ at different values, depending upon which state the output is in. Whether the connection to $+V_1$ and R_1 is required or not depends upon whether a positive threshold is required when $V_{out} = 0$.

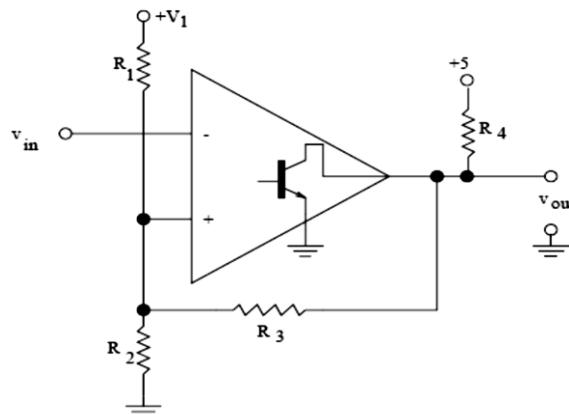


Fig.4.33: Schmitt trigger

Referring to Fig. 4.34, we start with $V_{in} = V_- < V_+$. The output is in the +5 V state. In this case the threshold produced by the voltage divider, V_h , is the larger value due to the contribution of V_{out} . When the input crosses the threshold, the output changes to the other state of 0 V. The divider then gives a lower threshold V_l . Having two thresholds provides comparator stability and noise immunity. Any noise which is $\ll (V_h - V_l)$ will not affect the operation of the comparator.

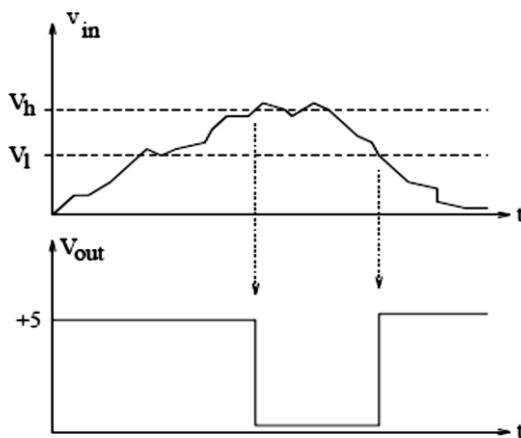


Figure 4.34: Examples of Schmitt trigger signals versus time. Top: v_{in} ; the dashed lines indicate the two thresholds set up at the + input of the comparator. Bottom: v_{out}

Note that the resistor $R1$ is not necessary if $V_1 = 0$. Also, a negative threshold could be set in two ways. The resistor chain forming the threshold could be connected to negative voltage, rather than ground, or the emitter of the output transistor could be connected to negative voltage, thus producing an output with low state at this negative voltage.

4.20 Introduction to oscillator

Every oscillator has at least one active device be it a transistor or even the old valve. It consists of three main components, an Amplifier, frequency determining network and feedback network.

The frequency-determining network is the core of the oscillator and deals with the generation of the specified frequency.

The desired frequency may be generated by using an inductance–capacitance (*LC*) circuit, a resistance–capacitance (*RC*) circuit or a piezoelectric crystal and may fall into the general form Fig. 4.35

Each of these networks produces a particular frequency depending on the values of the components and the cut of the crystal

At turn on, when power is first applied, random noise is generated within our active device and then amplified. This noise is fed back positively through frequency selective circuits to the input where it is amplified again and so on.

Ultimately a state of equilibrium is reached where the losses in the circuit are made good by consuming power from the power supply and the frequency of oscillation is determined by the

external components, be they inductors and capacitors (L.C.) or a crystal. The amount of positive feedback to sustain oscillation is also determined by external components.

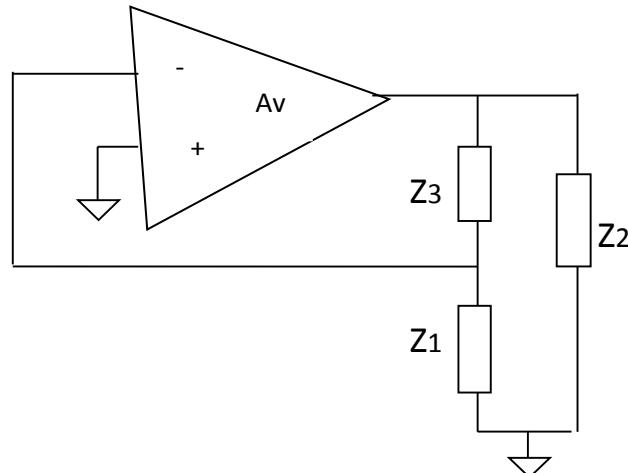


Fig. 4.35 General form of oscillator

The load impedance Z_L will be in parallel with Z_2 . The gain without feedback is $A = -A_v Z_L / (Z_L + Z_o)$. The feedback factor is $\beta = -Z_1 / (Z_1 + Z_3)$

The loop gain is found to be

$$-A\beta = \frac{-A_v Z_1 Z_2}{R_o(Z_1 + Z_2 + Z_3) + Z_2(Z_1 + Z_3)}$$

If the impedances are pure reactances then:

$$Z_1 = jX_1, \quad Z_2 = jX_2, \quad Z_3 = jX_3$$

For an inductor, $X = wL$ and for capacitance, $X = -\frac{1}{wC}$ then,

$$-A\beta = \frac{+A_v X_1 X_2}{jR_o(X_1 + X_2 + X_3) + X_2(X_1 + X_3)}$$

and

$$X_1 + X_2 + X_3 = 0$$

$$-A\beta = \frac{A_v X_1 X_2}{-X_2(X_1 + X_3)} = \frac{-A_v X_1}{X_1 + X_3}$$

$$-A\beta = \frac{A_v X_1}{-X_2}$$

If the X_1 and X_2 are capacitors and X_3 is an inductor, the circuit is called a Colpitts oscillator (Fig. 4.36). If the X_1 and X_2 are inductors and X_3 is a capacitor, the circuit is called a Hartley oscillator (Fig. 4.37).

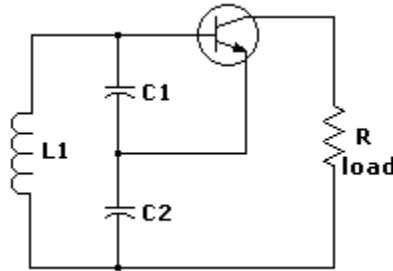


Fig. 4.36 The basic Colpitts oscillator circuit

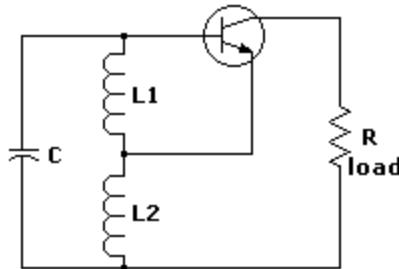


Fig. 4.37 Schematic of a Hartley oscillator

4.20.1 Crystal Oscillators

Crystal oscillators are oscillators where the primary frequency determining element is a quartz crystal. Because of the inherent characteristics of the quartz crystal the crystal oscillator may be held to extreme accuracy of frequency stability. Temperature compensation may be applied to crystal oscillators to improve thermal stability of the crystal oscillator.

Crystal oscillators are usually, fixed frequency oscillators where stability and accuracy are the primary considerations. For example it is almost impossible to design a stable and accurate LC oscillator for the upper HF and higher frequencies without resorting to some sort of crystal control, hence the reason for crystal oscillators (Fig. 4.38)

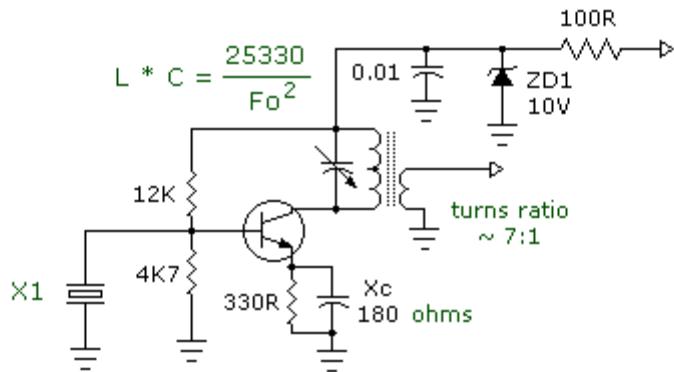


Fig. 4.38 Schematic of a crystal oscillator

4.21 Voltage Regulations

The function of a voltage regulator is to provide a well-specified and constant output voltage level from a poorly specified and sometimes fluctuating input voltage. There are two distinctly different types of IC voltage regulators: Series Regulators and Switching Regulators.

Series Regulators: The series regulators control the output voltage by controlling the voltage drop across a power transistor which is connected in series with the load. The power transistor is operated in the linear region. The series or series pass type voltage regulator is connected in series between the load and the regulated supply line. It is a feedback circuit comprised of reference voltage element, the error amp and series pass element as shown in Fig. 4.39.

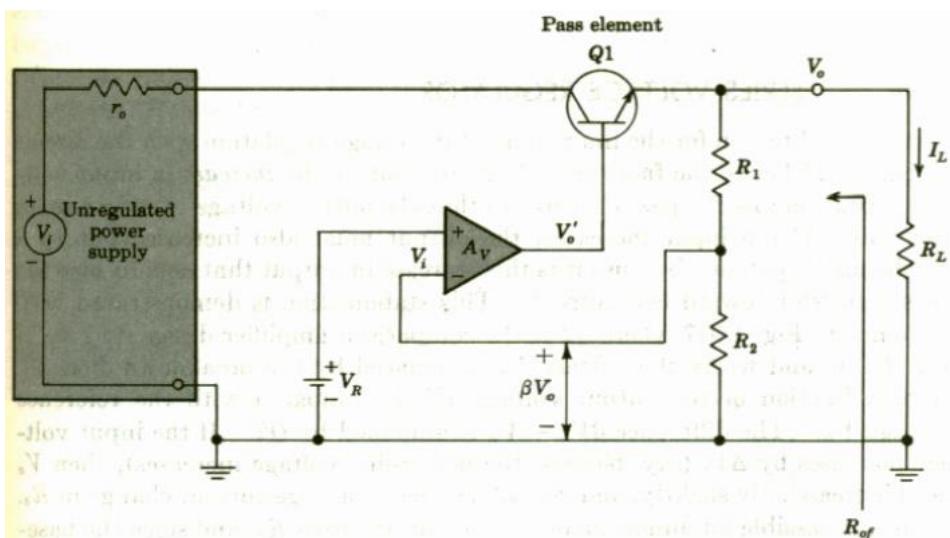


Fig. 4.39 The series regulator using Op-amp

The error amp compares V_R , the sampled voltage V_S and generates a corrective error signal to regulate the voltage drop across the pass element such that the $V_R = V_S$ condition is fulfilled. If we assume that the voltage gain of the pass element is approximately unity and that the amp gain A is very large, Fig. 4.40.

$$\text{Then } V_O = AV_i = A(V_R - \propto V_O)$$

$$\Rightarrow V_O = \frac{A}{1 + \propto A} V_R \quad \text{Where } \propto = \frac{R_2}{R_1 + R_2}$$

Assuming that $\propto A \gg 1$

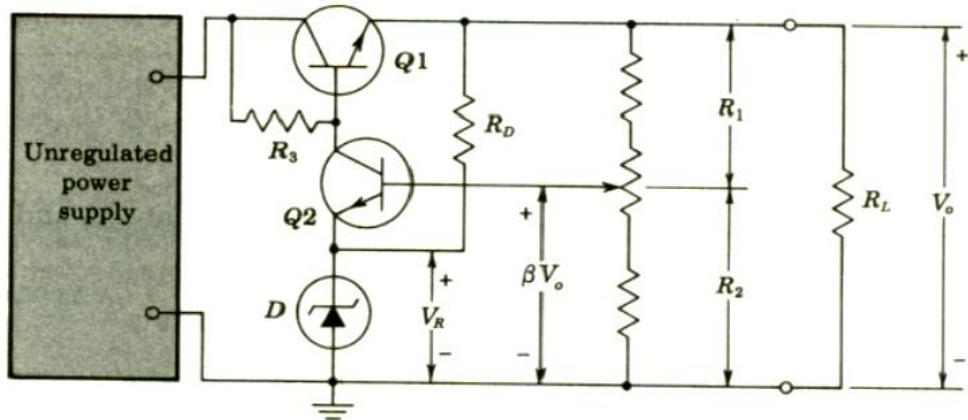


Fig. 4.40 Series regulators using BJT

4.21.1 Protection Circuits

In order to prevent voltage regulator circuits from burning out or suffering permanent damage under accidental overload conditions, a number of faults protection precautions are necessary. Normally three different types of protection circuitry are employed:

- (1) Short circuit or current-limit protection against accidental current overloads,
 - (2) Protection against excessive input-output voltage differentials
 - (3) Protection against excessive junction temperature.
1. Short-circuit protection requirements can be met by either passive or active current limiting at the output. If passive is rarely used as it greatly deteriorates the load regulation characteristic. However, active short-cut protection is mostly used.

In all cases, the total current through the output transistor Q_0 is sensed through a sensing resistor R_{SC} and the resulting voltage drop is used to turn on the normally-off protection transistor Q_1 when this voltage becomes sufficiently large. When Q_1 turns on it shuts every I_B and causes the output current to limit itself to a safe max value, $I(max) = \frac{V_{BE}}{R_{SC}}$.

4.21.2 Stabilization

Since the output dc voltage V_o may depend on the input unregulated dc voltage V_i , load current I_L and temperature T, then the change ΔV_o in output voltage of a power supply can be expressed as:

$$\Delta V_o = \frac{\partial V_o}{\partial V_i} \Delta V_i + \frac{\partial V_o}{\partial I_L} \Delta I_L + \frac{\partial V_o}{\partial T} \Delta T$$

$$\text{OR } \Delta V_o = S_V \Delta V_i + R_o \Delta I_L + S_T \Delta T$$

$$\text{Thus } S_V = \left. \frac{\Delta V_o}{\Delta V_i} \right| \Delta I_L = \Delta T = 0 \quad \text{input regulation factor}$$

$$R_o = \left. \frac{\Delta V_o}{\Delta I_L} \right| \Delta V_i = \Delta T = 0 \quad \text{Output resistance}$$

$$S_T = \left. \frac{\Delta V_o}{\Delta V_i} \right| \Delta V_i = \Delta I_L = 0 \quad \text{Temperature Coefficient}$$

A series regulator using transistor as amplifier is shown in Fig. 4.41 where

- Q_1 serves as the error amplifier.
- Zener or breakdown diode serves as the battery to provide reference voltage
- If V_o changes by ΔV due to change in ΔV_i then Q_1 causes large current to pass through R_3 to stabilize V_o .

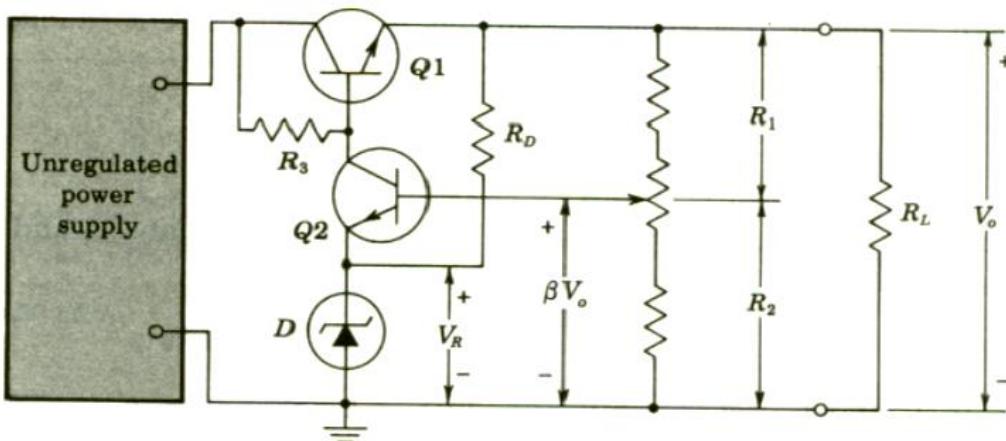


Fig. 4.41 A series regulator using transistor as amplifier

Analysis

$$V_o = V_R + V_{BE1} + \frac{R_1}{R_1+R_2} V_o$$

$$= (V_R + V_{BE1}) \left(1 + \frac{R_1}{R_2}\right) = \frac{V_R + V_{BE1}}{\infty} = \frac{V_R}{\infty}$$

4.22 Switching Regulators

Areas of application: Used in areas where high power and high efficiency is required.

Principle of operation:

- Pass transistor is used as controlled switch
- Cutoff – no current, no power dissipation
- Saturated – nearly a short, less voltage drop across it; dissipates only small amount of average power.

Advantages: It is versatile – voltage less than, greater than or of opposite polarity to the input voltage

Drawback:

- Complex and require external components as inductors or transformers
- Generate more noise (RFI) and output ripple
- Not recommended for powering very low level signal processing circuitry.

Design (Composition): - 3 basic blocks

- The switching element (eg. Power transistor)
- Control circuit for duty cycle setting
- Output circuit which converts the pulsed input power to a steady output power flow

Classes:

- Single – ended inductor circuits
- Diode – capacitor circuits
- Transformer – coupled circuits

Chapter 5: Power amplifiers

CHAPTER OBJECTIVES

- The differences between classes A, AB, and C amplifiers
- What causes amplifier distortion
- Efficiency of various classes of amplifiers
- Power calculations for various class amplifiers

5.1 Introduction

An amplifier may be required to drive a loudspeaker or a motor, and in this application a large signal amplifier generating large swings of current and voltage is required. Such amplified are usually called power Amplifiers. **Power amplifiers are used to feed power into an antenna of a transmitter.** They usually require a booster amplifier to raise the power level to the value required in order to drive the final amplifier which is responsible for feeding large power levels into the load. Note that matching stages are required in order to match the output of one stage to the input impedance of the next stage for maximum power transfer. There are many types of amplifiers that are used for different applications as audio, filters and tuned amplifiers.

Generally a power amplifier has low internal impedance, enabling large currents to be produced. The voltage amplifier, on the other hand, has high internal impedance, enabling large voltages to be developed. A power amplifier must be capable of staying within its rated specifications, distortion must be kept low and the efficiency of the amplifier must be as high as possible. In order to achieve these aims there are many circuits available, some of which are more suitable than others.

5.2 Types of power amplifier

Basically, **amplifier classes represent the amount the output signal varies over one cycle of operation for a full cycle of input signal.** There are about four popular types of power amplifier frequently used in audio power applications: the class A (single-ended) amplifier; the class B push-pull (transformer) amplifier; and the class B complementary pair push-pull amplifier. Each of these types will be considered in turn. **The class C amplifier is mainly used in RF transmitter circuits while the class D is used for digital applications.**

Class A:

The output signal varies for a full 360° of the input signal. Figure 12.1 a shows that this requires the Q -point to be biased at a level so that at least half the signal swing of the output may vary up and down without going to a high enough voltage to be limited by the supply voltage level or too low to approach the lower supply level, or 0 V in this description.

Class B:

A class B circuit provides an output signal varying over one-half the input signal cycle, or for 180° of signal, as shown in Fig. 12.1 b. The dc bias point for class B is at 0 V, with the output then varying from this bias point for a half-cycle. Obviously, the output is not a faithful reproduction of the input if only one half-cycle is present. Two class B operations—one to provide output on the positive-output half-cycle and another to provide operation on the negative-output half-cycle—are necessary. The combined half-cycles then provide an output for a full 360° of operation. This type of connection is referred to as *push pull operation*, which is discussed later in this chapter. Note that **class B operation by itself creates a much distorted output signal** since reproduction of the input takes place for only 180° of the output signal swing.

Class AB:

An amplifier may be biased at a dc level above the zero-base-current level of class B and above one-half the supply voltage level of class A; this bias condition is class AB. Class AB operation still requires a push–pull connection to achieve a full output cycle, but the dc bias level is usually closer to the zero-base-current level for better power efficiency, as described shortly. For class AB operation, the output signal swing occurs between 180° and 360° and is neither class A nor class B operation.

Class C:

The output of a class C amplifier is biased for operation at less than 180° of the cycle and **will operate only with a tuned (resonant) circuit**, which provides a full cycle of operation for the tuned or resonant frequency. This operating class is therefore used in special areas of tuned circuits, such as radio or communications.

Class D:

This operating class is a form of amplifier operation using pulse (digital) signals, which are on for a short interval and off for a longer interval. Using digital techniques makes it possible to obtain a signal that varies over the full cycle (using sample- and-hold circuitry) to recreate the output from many pieces of input signal. The major advantage of class D operation is that the amplifier is “on” (using power) only for short intervals and the overall efficiency can practically be very high.

5.3 Amplifier Efficiency

The power efficiency of an amplifier, defined as the ratio of power output to power input, improves (gets higher) going from class A to class D. In general terms, we see that a class A amplifier, with dc bias at one-half the supply voltage level, uses a good amount of power to maintain bias, even with no input signal applied. This results in very poor efficiency,

especially with small input signals, when very little ac power is delivered to the load. In fact, the maximum efficiency of a class A circuit, occurring for the largest output voltage and current swing, is only 25% with a direct or series-fed load connection and 50% with a transformer connection to the load. Class B operation, with no dc bias power for no input signal, can be shown to provide a maximum efficiency that reaches 78.5%. Class D operation can achieve power efficiency over 90% and provides the most efficient operation of all the operating classes. Since class AB falls between class A and class B in bias, it also falls between their efficiency ratings—between 25% (or 50%) and 78.5%. Table 5.1 summarizes the operation of the various amplifier classes. This table provides a relative comparison of the output cycle operation and power efficiency for the various class types. In class B operation, a push-pull connection is obtained using either a transformer coupling or by using complementary (or quasi-complementary) operation with *npn* and *pnp* transistors to provide operation on opposite-polarity cycles. Although transformer operation can provide opposite-cycle signals, the transformer itself is quite large in many applications. A transformerless circuit using complementary transistors provides the same operation in a much smaller package. Circuits and examples are provided later in this chapter.

Table 5.1 Comparison of Amplifier Classes

Class				
A	AB	B	C ^a	D
Operating cycle 360°	180° to 360°	180°	Less than 180°	Pulse operation
Power efficiency	25% to 50%	Between 25%	78.5% (50%) and 78.5%	Typically over 90%

Class C is usually not used for delivering large amounts of power, and thus the efficiency is not given here.

5.4 Series-Fed Class A Amplifier

The simple fixed-bias circuit connection shown in Fig. 5.2 can be used to discuss the main features of a class A series-fed amplifier. The only differences between this circuit and the small-signal version considered previously is that the signals handled by the large-signal circuit are in the range of volts, and the transistor used is a power transistor that is capable of operating in the range of a few to tens of watts. As will be shown in this section, this circuit is not the best to use as a large-signal amplifier because of its poor power efficiency. The beta of a power transistor is generally less than 100, the overall amplifier circuit using power transistors that are capable of handling large power or current while not providing much voltage gain.

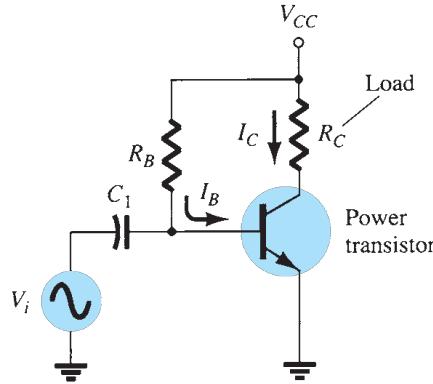


Fig. 5.2 Series-fed class A large-signal amplifier

5.4.1 DC Bias Operation

The dc bias set by V_{CC} and R_B fixes the dc base-bias current at

$$I_B = \frac{V_{CC} - 0.7}{R_B}$$

with the collector current then being

$$I_B = \beta I_C$$

with the collector-emitter voltage the

$$V_{CE} = V_{CC} - I_C R_C$$

To appreciate the importance of the dc bias on the operation of the power amplifier, consider the collector characteristic shown in Fig. 5.3. A dc load line is drawn using the values of V_{CC} and R_C .

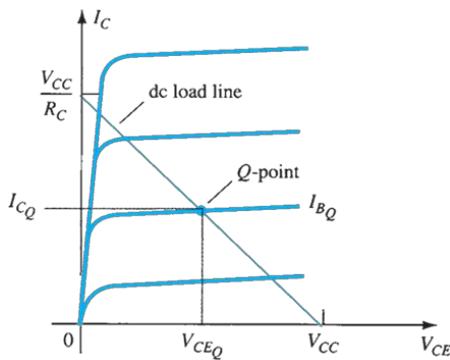


Fig. 5.3: Transistor characteristic showing load line and Q-point.

The intersection of the dc bias value of I_B with the dc load line then determines the operating point (Q-point) for the circuit. If the dc bias collector current is set at one-half the possible

signal swing (between 0 and V_{CC} / R_C), the largest collector current swing will be possible. Additionally, if the quiescent collector–emitter voltage is set at one-half the supply voltage, the largest voltage swing will be possible. With the Q-point set at this optimum bias point, the power considerations for the circuit of Fig. 12.2 are determined as described next.

5.4.2 AC Operation

When an input ac signal is applied to the amplifier of Fig. 5.2, the output will vary from its dc bias operating voltage and current. A small input signal, as shown in Fig. 5.4, will cause the base current to vary above and below the dc bias point, which will then cause the collector current (output) to vary from the dc bias point set as well as the collector–emitter voltage to vary around its dc bias value. As the input signal is made larger, the output will vary further around the established dc bias point until either the current or the voltage reaches a limiting condition. For the current this limiting condition is either zero current at the low end or V_{CC} / R_C at the high end of its swing. For the collector–emitter voltage, the limit is either 0 V or the supply voltage, V_{CC} .

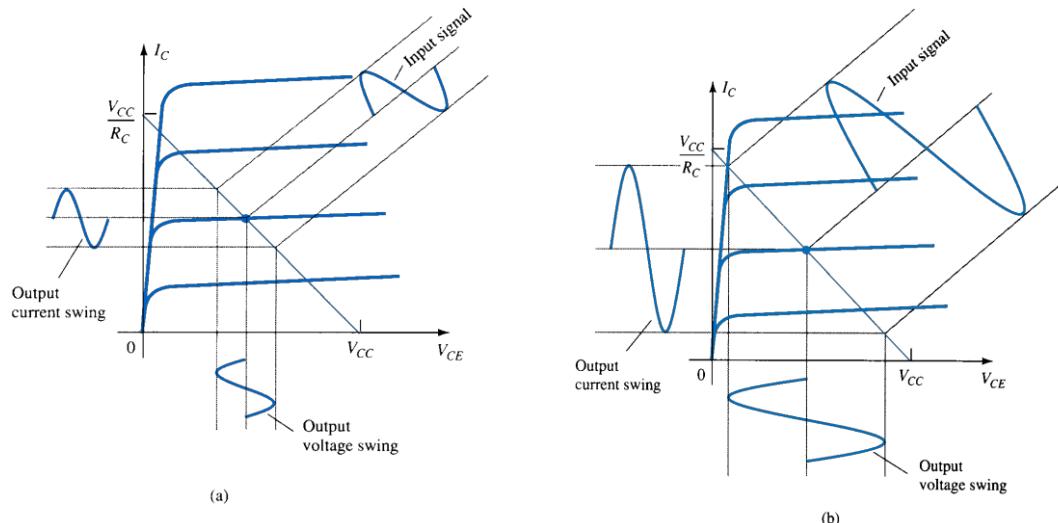


Fig. 5.4: Amplifier input and output signal variation.

5.4.3 Power Considerations

The power into an amplifier is provided by the supply voltage. With no input signal, the dc current drawn is the collector bias current I_{CQ} . The power then drawn from the supply is

$$P_{i(dc)} = V_{CC}I_{CQ}$$

Even with an ac signal applied, the average current drawn from the supply remains equal to

the quiescent current I_{CQ} , so that Eq. (12.4) represents the input power supplied to the class A series-fed amplifier.

5.4.4 Output Power:

The output voltage and current varying around the bias point provide ac power to the load. This ac power is delivered to the load R_C in the circuit of Fig. 5.2. The ac signal V_i causes the base current to vary around the dc bias current and the collector current around its quiescent level I_{CQ} . As shown in Fig. 5.4, the ac input signal results in ac current and ac voltage signals. The larger the input signal, the larger is the output swing, up to the maximum set by the circuit. The ac power delivered to the load (R_C) can be expressed in a number of ways.

Using RMS signals. The ac power delivered to the load (R_C) may be expressed using

$$\begin{aligned} P_o(ac) &= V_{CE}(rms)I_C(rms) \\ P_o(ac) &= I_C^2(rms)R_C \\ P_o(ac) &= \frac{V_C^2}{R_C} (rms) \end{aligned}$$

5.4.5 Efficiency

The efficiency of an amplifier represents the amount of ac power delivered (transferred) from the dc source. The efficiency of the amplifier is calculated using

$$\eta = \frac{P_o(ac)}{P_{i(dc)}} \times 100\%$$

Maximum Efficiency: For the class A series-fed amplifier, the maximum efficiency can be determined using the maximum voltage and current swings. For the voltage swing it is

$$\text{Maximum } V_{CE}(p-p) = V_{CC}$$

For the current swing it is

$$\text{Maximum } I_C(p-p) = \frac{V_{CC}}{R_C}$$

Using the maximum voltage swing in Eq. (12.7) yield

$$\text{Maximum } P_o(ac) = \frac{V_{cc}(V_{cc}/R)}{8}$$

$$\text{Maximum } P_o(ac) = \frac{V_{cc}^2}{8R_C}$$

The maximum power input can be calculated using the dc bias current set to one-half the maximum value:

$$\text{Maximum } P_i(dc) = V_{cc} (\text{maximum } I_C) = V_{cc} \frac{V_{cc}/R_C}{2}$$

$$\text{Maximum } P_i(dc) = \frac{V_{cc}^2}{2R_C}$$

We can then use Eq. (12.8) to calculate the maximum efficiency:

$$\text{Maximum \%}\eta = \frac{\text{Maximum } P_o(ac)}{\text{Maximum } P_i(dc)} \times 100\%$$

$$\text{Maximum \%}\eta = \frac{V_{cc}^2/8R_C}{V_{cc}^2/2R_C} \times 100\%$$

25%

Using the maximum voltage swing in Eq. (12.7) yield

$$\text{Maximum } P_o(ac) = \frac{V_{cc}(V_{cc}/R)}{8}$$

$$\text{Maximum } P_o(ac) = \frac{V_{cc}^2}{8R_C}$$

The maximum power input can be calculated using the dc bias current set to one-half the maximum value:

$$\text{Maximum } P_i(dc) = V_{cc} (\text{maximum } I_C) = V_{cc} \frac{V_{cc}/R_C}{2}$$

$$\text{Maximum } P_i(dc) = \frac{V_{cc}^2}{2R_C}$$

We can calculate the maximum efficiency:

$$\text{Maximum \%}\eta = \frac{\text{Maximum } P_o(ac)}{\text{Maximum } P_i(dc)} \times 100\%$$

$$\text{Maximum \%}\eta = \frac{V_{cc}^2/8R_C}{V_{cc}^2/2R_C} \times 100\%$$

25%

The maximum efficiency of a class A series-fed amplifier is thus seen to be 25%. Since this maximum efficiency will occur only for ideal conditions of both voltage swing and current swing, most series-fed circuits will provide efficiencies of much less than 25%.

5.5 Class A (single-ended) amplifier

A single-ended power amplifier uses a single transistor with the usual biasing arrangement as for a voltage amplifier, but there the similarity ends. A typical circuit is shown in Fig. 5.5. Unlike a small signal voltage amplifier this circuit has to drive a current operated load, and this requires large collector current swings to operate the matching transformer and loudspeaker. A voltage amplifier would use a high resistive load but here the load is the low resistance primary of a transformer, the transformer being used to match the high collector resistance of the transistor.

When dealing with power amplifiers it is necessary to know the operating conditions as well as the power rating of the active device. Figure 5.6 shows a set of output characteristics together with the power dissipation curve and ac and dc load lines. The power curve shows the operational region inside which the device will operate within its rated power value. This area is marked *ABCD*. Often a heat sink has to be attached to the device to achieve the rated value.

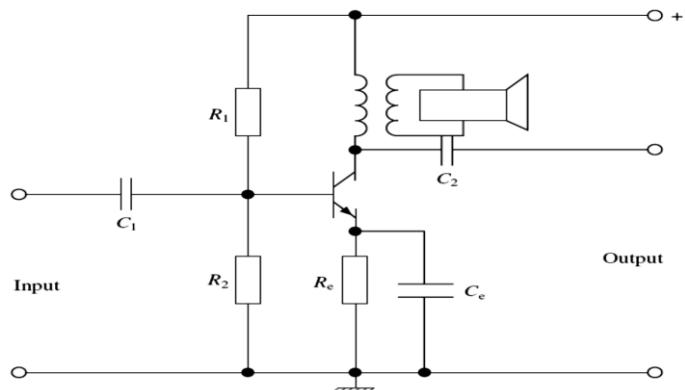


Fig. 5.5: A typical Class A Power Amplifier

The dc load line is determined by knowing the values of the collector resistance (R_C) and emitter resistance (R_E). The slope of the dc load line is then given as:

$$\text{Slope} = \frac{1}{R_C + R_E}$$

The value of R_E is generally between $500\ \Omega$ and $1000\ \Omega$. The dc load line is drawn for the dc operating conditions of the device without the load attached. The ac. load line takes the load (R_L) into consideration so that

$$R_T = \frac{R_C R_L}{R_C + R_L}$$

In summary, the dc load line is used to set up the quiescent conditions without an input signal, while the ac load line sets up the amplifier for input signal conditions. While graphical solutions are seldom used in problem-solving, it is instructive to consider the meaning of characteristics under dc and ac operating conditions. The dc power in this case is the product of the supply voltage and the dc component of the collector current, i.e.

$$P_{DC} = V_{CC}I_c$$

Because of losses due to transformer resistance, emitter resistance and collector dissipation, the output a.c. power delivered to the load is less than the d.c. power. Also since the main power loss is in the collector,

$$P_{DC} = P_{AC} + P_C$$

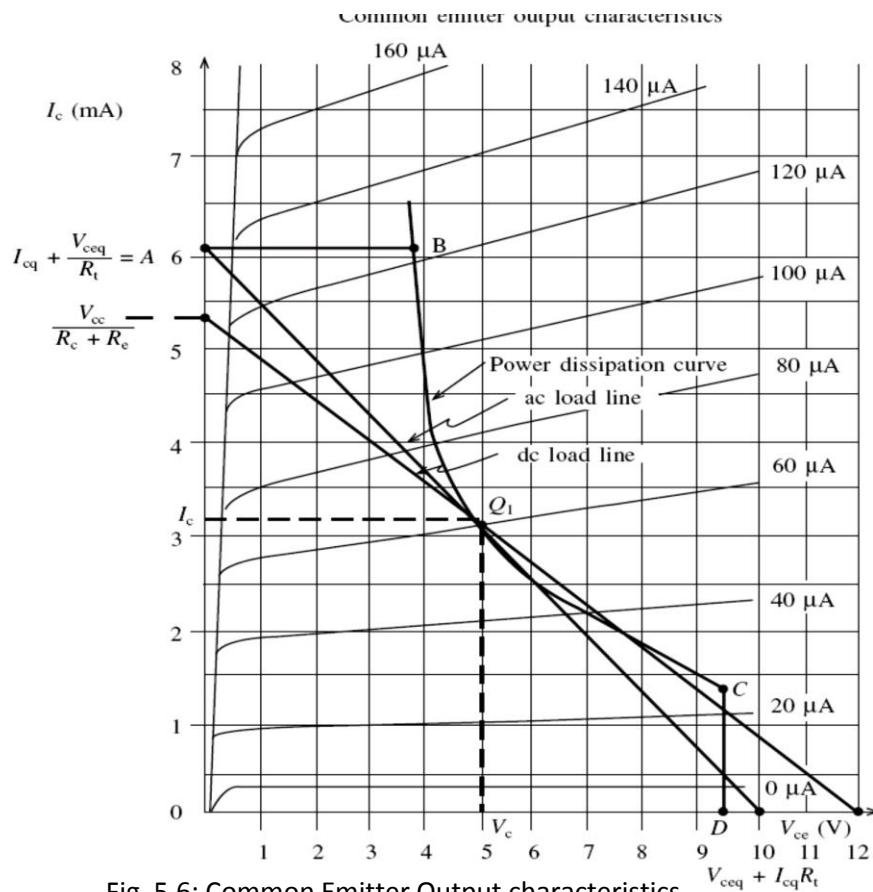


Fig. 5.6: Common Emitter Output characteristics

The following points should be observed from Fig. 5.6:

- (a) The ac load line sets the maximum limits of the current and voltage swings at the output.
- (b) The quiescent point sets the d.c. operating conditions for the device and should be chosen to give an undistorted output. If this is not chosen properly, flattening of the waveform could occur.
- (c) The intersection of the d.c. and a.c. load lines determines the Q-point, and this is normally achieved by the bias resistors.

- (d) When no signal is applied, the quiescent voltage equals the supply voltage.
- (e) When no signal is applied, the quiescent current is half the maximum collector current.
- (f) The power dissipation curve sets the limits to how much power may be dissipated in the collector of the transistor.
- (g) The corresponding base current can be determined for each collector current.
- (h) The turns ratio of the transformer (n) transforms the actual load of loudspeakers (R_2) into the optimum load (R_1) of the transistor, i.e.

$$n = \sqrt{\frac{R_1}{R_2}}$$

- (i) Maximum collector dissipation occurs when no signal is applied.

Figure 5.7 shows the effect of an input signal. The resultant swings of the collector current and voltage are given as peak-to-peak.

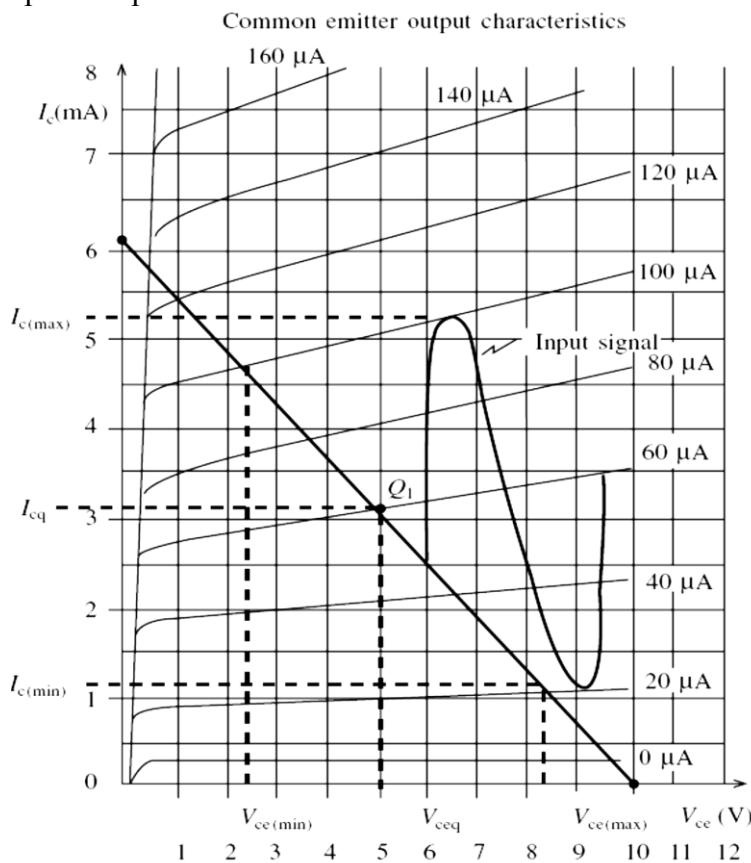


Fig. 5.7: CE output characteristics

In the above characteristics the current and voltage swing between cut-off and saturation.

The efficiency of the stage will be 50% under these conditions but the distortion will be severe so in practice the actual swings are reduced. This results in an efficiency of about 25%. It is for this reason that this type of circuit is not often used.

5.5.1 Practical analysis of class A single-ended parameters

The application of an ac signal to a power amplifier causes large current (I_C) and voltage (V_{ce}) swings. The collector current swings between $I_{C(\max)}$ and $I_{C(\min)}$, while the Collector-emitter voltage swings between $V_{ce(\max)}$ and $V_{ce(\min)}$. The average current and the average voltage are given by:

$$\frac{V_{ce(\max)} - V_{ce(\min)}}{2} \text{ and } \frac{I_{c(\max)} - I_{c(\min)}}{2}$$

If I_m (V_m) represents the peak sinusoidal current (voltage) swing, it is also given by

$$I_c = \frac{I_m}{\sqrt{2}} = \frac{I_{c(\max)} - I_{c(\min)}}{2\sqrt{2}}$$

and

$$V_c = \frac{V_m}{\sqrt{2}} = \frac{V_{ce(\max)} - V_{ce(\min)}}{2\sqrt{2}}$$

The output power in the load is generally given in *rms* values, and if the matching transformer is assumed to be 100% efficient then the output power ($P_{ac(rms)}$) is given by

$$P_{ac(rms)} = \frac{V_m I_m}{2} = \frac{I_m^2 R_L}{2R_L} = \frac{V_m^2}{2R_L}$$

Which may also be written as:

$$\begin{aligned} P_{ac(rms)} &= \frac{I_{c(\max)} - I_{c(\min)}}{2\sqrt{2}} \times \frac{V_{ce(\max)} - V_{ce(\min)}}{2\sqrt{2}} \\ &= \frac{(I_{c(\max)} - I_{c(\min)})(V_{ce(\max)} - V_{ce(\min)})}{8} \end{aligned}$$

An alternative expression given in terms of the primary resistance (R_1), the secondary load resistance (R_2) and the turns ratio is $P_{ac(rms)} = I^2 R_1$; hence

$$P_{ac(rms)} = \left[\frac{(I_{c(\max)} - I_{c(\min)})^2}{8} \right] n^2 R_2$$

A measure of the ability of an active to convert the dc power of a supply into ac (signal) power delivered to a load is called the conversion efficiency and it is also called collector-circuit efficiency for a transistor amplifier.

The collector efficiency is given by

$$\eta = \frac{\text{signal power delivered to load}}{\text{dc power supplied to output circuit}} \times 100\%$$

$$\eta = \frac{P_{ac(rms)}}{P_{dc}} \times 100\%$$

$$\eta = \frac{\frac{1}{2}V_m I_m}{V_{cc} I_c} \times 100\% = 50 \frac{V_m I_m}{V_{cc} I_c}$$

5.6 Class B push-pull (transformer) amplifier

Only class A amplification gives a distortionless output. By using push-pull circuits, however, class B amplification can be obtained with no output distortion. Furthermore, higher efficiencies are achieved. An added bonus is the elimination of even harmonic distortion which drives the collector current beyond its maximum permitted swing. The result of this is that an output power almost double that of a single transistor is produced.

A typical circuit is shown in Fig. 5.8. The driver circuit splits the phase of the input signal into two signals which are in antiphase to one another. This is done by taking the driver transformer secondary winding centre tap to the earth or common line. When no signal is present the only current flowing in the transistors is the quiescent current. This quiescent current does not produce any dc magnetization of the output transformer core because the magnetic forces effectively cancel. The output transformer can therefore be made smaller.

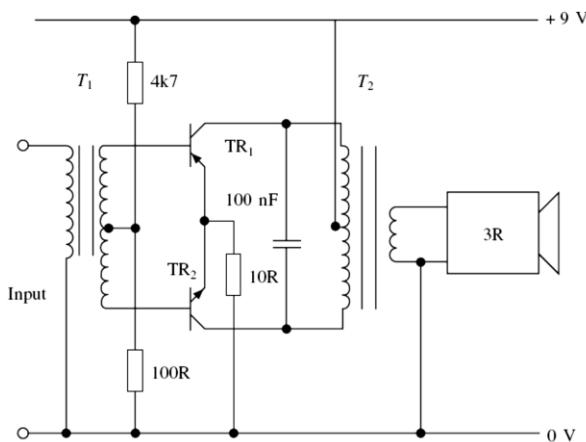


Fig. 5.8: A typical Class B Power Amplifier

When a signal is applied the antiphase base currents will produce antiphase collector currents. These collector currents effectively add in the output transformer and the ac power is fed via the secondary to R_L . The signal currents do not pass through the power supply or bias components. If the supply is derived from ac mains there is no tendency for mains hum to be introduced in this stage.

The operation of this type of amplifier is more clearly seen in Fig. 5.9, which shows the two sets of output characteristics for both transistors combined to form the composite characteristic. The point V_{cc} represents the operating point of both transistors and hence the two a.c. load lines coincide for transistors T_1 and T_2 . At point 1 on the input signal for T_1 the collector current is maximum and this is represented by D on the common characteristics. At point 2 the transistor is at cut-off point A and no collector current flows in either transistor. At point 3 the collector current of T_2 is maximum and the collector-emitter voltage is zero. This is point E . If all the variations of collector current and collector-emitter voltage were plotted the composite curve shown in Fig 5.10 would be produced.

5.6.1 Crossover distortion

Push-pull power amplifiers are subject to distortion as shown in Fig. 5.10(a). The mutual characteristics are shown in Fig. 5.10(b), in which the non-linear input characteristics cause distortion as one transistor turns on and another turns off. This effect may be reduced by introducing class AB biasing. Such biasing causes both the output transistors to conduct a small collector current when no signal is fed to the amplifier. Normally 0.6 V is provided by means of two resistors or two diodes. However, diodes are generally preferable because of temperature changes. This means that the potential difference across them will vary in the same way as the base-emitter voltage of the output transistors. One particular configuration is shown in Fig. 5.11, which shows the application of two diodes in the biasing circuit, preventing crossover distortion.

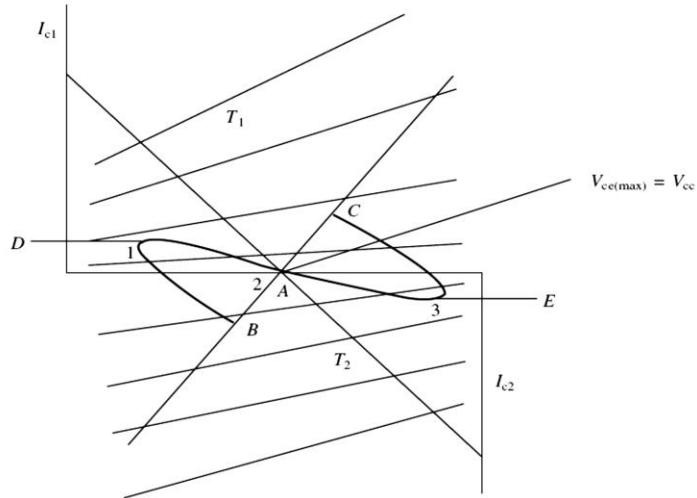


Fig. 5.9: Output waveform of a Class B Amplifier

5.2.3 Class B Complementary pair push-pull

This type of power amplifier performs in exactly the same way as the transformer type except that two different transistors are now used, i.e. npn and pnp, which complement each other to give a faithful reproduction of the input voltage. A typical practical circuit is shown in Fig. 5.11. Once again each transistor only handles 180° of the input signal, and when there is no input signal both the transistors are switched off. Hence there is no current drawn by the system at the output which once again increases the efficiency of the system. As before, if the input swings positive T_1 will

switch on and current will flow through R_L . When the input swings negative T_1 is off while T_2 is switched on, thus causing a current once again through R_L . T_1 thus pushes the current through R_L , while T_2 pulls the current through R_L . Several practical points should be noted about this circuit:

- (a) Figure 5.11 showed that the supply voltage indicated at the crossover point of the characteristic was V_{cc} . This is not the case with the complementary circuit, where the supply voltage is equal to half the maximum collector-emitter voltage of the transistors used. Otherwise the characteristics are identical for this configuration. In Figure 5.11 the two $10\ \Omega$ resistors set the bias conditions so that the junction is at half the supply voltage ($V_{cc}/2$).
- (b) Diodes are used rather than bias resistors because they are manufactured from silicon and hence have similar temperature characteristics to the transistors. Also if they are mounted on the same heat sink they will undergo similar temperature and voltage changes.
- (c) Complementary pair transistors are available in matched pairs in order to ensure they have identical characteristics.
- (d) The use of the diodes provides class AB biasing.

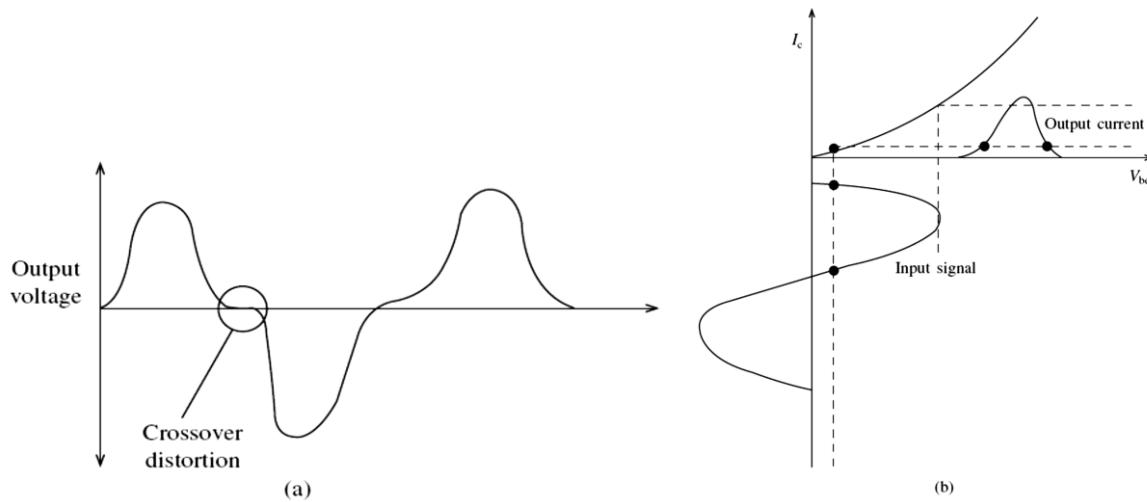


Fig. 5.10: Crossover distortion

5.2.3.1 Practical analysis of class B push-pull parameters

Both the push-pull transformer transforms and complementary pair types follow the same analysis, except that the supply voltage is V_{cc} in the transformer type and $V_{cc}/2$ for the complementary type. The parameters will be derived using the complementary symmetry circuit similar to the type used in Fig. 5.12. In this circuit a single power supply is used and the capacitor C ($100\ \mu F$ in this case) may be calculated by using the expression:

$$f = \frac{1}{2\pi CR_1}$$

Where R_l is the load resistance and f is the lower frequency of the frequency response. Note that if a dual power supply is used the coupling capacitor is not necessary. The collector current in each transistor takes the form of a series of rectified pulses.

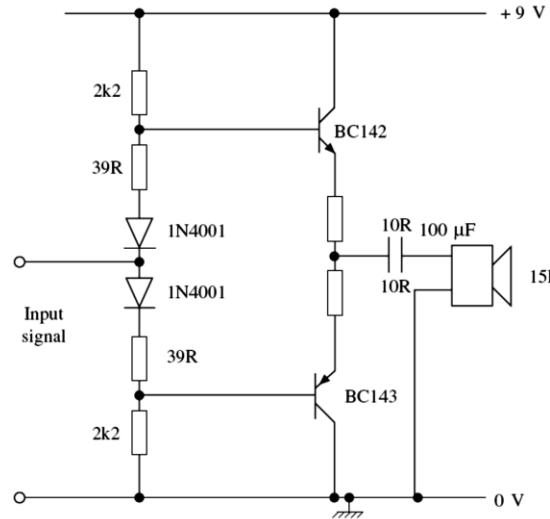


Fig. 5.11: A Class AB Push-Pull Amplifier

A Fourier analysis of this waveform will give an instantaneous value of

$$i_c = \frac{I_{c(max)}}{\pi} + \frac{I_{c(max)}}{2\pi} \sin\omega t - \frac{2I_{c(max)}}{3\pi} \cos 2\omega t$$

The first term in this expansion represents a d.c. component and the second term is the fundamental frequency component. Harmonics can be ignored as these are mostly reduced to a small percentage or eliminated entirely.

The fundamental rms. ac power produced by each transistor to a load is

$$P_{ac(rms)} = \left(\frac{I_{c(rms)}}{2\sqrt{2}} \right)^2 R_1$$

Note that R_l is the load into which the transistor feeds. Therefore total power delivered by both transistors is

$$P_{ac(rms)} = \frac{I_{c(max)}^2 R_1}{4}$$

Also the d.c. power taken by each transistor is

$$\frac{I_{c(max)} V_{cc}}{2\pi}$$

Hence total power is

$$P_{dc} = \frac{I_{c(max)} V_{cc}}{\pi}$$

So the efficiency is given by

$$\eta = \frac{P_{ac}}{P_{dc}} \times 100\% = \frac{I_{c(max)}^2 R_1 \pi}{4 I_{c(max)} V_{cc}} \times 100\% = \frac{I_{c(max)} R_1 \pi}{4 V_{cc}} \times 100\%$$

The same solution can be achieved by using

$$P_{ac(rms)} = \left[\frac{(I_{c(max)} - I_{c(min)}) (V_{ce(max)} - V_{ce(min)})}{2\sqrt{2} \cdot 2\sqrt{2}} \right] \times 2$$

As $I_{c(min)}$ and $I_{ce(min)}$ are small then

$$P_{ac(rms)} = \frac{I_{c(max)} \times V_{cc} \times 2}{8} = \frac{I_{c(max)} \times V_{cc}}{4}$$

One final consideration when selecting an integrated circuit or transistor for an application is its power rating. The total collector dissipation is given as

$$P_c = P_{dc} - P_{ac}$$

$$= \frac{I_{c(max)} V_{cc}}{\pi} - \frac{I_{c(max)} V_{ce(max)}}{2}$$

Since

$$I_{c(max)} = \frac{V_{ce(max)}}{R_1}$$

$$P_d = \frac{V_{cc} V_{ce(max)}}{\pi R_1} - \frac{V_{ce(max)}^2}{2 R_1}$$

Differentiate (5.36) to determine the maximum dissipation:

$$\frac{dP_d}{dV_{ce(max)}} = \frac{V_{cc}}{\pi R_1} - \frac{2V_{ce(max)}}{2R_1}$$

Therefore

$$V_{ce(max)} = \frac{V_{cc}}{\pi}$$

Substituting (5.37) into (5.36) gives

$$P_{d(max)} = \frac{V_{cc}^2}{\pi^2 R_1} - \frac{V_{cc}^2}{2\pi^2 R_1} = \frac{V_{cc}^2}{2\pi^2 R_1}$$

Since the maximum power occurs when $V_{ce(max)} = V_{cc}/2$ for complementary symmetry, and this occurs at $P_{ac(max)} = V_{cc}^2 / 8R_1$ then

$$P_{c(max)} = \frac{4P_{ac(max)}}{\pi^2} \cong 0.4P_{ac(max)}$$

This is the total power dissipation for both transistors used in a push-pull arrangement.

5.4 Calculating power and efficiency

Any machine is required to convert energy into a usable form, and the power amplifier is no exception. In this case the dc power from the supply has to be converted to ac power to drive an external device, and this has to be done efficiently. Several examples are given below which should clarify the use of different configurations under different applications.

5.5: Worked Examples

Example 5.5.1

The supply voltage of a complementary amplifier is 30 V and the output feeds into a load of 12 Ω. Determine:

- The maximum collector current if an efficiency of 60% is required;
- The maximum rated values of the transistors used.

Solution

(a)

$$\eta = \frac{I_{c(max)} R_L}{4V_{cc}}$$

$$I_{cc(max)} = \frac{4V_{cc}\eta}{R_L} = \frac{4 \times 30 \times 0.6}{12\pi} = 1.91A$$

$$P_{c(max)} = \frac{4P_{ac(max)}}{\pi^2}$$

$$P_{ac(max)} = \frac{V_{cc}^2}{8R_L} = \frac{900}{96}$$

$$P_{c(max)} = \frac{4x900}{96\pi^2} = 3.80W$$

Hence each transistor rated at 1.90 W.

Example 5.5.2

A class B push-pull transformer power amplifier has an output load of 50 Ohms. Determine:

- The maximum collector current produced in the primary by both transistors if the a.c. power delivered to the primary is 12.5 W;
- The value of supply voltage required under these conditions;

(c) The efficiency of the amplifier.

Solution

(a)

Since, for transformer push-pull,

$$P_{ac(rms)} = \frac{I_{c(max)}^2 R_L}{4}$$

$$I_c = \sqrt{\frac{4 \times 12.5}{50}} = 1A$$

(b)

$$P_{ac(rms)} = \frac{I_{c(max)} V_{cc}}{2}$$

$$V_{cc} = \frac{2P_{ac(rms)}}{I_{c(max)}} = \frac{2 \times 12.5}{1} = 25V$$

(c)

$$\eta = \frac{P_{ac(rms)}}{P_{dc}} \times 100\%$$

$$P_{dc} = \frac{2I_{c(max)} V_{cc}}{\pi} = \frac{2 \times 1 \times 25}{\pi} = 15.0$$

$$\eta = 1.25 \times \frac{\pi}{50} \times 100\% = 78.5\%$$

Example 5.5.3

A complementary push-pull amplifier has to deliver 2.5 W into a load of 8Ω . Determine:

- (a) The maximum power dissipation required for each transistor;
- (b) The supply voltage required;
- (c) The peak load current.

Solution

(a)

$$\frac{4P_{\text{ac(max)}}}{\pi^2} = \frac{4 \times 2.5}{\pi^2} = 1.01 \text{ W}$$

(b) Since

$$P_{\text{c(max)}} = \frac{V_{\text{cc}}^2}{2\pi^2 R_l}$$

$$V_{\text{cc}} = \sqrt{P_{\text{c(max)}} 2\pi^2 R_l} = \sqrt{\frac{10}{\pi^2} \times 2\pi^2 \times 8} = \sqrt{160} = 12.65 \text{ V}$$

(c)

$$P_{\text{ac(rms)}} = \frac{V_1^2}{R_l}$$

$$\therefore V_1 = \sqrt{P_{\text{ac(rms)}} R_l} = \sqrt{2.5 \times 8} = 4.5 \text{ V}$$

$$\therefore V_{(\text{max})} = \sqrt{2} \times \sqrt{20} = \sqrt{40} = 6.32 \text{ V}$$

\therefore Peak load current is

$$I_{(\text{max})} = \frac{V_{(\text{max})}}{R_l} = \frac{6.32}{8} = 0.79 \text{ A}$$

Example 5.5.4

The complementary push-pull audio amplifier shown in Fig. 5.14 has to provide 5 W into a load of 4Ω . The 3 dB bandwidth of the amplifier has to be flat between 80 Hz and 18 kHz. The data for the two transistors are as follows: $I_{\text{C(max)}} = 4 \text{ A}$, $P_{(\text{max})} = 36 \text{ W}$, $h_{\text{FE}} = 40$ and $V_{\text{CE(max)}} = 45 \text{ V}$. Determine:

- The value of C_1 ;
- The value of V_{CE} ;
- The value of base current;
- The values of R_5 and R_6

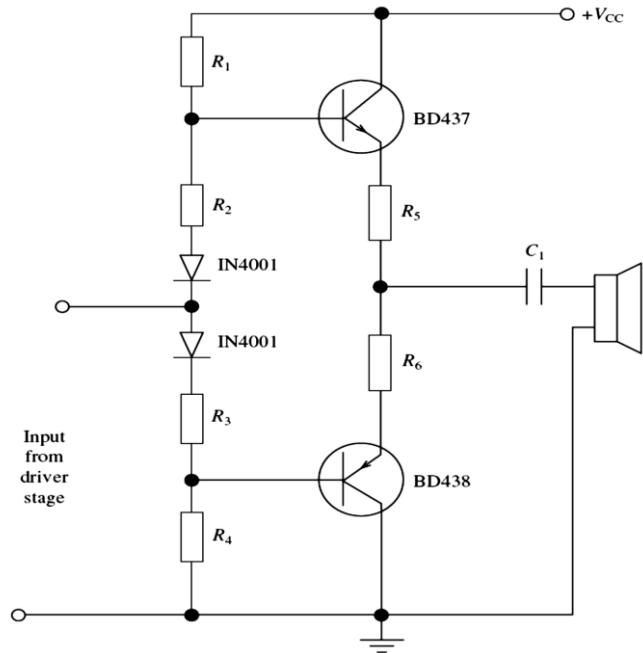


Fig. 5.14

Solution

(a)

$$f = \frac{1}{2\pi R_1 C_1}$$

$$\therefore C_1 = \frac{1}{2\pi f R_1} = \frac{1}{2\pi \times 80 \times 4} = 497.4 \mu\text{F}$$

Select a 500 μF capacitor

(a) The specification is for 5 W into a 4 Ω load.

$$\therefore V_L = \sqrt{P_{AC(\text{rms})} \times R_L} = \sqrt{5 \times 4} = 4.47 \text{ V}$$

$$\therefore V_{\text{max}} = \sqrt{2} \times \sqrt{20} = 6.32 \text{ V}$$

Example 5.5.5

An amplifier has to work with a 35 V supply and has to be capable of drawing a current of 2.5 A from the supply. A single npn transistor is biased so that under the quiescent conditions $I_C = 1.75$ A and $V_{CE} = 30$ V. Under these conditions 35 W is applied to the load when the output voltage is 18 V r.m.s. Select a suitable transistor.

Solution

From the information given we obtain

$$P_{DC} = 2.5 \times 35 = 87.5 \text{ W}$$

$$P_{AC} = 35 \text{ W}$$

$$P_{CQ} = P_{DC} - P_{AC} = 87.5 - 35 = 52.5 \text{ W}$$

$$I_{rms} = \frac{P_{AC}}{V_{rms}} = \frac{35}{18} = 1.95 \text{ A}$$

Any transistor with ratings higher than these requirements will be suitable – for example, a TIP41 with $P_{tot} = P_{C(max)} = 65 \text{ W}$, $I_{CQ} = 6 \text{ A}$ and $V_{CEQ} = 40 \text{ V}$.

Example 5.5.6

A single-ended transistor power amplifier takes a mean collector current of 1 A from a 12 V supply and delivers an ac power of 2.4 W to a transformer-coupled load. Calculate:

- The collector dissipation if all other losses are ignored;
- The collector efficiency;
- The turns ratio of the transformer if the output resistance of the transistor is 1.2 kΩ and the load resistance is 12 Ω.

Solution

(a)

$$P_{dc} = 12 \times 1 = 12 \text{ W}$$

(b)

$$\eta = \frac{2.4 \times 100}{12} = \frac{P_{ac}}{P_{dc}} \times 100 = 20\%$$

(c)

$$n = \sqrt{\frac{R_1}{R_2}} = \sqrt{\frac{1200}{12}} = 10 : 1$$

Example 5.5.8

Example 5.5.9

A complementary pair class B push-pull amplifier has a supply voltage of 45 V and the transistors are biased so that they are sinusoidally driven to provide a current which is 80% of the maximum value. Calculate:

- (a) The output power supplied to a speaker having a resistance of 15 Ω;
- (b) The collector efficiency;
- (c) The power rating of the transistors.

Solution

- (a) The output power is given by

$$\frac{V_{CC} \times I_{C(max)}}{4} = \frac{V_{CC}^2}{8R_L}$$

Hence

$$I_{C(max)} = \frac{V_{CC}}{2R_L} = \frac{45}{30} = 1.5 \text{ A}$$

Biasing gives 80% swing, so

$$I_{C(max)} = 0.8 \times 1.5 = 1.2 \text{ A}$$

Hence output power is

$$\frac{V_{CC} \times I_{C(max)}}{4} = \frac{45 \times 1.2}{4} = 13.5 \text{ W}$$

(b)

$$P_{dc} = \frac{I_{C(max)} V_{CC}}{\pi} = \frac{1.2 \times 45}{\pi} = 17.2 \text{ W}$$

$$\eta = \frac{13.5}{17.2} \times 100 = 78.5\%$$

- (b) The maximum output power is given by

$$P_{(max)} = \frac{V_{CC}^2}{8R_L} = \frac{(45)^2}{8 \times 15} = 16.9 \text{ W}$$

The maximum collector power dissipation is given approximately by $0.4P_{max}$:

$$P_{C(max)} = 0.4 \times 16.9 = 6.8 \text{ W}$$

Therefore power rating of each transistor is 3.4 W.

Example 5.10

An amplifier has to work with a 38 V supply and draw a current of 2 A from the d.c. supply. A single npn transistor is biased so that under quiescent conditions $I_C = 1.64 \text{ A}$,

$V_{CE} = 25 \text{ V}$. This delivers 35 W into its load when the output voltage is 20 V r.m.s. Select a suitable transistor.

Solution

The steps involved in this type of practical problem are given below

$$P_{dc} = I_C \times V_{CC} = 2 \times 38 = 76 \text{ W}.$$

$$P_{ac} = 35 \text{ W}$$

The quiescent power is given by

$$P_{CQ} = I_{CQ} \times V_{CQ} = P_{dc} - P_{ac} = 41 \text{ W}$$

So

$$I_{C(rms)} = \frac{P_{ac}}{V_{o(rms)}} = \frac{35}{20} = 1.75 \text{ A}$$

Hence any transistor with ratings higher than these requirements will be suitable. A TIP41 is a suitable choice as it has the following characteristics:

$$P_{tot} = P_{c(max)} = 65W \quad \text{and} \quad I_{CQ} = 6 \text{ A}$$

$$V_{CEQ} = 40 \text{ V} \quad \text{and} \quad P_{CQ} = 1.64 \times 25 = 41 \text{ W}$$