

40 - squares

4 - corners

2 - pads/centers

120 Ω/square

$$R = 120 \Omega/\text{square} \times 40 \text{ square}$$

$$+ 4 \times 0.6 \times 120 + 2 \times 0.6 \times 120$$

$$R = 5232 \Omega$$

Z



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SCHOOL OF ENGINEERING

DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING

Level 300: First Semester Examinations 2019/2020

Bachelor of Science (Computer Engineering, Electrical & Electronic Engineering)

ELNG 303: LINEAR ELECTRONIC CIRCUITS

DECEMBER, 2019

MDK

Time: 2½ hours

INSTRUCTIONS: ANSWER ALL FOUR QUESTIONS)

Question One [3+(2+4)+4=13]

- a) With the aid of diagrams, briefly describe the process of photolithography used in the fabrication of monolithic ICs.
- b) A circuit is built around a bi-polar NPN transistor. The base network has a diode and a capacitor in series while the collector is connected to a power supply through a resistor. If the emitter is connected to ground:
 - i) Draw the circuit
 - ii) Provide all the masking layout of the circuit
- c) Fig1.1 shows a p-diffusion resistor fabricated with a sheet resistance of 120 Ohm per square. The corners and the pads are estimated to have 0.6 of the value of a regular sheet resistance. Find the value of the resulting resistor.

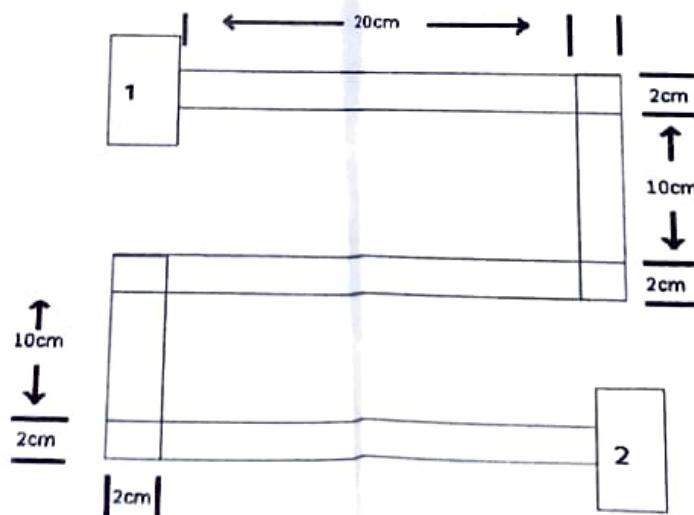


Fig1.1

- * Infinite input impedance
- ✗ Infinite bandwidth
- * Zero output impedance
- * Infinite open-loop voltage gain
- * Infinite common-mode rejection ratio.

Question Two [2+4+6+6=18]

- a) Mention the characteristics of an ideal op-amp.
- b) Draw a shunt regulator and clearly show the four main elements. Derive an expression for the output voltage.
- c) A differential amplifier has an output voltage given by $V_o = 9 V_1 - 10V_2$. The two inputs are $V_1 = 10 \text{ mV}$ and $V_2 = 20 \text{ mV}$. Determine common mode input voltage, common mode gain and the differential gain.
- d) In Op-Amp circuit of Fig. 2.1, find V_o in terms of V_1 and V_2 assume the ideal op amp model. Find an expression for V_o . If $V_{I1} = 1.5\text{V}$ and $V_2' = 3.0\text{V}$, find V_o for $R_1 = 1\text{k}\Omega$ and $R_2 = 2\text{k}\Omega$

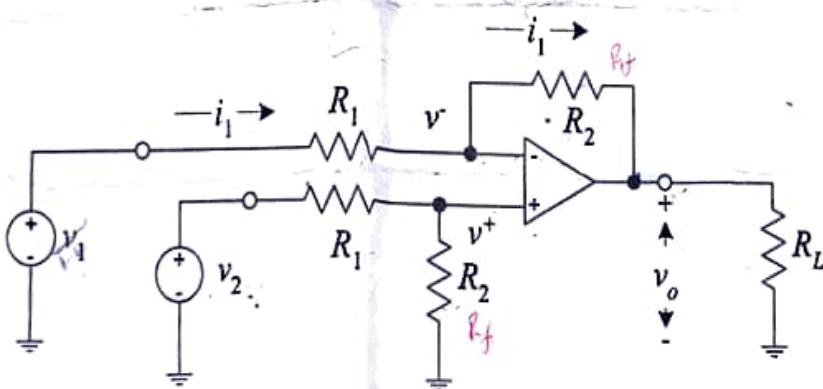


Fig 2.1

$$\text{Max. } \eta = \frac{I_1 V_L \times 10^{-6}}{4 V_{cc}}$$

Answer $V_{cc} \rightarrow V_{cc}$

$$\eta = \frac{I_1 \times 10^{-6}}{4}$$

$$\eta = 78.5\%$$

Question Three [2+4+(2x3)=12]

- a) State and explain the various classifications of power amplifiers.
A, AB, B, C, D
- b) For a class B power amplifier, show that the maximum efficiency is 78.5%.
- c) For a class B amplifier providing a 20V peak-to-peak signal to an 8Ω speaker and a power supply of $V_{cc} = 15\text{V}$, determine:
 - Input power
 - Output power
 - Circuit efficiency

$$P_{dc} = \frac{2V_{cc} I_R}{\pi} = , \quad i_R = \frac{2}{8}$$

$$P_{o(av)} = \frac{V_L^2}{2R_L} = \quad V_L = V_{cc} = 20$$

$$\eta = \frac{P_{o(av)}}{P_{dc}} \times 10^2 \quad \text{Page 2 of 3}$$

Question Four [4+4+(3x3)=17]

M.D.K

Consider the common-emitter BJT amplifier circuit shown in Figure 4.1. Take $\beta_1 = \beta_2 = 200$, $V_{BE} = 0.7V$ and thermal voltage as 26V. Answer the following questions.

(a) Determine the emitter current I_{E2} , I_E and hence r_{e2} and r_{e1}

(b) Draw the AC equivalent circuit and determine:

- Input impedance, Z_1 , Z_2 and Z_{in}
- Gain of the transistor, A_{v2} and A_{v1}
- Output voltage gain with signal, A_{vs}

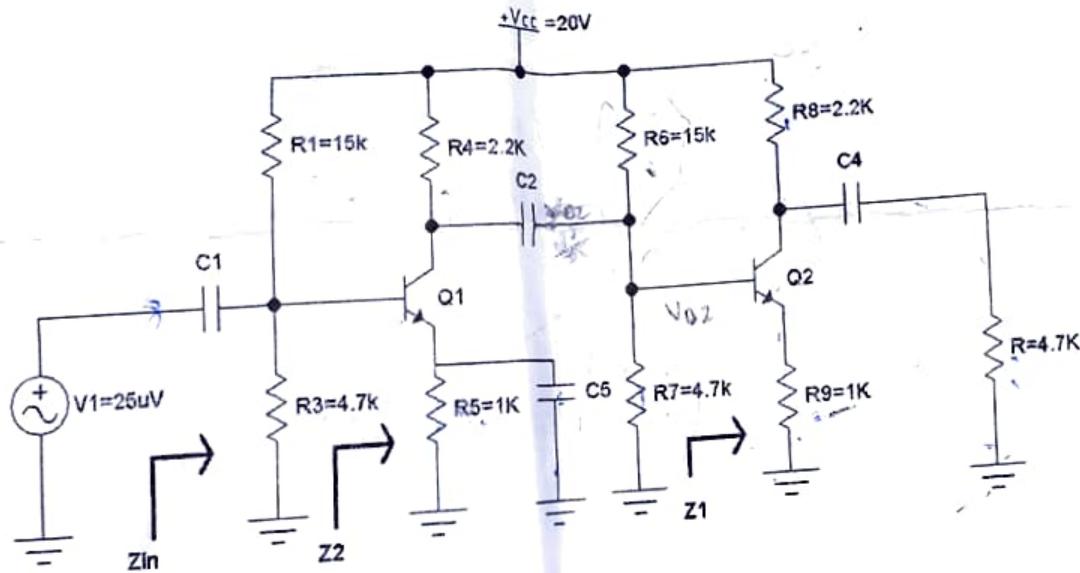


Fig. 4.1

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DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING

Level 300: End of Semester Examinations 2021/2022

Bachelor of Science (Computer, Electrical & Electronic Engineering)

ELNG 303: LINEAR ELECTRONIC CIRCUITS

May/June, 2022

MDK

Time: 2½ hours

Material required: Class material (**To be brought in by students**)

INSTRUCTIONS: ANSWER ALL QUESTIONS

Question 1 (12 Marks)

- (a) State and explain briefly the five planar processes in the fabrication of monolithic IC
- State the main difference between negative and positive photoresist and at what condition each is applied
 - State the significance of passivation in IC fabrication and the material used.
- (b) Provide a step-by-step masking levels for the fabrication of a **NPN** Transistor indicating the type of photo-resist used.

Question 2 (20 Marks)

MDK

The two-stage amplifier shown in Fig. 2 is designed with a **FET**, TR1 and silicon **BJT**, Q1 with the manufacturer's specifications for β (Q1) at 25°C as 150 and g_m (TR1) as $3500\mu\text{A}$. Given $R_g=1.5\text{k}\Omega$ $R_i=6\text{ M}\Omega$, $R_2=4\text{M}\Omega$ $R_d=2.4\text{k}\Omega$, $R_s=500\Omega$, $R_3=15\text{k}\Omega$, $R_4=4.7\text{k}\Omega$, $R_c=2.7\text{k}\Omega$, $R_e=470\Omega$, $R_L=2.2\text{k}\Omega$ and supply voltage as 20V. Using the Fig.2 and component values given, answer the following questions.

Calculate:

- Draw the small signal equivalent circuit using the model treated in class
- Emitter current I_E
- Emitter resistance r_e
- Voltage gain at stage 2 (BJT), A_{v2}
- Calculate input impedance of the second stage BJT), Z_2
- Calculate the gain of the first stage (FET), A_{v1}
- Calculate the input impedance of the first stage Z_1
- Calculate the overall gain with signal, A_{vs}
- If V_s is a sinusoidal voltage of $5\text{mV}\cos\omega t$, what will the output voltage be?
- On the same graph plot the input and output voltage against ωt .

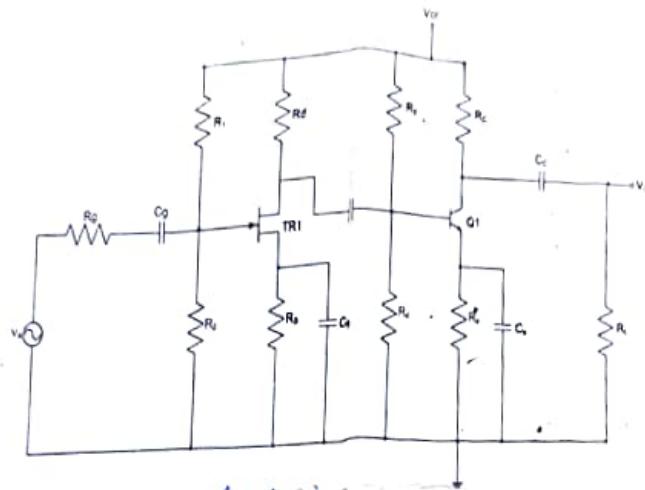


Fig. 2

MDK

Question 3 (16 Marks)

- (a) State and explain the difference between Class A and Class B power amplifiers.
- (b) How do you minimize the effect of crossover distortion in class B power amplifier?
- (c) A class A power amplifier is supplied with 20V and biased to operate at a quiescent base current of 19.3mA with a base peak current of 10mA and a collector load of 20Ω . Given that $\beta=25$, calculate the amplifier:
 - i Input power, $P_{i(dc)}$
 - ii Output power, $P_{o(ac)}$
 - iii Efficiency, η
- (d) A complementary push-pull amplifier has to deliver 2.5 W into a load of 8Ω . Determine:
 - (i) The maximum power dissipation required for each transistor;
 - (ii) The supply voltage required;
 - (iii) The peak load current.

MDR

Question 4 (12 Marks)

- (a) State five characteristics of an ideal op-amp.
- (b) For the difference amplifier shown in Fig. 4.1, find an expression for the output voltage V_o . Evaluate V_o if $R_1 = 10k\Omega$, $R_2 = R_3 = 15k\Omega$ and $R_f = 20k\Omega$.
- (c) Evaluate the gain.

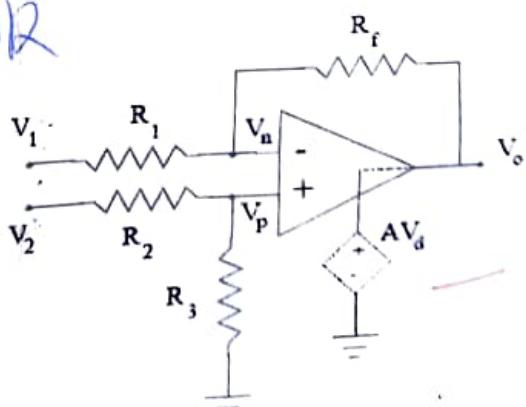


Fig. 4.1



UNIVERSITY OF ENERGY AND NATURAL RESOURCES, SUNYANI, GHANA

SCHOOL OF ENGINEERING

DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING

Level 300: First Semester Examinations 2020/2021

Bachelor of Science (Computer Engineering, Electrical & Electronic Engineering)

ELNG 303: LINEAR ELECTRONIC CIRCUITS

April, 2021

Time: 2½ hours

MDK

Material required: Class material (To be brought in by students)

STRUCTIONS: ANSWER ALL QUESTIONS (each question carries 15marks)

Question 1 ✓

(a) The following processes are used in the fabrication of monolithic ICs, explain each of them in detail:

- i. Oxidation
- ii. Diffusion
- iii. Epitaxy
- iv. Photolithography
- v. Thin Film Deposition



(b) Using the list in (a) provide a step-by-step masking levels of the fabrication of NPN transistor indicating the type of photo-resist used.

Question 2

MDK

The two-stage amplifier shown in Fig. 2 is designed with a FET, TR1 and silicon BJT, Q1 with the manufacturer's specifications for β (Q1) at 25°C as 150 and g_m (TR1) as $3500\mu\text{S}$. Given $R_g=1.5\text{k}\Omega$, $R_1=6\text{ M}\Omega$, $R_2=4\text{M}\Omega$, $R_d=2.4\text{k}\Omega$, $R_s=500\Omega$, $R_3=15\text{k}\Omega$, $R_4=4.7\text{k}\Omega$, $R_e=2.7\text{k}\Omega$, $R_L=2.2\text{k}\Omega$ and supply voltage as 20V. Using the Fig. 2 and component values given, answer the following questions.

Calculate:

- i) Emitter current I_E
- ii) Emitter resistance r_e
- iii) Voltage gain at stage 2, A_{v2}
- iv) Calculate input impedance of the second stage, Z_2
- v) Calculate the gain of the first stage, A_{v1}
- vi) Calculate the input impedance of the first stage Z_1
- vii) Calculate the overall gain, A
- viii) If v_g is a sinusoidal voltage of $5\text{mV}\cos\omega t$, what will the output voltage be?

V_{o2}



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SCHOOL OF ENGINEERING
DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING
Level 300 Mid-Semester Examinations 2021/2022

Bachelor of Science (Computer, Electrical and Electronic Engineering)

ELNG 303: LINEAR ELECTRONIC CIRCUITS
April, 2022

Time: 1 hour

Attempt all questions

Question 1

(a) Briefly explain the following terms as applied to IC fabrication

- (i) Epitaxial Growth
- (ii) Photolithography
- (iii) Thin film deposition

(b) A circuit is built around a bi-polar NPN transistor. The base network has a diode and a capacitor in series while the collector is connected to a power supply through a resistor. If the emitter is connected to ground:

- i) Draw the circuit
- ii) Provide all the masking layout of the circuit.

MDK

Question 2

Given the circuit diagram of Fig. 2 with $V_{cc} = 12V$, and $\beta=52$.

(a) Using the r_e model; draw the small signal equivalent circuit.

(b) Determine:

- (i) The gain of the transistor.
- (ii) The input impedance of the transistor.
- (iii) The overall gain of the amplifier.

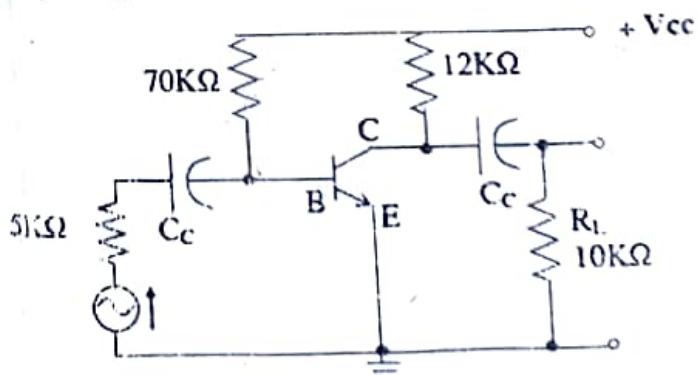


Fig. 2

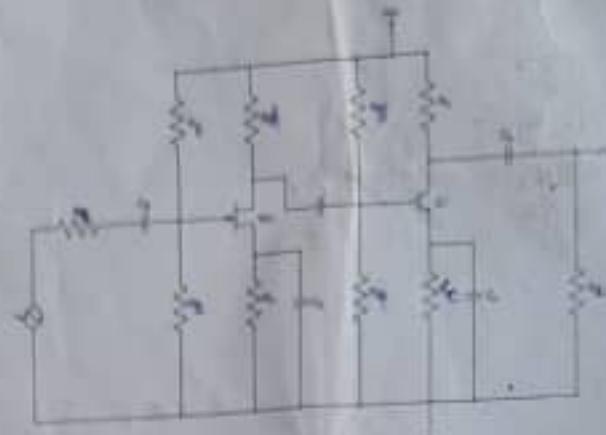


Fig. 2

$$\frac{-R_C}{R_C + R_L} = \frac{2.2}{19.5 + 15.2} = 0.55$$

Question 3 (16 Marks)

- State and explain the difference between Class A and Class B power amplifiers.
- How do you minimize the effect of crossover distortion in class B power amplifier?
- A class A power amplifier is supplied with 20V and biased to operate at a quiescent base current of 19.3mA with a base peak current of 10mA and a collector load of 20Ω. Given that $\beta=25$. Calculate the amplifier
 - Input power, P_{in}
 - Output power, P_{out}
 - Efficiency, η
- A complementary push-pull amplifier has to deliver 2.5 W into a load of 8 Ω. Determine
 - The maximum power dissipation required for each transistor.
 - The supply voltage required.
 - The peak load current.

Question 4 (12 Marks)

- State five characteristics of an ideal op-amp.
- For the difference amplifier shown in Fig. 4.1, find an expression for the output voltage V_o . Evaluate V_o if $R_1 = 10k\Omega$, $R_2 = R_3 = 15k\Omega$ and $R_f = 20k\Omega$.
- Evaluate the gain.

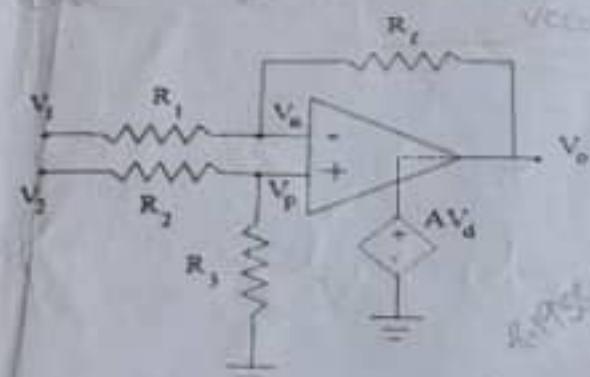


Fig. 4.1



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SCHOOL OF ENGINEERING

DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING

Level 300: End of Semester Examinations 2021/2022

Bachelor of Science (Computer, Electrical & Electronic Engineering)

ELNG 303: LINEAR ELECTRONIC CIRCUITS

Time: 2½ hours

May/June, 2022

Material required: Class material (To be brought in by students)

INSTRUCTIONS: ANSWER ALL QUESTIONS**Question 1 (12 Marks)**

- (a) State and explain briefly the five planar processes in the fabrication of monolithic IC
- State the main difference between negative and positive photoresist and at what condition each is applied
 - State the significance of passivation in IC fabrication and the material used.
- (b) Provide a step-by-step masking levels for the fabrication of a **NPN Transistor** indicating the type of photo-resist used.

Question 2 (20 Marks)

The two-stage amplifier shown in Fig. 2 is designed with a **FET**, TR1 and silicon **BJT**, Q1 with the manufacturer's specifications for β (Q1) at 25°C as 150 and g_m (TR1) as 3500 μ A/ V . Given $R_g = 1.5k\Omega$, $R_1 = 6M\Omega$, $R_2 = 4M\Omega$, $R_d = 2.4k\Omega$, $R_s = 500\Omega$, $R_3 = 15k\Omega$, $R_a = 4.7k\Omega$, $R_c = 2.7k\Omega$, $R_e = 470\Omega$, $R_L = 2.2k\Omega$ and supply voltage as 20V. Using the Fig. 2 and component values given, answer the following questions.

Calculate

- Draw the small signal equivalent circuit using the model treated in class
- Emitter current I_E
- Emitter resistance r_e
- Voltage gain at stage 2 (BJT), A_{v2}
- Calculate input impedance of the second stage BJT), Z_2
- Calculate the gain of the first stage (FET), A_{v1}
- Calculate the input impedance of the first stage Z_1
- Calculate the overall gain with signal, A_{vs}
- If V_s is a sinusoidal voltage of $5mV \cos \omega t$, what will the output voltage be?
- On the same graph plot the input and output voltage against ωt .

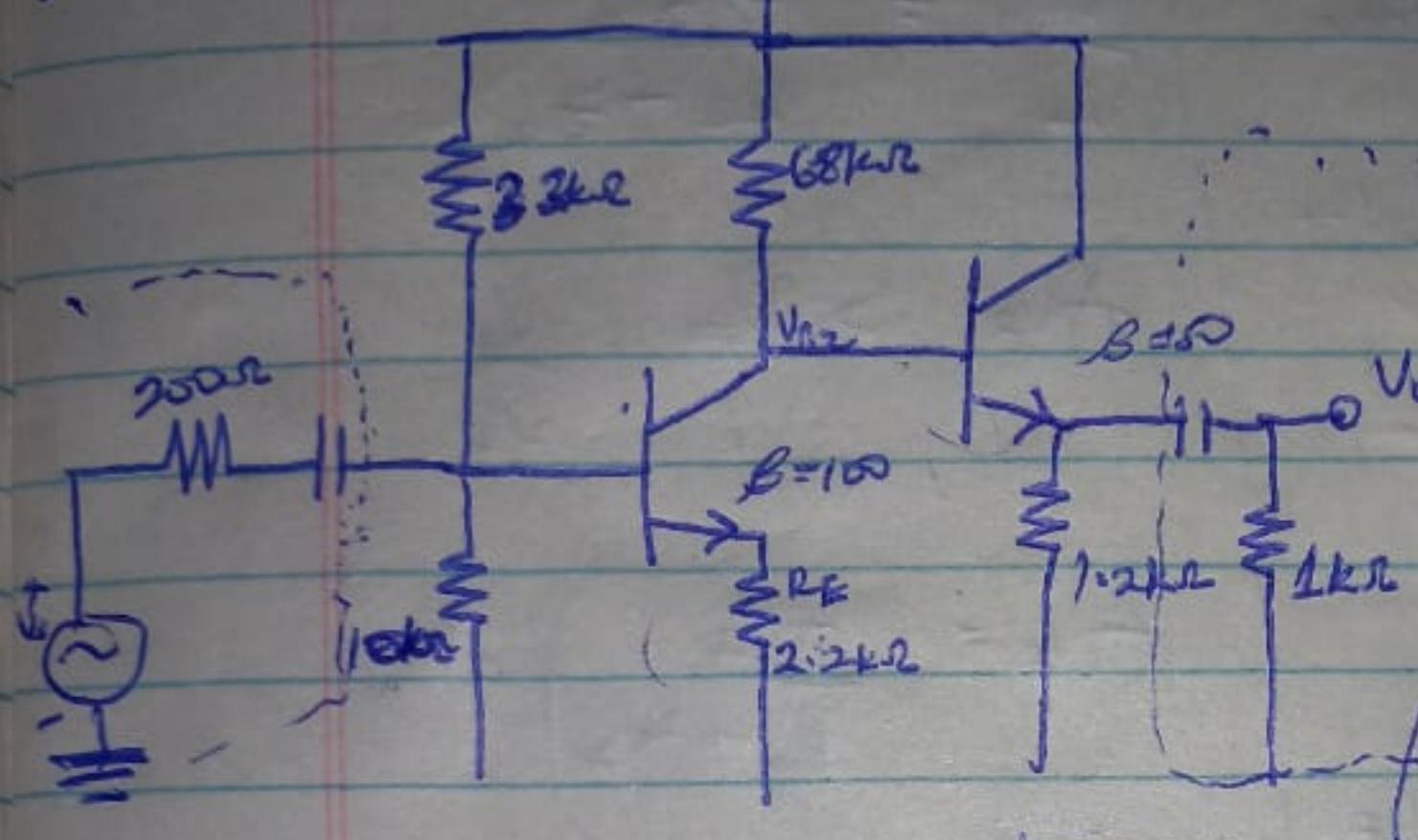
$$A_{V3} = A_1 \left(\frac{z_2}{R_o + R_{S2}} \right)$$

$$\Rightarrow 171.02 \left(\frac{10}{0.3k+10} \right)$$

$$A_{IS} = 166.03 \underline{5.52}$$

Q

$$V_{CE} = 14V$$



2nd Transistor

$$V_{CE} = I_{c2}R_L + V_{B2}$$

$$V_{B2} = V_{CC} - I_{c2}R_L$$

$$V_{B2} = V_{BE} + V_E$$

$$V_E = V_{B2} - V_{BE}$$

$$V_E = \frac{I_E}{R_E}; \bar{E}_2 = \frac{V_E}{R_E}$$

Find $I_E, I_C, V_{B2}, I_{B2}, V_{CE2}$

Small signal

$$\frac{R_m}{R_m + R_B} = R_1 // R_2$$

$$V_{B2} = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$V_E = r_e \bar{I}_B \quad Z_i = \frac{V}{\bar{I}_B}$$

$$r_e = 26mV$$

$$Z_i = \frac{i_B(\beta + 1)r_e}{1 + \beta r_e}$$

$$V_{BB} = I_B R_B + V_{BE} + V_E$$

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E$$

$$\text{But } I_E = (\beta + 1) I_B$$

$$V_{BB} - V_{BE} = I_B (R_B + R_E + \beta R_E) \quad \text{--- (1)}$$

$V_{BB} = V_{BE}$ from (1) find

the I_B

$$Z_o = (\beta + 1) r_e$$

$\beta \gg$

$$Z_i = \beta r_e$$

$$V_E = \bar{I}_E r_e$$

$$Z_i = \frac{V_E}{\bar{I}_B} = \frac{(\beta + 1) \bar{I}_B r_e}{\bar{I}_B}$$

$$V_{in} = i_e R_E$$

$$i_e \approx i_c$$

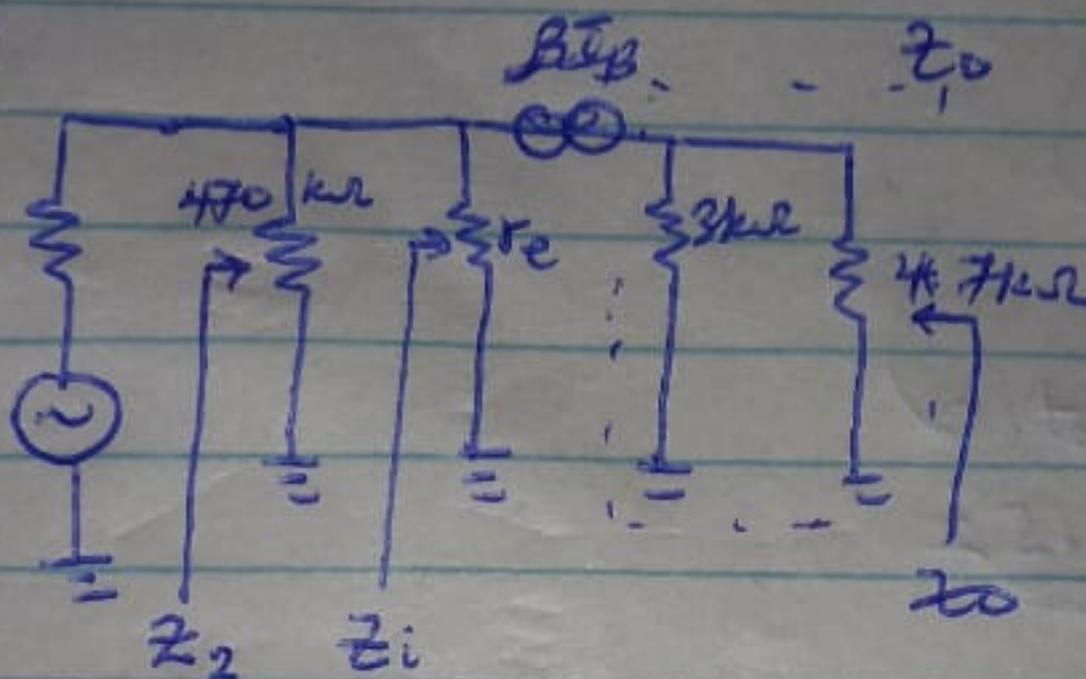
$$V_{in} = i_c R_E$$

$$V_{out} = i_c R_L'$$

$$A_v = \frac{V_{out}}{V_{in}}$$

$$\rightarrow \frac{i_c R_L'}{i_c R_E}$$

$$A_v = \frac{R_L'}{r_e}$$



$$z_1 = B_E r_e$$

$$\Rightarrow 100(10)$$

$$\Rightarrow 1000 \Omega$$

$$\Rightarrow 1k\Omega$$

$$z_2 \Rightarrow 1 \cdot 200 \Omega$$

$$R_L' \parallel R_L$$

$$z_0 = 3k\Omega \parallel 4.7k\Omega$$

$$\Rightarrow \frac{3 \times 4.7}{3 + 4.7}$$

$$\Rightarrow 1.83k\Omega$$

DC analysis

$$R_B = 4.7k\Omega$$

$$V_B = \frac{V_{cc} - V_{BE}}{R_B}$$

$$V_B = \frac{12 - 0.7}{4.7k}$$

$$I_B = 2.553 \text{ mA}$$

$$\Rightarrow 2.404 \text{ mA}$$

$$z_2 = R_L' \parallel B_E r_e$$

$$\frac{4.7k \times 10.7}{4.7k + 10.7}$$

$$\Rightarrow 9.99 \Omega$$

$$\Rightarrow 9.99 \Omega$$

$$\approx 10 \Omega$$

$$I_C = B_E I_B$$

$$I_C = (1 + B) I_B$$

$$= (1 + 100) I_B$$

$$\Rightarrow 2.43 \text{ mA}$$

$$A_v = \frac{z_0}{z_1}$$

$$\Rightarrow R_L'$$

$$r_e$$

$$\Rightarrow 1.83k$$

$$10.7$$

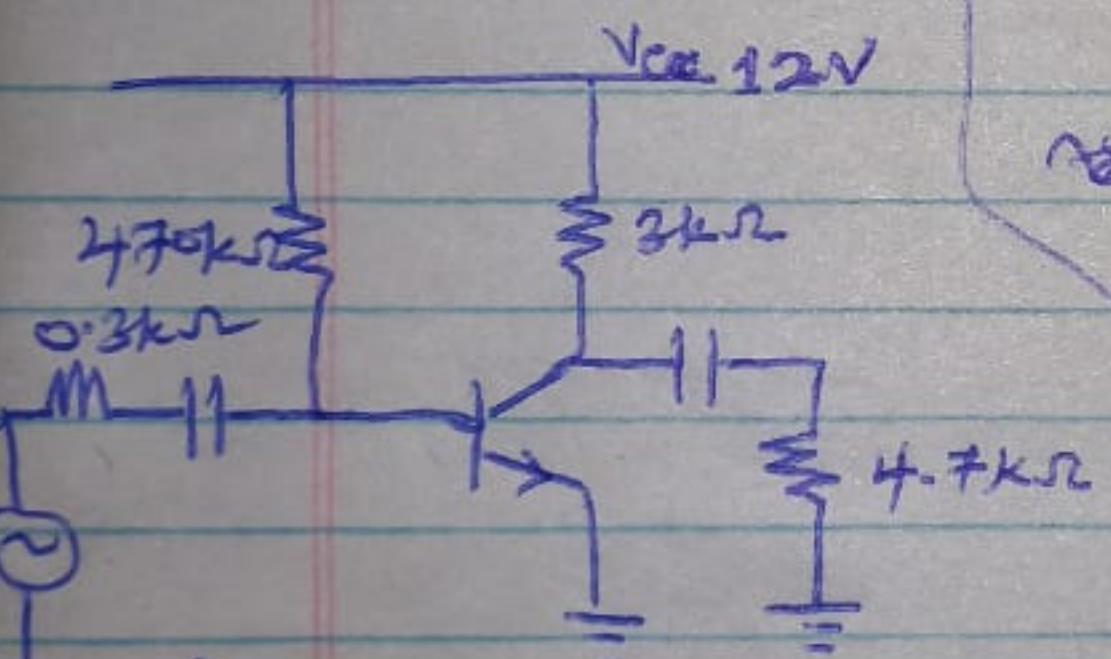
$$r_e = \frac{26 \text{ mV}}{2.43 \text{ mA}}$$

$$= 10.699 \Omega$$

$$\approx 10.70 \Omega$$

$$A_v = 188$$

$$A_v = 188$$



draw eqn out.

Find r_e , z_1 , z_0 , A_v

A_{v_s} , z_2

$$I_F = (1 + B) I_B$$

$$= (1 + 100) I_B$$

$$\Rightarrow 2.43 \text{ mA}$$

$$A_v = \frac{z_0}{z_1}$$

$$\Rightarrow R_L'$$

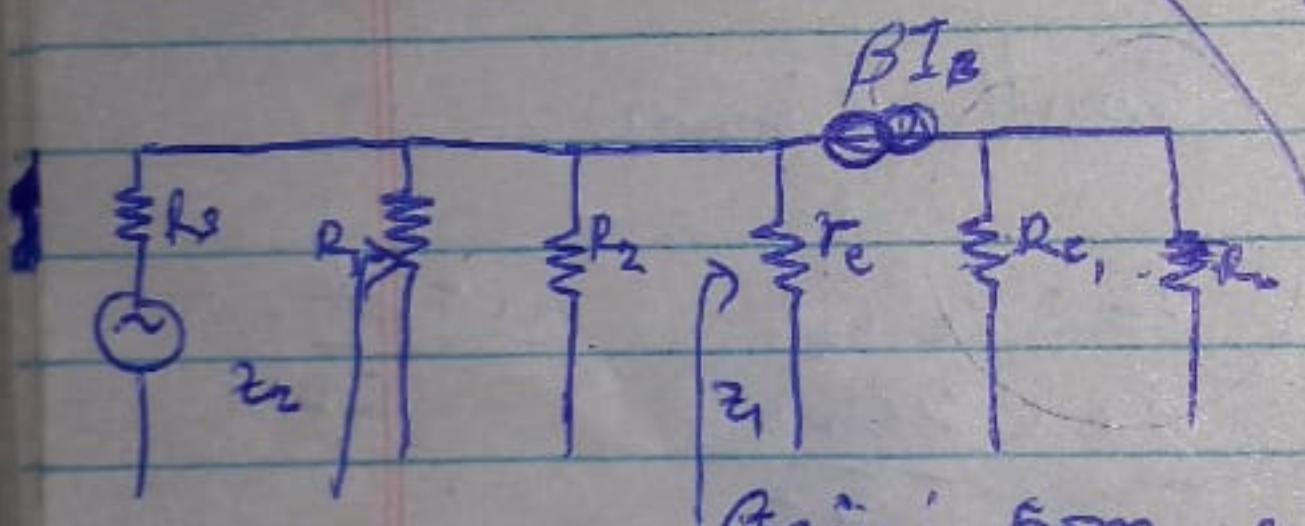
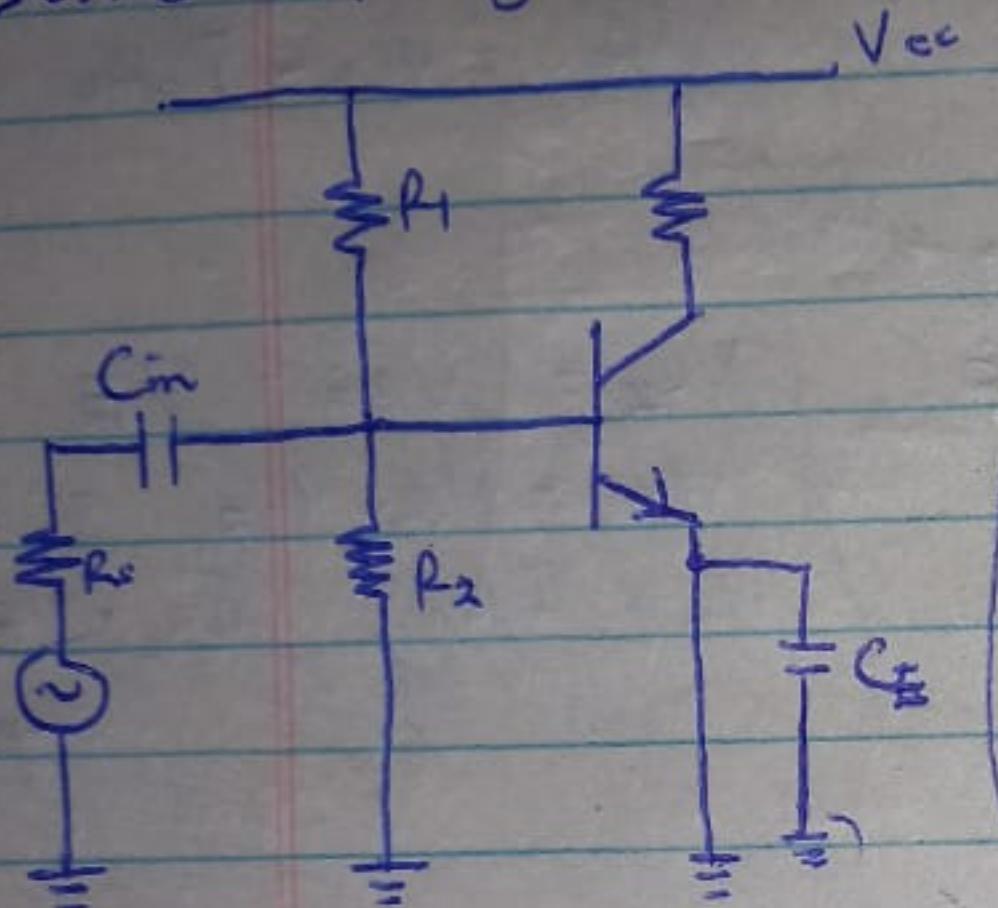
$$r_e$$

$$\Rightarrow 1.83k$$

$$10.7$$

voltage gain
input impedance

replace every dc voltage source with ground.



$$\text{Gain} : \frac{V_i}{V_s} = \frac{R_l'}{z_2}$$

$$R_l' = R_l / (1 + \beta)$$

z_2 = input impedance of the entire circuit

$$z_2 = B r_e$$

$$z_2 = R_1 \parallel R_2 \parallel B r_e$$



$$V_i = \frac{z_2}{R_s + z_2} \times V_s$$

$A_{VS} = \text{small signal gain}$

$\rightarrow A_V = \text{gain of the transistor}$

$$\frac{V_i}{V_s} = \frac{z_2}{R_s + z_2}$$

$$A_{VS} \rightarrow V_2 \cdot \frac{V_i}{V_s}$$

$$A_{VS} = \left(\frac{z_3}{R_s + z_2} \right) A_V$$

The C_E (emitter bypass capacitor) holds the emitter constant such that when the base voltage varies, the emitter voltage is held constant.

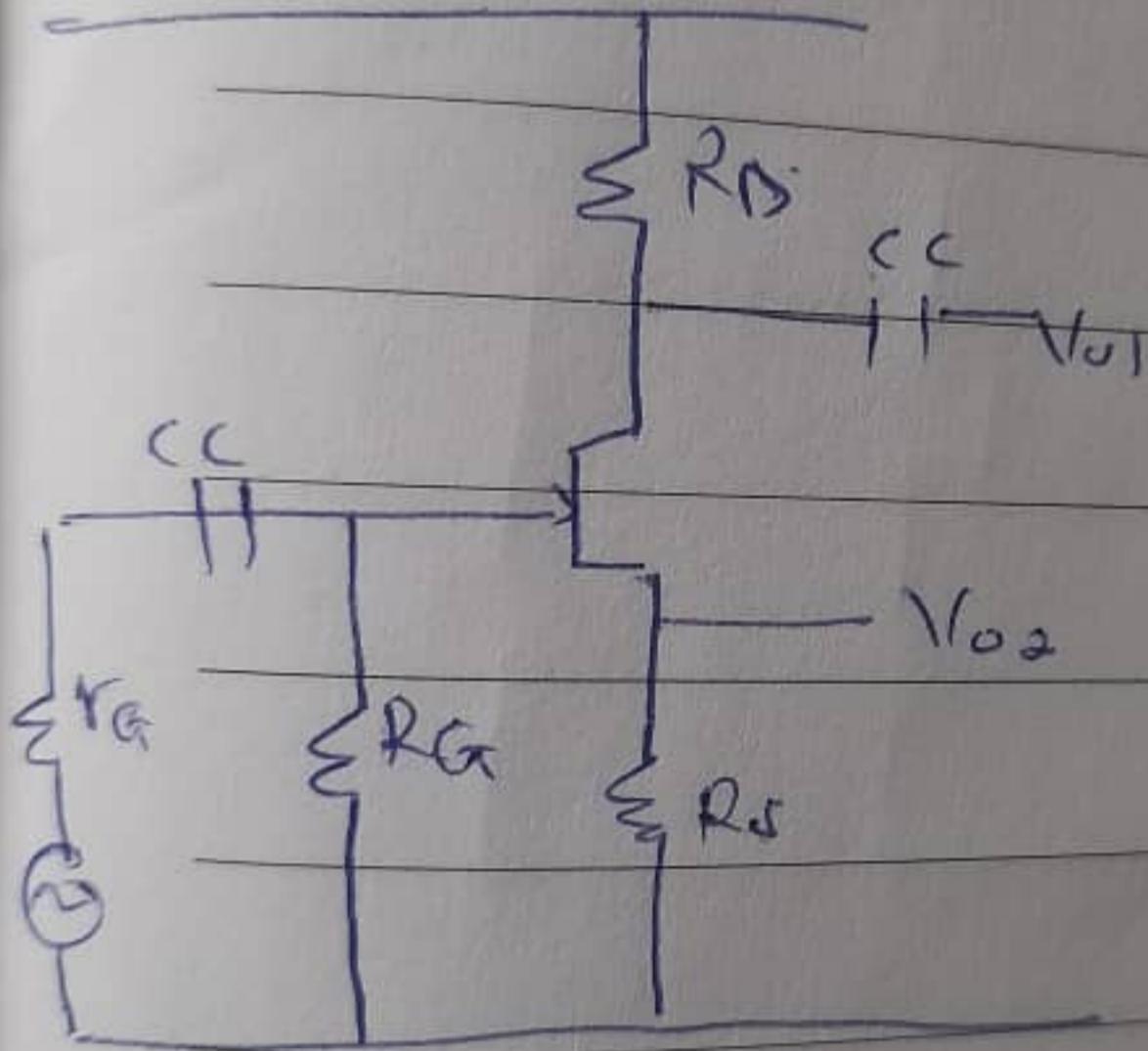
For small signal analysis, only a small portion of the DC load line is used.

The Common-Emitter amplifier is the only transistor amplifier config that produces a 180° phase shift from V_{in} and V_{out} .

(2)

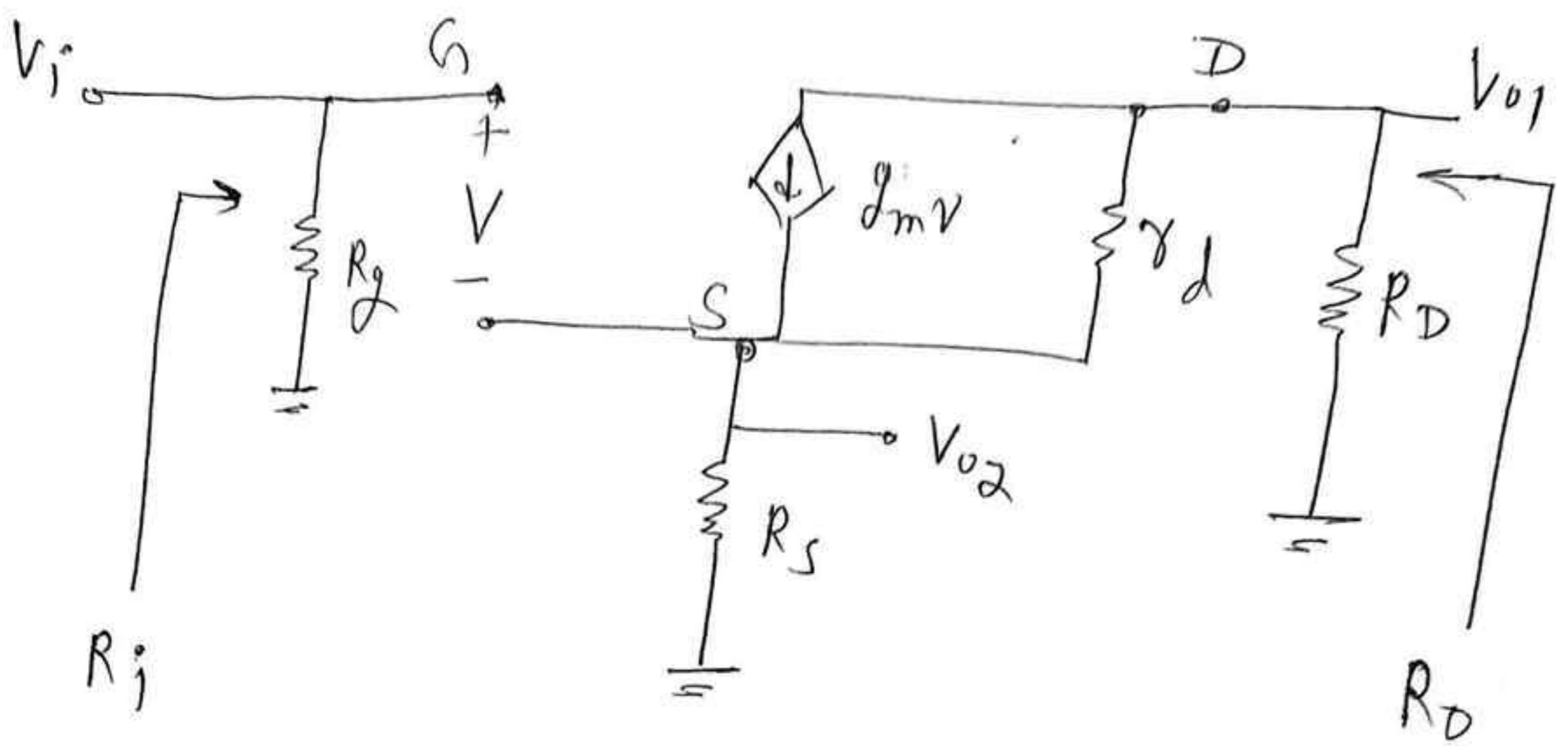
Assignment .

Consider the circuit below



Find an expression for
 $V_{o1} + V_{o2}$.

OPERATIONAL AMPLIFIERS.



at node - S

$$\frac{V_{o2}}{R_s} + \frac{V_{o2} - V_{o1}}{r_d} = I_m V$$

$$V_j = V + V_{o2} \Rightarrow V = V_j - V_{o2}$$

$$\frac{V_{o2}}{R_s} + \frac{V_{o2} - V_{o1}}{r_d} = I_m (V_j - V_{o2})$$

$$V_{o2} \left(\frac{1}{R_s} + \frac{1}{r_d} + I_m \right) = I_m V_j + \frac{V_{o1}}{r_d} \quad (1)$$

at node - D

$$\frac{V_{o1}}{R_D} + \frac{V_{o1} - V_{o2}}{r_d} + I_m V = 0$$

$$Z_0 = \text{output impedance} = (r_d + R_S) \| R_D$$

$$Z_0 = 25115 = 4.167 \text{ k}\Omega$$

$$M = g_m r_d = 2 \times 20 = 40$$

$$V_{O1} = \frac{-40 \times 5000 \times V_i}{5000 + 2000 + 5000 \times 40} = -0.8696 V_i$$

$$V_{O1} = -0.8696 V_m \sin \omega t$$

$$R_S = R_D$$

$$V_{O1} = -V_{O2}$$

$$V_{O2} = 0.8696 V_m \sin \omega t$$

$$V_{o1} = \frac{-\mu R_D V_i}{R_D + r_d + (\mu+1)R_S}$$

$$V_{o2} = \frac{V_{o1} (R_D + r_d) + \mu R_D V_i}{R_D (\mu+1)}$$

$$= - \frac{\mu R_D V_i (R_D + r_d)}{R_D + r_d + (\mu+1)R_S} + \frac{\mu R_D V_i}{R_D (\mu+1)}$$

$$V_{o2} = \frac{\mu R_S V_i}{R_D + r_d + (\mu+1)R_S}$$

$R_i = R_g$ = Input impedance

$$R_i = 1M\Omega$$

$$V_{o1} \left(\frac{1}{R_D} + \frac{1}{r_d} \right) + g_m v_i = V_{o2} \left(g_m + \frac{1}{r_d} \right) - 2$$

From - (2) $V_{o2} = \frac{V_{o1}(R_D + r_d) + g_m R_D r_d v_i}{(g_m r_d + 1) R_D}$

$$M = g_m r_d$$

$$V_{o2} = \frac{V_{o1}(R_D + r_d) + M R_D v_i}{(M+1) R_D}$$

~~input~~ in put eqn (1)

$$\left(\frac{R_s + r_d + g_m R_s r_d}{R_s r_d} \right) \frac{(V_{o1}(R_D + r_d) + M R_D v_i)}{(M+1) R_D} = g_m v_i + \frac{V_{o1}}{r_d}$$

$$V_{o1} = - \frac{g_m r_d R_D v_i}{R_D + r_d + (g_m r_d + 1) R_s}$$

Question 2 (20 Marks)

MDK

The two-stage amplifier shown in Fig. 2 is designed with a *FET*, TR1 and silicon *BJT*, Q1 with the manufacturer's specifications for β (Q1) at 25°C as 150 and g_m (TR1) as $3500\mu\text{S}$. Given $R_g=1.5\text{k}\Omega$, $R_1=6\text{ M}\Omega$, $R_2=4\text{M}\Omega$, $R_d=2.4\text{k}\Omega$, $R_s=500\Omega$, $R_3=15\text{k}\Omega$, $R_4=4.7\text{k}\Omega$, $R_c=2.7\text{k}\Omega$, $R_e=470\Omega$, $R_L=2.2\text{k}\Omega$ and supply voltage as 20V. Using the Fig.2 and component values given, answer the following questions.

Calculate:

- i) Draw the small signal equivalent circuit using the model treated in class
- ii) Emitter current I_E
- iii) Emitter resistance r_e
- iv) Voltage gain at stage 2 (BJT), A_{v2}
- v) Calculate input impedance of the second stage BJT, Z_2
- vi) Calculate the gain of the first stage (FET), A_{v1}
- vii) Calculate the input impedance of the first stage Z_1
- viii) Calculate the overall gain with signal, A_{vs}
- ix) If V_s is a sinusoidal voltage of $5\text{mV}\cos\omega t$, what will the output voltage be?
- x) On the same graph plot the input and output voltage against ωt .

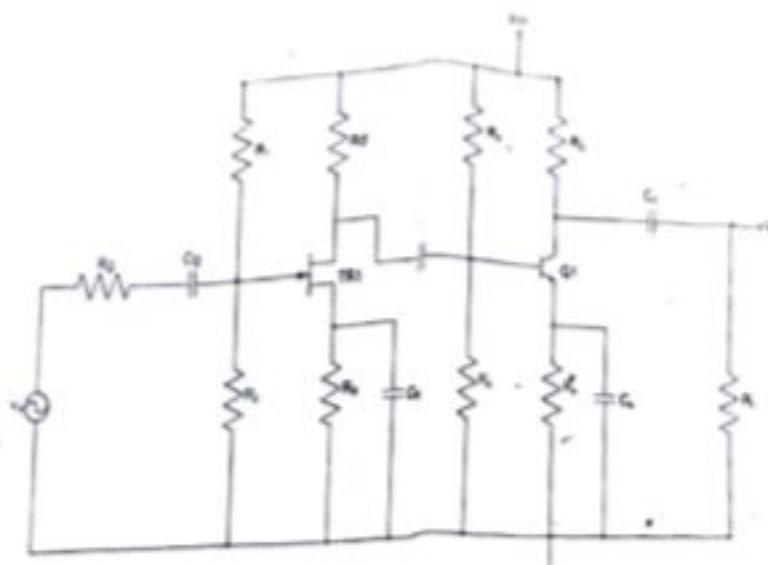
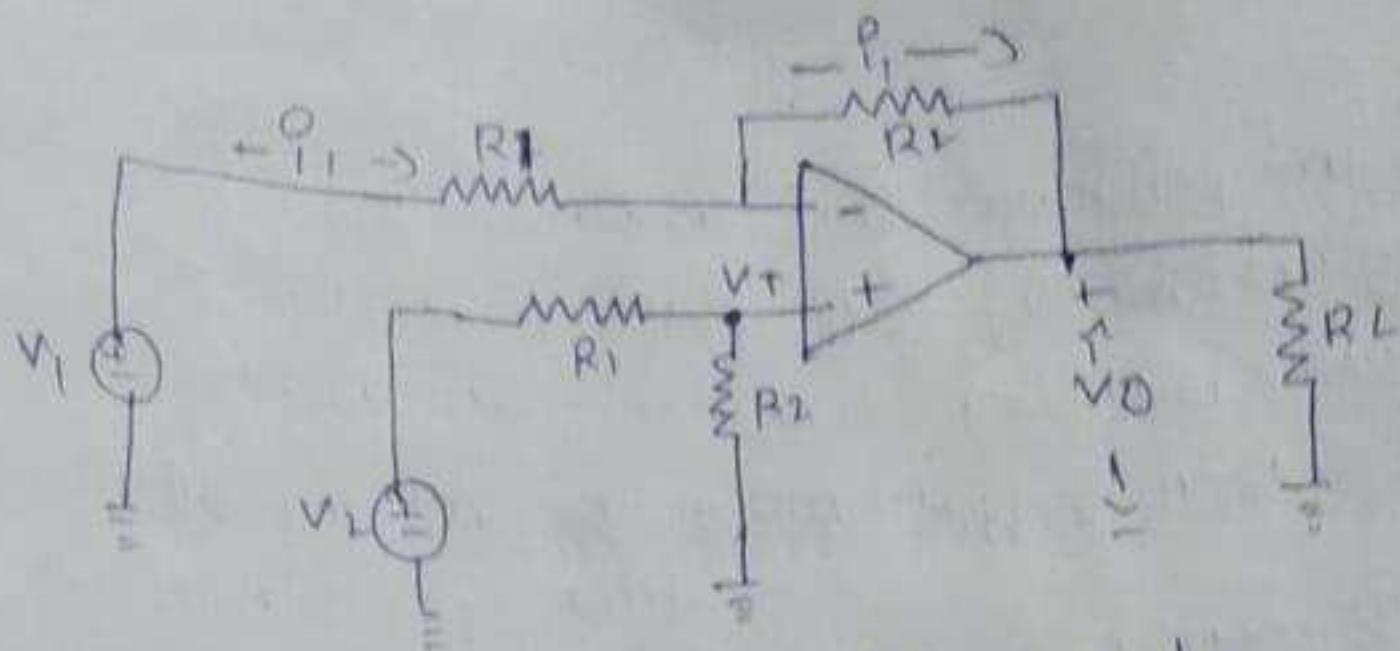


Fig. 2

MDK

D)



According to Voltage divider rule

$$V^t = \frac{R_2}{R_1 + R_2} \times V_2$$

Output voltage due to V_2 is

$$\begin{aligned} V_{\text{out}} &= \left[1 + \frac{R_L}{R_1} \right] V^t \\ &= \left[1 + \frac{R_L}{R_1} \right] \times \frac{R_2}{R_1 + R_2} \times V_2 \\ &= \frac{R_2}{R_1} \times V_2 \end{aligned}$$

Vout due to V_1 and V_2 is

$$V_{\text{out}} = \left(-\frac{R_2}{R_1} \right) V_1 + \left(\frac{R_L}{R_1} \right) V_2$$

$$V_{\text{out}} = \frac{R_2}{R_1} (V_2 - V_1)$$

Given $V_1 = 1.5V$, $V_2 = 3.0V$, $R_1 = 1k\Omega$, $R_2 = 2k\Omega$

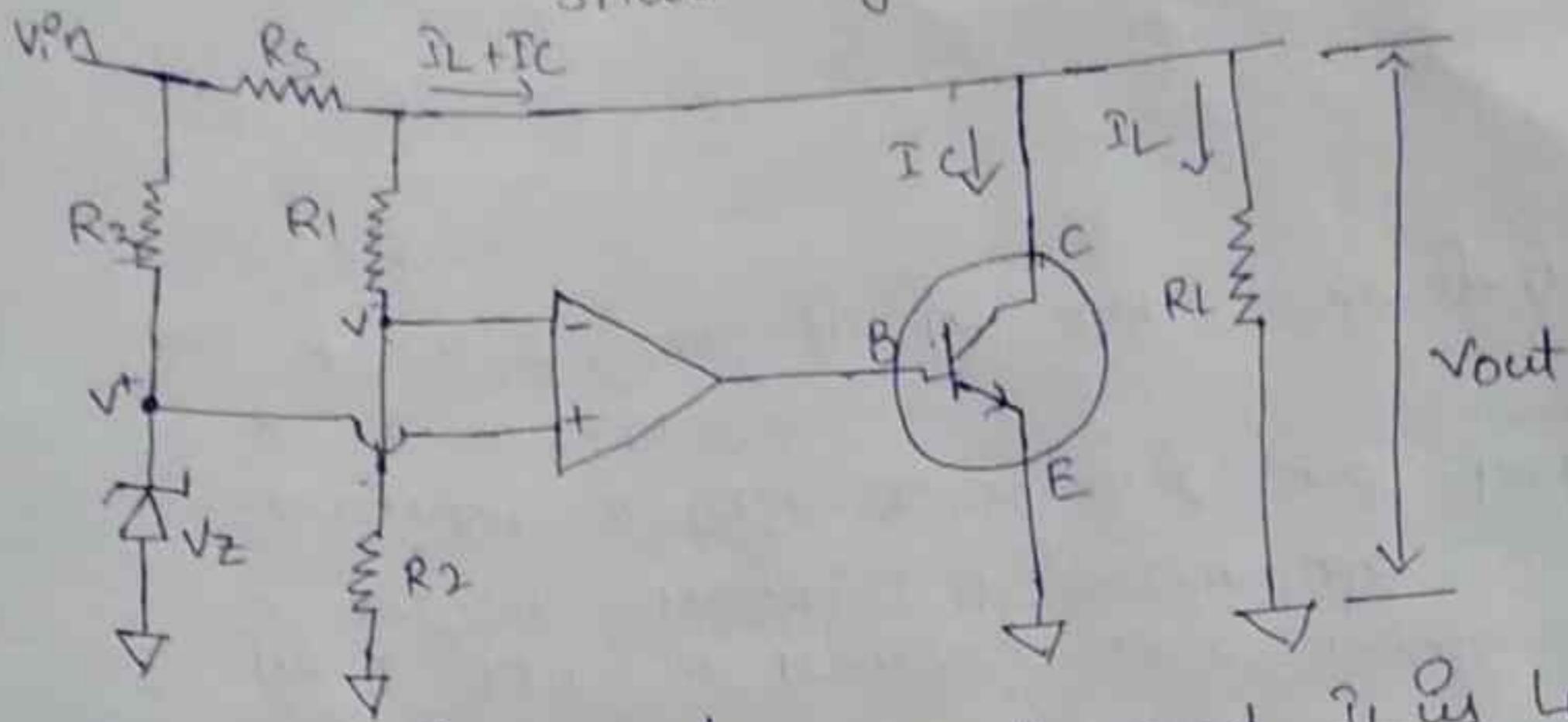
$$\begin{aligned} V_{\text{out}} &= \frac{R_2}{R_1} (V_2 - V_1) \\ &= \frac{2k\Omega}{1k\Omega} (3 - 1.5) \\ &= 2k(1.5) \\ &= 1.5 \times 10^3 \\ &= 15 \times 10^2 V. \end{aligned}$$

Characteristics of Ideal OP-amp

- 1) Ideal OP-amp has infinite input impedance
It is about 2 Mohm.
- 2) Low output impedance for ideal op-amp.
It is about 200 ohm.
- 3) Ideal OP-amp has very large voltage gain at low frequency. Thus, small changes in voltages can be amplified by using an OP-amp.
- 4) Ideal OP-amp has infinite bandwidth.
- 5) Ideal OP-amp has infinite common-mode rejection ratio.
- 6) Ideal OP-amp has Power Supply rejection ratio as infinite. It has infinite Power Supply rejection ratio.

B)

Shunt voltage Regulator (OR)
shunt Regulator



Here I_C is collector current and I_L is Load current.
OP-amp operates in negative feedback mode.
Due to the negative feedback, v^+ and v^-
are equal.

$$v^- = v^+ = v_Z = \frac{R_2}{R_1 + R_2} \times V_{out}$$

$$V_{out} = V_Z \times \left[1 + \frac{R_1}{R_2} \right]$$

V_Z = Reference voltage

In this circuit, by selecting the values of V_Z , R_1 and R_2 , we can decide the regulated output voltage.

c)

output voltage given by

$$V_0 = 9V_1 - 10V_2 = -110$$

$$V_1 = 10 \text{ mV}$$

$$V_2 = 20 \text{ mV}$$

$$\begin{aligned} \text{common mode input voltage} &= \frac{V_1 + V_2}{2} \\ &= \frac{10 + 20}{2} = \frac{30}{2} \\ V_C &= 15 \text{ mV} \end{aligned}$$

$$\begin{aligned} \text{common mode gain (A}_C\text{)} &= \frac{V_0}{V_C} \\ &= \frac{-110}{15} \\ A_C &= -7.333 \text{ mV} \end{aligned}$$

$$\text{Differential gain (A}_d\text{)} = \frac{V_0}{V_1 - V_2}$$

$$V_1 - V_2 = 10 - 20 = -10 \text{ mV}$$

$$\begin{aligned} A_d &= \frac{V_0}{V_1 - V_2} \\ &= \frac{-110}{-10} \\ A_d &= 11 \text{ mV} \end{aligned}$$

(iv) input impedance of 2nd stage:-

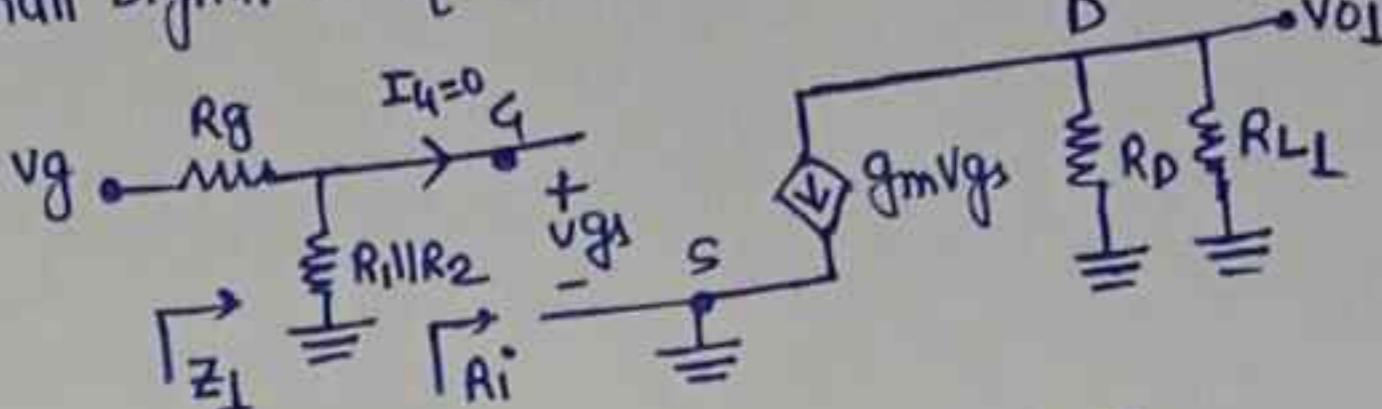
$$Z_2 = (R_g \parallel R_4) \parallel g_{m1} = [R_{th} \parallel g_{m1}] = [3.57 \parallel 0.476] = \frac{3.57 \times 0.476}{3.57 + 0.476}$$

$$Z_2 = 0.42 \text{ k}\Omega$$

(v) gain of the 1st stage: draw small signal AC equivalent circuit for TR1

$\therefore R_{L1}$ = Load Resistance for TR1

$$R_{LL} = Z_2 = 0.42 \text{ k}\Omega$$



small signal model for TR1

$$\text{gain } A_{V1} = \frac{V_{O1}}{Vg} = \frac{V_{O1}}{V_{gs}} \times \frac{V_{gs}}{Vg}$$

$$A_{V1} = \frac{V_{O1}}{Vg} = \frac{-g_m V_{gs} (R_D \parallel R_{L1})}{V_{gs}} \times \frac{(R_1 \parallel R_2)}{(R_1 \parallel R_2) + R_g}$$

$$A_{V1} = \frac{V_{O1}}{Vg} = -g_m (R_1 \parallel R_{L1}) \times \frac{(R_1 \parallel R_2)}{(R_1 \parallel R_2) + R_g} \frac{V}{V}$$

$$A_{V1} = \frac{V_{O1}}{Vg} = -3.5 (2.4 \parallel 0.42) \times \frac{(6000 \parallel 4000)}{(6000 \parallel 4000) + 1.5} \frac{V}{V}$$

$$A_{V1} = \frac{V_{O1}}{Vg} = -1.25028 \frac{V}{V}$$

$$\therefore R_i = \frac{V_{gs}}{I_d} = \frac{V_{gs}}{0} = \infty$$

$$R_1 = 6 \text{ m}\Omega = 6000 \text{ k}\Omega$$

$$R_2 = 4 \text{ m}\Omega = 4000 \text{ k}\Omega$$

(vi) input impedance of the 1st stage:-

$$Z_1 = (R_1 \parallel R_2) \parallel R_i = (R_1 \parallel R_2) \parallel \infty = [R_1 \parallel R_2]$$

$$Z_1 = 2.4 \text{ m}\Omega (\text{or}) 2400 \text{ k}\Omega$$

$$= [6 \text{ m}\Omega \parallel 4 \text{ m}\Omega] = \frac{6 \times 4}{6+4} \text{ m}\Omega$$

$$\text{overall voltage gain } A = \frac{V_o}{Vg} = A_{V1} \times A_{V2} = -1.25028 \times -381.857$$

$$A = \frac{V_o}{Vg} = 477.428 \frac{V}{V}$$

$$Vg = 5 \cos \omega t \text{ mVolts}$$

$$\therefore \frac{V_o}{Vg} = 477.428$$

$$V_o = 477.428 \times Vg = 477.428 \times 5 \cos \omega t \text{ mV}$$

$$V_o = 2387.140 \cos \omega t \text{ mV}$$

Put this value in above equation:

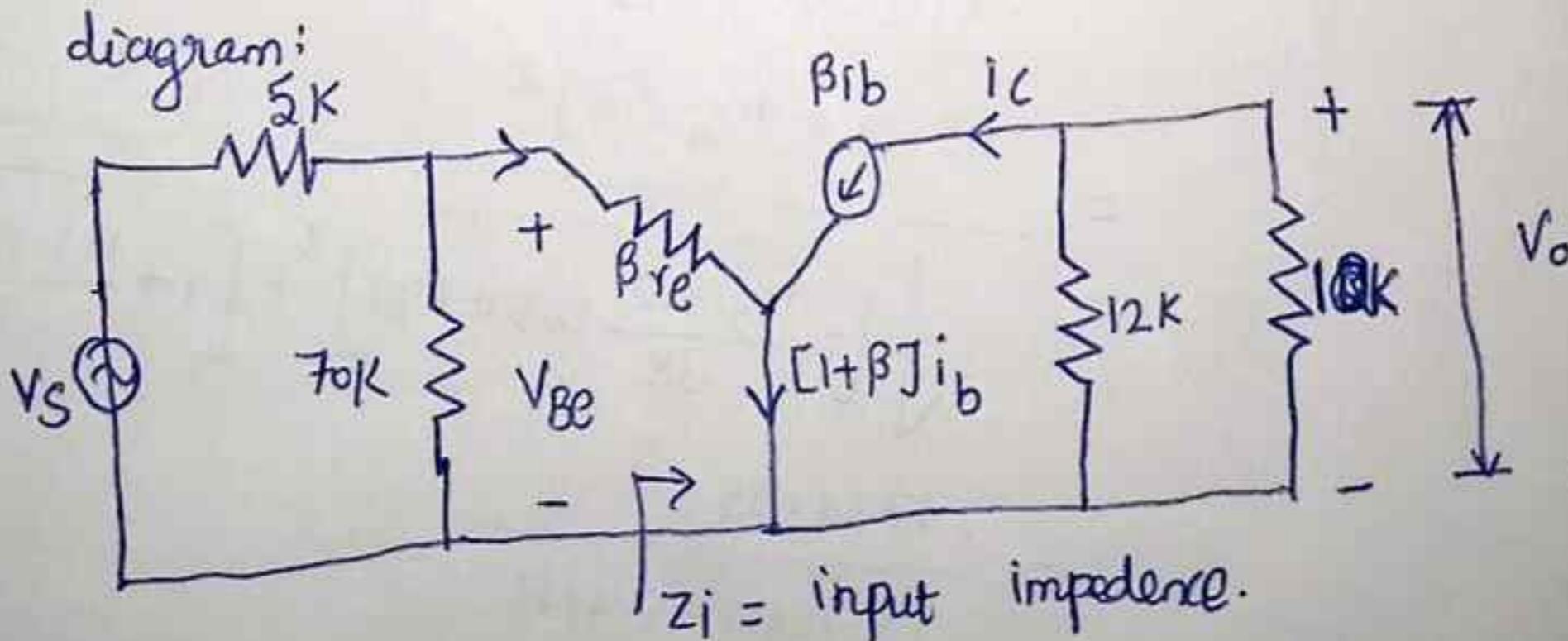
$$A_{VS} = A_V \times \frac{\sqrt{\beta e}}{V_S}$$

$$= -1.782 \times 10^3 \times 0.03$$

$$A_{VS} = -0.0534 \times 10^3.$$

a) AC Analysis: Small Signal analysis:

Circuit diagram:



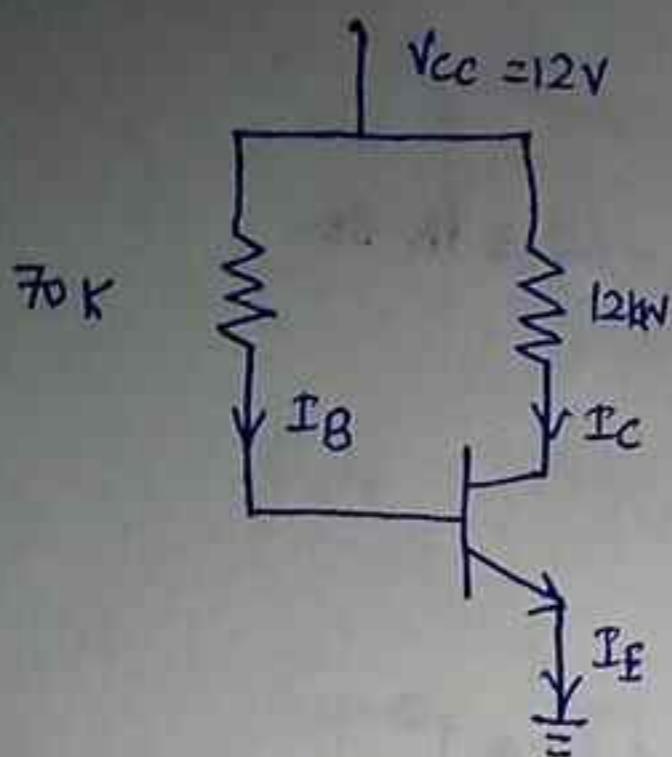
$$Z_i = \text{input impedance} = \beta r_e$$

$$Z_i = 52 [3.06] = 159.4 \Omega.$$

Solution:

Given Circuit is:

DC Analysis:



We know that

$$V_{BE} = 0.7V$$

$$-12 + 70K I_B + V_{BE} = 0$$

$$I_B = 0.16mA$$

$$I_C = \beta I_B = 50 \times 0.16mA$$

$$I_C = 8.32mA.$$

$$I_E = I_C + I_B$$

$$= 8.32 + 0.16$$

$$I_E = 8.48mA$$

$$r_e = \frac{V_T}{I_E} \quad \text{where } V_T = \text{Thermal Voltage} = 26mV.$$

$$r_e = \frac{26mV}{8.48mA} = 3.06\Omega$$

$$\text{b) } A_V = \frac{-i_C [12k \parallel 10k]}{i_b [\beta r_e]} = \frac{-\beta i_B [12k \parallel 10k]}{i_B \beta r_e} = \frac{-[12k \parallel 10k]}{r_e} = \frac{-5.45k}{3.06}$$

$$A_V = -1.782 \times 10^3.$$

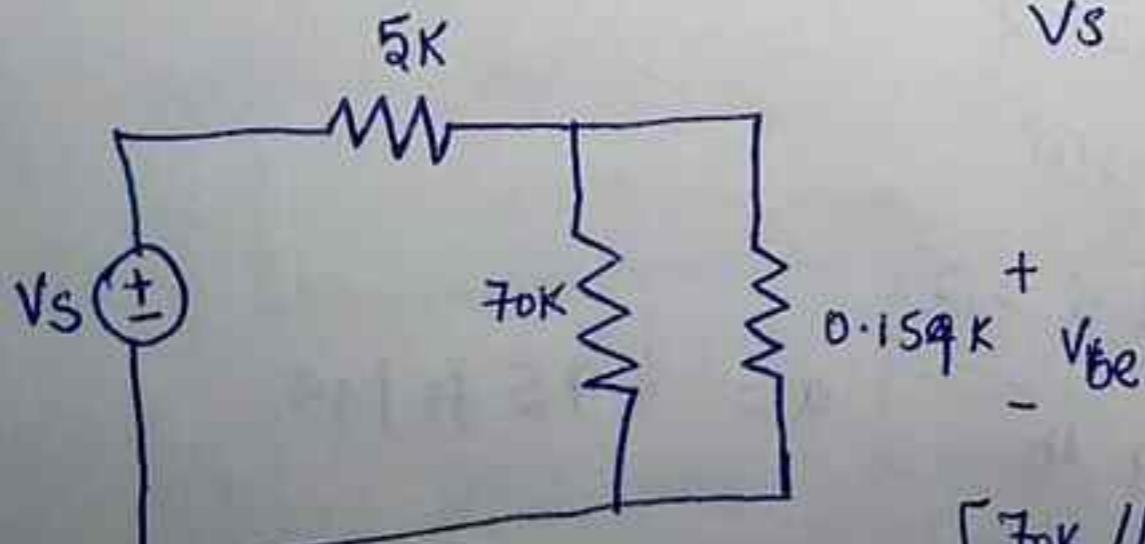
Input Impedance:

$$Z_i = \beta r_e = 50 [3.06] = 159.4\Omega$$

overall gain $[A_{VS}]$:

$$A_{VS} = \left[\frac{V_o}{V_s} \right] = \left[\frac{V_o}{V_{BE}} \right] \times \left[\frac{V_{BE}}{V_s} \right]$$

$$A_{VS} = A_V \times \frac{V_{BE}}{V_s}$$



$$V_{BE} = V_s \times \frac{[70k \parallel 0.159k] \approx 0.159k}{5k \parallel 0.159k}$$

$$\frac{V_{BE}}{V_s} = 0.03$$

Ans ② FET
 $\beta = 150$

FET FET

$$g_m = 3500 \mu S = 3500 \times 10^{-3} mS = 3.5 mS$$

(i) Dc Analysis: all capacitor are open circuit and draw dc Equivalent ckt for θ_L

$$R_{Th} = R_3 || R_4 = 15 || 4.7 = \frac{15 \times 4.7}{15 + 4.7} = 3.57 k\Omega$$

$$V_{Th} = V_{CC} \times \frac{R_4}{R_3 + R_4} = 20 \times \frac{4.7}{15 + 4.7} = 4.77 V$$

$$\text{KVL: } -V_{Th} + I_B R_{Th} + V_{BE} + R_e(1+\beta) I_B = 0$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + R_e(1+\beta)} = \frac{4.77 - 0.7}{3.57 + 470(1+150)}$$

$$I_B = 0.05460 \text{ mA}$$

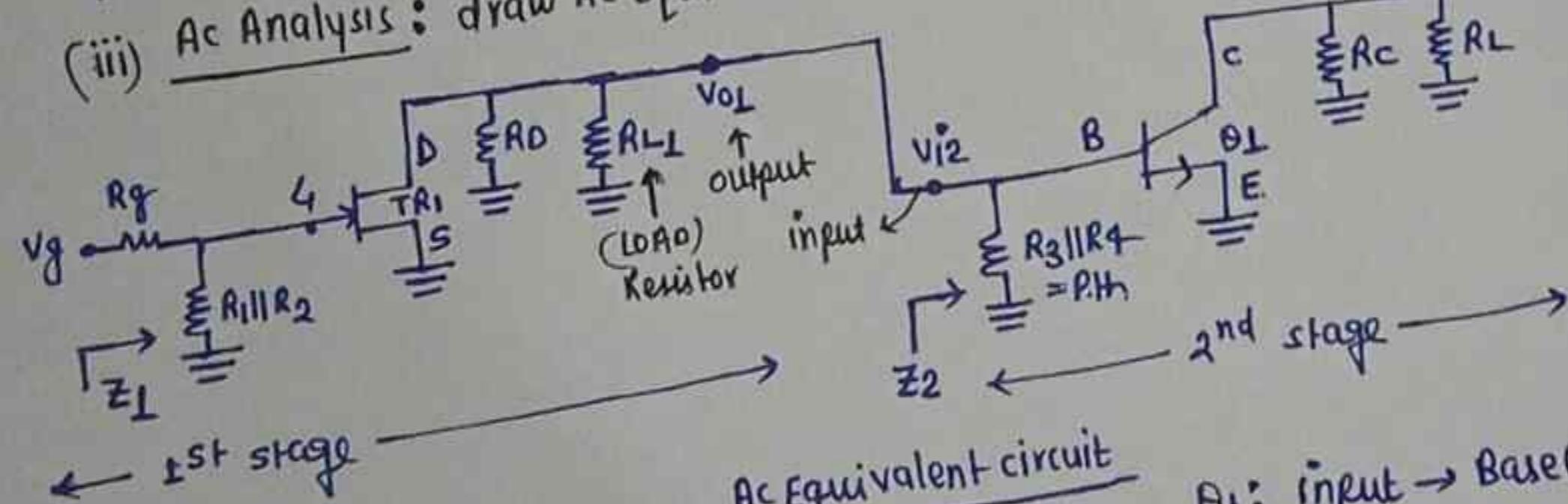
$$I_C = \beta I_B = 150 \times 0.05460 \text{ mA} = 8.190 \text{ mA}$$

$$\text{Emitter Current } I_E = I_B + I_C = 0.05460 \text{ mA} + 8.190 \text{ mA} = 8.244 \text{ mA}$$

$$I_E = 8.244 \text{ mA}$$

$$(ii) \text{ Ac Emitter Resistance } R_e = \frac{V_T}{I_E} = \frac{26 \text{ mV}}{8.244 \text{ mA}} = 3.153 \Omega$$

(iii) Ac Analysis: draw Ac Equivalent circuit by considering all capacitor with short circuit



TR₁: input \rightarrow Gate(4)
 output \rightarrow Drain(D) \Rightarrow common source (cs)
 grounded \rightarrow source(S)

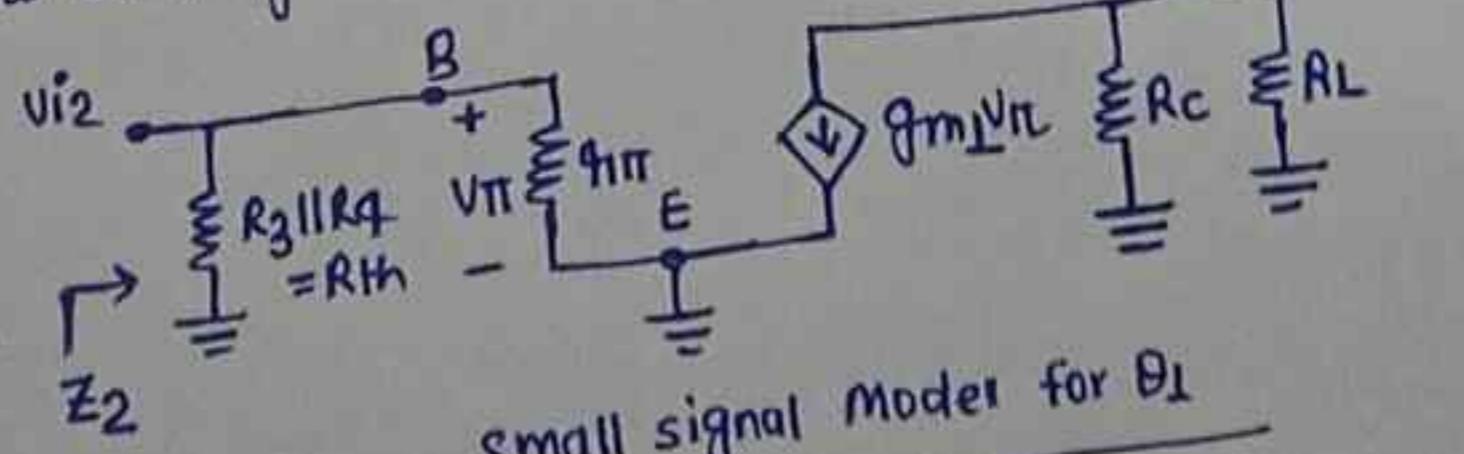
θ_L : input \rightarrow Base(B)
 output \rightarrow Collector(C) \Rightarrow Common Emitter Amp
 grounded \rightarrow Emitter(E)

$\therefore R_{L1} = Z_2$ due to loading effect when two Amps are in cascaded connection

Voltage gain at stage ① : draw small signal Ac Equivalent ckt using π Model

$$\therefore g_{m1} = \frac{I_C}{V_T} = \frac{8.190 \text{ mA}}{26 \text{ mV}} = 315 \text{ mS}$$

$$h_{IT} = \frac{\beta}{g_{m1}} = \frac{150}{315 \text{ mS}} = 0.476 \text{ k}\Omega$$



small signal model for θ_L

$$\text{Voltage gain } AV_1 = \frac{V_O}{V_{I2}}$$

$$AV_1 = \frac{V_O}{V_{I2}} = \frac{-g_{m1} V_{T1} (R_c || R_L)}{V_T} = -g_{m1} (R_c || R_L) = -315 (2.7 || 2.2) = -315 \times \frac{2.7 \times 2.2}{2.7 + 2.2}$$

$$AV_1 = \frac{V_O}{V_{I2}} = -381.857 \frac{V}{V}$$

(-) sign due to common Emitter Amp of 180° phase shift b/w V_O and V_{I2}

Step 2

Oxidation

Atoms of oxygen transform silicon layers on top of the wafer to silicon dioxide in the oxidation cycle.

Particle Implantation

Particle Implantation is the most common method for introducing dopant pollution into semiconductors. An electrical field accelerates the ionized particles, which are then focused on the semiconductor wafer.

Diffusion

To strengthen barrage incited cross-section absconds, a dispersion stage is used after particle implantation.

Step 1

a)

There are multiple stages in planar process technology as applied to IC fabrication

Lithography

Lithography is the process of putting a thin, homogeneous coating of thick fluid (photograph oppose) to the wafer surface in order to define the pattern. Heating solidifies the picture opposition, which is then selectively erased by projecting light via a reticle holding veil data.

Etching

The process of removing unwanted material from the wafer's surface. Methods for cutting specialists are used to shift the photograph contrary to the wafer.

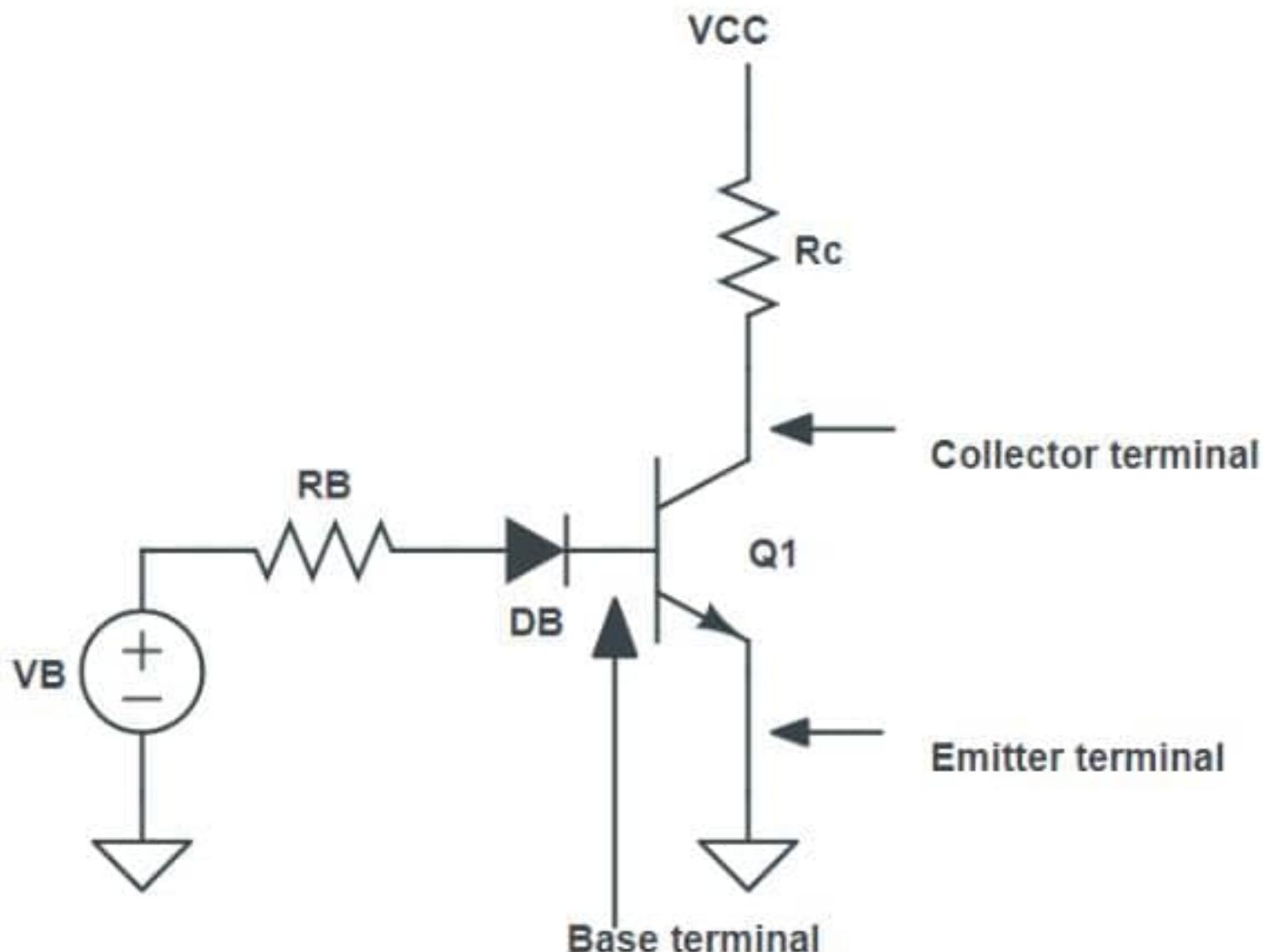
Films of various materials are deposited on the wafer during the deposition process.

Synthetic Mechanical Cleaning is a planarization process that involves applying a compound slurry to the wafer surface with etchant experts.

Step 3

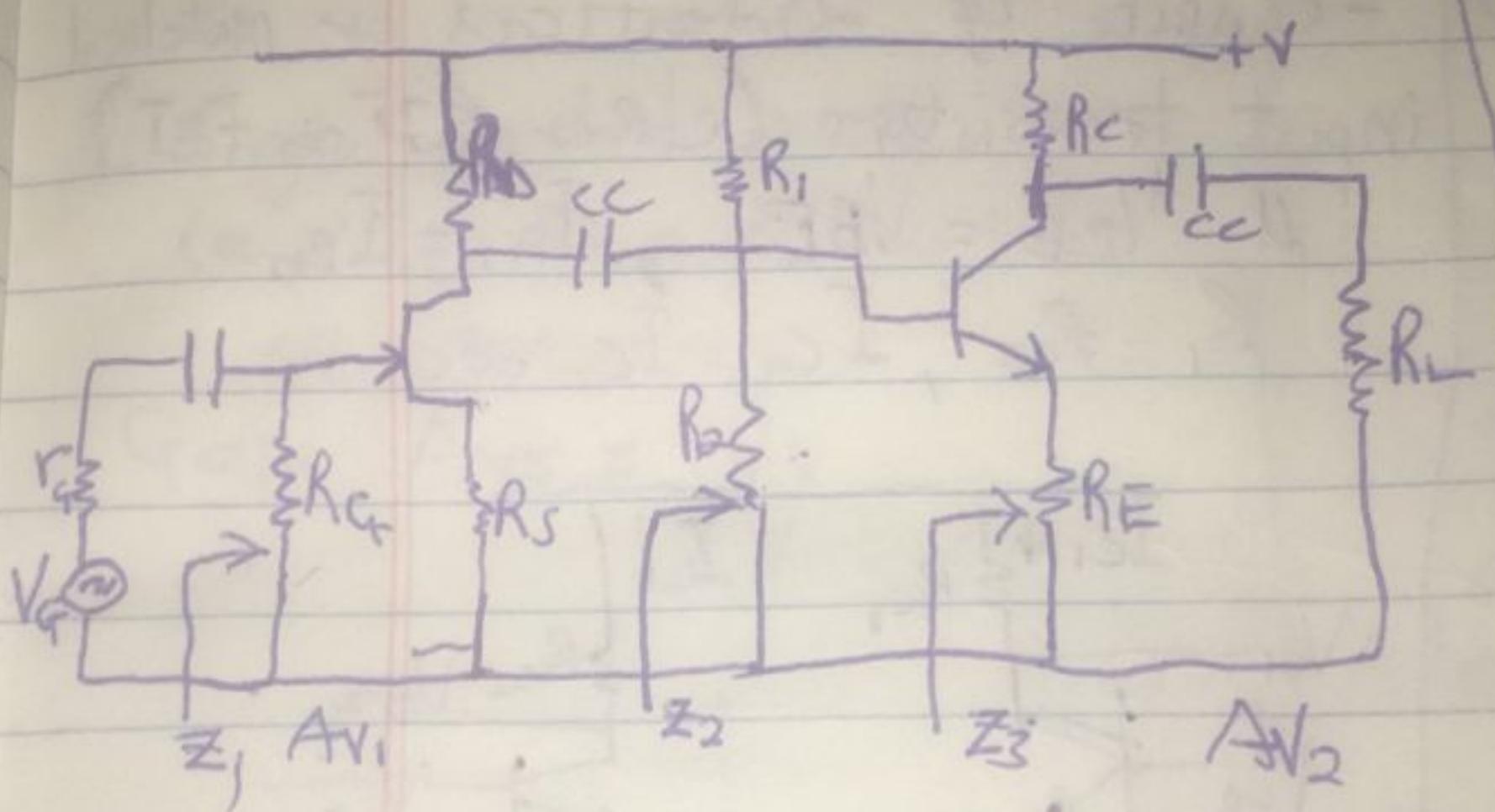
b)

Circuit diagram with masking layout

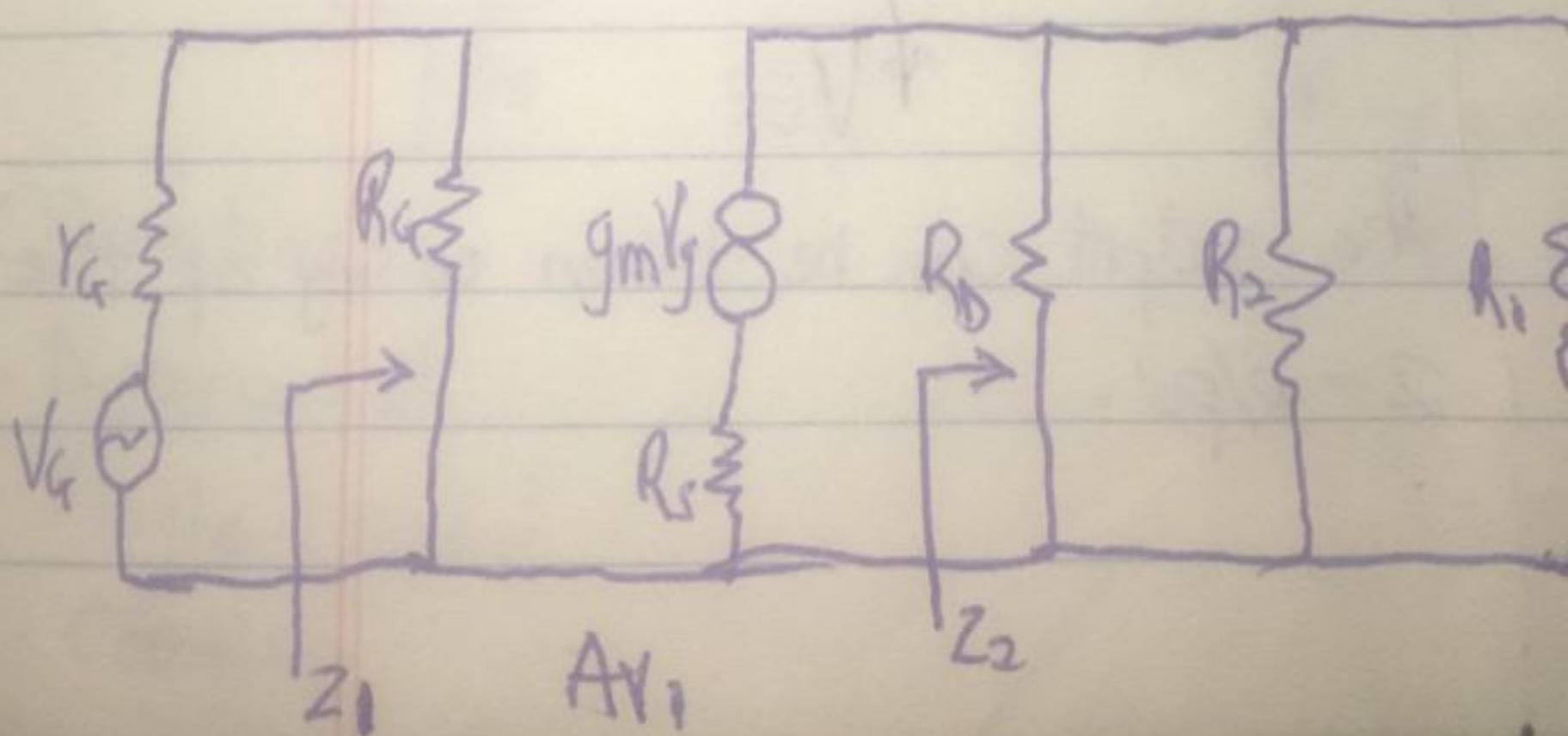


$$A_{VS} = \left(\frac{Z_2}{R_S + Z_2} \right) \cdot A_V$$

Consider the cct of fig x.1

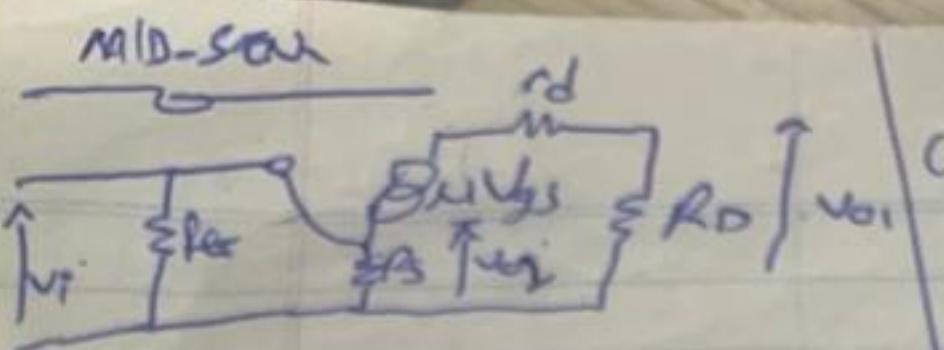


1. Draw small signal Equivalent Circuit
2. Find A_{V1} , A_{V2} , Z_1 , Z_2 , Z_3 , A_{VG} .



Question 3

- a) State and explain the different types of power amplifiers ~~A, B, C, D~~.
- b) A complementary pair class B push-pull amplifier has a supply voltage of 45 V and the transistors are biased so that they are sinusoidally driven to provide a current which is 0.75 of the maximum value. Calculate:
- (i) The output power supplied to a speaker having a resistance of $15\ \Omega$
 - (ii) The collector efficiency
 - (iii) The power dissipation of the transistors.



$$V_i = V_{GS} + I_D R_S$$

$$V_{GS} = V_i - I_D R_S$$

$$V_{GS} = V_i - I_D R_S$$

$$I_D = \frac{N V_{GS}}{R_D + R_S + r_d}$$

$$I_D = \frac{N (V_i - I_D R_S)}{R_D + R_S + r_d}$$

$$I_D (R_D + R_S + r_d) = N V_i - N I_D R_S$$

$$I_D (R_D + R_S + r_d) + N I_D R_S = N V_i$$

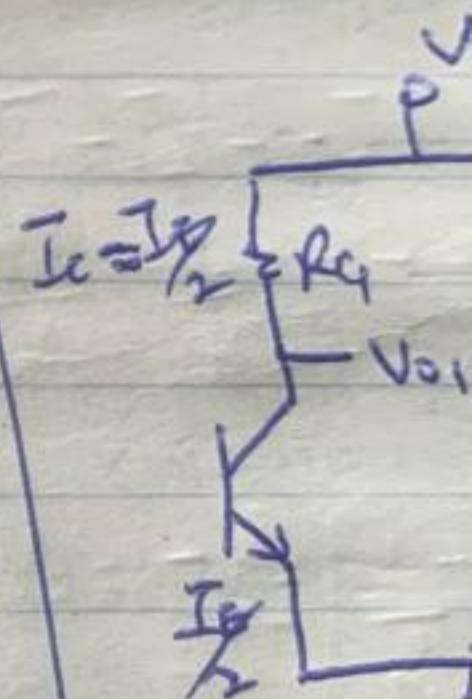
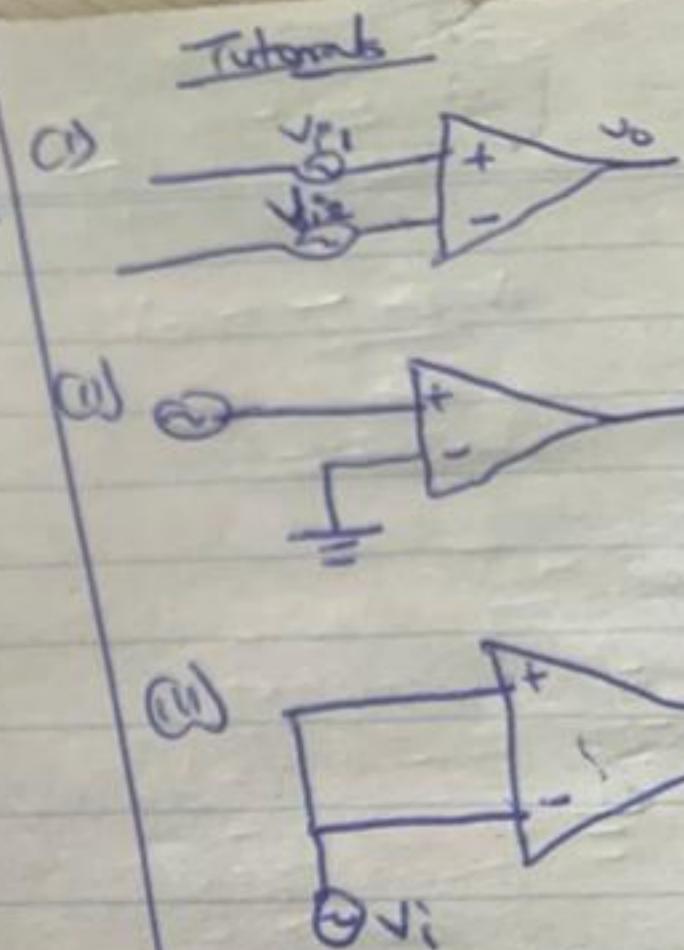
$$I_D (R_D + R_S + r_d + N R_S) = N V_i$$

$$I_D = \frac{N V_i}{R_D + R_S + r_d + N R_S}$$

$$I_D = \frac{N V_i}{R_D + r_d + (1/f) N R_S}$$

$$V_{O1} = -I_D R_D$$

$$V_{O2} = I_D R_D$$



$$I_{B1} = I_{B2}$$

$$B_1 = B_2$$

Assum

R

Question 2

MDK

The two-stage amplifier shown in Fig. 2 is designed with a *FET*, TR1 and silicon *BJT*, Q1 with the manufacturer's specifications for β (Q1) at 25°C as 150 and g_m (TR1) as $3500\mu\text{S}$. Given $R_g = 1.5\text{k}\Omega$, $R_1 = 6\text{ M}\Omega$, $R_2 = 4\text{M}\Omega$, $R_d = 2.4\text{k}\Omega$, $R_s = 500\Omega$, $R_3 = 15\text{k}\Omega$, $R_4 = 4.7\text{k}\Omega$, $R_c = 2.7\text{k}\Omega$, $R_e = 470\Omega$, $R_L = 2.2\text{k}\Omega$ and supply voltage as 20V. Using the Fig. 2 and component values given, answer the following questions.
Calculate:

- i) Emitter current I_E
- ii) Emitter resistance r_e
- iii) Voltage gain at stage 2, A_{V2}
- iv) Calculate input impedance of the second stage, Z_2
- v) Calculate the gain of the first stage, A_{V1}
- vi) Calculate the input impedance of the first stage Z_1
- vii) Calculate the overall gain, A
- viii) If v_g is a sinusoidal voltage of $5\text{mVcos}\omega t$, what will the output voltage be?

← Answer 1 of 1



Ans ② For BJT

For FET

$\beta = 150$

$$R_{in} = 350 \Omega \text{ k} \Omega = 350 \times 10^3 \Omega = 2.6 \text{ M}\Omega$$

(i) DC Analysis: all capacitors are open circuit and draw dc equivalent CKE for B_2

$$R_{in} = R_3 || R_4 = 15 || 4.7 = \frac{15 \times 4.7}{15 + 4.7} = 3.57 \text{ k}\Omega$$

$$V_{TH} = V_{BE} \frac{R_4}{R_3 + R_4} = 26 \times \frac{4.7}{15 + 4.7} = 4.77 \text{ V}$$

$$\text{KVL: } -V_{TH} + I_B R_{in} + V_{BE} + R_E (I_B + I_E) = 0$$

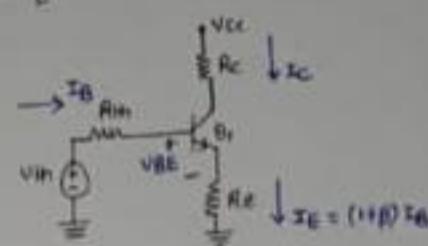
$$I_B = \frac{V_{TH} - V_{BE}}{R_{in} + R_E (1 + \beta)} = \frac{4.77 - 0.7}{3.57 + 1.47 \times 150}$$

$$I_B = 0.05460 \text{ mA}$$

$$I_C = \beta I_B = 150 \times 0.05460 \text{ mA} = 8.190 \text{ mA}$$

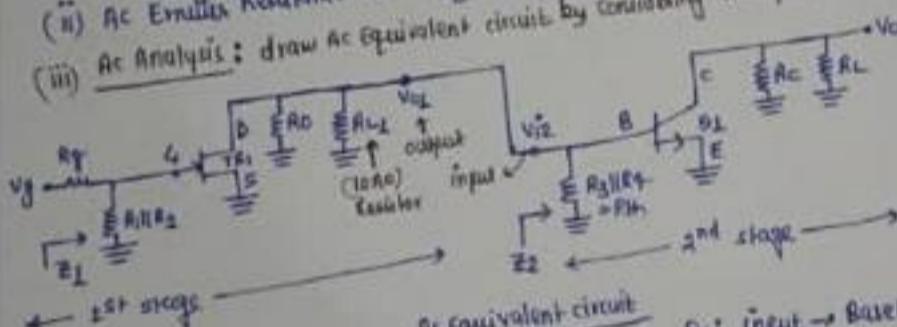
$$\text{Emitter Current } I_E = I_B + I_C = 0.05460 \text{ mA} + 8.190 \text{ mA} = 8.244 \text{ mA}$$

$$I_E = 8.244 \text{ mA}$$



(ii) AC Emitter Resistance $R_E = \frac{V_T}{I_E} = \frac{26 \text{ mV}}{8.244 \text{ mA}} = 3.153 \text{ k}\Omega$

(iii) AC Analysis: draw AC equivalent circuit by considering all capacitor with short circuit



TR1: input → Gate(4)
output → Drain(6) → common source (cs)
Grounded → Source(5)

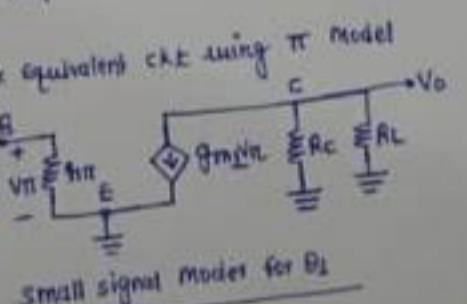
TR1: input → Base(B)
output → Collector(C) ⇒ Common Emitter Amp
Grounded → Emitter(E)

∴ $R_L = Z_2$ due to loading effect when two amp's are in cascaded connection

Voltage gain at stage ②: draw small signal AC equivalent CKE using π model

$$\therefore g_m \frac{Z_2}{V_T} = \frac{8.190 \text{ mA}}{26 \text{ mV}} = 315 \text{ mS}$$

$$r_{in} = \frac{P}{g_m} = \frac{150}{315 \text{ mS}} = 0.476 \text{ k}\Omega$$



Voltage gain A_{V2} = $\frac{V_o}{V_{d2}}$

$$A_{V2} = \frac{V_o}{V_{d2}} = -g_m \frac{V_{d2} (R_L || R_{RL})}{V_T} = -g_m (R_L || R_{RL})$$

$$A_{V2} = \frac{V_o}{V_{d2}} = -381 \cdot 857 \frac{\text{V}}{\text{V}}$$

⇒ sign due to common Emitter Amp of 180° phase shift b/w V_o and V_{d2}

(iv) Input impedance of 2nd stage :-

$$Z_2 = (R_3 || R_4) || r_{in} = [R_{in} || r_{in}] = [3.57 || 0.476] = \frac{3.57 \times 0.476}{3.57 + 0.476}$$

$$Z_2 = 0.42 \text{ k}\Omega$$

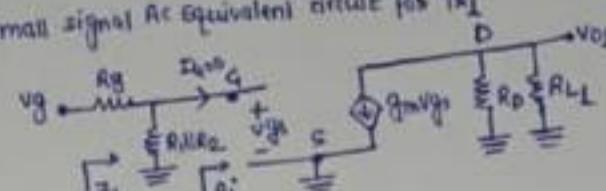
(v) Gain of the 1st stage: draw small signal AC equivalent circuit for TR1

∴ $R_{L1} = \text{Load Resistance for TR1}$

$$R_{L1} = Z_2 = 0.42 \text{ k}\Omega$$

$$\text{Gain } A_{V1} = \frac{V_{o1}}{V_g} = \frac{V_{o1}}{V_{g1}} \times \frac{V_{g1}}{V_g}$$

$$A_{V1} = \frac{V_{o1}}{V_g} = \frac{-g_m V_{g1} (R_{L1} || R_{L1})}{V_{g1}} \times \frac{(R_{L1} || R_{L1})}{(R_{L1} || R_{L1}) + R_{in}}$$



small signal model for TR1

Fig. 2.1

Question 3

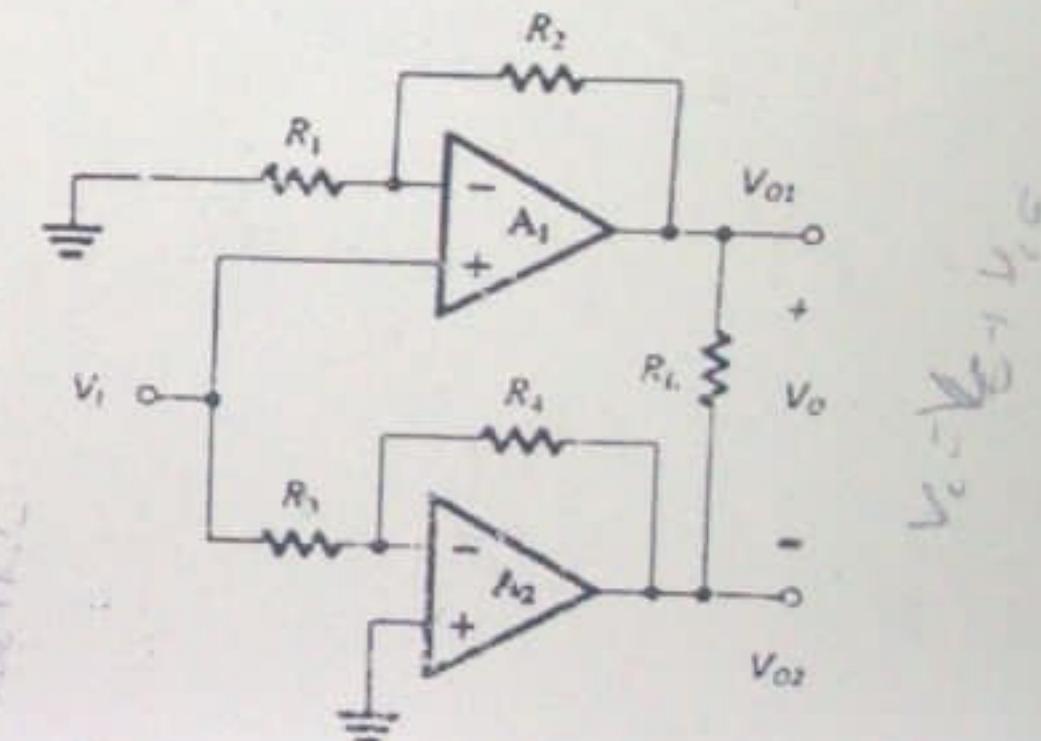
(a) State four characteristics of an ideal op-amp.

(b) Fig. 3.1 shows the schematic of the two op-amp instrumentation amplifier. Find

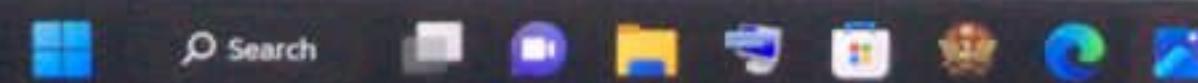
- i. ✓ An expression for V_{O1} and V_{O2} .
- ii. ✓ Hence or otherwise an expression V_0 if $R_1 = R_2 = R_3 = R_4$
- iii. ✓ The current through R_L if $R_L = 10K\Omega$ and $V_i = 5V$.

Fig. 3.1

$$\begin{aligned}R_C &= R_C / R_L \\R_C &= R_C + R_L \\V_C &= V_C / R_C + R_L \\V_C &= V_C / R_C + R_L\end{aligned}$$



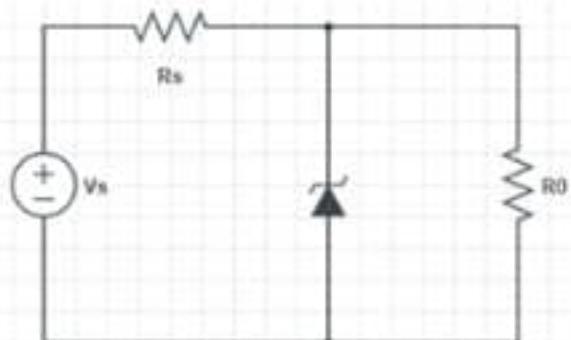
Question 4



Step 1

The shunt regulator or shunt voltage regulator is a form of voltage regulator where the regulating element shunts the current to ground. The shunt regulator operates by maintaining a constant voltage across its terminals and it takes up the surplus current to maintain the voltage across the load. One of the most common examples of the shunt regulator is the simple Zener diode circuit where the Zener diode acts as the shunt element.

The circuit of a shunt regulator can be made as follows:



Step 2

So, the four main elements of a shunt regulator are input voltage source, Source resistance, Zener diode and the output resistance. In this circuit, the series resistor drops the voltage from the source to the Zener diode and load. As the Zener diode maintains its voltage, any variations in load current do not affect the voltage across the Zener diode. It takes up the current variations required to ensure the correct drop across the series resistor. In this way it shunts sufficient current to maintain the voltage across its terminals and hence the load.

Step 3

(2):

Given:

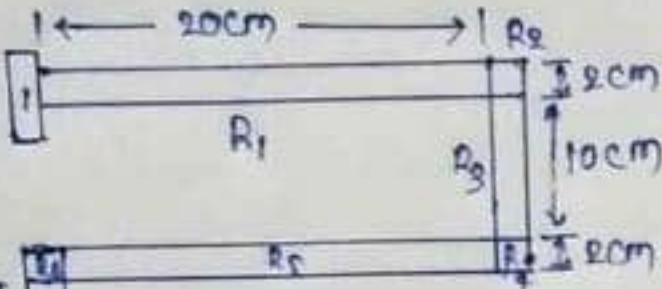
$$V_0 = 9V_1 - 10V_2$$

$$V_1 = 10mV$$

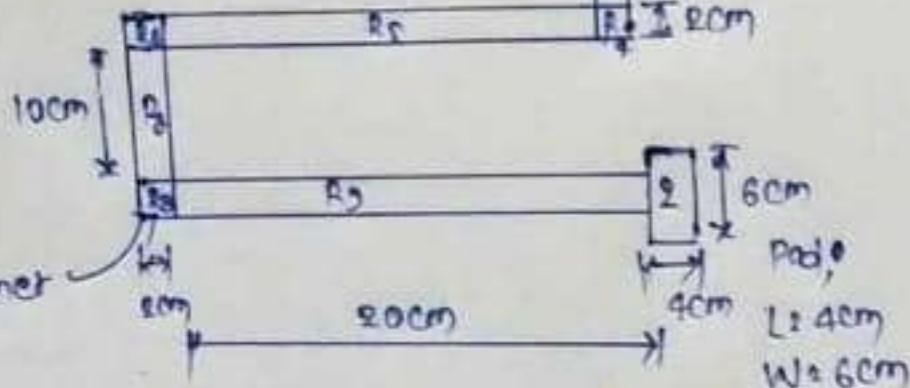
$$V_2 = 20mV$$

So, the output voltage is:

$$V_0 = 9 * 10mV - 10 * 20mV$$



Resistor length is always the parallel to current flow.



we can see that,

$$R_1 = R_5 = R_9$$

$$R_8 = R_2$$

$$\text{and } R_2 = R_4 = R_6 = R_8$$

$$R = S \left(\frac{L}{W} \right) \quad \text{where, } S = \text{sheet resistance} \Omega/\text{square},$$

L = length of the resistor

W = width of the resistor.

sheet resistance (regular) = $1200 \Omega/\text{sq}$.

dots/corners sheet resistance

$$= 120 \times 0.6 = 22 \Omega/\text{sq}$$

$$\text{Resulting resistance} = R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7 + R_8 + R_9 + 2 R_p$$

$$= 9R_1 + 4R_2 + 2R_3 + 2R_p$$

$$= 3 \times \left(1200 \times \left(\frac{20}{2} \right) \right) + 4 \left(72 \times \left(\frac{9}{2} \right) \right) + 2 \left(1200 \times \left(\frac{10}{2} \right) \right) + 2 \times \left(72 \times \left(\frac{4}{6} \right) \right)$$

$$= 3 \times 1200 + 4 \times 22 + 2 \times 600 + 2 \times 48$$

$$= 3600 + 88 + 1200 + 96$$

Hence, Value of resulting resistor = 5184 \Omega

So, the output voltage is:

$$V_o = 9 * 10mV - 10 * 20mV$$

$$V_o = 90mV - 200mV$$

$$V_o = -110mV$$

Step 4

The common mode voltage is:

$$V_{cm} = \frac{V_1 + V_2}{2}$$

$$V_{cm} = \frac{10 + 20}{2}$$

$$V_{cm} = 15mV$$

The common mode gain is:

$$A_c = \frac{V_{out}}{V_{cm}}$$

$$A_c = \frac{-110mV}{15mV}$$



MDK

UNIVERSITY OF ENERGY AND NATURAL RESOURCES, SUNYANI, GHANA

SCHOOL OF ENGINEERING

DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING

Level 300: First Semester Examinations 2020/2021

Bachelor of Science (Computer Engineering, Electrical & Electronic Engineering)

ELNG 303: LINEAR ELECTRONIC CIRCUITS

April, 2021

Time: 2½ hours

Material required: Class material (**To be brought in by students**)

INSTRUCTIONS: ANSWER ALL QUESTIONS (each question carries 15marks)

Question 1

- (a) The following processes are used in the fabrication of monolithic ICs, explain each of them in detail:
- Oxidation
 - Diffusion
 - Epitaxy
 - Photolithography
 - Thin Film Deposition
- (b) Using the list in (a) provide a step-by-step masking levels of the fabrication of NPN transistor indicating the type of photo-resist used.

Question 2

The two-stage amplifier shown in Fig. 2 is designed with a FET, TR1 and silicon BJT, Q1 with the manufacturer's specifications for β (Q1) at 25°C as 150 and g_m (TR1) as 3500 μ S. Given $R_g=1.5k\Omega$, $R_1=6M\Omega$, $R_2=4M\Omega$, $R_d=2.4k\Omega$, $R_s=500\Omega$, $R_3=15k\Omega$, $R_4=4.7k\Omega$, $R_c=2.7k\Omega$, $R_e=470\Omega$, $R_L=2.2k\Omega$ and supply voltage as 20V. Using the Fig. 2 and component values given, answer the following questions.

Calculate:

- Emitter current I_E
- Emitter resistance r_e
- Voltage gain at stage 2, A_{v2}
- Calculate input impedance of the second stage, Z_2
- Calculate the gain of the first stage, A_{v1}
- Calculate the input impedance of the first stage Z_1
- Calculate the overall gain, A
- If v_g is a sinusoidal voltage of $5mV \cos \omega t$, what will the output voltage be?

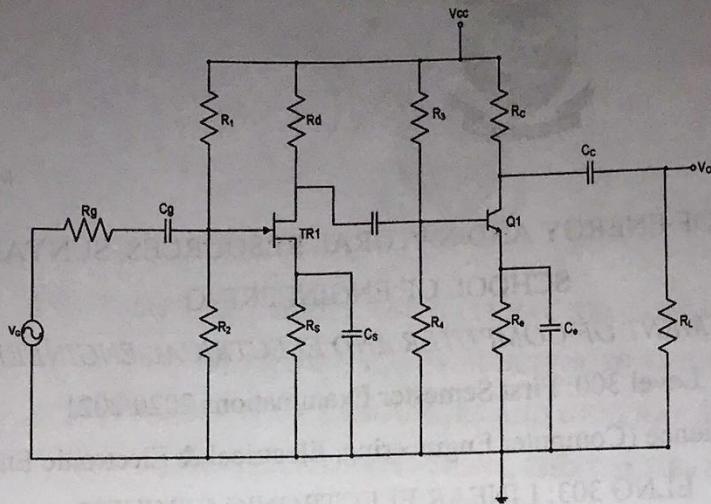


Fig. 2

Question 3

- State and explain the different types of power amplifiers
- A complementary pair class B push-pull amplifier has a supply voltage of 45 V and the transistors are biased so that they are sinusoidally driven to provide a current which is 0.75 of the maximum value. Calculate:
 - The output power supplied to a speaker having a resistance of $15\ \Omega$
 - The collector efficiency
 - The power dissipation of the transistors.

gmV_ds

Question 4

- State the characteristics of an ideal op-amp.
- Fig. 4 shows the schematic of the two op-amp instrumentation amplifier. Find
 - An expression for V_{O1} and V_{O2}
 - Hence or otherwise an expression if $R_1 = R_2 = R_3 = R$
 - The current through R_L if $R_L = 10\text{K}\Omega$ and $V_i = 5\text{V}$

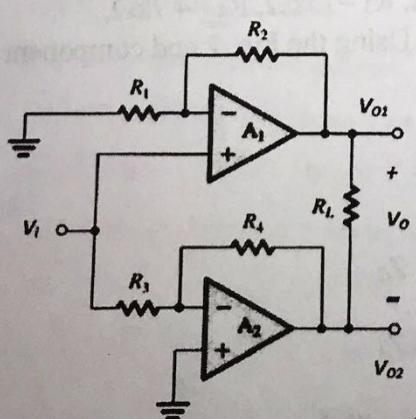


Fig. 4

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$P_{\text{max}} = \frac{V_\text{cc}}{8R_\text{L}}$
 β_{max}

DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING

ELNG 303 – LINEAR ELECTRONIC CIRCUITS, 2018/2019

MID-SEMESTER EXAMINATION

September, 2018

Duration: 70 minutes

Instruction(s): Answer all questions

Question 1.

- List 5 basic processes involved in fabricating an IC using the planner technology.
- For the amplifier shown in figure 1 below take $\beta = 100$ and $r_e = \frac{26mV}{I_E}$
 - Find emitter current I_E and collector current I_C
 - Draw the small signal equivalent circuit using the r_e model
 - Calculate the transistor gain $= 57.7$
 - Calculate the input impedance Z_{in} and output impedance Z_{out}

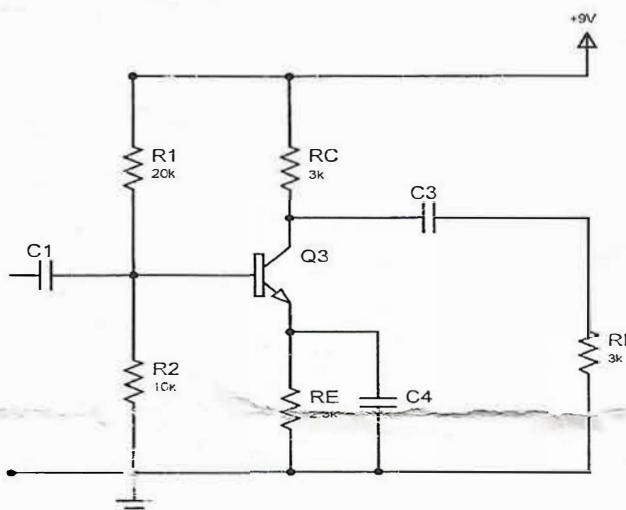


Figure 1

Question 2.

- List out 5 characteristics of ideal Op-Amp
- For the given op-amp circuit in figure 2 below
 - Calculate V_0
 - Find the current I_L flowing through R_L

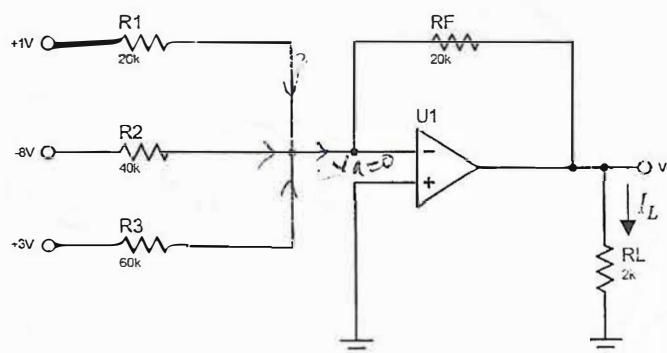


Figure 2: Op-amp circuit



Expt
Epitaxial Growth
Oxidation
Diffusion
Film Deposition

UNIVERSITY OF ENERGY AND NATURAL RESOURCES, SUNYANI, GHANA

SCHOOL OF ENGINEERING

DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING

MIDSEMESTER EXAMINATION, 2017

Bachelor of Science (Computer Engineering, Electrical and Electronic Engineering)

CENG 303: LINEAR ELECTRONIC CIRCUITS

October, 2017

Duration: 1 hr 20min.

INSTRUCTIONS: Answer all Questions. [20 Marks]

Question 1 [10 marks]

- a) List and explain the planar process technology as applied to IC fabrication
- b) A circuit is built around a bi-polar NPN transistor. The Base network has a resistor (R_B) and diode (D_B) in series with the cathode of the diode connected to the base while the collector is connected to a power supply (V_{cc}) through a resistor (R_c). If the emitter is connected to ground:
 - i. Draw the circuit
 - ii. Provide all the masking layout of the circuit.

Question 2 [10 marks]

For the circuit shown in Fig. 1, the transistor parameters are $\beta = 150$, $V_{BE} = 0.7V$ and $V_T = 26mV$.

- a) Determine the operating point parameters
- b) Draw the small signal equivalent circuit based on the r_e model
- c) Determine:
 - i. Gain of the transistor, A_v
 - ii. Input impedance, Z_{in}
 - iii. Gain with signal, A_{vs}
 - iv. Output voltage, given that $V_s = 30mV \sin \omega t$

Photolithography

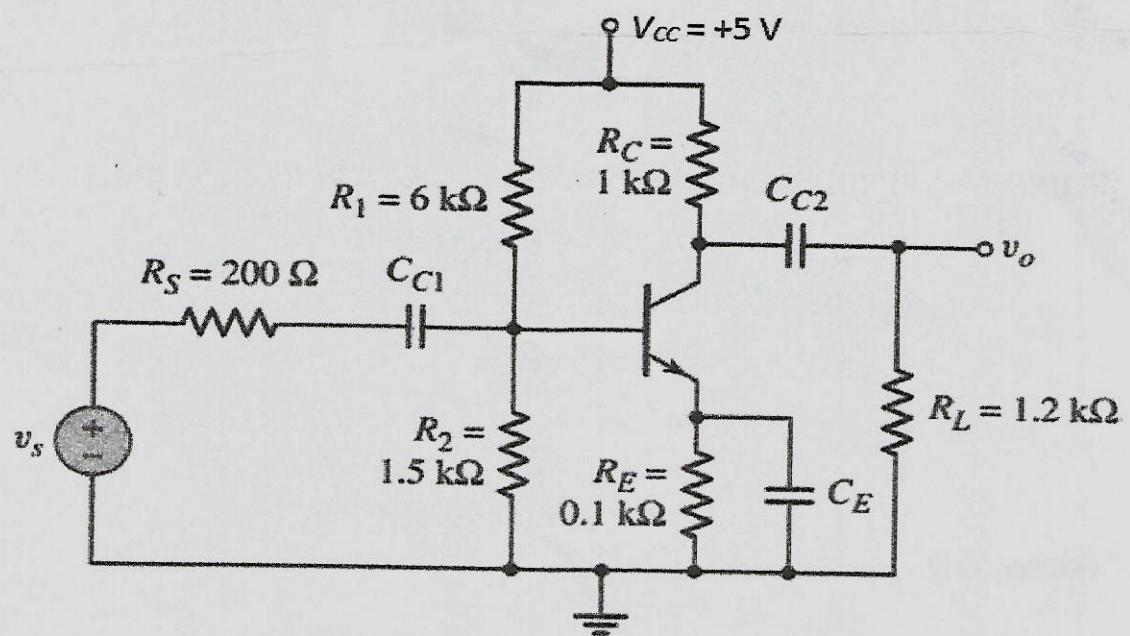
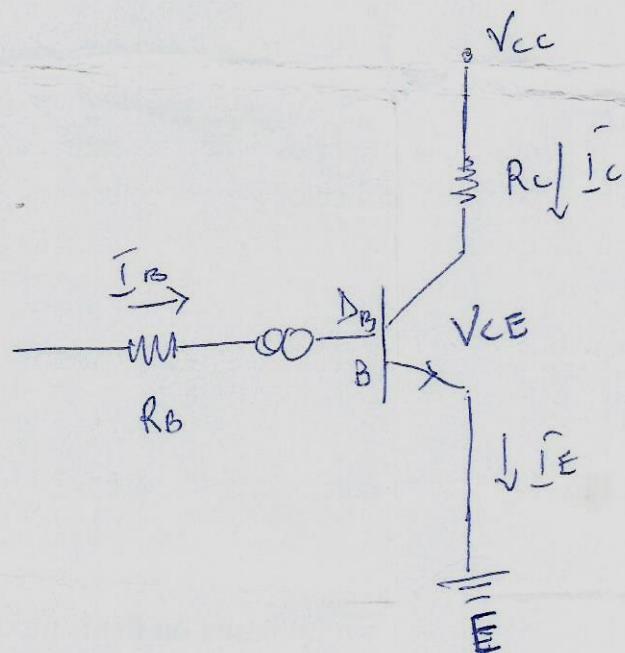


Fig 1





UNIVERSITY OF ENERGY AND NATURAL RESOURCES, SUNYANI, GHANA

SCHOOL OF ENGINEERING

DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING

Level 300: First Semester Examinations 2018/2019

Bachelor of Science (Computer Engineering, Electrical & Electronic Engineering)

ELNG 303: LINEAR ELECTRONIC CIRCUITS

DECEMBER, 2018

TIME: 2½ hours

INSTRUCTIONS: **ANSWER ALL FIVE QUESTIONS: LECTURE MATERIALS CAN BE USED)**

Question 1 [(2x4)+(2+6)=16]

(a) Briefly explain the following terms as applied to IC fabrication

- (i) Epitaxial Growth
- (ii) Oxidation
- (iii) Photolithography
- (iv) Thin film deposition

(b) A circuit is built around a bi-polar NPN transistor. The base network has a diode and a capacitor in series while the collector is connected to a power supply through a resistor. If the emitter is connected to ground:

- i) Draw the circuit
- ii) Provide all the masking layout of the circuit

Question 2 [(4+(4x2)+(2x2)=14]

(a) Given the circuit of Fig. 2.1, draw the small signal equivalent circuit assuming that $r_D = \infty\Omega$ and show that:

$$V_{o1} = -\frac{g_m R_D}{1+g_m R_s} \quad \text{and} \quad V_{o2} = -\frac{g_m R_s}{1+g_m R_s}$$

For $g_m=2mS$, $R_G=1M\Omega$, $R_s=R_D=5k\Omega$, find V_{o1} and V_{o2} if $V_i=20mV \sin\omega t$.

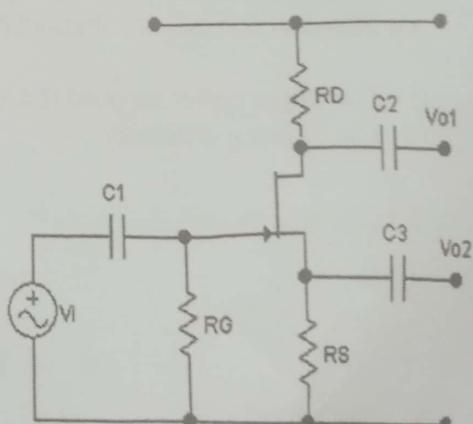


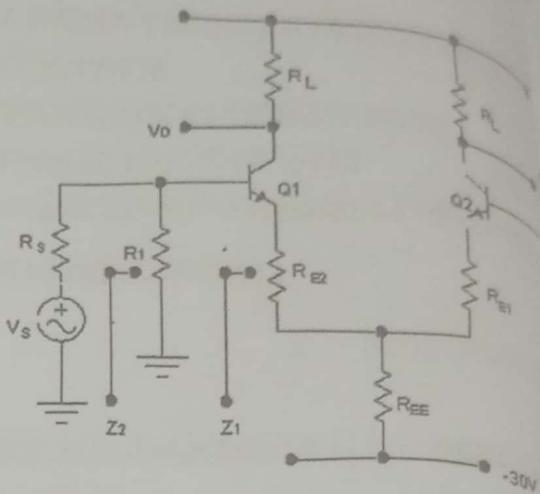
Fig. 2.1

Question 3 [4+(2x5)=14]

(a) State four characteristics of an ideal op-amp.

- (b) For the differential circuit shown in Fig. 3.1, given that $\beta=100$, $R_{E1}=R_{E2}=250\Omega$, $R_{EE}=10k\Omega$, $R_1=50k\Omega$, $R_S=10k\Omega$, $R_L=10k\Omega$ and $V_s = 10mV$, determine:
- The current I_E through R_{EE}
 - The value of r_e , the emitter resistance
 - The impedance Z_1 looking through the base
 - The impedance Z_2
 - The output voltage V_o

Fig. 3.1

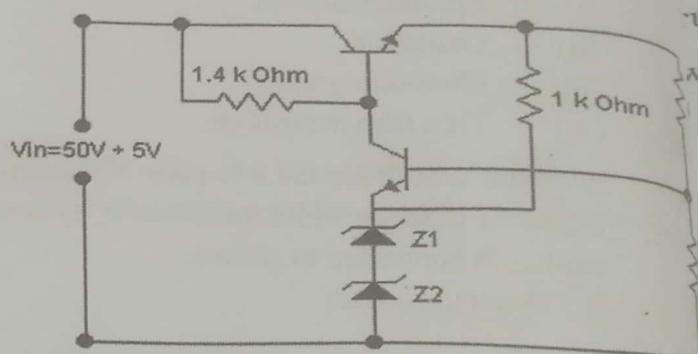


Question 4 [4+4=8]

(a) Distinguish between series and switching voltage regulators

- (b) For the series voltage regulator shown in Fig. 4.1, determine the output regulated voltage if $V_{Z1} = V_{Z2} = 7.5V$, $V_{BE} = 0.7V$, $R_1 = 930\Omega$ and $R_2 = 1570\Omega$.

Fig. 4.1



Question 5 [4+(2x2)=8]

(a) State the differences between the various types of power amplifier

(b) A complementary pair class B push-pull amplifier has a supply voltage of 45 V and the transistors are biased so that they are sinusoidally driven to provide a current 1.2A. Calculate:

- The output power supplied to a speaker having a resistance of 15Ω
- The collector efficiency

duction (s):
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- What is a
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UNIVERSITY OF ENERGY AND NATURAL RESOURCES, SUNYANI, GHANA

SCHOOL OF ENGINEERING

DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING

Level 300: First Semester Examinations 2020/2021

Bachelor of Science (Computer Engineering, Electrical & Electronic Engineering)

ELNG 303: LINEAR ELECTRONIC CIRCUITS

April, 2021

Time: 2½ hours

Material required: Class material (To be brought in by students)

INSTRUCTIONS: ANSWER ALL QUESTIONS (each question carries 15marks)

Question 1

(a) The following processes are used in the fabrication of monolithic ICs, explain each of them in detail:

- i. Oxidation
- ii. Diffusion
- iii. Epitaxy
- iv. Photolithography
- v. Thin Film Deposition

(b) Using the list in (a) provide a step-by-step masking levels of the fabrication of NPN transistor indicating the type of photo-resist used.

Question 2

The two-stage amplifier shown in Fig. 2 is designed with a *FET*, *TR1* and silicon *BJT*, *Q1* with the manufacturer's specifications for β (*Q1*) at 25°C as 150 and g_m (*TR1*) as $3500\mu\text{S}$.

Given $R_g=1.5\text{k}\Omega$, $R_1=6\text{M}\Omega$, $R_2=4\text{M}\Omega$, $R_d=2.4\text{k}\Omega$, $R_s=500\Omega$, $R_3=15\text{k}\Omega$, $R_4=4.7\text{k}\Omega$, $R_c=2.7\text{k}\Omega$, $R_e=470\Omega$, $R_L=2.2\text{k}\Omega$ and supply voltage as 20V. Using the Fig. 2 and component values given, answer the following questions.

Calculate:

- i) Emitter current I_E
- ii) Emitter resistance r_e
- iii) Voltage gain at stage 2, A_{v2}
- iv) Calculate input impedance of the second stage, Z_2
- v) Calculate the gain of the first stage, A_{v1}
- vi) Calculate the input impedance of the first stage Z_1
- vii) Calculate the overall gain, A
- viii) If v_g is a sinusoidal voltage of $5\text{mV}\cos\omega t$, what will the output voltage be?

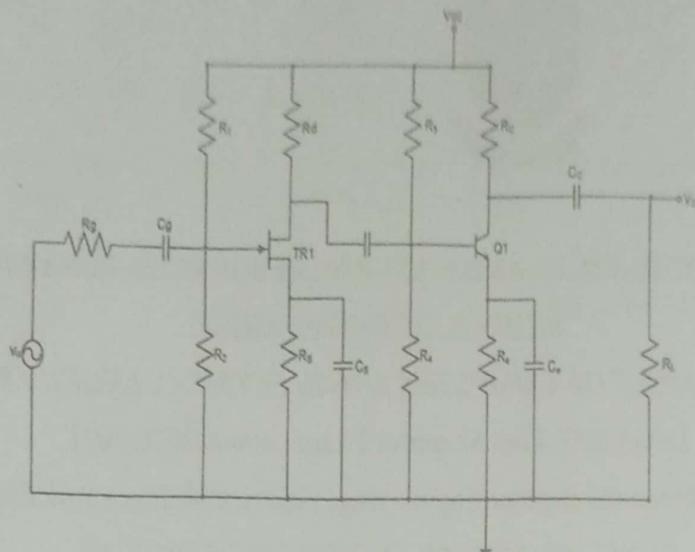


Fig. 2

Question 3

- State and explain the different types of power amplifiers
- A complementary pair class B push-pull amplifier has a supply voltage of 45 V and the transistors are biased so that they are sinusoidally driven to provide a current which is 0.75 of the maximum value. Calculate:
 - The output power supplied to a speaker having a resistance of 15Ω
 - The collector efficiency
 - The power dissipation of the transistors.

Question 4

- State the characteristics of an ideal op-amp.
- Fig. 4 shows the schematic of the two op-amp instrumentation amplifier. Find
 - An expression for V_{O1} and V_{O2}
 - Hence or otherwise an expression if $R_1 = R_2 = R_3 = R$
 - The current through R_L if $R_L = 10K\Omega$ and $V_i = 5V$

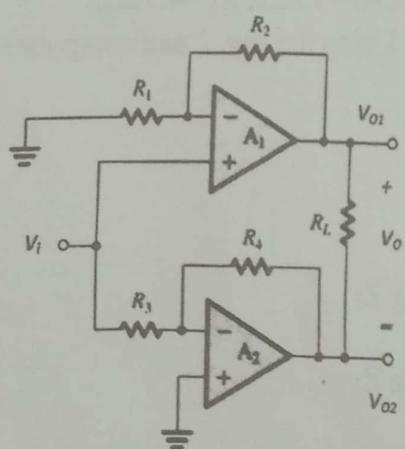


Fig. 4

$$g_m = g_{m0} \left(1 - \frac{\sqrt{g_s}}{V_p}\right)$$

$$g_{m0} = \frac{2\sqrt{g_s}}{|V_p|}$$

UNIVERSITY OF ENERGY AND NATURAL RESOURCES, SUNYANI



SCHOOL OF ENGINEERING

DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING

BSc. (Computer; Electrical & Electronic Engineering)

Mid-Semester Examination, 202/2024

LEVEL 300

ELNG 303: LINEAR ELECTRONIC CIRCUITS

March, 2023

TIME: 1 HOUR

Answer all Questions

Question 1 [5 marks]

Draw the schematic layout diagram of lateral PNP and provide all the masking and diffusion steps in the design.

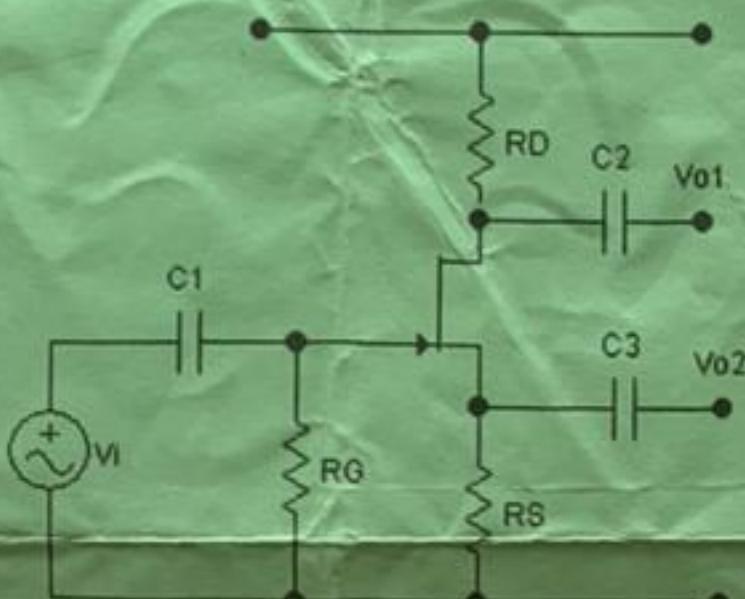
Question 2 {[4+4+4)+(2+2+2)}= 18 marks}}

a) Given the circuit of Fig. 2.1, draw the small signal equivalent circuit and show that:

$$V_{o1} = -\frac{\mu R_D V_i}{R_D + r_d + (\mu + 1)R_S} \quad \text{and} \quad V_{o2} = \frac{\mu R_S V_i}{R_D + r_d + (\mu + 1)R_S}$$

where $\mu = g_m r_d$

b) For $g_m = 2 \text{ mS}$, $r_d = 20 \text{ k}\Omega$, $R_G = 1 \text{ M}\Omega$, $R_S = R_D = 5 \text{ k}\Omega$, find V_{o1} and V_{o2} if $V_i = V_m \sin \omega t$. What is the impedances seen from the drain and source terminals?



$$R = \sqrt{\frac{L}{\omega}}$$

494 (515)

Fig. 2.1

Question 3

a) State the five characteristics of an ideal op-amp.

b) Using Fig. 3.1 show that the output is given by

$$V_o = \left(\frac{R_2}{R_2 + R_f} \right) \left(\frac{R_3}{R_1 + R_3} \right) V_1 - \frac{R_f}{R_2} V_2$$

Hence if $R_1 = 20\text{k}\Omega$, $R_2 = 100\text{k}\Omega$, $R_3 = 20\text{k}\Omega$, $R_f = 100\text{k}\Omega$, $V_1 = 2.5\text{V}$ and $V_2 = 1.5\text{V}$, determine the value of V_o .

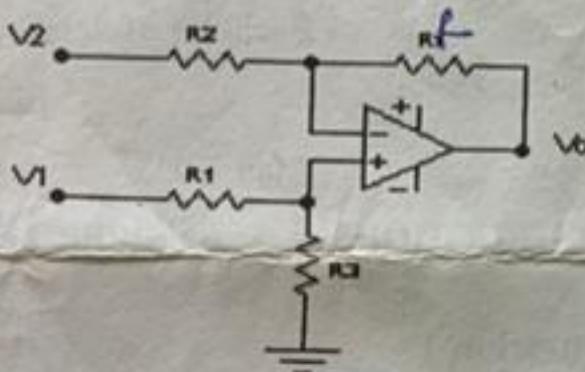


Fig. 3.1

- c) For the series regulator given in Fig. 3.2, $V_{in} = 15\text{V}$, $R = 200\Omega$, the transistor $\beta = 50$, $R_L = 1.2\text{K}\Omega$, $V_Z = 10\text{V}$ and $V_{BE} = 0.4\text{V}$. Calculate:
 (i) output voltage
 (ii) load current
 (iii) the base current in the transistor
 (iv) zener current.

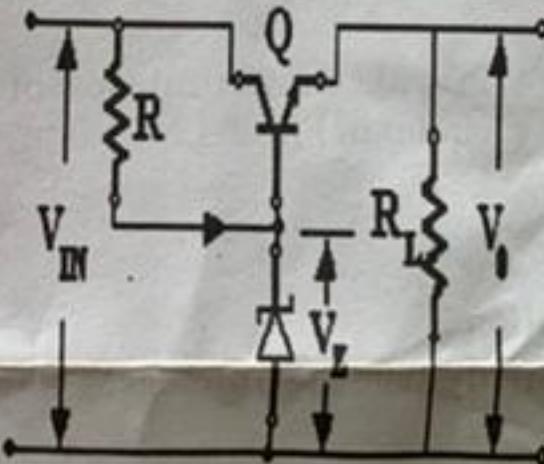


Fig. 3.2

Question 4

a) State and explain the difference between Class A and Class B power amplifiers

b) Class A power amplifiers are regarded as very inefficient power amplifiers. Show that the efficiency of a Class A power amplifier cannot exceed 25%

- c) For a class B amplifier using a supply of $V_{cc} = 25\text{V}$ and driving a load of 4Ω . Calculate the
 i) maximum input power,
 ii) maximum output power,
 iii) maximum efficiency
 iv) input voltage for maximum power operation and
 v) power dissipated by the output transistors at this voltage.

UNIVERSITY OF ENERGY AND NATURAL RESOURCES, SUNYANI, GHANA
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DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING

Level 300: First Semester Examinations 2022/2023

Bachelor of Science (Computer Engineering, Electrical & Electronic Engineering)
 ELNG 303: LINEAR ELECTRONIC CIRCUITS

May, 2023

Time: 2 hours

INSTRUCTIONS: ANSWER ALL QUESTIONS (each question carries 15 marks)

Question 1

- a) Define the following as applied to IC fabrication process.
- epitaxy
 - oxidation
 - photolithography
 - thin-film deposition

- b) Provide the vertical view of the masking layout of the circuit in Fig. 1.1

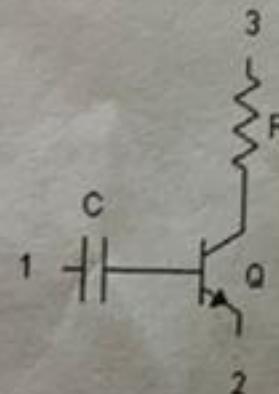


Fig. 1.1

Question 2

- a) Briefly state the differences between Bipolar Transistor and Field Effect Transistor.
- b) Given the circuit of Fig. 2.1, draw the small signal equivalent circuit and show that:

$$V_{o1} = -\frac{\mu R_D V_i}{R_D + r_d + (\mu + 1)R_s} \quad \text{and} \quad V_{o2} = \frac{\mu R_s V_i}{R_D + r_d + (\mu + 1)R_s}$$

where $\mu = g_m r_d$

- c) For $g_m = 2 \text{ mS}$, $r_d = 20 \text{ k}\Omega$, $R_G = 1 \text{ M}\Omega$, $R_S = R_D = 5 \text{ k}\Omega$, find V_{o1} and V_{o2} if $V_i = V_m \sin \omega t$. What is the impedances seen from the drain and source terminals?

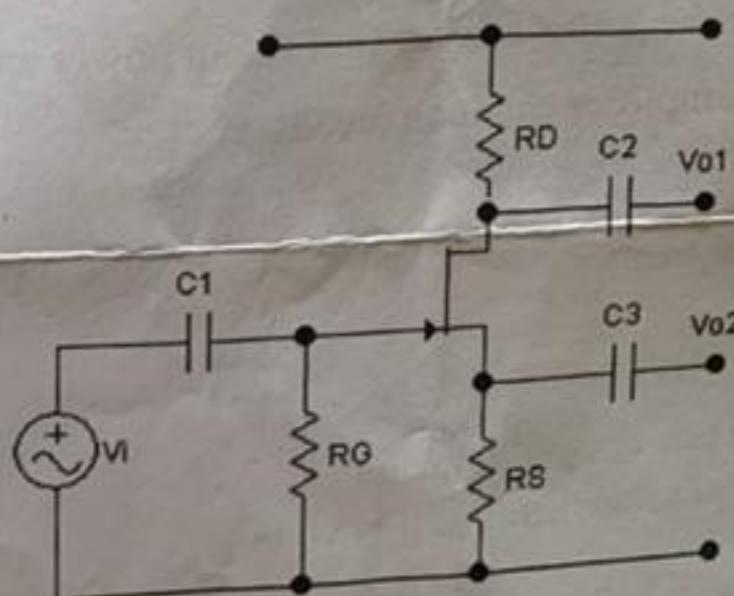


Fig. 2.1