UNIVERSITY OF ENERGY AND NATURAL RESOURCES, SUNYANI, GHANA
SCHOOL OF ENGINEERING
DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING
Level 300: First Semester Examinations 2019/2020
Bachelor of Science (Computer Engineering, Electrical & Electronic Engineering)
ELNG 303: LINEAR ELECTRONIC CIRCUITS
DECEMBER, 2019 MDK Time: 2½ hours

INSTRUCTIONS: ANSWER ALL FOUR QUESTIONS)

Question One [3+(2+4)+4=13]

a) With the aid of diagrams, briefly describe the process of photolithography used in the fabrication of monolithic ICs.

b) A circuit is built around a bi-polar NPN transistor. The base network has a diode and a capacitor in series while the collector is connected to a power supply through a resistor. If the emitter is connected to ground:
   i) Draw the circuit
   ii) Provide all the masking layout of the circuit

c) Fig1.1 shows a p-diffusion resistor fabricated with a sheet resistance of 120 Ohm per square. The corners and the pads are estimated to have 0.6 of the value of a regular sheet resistance. Find the value of the resulting resistor.

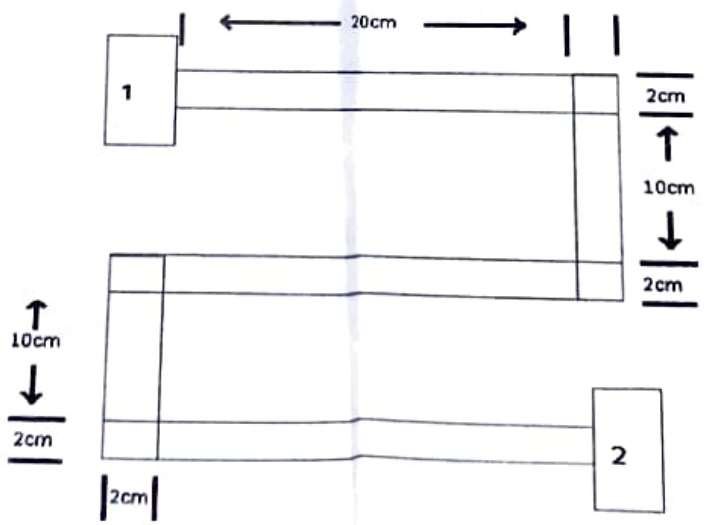

Fig1.1

* Infinite input impedance
* Infinite bandwidth
* Zero output impedance
* Infinite open-loop voltage gain
* Infinite common-mode rejection ratio.

Question Two [2+4+6+6=18]

a) Mention the characteristics of an ideal op-amp.

b) Draw a shunt regulator and clearly show the four main elements. Derive an expression for the output voltage.

c) A differential amplifier has an output voltage given by $Vo = 9\ V_1 - 10V_2$. The two inputs are $V_1 = 10$ mV and $V_2 = 20$ mV. Determine common mode input voltage, common mode gain and the differential gain.

d) In Op-Amp circuit of Fig. 2.1, find *Vo* in terms of *V1* and *V2* assume the ideal op amp model. Find an expression for *Vo*. If $V_1 = 1.5$V and $V_2 = 3.0$V, find *Vo* for $R_1 = 1k\Omega$ and $R_2 = 2k\Omega$

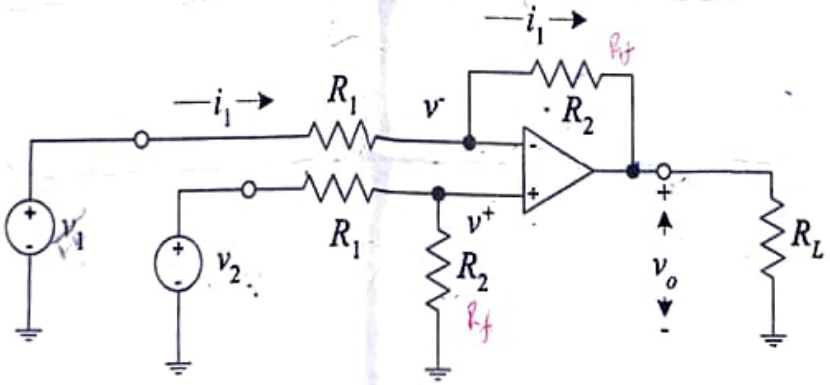

Fig 2.1

Question Three [2+4+(2x3) =12]

a) State and explain the various classifications of power amplifiers.

b) For a class B power amplifier, show that the maximum efficiency is 78.5%.

c) For a class B amplifier providing a 20V peak-to-peak signal to an 8 Ω speaker and a power supply of $V_{cc} = 15$V, determine:
   i) Input power
   ii) Output power
   iii) Circuit efficiency

Question Four [4+4+(3x3) =17]

Consider the common-emitter BJT amplifier circuit shown in Figure 4,1. Take $\beta_1 = \beta_2 = 200$, $V_{BE} = 0.7V$ and thermal voltage as 26V. Answer the following questions.

(a) Determine the emitter current I_{E2}, I_{E1} and hence r_{e2} and r_{e1}

(b) Draw the AC equivalent circuit and determine:
- i) Input impedance, Z_1, Z_2 and Z_{in}
- ii) Gain of the transistor, A_{v2} and A_{v1}
- iii) Output voltage gain with signal, A_{vs}

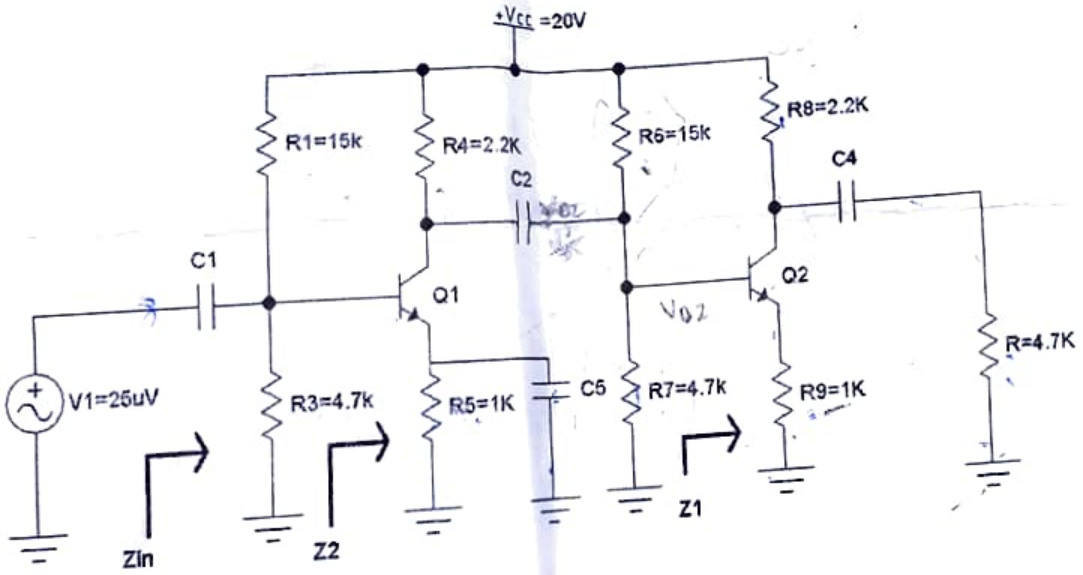

Fig. 4.1

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DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING

Level 300: End of Semester Examinations 2021/2022

Bachelor of Science (Computer, Electrical & Electronic Engineering)

ELNG 303: LINEAR ELECTRONIC CIRCUITS

May/June, 2022 MDK Time: 2½ hours

Material required: Class material (**To be brought in by students**)

INSTRUCTIONS: ANSWER ALL QUESTIONS

Question 1 (12 Marks)

(a) State an explain briefly the five planar processes in the fabrication of monolithic IC

i State the main difference between negative and positive photoresist and at what condition each is applied

ii State the significance of passivation in IC fabrication and the material used.

(b) Provide a stet-by-step masking levels for the fabrication of a **NPN** Transistor indicating the type of photo-resist used.

Question 2 (20 Marks) MDK

The two-stage amplifier shown in Fig. 2 is designed with a *FET*, TR1 and silicon *BJT*, Q1 with the manufacturer's specifications for β (Q1) at 25°C as 150 and g_m (TR1) as 3500μS. Given Rg=1.5kΩ R_1=6 MΩ, R_2 =4MΩ R_d =2.4kΩ, Rs=500Ω, R_3 =15kΩ, R_4 =4.7kΩ, Rc=2.7kΩ, Re=470Ω, R_L=2.2kΩ and supply voltage as 20V. Using the Fig.2 and component values given, answer the following questions.

Calculate:

i) Draw the small signal equivalent circuit using the model treated in class
ii) Emitter current I_E
iii) Emitter resistance r_e
iv) Voltage gain at stage 2 (BJT), A_{V2}
v) Calculate input impedance of the second stage BJT), Z_2
vi) Calculate the gain of the first stage (FET), A_{V1}
vii) Calculate the input impedance of the first stage Z_1
viii) Calculate the overall gain with signal, A_{VS}
ix) If Vs is a sinusoidal voltage of 5mVcosωt, what will the output voltage be?
x) On the same graph plot the input and output voltage against ωt.

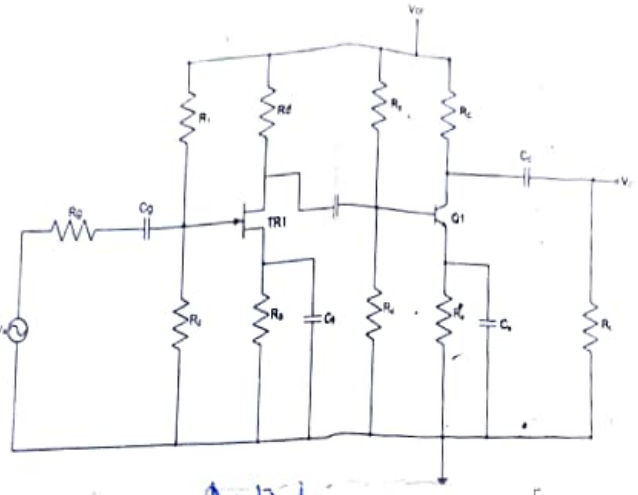

Fig. 2

MDK

Question 3 (16 Marks)

(a) State and explain the different between Class A and Class B power amplifiers.

(b) How do you minimize the effect of crossover distortion in class B power amplifier?

(c) A class A power amplifier is supplied with 20V and biased to operate at a quiescent base current of 19.3mA with a base peak current of 10mA and a collector load of 20 Ω. Given that β=25, Calculate the amplifier:

i Input power, $P_{i(dc)}$
ii Output power, $P_{o(ac)}$
iii Efficiency, η

(d) A complementary push-pull amplifier has to deliver 2.5 W into a load of 8 Ω. Determine:
(i) The maximum power dissipation required for each transistor;
(ii) The supply voltage required;
(iii) The peak load current.

MDK

Question 4 (12 Marks)

(a) State five characteristics of an ideal op-amp.

(b) For the difference amplifier shown in Fig. 4.1, find an expression for the output voltage Vo. Evaluate Vo if R_1 =10kΩ, R_2 =R_3 =15kΩ and R_f = 20kΩ.

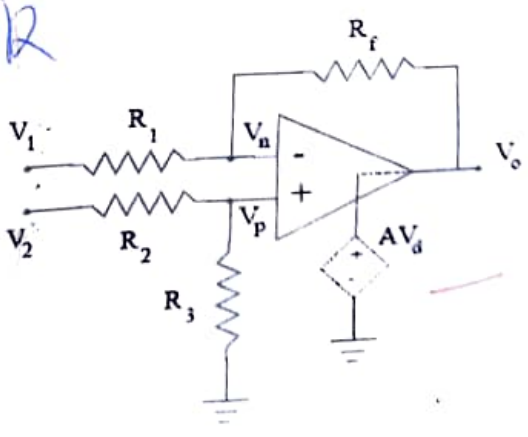

Fig. 4.1

(c) Evaluate the gain.

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Level 300: First Semester Examinations 2020/2021

Bachelor of Science (Computer Engineering, Electrical & Electronic Engineering)

ELNG 303: LINEAR ELECTRONIC CIRCUITS

April, 2021 MDK Time: 2½ hours

terial required: Class material (**To be brought in by students**)

STRUCTIONS: ANSWER ALL QUESTIONS (each question carries 15marks)

estion 1

(a) The following processes are used in the fabrication of monolithic ICs, explain each of them in detail:

i. Oxidation
ii. Diffusion
iii. Epitaxy
iv. Photolithography
v. Thin Film Deposition

(b) Using the list in (a) provide a stet-by-step masking levels of the fabrication of NPN transistor indicating the type of photo-resist used.

estion 2 MDK

e two-stage amplifier shown in Fig. 2 is designed with a *FET*, TR1 and silicon *BJT*, Q1 h the manufacturer's specifications for β (Q1) at 25°C as 150 and g_m (TR1) as 3500μS. ven Rg=1.5kΩ R_1=6 MΩ, R_2 =4MΩ R_d =2.4kΩ, Rs=500Ω, R_3 =15kΩ, R_4 =4.7kΩ, =2.7kΩ, Re=470Ω, R_L=2.2kΩ and supply voltage as 20V. Using the Fig. 2 and component ues given, answer the following questions.

lculate:

i) Emitter current I_E
ii) Emitter resistance r_e
iii) Voltage gain at stage 2, A_{V2}
iv) Calculate input impedance of the second stage, Z_2
v) Calculate the gain of the first stage, A_{V1}
vi) Calculate the input impedance of the first stage Z_1
vii) Calculate the overall gain, A
viii) If vg is a sinusoidal voltage of 5mVcosωt, what will the output voltage be?

. Diawuo

UNIVERSITY OF ENERGY AND NATURAL RESOURCES, SUNYANI, GHANA
SCHOOL OF ENGINEERING
DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING
Level 300 Mid-Semester Examinations 2021/2022

Bachelor of Science (Computer, Electrical and Electronic Engineering)

ELNG 303: LINEAR ELECTRONIC CIRCUITS
April, 2022 Time: 1 hour

Attempt all questions

Question 1

(a) Briefly explain the following terms as applied to IC fabrication

(i) Epitaxial Growth
(ii) Photolithography
(iii) Thin film deposition

(b) A circuit is built around a bi-polar NPN transistor. The base network has a diode and a capacitor in series while the collector is connected to a power supply through a resistor. If the emitter is connected to ground:

i) Draw the circuit
ii) Provide all the masking layout of the circuit.

Question 2

Given the circuit diagram of Fig. 2 with $V_{CC} = 12V$, and $\beta = 52$.

(a) Using the re model; draw the small signal equivalent circuit.

(b) Determine:

(i) The gain of the transistor.
(ii) The input impedance of the transistor.
(iii) The overall gain of the amplifier.

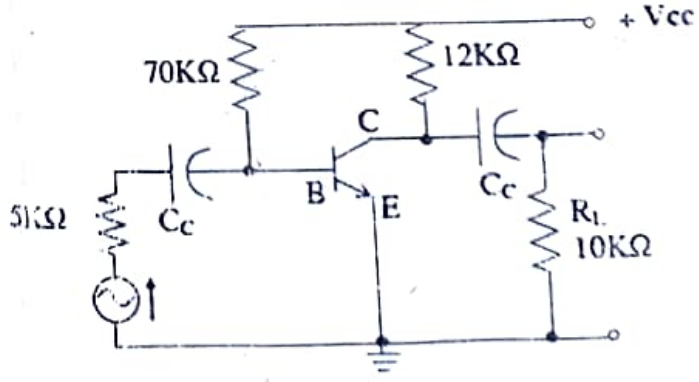

Fig. 2