C A A A A A

							A A A				
Cape Use	PIN	PROC NAME	NAME	MODE0	MODE1	MODE2	MODE3	MODE4	MODE5	MODE6	MOD
							GND				
		R9	GPIO1_6	gpmc_ad6	mmc1_dat6				-	-	gpio1
		Т9	GPIO1_7	gpmc_ad7	mmc1_dat7				-	-	gpio1
		R8	GPIO1_2	gpmc_ad2	mmc1_dat2				-	-	gpio1
		T8	GPIO1_3	gpmc_ad3	mmc1_dat3				-	-	gpio:
	7	R7	TIMER4	gpmc_advn_ale		timer4			-	-	gpio2
	8	T7	TIMER7	gpmc_oen_ren		timer7			-	-	gpio
С	9	T6	TIMER5	gpmc_be0n_cle		timer5			-	-	gpio
N C	10	U6	TIMER6	gpmc_wen		timer6			-	-	gpio
R C	11*	R12	GPIO1_13	gpmc_ad13	lcd_data18	mmc1_dat5*	mmc2_dat1	eQEP2B_in	pr1_mii0_txd1	pr1_pru0_pru_r30_15	gpio1
R	12*	T12	GPIO1_12	gpmc_ad12	lcd_data19	mmc1_dat4*	mmc2_dat0	EQEP2A_IN	pr1_mii0_txd2	pr1_pru0_pru_r30_14	gpio1
N CAN	13*	T10	EHRPWM2B	gpmc_ad9	lcd_data22	mmc1_dat1*	mmc2_dat5	ehrpwm2B	pr1_mii0_col	-	gpio0
	14*	T11	GPIO0_26	gpmc_ad10	lcd_data21	mmc1_dat2*	mmc2_dat6	ehrpwm2_tripzone	pr1_mii0_txen	-	gpio(
	15*	U13	GPIO1_15	gpmc_ad15	lcd_data16	mmc1_dat7*	mmc2_dat3	eQEP2_strobe	pr1_ecap0_ecap_capin_apw	pr1_pru0_pru_r31_15	gpio1
	16*	V13	GPIO1_14	gpmc_ad14	lcd_data17	mmc1_dat6*	mmc2_dat2	eQEP2_index	m o pr1_mii0_txd0	pr1_pru0_pru_r31_14	gpio1
	17*	U12	GPIO0_27	gpmc_ad11	lcd_data20	mmc1_dat3*	mmc2_dat7	ehrpwm0_synco	pr1_mii0_txd3	-	gpio(
								cmpwino_synco			
	18	V12	GPIO2_1	gpmc_clk_mux0	lcd_memory_clk	gpmc_wait1	mmc2_clk		pr1_mdio_mdclk	mcasp0_fsr	gpio
N AN	19*	U10	EHRPWM2A	gpmc_ad8	lcd_data23	mmc1_dat0*	mmc2_dat4	ehrpwm2A	pr1_mii_mt0_clk	-	gpio0
		V9	GPIO1_31	gpmc_csn2	gpmc_be1n	mmc1_cmd*		pr1_edio_data_out7	pr1_pru1_pru_r30_13	pr1_pru1_pru_r31_13	gpio
		U9	GPIO1_30	gpmc_csn1	gpmc_clk	mmc1_clk*		pr1_edio_data_out6	pr1_pru1_pru_r30_12	pr1_pru1_pru_r31_12	gpio
		V8	GPIO1_5	gpmc_ad5	mmc1_dat5			-	-	-	gpio
		U8	GPIO1_4	gpmc_ad4	mmc1_dat4			-	-	-	gpio
		V7	GPIO1_1	gpmc_ad1	mmc1_dat1			-	-	-	gpio
		U7	GPIO1_0	gpmc_ad0	mmc1_dat0			-	-	-	gpic
	26	V6	GPIO1_29	gpmc_csn0				-	-	-	gpio
W	27*	U5	GPIO2_22	lcd_vsync*	gpmc_a8			pr1_edio_data_out2	pr1_pru1_pru_r30_8	pr1_pru1_pru_r31_8	gpio
W	28*	V5	GPIO2_24	lcd_pclk*	gpmc_a10			pr1_edio_data_out4	pr1_pru1_pru_r30_10	pr1_pru1_pru_r31_10	gpio
W	29*	R5	GPIO2_23	lcd_hsync*	gpmc_a9			pr1_edio_data_out3	pr1 pru1 pru r30 9	pr1_pru1_pru_r31_9	gpio
W	30*	R6	GPIO2_25	lcd_ac_bias_en*	gpmc_a11			pr1_edio_data_out5	pr1_pru1_pru_r30_11	pr1_pru1_pru_r31_11	gpio
	31*	V4	UART5_CTSN	lcd_data14*	gpmc_a18	eQEP1_index	mcasp0_axr1	uart5_rxd	pr1_mii0_rxd3	uart5_ctsn	gpio(
	32*	T5	UART5_RTSN	lcd_data15*	gpmc_a19	eQEP1_strobe	mcasp0_ahclkx	mcasp0_axr3	pr1_mii0_rxdv	uart5_rtsn	gpio(
R C	33*	V3	UART4_RTSN	lcd_data13*	gpmc_a17	eQEP1B_in	mcasp0_fsr	mcasp0_axr3	pr1_mii0_rxer	uart4_rtsn	gpio
	34*	U4	UART3_RTSN	lcd_data11*	gpmc_a15	ehrpwm1B	mcasp0_ahclkr	mcasp0_axr2	pr1_mii0_rxd0	uart3_rtsn	gpio
R	35*	V2	UART4_CTSN	lcd_data12*	gpmc_a16	eQEP1A_in	mcasp0_aclkr	mcasp0_axr2	pr1_mii0_rxlink	uart4_ctsn	gpio
	36*	U3	UART3_CTSN	lcd_data10*	gpmc_a14	ehrpwm1A	mcasp0_axr0	-	pr1_mii0_rxd1	uart3_ctsn	gpio2
	37*	U1	UART5_TXD	lcd_data8*	gpmc_a12	ehrpwm1_tripzone	mcasp0_aclkx	uart5_txd	pr1_mii0_rxd3	uart2_ctsn	gpio2
N C	38*	U2	UART5_RXD	lcd_data9*	gpmc_a13	ehrpwm0_synco	mcasp0_fsx	uart5_rxd	pr1_mii0_rxd2	uart2_rtsn	gpio
W	39*	T3	GPIO2_12	lcd_data6*	gpmc_a6		eQEP2_index	pr1_edio_data_out6	pr1_pru1_pru_r30_6	pr1_pru1_pru_r31_6	gpio2
w	40*	T4	GPIO2_13	lcd_data7*	gpmc_a7		eQEP2_strobe	pr1_edio_data_out7	pr1_pru1_pru_r30_7	pr1_pru1_pru_r31_7	gpio2
W	41*	T1	GPIO2_10	lcd_data4*	gpmc_a4		eQEP2A_in	-	pr1_pru1_pru_r30_4	pr1_pru1_pru_r31_4	gpio2
w	42*	T2	GPIO2_11	lcd_data5*	gpmc_a5		eQEP2B_in	-	pr1_pru1_pru_r30_5	pr1_pru1_pru_r31_5	gpio2
N C	43*	R3	GPIO2_8	lcd_data2*	gpmc_a2		ehrpwm2_tripzone	-	pr1_pru1_pru_r30_2	pr1_pru1_pru_r31_2	gpio
N	44*	R4	GPIO2_9	lcd_data3*	gpmc_a3		ehrpwm0_synco	-	pr1_pru1_pru_r30_3	pr1_pru1_pru_r31_3	gpio
N	45*	R1	GPIO2_6	lcd_data0*	gpmc_a0		ehrpwm2A	-	pr1_pru1_pru_r30_0	pr1_pru1_pru_r31_0	gpio
N C	46*	R2	GPIO2_7	lcd_data1*	gpmc_a1		ehrpwm2B	-	pr1_pru1_pru_r30_1	pr1_pru1_pru_r31_1	gpio

Tape Use PIN N/	A10 T17	gpmc_wait0 gpmc_be1n gpmc_wpn gpmc_a2 gpmc_a0 gpmc_a3 spi0_cs0 spi0_d1 uart1_rtsn uart1_ctsn spi0_d0 spi0_sclk gpmc_a1 uart1_txd mcasp0_ahclkx	mii2_crs mii2_col mii2_rxerr mii2_txd3 gmii2_txen mii2_txd2 mmc2_sdwp mmc1_sdwp timer5 timer6 uart2_txd uart2_rxd gmii2_rxdv mmc2_sdwp	gpmc_csn4 gpmc_csn6 gpmc_csn5 rgmii2_td3 rmii2_tctl rgmii2_td2 I2C1_SCL I2C1_SDA dcan0_rx dcan0_tx I2C2_SCL I2C2_SDA rgmii2_rxdv dcan1_rx	rmii2_crs_dv mmc2_dat3 rmii2_rxerr mmc2_dat1 mii2_txen mmc2_dat2 ehrpwm0_synci ehrpwm0_tripzone I2C2_SCL I2C2_SDA ehrpwm0B ehrpwm0A mmc2_dat0 I2C1_SCL	MODE4 GND 3.3V VDD_5V SYS_5V PWR_BUT Reset Out mmc1_sdcd gpmc_dir mmc2_sdcd gpmc_a18 gpmc_a16 gpmc_a19 spi1_cs1 spi1_cs0	pr1_mii1_col pr1_mii1_rxlink pr1_mii1_txen pr1_mii1_txd2 pr1_mii1_txd1 pr1_edio_data_in1 pr1_edio_data_in0 pr1_uart0_rts_n pr1_uart0_tcs_n pr1_edio_latc_in pr1_edio_sof pr1_mii1_txd3	uart4_rxd mcasp0_aclkr uart4_txd ehrpwm1A ehrpwm1E pr1_edio_data_out1 pr1_edio_data_out0 pr1_edc_latch1_in pr1_edc_latch0_in EMU3 EMU2 ehrpwm0_synco	gpio0[30 gpio1[2: gpio0[3] gpio1[1: gpio1[4: gpio0[4: gpio0[4: gpio0[12: gpio0[3] gpio0[2: gpio1[1:
W 3,4 W 5,6 7,8 9 10 YA, n 11 N 12 N C 13 N AN A 14 N 15 N CAN A 16 A, 17 A, 18 A, 19 A, 19 YA, YA, 21 YA, 22 YA, YA, 21 YA, 22 YA, YA, YA, 22 YA,	T17 UART4_RXD U18 GPIO1_28 U17 UART4_TXD U14 EHRPWM1A R13 GPIO1_16 T14 EHRPWM1B A16 I2C1_SCL B16 I2C1_SDA D17 I2C2_SCL D18 I2C2_SDA B17 UART2_TXD A17 UART2_RXD V14 GPIO1_17 D15 UART1_TXD A14 GPIO3_21	gpmc_be1n gpmc_wpn gpmc_a2 gpmc_a0 gpmc_a3 spi0_cs0 spi0_d1 uart1_rtsn uart1_ctsn spi0_d0 spi0_sclk gpmc_a1 uart1_txd	mil2_col mil2_rxerr mil2_txd3 gmil2_txen mil2_txd2 mmc2_sdwp mmc1_sdwp timer5 timer6 uart2_txd uart2_rxd gmil2_rxdv mmc2_sdwp	gpmc_csn6 gpmc_csn5 rgmii2_td3 rmii2_tctl rgmii2_td2 I2C1_SCL I2C1_SDA dcan0_rx dcan0_tx I2C2_SCL I2C2_SDA rgmii2_rxdv	mmc2_dat3 rmii2_rxerr mmc2_dat1 mii2_txen mmc2_dat2 ehrpwm0_synci ehrpwm0_tripzone I2C2_SCL I2C2_SDA ehrpwm0B ehrpwm0A mmc2_dat0	3.3V VDD_5V SYS_5V PWR_BUT Reset Out mmc1_sdcd gpmc_dir mmc2_sdcd gpmc_a18 gpmc_a16 gpmc_a19 spi1_cs1 spi1_cs0	pr1_mii1_rxlink pr1_mii1_txen pr1_mii1_txe2 pr1_mii1_txd1 pr1_edio_data_in1 pr1_edio_data_in0 pr1_uart0_rts_n pr1_uart0_cts_n pr1_edio_lato_in pr1_edio_sof pr1_mii1_txd3	mcasp_aclkr uart4_txd ehrpwm1A ehrpwm1_tripzone_input ehrpwm1B pr1_edio_data_out1 pr1_edio_data_out0 pr1_edc_latch1_in pr1_edc_latch0_in EMU3 EMU2 ehrpwm0_synco	gpio1[2 gpio0[3 gpio1[18 gpio1[1] f gpio0[5 gpio0[4 gpio0[1: gpio0[1: gpio0[3 gpio0[2
W 5,6 7,8 9 10 YA, n 11 N 12 N C 13 N AN A 14 N 15 N CAN A 16 A, 17 A, 18 A, 19 A, 19 YA, 21 YA, 21 YA, 22 YA, 21 YA, 22 YA, 22 YA YA, 22 YA YA, 22 YA YA YA ZA YA YA ZA ZA YA ZA ZA YA ZA ZA YA ZA ZA ZA YA ZA	T17 UART4_RXD U18 GPIO1_28 U17 UART4_TXD U14 EHRPWM1A R13 GPIO1_16 T14 EHRPWM1B A16 I2C1_SCL B16 I2C1_SDA D17 I2C2_SCL D18 I2C2_SDA B17 UART2_TXD A17 UART2_RXD V14 GPIO1_17 D15 UART1_TXD A14 GPIO3_21	gpmc_be1n gpmc_wpn gpmc_a2 gpmc_a0 gpmc_a3 spi0_cs0 spi0_d1 uart1_rtsn uart1_ctsn spi0_d0 spi0_sclk gpmc_a1 uart1_txd	mil2_col mil2_rxerr mil2_txd3 gmil2_txen mil2_txd2 mmc2_sdwp mmc1_sdwp timer5 timer6 uart2_txd uart2_rxd gmil2_rxdv mmc2_sdwp	gpmc_csn6 gpmc_csn5 rgmii2_td3 rmii2_tctl rgmii2_td2 I2C1_SCL I2C1_SDA dcan0_rx dcan0_tx I2C2_SCL I2C2_SDA rgmii2_rxdv	mmc2_dat3 rmii2_rxerr mmc2_dat1 mii2_txen mmc2_dat2 ehrpwm0_synci ehrpwm0_tripzone I2C2_SCL I2C2_SDA ehrpwm0B ehrpwm0A mmc2_dat0	VDD_5V SYS_5V PWR_BUT Reset Out mmc1_sdcd gpmc_dir mmc2_sdcd gpmc_a18 gpmc_a16 gpmc_a19 spi1_cs1 spi1_cs0	pr1_mii1_rxlink pr1_mii1_txen pr1_mii1_txe2 pr1_mii1_txd1 pr1_edio_data_in1 pr1_edio_data_in0 pr1_uart0_rts_n pr1_uart0_cts_n pr1_edio_lato_in pr1_edio_sof pr1_mii1_txd3	mcasp_aclkr uart4_txd ehrpwm1A ehrpwm1_tripzone_input ehrpwm1B pr1_edio_data_out1 pr1_edio_data_out0 pr1_edc_latch1_in pr1_edc_latch0_in EMU3 EMU2 ehrpwm0_synco	gpio1[2 gpio0[3 gpio1[1: gpio1[1] f gpio0[5 gpio0[4 gpio0[1: gpio0[3 gpio0[2]
7,8 9 10 YA n 11 N 12 N C 13 N AN A 14 N 15 N CAN A 16 A 17 A 18 A 19 A 19 YA 19 YA 20 YA 21 YA 21 YA 22 XY 24 N 25 N 26 N 29	T17 UART4_RXD U18 GPIO1_28 U17 UART4_TXD U14 EHRPWM1A R13 GPIO1_16 T14 EHRPWM1B A16 I2C1_SCL B16 I2C1_SDA D17 I2C2_SCL D18 I2C2_SDA B17 UART2_TXD A17 UART2_RXD V14 GPIO1_17 D15 UART1_TXD A14 GPIO3_21	gpmc_be1n gpmc_wpn gpmc_a2 gpmc_a0 gpmc_a3 spi0_cs0 spi0_d1 uart1_rtsn uart1_ctsn spi0_d0 spi0_sclk gpmc_a1 uart1_txd	mil2_col mil2_rxerr mil2_txd3 gmil2_txen mil2_txd2 mmc2_sdwp mmc1_sdwp timer5 timer6 uart2_txd uart2_rxd gmil2_rxdv mmc2_sdwp	gpmc_csn6 gpmc_csn5 rgmii2_td3 rmii2_tctl rgmii2_td2 I2C1_SCL I2C1_SDA dcan0_rx dcan0_tx I2C2_SCL I2C2_SDA rgmii2_rxdv	mmc2_dat3 rmii2_rxerr mmc2_dat1 mii2_txen mmc2_dat2 ehrpwm0_synci ehrpwm0_tripzone I2C2_SCL I2C2_SDA ehrpwm0B ehrpwm0A mmc2_dat0	SYS_5V PWR_BUT Reset Out mmc1_sdcd gpmc_dir mmc2_sdcd gpmc_a18 gpmc_a16 gpmc_a19 spi1_cs1 spi1_cs0	pr1_mii1_rxlink pr1_mii1_txen pr1_mii1_txe2 pr1_mii1_txd1 pr1_edio_data_in1 pr1_edio_data_in0 pr1_uart0_rts_n pr1_uart0_cts_n pr1_edio_lato_in pr1_edio_sof pr1_mii1_txd3	mcasp_aclkr uart4_txd ehrpwm1A ehrpwm1_tripzone_input ehrpwm1B pr1_edio_data_out1 pr1_edio_data_out0 pr1_edc_latch1_in pr1_edc_latch0_in EMU3 EMU2 ehrpwm0_synco	gpio1[2 gpio0[3 gpio1[1 gpio1[1 f gpio0[5 gpio0[4 gpio0[1 gpio0[3 gpio0[3
9 10 YA, n 11 N 12 N 12 N 13 N 14 N 15 N 15 N 16 A 17 A 18 A 17 A 18 A 19 A 19 YA 19 YA 20 YA YA 21 YA YA 22 X Y N 24 N 25 X R C 27 C 28 N	T17 UART4_RXD U18 GPIO1_28 U17 UART4_TXD U14 EHRPWM1A R13 GPIO1_16 T14 EHRPWM1B A16 I2C1_SCL B16 I2C1_SDA D17 I2C2_SCL D18 I2C2_SDA B17 UART2_TXD A17 UART2_RXD V14 GPIO1_17 D15 UART1_TXD A14 GPIO3_21	gpmc_be1n gpmc_wpn gpmc_a2 gpmc_a0 gpmc_a3 spi0_cs0 spi0_d1 uart1_rtsn uart1_ctsn spi0_d0 spi0_sclk gpmc_a1 uart1_txd	mil2_col mil2_rxerr mil2_txd3 gmil2_txen mil2_txd2 mmc2_sdwp mmc1_sdwp timer5 timer6 uart2_txd uart2_rxd gmil2_rxdv mmc2_sdwp	gpmc_csn6 gpmc_csn5 rgmii2_td3 rmii2_tctl rgmii2_td2 I2C1_SCL I2C1_SDA dcan0_rx dcan0_tx I2C2_SCL I2C2_SDA rgmii2_rxdv	mmc2_dat3 rmii2_rxerr mmc2_dat1 mii2_txen mmc2_dat2 ehrpwm0_synci ehrpwm0_tripzone I2C2_SCL I2C2_SDA ehrpwm0B ehrpwm0A mmc2_dat0	PWR_BUT Reset Out mmc1_sdcd gpmc_dir mmc2_sdcd gpmc_a18 gpmc_a16 gpmc_a19 spi1_cs1 spi1_cs0	pr1_mii1_rxlink pr1_mii1_txen pr1_mii1_txe2 pr1_mii1_txd1 pr1_edio_data_in1 pr1_edio_data_in0 pr1_uart0_rts_n pr1_uart0_cts_n pr1_edio_lato_in pr1_edio_sof pr1_mii1_txd3	mcasp_aclkr uart4_txd ehrpwm1A ehrpwm1_tripzone_input ehrpwm1B pr1_edio_data_out1 pr1_edio_data_out0 pr1_edc_latch1_in pr1_edc_latch0_in EMU3 EMU2 ehrpwm0_synco	gpio1[: gpio0[: gpio1[: gpio1]: f gpio0[: gpio0[: gpio0[: gpio0[: gpio0[:
10 YA n 11 N N 12 N C 13 N A A 16 A A 17 A A 18 A A 19 A YA YA YA YA YA YA YA YA YA	T17 UART4_RXD U18 GPIO1_28 U17 UART4_TXD U14 EHRPWM1A R13 GPIO1_16 T14 EHRPWM1B A16 I2C1_SCL B16 I2C1_SDA D17 I2C2_SCL D18 I2C2_SDA B17 UART2_TXD A17 UART2_RXD V14 GPIO1_17 D15 UART1_TXD A14 GPIO3_21	gpmc_be1n gpmc_wpn gpmc_a2 gpmc_a0 gpmc_a3 spi0_cs0 spi0_d1 uart1_rtsn uart1_ctsn spi0_d0 spi0_sclk gpmc_a1 uart1_txd	mil2_col mil2_rxerr mil2_txd3 gmil2_txen mil2_txd2 mmc2_sdwp mmc1_sdwp timer5 timer6 uart2_txd uart2_rxd gmil2_rxdv mmc2_sdwp	gpmc_csn6 gpmc_csn5 rgmii2_td3 rmii2_tctl rgmii2_td2 I2C1_SCL I2C1_SDA dcan0_rx dcan0_tx I2C2_SCL I2C2_SDA rgmii2_rxdv	mmc2_dat3 rmii2_rxerr mmc2_dat1 mii2_txen mmc2_dat2 ehrpwm0_synci ehrpwm0_tripzone I2C2_SCL I2C2_SDA ehrpwm0B ehrpwm0A mmc2_dat0	Reset Out mmc1_sdcd gpmc_dir mmc2_sdcd gpmc_a18 gpmc_a16 gpmc_a19 spi1_cs1 spi1_cs0	pr1_mii1_rxlink pr1_mii1_txen pr1_mii1_txe2 pr1_mii1_txd1 pr1_edio_data_in1 pr1_edio_data_in0 pr1_uart0_rts_n pr1_uart0_cts_n pr1_edio_lato_in pr1_edio_sof pr1_mii1_txd3	mcasp_aclkr uart4_txd ehrpwm1A ehrpwm1_tripzone_input ehrpwm1B pr1_edio_data_out1 pr1_edio_data_out0 pr1_edc_latch1_in pr1_edc_latch0_in EMU3 EMU2 ehrpwm0_synco	gpio1[: gpio0[: gpio1[: gpio1]: f gpio0[: gpio0[: gpio0[: gpio0[: gpio0[:
YA n 11 N 12 N C 13 N AN A 14 N 15 N CAN A 16 A 17 A 18 A 19 A 19 A 20 YA 21 YA 21 YA 22 N 23 Y 24 N 25 N 26 N 29	T17 UART4_RXD U18 GPIO1_28 U17 UART4_TXD U14 EHRPWM1A R13 GPIO1_16 T14 EHRPWM1B A16 I2C1_SCL B16 I2C1_SDA D17 I2C2_SCL D18 I2C2_SDA B17 UART2_TXD A17 UART2_RXD V14 GPIO1_17 D15 UART1_TXD A14 GPIO3_21	gpmc_be1n gpmc_wpn gpmc_a2 gpmc_a0 gpmc_a3 spi0_cs0 spi0_d1 uart1_rtsn uart1_ctsn spi0_d0 spi0_sclk gpmc_a1 uart1_txd	mil2_col mil2_rxerr mil2_txd3 gmil2_txen mil2_txd2 mmc2_sdwp mmc1_sdwp timer5 timer6 uart2_txd uart2_rxd gmil2_rxdv mmc2_sdwp	gpmc_csn6 gpmc_csn5 rgmii2_td3 rmii2_tctl rgmii2_td2 I2C1_SCL I2C1_SDA dcan0_rx dcan0_tx I2C2_SCL I2C2_SDA rgmii2_rxdv	mmc2_dat3 rmii2_rxerr mmc2_dat1 mii2_txen mmc2_dat2 ehrpwm0_synci ehrpwm0_tripzone I2C2_SCL I2C2_SDA ehrpwm0B ehrpwm0A mmc2_dat0	mmc1_sdcd gpmc_dir mmc2_sdcd gpmc_a18 gpmc_a16 gpmc_a19 spi1_cs1 spi1_cs0	pr1_mii1_rxlink pr1_mii1_txen pr1_mii1_txe2 pr1_mii1_txd1 pr1_edio_data_in1 pr1_edio_data_in0 pr1_uart0_rts_n pr1_uart0_cts_n pr1_edio_lato_in pr1_edio_sof pr1_mii1_txd3	mcasp_aclkr uart4_txd ehrpwm1A ehrpwm1_tripzone_input ehrpwm1B pr1_edio_data_out1 pr1_edio_data_out0 pr1_edc_latch1_in pr1_edc_latch0_in EMU3 EMU2 ehrpwm0_synco	gpio1[gpio0[gpio1[: gpio1[: f gpio0[gpio0[: gpio0[: gpio0[: gpio0[: gpio0[: gpio0[: gpio0[: gpio0[: gpio0[]
N C 12 13 14 15 15 16 16 17 17 18 18 18 18 18 18 18 18 18 18 19 18 19 19 19 19 19 19 19 19 19 19 19 19 19	U18 GPIO1_28 U17 UART4_TXD U14 EHRPWM1A R13 GPIO1_16 T14 EHRPWM1B A16 I2C1_SCL B16 I2C1_SDA D17 I2C2_SCL D18 I2C2_SDA B17 UART2_TXD A17 UART2_RXD V14 GPIO1_17 D15 UART1_TXD A14 GPIO3_21	gpmc_be1n gpmc_wpn gpmc_a2 gpmc_a0 gpmc_a3 spi0_cs0 spi0_d1 uart1_rtsn uart1_ctsn spi0_d0 spi0_sclk gpmc_a1 uart1_txd	mil2_col mil2_rxerr mil2_txd3 gmil2_txen mil2_txd2 mmc2_sdwp mmc1_sdwp timer5 timer6 uart2_txd uart2_rxd gmil2_rxdv mmc2_sdwp	gpmc_csn6 gpmc_csn5 rgmii2_td3 rmii2_tctl rgmii2_td2 I2C1_SCL I2C1_SDA dcan0_rx dcan0_tx I2C2_SCL I2C2_SDA rgmii2_rxdv	mmc2_dat3 rmii2_rxerr mmc2_dat1 mii2_txen mmc2_dat2 ehrpwm0_synci ehrpwm0_tripzone I2C2_SCL I2C2_SDA ehrpwm0B ehrpwm0A mmc2_dat0	gpmc_dir mmc2_sdcd gpmc_a18 gpmc_a16 gpmc_a19 spi1_cs1 spi1_cs0	pr1_mii1_rxlink pr1_mii1_txen pr1_mii1_txe2 pr1_mii1_txd1 pr1_edio_data_in1 pr1_edio_data_in0 pr1_uart0_rts_n pr1_uart0_cts_n pr1_edio_lato_in pr1_edio_sof pr1_mii1_txd3	mcasp_aclkr uart4_txd ehrpwm1A ehrpwm1_tripzone_input ehrpwm1B pr1_edio_data_out1 pr1_edio_data_out0 pr1_edc_latch1_in pr1_edc_latch0_in EMU3 EMU2 ehrpwm0_synco	gpio1[gpio0[gpio1[: gpio1[: f gpio0[gpio0[: gpio0[: gpio0[: gpio0[: gpio0[: gpio0[: gpio0[: gpio0[: gpio0[]
N C 13 14 15 16 17 18 18 18 18 18 18 18 18 18 18 18 18 18	U17	gpmc_wpn gpmc_a2 gpmc_a0 gpmc_a3 spi0_cs0 spi0_d1 uart1_rtsn uart1_ctsn spi0_d0 spi0_sclk gpmc_a1 uart1_txd	mii2_rxerr mii2_txd3 gmii2_txen mii2_txd2 mmc2_sdwp mmc1_sdwp timer5 timer6 uart2_txd uart2_rxd gmii2_rxdv mmc2_sdwp	gpmc_csn5 rgmii2_td3 rmii2_tctl rgmii2_td2 I2C1_SCL I2C1_SDA dcan0_rx dcan0_tx I2C2_SCL I2C2_SDA rgmii2_rxdv	rmii2_rxerr mmc2_dat1 mii2_txen mmc2_dat2 ehrpwm0_synci ehrpwm0_tripzone I2C2_SCL I2C2_SDA ehrpwm0B ehrpwm0A mmc2_dat0	mmc2_sdcd gpmc_a18 gpmc_a16 gpmc_a19 spi1_cs1 spi1_cs0	pr1_mii1_txen pr1_mii1_txd2 pr1_mii1_txd1 pr1_edio_data_in1 pr1_edio_data_in0 pr1_uart0_rts_n pr1_uart0_cts_n pr1_edio_latto_in pr1_edio_sof pr1_mii1_txd3	uart4_txd ehrpwm1A ehrpwm1_tripzone_input ehrpwm1B pr1_edio_data_out1 pr1_edio_data_out0 pr1_edc_latch1_in pr1_edc_latch0_in EMU3 EMU2 ehrpwm0_synco	gpio0[gpio1[: gpio1[: f gpio0[: gpio0[: gpio0[: gpio0[: gpio0[: gpio0[: gpio0[:
N AN A 14 14 15 15 16 16 17 17 17 18 18 18 18 18 18 18 18 18 19 18 18 19 18 19 18 19 19 19 19 19 19 19 19 19 19 19 19 19	U14 EHRPWM1A R13 GPIO1_16 T14 EHRPWM1B A16 I2C1_SCL B16 I2C1_SDA D17 I2C2_SCL D18 I2C2_SDA B17 UART2_TXD A17 UART2_RXD V14 GPIO1_17 D15 UART1_TXD A14 GPIO3_21	gpmc_a2 gpmc_a0 gpmc_a3 spi0_cs0 spi0_d1 uart1_rtsn uart1_ctsn spi0_d0 spi0_sclk gpmc_a1 uart1_txd	mii2_txd3 gmii2_txen mii2_txd2 mmc2_sdwp mmc1_sdwp timer5 timer6 uart2_txd uart2_rxd gmii2_rxdv mmc2_sdwp	rgmii2_td3 rmii2_tctl rgmii2_td2 I2C1_SCL I2C1_SDA dcan0_rx dcan0_tx I2C2_SCL I2C2_SDA rgmii2_rxdv	mmc2_dat1 mii2_txen mmc2_dat2 ehrpwm0_synci ehrpwm0_tripzone 12C2_SCL 12C2_SDA ehrpwm0B ehrpwm0A mmc2_dat0	gpmc_a18 gpmc_a16 gpmc_a19 spi1_cs1 spi1_cs0	pr1_mii1_txd2 pr1_mii_mt1_clk pr1_mii1_txd1 pr1_edio_data_in1 pr1_edio_data_in0 pr1_uart0_rts_n pr1_uart0_cts_n pr1_edio_latch_in pr1_edio_sof pr1_mii1_txd3	ehrpwm1A ehrpwm1_tripzone_input ehrpwm1B pr1_edio_data_out1 pr1_edio_data_out0 pr1_edc_latch1_in pr1_edc_latch0_in EMU3 EMU2 ehrpwm0_synco	gpio1[gpio1[f gpio0] gpio0[gpio0[gpio0[gpio0] gpio0[gpio0]
N CAN A 16 A 17 A 18 A 19 A 19 A 20 YA 21 YA 22 YA 17 A 18 YA 22 YA 19 A 22 YA 19 A 22 YA 19 A 22 YA 19 A 24 A 19 A 1	R13 GPIO1_16 T14 EHRPWM1B A16 I2C1_SCL B16 I2C1_SDA D17 I2C2_SCL D18 I2C2_SDA B17 UART2_TXD A17 UART2_RXD V14 GPIO1_17 D15 UART1_TXD A14 GPIO3_21	gpmc_a0 gpmc_a3 spi0_cs0 spi0_d1 uart1_rtsn uart1_ctsn spi0_d0 spi0_sclk gpmc_a1 uart1_txd	gmii2_txen mii2_txd2 mmc2_sdwp mmc1_sdwp timer5 timer6 uart2_txd uart2_rxd gmii2_rxdv mmc2_sdwp	rmii2_tctl rgmii2_td2 I2C1_SCL I2C1_SDA dcan0_rx dcan0_tx I2C2_SCL I2C2_SDA rgmii2_rxdv	mii2_txen mmc2_dat2 ehrpwm0_synci ehrpwm0_tripzone 12C2_SCL 12C2_SDA ehrpwm0B ehrpwm0A mmc2_dat0	gpmc_a16 gpmc_a19 spi1_cs1 spi1_cs0	pr1_mii_mt1_clk pr1_mii1_txd1 pr1_edio_data_in1 pr1_edio_data_in0 pr1_uart0_rts_n pr1_uart0_cts_n pr1_edio_latch_in pr1_edio_sof pr1_mii1_txd3	ehrpwm1_tripzone_input ehrpwm1B pr1_edio_data_out1 pr1_edio_data_out0 pr1_edc_latch1_in pr1_edc_latch0_in EMU3 EMU2 ehrpwm0_synco	gpio1[f gpio0 gpio0 gpio0[gpio0[gpio0] gpio0]
N CAN A 16 A 17 A 18 B 18 B 18 B 19 B 19 B 19 B 19 B 19 B	T14 EHRPWM1B A16 I2C1_SCL B16 I2C1_SDA D17 I2C2_SCL D18 I2C2_SDA B17 UART2_TXD A17 UART2_RXD V14 GPIO1_17 D15 UART1_TXD A14 GPIO3_21	gpmc_a3 spi0_cs0 spi0_d1 uart1_rtsn uart1_ctsn spi0_d0 spi0_sclk gpmc_a1 uart1_txd	mii2_txd2 mmc2_sdwp mmc1_sdwp timer5 timer6 uart2_txd uart2_rxd gmii2_rxdv mmc2_sdwp	rgmii2_td2 I2C1_SCL I2C1_SDA dcan0_rx dcan0_tx I2C2_SCL I2C2_SDA rgmii2_rxdv	mmc2_dat2 ehrpwm0_synci ehrpwm0_tripzone I2C2_SCL I2C2_SDA ehrpwm0B ehrpwm0A mmc2_dat0	gpmc_a19 spi1_cs1 spi1_cs0	pr1_mii1_txd1 pr1_edio_data_in1 pr1_edio_data_in0 pr1_uart0_rts_n pr1_uart0_tts_n pr1_edio_latch_in pr1_edio_sof pr1_mii1_txd3	ehrpwm1B pr1_edio_data_out1 pr1_edio_data_out0 pr1_edc_latch1_in pr1_edc_latch0_in EMU3 EMU2 ehrpwm0_synco	f gpio0 gpio0 gpio0[gpio0 gpio0
A 17 A 18 18 18 19 17 A 19 17	A16 I2C1_SCL B16 I2C1_SDA D17 I2C2_SCL D18 I2C2_SDA B17 UART2_TXD A17 UART2_RXD V14 GPIO1_17 D15 UART1_TXD A14 GPIO3_21	spi0_cs0 spi0_d1 uart1_rtsn uart1_ctsn spi0_d0 spi0_sclk gpmc_a1 uart1_txd	mmc2_sdwp mmc1_sdwp timer5 timer6 uart2_txd uart2_rxd gmii2_rxdv mmc2_sdwp	I2C1_SCL I2C1_SDA dcan0_rx dcan0_tx I2C2_SCL I2C2_SDA rgmii2_rxdv	ehrpwm0_synci ehrpwm0_tripzone I2C2_SCL I2C2_SDA ehrpwm0B ehrpwm0A mmc2_dat0	spi1_cs1 spi1_cs0	pr1_edio_data_in1 pr1_edio_data_in0 pr1_uart0_rts_n pr1_uart0_cts_n pr1_edio_latch_in pr1_edio_sof pr1_mii1_txd3	pr1_edio_data_out1 pr1_edio_data_out0 pr1_edc_latch1_in pr1_edc_latch0_in EMU3 EMU2 ehrpwm0_synco	gpio0 gpio0 gpio0[gpio0 gpio0
A 18 18 18 18 19 11 19 1	B16 I2C1_SDA D17 I2C2_SCL D18 I2C2_SDA B17 UART2_TXD A17 UART2_RXD V14 GPIO1_17 D15 UART1_TXD A14 GPIO3_21	spi0_d1 uart1_rtsn uart1_ctsn spi0_d0 spi0_sclk gpmc_a1 uart1_txd	mmc1_sdwp timer5 timer6 uart2_txd uart2_rxd gmii2_rxdv mmc2_sdwp	I2C1_SDA dcan0_rx dcan0_tx I2C2_SCL I2C2_SDA rgmii2_rxdv	ehrpwm0_tripzone I2C2_SCL I2C2_SDA ehrpwm0B ehrpwm0A mmc2_dat0	spi1_cs0	pr1_edio_data_in0 pr1_uart0_rts_n pr1_uart0_cts_n pr1_edio_latch_in pr1_edio_sof pr1_mii1_txd3	pr1_edio_data_out1 pr1_edio_data_out0 pr1_edc_latch1_in pr1_edc_latch0_in EMU3 EMU2 ehrpwm0_synco	gpio0 gpio0[gpio0[gpio0 gpio0
A, 19 [19 [19 [19 [19 [19 [19 [19 [19 [19	D17 I2C2_SCL D18 I2C2_SDA B17 UART2_TXD A17 UART2_RXD V14 GPIO1_17 D15 UART1_TXD A14 GPIO3_21	uart1_rtsn uart1_ctsn spi0_d0 spi0_sclk gpmc_a1 uart1_txd	timer5 timer6 uart2_txd uart2_rxd gmii2_rxdv mmc2_sdwp	dcan0_rx dcan0_tx I2C2_SCL I2C2_SDA rgmii2_rxdv	I2C2_SCL I2C2_SDA ehrpwm0B ehrpwm0A mmc2_dat0	spi1_cs0	pr1_uart0_rts_n pr1_uart0_cts_n pr1_edio_latch_in pr1_edio_sof pr1_mii1_txd3	pr1_edc_latch1_in pr1_edc_latch0_in EMU3 EMU2 ehrpwm0_synco	gpio0[gpio0[gpio0 gpio0
A 20 E YA 21 E YA 22 YA 22 YA 23 YA 24 E YA 25 YA 26 E YA 26 E YA 28 YA 29 E YA 20 E Y	D18 I2C2_SDA B17 UART2_TXD A17 UART2_RXD V14 GPIO1_17 D15 UART1_TXD A14 GPIO3_21	uart1_ctsn spi0_d0 spi0_sclk gpmc_a1 uart1_txd	timer6 uart2_txd uart2_rxd gmii2_rxdv mmc2_sdwp	dcan0_rx dcan0_tx I2C2_SCL I2C2_SDA rgmii2_rxdv	I2C2_SDA ehrpwm0B ehrpwm0A mmc2_dat0	spi1_cs0	pr1_uart0_cts_n pr1_edio_latch_in pr1_edio_sof pr1_mii1_txd3	pr1_edc_latch0_in EMU3 EMU2 ehrpwm0_synco	gpio0[gpio0 gpio0
YA 21 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	B17	spi0_d0 spi0_sclk gpmc_a1 uart1_txd	uart2_txd uart2_rxd gmii2_rxdv mmc2_sdwp	I2C2_SCL I2C2_SDA rgmii2_rxdv	ehrpwm0B ehrpwm0A mmc2_dat0		pr1_edio_latch_in pr1_edio_sof pr1_mii1_txd3	EMU3 EMU2 ehrpwm0_synco	gpio0 gpio0
YA) 22 / 23 / 23 / 24 / 25 / 25 / 26 / 27 / 28 / 29 / 29 / 29	A17 UART2_RXD V14 GPIO1_17 D15 UART1_TXD A14 GPIO3_21	spi0_sclk gpmc_a1 uart1_txd	uart2_rxd gmii2_rxdv mmc2_sdwp	I2C2_SDA rgmii2_rxdv	ehrpwm0A mmc2_dat0	gpmc_a17	pr1_edio_sof pr1_mii1_txd3	EMU2 ehrpwm0_synco	gpio0
Y 24 [N 25] Y 26 [N 27] Y 28 [N 29] E	V14 GPIO1_17 D15 UART1_TXD A14 GPIO3_21	gpmc_a1 uart1_txd	gmii2_rxdv mmc2_sdwp	rgmii2_rxdv	mmc2_dat0	gpmc_a17	pr1_mii1_txd3	ehrpwm0_synco	
Y 24 17 18 18 18 18 18 18 18 18 18 18 18 18 18	D15 UART1_TXD A14 GPIO3_21	uart1_txd	mmc2_sdwp			gpmc_a17			gpio1
N 25 7 26 17 27 28 18 N 29 18	A14 GPIO3_21			dcan1_rx	I2C1_SCL		1+0 +'	4 0 5:1:	
Y 26 17 17 17 17 17 17 17 17 17 17 17 17 17		mcasp0_ahclkx	0500				pr1_uart0_txd	pr1_pru0_pru_r31_16	gpio0
R C 27 0	D16 UART1 RYD		eQEP0_strobe	mcasp0_axr3	mcasp1_axr1	EMU4_mux2	pr1_pru0_pru_r30_7	pr1_pru0_pru_r31_7	gpio3
N 29 8	DIO OMINIT_IVAD	uart1_rxd	mmc1_sdwp	dcan1_tx	I2C1_SDA		pr1_uart0_rxd	pr1_pru1_pru_r31_16	gpio0[
N 29	C13 GPIO3_19	mcasp0_fsr	eQEP0B_in	mcasp0_axr3	mcasp1_fsx	EMU2_mux2	pr1_pru0_pru_r30_5	pr1_pru0_pru_r31_5	gpio3
	C12 SPI1_CS0	mcasp0_ahclkr	ehrpwm0_synci	mcasp0_axr2	spi1_cs0	eCAP2_in_PWM2_out	pr1_pru0_pru_r30_3	pr1_pru0_pru_r31_3	gpio3
N 30 F	B13 SPI1_D0	mcasp0_fsx	ehrpwm0B		spi1_d0	mmc1_sdcd_mux1	pr1_pru0_pru_r30_1	pr1_pru0_pru_r31_1	gpio3
50	D12 SPI1_D1	mcasp0_axr0	ehrpwm0_tripzone		spi1_d1	mmc2_sdcd_mux1	pr1_pru0_pru_r30_2	pr1_pru0_pru_r31_2	gpio3
31	A13 SPI1_SCLK	mcasp0_aclkx	ehrpwm0A		spi1_sclk	mmc0_sdcd_mux1	pr1_pru0_pru_r30_0	pr1_pru0_pru_r31_0	gpio3
W 32	VADC					VADC			
33	C8 AIN4					AIN4			
34	AGND					AGND			
W W C 35	A8 AIN6					AIN6			
W W 36	B8 AIN5					AIN5			
37	B7 AIN2					AIN2			
38	A7 AIN3					AIN3			
39	B6 AINO					AIN0			
40	C7 AIN1					AIN1			
N C 41#	D14	xdma_event_intr1		tclkin	clkout2	timer7_mux1	EMU3_mux0		gpio0
72#	D13	mcasp0_axr1	eQEP0_index		Mcasp1_axr0	emu3			gpio3[
	C18	eCAP0_in_PWM0_out	uart3_txd	spi1_cs1	pr1_ecap0_ecap	spi1_sclk	xdma_event_intr2		gpio0[
R 42@	C10	CCALO_III_FWINO_OUL			_capin_apwm_o				
,	B12	Mcasp0_aclkr	eQEP0A_in	Mcaspo_axr2	Mcasp1_aclkx				gpio3[