Curriculum Vitae

Efrat Zusman

Junior Verification Engineer

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Professional Summary

Highly motivated Junior Verification Engineer with hands-on experience in digital design verification gained at NVIDIA. Possessing strong foundational knowledge in VLSI systems, SystemVerilog UVM, and Python scripting, I excel at developing comprehensive test plans, debugging complex digital designs, and contributing to verification methodology improvements. Eager to apply skills in a dynamic ASIC verification environment.

Work Experience

Verification Engineer Student | NVIDIA | Jul 2021 – Jul 2022

- Performed block-level verification of digital modules utilizing industry-standard SystemVerilog and UVM methodologies.
- Developed and implemented comprehensive test benches, functional and code coverage plans, and debugged complex digital design issues.
- Contributed to the development of verification scripts and flows using Python to enhance efficiency and automation.

Design Engineer Student | NVIDIA | Apr 2020 – Jul 2021

- Participated in the design and integration of digital blocks, applying fundamental digital design concepts.
- Executed RTL design, synthesis, and timing analysis, including assisting with low-power design techniques.

Key Projects

RISC-V CPU

- Implemented a single-cycle RISC-V CPU from scratch in Verilog.
- Conducted functional verification and successfully tested the design on an FPGA.

Pipelined CPU Design

- Designed a 5-stage pipelined CPU in Verilog, emphasizing CPU architecture principles.
- Verified functionality using custom test benches and implemented on an FPGA.

Convolutional Neural Network (CNN) Accelerator

- Developed a hardware accelerator for CNN operations in Verilog.
- Optimized the design for throughput and power efficiency, demonstrating advanced digital design skills.

Technical Skills

- **Verification Methodologies:** SystemVerilog, UVM, Object-Oriented Programming (OOP),

Test Bench Development, Coverage Analysis, Debugging

- **Hardware Description Languages (HDLs):** Verilog, VHDL
- **Programming Languages:** Python, C, C++, Java, MATLAB
- **EDA Tools:** Cadence NCSIM, Synopsis VCS, Verdi, SpyGlass, QuestaSim, Vivado
- **Hardware/Concepts:** ASIC Design, RTL Design, Digital Design, CPU Architecture, FPGA, Synthesis, Timing Analysis, Low-Power Design, VLSI Systems
- **Other Tools:** Git, Agile

Education

B.Sc. Electrical Engineering | Technion - Israel Institute of Technology | 2018 - 2022 | GPA: 85.3