Optimized CV

Efrat Zusman
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Professional Summary

Highly motivated and results-driven Junior Verification Engineer with hands-on ASIC verification experience at NVIDIA and a strong academic record (B.Sc. in Electrical and Computer Engineering, 90 GPA). Eager to apply expertise in SystemVerilog, UVM, Python scripting, and industry-standard EDA tools to contribute to MaxLinear's innovative digital design verification challenges. A collaborative team player with a foundational understanding of VLSI systems and digital design methodologies, seeking to grow skills in a dynamic global environment.

Experience

Verification Student | NVIDIA, Israel | August 2023 – Present

- Developed and implemented block-level verification environments for complex digital modules using SystemVerilog and UVM.
- Created comprehensive test plans and wrote targeted/constrained random test cases, analyzing coverage for verification closure.
- Debugged intricate hardware/software interactions, identifying root causes of failures to ensure functional correctness.
- Collaborated effectively with design engineers to define verification strategies and improve design quality.
- Contributed to the automation of verification flows and regression management using Python scripting.

Software Engineer (Volunteer) | Project Lead The Way | February 2022 – August 2023

- Led a team of 4 volunteers in developing educational software, designing user interfaces with React and JavaScript.
- Managed project timelines and deliverables, demonstrating strong organizational and teamwork skills.

Education

B.Sc. in Electrical and Computer Engineering (Software Engineering) | Ben Gurion University of the Negev | 2021 – Present

- Expected Graduation: 2025
- Grade Average: 90
- Relevant Coursework: Digital Systems Design, Computer Architecture, Data Structures & Algorithms, C++ Programming, Operating Systems, OOP, Microprocessors, Discrete Mathematics, Data Bases, Computer Networks.

Key Projects

RISC-V CPU Verification (Academic Project)

- Designed and implemented a complete verification environment for a 5-stage pipelined RISC-V CPU.
- Utilized the UVM framework with SystemVerilog, achieving 100% functional coverage for all instruction sets.
- Developed random instruction generation and directed tests to rigorously validate CPU

functionality.

Network Packet Analyzer (Academic Project)

- Developed a C++-based tool with a Qt GUI for capturing, decoding, filtering, and visualizing network packets.

Technical Skills

- Hardware Description Languages: Verilog, SystemVerilog
- Verification Methodologies: UVM, Functional Coverage, Constrained Random Verification (CRV), Regression Testing
- Programming Languages: Python, C++, JavaScript, React, Java (Basic)
- EDA Tools: Cadence Incisive, Synopsys VCS, Siemens QuestaSim
- Operating Systems: Linux, Windows
- Version Control: Git, SVN
- Concepts: VLSI Systems, Digital Design, Computer Architecture, Object-Oriented Programming (OOP)