

CONFIGURATION DE LA PLL

IP Symbol

Resource

☐ Show disabled ports

Component Name

PLL

Clocking Options

Output Clocks

Port Renaming

MMCM Settings

Summary

Clock Monitor

☐ Enable Clock Monitoring

Primitive

☒ MMCM ☐ PLL

Clocking Features

☒ Frequency Synthesis ☐ Minimize Power ☐ Phase Alignment ☐ Spread Spectrum ☐ Dynamic Reconfig ☐ Dynamic Phase Shift ☐ Safe Clock Startup

Jitter Optimization

☒ Balanced ☐ Minimize Output Jitter ☐ Maximize Input Jitter filtering

Dynamic Reconfig Interface

☒ AXI4Lite ☐ DRP ☐ Phase Duty Cycle Config ☐ Write DRP registers

Input Clock Information

Input Clock	Port Name	Input Frequency(MHz)	Jitter Options	Input Jitter	Source
Primary	clk	125	10.000 - 800.000	0.010	Single ended clock capable pin
Secondary	clk_in2	100.000	75.000 - 150.000	0.010	Single ended clock capable pin

reset

clk_25

clk

locked

IP Symbol

Resource

☐ Show disabled ports

Component Name

PLL

Clocking Options

Output Clocks

Port Renaming

MMCM Settings

Summary

The phase is calculated relative to the active input clock.

Output Clock	Port Name	Output Freq (MHz)		Phase (degrees)		Duty Cycle (%)		Drives
		Requested	Actual	Requested	Actual	Requested	Actual	
<input checked="" type="checkbox"/> clk_out1	clk_25	20	20.00000	0.000	0.000	50.000	50.0	BUFG
<input type="checkbox"/> clk_out2	clk_out2	100.000	N/A	0.000	N/A	50.000	N/A	BUFG
<input type="checkbox"/> clk_out3	clk_out3	100.000	N/A	0.000	N/A	50.000	N/A	BUFG
<input type="checkbox"/> clk_out4	clk_out4	100.000	N/A	0.000	N/A	50.000	N/A	BUFG
<input type="checkbox"/> clk_out5	clk_out5	100.000	N/A	0.000	N/A	50.000	N/A	BUFG
<input type="checkbox"/> clk_out6	clk_out6	100.000	N/A	0.000	N/A	50.000	N/A	BUFG
<input type="checkbox"/> clk_out7	clk_out7	100.000	N/A	0.000	N/A	50.000	N/A	BUFG

☐ USE CLOCK SEQUENCING

Clocking Feedback

Source

☒ Automatic Control On-Chip ☐ Automatic Control Off-Chip ☐ User-Controlled On-Chip ☐ User-Controlled Off-Chip

Signaling

☒ Single-ended ☐ Differential

Output Clock	Sequence Number
clk_out1	1
clk_out2	1
clk_out3	1
clk_out4	1
clk_out5	1
clk_out6	1
clk_out7	1

reset

clk_25

clk

locked

CONFIGURATION DE LA FIFO

FIFO Generator (13.2)

[Documentation](#) [IP Location](#) [Switch to Defaults](#)

Show disabled ports

+ FIFO_WRITE

+ FIFO_READ

clk

srst

Component Namepixel_FIFO

BasicNative PortsStatus FlagsData CountsSummary

Read Mode

☒ Standard FIFO☐ First Word Fall Through

Data Port Parameters

Write Width41,2,3,..,1024

Write Depth1024Actual Write Depth: 1024

Read Width4

Read Depth1024Actual Read Depth: 1024

ECC, Output Register and Power Gating Options

☐ ECCHard ECC☐ Single Bit Error Injection☐ Double Bit Error Injection

☐ ECC Pipeline Reg☐ Dynamic Power Gating

☐ Output RegistersEmbedded Registers

Initialization

☒ Reset Pin

Reset TypeSynchronous Reset

Full Flags Reset Value0

☒ Dout Reset Value0(Hex)

Read Latency : 1