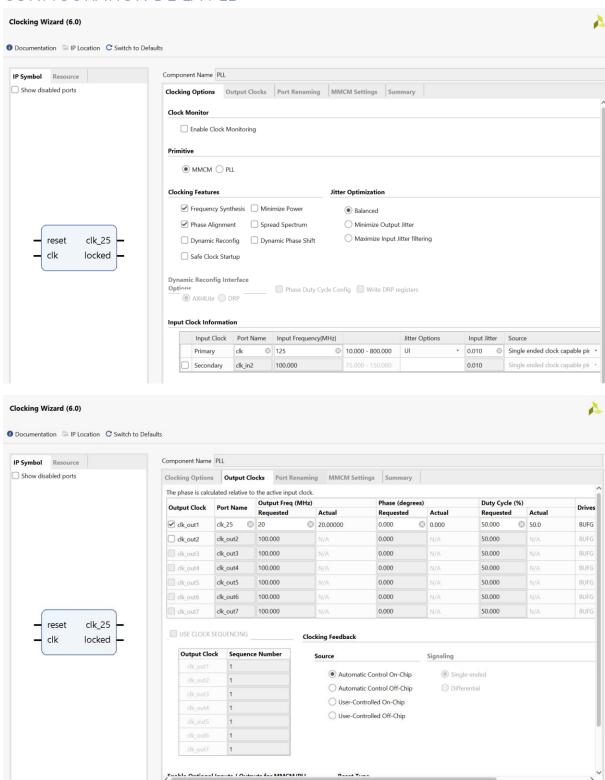
CONFIGURATION DE LA PLL



CONFIGURATION DE LA FIFO

