CS223-1 Digital Design
LAB 1 Preliminary Report

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Lab 01 Preliminary Work

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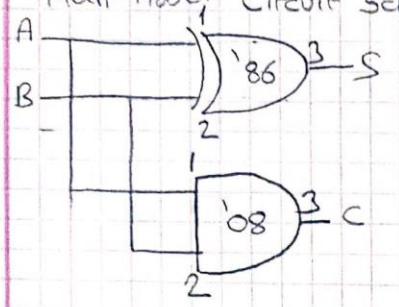
Half Adder Circuit Schematic:



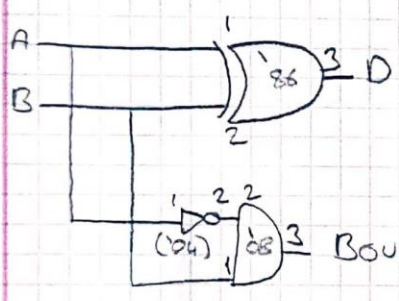
IC List

① One 74LS86 Quad 2-input XOR Gate

② One 74LS08 Quad 2-input AND Gate

*74LS86	*74LS08
GND-7	GND-7
+5V-14	+5V-14

Half Subractor Circuit Schematic:



IC List

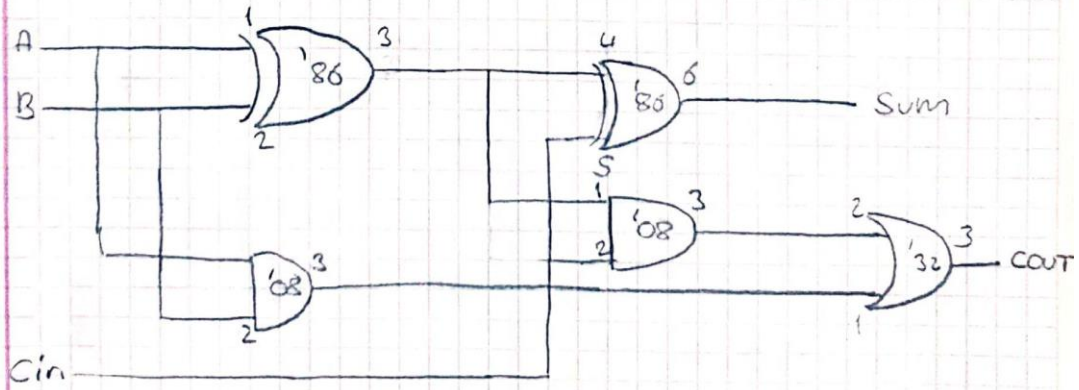
① One 74LS86 Quad 2-input XOR Gate

② One 74LS04 HEXInverting Gate

③ One 74LS08 Quad 2input AND Gate

*74LS86	*74LS04	*74LS08
GND-7	GND-7	GND-7
+5V-14	+5V-14	+5V-14

Full Adder Circuit Schematic:



IC List

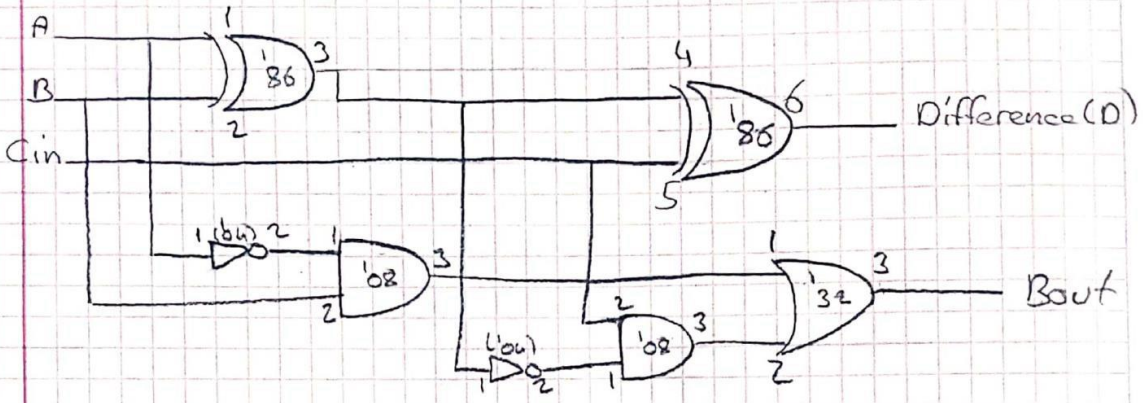
① Two 74LS86 Quad 2-input XOR Gate

② Two 74LS08 Quad 2-input AND Gate

③ One 74LS32 quad 2-input OR Gate

*74LS86	*74LS08	*74LS32
GND-7	GND-7	GND-7
+5V-14	+5V-14	+5V-14

Full Subractor Circuit Schematic:

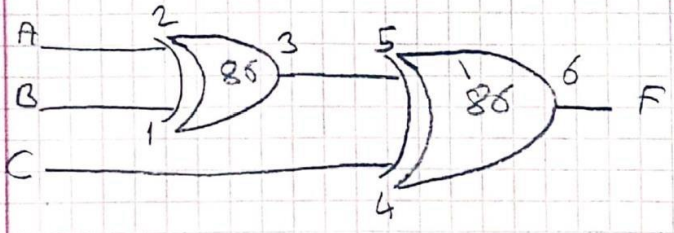


IC List

① Two 74LS86 Quad 2-input XOR Gate
② Two 74LS04 HEX Inverting Gate
③ Two 74LS08 Quad 2-input AND Gate
④ One 74LS32 Quad 2-input OR Gate

*74LS86	*74LS04	*74LS08	*74LS32
GND-7	GND-7	GND-7	GND-7
+5V-14	+5V-14	+5V-14	+5V-14

Three-input XOR Gate with two-input XOR Gates Circuit Schematic: $F = A \oplus B \oplus C$



IC List

① Two 74LS86 Quad 2-input XOR Gate

*74LS86

GND - 7
+5V - 14