CS 223 - Digital Design

Section – 2

Lab – 04

Erdem Ege Eroğlu

21601636

23.04.2020

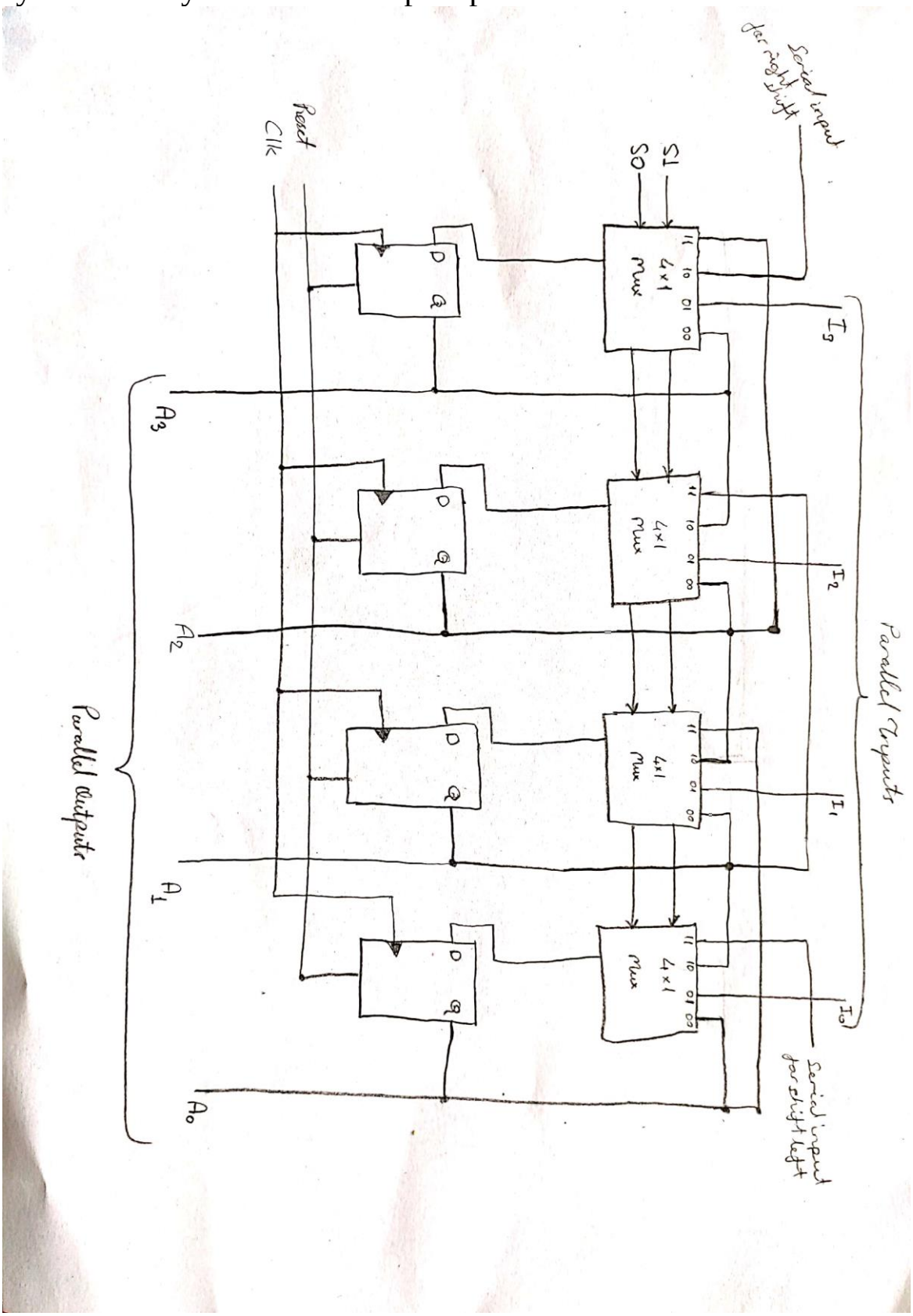
(b) Write a SystemVerilog module for synchronously resettable D flip-flop.

```
module sillyfunction(
   input logic D,clk,sync_reset,
   output logic Q
    );
   always @(posedge clk)
   begin
     if(sync_reset==1'b1)
      Q <= 1'b0;
    else
      Q <= D;
    end
endmodule

// TESCH BENCH
module sillyfunctiontest( );
   logic D, clk, reset;
   logic Q;
   sillyfunction dut(D,clk,reset,Q);
   initial begin
     clk=0;
       forever #1 clk = ~clk;
   end
```

```
    initial begin
     reset=1;
     D <= 0;
     #10;
     reset=0;
     D <= 1;
     #10;
     D <= 0;
     #10;
     D <= 1;
    end
endmodule
```

(c) Draw a circuit schematic (block diagram) for the internal design of the multifunction register by using 4:1 multiplexers and synchronously resettable D flip-flops.



(d) Write a *Structural* SystemVerilog module for the multifunction register you designed in part (c) and a testbench for it.

```
module mux4_1( a, b, c, d, s0, s1, out );
   input logic a,b,c,d;
   input logic s0,s1;
   output logic out;

   always @ (a or b or c or d or s0 or s1)
   begin

      case(s0|s1)
      2'b00 : out <= a;
      2'b01 : out <= b;
      2'b10 : out <= c;
      2'b11 : out <= d;
      endcase
   end
endmodule
module d_ff(
   input logic D,clk,sync_reset,
   output logic Q
   );
   always @(posedge clk)
   begin
     if(sync_reset==1'b1)
```

```
      Q <= 1'b0;
    else
      Q <= D;
    end
endmodule
module multi_register(i0,i1,i2,i3,s0,s1,clk,reset,shiftR,shiftL,a0,a1,a2,a3 );
   input i0,i1,i2,i3,s0,s1,clk,reset,shiftR,shiftL;
   output a0,a1,a2,a3;
   logic t0,t1,t2,t3;

   mux4_1 u1(a3,i3,shiftR,a2,s0,s1,t0);
   d_ff u2(t0,clk,reset,a3);
   mux4_1 u3(a2,i2,a3,a1,s0,s1,t1);
   d_ff u4(t1,clk,reset,a2);
   mux4_1 u5(a1,i1,a2,a0,s0,s1,t2);
   d_ff u6(t2,clk,reset,a1);
   mux4_1 u7(a0,i0,a1,shiftL,s0,s1,t3);
   d_ff u8(t3,clk,reset,a0);

endmodule

module multi_register_testbench( );
   logic i0,i1,i2,i3,s0,s1,clk,reset,shiftR,shiftL;
   logic a0,a1,a2,a3;

   multi_register dut(i0,i1,i2,i3,s0,s1,clk,reset,shiftR,shiftL,a0,a1,a2,a3 );

   initial begin
```

```
    i0 = 1; i1 = 1; i2 = 1; i3=1; s0 =1; s1=1; clk=0; reset=1; shiftR=1; shiftL=1; #10;
    i0 = 1; i1 = 1; i2 = 1; i3=1; s0 =1; s1=0; clk=1; reset=0; shiftR=1; shiftL=1; #10;
    i0 = 0; i1 = 0; i2 = 1; i3=0; s0 =1; s1=0; clk=0; reset=0; shiftR=1; shiftL=0; #10;
    i0 = 0; i1 = 1; i2 = 0; i3=0; s0 =0; s1=1; clk=1; reset=0; shiftR=1; shiftL=0; #10;
    i0 = 1; i1 = 1; i2 = 1; i3=1; s0 =0; s1=1; clk=0; reset=0; shiftR=1; shiftL=1; #10;
    i0 = 1; i1 = 0; i2 = 0; i3=0; s0 =1; s1=1; clk=1; reset=0; shiftR=1; shiftL=1; #10;
    i0 = 0; i1 = 1; i2 = 0; i3=1; s0 =1; s1=1; clk=0; reset=0; shiftR=1; shiftL=0; #10;
    i0 = 0; i1 = 0; i2 = 0; i3=0; s0 =0; s1=0; clk=1; reset=0; shiftR=1; shiftL=1; #10;
    i0 = 1; i1 = 1; i2 = 1; i3=1; s0 =1; s1=1; clk=0; reset=0; shiftR=1; shiftL=0; #10;
    i0 = 0; i1 = 0; i2 = 0; i3=0; s0 =0; s1=0; clk=1; reset=1; shiftR=0; shiftL=1; #10;
    i0 = 1; i1 = 1; i2 = 1; i3=0; s0 =0; s1=0; clk=0; reset=0; shiftR=0; shiftL=1; #10;
    i0 = 1; i1 = 1; i2 = 0; i3=0; s0 =0; s1=0; clk=1; reset=0; shiftR=0; shiftL=1; #10;
    i0 = 1; i1 = 1; i2 = 1; i3=1; s0 =1; s1=1; clk=0; reset=0; shiftR=0; shiftL=1; #10;
    i0 = 1; i1 = 1; i2 = 1; i3=1; s0 =1; s1=0; clk=1; reset=0; shiftR=0; shiftL=1; #10;
    i0 = 0; i1 = 0; i2 = 1; i3=0; s0 =1; s1=0; clk=0; reset=0; shiftR=0; shiftL=1; #10;
    i0 = 0; i1 = 1; i2 = 0; i3=0; s0 =0; s1=1; clk=1; reset=0; shiftR=0; shiftL=1; #10;
    i0 = 1; i1 = 1; i2 = 1; i3=1; s0 =0; s1=0; clk=0; reset=0; shiftR=0; shiftL=1; #10;
    i0 = 1; i1 = 0; i2 = 0; i3=0; s0 =1; s1=1; clk=1; reset=1; shiftR=0; shiftL=0; #10;
    i0 = 0; i1 = 1; i2 = 0; i3=0; s0 =0; s1=1; clk=0; reset=0; shiftR=0; shiftL=0; #10;
    i0 = 0; i1 = 0; i2 = 0; i3=0; s0 =0; s1=0; clk=1; reset=0; shiftR=0; shiftL=0; #10;
    i0 = 1; i1 = 1; i2 = 1; i3=1; s0 =1; s1=1; clk=0; reset=0; shiftR=0; shiftL=0; #10;
    i0 = 0; i1 = 0; i2 = 0; i3=0; s0 =0; s1=0; clk=1; reset=0; shiftR=0; shiftL=0; #10;
    i0 = 1; i1 = 1; i2 = 0; i3=0; s0 =0; s1=0; clk=0; reset=1; shiftR=0; shiftL=0; #10;
    i0 = 1; i1 = 1; i2 = 0; i3=0; s0 =0; s1=0; clk=1; reset=1; shiftR=0; shiftL=0; #10;
    end
endmodule
```