

Digital Design CS223

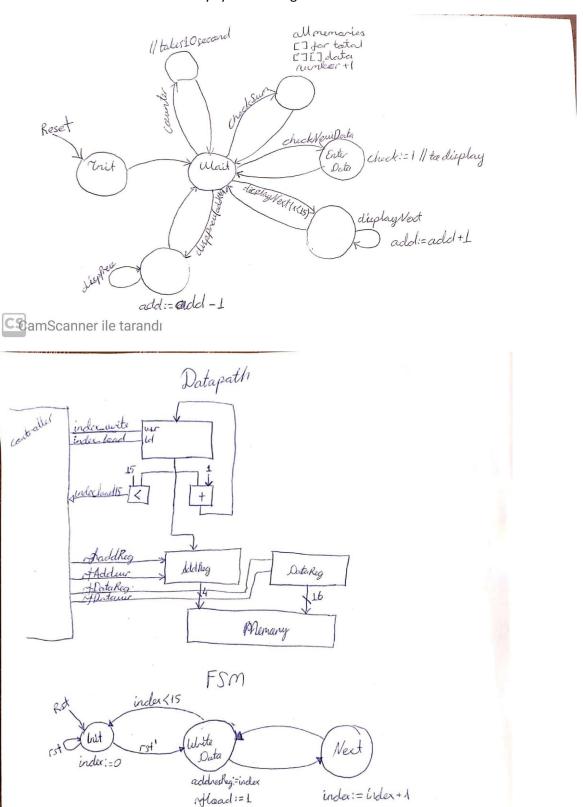
Laboratory Project – Two's complement Checksum for Memory

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We were asked to build a system that is capable of checksum on Basys 3 bord. So, I need to design HLSM and then FSM and eventually system verilog code and xdc file.



MDatareg: 0

amScanner ile tarandı

In order to implement this project, I used arrays for data and their address. My project designed for taking 8 values and put them 4 bit addresses.

When up button clicked, it runs checksum.

Left button is used for checking the previous data and its address.

Right button is used for checking the next data and its index.

Down button is implemented to display 10 second counter.

Center button is designed to add new data and their address to the array.

8-15 switches are used to determine data and 0-3 switches are used to determine data's address.

I benefit from those 2 websites to implement my design:

https://www.fpga4student.com/2017/09/seven-segment-led-display-controller-basys3-fpga.html

 $\underline{https://github.com/raleighlittles/Basys3CountdownClock/blob/master/seven-segment-counter.v}$ 

Also I make use of attachments on unilica, lecture notes, and office hours.