Bilkent University CS224 Spring 2020

Design Report

Lab6

Section 1

Ege Türker – 21702993

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**Part 2) Experiments with Data Cache Parameters**

**Report for 50x50 matrix**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Block Size**  **Cache Size** | 16 words | 32 words | 64 words | 128 words | 256 words |
| 1024 bytes | %88/2507 misses | %88/2504 misses | %69/1970 misses | %35/1009 misses | %19/551 misses |
| 2048 bytes | %57/1621 misses | %88/2504 misses | %69/1970 misses | %35/1001 misses | %19/551 misses |
| 4096 bytes | %34/979 misses | %57/1638 misses | %69/1970 misses | %35/1001 misses | %19/551 misses |
| 8192 bytes | %33/952 misses | %32/927 misses | %27/762 misses | %14/413 misses | %11/306 misses |
| 16384 bytes | %6/164 misses | %3/84 misses | %1/42 misses | %1/21 misses | %0/12 misses |

1. **Direct Mapped Caches**

**Row-major summation table**

**Column-major summation table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Block Size**  **Cache Size** | 16 words | 32 words | 64 words | 128 words | 256 words |
| 1024 bytes | %6/164 misses | %3/83 misses | %1/42 misses | %1/22 misses | %0/12 misses |
| 2048 bytes | %6/164 misses | %3/83 misses | %1/42 misses | %1/22 misses | %0/12 misses |
| 4096 bytes | %6/164 misses | %3/83 misses | %1/42 misses | %1/22 misses | %0/12 misses |
| 8192 bytes | %6/164 misses | %3/83 misses | %1/42 misses | %1/22 misses | %0/12 misses |
| 16384 bytes | %6/164 misses | %3/84 misses | %1/42 misses | %1/22 misses | %0/12 misses |

1. **Fully Associative Caches**

Only significant change was between medium hit rate’s direct mapped vs fully associative cache -LRU. Miss rate increased from %57 to %88. Other 8 values didn’t change noticeably.

1. **N-way Set Associative Caches**

For medium hit rate configuration, LRU block replacement resulted in %88 miss rate regardless the block size. However random block replacement resulted in %58 miss rate, which is considerably better.

For good hit rate configuration, regardless of block replacement or block size, cache memory hit almost all of the data, resulting in %0(12/8565) miss rate.

**Report for 150x150 matrix**

1. **Direct Mapped Caches**

**Row-major summation table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Block Size**  **Cache Size** | 16 words | 32 words | 64 words | 128 words | 256 words |
| 1024 bytes | %98/23929 misses | %98/22504 misses | %98/22502 misses | %98/22501 misses | %58/13237 misses |
| 2048 bytes | %98/22507 misses | %98/22504 misses | %98/22502 misses | %98/22501 misses | %58/13237 misses |
| 4096 bytes | %96/21984 misses | %98/22504 misses | %98/22502 misses | %98/22501 misses | %58/13237 misses |
| 8192 bytes | %82/18684 misses | %90/20590 misses | %98/22502 misses | %98/22501 misses | %58/13237 misses |
| 16384 bytes | %29/6614 misses | %59/13523 misses | %94/21557 misses | %98/22501 misses | %58/13237 misses |

**Column-major summation table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Block Size**  **Cache Size** | 16 words | 32 words | 64 words | 128 words | 256 words |
| 1024 bytes | %6/1414 misses | %3/708 misses | %2/354 misses | %1/177 misses | %0/89 misses |
| 2048 bytes | %6/1414 misses | %3/708 misses | %2/354 misses | %1/177 misses | %0/89 misses |
| 4096 bytes | %6/1414 misses | %3/708 misses | %2/354 misses | %1/177 misses | %0/89 misses |
| 8192 bytes | %6/1414 misses | %3/708 misses | %2/354 misses | %1/177 misses | %0/89 misses |
| 16384 bytes | %6/1414 misses | %3/708 misses | %2/354 misses | %1/177 misses | %0/89 misses |

1. **Fully Associative Caches**
2. **N-way Set Associative Caches**

For medium hit rate configuration, LRU block replacement resulted in the same miss rate regardless the block size. Also random block replacement resulted in %58 miss rate, which is the same as direct mapping.

For good hit rate configuration, miss rate of %29 fell to %8 and %6 for LRU and random respectively. Which is considerably more efficient.