

AXP717 Single Cell NVDC PMU with E-gauge

1 Features

- 3.9V–5.5V Input Operating Range and Support single Cell Battery
- Battery fuel gauge: E-gauge 3.0
- Support TWSI(Two Wire Serial Interface) and RSB(Reduced Serial Bus)
- 3A switch charger, CV accuracy +/-0.5%
- Support USB BC1.2& type C CC input
- High battery discharge efficiency with 30 m Ω
- High integration includes all MOSFETS, current sensing and loop compensation
- Power off current <35uA (BATFET off RTCLDO output on)
- Ultra low power mode(Green mode)support
- 4 DCDC(DCDC4 is not available in charger mode)

DCDC1:0.5~1.54V, IMAX=4A

DCDC2: 0.5~3.4V, IMAX=3A

DCDC3: 0.5~1.84V, IMAX=1.5A

DCDC4: 1.0~3.7V, IMAX=3A

• 14 LDOS

RTCLDO: 1.8V/2.5V/3V/3.3V, 30mA; Support

supplied by backup battery (button battery)

A/B/CLDO: 0.5~3.5V, 0.1V/step

ALDO2, BLDO1/3, CLDO1/3/4: IMAX=500mA

ALDO1/4, BLDO4, CLDO2: IMAX=400mA

ALDO3, BLDO2: IMAX=200mA

CPUSLDO: for CPUs, 0.5~1.4V, IMAX=30mA,

Supplied by DCDC3

- Startup sequence and default voltage of DCDC/LDO setting
- Sleep/Wake up/Fast Wake up support
- Charging LED with breathing function
- Protection

Input Over-Voltage Protection

Battery Thermal Sense Hot/Cold Charge

Suspend

Programmable Safety Timer for Charger

Die Thermal regulation for Charger

Thermal Shutdown

DCDC Over-Voltage/Under-Voltage Protection

LDO Current Limit Protection

2 Applications

Tablets, E-ink , Smart speaker, Vacuum

3 Description

AXP717 is a highly integrated power management IC (PMIC) targeting at single cell Li-battery(Li-ion or Li-polymer) applications that require multi-channel power conversion outputs. It provides an easy and flexible power management solution for multi-core processors to meet the complex and accurate requirements of power control.

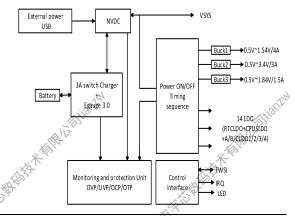
AXP717 supports NVDC switch charge. Besides, it supports 17 channel power outputs which include 3 channels DC-DC and 14 channels LDO. To ensure the security and stability of the system, AXP717 provides multiple channels 14-bit ADC for voltage/temperature monitor and integrates protection circuits such as over-voltage protection (OVP), over-current protection (OCP) and over-temperature protection (OTP). Moreover, AXP717 features a unique E-Gauge™ (Fuel Gauge) system, making power gauge easy and exact.

AXP717 supports TWSI and RSB for system to dynamically adjust output voltages, charge current and configure interrupt condition

Device Information

Part Number	Package	Body Size
AXP717	QFN-52	6mm * 6mm

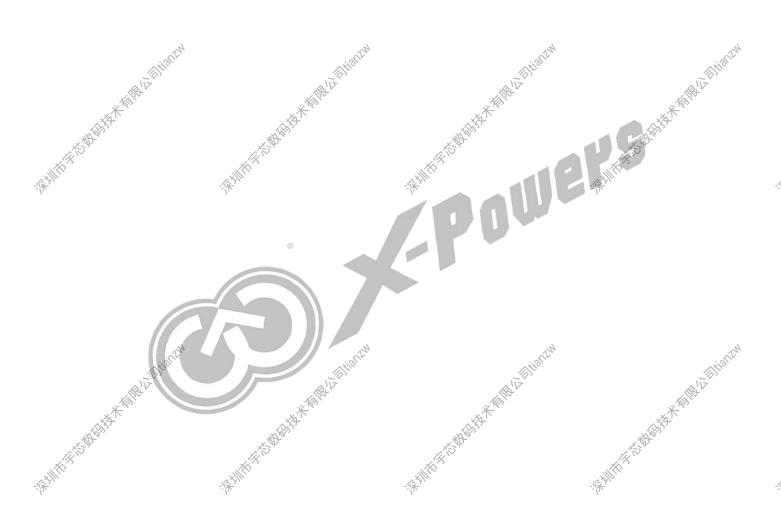
Simplified Application Diagram





Revision History

Revision	Date	Author	Description
1.0	May 13, 2021	AWA 1017	Initial version 🦸
1.1	Jan. 11, 2022	AWA 1017	Update IMAX of ALDO2/ BLDO1/BLDO3/CLDO1/CLDO3/CLDO4



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4 Pin Configuration and Functions

Figure 4-1 Pin Map

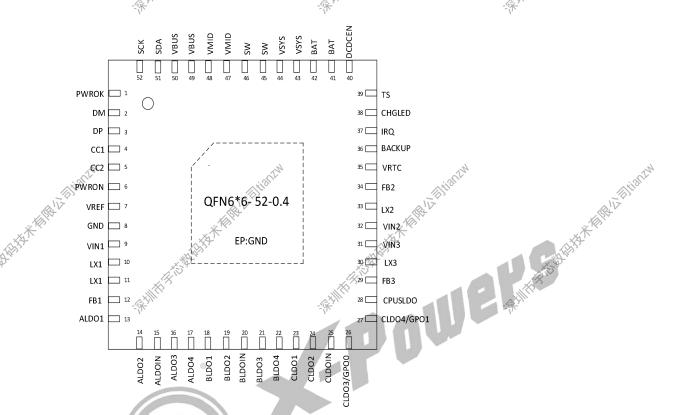


Table 4-1 Pin Description

NO.	Pin Name	I/O ⁽¹⁾	Description
Ť	PWROK	DIO	Power good indication output
2	DM /ii	DIO	BC1.2 detection, connect to DM of USB connector
3	DP AND THE PROPERTY OF THE PRO	DIO	BC1.2 detection, connect to DP of USB connector
4	CC1	DIO	Type-C cc logic, connect to CC1 of USB connector
5	CC2	DIO	Type-C cc logic, connect to CC2 of USB connector
6	PWRON	DIO	Power On-Off key input, Internal pulled up.
7	VREF	Р	Internal reference voltage
8	GND	G	GND for internal analog circuit
9	VIN1	PI	DCDC1 input source
10/11	LX1	PIO	Inductor pin for DCDC1
12	FB1	Al	DCDC1 feedback pin

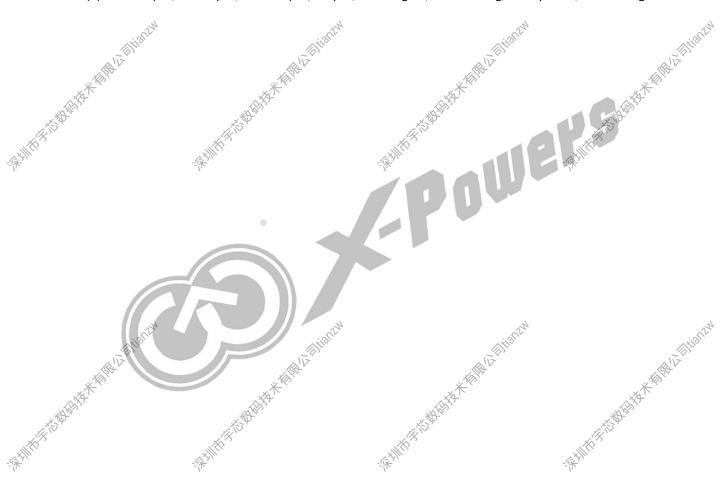


	. 117			
	13	ALDO1	PO	Output pin of ALDO1
×4	14	ALDO2	PO A	Output pin of ALDO2
	15	ALDOIN	PI	ALDO input source, connected to VSYS
	16	ALDO3	РО	Output pin of ALDO3
	17	ALDO4	РО	Output pin of ALDO4
	18	BLDO1	РО	Output pin of BLDO1
	19	BLDO2	РО	Output pin of BLDO2
	20	BLDOIN	PI	BLDO input source, connected to VSYS or DCDC output
	21	BLDO3	РО	Output pin of BLDO3
	22	BLDO4	РО	Output pin of BLDO4
	23	CLDO1	PO	Output pin of CLDO1
	24	CLDO2	PO	Output pin of CLDO2
-`	25	CLDOIN	PI	CLDO input source, connected to VSYS or DCDC output
	26	CLDO3/GPO0	РО	Output pin of CLDO3 or GPO0(open drain)
	27	CLDO4/GPO1	РО	Output pin of CLDO4 or GPO1(push pull)
	28	CPUSLDO	PO _©	Output pin of CPUSLDO
	29	FB3	Al	DCDC3 feedback pin
	30	LX3	PIO	Inductor pin for DCDC3
	31	VIN3	PI	DCDC3 input source
	32	VIN2	PI	DCDC2 input source
	33	LX2	PIO	Inductor pin for DCDC2
	34	FB2	Al	DCDC2 feedback pin
	35	VRTC	PO	RTC power output
	36	BACKUP ************************************	Р	Input pin of backup battery.
				IRQ output.
	37	IRQ	DIO	Connect the IRQ to a logic rail via a resistor. The IRQ pin sends a low level signal to host to report device status and fault.
F				Charge status output to indicate various charger operation.
	38	CHGLED	DO	In no battery mode, CHGLED pin can be the feedback pin of DCDC4
	39	TS	Al	Battery Temperature Sensor Input
H	_18	Highto.		Be connected to external DCDC enable pin. The start-up sequence of
	. 117		,	NV AND
	40	DCDCEN	DO N	DCDCEN is the same as that of CLDO2.



			AN A
BAT		P	Battery connection point
44 VSY	5	P	System connection point
46 SW		P	Switching node connecting to output inductor
48 VMI	D F	Р	VMID Power output
50 VBU	S	Р	VBUS input
SDA		DIO	Data pin for serial interface.
SCK		DI	Clock pin for serial interface.
	144 VSYS 146 SW 148 VMI 50 VBU SDA	14 VSYS 16 SW 18 VMID 50 VBUS SDA	14 VSYS P 16 SW P 18 VMID P 50 VBUS P SDA DIO

(1) O for output, I for input, IO for input/output, D for digital, A for analog, P for power, and G for ground.



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5 Specifications

5.1 Absolute Maximum Ratings (1)

Over operating free-air temperature range (unless otherwise noted)

Table 5-1 Absolute Maximum Ratings

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
VBUS		-0.3	12	V
Others pin (exp VBUS,EP,	Voltage range(with respect to GND)	10.7 th -0.3	7	V
GND	voltage range(with respect to GND)	-0.3	7	V
EP to GND		-0.3	0.3	V
T _a	Operating Temperature Range	-40	85	°C
T _J	Junction Temperature Range	-40	125	°C
Ts	Storage Temperature Range	-40	150	°C
TLEAD	Maximum Soldering Temperature (at leads, 10sec)		300	°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

Table 5-2 ESD Ratings

		VALUE	UNIT
VECD	Human body model(HBM) ⁽¹⁾	±2000	>
VESD TELLIFICATION	Charged device model(CDM) ⁽²⁾	±750	Valida

(1) Reference: ESDA/JEDEC JS-001-2017.

(2) Reference: ESDA/JEDEC JS-002-2018.



5.3 Recommended Operating Conditions

Table 5-3 Recommended Operating Conditions

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
VIN	Input voltage(VBUS)	3.9	5.5	V
VBAT	Battery voltage		4.4	V

5.4 Thermal Information

Table 5-4 Thermal Information

Thermal Met	ric(1)	A CONTRACTOR OF THE PARTY OF TH	VALUE	UNIT		
θ_{JA}	Junction-to-ambient thermal resistance	X THE	24.43			
θ _{ЈВ}	Junction to-board thermal resistance					
θ _{JC}	Junction-to-case(top) thermal resistance	DOM.	11.91			

⁽¹⁾Thermal metrics are calculated refer to JEDEC document JESD51

5.5 Electrical Characteristics

Table 5-5 Electrical Characteristics

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	UNIT
QUIESCENT	CURRENTS	A STATE OF THE STA			Thu,	
	Fillips.	no VBUS, BATFET Disabled, with only RTCLDO on;	-17	35		uA
Іват	Battery discharge current in different cases.	no VBUS, BATFET enabled, PMIC is power on, all DCDC/ ALDO/ BLDO/ CLDO is off		300		uA
		no VBUS, PMIC is work in green mode.		100		uA
VBUS/BAT	POWER UP	L. Bright				Takin
VVBUS_OP	VBUS operating range	X A STATE OF THE S	3.9		5.5	V
V _{VBUS_UVLOZ}	VBUS under voltage threshold	× ##	3.5	***	3.9	V



×××××××××××××××××××××××××××××××××××××××	VSLEEPZ	Sleep mode rising threshold(VBUS-VBAT)	CAN THE PARTY OF T		150	N. KA. K. K.	mV
V _{VBUS} OV		VBUS over-voltage rising threshold	SEE	-41	7 / ⁽⁴⁾		,
	V _{BAT_UVLO}	VBAT under voltage threshold		- (1	2.3	\	/
	V _{BAT_UVLOZ}	VBAT under voltage hysteresis			2.45	\	,
	V _{OFF}	VSYS power off threshold		2.6		3.3	/
	V _{OFF_HYST}	VSYS power off hysteresis			0.3	\	7
	V _{SYS_OVP}	VSYS over-voltage turn-off		5.8		6	/
	THERMAL REC	GULATION AND THERMAL SHU	rdown all tight of the control of th	•		•	Thian?
XX	Тѕнит	Thermal Shutdown Rising Temperature	Temperature rising	4	145	A A A A A A A A A A A A A A A A A A A	C
	T _{SHUT_HYS}	Thermal Shutdown Hysteresis	Temperature falling		20 4	o	°C
	Battery Charg	er	100W				
	V _{BATREG_} RANGE	Typical Charge voltage range	V _{BATREG} =4.0/4.1/4.2/4.35/4.4V	4		4.4	V
	V _{BATREG}	Charge voltage resolution accuracy	V _{BAT} = 4.2V, TJ = 25 ℃	-0.50%		0.50%	
	Ichg_reg_range	Typical Fast charge current regulation range	, italih	0		3072	mA
××	Ichia_reg_acc	Fast charge current regulation accuracy	V _{BAT} = 3.2V or 3.8V, I _{CHG} =1024mA,T _J = 25°C	-20%		20%	[V]
, ,	V _{BATLOWV}	Battery low voltage threshold	Fast charge to precharge		3	S	V
	I _{PRECHG_RANGE}	Precharge current range	A A A A A A A A A A A A A A A A A A A	64	William,	1024	mA
	I _{PRECHG_ACC}	Precharge current accuracy	V_{BAT} =2.5V, I_{PRECHG} = 256mA, T_J = 25 $^{\circ}$ C	-30%		30%	
	I _{TERM_RANGE}	Termination current range		64		1024	mA
	V _{TRICHG}	Battery trickle charge threshold	V _{BAT} falling		2		V
	ITRICHG HIRRITIN	Battery trickle charge current	V _{BAT} < 2 V		10		mA _N
××	Vяєсна	Recharge Threshold below VBATREG	V _{BAT} falling		100	A FAIR	mV



(^)						-(A)
FSW	PWM Switching Frequency	ZINIV.		1.5	× KINS	MHz
POWER-PAT	H MANAGEMENT	ALE PARTY AND THE PARTY AND TH				
Vena	Typical system regulation	Isys = 0A, V _{BAT} > VS _{YS_MIN} , BATFET Disabled	-%	V _{BAT} + 50mV		V
V_{SYS}	voltage	Isys= 0A, V _{BAT} <v<sub>SYS_MIN, BATFET Disabled</v<sub>		V _{SYS_MIN} + 150mV		V
V _{SYS MIN}		$V_{BAT} < V_{SYS_MIN}$, SYS_MIN = 3.5V , ISYS= 0A		3.65		V
Input Voltag	e / Current Regulation		•			
VINDPM_RANGE	Typical Input voltage regulation range	MRUZ dia ti	3.88		5.08	K Wild
VINDPM_ACC	Input voltage regulation accuracy	V _{INDPM} =4.36V	-3%		3%	
I _{INDPM_RANGE}	Input current regulation range	· 读别用	100	Hillip	3250	mA
I _{INDPM_ACC}	Input current regulation accuracy	I _{INLIM} =500mA	450		550	mA
BAT OVER-VOLTAGE						
V _{BATOVP}	Battery over-voltage threshold	$V_{ extsf{BAT}}$ rising, as percentage of $V_{ extsf{BAT}_ extrm{REG}}$		104%* V _{BAT_REG}		V
V _{BATOVP} hyst	Battery over-voltage hysteresis	V _{BAT} falling, as percentage of V _{BAT_REG}		2%		IN THE
DCDC				4	NA KAN	
DCDC1/2/3	A STORY	A THE STATE OF THE		(A)(S)	×	
V _{IN}	Input Voltage	Frill Co	2.6		5.5	V
UVP				85%		
OVP				130%		
FSW	Switching Frequency			3		MHz
Accuracy	Output Assuras:	Accuracy, PWM mode, V _{OUT} <1V	-30		30	mV
Accuracy	Output Accuracy	Accuracy, PWM mode, V _{OUT} >1V	-3.00%		3.00%	
DCDC1	ALIVA HILD	ALIVA HIS			R	IN ANTO
Vouт	Output Voltage	Output Range	0.5		1.54	V
	(X)	(X)		- 1	/γ),	



THE IV		Step Size, V _{OUT} =0.5V~1.2V		10	- 1	mV		
*	A STATE OF THE STA	Step Size, V _{OUT} =1.22V~1.54V		20	XAT	mV		
l _{out}	Output Load Current	A A A A A A A A A A A A A A A A A A A		4 /4		А		
DCDC2	- Frith	- Frank	-51	X XIII.	•	•		
		Output Range	0.5		3.4	V		
.,	0. 10. 11/6/15 00	Step Size, V _{OUT} =0.5V~1.2V		10		mV		
V _{OUT}	Output Voltage	Step Size, V _{OUT} =1.22V~1.54V		20		mV		
		Step Size, V _{OUT} =1.6~3.4V		100		mV		
lout giant	Output Load Current	Tin Distal	124	3		A		
DCDC3		A STATE OF THE STA				SIV.		
*	K. K.	Output Range	0.5		1.84	V		
V _{OUT}	Output Voltage	Step Size, Vour=0.5V~1.2V	1	10		mV		
		Step Size, V _{OUT} =1.22V~1.84V	1	20		mV		
I _{OUT}	Output Load Current	1000		1.5		А		
DCDC4	©							
V_OUT	Output Voltage	Output Range	1.0		3.7	V		
V001	Output Voltage	Step Size		100		mV		
lout Conti	Output Load Current		ZN	3		A		
LDO	A LIVE							
RTCLDO					~XXX			
V_OUT	Output Voltage		1.8		3.3	V		
VOUT	Output voltage accuracy	· Frinth .	-10%		+10%			
l _{оит}	Output Load Current			30		mA		
CPUSLDO								
VIN	Input Voltage	Input is DCDC3	0.8		1.84	V		
		Output Range	0.5		1.4	V		
-13	n e	Step size	13	50		mV		
Vout Children	Output Voltage	Accuracy, VIN=0.8V~1.84V	-30		30	mV		
KAN	THE THE PERSON NAMED IN COLUMN TO TH	V _{OUT} <1V, I _{load} =10mA			X.T	-		
-		Accuracy,VIN=0.8V~1.84V,	-3%		3%			
	~ \\	~ \\		~ \\				



	Will Co	Will's				A	(P)
	Z MIRLIV	z Killa IV	V _{OUT} >1V, I _{load} =10mA			- A	V
DY.	I _{оит}	Output Load Current	AND THE PERSON NAMED IN COLUMN TO TH		30	XA	mA
	ILIM	Current Limit			300		mA
	ALDO/BLDO/	CLDO 1~4	\$ ⁷		Ž.		
	VIN	Input Voltage		2.6		5.5	V
	V_{Drop}	Dropout	V _{OUT} =3.3V		200		mV
			Output Range	0.5		3.5	V
			Step size		100		mV
×	Killiku Tilitatu	* Killikatu	Accuracy, ALDOIN=2.6V~5.5V, V _{OUT} <1V, I _{load} =10mA only for ALDO3/4	-20		20	mV ijari
	Vouт	Output Voltage	Accuracy, ALDOIN=2.6V~5.5V, V _{OUT} >1V, l _{load} =10mA only for ALDO3/4	-2%	Military 13 Marie	2%	
		•	Accuracy, xLDOIN=2.6V~5.5V, V _{OUT} <1V, I _{load} =10mA	-30		30	mV
			Accuracy,xLDOIN=2.6V~5.5V, V _{OUT} >1V, I _{load} =10mA	-3%		3%	
			ALDO2, BLDO1/3, CLDO1/3/4		500		mA
	IOUT THERETON	Output Load Current	ALDO1/4, BLDO4, CLDO2		400		mA;
	E Hille IV	A STATE OF THE STA	ALDO3, BLDO2		200	A TOP STATE OF THE PERSON NAMED IN COLUMN TO THE PERSON NAMED IN C	mA
ŊŸ.	ILIM	Current Limit			500	X	mA
	BOOST	A STATE OF THE STA	A Print of the Pri		WA KIND		
	V _{BST_REG_RANGE}	Typical Boost mode regulation voltage range	\$\sqrt{\partial}\$	4.55	, Y	5.51	V
	V _{BST_REG_STEP}	Typical Boost Mode Regulation voltage step			64		mV
	V _{BST_REG_ACC}	Boost mode regulation voltage accuracy	V _{BST} =5.126V	-3%		3%	
	V _{BST_BAT_L} OWV	Battery voltage exiting boost mode	BAT falling	2.4	2.6	3.0	Validari
Į, X	T _{BST}	Boost mode output current range	A SHIPPE TO SHIP		× 100	1,5	Α
		200			200		

15



X-Powers	

	Willion.	illo.	William .			A	(P/T)
X	VBST_OVP	Boost mode over-voltage threshold	Rising threshold	5.8		6.4	>
V _{BST_OVP_HYS} threshold PWM Swi		Boost mode over-voltage threshold hysteresis	Falling threshold	100	訓問其為	300	mV
		PWM Switching Frequency, and digital clock	Oscillator frequency	-77	1.5		MHz
-	TWI&IO						
-	TWI INTERFA	CE (SCL, SDA)					
,	VIH	Input high threshold level, SCL and SDA	Pull-up rail 1.8V	1.3			V
,	VIL	Input low threshold level	Pull-up rail 1.8V			0.8	Applica
VOL Output low threshold level		Output low threshold level	Sink Current = 5mA, sink current	41		0.4	V
		Characteristics (IRQ/PWRON/P	WROK)		HH		
,	VIH Input high threshold level		* A A W	1.3			V
,	VIL	Input low threshold level	/ PU			0.8	V

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6 Detail Description

6.1 Overview

AXP717 is a highly integrated power management IC(PMIC) targeting at single cell Li-battery (Li-ion or Li-polymer) applications that require multi-channel power conversion outputs. It provides an easy and flexible power management solution for multi-core processors to meet the complex and accurate requirements of power control.

AXP717 supports 3A switch charger. Besides, it supports 17 channel power outputs which include 3 channel DCDCs and 14 channel LDOs. To ensure the security and stability of the system, AXP717 provides multiple channels 14-bit ADC for voltage/temperature monitor and integrates protection circuits such as over-voltage protection(OVP), over-current protection(OCP) and over-temperature protection(OTP). Moreover, AXP717 features a unique E-Gauge™ (Fuel Gauge) system, making power gauge easy and exact.

AXP717 supports TWSI and RSB for system to dynamically adjust output voltages, charge current and configure interrupt condition.

AXP717 is available in 6mm x 6mm 52-pin QFN package.

Miller Bakkling Karak Bakkling Karak

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Function Block Diagram 6.2 BLOCK DIAGRAM RBFET VBUS Gate BUCK CONTROL Control SYS CHGLED 📮 SYS CHARGER LED LOGIC charger control Ŧ BAT BAT Φ ВАТ EGauge TS Register & OTP V IN 1 Walled To High The ВG VREF ON OFF SEQUENCE LX2 FB2 V IN 3 SYSTEM CONTROL LX3 SDA FB3 CPUSLDO Control ALDO IN ALDO A LD O 2 ALDO3 ALDO4 BLD 03 BL.DO C LD O IN DΡ C LD O 1 C LD O 2 D M C LD O 3, \dot{G} P O O C LD O 4/G P O 1 RTCLDOI VRTC **₼** B A C K U P



6.3 Serial Interface Communication

AXP717 supports TWSI protocol and performs as a TWSI slave device with default address 0x68/0x69(8 bits). When AXP717 powers on, SCK/SDA pin of TWSI will be pulled up to IO Power and then Host can adjust and monitor AXP717 with rich feedback information.

Besides, AXP717 supports RSB for Allwinner platform with address 0x01D1 or 0x0273 by customer.

Note: "Host" here refers to processor.

6.4 Power Path

VBUS as the charger input, connecting to VSYS pin through a switch charger, provides power to system and charges battery through BATFET. Charge current can be adjusted automatically according to the feedback current which is detected with an internal resistor.

The device provides automatic power path selection for system from VBUS, battery or both. When battery voltage is above VSYS, BATFET is turned on and AXP717 enters supplement mode. If an adapter is not inserted, system current is provided only by battery. At this time, BATFET is at fully on state.

6.5 Power On/Off and reset

6.5.1 Power on reset(POR)

AXP717 is powered from the higher voltage between VBUS and BAT. When VBUS voltage(V_{VBUS}) is higher than V_{VBUS_UVLOZ} or BAT voltage(V_{BAT}) is higher than V_{BAT_UVLOZ} , the device is POR, and all registers are reset to the default value.

6.5.2 Power up from BAT

If only battery is present and V_{BAT} is higher than UVLO threshold, BATFET(connecting battery to system) is off by default and need to be turned on by pressing the PWRON key or inserting an adapter. Serial Interface communication is not available before power on.

6.5.3 Power up from VBUS

When VBUS is inserted and V_{VBUS} is higher than V_{VBUS_UVLOZ} , the VBUS insertion IRQ is sent and the register bit reg49H[7] is set to 1 to indicate VBUS is inserted. Then PMU detects the input source whether it is good or not. If VBUS is good, the RBFET is open and VSYS is working.

6.5.3.1 Good source condition

PMU needs to check the power capability of the input source. Only when the input source meets the following requirements can it start the buck converter.

a. VBUS voltage is lower than V_{ACOV}(typical 7V)



b VBUS voltage is higher than V_{VBUSUVLO} when pulling I_{BADBUS}(typical 25mA)

Once the input source meets the requirements above, the register bit reg00H[5](VBUS_GD) is set to 1 to indicate the input source is good.

6.5.3.2 Set input voltage limit(VINDPM)

AXP717 supports wide range of input voltage(3.9V \sim 5.5V). V_{INDPM} can be set through reg16H[3:0]. The range of V_{INDPM} is from 3.88V to 5.08V and the step is 80mV.

When VBUS voltage reaches V_{INDPM} , the charge current will decrease automatically until the current is zero. If I_{SYS} is over the input power supply capability, VSYS will drop. If V_{BAT} is above VSYS, PMU will enter the supplement mode.

6.5.3.3 Set input current limit(IINDPM)

AXP717 supports input current limit to avoid adaptor overload. I_{INDPM} can be set through reg17H[5:0]. The range of I_{INDPM} is from 100mA to 3.25A and the step is 100mA.

When input current reaches I_{NDPM} , the charge current will decrease automatically until the current is zero. If I_{SYS} is over the input power supply capability, VSYS will drop. If V_{BAT} is above VSYS, PMU will enter the supplement mode.

6.5.4 System power on/off management

PMU has power off and power on status. When at off state, all voltage outputs are turned off except RTCLDO.

6.5.4.1 Power on-off Key (POK)

EN/PWRON pin can be customized as PWRON pin or EN pin. The default is PWRON pin. The Power on-off Key (POK) can be connected between PWRON pin and GND of AXP717. AXP717 can automatically identify the four status (Long-press, Short-press, Negative edge, Positive edge) and then correspond respectively.

6.5.4.2 Power on

1. When EN/PWRON pin is customized as PWRON pin, power on sources include:

- (1). POK. AXP717 can be powered on by pressing and holding POK for a period of time that longer than "ONLEVEL".
- (2). VBUS low to high. The function can be configured by customization.
- (3). VBAT low to high. The function can be configured by customization.
- (4). IRQ Low level. IRQ pin is low level for more than 16ms, AXP717 will be powered on. The function can be configured by customization.
- (5). Battery is charged to normal(VBAT>3.3V and is charging). The function can be configured by customization.
- 2.When EN/PWRON pin is customized as EN pin, AXP717 can be powered on by EN pin from low to high(0.6V).



After power on, DCDCs and LDOs will be soft booted in preset timing sequence. If IRQ low level is the power on source, AXP717 can be configured for fast power on by REG2FH [5], and the DCDCs/LDOs start sequence can be configured by REG2FH.

6.5.4.3 Power Off

- 1. When EN/PWRON pin is customized as PWRON pin, power off sources include:
- (1). POK. AXP717 can be powered off by pressing and holding POK for a period of time that longer than "OFFLEVEL". The function can be configured by REG22H [1] and REG22H [0] decides whether the PMU auto turns on or not when it shuts down after OFFLEVEL POK.
- (2). Write "1" to REG27H [0].
- (3). VSYSGOOD high to low. When VSYS<VOFF or VBUS>7V, AXP717 will be powered off. The default of VOFF is 2.6V which can be configured by REG24H [6:4].
- (4) The output voltage of DCDC is 15% lower than the setting value. The function can be configured by REG23H [3:0].
- (5). The output voltage of DCDC is much larger than their setting(130%). The function can be configured by REG23H [4].
- (6). Die temperature is over the warning level2(145℃). The function can be configured by REG22H [2].
- (7). LDO over current(typical 500mA for ALDO/BLDO/CLDO). The function can be configured by REG22H [3].

VBUS or VBAT

VSYS

<Ims

Internal POWER EN

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Figure 6-1 System power up and shut down sequence

6.5.4.4 Sleep and wakeup

When the running system needs to enter Sleep mode, maybe one or several power outputs should be disabled or changed to other voltage. Wakeup can be initiated by the following sources:

1. Software wakeup (REG25H [1] is set to 1)

PWROK

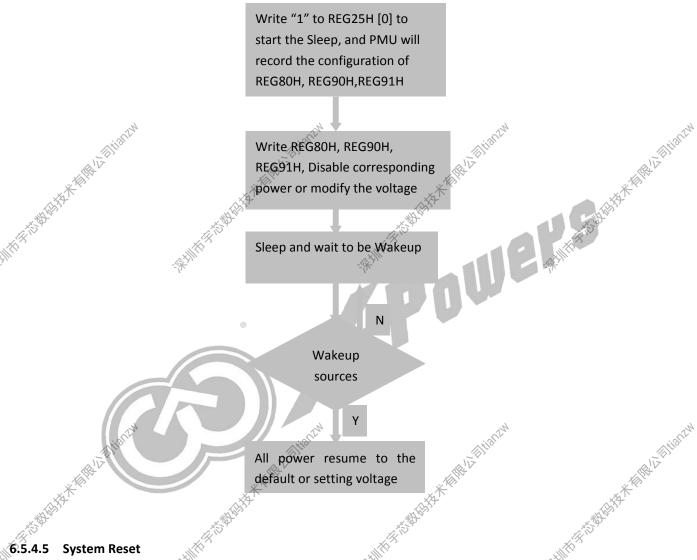
2. IRQ pin wakeup (REG 25H [5] =1 and IRQ pin is low level for more than 4ms)



These sources will make all the power outputs resume to the default voltage or the setting voltage, which is configured by REG25H[2], and all shutdown powers will resume by the startup sequence.

The control process under sleep and wakeup modes is as below.

Figure 6-2 Sleep and Wakeup



System reset means the related registers will be reset when PMU is power off. The system will power off and then power on. VRTC will not be off during restart. Restart can be initiated by the following sources:

(1). PWROK drive low.

The PWROK pin can be used as the reset signal of application system. During AXP717 startup, PWROK outputs low level, which will be pulled up to startup the system after output voltage reaches the regulated value.

When application system works normally, if the PWROK pin is driven low for 128us, the PMU will be restarted. The function can be configured by REG27H [3].

- (2). Write "1" to REG27H [1] to restart the PMU.
- (3). Watchdog timeout. The function can be configured by REG19H [0] and REG1AH [5:4].



6.5.4.6 POR

Power on reset means all the registers will be reset when PMU is power down. All voltage outputs are turned off including RTCLDO and VREF. Pressing and holding POK for more than 16s can force POR.

6.5.4.7 Fast power on/Fast Wake up

If fast power on and fast wake up function is enabled by REG3FH, all voltage outputs are turned on based on the timing sequence set by REG28H~REG2BH. The startup interval is 0.4ms.

6.5.4.8 Green mode

AXP717 has ultra-low power mode(Green mode) to support the application such as Elink.

There are two ways to let AXP717 enter to green mode.

- (1) Disable all the power rails, and only enable CPUSLDO/DCDC3/BLDO2 then set REG1DH[0] to enable green mode. To exit green mode, host needs to clear REG1D[0].
- (2) Set REG25H[0] to enter sleep mode, and configure the power rails on/off in sleep mode. Then set REG2AH[1] and REG25H[6] to let the device enter to both sleep and green mode automatically. In this way, there is a delay time before sleep and green mode taking effect.

In Green mode, the quiescent power consumption is much lower than normal status. However, the voltage output accuracy and capacity is worse. The following table shows the capacity and accuracy of the voltage output.

Table 6-1 The capacity and accuracy in Green mode

Output Path	Accuracy	Load Capacity(Max)
CPUSLDO	+-5%	10mA
RTCLDO: BELL	+-5%,87,77	5mA
DCDE3	€ 15%	10mA
BLDO2	+-5%	5mA

6.6 Multi-Power Outputs

The following table has listed the multi-power outputs and their functions of AXP717.

Table 6-2 Multi-Power Outputs

Output Path	Туре	Default Voltage	Startup Sequence	Application Suggestion	Load Capacity
DCDC1	виск	a kianzw		CPU skienth	4000mA
DCDC2	ВИСК	Customization	Customization	VSYS/VDD-USB/DRAM	3000mA
DCDC3	ВИСК	A A A A A A A A A A A A A A A A A A A	×	VCC-DRAM	1500mA



	//\\\\					//*
××.	DEDC4	BUCK	NA THE TOTAL PROPERTY OF THE PARTY OF THE PA		Not available in charger mode	3000mA
	ALDO1	LDO			AVDD-CSI	400mA
	ALDO2	LDO			IO/AF-CSI VCC-PE	200mA
	ALDO3	LDO		./v.	VCC-USB/VCC-PL	200mA
	ALDO4	LDO			AVCC/PLL/DRAM	400mA
	BLDO1	LDO			WIFI	400mA
	BLDO2	LDO			LPDDR	200mA
	BLDO3	LDO			MOTOR	200mA
	BLDO4	LDO	* The land of the second		DVDD-CSI	400mA
	CLDO1	LDO	A LIV		MIPI/LVDS.etc	400mA
X	ČLDO2	LDO	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	,X	ČTP	400mA
	CLDO3	LDO X			VCC-SENSOR/NAND.etc	400mA
	CLDO4	LDO			LCD	400mA
	VCPUS	LDO		71	CPUs	30mA
	VRTC	LDO	(Q)	Always on	RTC	30mA

AXP717 includes 4 synchronous step-down DCDCs and 14 LDOs. The work frequency of DC-DC 1/2/3 is 3MHz and DCDC4 is 1.5MHz. External small inductors and capacitors can be connected. In addition, DCDC 1/2/3 can be set in fixed PWM mode or auto mode (automatically switchable according to the load). See register REG81H.

DCDC1/2/3 has DVM enable option. In DVM mode, when there is a change in the output voltage, DCDC will change to the new targeted value step by step. It supports two kinds of DVM slope: 1 step/15.625us and 1step/31.250us. The slope can be chosen by REG82H [0].

AXP717 can configure the default voltage, the startup sequence and other control of all power output.

Startup sequence: The startup sequence has eight levels from 0 to 7. When the sequence is 0, it means the output is booted at the first step. When the sequence code is 1, it means the output is booted at the second step. When the sequence is 7, it means the output is not booted.

Default voltage setting: The default voltage of each channel can be set to each step within the output range.

6.7 Multi-Function Pin Description

EN/PWRON



EN/PWRON can be customized as EN pin or PWRON PIN. When it is configured as PWRON pin, a Power on-off Key (POK) can be connected between PWRON pin and GND. When it is configured as EN pin, it can be used for dial switch.

CLDO4/GPO1

It can be customized as LDO or GPO. When customized as GPO, it is push-pull. GPO1 output is configured by REG1CH [4].

CLDO3/GPO0

It can be customized as LDO or GPO. When customized as GPO, it is open-drain. GPO0 output is configured by REG1CH [0].

6.8 Charger

6.8.1 Characteristics

- Range of input voltage:3.9V~5.5V, switch charger, supports single cell Li-battery
- Pre-charge current settable (I_{PRE-CHG}, reg61H [3:0]), default:128mA, range: 0mA~960mA, step:64mA
- Fast charge current settable (I_{CHG}, reg62H[5:0]), default:1024mA, range: 0mA~3072mA, step:64mA
- Target charge voltage settable (V_{REG}, reg64H[2:0]), default:4.2V, range: 4.0v/4.1v/4.2v/4.35v/4.4v/5.0v
- Termination current settable(Iterm,reg63H[3:0]),default:384mA,range:64~1024,step:64mA
- Accuracy of target voltage:±0.5%(testing ambient temperature:25 °C, target voltage:4.2V)

6.8.2 Charging condition

- VBUS is present and available, V_{VBUS}>V_{BAT}+V_{SLEEPZ}
- Input source detection finishes (reg00H [5] =1)
- Charging is enabled (reg19H [1] =1)
- Die temperature is lower than T_{SHUT}
- When TS pin is used to detect battery temperature, battery temperature is within the chargeable range
- V_{BAT} is lower than V_{BAT_OVP} and Battery is present
- No charger safety timer fault

6.8.3 Charging process

When PMU meets all charging conditions, it can complete the whole charging process without the participation of Host. The charging status can be known from the register bits reg01H[2:0]. The default values of charging parameters are shown as following. Host can modify registers to optimize the values through TWSI.



Table 6-3 Default values of charging parameters

Parameter	Default value
Charging voltage	4.2\(\vec{v}^2\)
Charging current	1.024A
Pre-charging current	128mA
Termination current	320mA
Temperature profile	Cold/hot
Safety timer in fast-charge	12hours

6.8.3.1 Pre-charge

When V_{BAT} is lower than $V_{BATLOWV}(3V)$, the charger is under pre-charge mode where charging current is limited to a value of $I_{PRE-CHG}$. Safety time in pre-charge is 50 minutes. If pre-charge process times out, PMU will stop charging and send a corresponding IRQ to Host. The function of safety timer can be disabled through reg67H [2].

6.8.3.2 Constant current charge

Once V_{BAT} is higher than $V_{BATLOWV}$ and lower than V_{REG} , the charger is under constant current charge mode. It will charge with constant current I_{CHG} .

6.8.3.3 Constant voltage charge

When V_{BAT} reaches target voltage (V_{REG}), the charger enters constant voltage charge mode. In this stage, the charger keeps the output voltage constant and step down charging current gradually, in order to fully charge battery.

When V_{BAT} is above V_{RECHG} and the charging current reduces under termination current (I_{TERM}), AXP717 reports charger done, stops charging (charger enable bit is still 1) and turns off BATFET. Meanwhile, IRQ is sent to Host.

When AXP717 is in regulation of input current(IDPM), input voltage(VDPM) or temperature(thermal regulation), the function of charging termination configured through reg63 H[4] is temporarily disabled and the speed of safety timer slows down. Whether to set safety timer during DPM or thermal regulation depends on reg67H [7].

6.8.3.4 Re-charge

After charge done, if V_{BAT} falls below V_{RECHG} , PMU will automatically enable charger without reinserting adapter.

No matter whether V_{BAT} is above V_{RECHG} or not, the charger is enabled when an adapter is inserted.

6.8.3.5 Battery detection

As long as an AC adapter is present and usable, battery detection will be enabled to detect whether battery is connected. Battery detection function is enabled by default and can be disabled through reg68H [0]. If the function is disabled, PMU considers that battery is always present. The detection result is saved in reg00H [3]



6.8.4 Charging protection

6.8.4.1 charger safety timer

Once starting pre-charge mode, PMU will enable timer1. If PMU cannot enter constant current charge mode from pre-charge within 50 minutes, PMU will enter battery safe mode and send IRQ to indicate the battery may be damaged.

When the charger enters into constant current charge mode, PMU will enable timer2. If PMU cannot finish the whole charge cycle within 12 hours, PMU will enter battery safe mode and send IRQ to indicate the battery may be damaged.

6.8.4.2 Battery safe mode

In battery safe mode, the charger always charges with 10mA current. PMU can quit battery safe mode with one of the following methods:

- V_{BAT}>V_{RECHG}
- Adapter removal
- Charger enable bit (reg18H [1]) is reset to 1
- Safety timer1 enable bit(reg67H [2]) or safety timer2 enable bit(reg67H [6]) is reset to 1

6.8.4.3 PMU die temperature protection

AXP717 has built-in temperature protection function through ADC to monitor internal temperature.

Under charging mode, the temperature point of thermal regulation can be set through reg65H[1:0]. When die temperature rises up to the setting point, the charging current will be decreased to decrease heat. When thermal regulation works, actual charge current is lower than the setting value and thermal regulation status(reg00H [1]) is set to 1. If die temperature rises up to T_{SHUT} (145°C), IRQ is sent and PMU is power off. When die temperature falls below hysteretic threshold (120°C), PMU is not power on automatically.

6.8.4.4 Battery temperature protection

AXP717 can monitor battery temperature, when TS pin is used to detect battery temperature and parallel with charger(reg50H[4]=0). The battery temperature sensitive resistor is connected between TS pin and GND. The suggestion resistance should be 10Kohm at 25°C ambient temperature. Through TS pin, PMU outputs constant current which can set through reg50H [1:0] to adapt different resistance. When the resistance is 10Kohm, the current should be set to 50uA. The enable bit of TS current source is configured through reg50H [3:2]. When current passes through the temperature sensitive resistor, PMU gets a detected voltage and calculates its value through ADC circuit. Take for example, TH11-3H103F temperature sensitive resistor of Mitsubishi Company. Using 50uA current source, the relationship among temperature, equivalent resistance, detected voltage and ADC data is as following.

Table 6-4 Relationship among temperature, equivalent resistance, detected voltage and ADC data

	Temperature	equivalent resistance	detected voltage	ADC DATA	THE IT	
ı	- Wilbertature	equita en l'esistante	actested rollage	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	-14	



)	-20°C	63.00Kohm	3.150V	189Ch
	-15°C	50.15Hohm	2.508	1398h
	-10°C	40.26Kohm	2.013V	FBAh
	-5°C	32.55Kohm	1.628V	CB8h
	0°C	26.49Kohm	1.325V	A5Ah
	5°C	21.68Kohm	1.084V	878h
	10°C	17.78Kohm	0.889V	6F2h
X	15°C	14.63Kohm	0.732V	5B8h
	20°C	12.07Kohm	0.604V	4B8h
	25°C	10.00Kohm	0.500V	3E8h
	30°C	8.320Kohm	0.416V	340h
	35°C	6.954Kohm	0.348V	2B8h
	40°C	5.839Kohm	0.292V	248h
X	45°C	4.924Kohm	0.246V	1ECh
	50°C	4.171Kohm	0.209V	1A2h
	55°C	3.549Kohm	0.177V	162h
	60°C	3.032Kohm	0.152V	130h

During battery charging process, if TS pin voltage is lower than VHTF-CHG or higher than VLTF-CHG (VHTF-CHG and VLTF-CHG can be set through reg55H and reg54H. The default value of VLTF-CHG is set around 0°C and VHTF-CHG around 45°C), which indicates battery temperature is too high or too low, then the charger is paused and IRQ is sent to notify Host. When battery temperature is back to the normal range, the charger will recovery automatically.



During battery discharging mode, if TS pin voltage is lower than VHTF-WORK or higher than VLTF-WORK (VHTF-WORK and VLTF-WORK can be set through reg57H and reg56H. The default value of VLTF-WORK is set around -10°C and VHTF-WORK around 55°C), which indicates battery temperature is too high or too low, then the boost is paused and IRQ is sent to notify Host. When battery temperature is back to the normal range, the boost will recovery automatically.

High temperature protection threshold hysteresis for VHTF-CHG and VHTF-WORK can be set through reg53H. Low temperature protection threshold hysteresis for VLTF-CHG and VLTF-WORK can be set through reg52H. The range of temperature detection can be expanded by adding more resistors.

Some battery may have no temperature sensitive resistor. Under this situation, TS pin can be pulled down to GND with a 10Kohm resistor externally or set as external input of ADC through register.

6.8.5 Charging indication

CHGLED pin uses open-drain/push-pull output method. It is internally pulled up to LDO. Its output drive capability is above 10mA. Detail function control is shown as the following table.

Table 6-5 CHGLED function

- F	Hi-Z	No charging(conditions are not met or battery		
		charged)		
		Charger internal abnormal alarm(including timer		
REG70H [2:0] = 000	25% 1Hz pull low/Hi-Z	out、die temperature over temperature、battery		
(Type A CHGLED)	jump	temperature out of charging range)		
Open Drain	25% 4Hz pull low/Hi-Z	Input source or battery over voltage		
Ristry	jump	Michael Michael Votes Votedge		
THE ID	Pull low	Charging Charging		
**	Hi-Z	No VBUS, and power supply by battery		
	25% 1Hz pull low/Hi-Z	Charging		
乘捌秸	jump	\$		
REG70H [2:0] = 001	25% 4Hz pull low/Hi-Z	Alarm, including input source or battery over		
(Type B CHGLED)	jump	voltage, battery temperature out of charging		
Open Drain		range, timer out ,die temperature over		
		temperature		
	Pull low	No battery or charge finished, and power supply		
	T un low	by VBUS		
REG70H[2:0]=010	Breathing LED controlled by charger(Breathing LED on in charging status)			
Breathing LED	Breathing LED controlled by charge (breathing LED on in charging status)			
REG70H[2:0]=011	Breathing LED controlled by	REG70H[6]		



7/^>	·/^>		7/\S
Breathing LED	A THE VIEW	ZAR IV	This later
REG70H[2:0]=110	- Children and a second		.xtelytan
CFG CHGLED	the output status is co	ontrolled by REG70H[5:4]	A CONTRACTOR OF THE PROPERTY O

Note: 1. LED is on when CHGLED pin is low. 2. Breathing LED display behavior controlled by REG72H~REG78H

6.8.6 DCDC4 mode

AXP717 works in charger mode by default to support single-cell application. If it is used in multi-cell or non-battery application, the charger module can be used as DCDC4. In DCDC4 mode, charger module works as a common buck, and CHGLED pin works as the feedback of DCDC4. In order to support multi-cell gauge, gauge will measure the battery voltage by external resistor divider from DP pin instead of VBAT pin. In DCDC4 mode, charging indication/battery detection/USB typeC/BC1.2 function is not available. User can select DCDC4 or charger mode by customization.

6.9 BOOST

AXP717 supports boost converter operation to deliver battery power to VBUS or VMID. The maximum output current support 1.5A. If below conditions are valid, boost will be enabled,

- (1)V_{BAT} is higher than boost mode disable threshold(REG1EH[3:2], default is 2.6V)
- (2) VBUS voltage is lower than VBAT+V_{SLEEP}
- (3)Boost mode is enabled(REG19H[4]=1)
- (4) Voltage at TS pin is within working range (REG56H/57H)

6.10 BATFET

BATFET connects system and battery. The on-resistance is low to 30mohm. The minimum system voltage is set by REG15H[2:0]. When battery voltage is below minimum system voltage, the BATFET operates in linear mode and system voltage is regulated at minimum system voltage setting. As the battery voltage rises, the BATFET can turn to full on.

If only battery is present, BATFET is off when the system is power off and can be turned on again by pressing the PWRON key or inserting an adapter.

6.11 RBFET

RBFET connects VMID and VBUS. The on-resistance is low to 100mOhm. It supports input and output current limit function. In boost mode, the output current limit value of RBFET is set through reg1EH [1:0].



6.12 ADC

AXP717 has a low speed 14 Bits SAR ADC for measuring BAT voltage, VBUS voltage, VSYS voltage, TS voltage and die temperature.

Table 6-6 ADC channel

No.	Channel function	000Н	001H	002Н	•••	FFFH
0	BAT voltage	0mV	1mV	2mV		8.192V
1	VBUS voltage	0mV	1mV	2mV		8.192V
2	VSYS voltage	0mV	1mV	∑2mV		8.192V
3	TS voltage	0mV	0.5mV	1mV		4.096V
4	die temperature	0mV	0.1mV	2mV	THE PARTY OF THE P	0.8192V

Note: ADC data is 14 bits. In order to get the complete data, TWSI must read the high 6 bits firstly and then the low 8 bits.

6.13 E-Gauge

The Fuel Gauge system is able to export information about battery capacity percentage (regA4H) and Battery Voltage (regC4H, regC5H). The Fuel Gauge can be enabled or disabled through reg0BH[2]. The Battery low warning level can be set through reg1BH, and IRQ will be sent out to alert the platform when the battery capacity percentage is lower than the warning level set through reg1BH.

Once a default battery is selected for a particular design, it is highly recommended to program the battery module to achieve better Fuel Gauge accuracy. Once the battery module data are available, user can write these information to battery parameter (REGA1H) after brom is enabled on each boot. Additionally, the Fuel Gauge system is capable to learn the battery characteristic automatically.

6.14 IRQ/BACKUP

6.14.1 IRQ

AXP717 has an IRQ pin which is used to indicate whether there interrupt events occur.

PMU Interrupt Controller monitors the trigger events such as over voltage, over current, PWRON pin signal, over temperature and so on. When the events occur and their IRQ enabled bits are set to 1 (Refer to registers



reg40H~44H), corresponding IRQ status will be set to 1 (Refer to registers reg48H~4CH), and IRQ pin will be pulled down. When Host detects triggered IRQ signal, Host will scan through the IRQ Status registers and respond accordingly. Meanwhile, Host will reset the IRQ status by writing "1" to status bit.

6.14.2 BACKUP

AXP717 has a backup pin which is used to connect backup battery. It is the source of RTCLDO when PMU has only backup battery.

When PMU is power on, the backup battery also can be charged by configuring reg19H[3]. The charger is working under linear mode with 100uA charge current and the termination voltage can be configured by reg6AH in range from 2.6V to 3.3V (default 2.9V).

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6.15 Register

6.15.1 Register List

	- **	
Address	Description	R/W
0X00	PMU status1	R
0X01	PMU status2	R
0X05	BC_detect	R
0X06	ILIM type	R
0X08	PMU fault	RW1C
OXOB V	module enable control1	RW
0X10	DCDC/LDO Discharge_configure	RW
0X14	Tshut configure	RW
0X15	Minimum system voltage control	RW
0X16	Input voltage limit control	RW
0X17	Input current limit control	RW
0X18	Reset the fuel gauge	RW
0X19	module enable control2	RW
0X1A	Watch dog control	RW
OX1B	Low Battery warning threshold setting	RW (S)
0X1¢	GPO configure	RW
0X1D	Low power configure	RW
0X1E	Boost configure	RW
0X20	PWRON status	R
0X21	PWROFF status	R
0X22	PWROFF_EN	RW
0X23	PWROFF of DCDC OVP/UVP control	RW
0X24	VSYS voltage for PWROFF threshold setting	RW
0X25	Sleep and Wakeup configure	RW
0X26	IRQLEVEL/OFFLEVEL/ONLEVEL setting	RW
0X27	Soft Poweroff configure	RW
0X28	Auto Sleep map0	RW
		V 707



0x29 Auto Sleep map1 RW 0x2A Auto Sleep map2 RW 0x2B Fast pwron setting 0 RW 0x2C Fast pwron setting 1 RW 0x2D Fast pwron setting 2 RW 0x2E Fast pwron setting 3 RW 0x2F Fast pwron setting 4 RW 0x3E TWI/RSB configure RW 0x40-0x44 IRQ Enable RW 0x52 TS_HYSL2H setting RW 0x50 TS pin configure RW 0x50 TS_HYSL2H setting RW 0x53 TS_HYSL2H setting RW 0x54 VLTF_CHG setting RW 0x55 VHTF_CHG setting RW 0x55 VHTF_WORK setting RW 0x59 VHTF_WORK setting RW 0x59 JIETA standard snable control RW 0x59 JIETA standard setting RW 0x61 Iprechg charger setting RW 0x62 ICC charger setting RW 0x63 Iterm charger setting and control RW <tr< th=""><th>Address</th><th>Description Property Control of the Control of the</th><th>R/W</th></tr<>	Address	Description Property Control of the	R/W
Content of the cont	0X29	Auto Sleep map1	RW
OX2C Fast pwron setting 1 RW OX2D Fast pwron setting 2 RW OX2E Fast pwron setting 3 RW OX2F Fast pwron setting 4 RW OX3E TWI/RSB configure RW OX3E TWI/RSB configure RW OX40-0X44 IRQ Enable RW OX50 TS pin configure RW OX50 TS pin configure RW OX52 TS HYSL2H setting RW OX52 TS HYSL2H setting RW OX53 TS_HYSL2L setting RW OX54 VLTF_CHG setting RW OX55 VHTF_CHG setting RW OX55 VHTF_CHG setting RW OX56 JIETA standard tenable control RW OX59 OX58 JIETA standard setting RW OX60 IDrechg charger setting RW OX61 IDrechg charger setting RW OX62 ICC charger setting RW OX63 Iterm charger setting RW OX64 CV charger voltage setting RW OX65 Thermal regulation threshold setting RW OX66 Battery detection control RW OX68 Battery detection control RW OX69 IR compensation RW OX60 CHGLED setting and control RW	0X2A	Auto Sleep map2	RW
OX2D Fast pwron setting 2 OX2E Fast pwron setting 3 OX2F Fast pwron setting 4 OX3E TWI/RSB configure OX40-0X44 IRQ Enable OX40-0X44 IRQ Enable OX50 TS pin configure OX50 TS pin configure OX51 TS HYSL2L setting OX52 TS HYSL2L setting OX53 TS HYSH2L setting OX54 VLTF_CHG setting OX55 VHTF_CHG setting OX56 VLTF_WORK setting OX57 VHTF_WORK setting OX58 JIETA standard setting OX60 IPECharger setting OX61 IPECharger setting OX62 ICC charger setting OX63 Iterm charger setting OX64 CV charger voltage setting OX65 Thermal regulation threshold setting OX66 Battery detection control OX68 Battery detection control OX68 Battery detection control OX69 IR compensation OX60 CHGLED setting and control OX60 RW OX60 DCC Configure(0/1/2) OX70 CHGLED setting and control OX60 RW OX70 CHGLED setting and control	0X2B	Fast pwron setting 0	RW
OX2E Fast pwron setting 3 RW OX2F Fast pwron setting 4 RW OX3E TWI/RSB configure RW OX40-0X44 IRQ Enable RW OX40-0X44 IRQ Status RW OX50 TS pin configure RW OX52 TS_HYSL2H setting RW OX52 TS_HYSL2H setting RW OX53 TS_HYSH2L setting RW OX54 VLTF_CHG setting RW OX55 VHTF_CHG setting RW OX55 VHTF_CHG setting RW OX56 JLTF_WORK setting RW OX57 VHTF_WORK setting RW OX58 JIETA standard Enable control RW OX60 ICC charger setting RW OX61 Iprechg charger setting RW OX62 ICC charger setting RW OX63 Iterm charger setting RW OX64 CV charger voltage setting RW OX65 Thermal regulation threshold setting RW OX66 Battery detection control RW OX68 Battery detection control RW OX69 IR compensation RW OX60 CHGLED setting and control RW OX60 CHGLED setting RW OX70 CHGLED setting and control RW	0X2C	Fast pwron setting 1	RW
OX2F Fast pwron setting 4 RW OX3E TWI/RSB configure RW OX40-0X44 IRQ Enable RW OX48-0X4C IRQ Status RW OX50 TS pin configure RW OX52 TS_HYSL2H setting RW OX53 TS_HYSH2L setting RW OX54 VLTF_CHG setting RW OX55 VHTF_CHG setting RW OX56 VLTF_WORK setting RW OX57 VHTF_WORK setting RW OX58 JIETA standard Enable control RW OX59-0XSB JIETA standard setting RW OX60 Item charger setting RW OX61 Iprechg charger setting RW OX62 ICC charger setting RW OX63 Item charger setting RW OX64 CV charger voltage setting RW OX65 Thermal regulation threshold setting RW OX66 Battery detection control RW OX67 Charger timeout setting and control RW OX68 Battery detection control RW OX69 IR compensation RW OX60 CHGLED setting and control RW OX60 CHGLED setting and control RW	0X2D	Fast pwron setting 2	RW
OX3E TWI/RSB configure RW OX40-0X44 IRQ Enable RW OX48-0X4C IRQ Status RW OX50 TS pin configure RW OX52 TS_HYSL2H setting RW OX53 TS_HYSH2L setting RW OX54 VLTF_CHG setting RW OX55 VHTF_CHG setting RW OX56 VHTF_WORK setting RW OX57 VHTF WORK setting RW OX57 VHTF WORK setting RW OX58 JIETA standard Enable control RW OX59-0X5B JIETA standard setting RW OX61 Iprechg charger setting RW OX62 ICC charger setting RW OX63 Iterm charger setting RW OX64 CV charger voltage setting RW OX65 Thermal regulation threshold setting RW OX66 Battery detection control RW OX67 Charger timeout setting and control RW OX68 Battery detection control RW OX69 IR compensation RW OX60 CHGLED setting and control RW OX60 DCDC ConfigureO/1/2 RW	0X2E	Fast pwron setting 3	RW
OX40-OX44 IRQ Enable OX48-OX4C IRQ Status OX50 TS pin configure OX52 TS_HYSL2H setting OX53 YS_HYSH2L setting OX54 VLTF_CHG setting OX55 VHTF_CHG setting OX56 VLTF_WORK setting OX57 VHTF_WORK setting OX58 JIETA standard Enable control OX58 JIETA standard setting OX61 Iprechg charger setting OX62 ICC charger setting OX63 Iterm charger setting OX64 CV charger voltage setting OX65 Thermal regulation threshold setting OX65 Thermal regulation threshold setting OX67 Charger timeout setting and control OX68 Battery detection control OX68 Battery detection control OX69 IR compensation OX60 CHGLED setting and control OX60 RW OX70 CHGLED setting and control OX60 RW OX70 CHGLED setting and control OX60 RW OX70 CHGLED setting and control	0X2F	Fast pwron setting 4	RW
0X48-0X4C IRQ Status 0X50 TS pin configure 0X52 TS_HYSL2H setting 0X53 TS_HYSH2L setting 0X54 VLTF_CHG setting 0X55 VHTF_CHG setting 0X56 VLTF_WORK setting 0X57 VHTF_WORK setting 0X58 JIETA standard Enable control 0X59-0X5B JIETA standard setting 0X61 Iprechg charger setting 0X62 ICC charger setting 0X63 Iterm charger setting 0X64 CV charger voltage setting 0X65 Thermal regulation threshold setting 0X67 Charger timeout setting and control 0X68 Battery detection control 0X69 IR compensation 0X60 RW 0X70 CHGLED setting and control RW 0X70 CHGLED setting and control RW 0X80-0X82 DCDC configure0/1/2 RW	0X3E	TWI/RSB configure	RW
OX50 TS pin configure OX52 TS_HYSL2H setting OX53 FS_HYSH2L setting OX54 VLTF_CHG setting OX55 VHTF_CHG setting OX55 VHTF_CHG setting OX56 VLTF_WORK setting OX57 VHTF_WORK setting OX58 JIETA standard Enable control OX59-0X5B JIETA standard setting OX61 Iprechg charger setting OX62 ICC charger setting OX63 Iterm charger setting OX64 CV charger voltage setting OX65 Thermal regulation threshold setting OX67 Charger timeout setting and control OX68 Battery detection control OX69 IR compensation OX60 CHGLED setting and control OX60 RW OX61 RW OX62 RW OX65 RW OX65 RW OX67 Charger timeout setting and control OX68 Battery detection control OX69 RW OX69 RC CHGLED setting and control OX60 CHGLED setting and control OX60 RW OX70 CHGLED setting and control OX80-0X82 DCDC configureO/1/2	0X40-0X44	IRQ Enable	RW Silias
OX52 TS_HYSL2H setting RW OX53 TS_HYSL2E setting RW OX54 VLTF_CHG setting RW OX55 VHTF_CHG setting RW OX56 VLTF_WORK setting RW OX57 VHTF_WORK setting RW OX58 JIETA standard Enable control RW OX59-OX5B JIETA standard setting RW OX61 Iprechg charger setting RW OX62 ICC charger setting RW OX63 Iterm charger setting RW OX64 CV charger voltage setting RW OX65 Thermal regulation threshold setting RW OX67 Charger timeout setting and control RW OX68 Battery detection control RW OX69 IR compensation RW OX60 CHGLED setting and control RW OX61 RW OX62 RW OX63 RW OX64 RW OX65 RW OX65 RW OX67 Charger timeout setting and control RW OX68 Battery detection control RW OX69 IR compensation RW OX69 RW OX60 CHGLED setting and control RW OX60 CHGLED setting and control RW OX80-OX82 DCDC configureO/1/2 RW	0X48-0X4C	IRQ Status	RW
OX53 TS_HYSH2L setting RW OX54 VLTF_CHG setting RW OX55 VHTF_CHG setting RW OX56 VLTF_WORK setting RW OX57 VHTF_WORK setting RW OX58 JIETA standard Enable control RW OX69 OX61 Iprechg charger setting RW OX62 ICC charger setting RW OX63 Iterm charger setting and control RW OX64 CV charger voltage setting RW OX65 Thermal regulation threshold setting RW OX67 Charger timeout setting and control RW OX68 Battery detection control RW OX69 IR compensation RW OX60 OX60 CHGLED setting and control RW OX80-0X82 DCDC configureO/1/2 RW OX80-0X82 DCDC configureO/1/2 RW	0X50	TS pin configure	RW
OX54 VLTF_CHG setting RW OX55 VHTF_CHG setting RW OX56 VLTF_WORK setting RW OX57 VHTF_WORK setting RW OX58 JIETA standard Enable control RW OX59-0X5B JIETA standard setting RW OX61 Iprechg charger setting RW OX62 ICC charger setting RW OX63 Item charger setting RW OX64 CV charger voltage setting RW OX65 Thermal regulation threshold setting RW OX66 Charger timeout setting and control RW OX67 Charger timeout setting and control RW OX68 Battery detection control RW OX69 IR compensation RW OX60 CHGLED setting and control RW OX60-0X82 DCDC configureO/1/2 RW	0X52	TS_HYSL2H setting	RW
OX55 VHTF_CHG setting RW OX56 VLTF_WORK setting RW OX57 VHTF_WORK setting RW OX58 JIETA standard Enable control RW OX59-0X5B JIETA standard setting RW OX61 Iprechg charger setting RW OX62 ICC charger setting RW OX63 Iterm charger setting RW OX64 CV charger voltage setting RW OX65 Thermal regulation threshold setting RW OX66 Charger timeout setting and control RW OX67 Charger timeout setting and control RW OX68 Battery detection control RW OX69 IR compensation RW OX60 CHGLED setting and control RW OX70 CHGLED setting and control RW OX80-0X82 DCDC configureO/1/2 RW	0X53	TS_HYSH2L setting	RW
OX56 VLTF_WORK setting RW OX57 VHTF_WORK setting RW OX58 JIETA standard Enable control RW OX69 Thermal regulation threshold setting RW OX67 Charger timeout setting and control RW OX68 Battery detection control RW OX69 RW OX69 RW OX6A Button battery charge termination voltage setting RW OX6A CHGLED setting and control RW OX80-OX82 DCDC configureO/1/2 RW OX80 RW OX80-OX82 DCDC configureO/1/2 RW	0X54	VLTF_CHG setting	RW
OX57 VHTF_WORK setting OX58 JIETA standard Enable control RW OX59-0X5B JIETA standard setting RW OX61 Iprechg charger setting OX62 ICC charger setting RW OX63 Iterm charger setting and control RW OX64 CV charger voltage setting RW OX65 Thermal regulation threshold setting RW OX67 Charger timeout setting and control RW OX68 Battery detection control RW OX69 IR compensation RW OX70 CHGLED setting and control RW OX70 CHGLED setting and control RW OX80-0X82 DCDC configureO/1/2 RW	0X55	VHTF_CHG setting	RW
OX58 JIETA standard Enable control RW Ox59-0X5B JIETA standard setting RW OX61 Iprechg charger setting RW OX62 ICC charger setting RW OX63 Iterm charger setting and control RW OX64 CV charger voltage setting RW OX65 Thermal regulation threshold setting RW OX67 Charger timeout setting and control RW OX68 Battery detection control RW OX69 IR compensation RW OX6A Button battery charge termination voltage setting RW OX70 CHGLED setting and control RW OX80-0X82 DCDC configureO/1/2 RW	0X56	VLTF_WORK setting	RW
0x59-0X5B JIETA standard setting RW 0X61 Iprechg charger setting RW 0X62 ICC charger setting RW 0X63 Iterm charger setting and control RW 0X64 CV charger voltage setting RW 0X65 Thermal regulation threshold setting RW 0X67 Charger timeout setting and control RW 0X68 Battery detection control RW 0X69 IR compensation RW 0X6A Button battery charge termination voltage setting RW 0X70 CHGLED setting and control RW 0X80-0X82 DCDC configure0/1/2 RW	0X57	VHTF_WORK setting	RW
OX61 Iprechg charger setting RW OX62 ICC charger setting RW OX63 Iterm charger setting and control RW OX64 CV charger voltage setting RW OX65 Thermal regulation threshold setting RW OX67 Charger timeout setting and control RW OX68 Battery detection control RW OX69 IR compensation RW OX6A Button battery charge termination voltage setting RW OX70 CHGLED setting and control RW OX80-0X82 DCDC configureO/1/2 RW OX80-0X82 DCDC configureO/1/2 RW OX60 RW OX60 RW OX80-0X82 DCDC configureO/1/2 RW OX60 RW OX60 RW OX80-0X82 DCDC configureO/1/2 RW OX60 RW OX60 RW OX60 RW OX80-0X82 DCDC configureO/1/2 RW OX60 R	0X58	JIETA standard Enable control	RW
OX62 ICC charger setting OX63 Iterm charger setting and control RW OX64 CV charger voltage setting RW OX65 Thermal regulation threshold setting RW OX67 Charger timeout setting and control RW OX68 Battery detection control RW OX69 IR compensation RW OX6A Button battery charge termination voltage setting RW OX70 CHGLED setting and control RW OX80-OX82 DCDC configureO/1/2 RW	0x59-0X5B	JIETA standard setting	RW
OX63 Iterm charger setting and control RW OX64 CV charger voltage setting RW OX65 Thermal regulation threshold setting RW OX67 Charger timeout setting and control RW OX68 Battery detection control RW OX69 IR compensation RW OX6A Button battery charge termination voltage setting RW OX70 CHGLED setting and control RW OX80-OX82 DCDC configureO/1/2 RW	0X61	Iprechg charger setting	RW
0X64 CV charger voltage setting RW 0X65 Thermal regulation threshold setting RW 0X67 Charger timeout setting and control RW 0X68 Battery detection control RW 0X69 IR compensation RW 0X6A Button battery charge termination voltage setting RW 0X70 CHGLED setting and control RW 0X80-0X82 DCDC configureO/1/2 RW	0X62	ICC charger setting	ŔW
OX65 Thermal regulation threshold setting OX67 Charger timeout setting and control OX68 Battery detection control RW OX69 IR compensation RW OX6A Button battery charge termination voltage setting OX70 CHGLED setting and control RW OX80-OX82 DCDC configure 0/1/2 RW	0X63	Iterm charger setting and control	RW
OX67 Charger timeout setting and control RW OX68 Battery detection control RW OX69 IR compensation RW OX6A Button battery charge termination voltage setting RW OX70 CHGLED setting and control RW OX80-0X82 DCDC configure0/1/2 RW	0X64	CV charger voltage setting	RW
OX68 Battery detection control RW OX69 IR compensation RW OX6A Button battery charge termination voltage setting RW OX70 CHGLED setting and control RW OX80-0X82 DCDC configure0/1/2 RW	0X65	Thermal regulation threshold setting	RW
0X69 IR compensation RW 0X6A Button battery charge termination voltage setting RW 0X70 CHGLED setting and control RW 0X80-0X82 DCDC configure0/1/2 RW	0X67	Charger timeout setting and control	RW
0X6A Button battery charge termination voltage setting RW 0X70 CHGLED setting and control RW 0X80-0X82 DCDC configure0/1/2 RW	0X68	Battery detection control	RW
0X70 CHGLED setting and control RW 0X80-0X82 DCDC configure0/1/2 RW	0X69	IR compensation	RW
0X80-0X82 DCDC configure0/1/2 RW	0X6A	Button battery charge termination voltage setting	RW
	0X70 (1) 110 110 110 110 110 110 110 110 110 1	CHGLED setting and control	RW STATE
0X83-0X86 DCDC1/2/3/4 voltage setting RW	0X80-0X82	DCDC configure0/1/2	RW
2001 2001 - 2001	0X83-0X86	DCDC1/2/3/4 voltage setting	RW



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	Address	Description Philip	R/W
XXX	0X90-0X91	LDOS ON/OFF control	RW
	0X93-0X9F	LDOS voltage setting	RW
	0XA1	Battery parameter Attilities	RW
	0XA2	Fuel gauge control	RW
	0XA4	Battery percentage data	R
	0XC0	ADC Channel enable control	RW
	0XC4-0XCB	VBAT/VBUS/VSYS/ICHG ADC data	R
	0XCD	ADC_data select	RW
	OXCE/OXCF	adc_dataiiiantt	R INITER
	OXE1	Type-C CC Audio Accessory enable	RW
Š	0XE3	Type-C CC mode control	RW
	0XE7	Type-C CC status	R

6.15.2 Register Description

6.15.2.1 REG 00: PMU status1

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5	VBUS good indication 0: not good 1: good	RO	POR	0
4	BATFET state 0: close 1: open	RO	POR	0
3	Battery present state 0: absent	RO	POR	0
2	Battery in Active Mode 0: in Normal 1: in Active Mode	RO	POR	0
1	Thermal regulation status 0: normal 1: in thermal regulation	RO	POR	0
0	Current Limit state 0: not in current limit state 1: in current limit state	RO	POR	0

6.15.2.2 REG 01: PMÜ status2

Bit	Description		W. C.	R/W	Reset	Default
7	Reserved	CHATTE TO THE TOTAL PROPERTY OF THE TOTAL PR	A A A	RO	/	0



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100	Battery Current Direction	No.	THE VY			THELIT
6:5	00: Standby	01: charge	R	0	POR	0
	10: discharge	11: Reserved				
4	System status indication	c till the second	D	0 &	POR	0
4	0: System is power off.	1: System is power on.	K	U	POR	
	VINDPM status			0	DOD	0
3	0: not in VINDPM	1: VINDPM	K	0	POR	0
	charging status					
	000: tri_charge	001: pre_charge				
2:0	010: constant charge(CC)	011: constant voltage(CV)	R	0	POR	0
	100: charge done	101 not charging	27	Ŋ		
	11X: Reserved	ONS WHITE	A VIZ			O VIZ

6.15.2.3 REG 05: BC_detect

Bit	Description		R/W	Reset	Default
	000:Reserved	001:SDR	18	HITT	
7:5	010:CDP	011:DCP	RO	POR	000b
	1XX:	1000			
4:0	Reserved		RO	/	0

6.15.2.4 REG 06: ILIM type

Bit	Description	R/W	Reset	Default
7:3	Reserved	RO	1	0
ALIV TO	001:power on default 010:VBUS remove default			A LIVE
2:0	011: TypeC CC 100:BC 1.2	R0	POR	000b
357	101: ACL 110:TWI register configure			7

6.15.2.5 REG 08: PMU fault

Bit	Description	R/W	Reset	Default
7:6	Reserved	/	/	00b
5	VBUS Over Voltage	RW1C	POR	0b
	0:VBUS<=7V 1:VBUS>7V			
4	DCDC Over Voltage			
	0: DCDC Voltage <= 130%	RW1C	POR	0b
117	1: DCDC Voltage > 130%			The state of the s
3	VSYS Over Voltage of 5V	RW1C	POR	Ob
× 20.	0: VSYS < 5V 1: VSYS >= 5V	KVVIC	PUR	POD



					///>	
	3/10/1V	VBAT UVLO(2.5V)	RW1C	POR	06	
Š	\$T	0: VBAT >= UVLO(2.5V) 1: VBAT < UVLO(2.5V)		. On		
,		Battery Over Temperature in Work mode				
	1	0: TS voltage≼= Tvhtf_work	RW1C	POR	0b	
		1: TS voltage> Tvhtf_work	~\			
		Battery Under Temperature in Work mode				
	0	0: TS voltage>= Tvltf_work	RW1C	POR	0b	
		1: TS voltage< Tvltf_work				

6.15.2.6 REG 0B: module enable control1

Bit	Description	R/W	Reset	Default
7:5	Reserved	RW	/	Ob No
**4	BC1.2 detect enable	RW	DOD	EFUSE
4	0:disable 1:enable	KVV	POR	0b
3	Type-C CC detect enable	RW	POR	EFUSE
5	0:disable 1:enable	NV S	POR	0b
2	Gauge enable	RW	POR	1b
	0:disable 1:enable ®	KVV	FOR	10
1	Reserved	RW	/	0b
0	Watchdog enable	RWAC	POR	0b
0	0:disable 1:enable	NVAC	PUN	OD .

6.15.2.7 REG 10 DCDC/LDO Discharge_configure

Bit	Description	R/W	Reset	Default
7:3	Reserved	RW	1	00100b
2	O:disable 1:enable	RW	POR	1b
1:0	Reserved	RW	/	10b

6.15.2.8 REG 14: Tshut configure

Bit	Description			R/W	Reset	Default
7:3	Reserved			RO	/	0
	13/1	erature Protection Level1 Co	onfiguration	anin		.:05
2:1	00: 115deg	01: 125deg		RW	POR	01b
Z KINGE V	10: 135deg	11: Reserved	**************************************			Z TOPE TO
0	DIE Temperatu	re Detect Enable	WE THE THE THE THE THE THE THE THE THE TH	RW	POR	1b



0: disable 1: enable

6.15.2.9 REG 15: Minimum system voltage control

Bit	Description	XST .		R/W	Reset	Default
7:3	Reserved ***		- FEITH	RO -	*/	00000b
	Minimun system	voltage limit				
	3.0+N*0.1 V					
2:0	000: 3.0V	001: 3.1V	010: 3.2V	RW	POR	101b
	011: 3.3V	100: 3.4V	101: 3.5V			
	110: 3.6V	111: 3.7V				

6.15.2.10 REG 16: Input voltage limit control

LO REG 16	: Input voltage li	mit control	Ŋ		anth		. o.C
Bit	Description	RELIVE TO THE PROPERTY OF THE		ALIV TO	R/W	Reset	Default
7:4	Reserved	, AX		XXX	RO	1	X (N)
33	VINDPM config	uration:	×	A CONTRACTOR OF THE PARTY OF TH			
	3.88+N*0.08 V	& ~		<i>'</i>	10	NA PARTIES	
	0000: 3.880	0001: 3.96V	0010; 4.04V	11		<i>\$111</i>	
3:0	0011: 4.12V	0100: 4.20V	0101: 4.28V	3 A V	514	POR	EFUSE
3.0	0110: 4.36V	0111: 4.44V			RW	POR	0110b
	1000: 4.52V	1001: 4.60V	1010: 4.68V	1011:			
	4.76V 11	.00: 4.84V 110	01: 4.92V	1110: 5.00V			
	1111: 5.08V						

6.15.2.11 REG 17: Input current limit control

Bit	Description	DIV This		R/W	Reset	Default
7:6 Reserved			**************************************	RO	/	* A STATE OF THE S
	Input current limit: 1	00+N*50mA	K. A. C.		A A A A A A A A A A A A A A A A A A A	,
5:0	000000: 100mA	000001: 150mA	000010: 200mA	RW	POR	EFUSE
	····	111110: 3200mA	111111: 3250mA	-5	<i>¥</i>	001000b

6.15.2.12 REG 18: Reset the fuel gauge

Bit	Description	R/W	Reset	Default
7:4	Reserved	RO	/	0
3	reset the gauge(includes registers) O: normal 1: reset	RWAC	POR	0b
2	reset the gauge besides registers 0: normal 1: reset	RW	POR	Ob
1:0	Reserved	RO	1 44	0



6.15.2.13 REG 19: module enable control2

	18/2			?		18/2
Š	Bit	Description		R/W	Reset	Default
	7:5	Reserved		RO	1	0
	4	Boost enable 0: disable	1: enable	RW	System Reset	0b
	3	Button Battery ch 0: disable	narge enable 1: enable	RW	System Reset	0b
	2	Battery charge le 0: disable	d enable 1: enable	RW	POR	1b
	1	Battery charge er	nable 1: enable	RW	System Reset	1b
	PRINT	Watchdog Modu 0: disable	le enable 1: enable	RW	System Reset	Op

6.15.2.14 REG 1A: Watchdog control

			1777	
Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
	Watchdog Reset Configuration			
	00: IRQ only 01: IRQ and System Reset			
5:4	10: System Reset and Pull down PWROK 1s	RW	POR	0b
	11: System Restart(PWROFF & PWRON)and Pull down PWROK			
	1s,	A.C.		all
3 1/2	watchdog clear signal	RWAC	POR	Ob ALZ BRIDE
2	0: normal 1: clear	RWAC	POR	OD
XX	TWSI watchdog timer configuration		, talky	7
2:0	000: 1s 001: 2s 010: 4s	RW	POR	110b
2.0	011: 8s 101: 32s	NVV -43	HUN	1100
	110: 64s 111: 128s	-1		

6.15.2.15 REG 1B: Gauge low battery warning threshold setting

Bit	Description	R/W	Reset	Default
	low battery warning threshold			
	5-20%, 1% per step			
7:4	0000: 5% 0001: 6%	RW	POR	1010b
ALIV TO THE PROPERTY OF THE PR	1111: 20% high	ant		THE VIEW STATES
***	low battery shutdown threshold	DIA	DOD .*	**
3:0	0-15%, 1% per step	RW	POR	0001b



		1/1.			
	THE IN	0000: 0%	0001: 1%	NO.	THE TOTAL PROPERTY OF THE PROP
Š,	A. T.		1111: 15%	A CONTRACTOR OF THE PROPERTY O	***

6.15.2.16 REG 1C: GPO configure

Bit	Description	R/W	Reset	Default
7:5	Reserved	RW	POR	000b
4	GPO1 Output Configure 0: Low 1: High	RW	POR	0b
3:1	Reserved	RW	POR	000b
0	GPO0 Output Configure 0: Low 1: High	RW	POR	0b

6.15.2.17 REG 1D: Low power configure

Bit	Description	A STATE OF THE STA	R/W	Reset	Default
7:1	Reserved	William Control of the Control of th	RO	POR	0000111 b
0	Green mode enable	1000	RW	System	0b
U	0: disable 1: enable		NVV	Reset	UD

6.15.2.18 REG 1E: Boost configure

Bit	Description	R/W	Reset	Default
7:4	Boost voltage regulation 4.55+0.064*N V 0000:4.550V 0001:4.614V 0010:4.678V 1110:5.446V 1111:5.510V	RW	System Reset	1001b
3:2	Boost Disable threshold 00:2.4V 01:2.6V 10:2.8V 11:3.0V	RW	POR	01b
1:0	Boost Output current limit 00: 500mA 01:900mA 10:1500mA 11:Disable current limit	RW	System Reset	00b

6.15.2.19 REG 20: PWRON status

	Bit	Description	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	Try Vil	R/W	Reset	Default
	7:6	Reserved	ALV TO SERVICE		RO	/	0
×	**************************************	POWERON alv	ways high when EN M	Node as POWERON Source	RO	System	Ob
		0: no	1: yes	A STATE OF THE PARTY OF THE PAR		Reset	



	///				//^>
×	4	Battery Insert and Good as POWERON Source 0: no 1: yes	RO	System Reset	06
ž.,	3	Battery Voltage > 3.3V when Charged as Source 0: no 1: yes	RO	System Reset	0b
	2	VBUS Insert and Good as POWERON Source 0: no 1: yes	RO	System Reset	0b
	1	IRQ PIN Pull-down as POWERON Source 0: no 1: yes	RO	System Reset	0b
	0	POWERON low for on level when POWERON Mode as POWERON Source 0: no 1: yes	RO	System Reset	Ob

6.15.2.20 REG 21: PWROFF status

	-1KD.	-10°			XØ`
Š	Bit	Description	R/W	Reset	Default
	7	Die Over Temperature as POWEROFF Source 0: no 1: yes	RO	POR	0b
	6	DCDC Over Voltage as POWEROFF Source 0: no 1: yes	RO	POR	0b
	5	DCDC Under Voltage as POWEROFF Source 0: no 1: yes	RO	POR	0b
	4	LDO over current as POWEROFF Source 0: no 1: yes	RO	POR	0b
	3	0: no 1: yes	RO	POR	Ob Nicolaine
×	2	POWERON always low when EN Mode as POWEROFF Source 0: no 1: yes	RO	POR	0b
	1	Software configuration as POWEROFF Source 0: no 1: yes	RO 🐴	POR	0b
	0	POWERON Pull down for off level when POWERON Mode as POWEROFF Source 0: no 1: yes	RO	POR	Ob

6.15.2.21 REG 22: PWROFF_EN

Bit	Description	R/W	Reset	Default
7:4	Reserved	RO	/	0000p
A TOPIC OF THE PERSON OF THE P	LDO Over-Current as POWEROFF Source enable	PIM	DOD	EFUSE
23	0: disable 1: enable	RW	POR	0b



	"//	(5)			7/^>	
	2	Reserved	RO	/	1b	
X	**	PWRON > OFFLEVEL as POWEROFF Source enable	RW	POR AND	EFUSE	
,	1	0: disable 1: enable	IVV	POR NATIONAL STATES	0b	l
		Function Select when REG22[2]=1 and button event occur	RW 🧐	POR	EFUSE	
	0	0: Power-off 1: Restart	r.vv '	PUK	0b	

6.15.2.22 REG 23: PWROFF of DCDC OVP/UVP control

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4	DCDC 120%(130%) high voltage turn off PMIC function O: disable 1: enable	RW	POR	1b
3	DCDC4 85% low voltage turn off PMIC function 0: disable 1: enable	RW	POR	Ob
2	DCDC3 85% low voltage turn off PMIC function 0: disable 1: enable	RW	POR	1b
1	DCDC2 85% low voltage turn off PMIC function 0: disable 1: enable	RW	POR	1b
0	DCDC1 85% low voltage turn off PMIC function 0: disable 1: enable	RW	POR	1b

6.15.2.23 REG 24: VSYS voltage for PWROFF threshold setting

Bit	Description	R/W	Reset	Default
7	Reserved	RO	/	0 Alian
6:4	Battery Voltage for POWEROFF 2.6~3.3V,0.1V/step,8steps 000: 2.6V 001: 2.7V 111: 3.3V	RW -	POR	EFUSE 000b
3	Reserved	RO	/	0
2	Check the PWROK Pin enable after all dcdc/ldo output valid 128ms 0: disable 1: enable	RW	POR	1b
1	POWEROFF Delay 4ms after PWROK disable 0: disable 1: enable	RW	POR	1b
0	POWEROFF Sequence Control 0: At the same time 1: the reverse of the startup	RW	POR	Obel ^{IV}



6.15.2.24 REG 25: Sleep and Wakeup configure

1(/)	16			160
Bit	Description	R/W	Reset	Default
7	Reserved	RO	1	0
6	Auto sleep enable	RWAC	System	0b
	0: disable 1: enable	NWAC .	Reset	OD
5	IRQ Pin low to Wakeup	RW	POR	0b
٦	0: disable 1: enable	KVV	FOR	OD
4:3	Reserved	RO	POR	00b
2	DCDC/LDO Voltage Select when Wakeup	RW	POR	0b
2	0: The Default 1: The voltage before wakeup	7 th	POR	OD
1	Wake Up enable	RWLC	System	Ob Alizabilia
1	Wake Up enable 0: disable 1: enable	KWLC	Reset	OB
0	SLEEP enable	RWLC	System	0b
	0: disable 13 enable	KWLC	Reset	OD.

6.15.2.25 REG 26: IRQLEVEL/OFFLEVEL/ONLEVEL setting

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5:4	IRQLEVEL configuration 00: 1s	RW	POR	01b
3:2	OFFLEVEL configuration 00: 4s 01: 6s 10: 8s 11: 10s	RW	POR	01b
1:0	ONLEVEL configuration 00: 128ms	RW 4	POR	EFUSE 10b

6.15.2.26 REG 27: Soft Poweroff configure

Bit	Description	R/W	Reset	Default
7:4	Reserved	RO	POR	0000b
3	PWROK PIN pull low to Restart the System	RW	POR	0b
3	0: disable 1: enable	7.0V	FOR	OD
2 117	PWRON 16s to shutdown the PMIC enable	RW	POR	1b . 117 11/10
Z	0: disable 1: enable	NVV	POR	10 TO
× 1	Restart the System POWOFF/POWON and reset the related	RWAC	POR	0b



	THE IN	registers	THE TOTAL PROPERTY OF THE PARTY			THE IT	
Š.	A TO	0: normal 1: reset	A A A A A A A A A A A A A A A A A A A			*	
0	0	Soft PWROFF		RWAC	POR	0b	
	0: Normal 1: PWROFF Configure	E HILLEY	KWAC	HOR	OD		

6.15.2.27 REG 28: Auto Sleep map0

Bit	Description	R/W	Reset	Default
7	ALDO4 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b
6	ALDO3 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b
5	ALDO2 PWROFF enable when auto_sleep configure 0: disable 1: enable ALDO1 PWROFF enable when auto_sleep configure 0: disable 1: enable		POR	Ob
4			POR	0b
3	DCDC4 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b
2	DCDC3 PWROFF enable when auto_sleep configure 0: disable	RW	POR	0b
1	DCDC2 PWROFF enable when auto_sleep configure 0: disable	RW	POR	0b
0	O: disable 1: enable	RW	POR	Ob North Hall

6.15.2.28 REG 29: Auto Sleep map1

	with the second			
Bit	Description	R/W	Reset	Default
7	CLDO4 PWROFF enable when auto_sleep config	gure RW	POR	0b
7	0: disable 1: enable	KVV	POR	Ob
	CLDO3 PWROFF enable when auto_sleep config		DOD	Ob
6	0: disable 1: enable	RW	POR	0b
_	CLDO2 PWROFF enable when auto_sleep config		DOD	0b
5	0: disable 1: enable	RW	POR	
4	GLDO1 PWROFF enable when auto_sleep config		DOD	Oh Silvi
4	0: disable 1: enable	RW	POR	Ob ATT
XX.	BLDO4 PWROFF enable when auto_sleep config		200	*
∌°3	0: disable 1: enable	RW	POR	′ 0b



					7///	
2	3/10/10	BLDO3 PWROFF enable when auto_sleep configure	RW	POR	06	
	*	0: disable 1: enable	NVV	PUN	***	
1	4	BLDO2 PWROFF enable when auto_sleep configure	DVA	POR	Ob	
	1	0: disable 1: enable	RW			
0	0	BLDO1 PWROFF enable when auto_sleep configure	DIA		Oh	
	0: disable 1: enable	RW	POR	0b		

6.15.2.29 REG 2A: Auto Sleep map2

Bit	Description	R/W	Reset	Default
7:2	Reserved	RO	POR	0b
1	GREEN MODE enable when auto sleep configure 0: disable 1: enable	RW	POR	Ob Shing
0	CPUSLDO PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b

6.15.2.30 REG 2B: Fast pwron setting 0

Bit	Description	R/W	Reset	Default
7:6	DCDC4 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
5:4	DCDC3 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
3:2	DCDC2 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	Ob Thirties
1:0	DCDC1 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b

645.2.31 REG 2C: Fast pwron setting 1

Bit	Description	R/W	Reset	Default
7:6	ALDO4 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
5:4	ALDO3 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
3:2	ALDO2 Fast Power On Start Sequence 00°10: Start Sequence Code 11: disable	RW	POR	0b
1;0	ALDO1 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	Observe



6.15.2.32 REG 2D: Fast pwron setting 2

18/2				180
Bit	Description	R/W	Reset	Default
7:6	BLDO4 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
5:4	BLDO3 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
3:2	BLDO2 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
1:0	BLDO1 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b

6.15.2.33 REG 2E: Fast pwron setting 3

	A1V			A 11/
Bit	Description	R/W	Reset	Default
7:6	CLDO4 Fast Power On Start Sequence	RW 🐗	POR) Ob
7.0	00~10: Start Sequence Code 11: disable	KW 1	PUR	OD
5:4	CLDO3 Fast Power On Start Sequence	RW	POR	0b
3.4	00~10: Start Sequence Code 11: disable			OD
3:2	CLDO2 Fast Power On Start Sequence	RW	202	0b
3.2	00~10: Start Sequence Code 11: disable	LVV	POR	UD
1:0	CLDO1 Fast Power On Start Sequence	RW	POR	Oh
1.0	00~10: Start Sequence Code 11: disable	KVV	PUK	0b

6.15.2.34 REG 2F: Fast pwron setting 4

		10.		2,610
Bit	Description	R/W	Reset	Default
Ž	Reserved	RO	POR	Ob
5	Fast Power On Enable 0: disable 1: enable	RW	POR	0b
4	Fast Wake up Enable 0: disable 1: enable		POR	0b
3:2	Reserved	RO	POR	00b
1:0	1:0 CPUSLDO Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable		POR	0b

6.15.2.35 REG 3E: TWI/RSB configure

	Bit	Descr	iption	A VZ Hid		R/W	Reset	Default	
	**·O	BUS N	∕lode Sele	et:	× ×	RW	POR 🕹	00h	
×	§ 7 :0	7Ch	: RSB	others: TWI	AND THE PERSON NAMED IN COLUMN TO TH	KVV	PUR	9-0011	



6.15.2.36 REG 40: IRQ Enable 0

100	10°			100
Bit	Description	R/W	Reset	Default
7	SOC drop to Warning Level2 IRQ enable 0: disable 1: enable	RW	System Reset	1b
6	SOC drop to Warning Level1 IRQ enable 0: disable 1: enable	RW	System Reset	1b
5	Reserved	RO	/	1b
4	Gauge New SOC IRQ enable 0: disable 1: enable	RW	System Reset	1b
3	Reserved	RO	/	0b
2	BOOST Over Voltage IRQ enable 0: disable 1: enable	RW	System Reset	Ob NV
1	VBUS Over Voltage IRQ enable 0: disable 1: enable	RW	System Reset	1b
0	VBUS Fault IRQ enable 0: disable 1: enable	RW	System Reset	1b

6.15.2.37 REG 41: IRQ Enable 1

Bit	Description	R/W	Reset	Default
7	VBUS Insert IRQ enable 0: disable 1: enable	RW	System Reset	1b
6	VBUS Remove IRQ enable 0: disable 1: enable	RW	System Reset	1b Alivarian
5	Battery Insert IRQ enable 0: disable 1: enable	RW	System Reset	1b
4	Battery Remove IRQ enable 0: disable 1: enable	RW	System Reset	1b
3	POWERON Short PRESS IRQ enable 0: disable 1: enable	RW	System Reset	1b
2	POWERON Long PRESS IRQ enable 0: disable 1: enable	RW	System Reset	1b
1	POWERON Negative Edge IRQ enable 0: disable 1: enable	RW	System Reset	0b
0	POWERON Positive Edge IRQ enable 0: disable 1: enable	RW	System Reset	Ob China



6.15.2.38 REG 42: IRQ Enable 2

18/7				180
Bit	Description	R/W	Reset	Default
7	Watchdog Expire IRQ enable 0: disable 1: enable	RW	System Reset	0b
6	LDO Over Current IRQ enable 0: disable 1: enable	RW	System Reset	1b
5	BATFET Over Current Protection IRQ enable 0: disable 1: enable	RW	System Reset	0b
4	Battery charge done IRQ enable 0: disable 1: enable	RW	System Reset	1b
3	Charger start IRQ(chgst_irq) enable 0: disable 1: enable	RW	System Reset	1b
2	DIE Over Temperature level1 IRQ enable 0: disable 1: enable	RW	System Reset	1b
1	Charger Safety Timer1/2 expire IRQ enable 0: disable 1: enable	RW	System Reset	1b
0	Battery Over Voltage Protection IRQ enable 0: disable 1: enable	RW	System Reset	1b

6.15.2.39 REG 43: IRQ Enable 3

Bit	Description	R/W	Reset	Default
7	BC1.2 detect finished IRQ enable 0: disable 1: enable	₩ RW	System Reset	1b
6	BC1.2 detect result change IRQ enable 0: disable 1: enable	RW	System Reset	1b
5	Reserved	RO	POR	0b
4	Battery Over Temperature Quit IRQ enable 0: disable 1: enable	RW	System Reset	1b
3	Battery Over Temperature in Charge mode IRQ enable 0: disable 1: enable	RW	System Reset	1b
2	Battery Under Temperature in Charge mode IRQ enable 0: disable 1: enable	RW	System Reset	1b
1	Battery Over Temperature in Work mode IRQ enable 0: disable 1: enable	RW	System Reset	1b
Ó	Battery Under Temperature in Work mode IRQ enable 0: disable 1: enable	RW	System Reset	1b



6.15.2.40 REG 44: IRQ Enable 4

Bit	Description	R/W	Reset	Default
7	Reserved Athlitti	RO 🦸		0b
6	Type-C device removed (unattached) IRQ enable 0: disable 1: enable	RW	System Reset	1b
5	Type-C device insert and detection finished IRQ enable 0: disable 1: enable	RW	System Reset	1b
4:0	Reserved	RO	/	00011b

6.15.2.41 REG 48: IRQ Status 0

		.\"		- Alle
Bit	Description	R/W	Reset	Default
XX	SOC drop to Warning Level IRQ			*
7	0: no irq 1: irq	RW1C	POR	0b
	when SOC >= Warning Level or SOC < shutdown Level to clear it	401		
	SOC drop to Shutdown Level IRQ	No.	System	
6	0: no irq 1: irq	RW1C	System	0b
	when SOC >= Shutdown Level to clear it		Reset	
5	Reserved	RO	POR	0b
4	Gauge New SOC IRQ	DVA/4.C	System	Ole
4	0: no irq 1: irq	RW1C	Reset	0b
2	is a cum	acth	System	Ol-
3	Reserved	RO	Reset	Ob Willow
N. T. WAR.	BOOST OverVoltage IRO	DIA/4.C	System	Ž.
3,72	0: no irq	RW1C	Reset	90b
1	VBUS OverVoltage IRQ	RW1C	System	0b
1	0: no irq 🔅 1: irq 💖	KVVIC	Reset	UD
0	VBUS Fault IRQ	RW1C	System	0b
	0: no irq 1: irq	IVVVIC	Reset	OD

6.15.2.42 REG 49: IRQ Status 1

Bit	Description	R/W	Reset	Default
7	VBUS Insert IRQ O: no irq 1: irq VBUS Remove to clear it	RW1C	System Reset	Ob Ob
6	VBUS Remove IRQ 0: no irq 1: irq	RW1C	System Reset	0b



				//\\	
THE LY	VBUS Insert to clear it			RELIV	
5	Battery Insert IRQ 0: no irq 1: irq Battery Remove to clear it	RW1C	System	Ob	
4	Battery Remove IRQ 0: no irq 1: irq Battery Insert to clear it	RW1C	System Reset	Ob	
3	POWERON Short PRESS IRQ 0: no irq	RW1C	System Reset	0b	
2	POWERON Long PRESS IRQ Octro irq 1: irq	RW1C	System Reset	0b	1
1	POWERON Negative Edge IRQ 0: no irq 1: irq	RW1C	System Reset	Ob Color	
0	POWERON Positive Edge IRQ 0: no irq 1: irq	RW1C	System Reset	0b	

6.15.2.43 REG 4A: IRQ Status 2

Bit	Description	R/W	Reset	Default
7	Watchdog Expire IRQ 0: no irq 1: irq	RW1C	System Reset	0b
6	LDO Over Current IRQ 0: no irq 1: irq LDO Current to normal to clear it.	RW1C	System Reset	0b
5	BATFET Over Current Protection IRQ 0: no irq 1: irg	RW1C	System Reset	06 P
4	Battery charge done IRQ 0: no irq 1: irq Battery charge start to clear it	RW1C	System Reset	Ob
3	Battery charge start IRQ 0: no irq 1: irq Battery charge done to clear it	RW1C	System Reset	Ob
2	DIE Over Temperature level1 IRQ 0: no irq 1: irq DIE Temperature to normal to clear it	RW1C	System Reset	0b
1	Charger Safety Timer1/2 expire IRQ 0: no irq 1: irq	RW1C	System Reset	Ob N
0	Battery Over Voltage Protection IRQ	RW1C	System	0b



	\$1\v	0: no irq 1: irq	NO TO THE PARTY OF	Reset	RIV	
A A A		Battery Voltage to normal to clear it	, XX		**	

6.15.2.44 REG 4B: IRQ Status 3

Bit	Description	R/W	Reset	Default
7	BC1.2 detect finished IRQ. 0: no irq 1: irq VBUS remove, bc1.2 detect again will clear it.	RW1C	System Reset	0b
6	BC1.2 detect result change IRQ 0: no irq 1: irq VBUS remove will clear it	RW1C	System Reset	0b
5	Reserved Reserved	RO	System Reset	Ob No Pictor
4	Battery Over Temperature Quit in Charge mode IRQ 0: no irq bcot_irq to clear it	RW1C	System Reset	Ob
3	Battery Over Temperature in Charge mode IRQ 0: no irq 1: irq bcotq_irq to clear it	RW1C	System Reset	0b
2	Battery Under Temperature in Charge mode IRQ 0: no irq 1: irq Battery Temperature to normal to clear it	RW1C	System Reset	0b
1	Battery Over Temperature in Work mode IRQ 0: no irq 1: irq Battery Temperature to normal to clear it	RW1C	System Reset	Ob Not The World
0	Battery Under Temperature in Work mode IRQ 0: no irq 1: irq Battery Temperature to normal to clear it	RW1C	System Reset	Ob

6.15.2.45 REG 4C: IRQ Status 4

Bit	Description	R/W	Reset	Default
7	Reserved	RO	System Reset	0b
6	Type-C device removed (unattached) IRQ status: 0: no irq 1: irq insert_irq to clear it	RW1C	System Reset	Ob Childs
5	Type-C device insert and detection finished IRQ status: 0: no irq 1: irq	RW1C	System Reset	0b



	-//	//	//\\\\	//\\		//\\	
	THE IV	remove irq to clear it	NIV NIV	HIV		N. T.	
X	4:0	Reserved	A. Carlotte and the second sec		RO	System 00000b	

6.15.2.46 REG 50: TS pin configure

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
	TS PIN function select:			
	0: TS pin is the battery temperature sensor input and will affect			EFUSE
4	the charger	RW	POR	
	1: TS pin is the external fixed input and doesn't affect the	h		0b
_//	scharger	307		
THE V	TS current source on/off enable			-1616
2.2	00: off	DIA	DOD W	EFUSE
3:2	01/10: on when TS channel of ADC is enabled	RW	POR	01b
	11: always on	18	Hillitia	
	current source to TS pin configuration			
1:0	00: 20uA	RW	POR	10b
	10: 50uA 11: 60uA			

6.15.2.47 REG 52: TS_HYSL2H setting

Bit	Description	R/W	Reset	Default
7:0	hysteresis for TS from low go to normal Thys = N*16mV (default 32mV)	RW	POR	2h

6.15.2.48 REG 53: TS_HYSH2L setting

*	Bit	Description	A STATE OF THE PARTY OF THE PAR	R/W	Reset	Default	
	7:0	hysteresis for 1S from high go to normal Thys = N*4mV (default 4mV)	-Filler	RW -	POR	1h	

6.15.2.49 REG 54: VLTFCHG setting

Bit	Description	R/W	Reset	Default	
	VLTF in voltage of charge configuration				
7:0	VLTF = N*32 mV (default is about 0deg)	RW	POR	29h	
	This is also T1 of JEITA	la.			-3

6.15.2.50 REG 55: VHTFCHG setting

Bit	Description	XX AND THE REAL PROPERTY OF THE PERTY OF THE	R/W	Reset	Default
7:0	VHTF in voltage of charge configuration	A A A A A A A A A A A A A A A A A A A	RW	POR	58h



	BRID	VHTF = N*2 mV (default is about 55deg)	JU V	E IV
_X	***	This is also T4 of JEITA	XXXXXX	XXXXX

6.15,2.51 REG 56: VLTFWORK setting

Bit	Description	R/W	Reset	Default	
7:0	VLTF in voltage of work configuration	25		3Eh	
7.0	VLTF = N*32 mV (default is about -10deg)	RW	POR	SEII	

6.15.2.52 REG 57: VHTFWORK setting

Bit	Description	R/W	Reset	Default
7:0	VHTF in voltage of work configuration VHTF = N*2 mV (default is about 60deg)	RW	POR	4Ch

6.15.2.53 REG 58: JIETA standard Enable control

Bit	Description			R/W	Reset	Default
7:1	Reserved		A STORY	RO		0
0	JEITA Standard Enab	e	深.Hill.	DW S	POR	EFUSE
U	0: disable	1: enable	1 MAY	RW	PUN	0b

6.15.2.54 REG 59: JEITA CV configuration

Bit	Description	R/W	Reset	Default
7:6	Current fall of Warm in JEITA Standard 00: 100% 01: 50% 10:25% 11:Reserved	RW	POR	00b
5:4	Current fall of Cool in JEITA Standard 00: 100% 01: 50% 10:25% 11:Reserved	RW	POR	01b
3:2	Reserved	RO	1	01b
1:0	Reserved	RO	1 3	00b

6.15.2.55 REG 5A: JIETA Cool configuration

Bit	Description	R/W	Reset	Default
7:0	Cool Temperature(T2) in voltage of charge configuration VHTF = N*16 mV (default is about 10deg)	RW	POR	37h

6.15.2.56 REG 5B: JIETA Warm configuration

Bit	Description	R/W	Reset	Default
7:0	Warm Temperature(T3) in voltage of charge configuration VHTF = N*8 mV (default is about 45deg)	RW	POR	1Eh



6.15.2.57 REG 61: Iprechg charger setting

100		X(D)	X(D)^			X()>`
Bit	Description			R/W	Reset	Default
7:4	Reserved			RO	1	0
	Precharge correr	nt limit:	- \$\frac{1}{2}	-4	XIII(II)	
	64*N mA		,	,		
3:0	0000: 0mA	0001: 64mA	0010: 128mA	RW	POR	0010b
		0100: 896mA	0101: 960mA			

6.15.2.58 REG 62: ICC charger setting

Bit	Description	Bilarth		R/W	Reset	Default
7:5	Reserved	W. L.	NO.	RO	1	0
XXXXX	constant current	charge current limit:				*
	64*N mA if N<=4	8,34	A STATE OF THE PARTY OF THE PAR	. 1	A SAME	
5:0	000000: 0mA	000001: 64mA	000010: 128mA	RW	POR	010000b
	·····	101110: 2944mA	101111: 3008mA	No.		
	110000~111111:	Reserved	APU			

6.15.2.59 REG 63: Iterm charger setting and control

Bit	Description			R/W	Reset	Default
7:6	Reserved			RO	/	0
	DPM to disbale ch	narger terminal		anth		(A) Tilde
5	0: enable charger	terminal	A A A A A A A A A A A A A A A A A A A	RW	POR	Ob Pro
XXXX	1: disable charger	terminal			X	*
4	Charging termina	tion of current enable	A STATE OF THE STA	RW	System	1b
	0: disable	1: enable		1100	Reset	10
	Termination curre	ent limit:	11.			
	64*N mA					
3:0	0000: 0mA	0001: 64mA	0010: 128mA	RW	POR	0101b
		0111: 896mA	1000: 960mA			

6.15.2.60 REG 64: CV charger voltage setting

Bit	.Description	ŔŴ	Reset	Default
7:3	Reserved	RO	/	O PLY ,
2:0	Charge voltage limit	RW	POR 🎺	个 010b
2.0	000: 4.0V 001: 4.1V	010; 4.2V	TOK MAN	0100



		110.			
	SELIZ	011: 4.35V	100: 4.4V	111: 5.0V	W. Liv
×××	X (N)	101~110: Reserved	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	XXXXXX	

6.15.2.61 REG 65: Thermal regulation threshold setting

Bit	Description	:Fille	R/W	Reset	Default	
7:2	Reserved		RO	/	0	
1:0	Thermal regulation the	reshold 01: 80deg	RW	System	10b	
	10: 100deg	11: 120deg		Reset		

6.15.2.62 REG 67: Charger timeout setting and control

Bit	Description	R/W	Reset	Default
** 7	safety timer1/2 setting during DPM or thermal regulation 0: safety timer not slowed during input DPM or thermal regulation 1: safety timer slowed during input DPM or thermal regulation	RW	POR	Thb
6	Fast charge safe timer enable 0: disable 1: enable	RW	POR	1b
5:4	Fast charge safety timer configuration 00: 5hours 10: 12hours 11: 20hours	RW	POR	10b
3	Reserved	RO	/	0
2	pre-charge safe timer enable 0: disable 1: enable	ŔW	POR	1b
1:0	pre-charge safe timer configuration 00: 40mins 10: 60mins 11: 70mins	RW	POR	10b

6.15.2.63 REG 68: Battery detection control

Bit	t Description		R/W	Reset	Default
7:1	Reserved		RO	/	0
0	battery detection ena	ble	RW	POR	1b
	0: disable	1: enable			

6.15.2.64 REG 69: IR compensation

Bit	Description	R/W	Reset	Default
7.4	Reserved	RO	/	0
0	IR Compensation Enable	RW	POR	0b



0: disable 1: enable

6.15.2.65 REG 6A: Button battery charge termination voltage setting

Bit	Description		宋期	R/W	Reset	Default
7:3				RO	/	0
	Button Battery	charge termination vol	tage			
	2.6~3.3V,100	mV/step,8steps				
2:0	000: 2.6V	001: 2.7V	010: 2.8V	RW	POR	011b
	011: 2.9V	100: 3.0V	101: 3.1V	La.		
	110: 3.2V	111: 3.3V		Wight True		Hiar

6.15.2.66 REG 70: CHGLED setting and control

			4 10	
Bit	Description	R/W	Reset	Default
7	Reserved ***	RO	1	0
6	CHGLED pin output breath enable when REG70[2:0]=011b 0: disable; 1: enable;	RW	System Reset	0b
5:4	CHGLED pin output when REG70[2:0]=110b 00: Hiz; 01: Low/Hiz 25%/75% duty 1Hz; 10: Low/Hiz 25%/75% duty 4Hz; 11: drive low;	RW	System Reset	00b
3	Reserved	RO	/	0
A.K.	CHGLED pin display function configuration 000: display with type A function 001: display with type B function			EFUSE
2:0	010: display with breath function controlled by charger 011: display with breath function controlled by REG70<6> 110: output controlled by the register REG70[5:4] 100/101/111: Reserved	RW	POR	000b

6.15.2.67 REG 80: DCDC configure0

Bit	Description			R/W	Reset	Default
7:4	Reserved	h.		RO	/	0b
3	DCDC4 enable			RW	System	EFUŞE ^{ÇİİLDÎ}
3 NOTE OF THE PERSON OF THE PE	0: disable	1: enable	RIV	NVV	Reset	EFUŞE
2	DCDC3 enable			RW	System	EFUSE



	*//	//	7//	7/A)			7/^>	_
	A STATE OF THE STA	0: disable	1: enable	No.		Reset	THE LIVE	
X	*	DCDC2 enable	XX.	XXXXX	RW	System	EFUSE	
	1	0: disable	1: enable	A STATE OF THE STA	KVV	Reset	EFUSE	
		DCDC1 enable		E HINTE	D)A/	S ystem	FFLICE	
	0	0: disable	1: enable	**	RW 🤻	Reset	EFUSE	

6.15.2.68 REG 81: DCDC configure1

Bit	Description			R/W	Reset	Default
7	DCDC frequency spread enable			DVA	System	0b
'	0: disable	1: enable		RW	Reset	OD
	DCDC frequency sprea	ad range control		RW	System	Ob S
6	0: 50KHz	1: 100kHz		,≎KVV	Reset	Ob Alighian
5/10	Reserved	XX N	×.X	RO	/	06
4	DCDC3 PWM/PFM Co	ntrol	AND THE PERSON NAMED IN COLUMN TO PERSON NAM	RW 📣	System	0b
4	0: Auto Switch	1: Always PWM		NV	Reset	OD
3	DCDC2 PWM/PFM Co	ntrol	深圳	RW	System	0b
5	0: Auto Switch	1: Always PWM	10AV	NVV	Reset	OD
2	DCDC1 PWM/PFM Co	ntrol		D\A/	System	0b
2	0: Auto Switch	1: Always PWM		RW	Reset	OD
	DCDC UVP debounce	time configuration				
1:0	00: 60us	01: 120us		RW	POR	00b
	10: 180us	11: 240us		ath		

6.15.2.69 REG 82: DCDC configure2

Bit	Description	R/W	Reset	Default
7:1	Reserved	RO		0
0	DVM voltage ramp control 0: 15.625 us/step 1: 31.250 us/step	RW -	System Reset	Ob

6.15.2.70 REG 83: DCDC1 voltage setting

	Bit	Description	R/W	Reset	Default
	7	DCDC1 DVM enable control 0: disable	RW	System	1b
	,	1: enable	nth n	Reset	10
	SPIZ	DCDC1 output voltage config	, o	System	The last of the la
	6:0	0.5~1.2V,10mV/step,71steps	RW	Reset >	EFUSE
ÿ	54	1.22~1.54V,20mV/step,17steps		Meset **	7



0000000: 0.50V 0000001: 0.51V 1000110: 1,20V 1001000: 1.24V 1010111: 1.54V 1011000~1111111: Reserved

6.15.2.71 REG 84 DCDC2 voltage setting

^\V		~1\Z				
Bit	Description	XXXXXX	XXXXXX	R/W	Reset	Default
7	DCDC2 DVM enable c	ontrol 1: enable	A. F. T.	RW	System Reset	1b
6:0	DCDC2 output voltage 0.5~1.2V,10mV/step, 1.22~1.54V,20mV/step, 1.6~3.4V,100mV/step, 0000000: 0.50V 0000001: 0.51V 1000110: 1.20V 1000111: 1.22V 1001000: 1.24V 1010111: 1.54V 1011000: 1.60V 1011001: 1.70V	71steps ep,17steps e,19steps	CPOU	RW SALLAN	System	EFUSE

6.15.2.72 REG 85: DCDC3 voltage setting

Ş	Bit	Description	A SHAPE		R/W	Reset	
---	-----	-------------	---------	--	-----	-------	--



						//^>	
	7/10/10	DCDC3 DVM enable control	No.	RW	System	16	
X	*	0: disable 1: enable	A A A A A A A A A A A A A A A A A A A	NVV	Reset	**	
J.		DCDC3 output voltage config					
		0.5~1.2V,10mV/step,71steps	EHIH	G	HILLER		
		1.22~1.84V,20mV/step,32steps	-7/*				
		0000000: 0.50V					
		0000001: 0.51V					
	6:0			RW	System	EFUSE	
		1000110: 1.20V			Reset		
		1000111: 1.22V		anin			V
	A.IV	1000111: 1.22V 1001000: 1.24V	A CONTRACTOR OF THE PARTY OF TH	,		AIV TO	
	× **		X.X.		×	X	
	3	1100110 1011	**************************************		The state of the s	7	
7		1100110: 1.84V	A THE STATE OF THE PARTY OF THE	. 01	410		
		1100111~1101000: Reserved	Ethlin.		FILLIA		

6.15.2.73 REG 86: DCDC4 voltage setting

Bit	Description	R/W	Reset	Default
7	Reserved	RO	1	0
	DCDC4 output voltage config			
	1.0~3.7V,100mV/step,24steps			
	00000: 1.0V	anth		
6:0	00001: 1.1V	RW	System	EFUSE
A. A. A. A. A. A. A. A. A. A. A. A. A. A	00000: 1.0V 00001: 1.1V 		Reset	X X
	11011: 3.7V		THE STATE OF THE PARTY OF THE P	
	11100~11111: Reserved	- <u>-</u> 5	FIII TO	

6.15.2.74 REG 90: LDOS ON/OFF control 0

Bit	Description			R/W	Reset	Default
7	bldo4 enable 0: disable	1: enable		RW	System Reset	EFUSE
6	bldo3 enable 0: disable	1: enable	. ئ	RW	System Reset	EFUSE
5	bldo2 enable 0: disable	1, enable	A A A A A A A A A A A A A A A A A A A	RW	System Reset	EFUSE
4	bldo1 enable	A A A A A A A A A A A A A A A A A A A	A THE PARTY OF THE	RW	System	EFUSE



		17.	//\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\		-		///>	
	THE LY	0: disable	1: enable	No.		Reset	RIV	
X	3	aldo4 enable	NA THE	CLIFFA K.	D\A/	System	FFLICE	
Ž.,	3	0: disable	1: enable		RW	Reset	EFUSE	
	2	aldo3 enable		-Şillifi.	DVA/	System	FFLICE	
	2	0: disable	1: enable	-* *	RW 🦸	Reset	EFUSE	
	1	aldo2 enable			DVA	System	FFLICE	
	1	0: disable	1: enable		RW	Reset	EFUSE	
		aldo1 enable			DIA	System	FFLICE	
	0	0: disable	1: enable		RW	Reset	EFUSE	

6.15.2.75 REG 91: LDQS ON/OFF control 1

	- CV		.CV		
Bit	Description		R/W	Reset	Default
7:5	Reserved	××××××××××××××××××××××××××××××××××××××	RO	/	6
4	cpusido enable		RW	System	EFUSE
-	0: disable	1: enable		Reset	
3	cldo4 enable	The state of the s	RW	System	EFUSE
	0: disable	1: enable	T(VV	Reset	LIOSE
2	cldo3 enable	•	RW	System	EFUSE
	0: disable	1: enable	IXVV	Reset	LIOSE
1	cldo2 enable		RW	System	EFUSE
1	0: disable	1: enable	IVVV	Reset	LFUSE
	cldo1 enable	a i lattiv	RW	System	FFLICE : S
0	0: disable	1: enable	%KW	Reset	EFUSE

6.15.2.76 REG 93: ALDO1 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO		0
	aldo1 output voltage configuration 0.5~3.5V, 100mV/step, 31steps	-1	,	
4:0	00000: 0.5V 00001: 0.6V	RW	System Reset	EFUSE
	 11110: 3.5V 11111: Reserved	SUTIN		iliag

6.15.2.77 REG 94: ALDO2 voltage setting

Bit	Description	TO THE PARTY OF TH		R/W	Reset Default
-----	-------------	--	--	-----	---------------



						///	
	7:5	A TOP TO THE PERSON OF THE PER	THE IT	RO	1	0	
X	*	aldo2 output voltage configuration	A A A A A A A A A A A A A A A A A A A			*	
		0.5~3.5V,100mV/step,31steps					
	4:0	00000: 0.50	深圳	RW	System	EFUSE	
	4.0	aldo2 output voltage configuration 0.5~3.5V, 100mV/step, 31steps 00000: 0.5V 00001: 0.6V		I I V V	Reset	LIOSE	
		11110: 3.5V 11111: Reserved					

6.15.2.78 REG 95: ALDO3 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	O This
A TOPPE OF THE PERSON OF THE P	aldo3 output voltage configuration			X TOP TO SERVICE STATE OF THE
XY.	0.5~3.5V,100mV/step,31steps		1 Right	7
4.0	00000: 0.5V	101	System	FFLICE
4:0	00001: 0.6V	RW	Reset	EFUSE
	/ DU ^v			
	11110: 3.5V 11111: Reserved			

6.15.2.79 REG 96: ALDO4 voltage setting

Bit	Description		R/W	Reset	Default
7:5	anth dijarih	Ž	RÔ	/	0
THE VE	aldo4 output voltage configuration	A KANANA			HAVY TO SEE SEE SEE SEE SEE SEE SEE SEE SEE SE
**	0.5~3.5V,100mV/step,31steps	THE PARTY OF THE P			*
4:0	00000: 0.5V		RW	System	EFUSE
7.0	00001: 0.6V	-\$\frac{1}{2}\frac{1}{	-48	Reset	LIOSE
		1	,		
	11110: 3.5V 11111: Reserved				

6.15.2.80 REG 97: BLDO1 voltage setting

Bit	Description	R/W	Reset	Default
7:5	in the second se	RO	/	0
117	bldo1 output voltage configuration	BULL	6 .	N. A. Hall
4:0	0.5~3.5V, 100mV/step, 31steps	RW	System Reset	EFUSE
× × ×	00000: 0.5V		****	9



1	M. Comments				AVI
1/2/	00001: 0.6V	No. 10 Page 10	RIV		RIV
		#HHY K	ALLIA A	*Ethy	*
	11110: 3.5V	11111: Reserved	A STATE OF THE PARTY OF THE PAR	A A A A A A A A A A A A A A A A A A A	

6.15.2.81 REG 98: BLDO2 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
	bldo2 output voltage configuration			
	0.5~3.5V,100mV/step,31steps			
4:0	00000: 0.5V 00001: 0.6V	ŔŴ	System Reset	EFUSE
A THE IV		A THE VIEW OF THE PARTY OF THE	.*	KARIV
3P ·	11110: 3.5V 11111: Reserved			,

6.15.2.82 REG 99: BLDO3 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	1	0
	bldo3 output voltage configuration			
	0.5~3.5V, 100mV/step, 31steps			
4:0	00000: 0.5V 00001: 0.6V	RW	System Reset	EFUSE
A ROLL	11110: 3.5V 11111: Reserved			* KIRLIVE

6.15.2.83 REG 9A: BLDO4 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
	bldo4 output voltage configuration			
	0.5~3.5V,100mV/step,31steps			
4:0	00000: 0.5V	RW	System	EFUSE
4.0	00001: 0.6V		Reset	LIOSE
_//		anin		
* TOP IN	11110: 3.5V 11111: Reserved			* The live of the



6.15.2.84 REG 9B: CLDO1 voltage setting

100				100.
Bit	Description	R/W	Reset	Default
7:5		RO	1	0
	cldo1 output voltage configuration	-	Fill Control	
	0.5~3.5V,100mV/step,31steps			
4:0	00000: 0.5V	RW	System	EFUSE
4.0	00001: 0.6V	I I V V	Reset	LIOSE
	11110: 3.5V 11111: Reserved			

6.15.2.85 REG 9C CLDO2 voltage setting

	Bit	Description	R/W	Reset	Default
Š	7:5		RO		0
	4:0	cldo2 output voltage configuration 0.5~3.5V, 100mV/step, 31steps 00000: 0.5V 00001: 0.6V 11110: 3.5V 11111: Reserved	RW	System Reset	EFUSE

6.15.2.86 REG 9D: CLDO3 voltage setting

	Bit	Description	R/W	Reset	Default
۸X	7:5		RO	1	O
		cldo3 output voltage configuration			
	0.5~3.5V, 100mV/ste 00000: 0.5V 00001: 0.6V	0.5~3.5V, 100mV/step, 31steps	-212		
		00000: 0.5V	RW	System	EFUSE
		00001: 0.6V	NVV	Reset	EFUSE
		11110: 3.5V 11111: Reserved			

6.15.2.87 REG 9E: CLDO4 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	cldo4 output voltage configuration	RW	System	EFUSE



	1	Hillo	Miles		, o		AVE	•
	K KIRIV	0.5~3.5V,100mV/step	o, 31steps	XX XX		Reset	KARIV	
*41/13	57	00000: 0.5V	7	ALL MAN		*46	7	
J. J. J. J. J. J. J. J. J. J. J. J. J. J		00001: 0.6V		THE STATE OF THE PARTY OF THE P		THE SALES		
Ķ.		Filler		A THE STATE OF THE	-43	Filligs,		
		11110: 3.5V	11111: Reserved					

6.15.2.88 REG 9F: CPUSLDO voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	cpusldo output voltage configuration 0.5~1.4V, 50mV/step, 20steps 00000: 0.50V 00001: 0.55V 10011: 1.40V 10100~11111: Reserved	RW	System	EFUSE

6.15.2.89 REG A1: Battery parameter

Bit	Description	R/W	Reset	Default
7:0	Battery parameter ROM	RO	POR	xx

6.15.2.90 REG A2: Fuel gauge control

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	Ob
5	Reserved		POR	0b
4	ROM or SRAM select	RW	POR	0b
4	1: select sram; 0: select rom;	-45	FILLON.	OD
3:1	Reserved	RO	/	0b
0	brom writer control	RW	POR	Oh
U	1:enable 0:disable	LVV	PUN	0b

6.15.2.91 REG A4: Battery percentage data

Bit	Description	R/W	Reset	Default
7:0	pattery percentage	RO	POR	00h

6.15.2.92 REG CO: ADC Channel enable control

Bit	Description	*ACTIVATION OF THE PERSON OF T	A CHAIN TO THE STATE OF THE STA	R/W	Reset Default
-----	-------------	--	--	-----	---------------



	- '//	3			7/\\
	Z KIRLIV	batton battery(backup battery) voltage measure ADC channel			× TANKA TV
Š	7	enable	RW	POR	0b
ž.,		0: disable 1: enable			
	6	VMID voltage measure ADC channel 0 enable	RW 🕉	POR	0b
	0	0: disable 1: enable	-71	CT OIL	OB
	5	charger current ADC channel enable	RW	POR	0b
	3	0: disable 1: enable	IVV	ron	OD
	4	die temperature measure ADC channel enable	RW	POR	0b
		0: disable 1: enable			
	3	system voltage voltage measure ADC channel enable	₽₩	POR	0b
		0: disable 1: enable	SUL		Thirds.
	2/4	VBUS voltage measure ADC channel enable	RW	POR	.06
Š	华	0: disable 1: enable			
	1	TS pin measure ADC channel enable	RW	POR	1b
	_	0: disable 1: enable		HILL	
	0	battery voltage measure ADC channel enable	RW	POR	1b
	-	0: disable 1: enable			,

6.15.2.93 REG C4: vbat_h

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0b
5:0	vbat[13:8]	RÒ	POR	0b

6.15.2.94 REG C5: vbat_l

Bit	Description		CHATA TO	R/W	Reset	Default
7:0	vbat[7:0]	A STATE OF THE STA		RO	POR	0b

6.15.2.95 REG C6: VBUS_h

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0b
5:0	VBUS[13:8]	RO	POR	0b

6.15.2.96 REG C7: VBUS_I

Bit	Description	24	R/W	Reset	Default
7:0	VBUS[7:0]	Pita.	RO	POR	Ob This

6.15.2.97 REG C8: VSYS_h

Ş	>'		Market Street	, (Sh),		N. Carlos	
	Bit	Description	***		R/W	Reset	Default



7:6%	Reserved	NIV TO THE PERSON OF THE PERSO	RIV.	RO	/	0b&\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\
5:0	VSYS[13:8]		THE THE PERSON NAMED IN COLUMN TWO IS NOT THE PERSON NAMED IN COLUMN TWO IS NAMED IN COLUMN TWO IS NAMED IN COLUMN TWO IS NAMED IN COLUMN TWO IS NAMED IN COLUMN TWO IS NAMED IN COLUMN TWO IS NAMED IN COLUMN TWO IS NAMED IN COLUMN TWO IS NAMED IN COLUMN TWO IS NAMED IN COLUMN TWO IS NAMED IN COLUMN TWO IS NAMED IN COLUMN TWO IS NAMED IN COLUMN TWO IS NAMED IN COLUMN TWO IS	RO	POR	0b

6.15.2.98 REG C9: VSYS_I

Bit	Description	森洲	R/W	Reset	Default
7:0	VSYS[7:0]		RO	POR	0b

6.15.2.99 REG CA: ICHG_h

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0b
5:0	ichg_h[13:8]	RO	POR	0b

6.15.2.100 REG CB: ICHG_I

X	Bît	Description	NXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	R/W	Reset	Default
- -	7:0	ichg_l[7:0]		RO	POR	0b

6.15.2.101 REG CD: ADC_data select

Bit	Description	1 MAY	R/W	Reset	Default
7:2	Reserved		RO	1	0
1:0	adc_data_h/adc_data_l select configure: 00: TS		RW	POR	0b

6.15.2.102 REG CE: adc_data_h

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	Ob
5:0	adc_data_h[13:8]	RO	POR	0b

6.15.2.103 REG CF: adc_data_l

Bit	Description	(*************************************	R/W	Reset	Default
7:0	adc_data_I[7:0]		RO	POR	0b

6.15.2.104 REG E1: Type-C CC Audio Accessory enable

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5	Audio Accessory Enable. 0: disable 1: enable	RW	POR	0 112
4:0	Reserved	RO	/	O



6.15.2.105 REG E3: Type-C CC mode control

	100		/(/>`	105			1(D)	_
Š	Bit	Description			R/W	Reset	Default	
	7:6	Reserved			RO		0	
	5	DRP port prefer to be	e SRC.	**************************************	RW -	POR	0b	
	J	0: unactive	1: active		IVV	ron	OD .	
	4	DRP port prefer to be	e SNK.		RW	POR	1b	
	4	0: unactive	1: active		IVV	ron		
		The Current Mode Co	ontrol.					
	3:2	0x: Default Mode			RW	POR	00b	
		10: 1.5A Mode	11: 3.0A Mode		actu			i
	AIV	The Port Mode Conti	rol.	A A A A A A A A A A A A A A A A A A A	Ç		A IV TAILO	
	1:0	00: Disable	01: SINK	X.X.	RW	POR	01b	
Š	57	10: SOURCE	11: DRP	ALL MAN			7	

6.15.2.106 REG E7: Type-C CC status

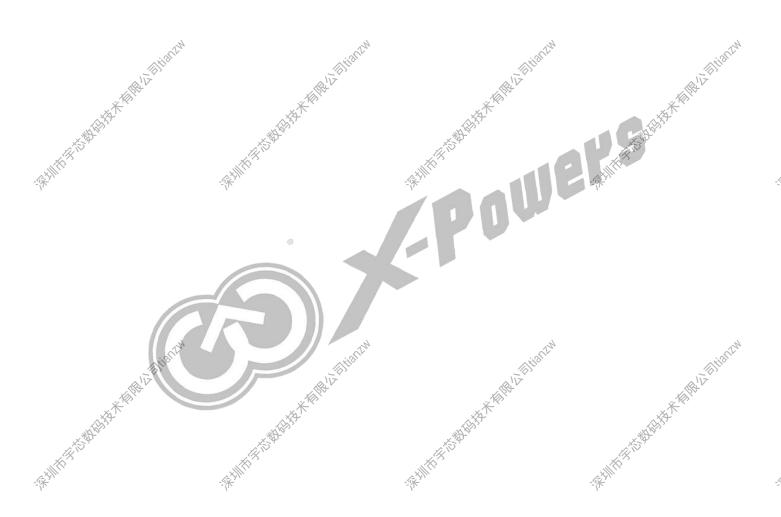
			FIII.	
Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
	The Power State of Source of CC Logic in HW mode			
5:4	00: POWER IDLE 01: POWER_DEF	RO	POR	00b
	10: POWER_1P5A			
	The State of CC Logic in HW mode	14		
	0000: DISABLE	BULL		_\B\tilas
THE V	The State of CC Logic in HW mode 0000: DISABLE 0001: UNATTACH_SNK			THE IV
*	0010: ATTACHWAIT_SNK			*
	0011: ATTACH_SNK		THE STATE OF THE PARTY OF THE P	
	0100: UNATTACH_SRC	-47	Fillight,	
	0101: ATTACHWAIT	-1		
3:0	0110: ATTACH_SRC	RO	POR	0000b
3.0	0111: AUDIO_ACSY			0000
	1000: Reserved			
	1001: TRY_SRC			
	1010: TRYWAIT_SNK	.4		
//	1011: TRY_SNK	anta		Wilds
TO THE PARTY	1010: TRYWAIT_SNK 1011: TRY_SNK 1100: TRYWAIT_SRC			THE VE
*	1101: Reserved			*
	1110: ERROR_RECOVERY		A A A A A A A A A A A A A A A A A A A	



1111: Reserved

Note:

Default value below "EFUSE" is the default efuse value if different EFUSE configuration is needed, please contact FAE/SD for support.



A THE THE PARTY OF

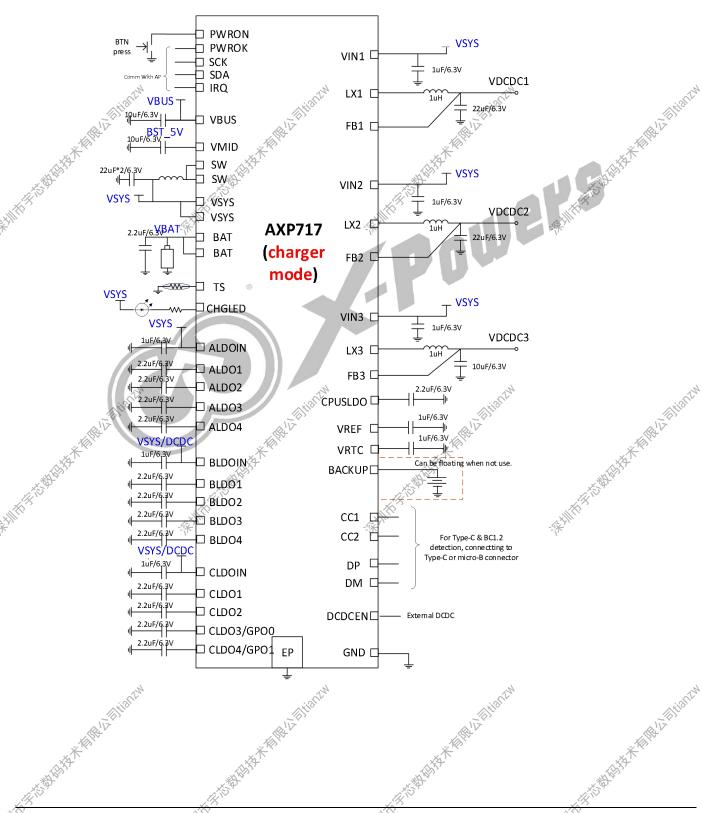
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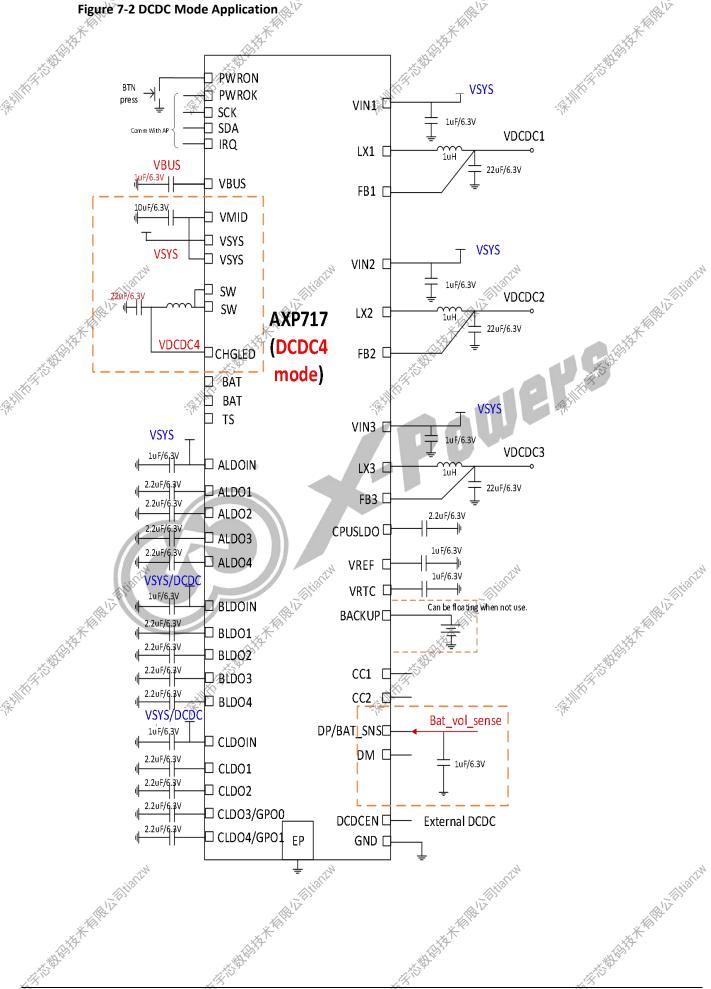
7 Application Information

7.1 Typical Application

Figure 7-1 Charger Mode Application









8 Package, Carrier, Storage and Baking Information

8.1 Package

AXP717 package is QFN6*6, 52-pin. Figure 8-1 shows AXP717 package.

Figure 8-1 Package Information

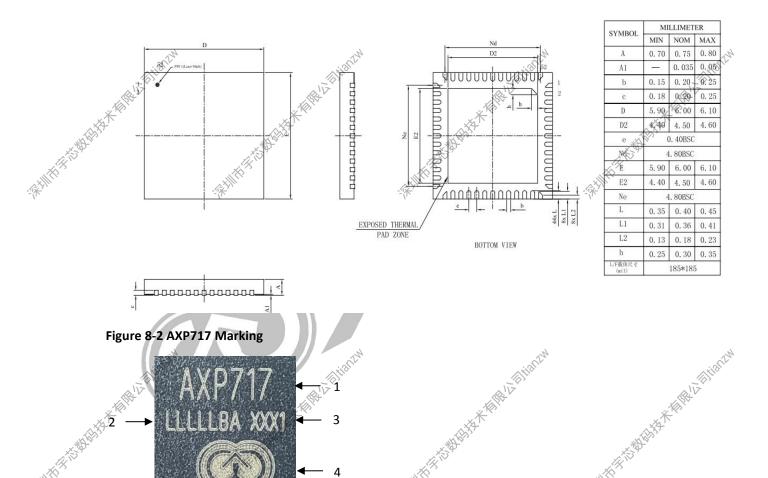


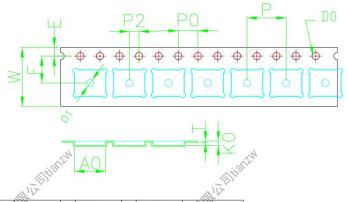
Table 8-1 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	AXP717	Product name	Fixed
2	LLLLLBA	Lot number	Dynamic
3	XXX1	Date code	Dynamic
4 A TO THE OWNER OF THE PARTY O	White The state of the state of	X-POWERS logo	Fixed
5	White dot	Package pin 1	Fixed



8.2 Carrier

Figure 8-3 AXP717 Tape Dimension Drawing



	WK	16.00±0.30	Р	8.00±0.10	A0	6.30±0.10	B0	6.30±0.10
8	8	0.00±0.10	P0	4.00±0.10	A1	,X	B1	
,7	Ε	1.75±0.10	P2	2.00±0.10			B2	
	F	7.50±0.10	DO	Ø1.50 ± 0.10	ΚO	0.85 20.05	K1	
	Τ	0.30±0.05	D1	ø1.50 ± 0:10		1/2 N		

Table 8-2 AXP717 Packing Quantity Information

Туре	Quantity	Part Number
Tape	3000pcs/Tape	AXP717

8.3 Storage

8.3.1 Moisture Sensitivity Level(MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factor floor longer than a high MSL device sample. ALL MSL are defined in the following table.

Table 8-3 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30℃/85%RH
2	1 year	≤30°C/60%RH
2a	4 weeks	≤30℃/60%RH
3 wishtin	168 hours	≤30°C/60%RH
4	72 hours	≤30°C/60%RH
5	48 hours	≤30℃/60%RH



5a	24 hours		≰30°C/60%RH	THE LEVEL TO SERVICE THE PROPERTY OF THE PROPE
6	Time on Label(TOL)	THE PARTY OF THE P	≤30°C/60%RH	TENTA TO

AXP717 device samples are classified as MSL3.

8.3.2 Bagged Storage Conditions

The shelf life of AXP717 are defined in the following table.

Table 8-4 Bagged Storage Conditions

Packing mode	Vac	cuum packing		
Storage temperature	20°	℃~26°C	.4	
Storage humidity	409	%~60%RH	Attanla	
Shelf life	6 m	nonths	A THE W	THE IT

8.3.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration of AXP717 is as follows

Table 8-5 Out-of-bag Duration

Storage temperature	20°C~26°C
Storage humidity	40%~60%RH
Moisture Sensitivity Level(MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, please refer to the latest IPC/JEDEC J-STD-020C.

8.4 Baking

It is not necessary to bake AXP717 if the conditions specified in Section 8.4.2 and Section 8.4.3 have not been exceeded. It is necessary to bake AXP717 if any condition specified in Section 8.4.2 and Section 8.4.3 have been exceeded.

Table 8-6 Baking Conditions

Surrounding	Condition	Note
Nitrogen	Tray: 125 ℃/8 hours Recommended condition. It is recommended	
active.	Tape: 60°C/72 hours	once, no more than three times.

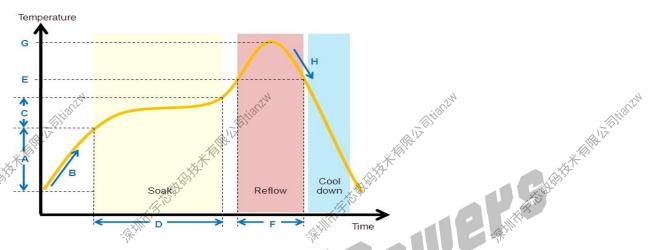


9 Reflow Profile

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste.

The following figure shows the typical reflow profile of AXP717 device sample.

Figure 9-1 AXP717 Typical Reflow Profile



Reflow profile conditions of AXP717 device sample is given in the following table.

Table 9-1 AXP717 Reflow Profile Conditions

	QTI typical SMT reflow profile conditions (for reference only)		
	Step	Reflow condition	
Faultsamout	N2 purge reflow usage (yes/no)	Yes, N2 purge used	
Environment	If yes, O2 ppm level	02 < 1500 ppm	
A A	Preheat ramp up temperature range	25°C -> 150°C	
В	Preheat ramp up rate	1.5~2.5 ℃ /sec	
C	Soak temperature range	150°C -> 190°C	
D A	Soak time	80~110 sec	
E	Liquidus temperature	217°C	
F	Time above liquidus	60-90 sec	
G	Peak temperature	240-250℃	
Н	Cool down temperature rate	≤4°C /sec	



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