



AMOLED driver IC

Jan. 2009
VER 1.1

TL2796

**960-channel source driver with power circuit
for 16M colors gate-IC-less AMOLED with PenTile Layout**

Tomato LSI Inc.

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TL2796

**960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout**

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1. FEATURE

- 480-RGB x 800-dot Gate-IC-less display controller/driver IC for 16M color(960ch-source driver with PenTile Layout)
- **Serial interface**
 - 3-Pin Serial Peripheral Interface
 - 4-Pin Serial Peripheral Interface
- **External Interface for Motion picture display(RGB Interface)**
 - 16/18/24-bit RGB Interface(VSYNC, HSYNC, ENABLE, DOTCLK, DB[23:0])
- **Various color-display control function**
 - 16,777,216 colors can be displayed at the same time (R/G/B separated gamma adjustment included)
 - 262,144 colors can be displayed
 - 65,536 colors, 8 colors can be displayed
- **Display function**
 - Support 480x800, 480x854 and 480x864 display resolution (PenTile RGBG layout)
 - Provide Gate driver control signal for AMOLED
 - Support Source data shift direction select
 - Operating frequency up to 33Mhz
 - Partial display function for low power consumption
- **Low-power operation supports:**
 - Power saving function (standby mode)
- **Operating voltage**

Applying voltage

 - IOVCC = 1.65 to 3.3V (interface I/O power supply)
 - VCC = 2.4 to 3.3V (internal logic power supply)
 - VCI = 2.5 to 3.3V (analogue power supply)

Generating voltage

 - VCI1OUT = Internal regulated voltage of VCI
 - VLOUT1 = 2 x VCI1OUT
 - VREG2OUT ≥ 4.5V @VCI = 2.8V (TYP)
 - VREG1OUT = 4.2V @VCI = 2.8V (TYP)
 - VLOUT2 = 3, 4 x VCI1OUT → VGH (4.6 ~ 6.0V)
 - VLOUT3 = -3, -4 x VCI1OUT → VGL (-7.8 ~ -6.4V)
 - VINT = -3.0 ~ -1.25V

Panel driving output

 - S1 to S960 : V0 to V255 grayscale
- **Gate-less signal** : VGH to VGL level

2. PIN DESCRIPTION

POWER PIN DESCRIPTION

| Signal | I/O | Connected to | Function | Unused pins |
|--------------------------|-----|-----------------------------|--|-------------|
| VCC | - | Power supply | Power supply for internal logic regulator circuit. VCC = 2.4 to 3.3V | - |
| IOVCC | - | Power supply | Supply with the power supply voltage for interface I/O pins (IM1-0, RESETB, CSB, RS, SCL, VSYNC, HSYNC, DOTCLK, ENABLE, DB23-0, SDI). IOVCC = 1.65 to 3.3V | - |
| VSS IOVSS | - | Power supply | System ground. VSS1 = Logic VSS, VSS2 = Oscillator VSS, VSS3 = Source driver VSS, VSS4 = Power VSS IOVSS = IO pad VSS. | - |
| VCCL | I/O | Capacitor for stabilization | Output from internal logic regulated voltage. Connect to a stabilizing capacitor. | - |
| VCI | I | Power supply | Power supply Analog circuit. An internal reference power supply for VCI1OUT. Connect a external voltage power supply(2.5 to 3.3V) | - |
| VCI1OUT | I/O | Capacitor for stabilization | Basic supply voltage for DCDC converter | |
| VLOUT1 | I/O | Capacitor for stabilization | Direct output voltage of the step up circuit 1. VLOUT1 = VCI1OUT X 2 | - |
| VLOUT2 | I/O | Capacitor for stabilization | Direct positive output voltage of the step up circuit 2 | - |
| VLOUT3 | I/O | Capacitor for stabilization | Direct negative output voltage of the step up circuit 2 | - |
| VGH | I/O | Capacitor for stabilization | Regulated gate driver voltage. | - |
| VGL | I/O | Capacitor for stabilization | Regulated gate driver voltage. | - |
| VINT | I/O | Capacitor for stabilization | Regulated panel pre-charge voltage. | - |
| C11+, C11- C12+, C12- | I/O | Step-up capacitor | Capacitor connection pin for the internal step up circuit 1. | - |
| C21+, C21- C22+, C22- | I/O | Step-up capacitor | Capacitor connection pin for the internal step up circuit 2. Connect a capacitor according to the step up magnification. | - |
| VREG1OUT | I/O | Capacitor for stabilization | Basic reference voltage for gamma voltages | - |
| VREG2OUT | I/O | Capacitor for stabilization | Regulated internal supply voltage for gray scale and source driver. | - |
| REGOFF | I | VSS / VCC | Internal logic regulator control input pin. Low : Use internal logic regulator for logic voltage(VCCL) High : Use external voltage for logic voltage(VCCL) | VSS |
| VGS | I | VSS or external resistor | Reference level for grayscale voltage generating circuit. Connect to an external variable resistor when adjusting a level for panel. | - |
| VPP1 | I | Power supply | MTP power supply, VPP1=21V | VSS |
| VPP2 | I | Power supply | MTP power supply, VPP2=5V | VCI |
| VPP3 | I | Open | Unused pin | Open |
| EXT_MV | I | ELVDD | Test pin | Open |
| ATEST | O | Open | Test pin | Open |

INTERFACE PIN DESCRIPTION

| Signals | I/O | Functions | Unused pins | | | | | | | | | |
|---------|--------|--|-------------|--------|----------|-----|-----|-----------------------------------|-------|-----|-----------------------------------|---|
| IM1-0 | I | <div>Pins to select interfacing mode with MPU.</div> <table><tr><th>IM1</th><th>IM0/ID</th><th>SPI mode</th></tr><tr><td>VSS</td><td>I/D</td><td>3-Pin Serial Peripheral Interface</td></tr><tr><td>IOVCC</td><td>VSS</td><td>4-Pin Serial Peripheral Interface</td></tr></table> <div>When 4-Pin serial Peripheral Interface is selected, IM0 pin is used for the device code ID setting(1: IOVCC, 0:VSS) Display data can't write or read via the Serial I/F, but instruction can write and device index can read.(SDO)</div> | IM1 | IM0/ID | SPI mode | VSS | I/D | 3-Pin Serial Peripheral Interface | IOVCC | VSS | 4-Pin Serial Peripheral Interface | - |
| IM1 | IM0/ID | SPI mode | | | | | | | | | | |
| VSS | I/D | 3-Pin Serial Peripheral Interface | | | | | | | | | | |
| IOVCC | VSS | 4-Pin Serial Peripheral Interface | | | | | | | | | | |
| CSB | I | Chip Select input signal. Low : the WVGA_IC is selected and accessible High : the WVGA_IC is not selected and not accessible Must be fixed to the high level while not used. | - | | | | | | | | | |
| RS | I | Select register. This signal uses a 4-Pin Serial Peripheral interface. Fix to the IOVCC or VSS level while use the 3-Pin Serial Peripheral interface. Low: Index/status, High: Control | VSS | | | | | | | | | |
| SCL | I | In Serial Peripheral Interface mode, serves as synchronizing clock signal. | - | | | | | | | | | |
| SDI | I | A serial data input(SDI) pin in SPI mode, Data are input on the rising edge of the SCL signal. | - | | | | | | | | | |
| SDO | O | For the bus interface above, unused pins must be floating. For a clock-synchronous serial interface, serves as the serial instruction data output pin (SDO). Output is from the falling edge of the SCL signal. | Open | | | | | | | | | |
| ENABLE | I | Data enable signal for RGB interface. Low : Valid (It is possible to access) High: Invalid (It is not possible to access) ENABLE signal inverts the polarity according to the EPL bit setting. Must be fixed to inactive level when not used. Note : 1. EPL : Bit in Driver Output Control register (R01h) 2. ENABLE : In the case of low active (default) | - | | | | | | | | | |
| VSYNC | I | Synchronous signal of frame. Low active : when VSPL = 0 High active : when VSPL = 1 VSPL: Bit in drive Output Control Register (R01h). Must be fixed to inactive level when not used. | - | | | | | | | | | |

| | | | |
|--------|---|---|------|
| HSYNC | I | Synchronous signal of line. Low active : when HSPL = 0 High active: when HSPL = 1 HSPL: Bit in drive Output Control Register (R01h). Must be fixed to inactive level when not used. | - |
| DOTCLK | I | Dot-clock signal. Data is read on the rising edge of this signal when DPL = 0 Data is read on the falling edge of this signal when DPL = 1 Must be fixed to inactive level when not used. | - |
| DB23-0 | I | Data bus. - 16M colors : DB23-0.(RGB 888) - 262K colors : DB23-18, DB15-10, DB7-2.(RGB 666) - 65K colors : DB23-19, DB15-10, DB7-3.(RGB 565) Unused pins must be connected to the IOVCC or VSS level. | VSS |
| FSYNC | O | Outputs a frame head pulse. (Amplitude is IOVCC to VSS). | Open |
| RESETB | I | Reset pin. Initializes the TL2796 when low. Must be reset after power-on. | - |

DISPLAY PIN DESCRIPTION

| Signals | I/O | Functions |
|----------|-----|--|
| S1~S960 | O | Source driver output pins. |
| FLM | O | Gate-less signal for AMOLED. |
| SFTCLK | O | |
| SFTCLKB | O | |
| SCLK1 | O | |
| SCLK2 | O | |
| EM_FLM | O | |
| EM_CLK1 | O | |
| EM_CLK1B | O | |
| EM_CLK2 | O | |
| EM_CLK2B | O | |
| ESR | O | |
| ELVDDON | O | ELVDD DC/DC converter ON/OFF control. (Amplitude is VCI to VSS). |

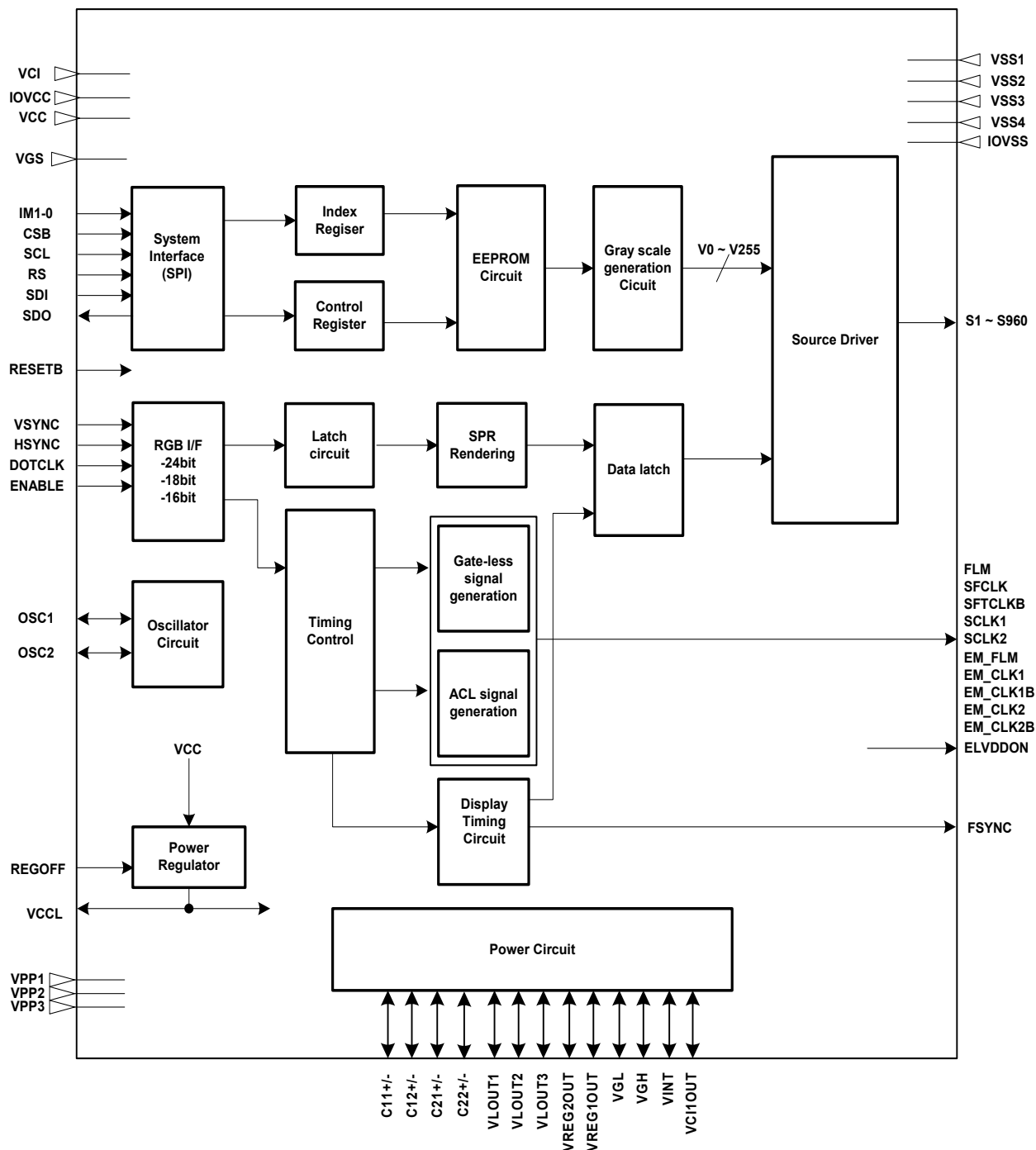
OSCILLATOR PIN DESCRIPTION

| Signals | I/O | Functions |
|------------|-----|---|
| OSC1/ OSC2 | I/O | Use an internal resistor for R-C oscillation. When input the clock from outside, input to OSC1, and open OSC2. |

DUMMY PIN DESCRIPTION

| Signals | I/O | Functions |
|------------------|-----|--|
| DUMS1 DUMS960 | O | Source channel output pads. Leave open. |
| IOVCCDUM | - | Use to fix the electric potential of unused interfaces. Leave open when not used. |
| IOVSSDUM | - | Use to fix the electric potential of unused interfaces. Leave open when not used. |
| DUMMYR1/2/3 | - | Short-circuit within the LSI for measuring COG connection resistance. DUMMYR1 – DUMMYR2 : short-circuit |
| DUMMY | - | Input or output dummy pads. Leave open. |

3. BLOCK DIAGRAM



4. INTRODUCTION

The TL2796 is a 960 channel output Source driver with built in Power circuit and Gray scale with PenTile Layout for 16M colors AMOLED panel. This IC can display to a maximum of 480RGB x 800dot (WVGA) graphics on 16M colors with TL2796.

As a system interface, the TL2796 has high speed Serial Peripheral Interface. The TL2796 can display a moving picture with 24/18/16 bits RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE and DB23-0).

The TL2796 is suitable for medium mobile products as smart phone corresponding to WWW browser, a PDA, PMP and display module for any other portable system.

5. FUNCTIONAL DESCRIPTION

TL2796 only support Serial Peripheral Interface (SPI) for instruction transmission and display data transmission can only write via the RGB interface.

5-1. Instruction Write/Read

TL2796 is enabling to instruction writing by selecting IM1-0 pin

| IM1 | IM0/ID | SPI mode |
|-------|--------|-----------------------------------|
| VSS | I/D | 3-Pin Serial Peripheral Interface |
| IOVCC | VSS | 4-Pin Serial Peripheral Interface |

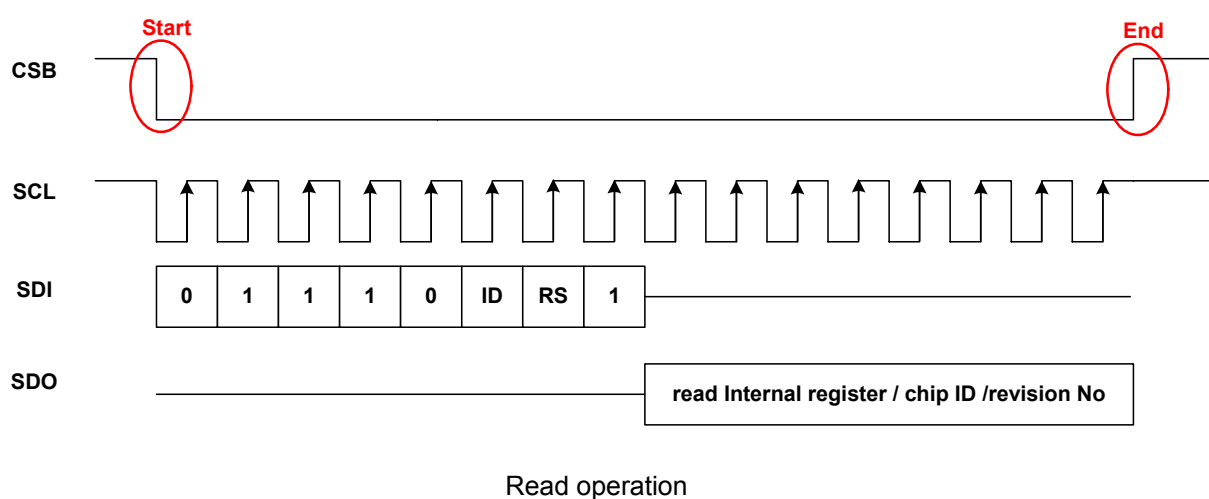
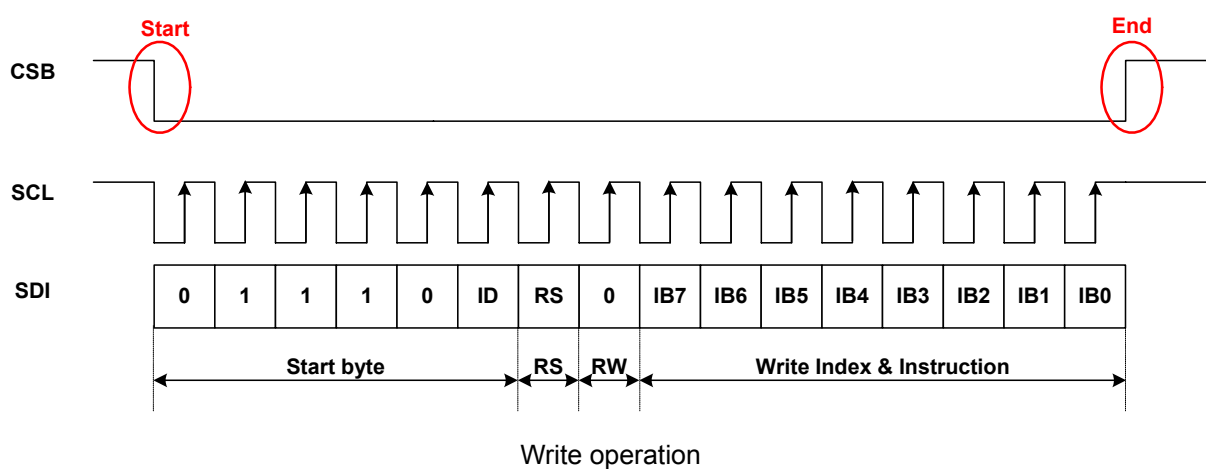
- 3-Pin Serial Peripheral Interface

| Start Byte | | Operation |
|------------|-----|-----------------------------------|
| RS | R/W | |
| 0 | 0 | Writing an index to IR. |
| 0 | 1 | Read chip Index & revision number |
| 1 | 0 | Writing into control register. |
| 1 | 1 | Read internal register. |

Start Byte Format

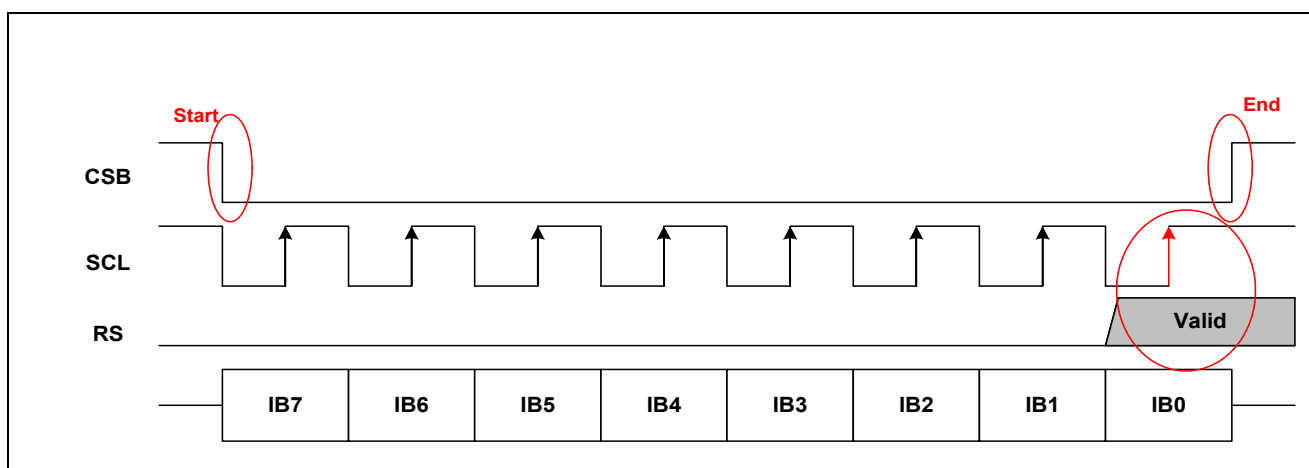
| Transmitted bits | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|-------------------|--------------------|----------------|---|---|---|---|----|-----|-----|
| Start byte format | Transmission start | Device ID code | | | | | | RS | R/W |
| | | 0 | 1 | 1 | 1 | 0 | ID | 0/1 | 0/1 |

Note 1) ID bit is selected with the IM0/ID pin.



- 4-Pin Serial Peripheral Interface

| RS | Operation |
|----|--------------------------------|
| 0 | Writing an index to IR. |
| 1 | Writing into control register. |

**5-2. Display data write (RGB I/F)**

The following interfaces are available as external display interface (RGB I/F). It is determined by setting bits of CM1-0.

| CM1 | CM0 | RGB Interface | Color mode | DB Pin |
|-----|-----|----------------------------|------------|---------------------|
| 0 | 0 | 24-bit RGB interface | 16M | DB23-0 |
| 0 | 1 | 18-bit RGB interface | 262K | DB23-18, 15-10, 7-2 |
| 1 | 0 | 16-bit RGB interface | 65K | DB23-19, 15-10, 7-3 |
| 1 | 1 | 24/18/16-bit RGB interface | 8 | DB23, 16, 7 |

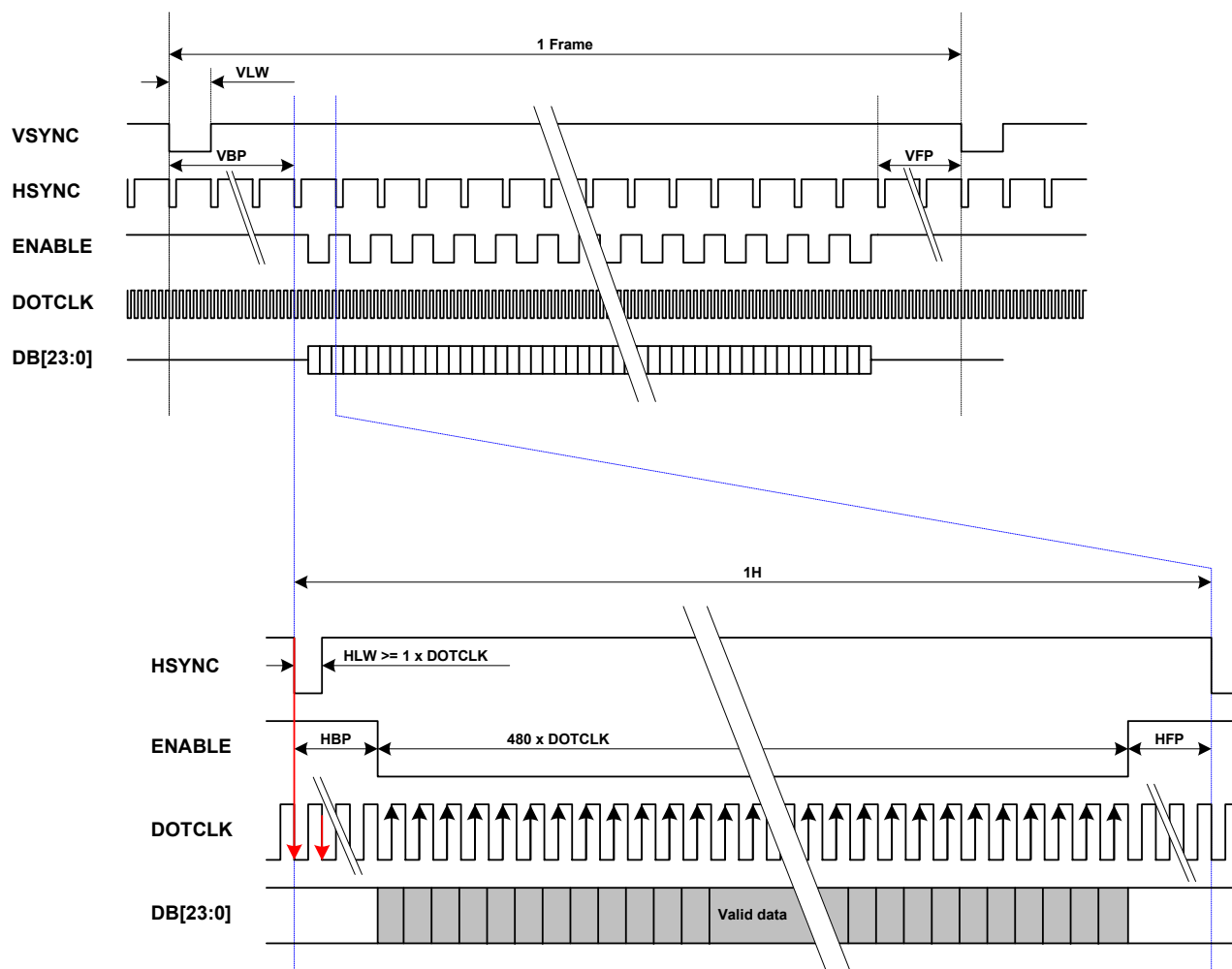
Note) When setting CM1-0 = "11", all data bits about R, G and B internally connected to MSB of each.

- ENABLE signals

The operation of "ENABLE" is shown below. ENABLE signal alone doesn't mean the updated address with writing data. "EPL" bit can switch the polarity of "ENABLE" signal.

| EPL | ENABLE | Display data |
|-----|--------|--------------|
| 0 | 0 | Valid |
| | 1 | Invalid |
| 1 | 0 | Invalid |
| | 1 | Valid |

- RGB interface timing



24 / 18 / 16-bit RGB interface timing

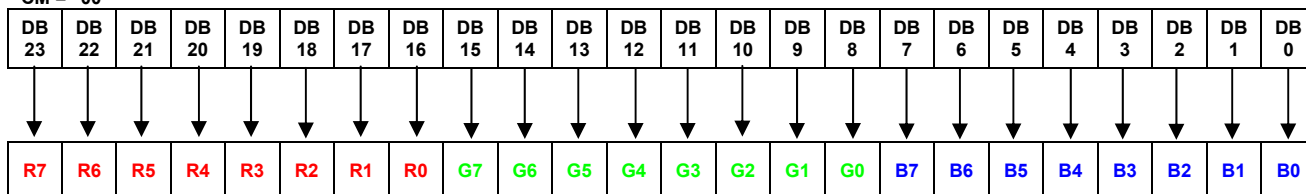
VLW: The period in which VSYNC is "Low" level. ($VLW \geq 1 \times \text{DOTCLK}$)
 HLW: The period in which HSYNC is "Low" level. ($HLW \geq 1 \times \text{DOTCLK}$)
 VBP: Vertical Back Porch. ($VBP \geq 4 \times \text{HSYNC}$)
 VFP: Vertical Front Porch. ($VFP \geq 4 \times \text{HSYNC}$)
 HBP: Horizontal Back Porch. ($HBP \geq 8 \times \text{DOTCLK}$)
 HFP: Horizontal Front Porch. ($HFP \geq 8 \times \text{DOTCLK}$)

Note) Signals (VSYNC, HSYNC and DB [23:0]) for RGB interface are latched by rising edge of DOTCLK.
 Therefore input of these signals (VSYNC, HSYNC and DB [23:0]) must be transition at falling edge of DOTCLK.

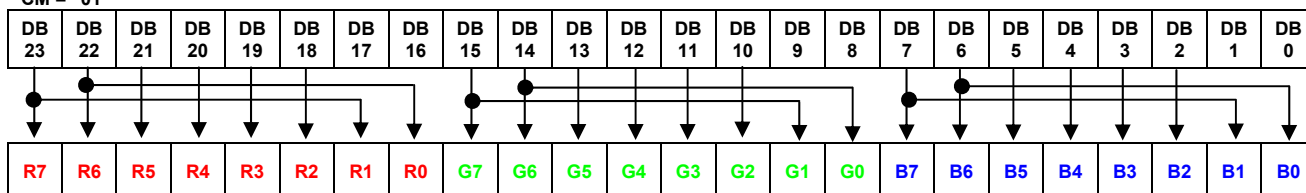
- RGB Assign

- 16M colors

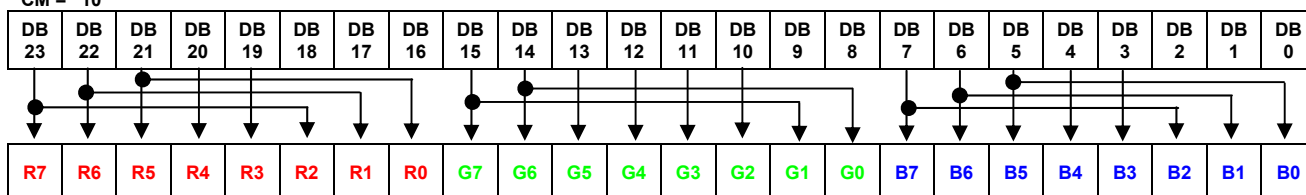
CM = "00"

- 262K colors

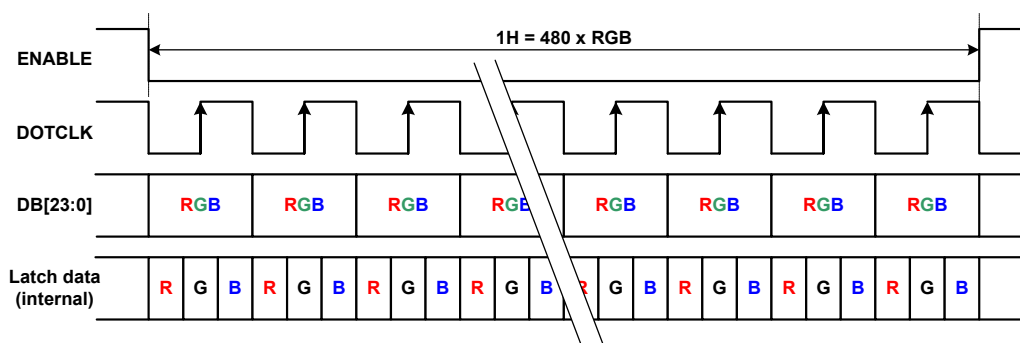
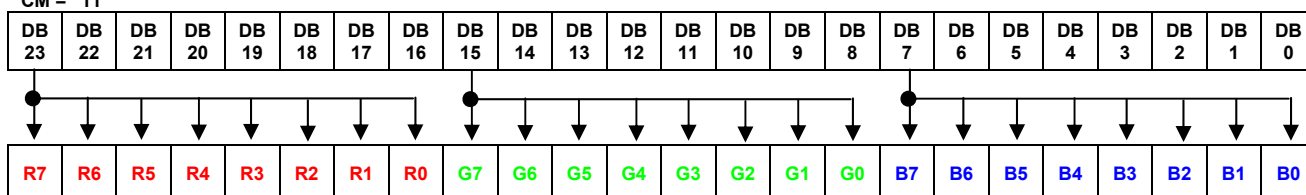
CM = "01"

- 65K colors

CM = "10"

- 8 colors

CM = "11"



5-3. Grayscale Voltage Generator

The grayscale voltage circuit generates OLED driving voltage that corresponds to the grayscale levels as specified in the grayscale gamma - adjusting resistor. 16,777,216 possible colors can be displayed at the same time.

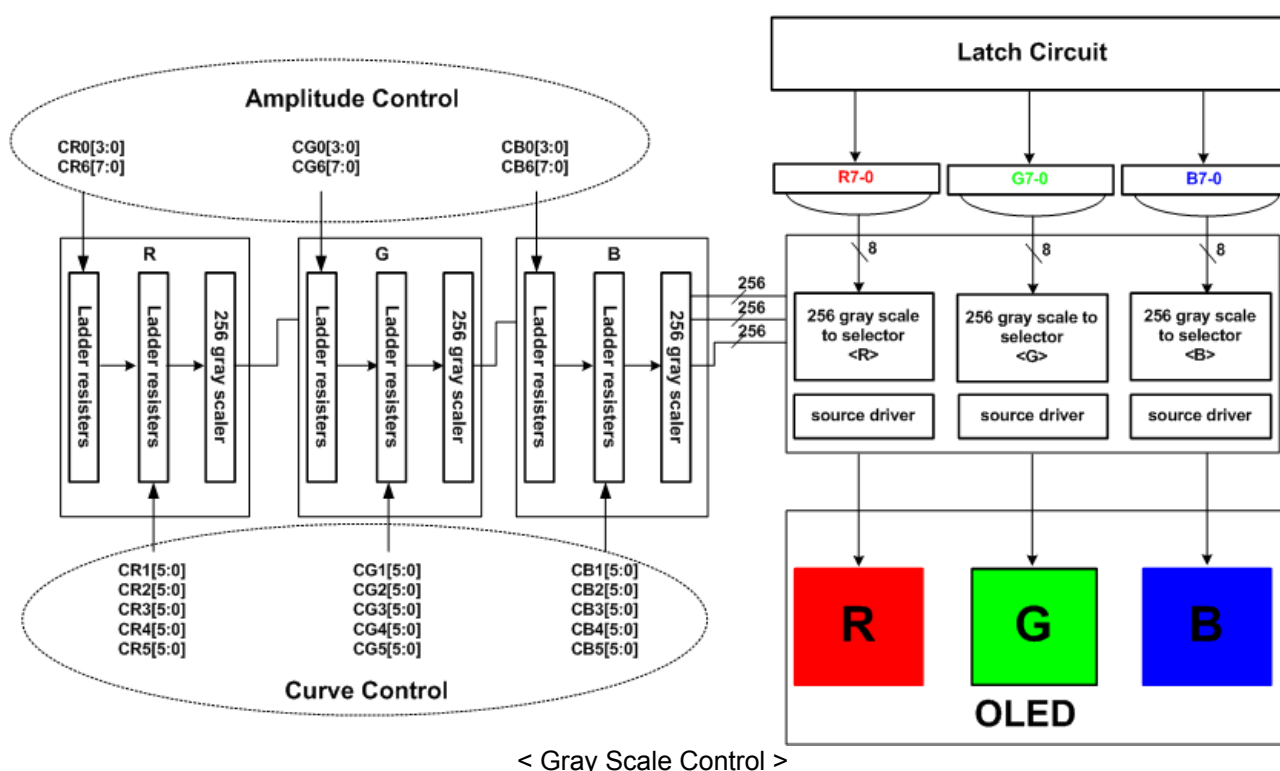
Gamma is set for R, G and B individually.

R, G, B Gamma Adjustment Function

TL2796 provides gamma adjustment function display 16M colors simultaneously.

The gamma adjustment is executed by the amplitude adjusting registers and curve adjusting registers.

Since those controls registers incorporate independent adjustment of the gamma function for R, G, B independently, it is highly possible that user determine the best appropriate configuration according to the trait of the display panel.

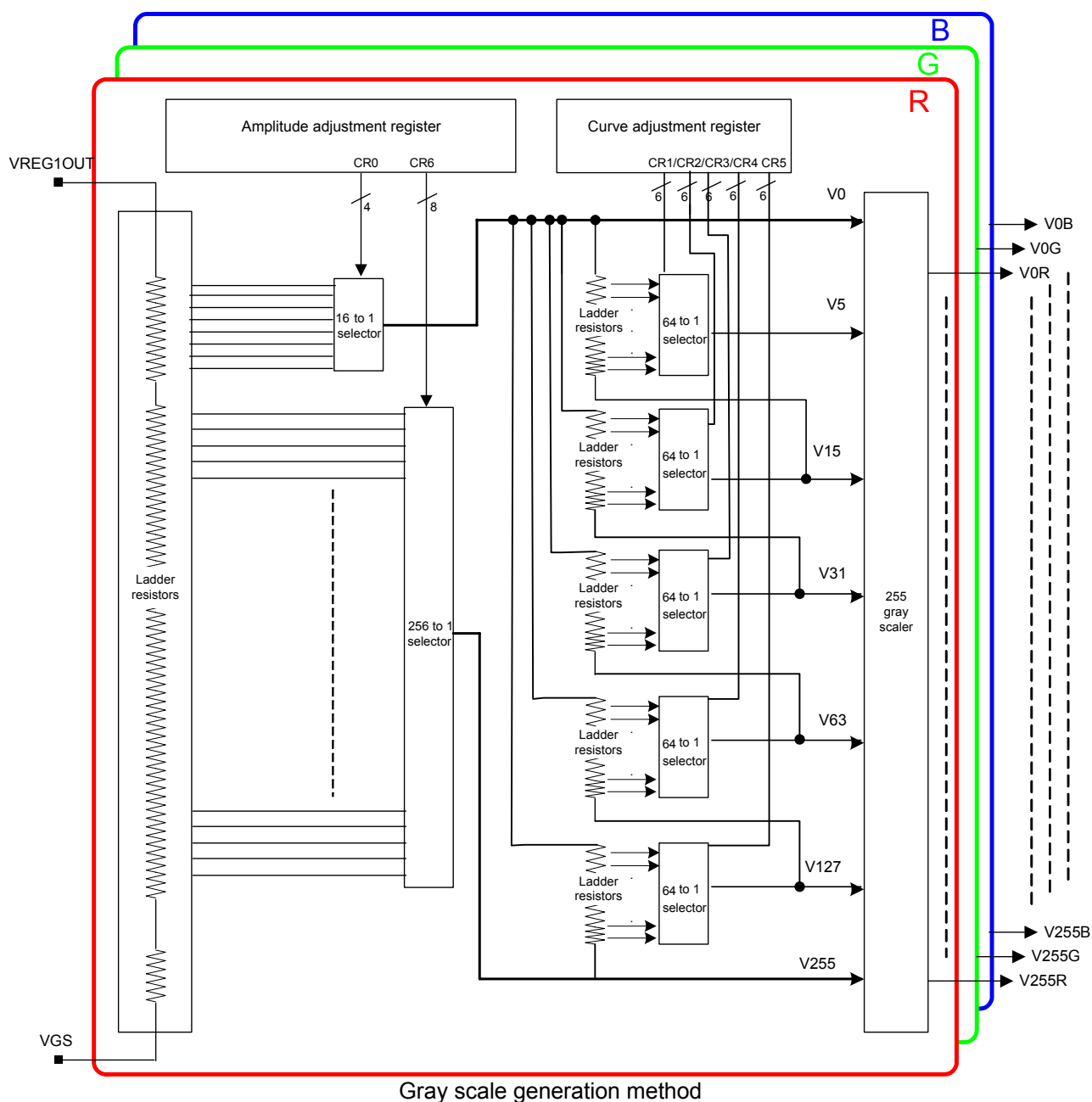


< Gray Scale Control >

Structure of Grayscale

Grayscale level can be determined by registers that adjust both amplitude and curve. Also, Period of each level is split by the internal ladder resistance and generates level between V0 to V255.

Amplitude adjusting part determines upper (V0) and lower (V255) bound voltage and curve adjusting part determines each 5 point (V5, V15, V31, V63, V127) voltages independently for flexible curve control.



Gray scale generation method

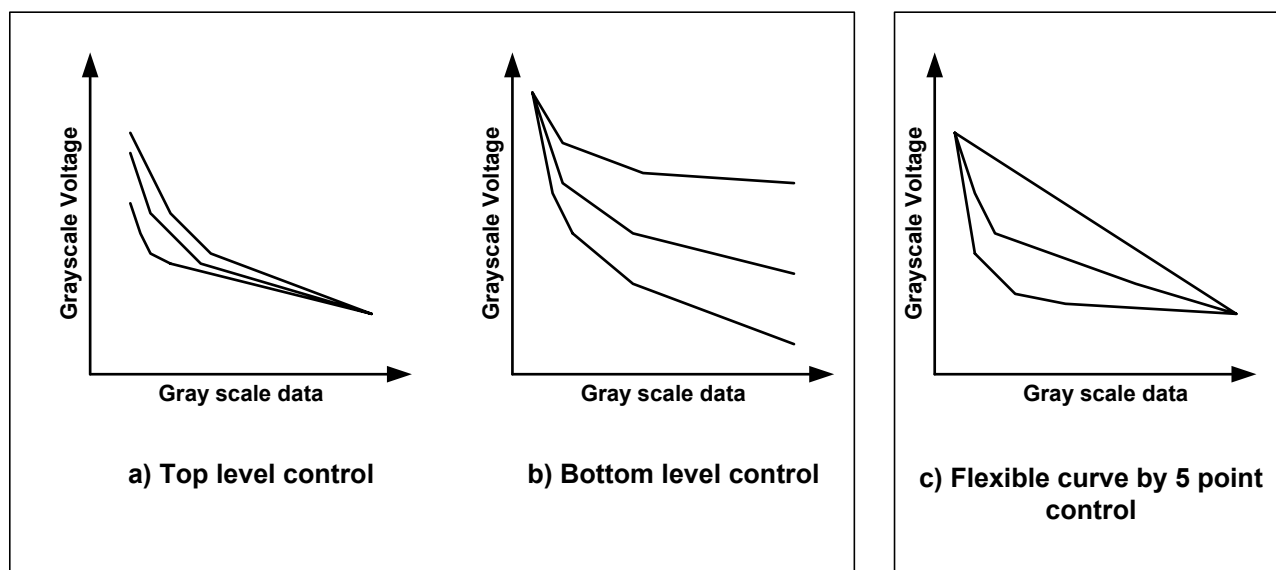
R,G,B Gamma Adjustment register

This block is the register to set up the grayscale voltage in accordance with the gamma specification of the panel.

This register can set up both amplitude and curve character of grayscale voltage respectively with corresponding bits as the function of grayscale number.

Each configuration can be made for R, G, B independently.

There shows the operation of each register below.



Amplitude adjustment

Curve adjustment

< The operation of Adjusting Register >

Amplitude Adjustment

This is the register for adjusting the amplitude of grayscale voltage.

The register for adjusting amplitude consists of two parts, one of which is for top level voltage (V0) and the other of which is for bottom level voltage (V255).

CR03-0, CG03-0 and CB03-0 registers control the top level voltage.

CR67-0, CG67-0 and CB67-0 registers control the bottom level voltage.

V0 and V255 are selected in divided voltage from ladder resistor strings between VGS and VREG1OUT.

Separate registers are prepared for R, G, B respectively.

| for TOP for BOTTOM | Content of configuration |
|-----------------------|--|
| CR0[3:0] | V0 Grayscale voltage adjusting for R |
| CG0[3:0] | V0 Grayscale voltage adjusting for G |
| CB0[3:0] | V0 Grayscale voltage adjusting for B |
| CR6[7:0] | V255 Grayscale voltage adjusting for R |
| CG6[7:0] | V255 Grayscale voltage adjusting for G |
| CB6[7:0] | V255 Grayscale voltage adjusting for B |

Amplitude adjusting register

| Resister Value CR0[3:0], CG0[3:0], CB0[3:0] | Formula of V0 |
|--|---------------------------------------|
| 0 0 0 0 | $VREG1OUT - (VREG1OUT \times 0/105)$ |
| 0 0 0 1 | $VREG1OUT - (VREG1OUT \times 1/105)$ |
| 0 0 1 0 | $VREG1OUT - (VREG1OUT \times 2/105)$ |
| 0 0 1 1 | $VREG1OUT - (VREG1OUT \times 3/105)$ |
| 0 1 0 0 | $VREG1OUT - (VREG1OUT \times 4/105)$ |
| 0 1 0 1 | $VREG1OUT - (VREG1OUT \times 5/105)$ |
| 0 1 1 0 | $VREG1OUT - (VREG1OUT \times 6/105)$ |
| 0 1 1 1 | $VREG1OUT - (VREG1OUT \times 7/105)$ |
| 1 0 0 0 | $VREG1OUT - (VREG1OUT \times 8/105)$ |
| 1 0 0 1 | $VREG1OUT - (VREG1OUT \times 9/105)$ |
| 1 0 1 0 | $VREG1OUT - (VREG1OUT \times 10/105)$ |
| 1 0 1 1 | $VREG1OUT - (VREG1OUT \times 11/105)$ |
| 1 1 0 0 | $VREG1OUT - (VREG1OUT \times 12/105)$ |
| 1 1 0 1 | $VREG1OUT - (VREG1OUT \times 13/105)$ |
| 1 1 1 0 | $VREG1OUT - (VREG1OUT \times 14/105)$ |
| 1 1 1 1 | $VREG1OUT - (VREG1OUT \times 15/105)$ |

Relationship between amplitude adjusting register and V0

| Register Value | Formula of V255 |
|-----------------------------------|--|
| CR6[7:0], CG6[7:0], CB6[7:0] | |
| 0 0 0 0 0 0 0 | $VREG1OUT - (VREG1OUT \times 51/255)$ |
| 0 0 0 0 0 0 1 | $VREG1OUT - (VREG1OUT \times 52/255)$ |
| 0 0 0 0 0 1 0 | $VREG1OUT - (VREG1OUT \times 53/255)$ |
| 0 0 0 0 0 1 1 | $VREG1OUT - (VREG1OUT \times 54/255)$ |
| 0 0 0 0 1 0 0 | $VREG1OUT - (VREG1OUT \times 55/255)$ |
| 0 0 0 0 1 0 1 | $VREG1OUT - (VREG1OUT \times 56/255)$ |
| 0 0 0 0 1 1 0 | $VREG1OUT - (VREG1OUT \times 57/255)$ |
| : | : |
| : | : |
| : | : |
| : | : |
| : | : |
| 1 0 1 0 1 1 0 0 | $VREG1OUT - (VREG1OUT \times 223/255)$ |
| 1 0 1 0 1 1 0 1 | $VREG1OUT - (VREG1OUT \times 224/255)$ |
| 1 0 1 0 1 1 1 0 | $VREG1OUT - (VREG1OUT \times 225/255)$ |
| 1 0 1 0 1 1 1 1 | $VREG1OUT - (VREG1OUT \times 226/255)$ |
| 1 0 1 1 0 0 0 0 | $VREG1OUT - (VREG1OUT \times 227/255)$ |
| 1 0 1 1 0 0 0 1 | $VREG1OUT - (VREG1OUT \times 228/255)$ |
| 1 0 1 1 0 0 1 0 | $VREG1OUT - (VREG1OUT \times 229/255)$ |
| 1 0 1 1 0 0 1 1 ~ 1 1 1 1 1 1 1 1 | $VREG1OUT - (VREG1OUT \times 230/255)$ |

< Relationship between amplitude adjusting register and V255 >

Curve Adjustment Register

The curve adjusting register is for adjusting the characteristic curve of the grayscale voltage as the function of grayscale number.

The curve adjusting register also controls R, G, B independently like the amplitude adjusting register.

The curve adjusting register is to make suitable adjustment of the grayscale curve.

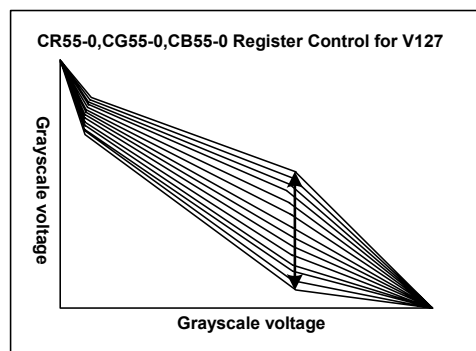
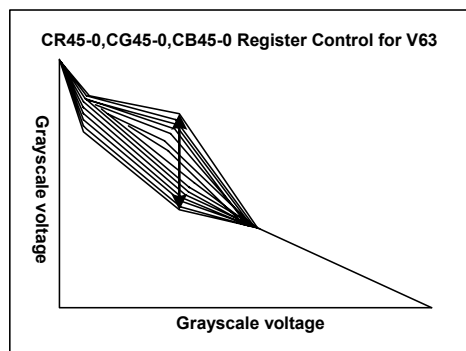
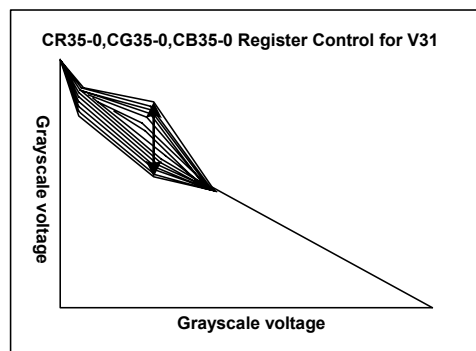
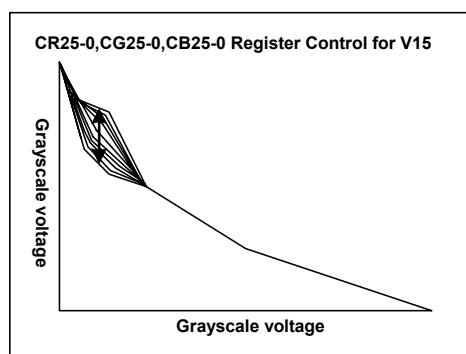
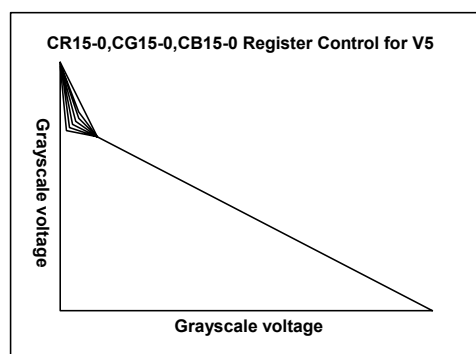
To accomplish the adjustment, it controls the each 4 reference voltage by the 64 to 1 selector.

The 64 –level reference voltage generated from the ladder resistor strings between V0 and V255.

The register for adjusting curve consists of 5 reference points – V5, V15, V31, V63 and V127.

| for R | for G | for B | Content of configuration |
|----------|----------|----------|----------------------------|
| CR1[5:0] | CG1[5:0] | CB1[5:0] | Grayscale Voltage for V5 |
| CR2[5:0] | CG2[5:0] | CB2[5:0] | Grayscale Voltage for V15 |
| CR3[5:0] | CG3[5:0] | CB3[5:0] | Grayscale Voltage for V31 |
| CR4[5:0] | CG4[5:0] | CB4[5:0] | Grayscale Voltage for V63 |
| CR5[5:0] | CG5[5:0] | CB5[5:0] | Grayscale Voltage for V127 |

<Gamma Curve Adjusting Register >



< Gamma curve adjustment >

Curve Adjustment

Below appears the table indicating the relation between the value of this register and voltage-dividing ratio.

| Curve Point | Register | Data | Formula |
|-------------|----------------------------------|--------|-----------------------------------|
| V5 | CR1[5:0] CG1[5:0] CB1[5:0] | 000000 | $V0 - (V0 - V15) \times 51/128$ |
| | | 000001 | $V0 - (V0 - V15) \times 52/128$ |
| | | 000010 | $V0 - (V0 - V15) \times 53/128$ |
| | | : | : |
| | | : | : |
| | | : | : |
| | | 111101 | $V0 - (V0 - V15) \times 112/128$ |
| | | 111110 | $V0 - (V0 - V15) \times 113/128$ |
| | | 111111 | $V0 - (V0 - V15) \times 114/128$ |
| V15 | CR2[5:0] CG2[5:0] CB2[5:0] | 000000 | $V0 - (V0 - V31) \times 58/128$ |
| | | 000001 | $V0 - (V0 - V31) \times 59/128$ |
| | | 000010 | $V0 - (V0 - V31) \times 60/128$ |
| | | : | : |
| | | : | : |
| | | : | : |
| | | 111101 | $V0 - (V0 - V31) \times 119/128$ |
| | | 111110 | $V0 - (V0 - V31) \times 120/128$ |
| | | 111111 | $V0 - (V0 - V31) \times 121/128$ |
| V31 | CR3[5:0] CG3[5:0] CB3[5:0] | 000000 | $V0 - (V0 - V63) \times 64/128$ |
| | | 000001 | $V0 - (V0 - V63) \times 65/128$ |
| | | 000010 | $V0 - (V0 - V63) \times 66/128$ |
| | | : | : |
| | | : | : |
| | | : | : |
| | | 111101 | $V0 - (V0 - V63) \times 125/128$ |
| | | 111110 | $V0 - (V0 - V63) \times 126/128$ |
| | | 111111 | $V0 - (V0 - V63) \times 127/128$ |
| V63 | CR4[5:0] CG4[5:0] CB4[5:0] | 000000 | $V0 - (V0 - V127) \times 64/128$ |
| | | 000001 | $V0 - (V0 - V127) \times 65/128$ |
| | | 000010 | $V0 - (V0 - V127) \times 66/128$ |
| | | : | : |
| | | : | : |
| | | : | : |
| | | 111101 | $V0 - (V0 - V127) \times 125/128$ |
| | | 111110 | $V0 - (V0 - V127) \times 126/128$ |
| | | 111111 | $V0 - (V0 - V127) \times 127/128$ |
| V127 | CR5[5:0] CG5[5:0] CB5[5:0] | 000000 | $V0 - (V0 - V255) \times 64/128$ |
| | | 000001 | $V0 - (V0 - V255) \times 65/128$ |
| | | 000010 | $V0 - (V0 - V255) \times 66/128$ |
| | | : | : |
| | | : | : |
| | | : | : |
| | | 111101 | $V0 - (V0 - V255) \times 125/128$ |
| | | 111110 | $V0 - (V0 - V255) \times 126/128$ |
| | | 111111 | $V0 - (V0 - V255) \times 127/128$ |

< Relationship between value of curve adjusting register and voltage-dividing ratio >

Gray scale level output Voltage

Below appears the table indicating the relation between the display data value and output voltage value.

Grayscale Output Voltage Formula

| Gray data | Output value | Gray data | Output value | Gray data | Output value |
|-----------|--------------------------------------|-----------|--|-----------|---|
| 0 | V0 | 44 | $V43 - \{(V43 - V47) \times 1/4\}$ | 88 | $V87 - \{(V87 - V91) \times 1/4\}$ |
| 1 | $V0 - \{(V0 - V5) \times 1/5\}$ | 45 | $V43 - \{(V43 - V47) \times 2/4\}$ | 89 | $V87 - \{(V87 - V91) \times 2/4\}$ |
| 2 | $V0 - \{(V0 - V5) \times 2/5\}$ | 46 | $V43 - \{(V43 - V47) \times 3/4\}$ | 90 | $V87 - \{(V87 - V91) \times 3/4\}$ |
| 3 | $V0 - \{(V0 - V5) \times 3/5\}$ | 47 | $V63 + \{(V31 - V63) \times 16/32\}$ | 91 | $V127 + \{(V63 - V127) \times 18/32\}$ |
| 4 | $V0 - \{(V0 - V5) \times 4/5\}$ | 48 | $V47 - \{(V47 - V51) \times 1/4\}$ | 92 | $V91 - \{(V91 - V95) \times 1/4\}$ |
| 5 | V5 | 49 | $V47 - \{(V47 - V51) \times 2/4\}$ | 93 | $V91 - \{(V91 - V95) \times 2/4\}$ |
| 6 | $V5 - \{(V5 - V10) \times 1/5\}$ | 50 | $V47 - \{(V47 - V51) \times 3/4\}$ | 94 | $V91 - \{(V91 - V95) \times 3/4\}$ |
| 7 | $V5 - \{(V5 - V10) \times 2/5\}$ | 51 | $V63 + \{(V31 - V63) \times 12/32\}$ | 95 | $V127 + \{(V63 - V127) \times 16/32\}$ |
| 8 | $V5 - \{(V5 - V10) \times 3/5\}$ | 52 | $V51 - \{(V51 - V55) \times 1/4\}$ | 96 | $V95 - \{(V95 - V99) \times 1/4\}$ |
| 9 | $V5 - \{(V5 - V10) \times 4/5\}$ | 53 | $V51 - \{(V51 - V55) \times 2/4\}$ | 97 | $V95 - \{(V95 - V99) \times 2/4\}$ |
| 10 | $V15 + \{(V5 - V15) \times 5/8\}$ | 54 | $V51 - \{(V51 - V55) \times 3/4\}$ | 98 | $V95 - \{(V95 - V99) \times 3/4\}$ |
| 11 | $V10 - \{(V10 - V15) \times 1/5\}$ | 55 | $V63 + \{(V31 - V63) \times 8/32\}$ | 99 | $V127 + \{(V63 - V127) \times 14/32\}$ |
| 12 | $V10 - \{(V10 - V15) \times 2/5\}$ | 56 | $V55 - \{(V55 - V59) \times 1/4\}$ | 100 | $V99 - \{(V99 - V103) \times 1/4\}$ |
| 13 | $V10 - \{(V10 - V15) \times 3/5\}$ | 57 | $V55 - \{(V55 - V59) \times 2/4\}$ | 101 | $V99 - \{(V99 - V103) \times 2/4\}$ |
| 14 | $V10 - \{(V10 - V15) \times 4/5\}$ | 58 | $V55 - \{(V55 - V59) \times 3/4\}$ | 102 | $V99 - \{(V99 - V103) \times 3/4\}$ |
| 15 | V15 | 59 | $V63 + \{(V31 - V63) \times 4/32\}$ | 103 | $V127 + \{(V63 - V127) \times 12/32\}$ |
| 16 | $V15 - \{(V15 - V19) \times 1/4\}$ | 60 | $V59 - \{(V59 - V63) \times 1/4\}$ | 104 | $V103 - \{(V103 - V107) \times 1/4\}$ |
| 17 | $V15 - \{(V15 - V19) \times 2/4\}$ | 61 | $V59 - \{(V59 - V63) \times 2/4\}$ | 105 | $V103 - \{(V103 - V107) \times 2/4\}$ |
| 18 | $V15 - \{(V15 - V19) \times 3/4\}$ | 62 | $V59 - \{(V59 - V63) \times 3/4\}$ | 106 | $V103 - \{(V103 - V107) \times 3/4\}$ |
| 19 | $V31 + \{(V15 - V31) \times 24/32\}$ | 63 | V63 | 107 | $V127 + \{(V63 - V127) \times 10/32\}$ |
| 20 | $V16 - \{(V16 - V23) \times 1/4\}$ | 64 | $V63 - \{(V63 - V67) \times 1/4\}$ | 108 | $V107 - \{(V107 - V111) \times 1/4\}$ |
| 21 | $V16 - \{(V16 - V23) \times 2/4\}$ | 65 | $V63 - \{(V63 - V67) \times 2/4\}$ | 109 | $V107 - \{(V107 - V111) \times 2/4\}$ |
| 22 | $V16 - \{(V16 - V23) \times 3/4\}$ | 66 | $V63 - \{(V63 - V67) \times 3/4\}$ | 110 | $V107 - \{(V107 - V111) \times 3/4\}$ |
| 23 | $V31 + \{(V15 - V31) \times 16/32\}$ | 67 | $V127 + \{(V63 - V127) \times 30/32\}$ | 111 | $V127 + \{(V63 - V127) \times 8/32\}$ |
| 24 | $V23 - \{(V23 - V27) \times 1/4\}$ | 68 | $V67 - \{(V67 - V71) \times 1/4\}$ | 112 | $V111 - \{(V111 - V115) \times 1/4\}$ |
| 25 | $V23 - \{(V23 - V27) \times 2/4\}$ | 69 | $V67 - \{(V67 - V71) \times 2/4\}$ | 113 | $V111 - \{(V111 - V115) \times 2/4\}$ |
| 26 | $V23 - \{(V23 - V27) \times 3/4\}$ | 70 | $V67 - \{(V67 - V71) \times 3/4\}$ | 114 | $V111 - \{(V111 - V115) \times 3/4\}$ |
| 27 | $V31 + \{(V15 - V31) \times 8/32\}$ | 71 | $V127 + \{(V63 - V127) \times 28/32\}$ | 115 | $V127 + \{(V63 - V127) \times 6/32\}$ |
| 28 | $V27 - \{(V27 - V31) \times 1/4\}$ | 72 | $V71 - \{(V71 - V75) \times 1/4\}$ | 116 | $V115 - \{(V115 - V119) \times 1/4\}$ |
| 29 | $V27 - \{(V27 - V31) \times 2/4\}$ | 73 | $V71 - \{(V71 - V75) \times 2/4\}$ | 117 | $V115 - \{(V115 - V119) \times 2/4\}$ |
| 30 | $V27 - \{(V27 - V31) \times 3/4\}$ | 74 | $V71 - \{(V71 - V75) \times 3/4\}$ | 118 | $V115 - \{(V115 - V119) \times 3/4\}$ |
| 31 | V31 | 75 | $V127 + \{(V63 - V127) \times 26/32\}$ | 119 | $V127 + \{(V63 - V127) \times 4/32\}$ |
| 32 | $V31 - \{(V31 - V35) \times 1/4\}$ | 76 | $V75 - \{(V75 - V79) \times 1/4\}$ | 120 | $V119 - \{(V119 - V123) \times 1/4\}$ |
| 33 | $V31 - \{(V31 - V35) \times 2/4\}$ | 77 | $V75 - \{(V75 - V79) \times 2/4\}$ | 121 | $V119 - \{(V119 - V123) \times 2/4\}$ |
| 34 | $V31 - \{(V31 - V35) \times 3/4\}$ | 78 | $V75 - \{(V75 - V79) \times 3/4\}$ | 122 | $V119 - \{(V119 - V123) \times 3/4\}$ |
| 35 | $V63 + \{(V31 - V63) \times 28/32\}$ | 79 | $V127 + \{(V63 - V127) \times 24/32\}$ | 123 | $V127 + \{(V63 - V127) \times 2/32\}$ |
| 36 | $V35 - \{(V35 - V39) \times 1/4\}$ | 80 | $V79 - \{(V79 - V83) \times 1/4\}$ | 124 | $V123 - \{(V123 - V127) \times 1/4\}$ |
| 37 | $V35 - \{(V35 - V39) \times 2/4\}$ | 81 | $V79 - \{(V79 - V83) \times 2/4\}$ | 125 | $V123 - \{(V123 - V127) \times 2/4\}$ |
| 38 | $V35 - \{(V35 - V39) \times 3/4\}$ | 82 | $V79 - \{(V79 - V83) \times 3/4\}$ | 126 | $V123 - \{(V123 - V127) \times 3/4\}$ |
| 39 | $V63 + \{(V31 - V63) \times 24/32\}$ | 83 | $V127 + \{(V63 - V127) \times 22/32\}$ | 127 | V127 |
| 40 | $V39 - \{(V39 - V43) \times 1/4\}$ | 84 | $V83 - \{(V83 - V87) \times 1/4\}$ | 128 | $V127 - \{(V127 - V131) \times 1/4\}$ |
| 41 | $V39 - \{(V39 - V43) \times 2/4\}$ | 85 | $V83 - \{(V83 - V87) \times 2/4\}$ | 129 | $V127 - \{(V127 - V131) \times 2/4\}$ |
| 42 | $V39 - \{(V39 - V43) \times 3/4\}$ | 86 | $V83 - \{(V83 - V87) \times 3/4\}$ | 130 | $V127 - \{(V127 - V131) \times 3/4\}$ |
| 43 | $V63 + \{(V31 - V63) \times 20/32\}$ | 87 | $V127 + \{(V63 - V127) \times 20/32\}$ | 131 | $V255 + \{(V127 - V255) \times 31/32\}$ |

 TL2796

**960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout**

| Gray data | Output value | Gray data | Output value | Gray data | Output value |
|-----------|-------------------------------------|-----------|-------------------------------------|-----------|------------------------------------|
| 132 | $V131-\{(V131-V135) \times 1/4\}$ | 176 | $V175-\{(V175-V179) \times 1/4\}$ | 220 | $V219-\{(V219-V223) \times 1/4\}$ |
| 133 | $V131-\{(V131-V135) \times 2/4\}$ | 177 | $V175-\{(V175-V179) \times 2/4\}$ | 221 | $V219-\{(V219-V223) \times 2/4\}$ |
| 134 | $V131-\{(V131-V135) \times 3/4\}$ | 178 | $V175-\{(V175-V179) \times 3/4\}$ | 222 | $V219-\{(V219-V223) \times 3/4\}$ |
| 135 | $V255+\{(V127-V255) \times 30/32\}$ | 179 | $V255+\{(V127-V255) \times 19/32\}$ | 223 | $V255+\{(V127-V255) \times 8/32\}$ |
| 136 | $V135-\{(V135-V139) \times 1/4\}$ | 180 | $V179-\{(V179-V183) \times 1/4\}$ | 224 | $V223-\{(V223-V227) \times 1/4\}$ |
| 137 | $V135-\{(V135-V139) \times 2/4\}$ | 181 | $V179-\{(V179-V183) \times 2/4\}$ | 225 | $V223-\{(V223-V227) \times 2/4\}$ |
| 138 | $V135-\{(V135-V139) \times 3/4\}$ | 182 | $V179-\{(V179-V183) \times 3/4\}$ | 226 | $V223-\{(V223-V227) \times 3/4\}$ |
| 139 | $V255+\{(V127-V255) \times 29/32\}$ | 183 | $V255+\{(V127-V255) \times 18/32\}$ | 227 | $V255+\{(V127-V255) \times 7/32\}$ |
| 140 | $V139-\{(V139-V143) \times 1/4\}$ | 184 | $V183-\{(V183-V187) \times 1/4\}$ | 228 | $V227-\{(V227-V231) \times 1/4\}$ |
| 141 | $V139-\{(V139-V143) \times 2/4\}$ | 185 | $V183-\{(V183-V187) \times 2/4\}$ | 229 | $V227-\{(V227-V231) \times 2/4\}$ |
| 142 | $V139-\{(V139-V143) \times 3/4\}$ | 186 | $V183-\{(V183-V187) \times 3/4\}$ | 230 | $V227-\{(V227-V231) \times 3/4\}$ |
| 143 | $V255+\{(V127-V255) \times 28/32\}$ | 187 | $V255+\{(V127-V255) \times 17/32\}$ | 231 | $V255+\{(V127-V255) \times 6/32\}$ |
| 144 | $V143-\{(V143-V147) \times 1/4\}$ | 188 | $V187-\{(V187-V191) \times 1/4\}$ | 232 | $V231-\{(V231-V235) \times 1/4\}$ |
| 145 | $V143-\{(V143-V147) \times 2/4\}$ | 189 | $V187-\{(V187-V191) \times 2/4\}$ | 233 | $V231-\{(V231-V235) \times 2/4\}$ |
| 146 | $V143-\{(V143-V147) \times 3/4\}$ | 190 | $V187-\{(V187-V191) \times 3/4\}$ | 234 | $V231-\{(V231-V235) \times 3/4\}$ |
| 147 | $V255+\{(V127-V255) \times 27/32\}$ | 191 | $V255+\{(V127-V255) \times 16/32\}$ | 235 | $V255+\{(V127-V255) \times 5/32\}$ |
| 148 | $V147-\{(V147-V151) \times 1/4\}$ | 192 | $V191-\{(V191-V195) \times 1/4\}$ | 236 | $V235-\{(V235-V239) \times 1/4\}$ |
| 149 | $V147-\{(V147-V151) \times 2/4\}$ | 193 | $V191-\{(V191-V195) \times 2/4\}$ | 237 | $V235-\{(V235-V239) \times 2/4\}$ |
| 150 | $V147-\{(V147-V151) \times 3/4\}$ | 194 | $V191-\{(V191-V195) \times 3/4\}$ | 238 | $V235-\{(V235-V239) \times 3/4\}$ |
| 151 | $V255+\{(V127-V255) \times 26/32\}$ | 195 | $V255+\{(V127-V255) \times 15/32\}$ | 239 | $V255+\{(V127-V255) \times 4/32\}$ |
| 152 | $V151-\{(V151-V155) \times 1/4\}$ | 196 | $V195-\{(V195-V199) \times 1/4\}$ | 240 | $V239-\{(V239-V243) \times 1/4\}$ |
| 153 | $V151-\{(V151-V155) \times 2/4\}$ | 197 | $V195-\{(V195-V199) \times 2/4\}$ | 241 | $V239-\{(V239-V243) \times 2/4\}$ |
| 154 | $V151-\{(V151-V155) \times 3/4\}$ | 198 | $V195-\{(V195-V199) \times 3/4\}$ | 242 | $V239-\{(V239-V243) \times 3/4\}$ |
| 155 | $V255+\{(V127-V255) \times 25/32\}$ | 199 | $V255+\{(V127-V255) \times 14/32\}$ | 243 | $V255+\{(V127-V255) \times 3/32\}$ |
| 156 | $V155-\{(V155-V159) \times 1/4\}$ | 200 | $V199-\{(V199-V203) \times 1/4\}$ | 244 | $V243-\{(V243-V247) \times 1/4\}$ |
| 157 | $V155-\{(V155-V159) \times 2/4\}$ | 201 | $V199-\{(V199-V203) \times 2/4\}$ | 245 | $V243-\{(V243-V247) \times 2/4\}$ |
| 158 | $V155-\{(V155-V159) \times 3/4\}$ | 202 | $V199-\{(V199-V203) \times 3/4\}$ | 246 | $V243-\{(V243-V247) \times 3/4\}$ |
| 159 | $V255+\{(V127-V255) \times 24/32\}$ | 203 | $V255+\{(V127-V255) \times 13/32\}$ | 247 | $V255+\{(V127-V255) \times 2/32\}$ |
| 160 | $V159-\{(V159-V163) \times 1/4\}$ | 204 | $V203-\{(V203-V207) \times 1/4\}$ | 248 | $V247-\{(V247-V251) \times 1/4\}$ |
| 161 | $V159-\{(V159-V163) \times 2/4\}$ | 205 | $V203-\{(V203-V207) \times 2/4\}$ | 249 | $V247-\{(V247-V251) \times 2/4\}$ |
| 162 | $V159-\{(V159-V163) \times 3/4\}$ | 206 | $V203-\{(V203-V207) \times 3/4\}$ | 250 | $V247-\{(V247-V251) \times 3/4\}$ |
| 163 | $V255+\{(V127-V255) \times 23/32\}$ | 207 | $V255+\{(V127-V255) \times 12/32\}$ | 251 | $V255+\{(V127-V255) \times 1/32\}$ |
| 164 | $V163-\{(V163-V167) \times 1/4\}$ | 208 | $V207-\{(V207-V211) \times 1/4\}$ | 252 | $V251-\{(V251-V255) \times 1/4\}$ |
| 165 | $V163-\{(V163-V167) \times 2/4\}$ | 209 | $V207-\{(V207-V211) \times 2/4\}$ | 253 | $V251-\{(V251-V255) \times 2/4\}$ |
| 166 | $V163-\{(V163-V167) \times 3/4\}$ | 210 | $V207-\{(V207-V211) \times 3/4\}$ | 254 | $V251-\{(V251-V255) \times 3/4\}$ |
| 167 | $V255+\{(V127-V255) \times 22/32\}$ | 211 | $V255+\{(V127-V255) \times 11/32\}$ | 255 | V255 |
| 168 | $V167-\{(V167-V171) \times 1/4\}$ | 212 | $V211-\{(V211-V215) \times 1/4\}$ | | |
| 169 | $V167-\{(V167-V171) \times 2/4\}$ | 213 | $V211-\{(V211-V215) \times 2/4\}$ | | |
| 170 | $V167-\{(V167-V171) \times 3/4\}$ | 214 | $V211-\{(V211-V215) \times 3/4\}$ | | |
| 171 | $V255+\{(V127-V255) \times 21/32\}$ | 215 | $V255+\{(V127-V255) \times 10/32\}$ | | |
| 172 | $V171-\{(V171-V175) \times 1/4\}$ | 216 | $V215-\{(V215-V219) \times 1/4\}$ | | |
| 173 | $V171-\{(V171-V175) \times 2/4\}$ | 217 | $V215-\{(V215-V219) \times 2/4\}$ | | |
| 174 | $V171-\{(V171-V175) \times 3/4\}$ | 218 | $V215-\{(V215-V219) \times 3/4\}$ | | |
| 175 | $V255+\{(V127-V255) \times 20/32\}$ | 219 | $V255+\{(V127-V255) \times 9/32\}$ | | |

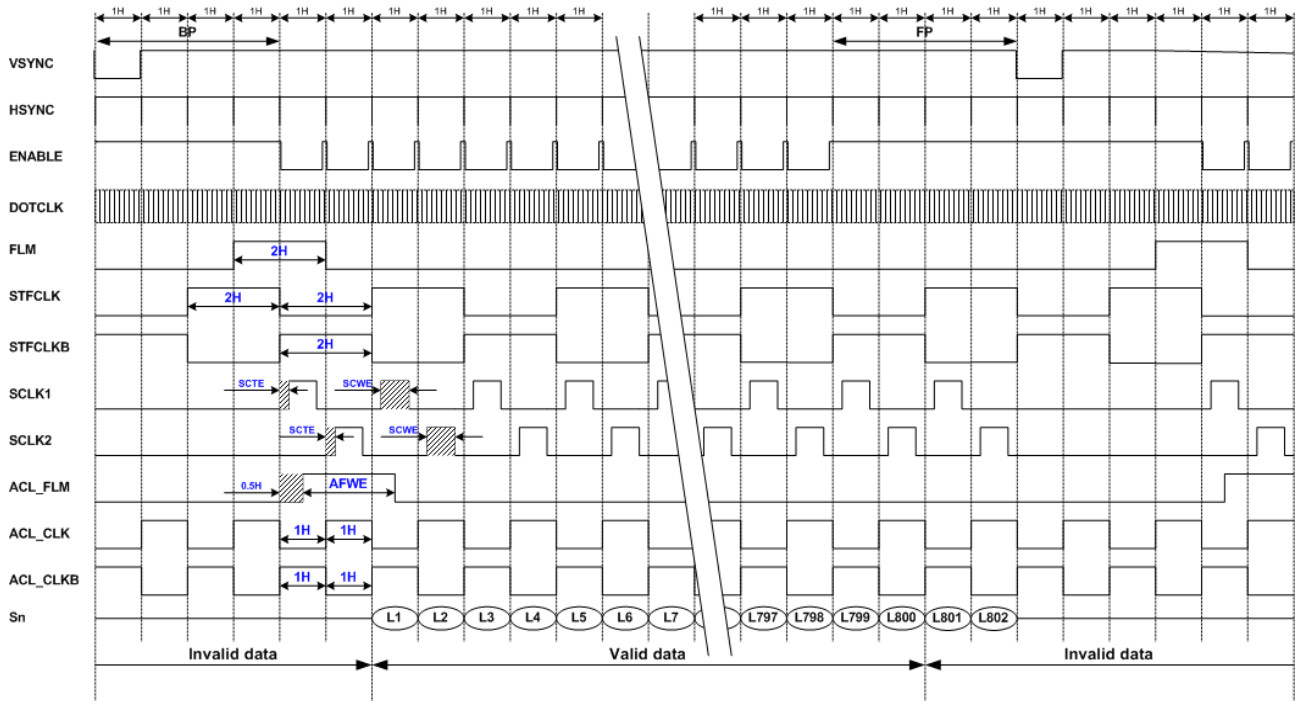
5-4. Panel Control

TL2796 outputs timing signals for controlling a panel with built-in gates. This IC has built-in level shifter for AMOLED panel. Output voltage level for high level is VGH voltage, for low level is VGL voltage.

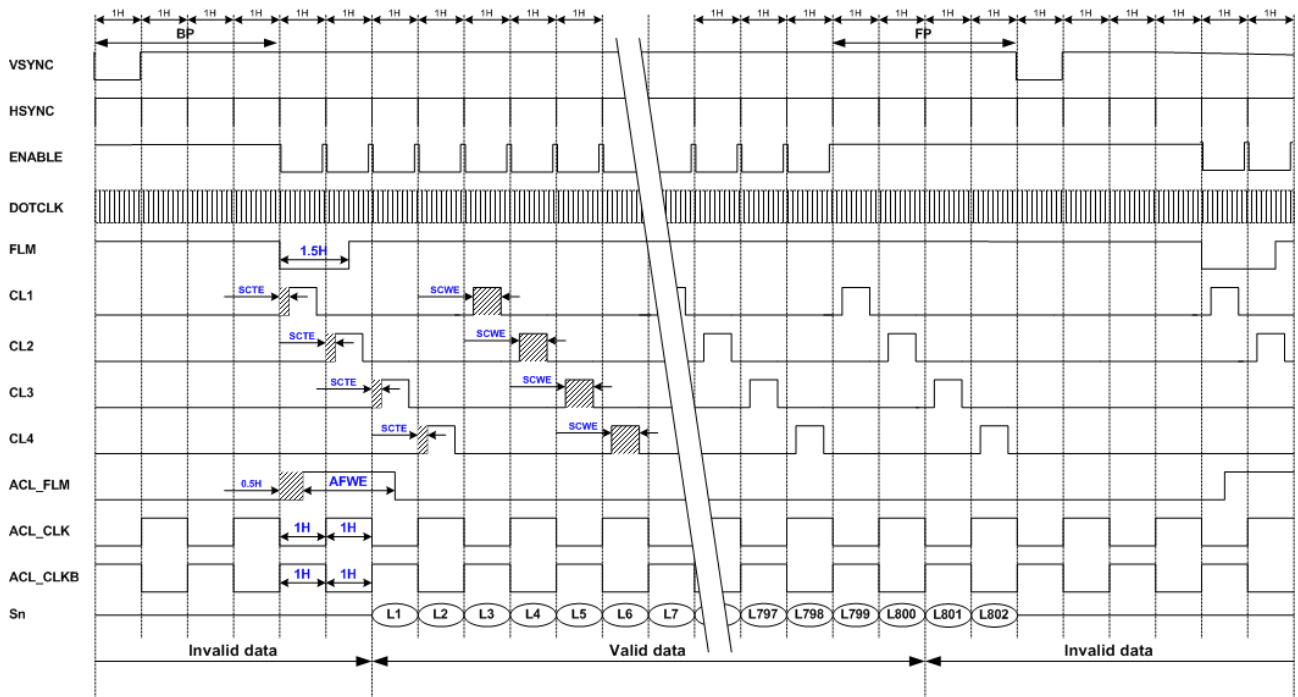
| LTPS Mode PAD Name | CMOS | Latch | PMOS-1 | PMOS-2 |
|-----------------------|--------------|--------------|--------------|--------------|
| | GTCON = "00" | GTCON = "01" | GTCON = "10" | GTCON = "11" |
| FLM | FLM | FLM | FLM | FLM |
| SFTCLKB(CLK1) | SFTCLKB | CL1 | CLK1 | CLK1 |
| SFTCLK(CLK2) | SFTCLK | CL2 | CLK2 | CLK2 |
| SCLK2(CLK3) | SCLK2 | CL3 | CLK3 | CLK3 |
| SCLK1 | SCLK1 | CL4 | - | - |
| ESR | ESR | ESR | ESR | ESR |
| EM_CLK2B | - | - | EM_CLK2B | EM_CLK2B |
| EM_CLK2 | - | - | EM_CLK2 | EM_CLK2 |
| EM_CLK1B | ACL_CLKB | ACL_CLKB | EM_CLK1B | EM_CLK1B |
| EM_CLK1 | ACL_CLK | ACL_CLK | EM_CLK1 | EM_CLK1 |
| EM_FLM | ACL_FLM | ACL_FLM | EM_FLM | EM_FLM |

LTPS signal timing setting table

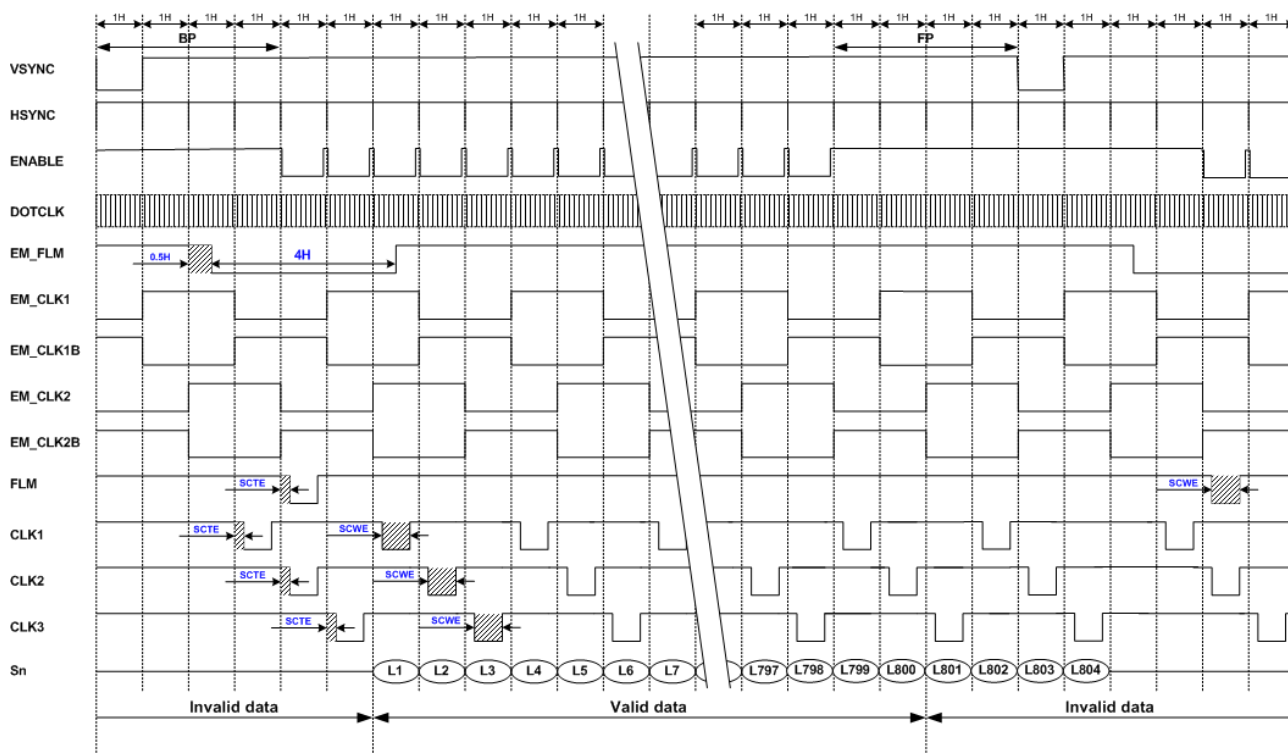
Panel interface timing with Type A (CMOS)



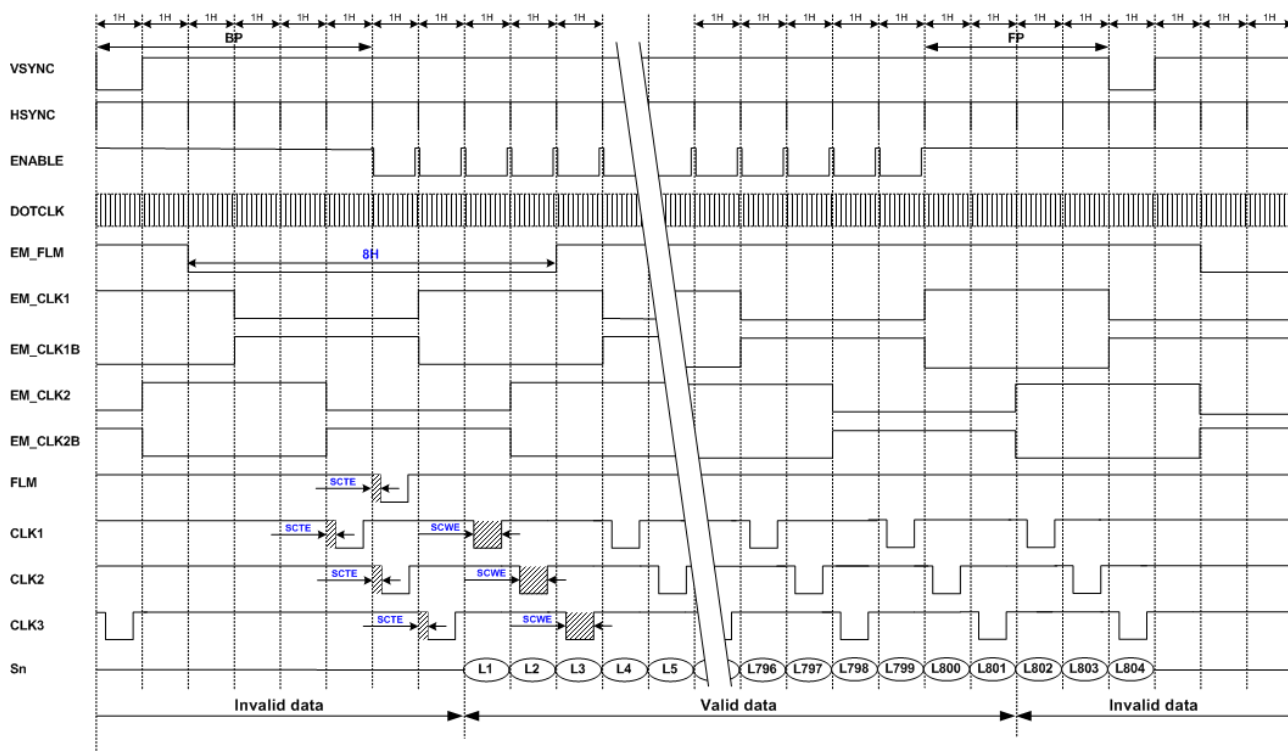
Panel interface timing with Type B (Latch)



Panel interface timing with Type C (PMOS-1)

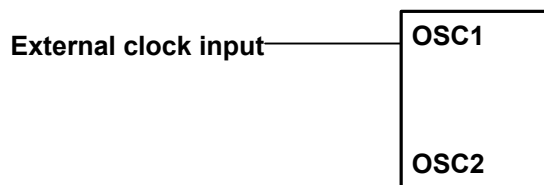


Panel interface timing with Type D (PMOS-2)

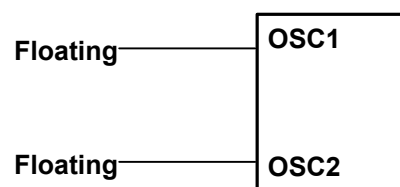


5-5. Oscillator Circuit (OSC)

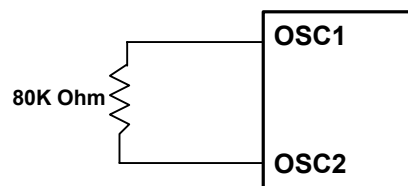
1) External Clock Mode



2) Internal Clock Mode

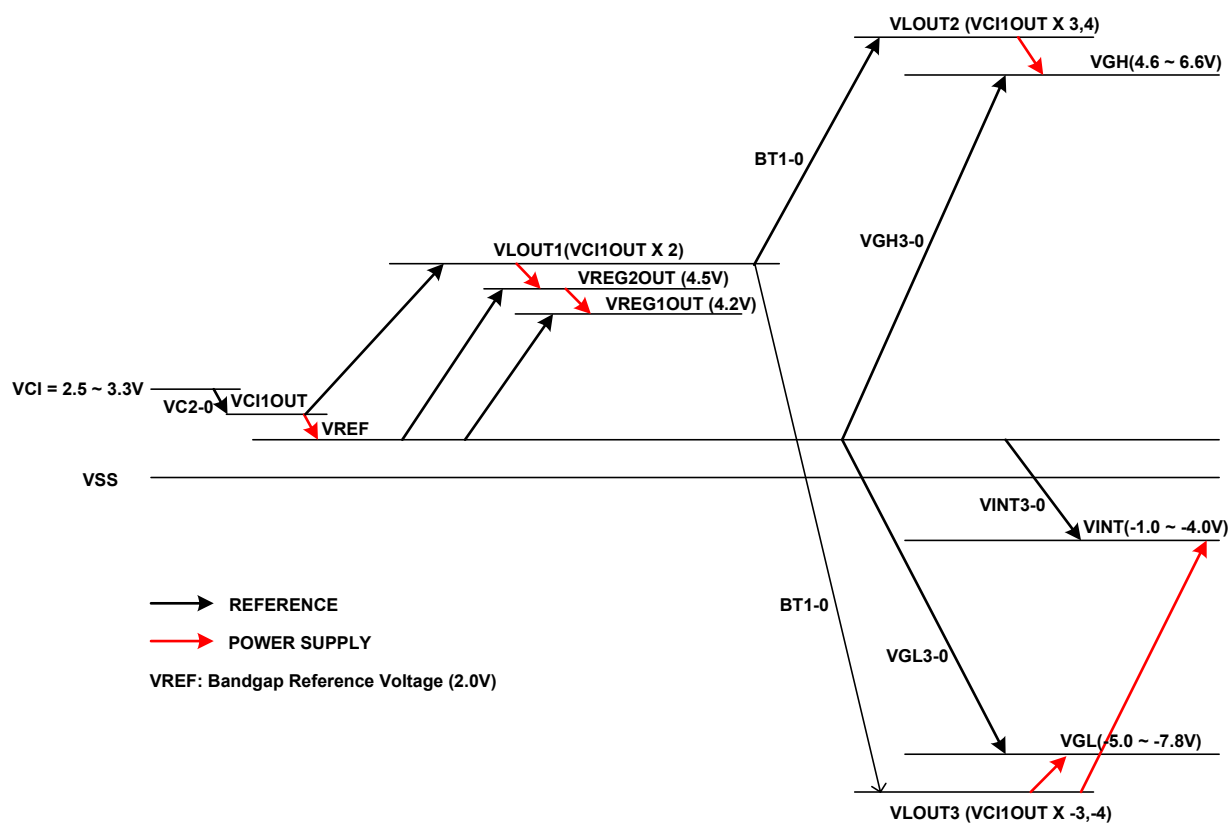


3) External Resistor Mode



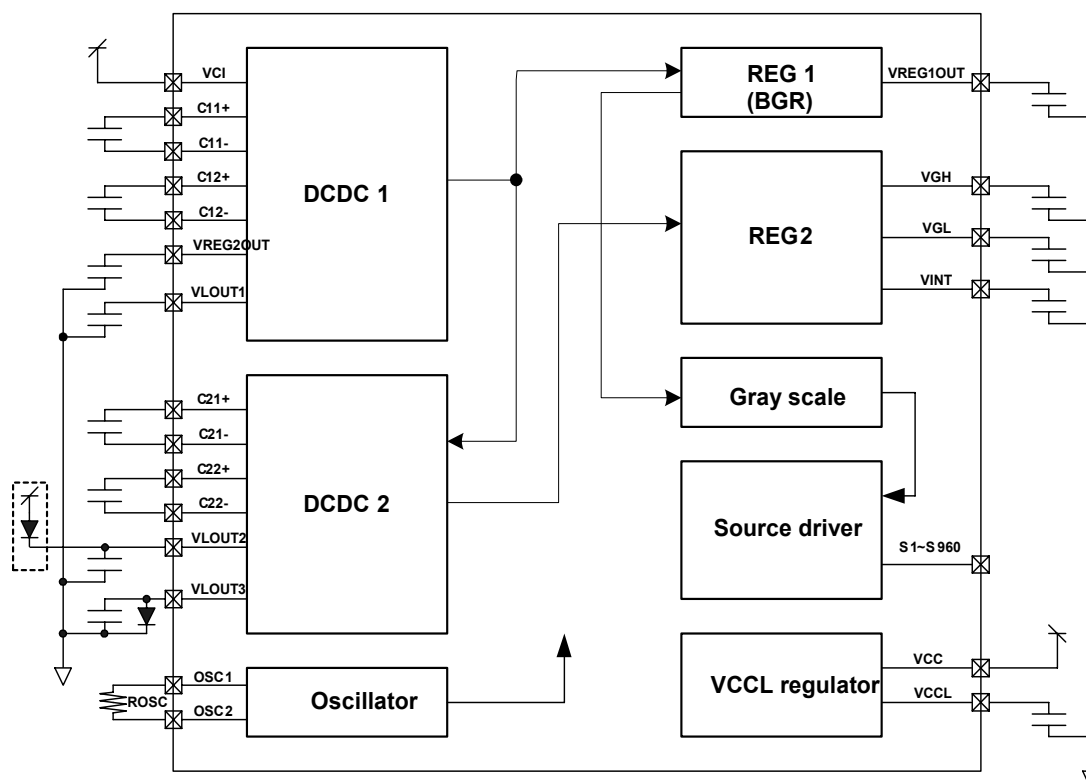
< Oscillation circuit >

5-6. Power Supply Circuit



<Pattern Diagram for Voltage Setting >

Power generation circuit block diagram



TL2796 OLED Driver voltage generation circuit

Note 1) Specification for shottky diode : $V_F < 0.4V$, $20mA$, $V_R > 30V$.

Note 2) Shottky diode must be placed from VLOUT3 to VSS within 100hm wiring resistance.

Note 3) In some cases, shottky diode can be placed from VCI to VLOUT2 in order to prevent sub-leakage current.

Specification on TL2796 power circuit and external elements

The following tables show the specification on external elements connected to a power circuit.

Capacitor

| Capacitance capacity | Recommended capacitor voltage | Connection pin |
|----------------------|-------------------------------|---|
| 1uF | 6V | VCCL, VCI1OUT, VREG1OUT, VREG2OUT, C11+/-, C12+/-, VLOUT1, VINT |
| | 10V | VGH |
| | 20V | C21+/-, C22+/-, VLOUT2 |
| 4.7uF | 16V | VGL, VLOUT3 |

Schottky diode

| Specification | Pin connection |
|---|----------------|
| $V_F < 0.4V/20mA@25^{\circ}C, V_R \geq 30V$ | VSS – VLOUT3 |

RESET Function

This IC is internally initialized by RESET input. The reset input must be held for at least 1mS.

Output pin initialization

- Source output(S1~S960) : Hi-z
- Gateless signal for AMOLED operation : VSS
- SPI output pin(SDO) : VSS
- Oscillator output pin(OSC1) : VSS

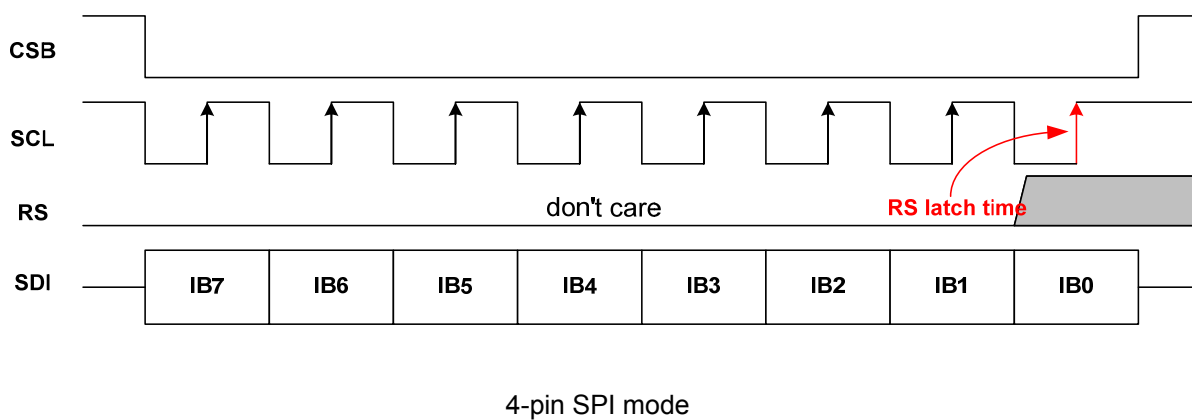
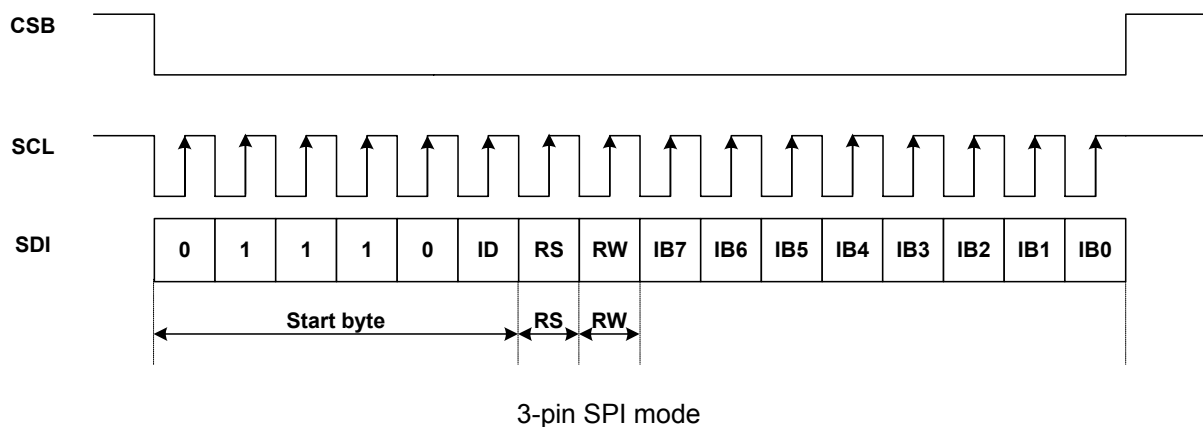
6. INSTRUCTION(REGISTERS)

OUTLINE

TL2796 can set the instruction via the 3-pin or 4-pin SPI. When instruction write via the 3-pin SPI, the first 8-bit transmit start-byte and the second 8-bit transmit instruction. But, the 4-pin SPI don't need to transmit start-byte.

There are eight categories of instructions that:

- Specify the index
- Read the chip index
- Read the revision number
- Control the display
- Control power management
- Process the graphics data
- Set grayscale level for the internal grayscale palette table



Instruction table

| Reg No. | Instruction | R/W <i>*Note2</i> | RS | Initial value | Code | | | | | | | |
|-----------|--------------------------------------|----------------------|----|---------------|------------------------------|----------|----------|----------|----------|----------|----------|----------|
| | | | | | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
| IR | Index | W | 0 | | 11h ~ 76h | | | | | | | |
| 00h ~ 02h | IC Information read (only 3-pin SPI) | R | 0 | | Read data(IC information) | | | | | | | |
| 07h | EEPROM control | W | 0 | 8'h00 | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 |
| 11h | Oscillator control | R/W | 0 | 8'hA0 | 1 | 0 | 1 | 0 | 0 | EXTR | EXT | OSC |
| 12h | Display control1 | R/W | 0 | 8'h08 | 0 | 0 | 0 | BP4 | BP3 | BP2 | BP1 | BP0 |
| 13h | | R/W | 0 | 8'h08 | 0 | 0 | 0 | FP4 | FP3 | FP2 | FP1 | FP0 |
| 14h | Display control2 | R/W | 0 | 8'h00 | 0 | 0 | 0 | REV | 0 | 0 | D1 | D0 |
| 15h | | R/W | 0 | 8'h00 | 0 | 0 | 0 | SS | VSPL | HSPL | DPL | EPL |
| 16h | | R/W | 0 | 8'h00 | 0 | 0 | PT1 | PT0 | 0 | 0 | CM1 | CM0 |
| 17h | Power control1 | R/W | 0 | 8'h22 | 0 | DC12 | DC11 | DC10 | 0 | DC02 | DC01 | DC00 |
| 18h | | R/W | 0 | 8'h33 | 0 | SAP2 | SAP1 | SAP0 | 0 | AP2 | AP1 | AP0 |
| 19h | | R/W | 0 | 8'h03 | 0 | 0 | 0 | 0 | 0 | GAP2 | GAP1 | GAP0 |
| 1Ah | Power control2 | R/W | 0 | 8'h00 | 0 | 0 | 0 | 0 | 0 | 0 | BT1 | BT0 |
| 1Bh | | R/W | 0 | 8'h3A | VGH3 | VGH2 | VGH1 | VGH0 | VGL3 | VGL2 | VGL1 | VGL0 |
| 1Ch | | R/W | 0 | 8'h05 | 0 | 0 | 0 | 0 | VINT3 | VINT2 | VINT1 | VINT0 |
| 1Dh | Power control3 | R/W | 0 | 8'hA1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | STB |
| 21h | VREF control | R/W | 0 | 8'h00 | 0 | 0 | 0 | 0 | | REF_MD | 0 | 0 |
| 22h | Logic voltage control | R/W | 0 | 8'hA4 | 1 | 0 | 1 | 0 | 0 | SVL2 | SVL1 | SVL0 |
| 23h | Power control4 | R/W | 0 | 8'h00 | 0 | 0 | 0 | 0 | 0 | VC2 | VC1 | VC0 |
| 24h | | R/W | 0 | 8'h77 | 0 | VRH2 | VRH1 | VRH0 | VRG3 | VRG2 | VRG1 | VRG0 |
| 26h | Display control3 | R/W | 0 | 8'hA0 | 1 | 0 | 1 | 0 | 0 | 0 | DMD1 | DMD0 |
| 27h | | R/W | 0 | 8'h00 | 0 | 0 | 0 | 0 | 0 | 0 | SOE | PCS |
| 28h | Display control4 <i>*Note1</i> | W | 0 | 16'h0000 | 1 st transmission | | | | | | | |
| | | | | | 0 | 0 | 0 | 0 | 0 | 0 | PSA9 | PSA8 |
| | | | | | 2 nd transmission | | | | | | | |
| | | | | | PSA7 | PSA6 | PSA5 | PSA4 | PSA3 | PSA2 | PSA1 | PSA0 |
| 29h | | W | 0 | 16'h031F | 1 st transmission | | | | | | | |
| | | | | | 0 | 0 | 0 | 0 | 0 | 0 | PEA9 | PEA8 |
| | | | | | 2 nd transmission | | | | | | | |
| | | | | | PEA7 | PEA6 | PEA5 | PEA4 | PEA3 | PEA2 | PEA1 | PEA0 |
| 30h | Gate-less signal control | R/W | 0 | 8'h02 | 0 | 0 | DL1 | DL0 | 0 | 0 | GTCON1 | GTCON0 |
| 31h | | R/W | 0 | 8'h08 | 0 | 0 | 0 | SCTE4 | SCTE3 | SCTE2 | SCTE1 | SCTE0 |
| 32h | | R/W | 0 | 8'h14 | 0 | 0 | 0 | SCWE4 | SCWE3 | SCWE2 | SCWE1 | SCWE0 |
| 35h | ACL control | R/W | 0 | 8'h00 | 0 | 0 | 0 | ACLON | 0 | 0 | ACLM1 | ACLM0 |
| 39h | Brightness control | R/W | 0 | 8'h44 | 0 | BVC2 | BVC1 | BVC0 | 0 | GMAS2 | GMAS1 | GMAS0 |
| 40h | gamma adjustment for R-gray | W | 0 | 8'h00 | 0 | 0 | 0 | 0 | CR03 | CR02 | CR01 | CR00 |
| 41h | | W | 0 | 8'h0D | 0 | 0 | CR15 | CR14 | CR13 | CR12 | CR11 | CR10 |
| 42h | | W | 0 | 8'h06 | 0 | 0 | CR25 | CR24 | CR23 | CR22 | CR21 | CR20 |
| 43h | | W | 0 | 8'h20 | 0 | 0 | CR35 | CR34 | CR33 | CR32 | CR31 | CR30 |
| 44h | | W | 0 | 8'h1C | 0 | 0 | CR45 | CR44 | CR43 | CR42 | CR41 | CR40 |
| 45h | | W | 0 | 8'h1A | 0 | 0 | CR55 | CR54 | CR53 | CR52 | CR51 | CR50 |
| 46h | | W | 0 | 8'h4F | CR67 | CR66 | CR65 | CR64 | CR63 | CR62 | CR61 | CR60 |
| 50h | gamma adjustment for G-gray | W | 0 | 8'h00 | 0 | 0 | 0 | 0 | CG03 | CG02 | CG01 | CG00 |
| 51h | | W | 0 | 8'h0D | 0 | 0 | CG15 | CG14 | CG13 | CG12 | CG11 | CG10 |
| 52h | | W | 0 | 8'h2C | 0 | 0 | CG25 | CG24 | CG23 | CG22 | CG21 | CG20 |
| 53h | | W | 0 | 8'h24 | 0 | 0 | CG35 | CG34 | CG33 | CG32 | CG31 | CG30 |
| 54h | | W | 0 | 8'h20 | 0 | 0 | CG45 | CG44 | CG43 | CG42 | CG41 | CG40 |
| 55h | | W | 0 | 8'h1C | 0 | 0 | CG55 | CG54 | CG53 | CG52 | CG51 | CG50 |
| 56h | | W | 0 | 8'h4A | CG67 | CG66 | CG65 | CG64 | CG63 | CG62 | CG61 | CG60 |
| 60h | gamma adjustment for B-gray | W | 0 | 8'h00 | 0 | 0 | 0 | 0 | CB03 | CB02 | CB01 | CB00 |
| 61h | | W | 0 | 8'h0D | 0 | 0 | CB15 | CB14 | CB13 | CB12 | CB11 | CB10 |
| 62h | | W | 0 | 8'h2B | 0 | 0 | CB25 | CB24 | CB23 | CB22 | CB21 | CB20 |
| 63h | | W | 0 | 8'h24 | 0 | 0 | CB35 | CB34 | CB33 | CB32 | CB31 | CB30 |
| 64h | | W | 0 | 8'h1D | 0 | 0 | CB45 | CB44 | CB43 | CB42 | CB41 | CB40 |
| 65h | | W | 0 | 8'h19 | 0 | 0 | CB55 | CB54 | CB53 | CB52 | CB51 | CB50 |
| 66h | | W | 0 | 8'h63 | CB67 | CB66 | CB65 | CB64 | CB63 | CB62 | CB61 | CB60 |
| 70h | EEPROM control | W | 0 | 8'h55 | 0 | EV255_C2 | EV255_C1 | EV255_C0 | 0 | EV127_C2 | EV127_C1 | EV127_C0 |
| 71h | | R/W | 0 | 8'h00 | 0 | 0 | 0 | 0 | EV127_R3 | EV127_R2 | EV127_R1 | EV127_R0 |
| 72h | | R/W | 0 | 8'h00 | 0 | 0 | 0 | 0 | EV127_G3 | EV127_G2 | EV127_G1 | EV127_G0 |
| 73h | | R/W | 0 | 8'h00 | 0 | 0 | 0 | 0 | EV127_B3 | EV127_B2 | EV127_B1 | EV127_B0 |
| 74h | | R/W | 0 | 8'h00 | 0 | 0 | 0 | EV255_R4 | EV255_R3 | EV255_R2 | EV255_R1 | EV255_R0 |
| 75h | | R/W | 0 | 8'h00 | 0 | 0 | 0 | EV255_G4 | EV255_G3 | EV255_G2 | EV127_G1 | EV127_G0 |
| 76h | | R/W | 0 | 8'h00 | 0 | 0 | 0 | EV255_B4 | EV255_B3 | EV255_B2 | EV127_B1 | EV127_B0 |

TL2796

960-channel source driver with power circuit for 16M colors gate-IC-less AMOLED with PenTile Layout

| Reg No. | Instruction | R/W | RS | Initial value | Code | | | | | | | |
|---------|--|---------|---------|---------------|------------------------------|---------|---------|---------|---------|---------|---------|---------|
| | | | | | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
| 90h | ACL pulse Width control* Note1 | W | 0 | 16'h 0103 | 1 st transmission | | | | | | | |
| | | | | | AFWE07 | AFWE06 | AFWE05 | AFWE04 | AFWE03 | AFWE02 | AFWE01 | AFWE00 |
| | | | | | 2 nd transmission | | | | | | | |
| AFWE17 | | AFWE16 | AFWE15 | AFWE14 | AFWE13 | AFWE12 | AFWE11 | AFWE10 | | | | |
| 91h | | W | 0 | 16'h 0507 | 1 st transmission | | | | | | | |
| | | | | | AFWE27 | AFWE26 | AFWE25 | AFWE24 | AFWE23 | AFWE22 | AFWE21 | AFWE20 |
| | | | | | 2 nd transmission | | | | | | | |
| AFWE37 | | AFWE36 | AFWE35 | AFWE34 | AFWE33 | AFWE32 | AFWE31 | AFWE30 | | | | |
| 92h | | W | 0 | 16'h090B | 1 st transmission | | | | | | | |
| | | | | | AFWE47 | AFWE46 | AFWE45 | AFWE44 | AFWE43 | AFWE42 | AFWE41 | AFWE40 |
| | | | | | 2 nd transmission | | | | | | | |
| AFWE57 | | AFWE56 | AFWE55 | AFWE54 | AFWE53 | AFWE52 | AFWE51 | AFWE50 | | | | |
| 93h | | W | 0 | 16'h0D0F | 1 st transmission | | | | | | | |
| | | | | | AFWE67 | AFWE66 | AFWE65 | AFWE64 | AFWE63 | AFWE62 | AFWE61 | AFWE60 |
| | | | | | 2 nd transmission | | | | | | | |
| AFWE77 | | AFWE76 | AFWE75 | AFWE74 | AFWE73 | AFWE72 | AFWE71 | AFWE70 | | | | |
| 94h | | W | 0 | 16'h 1113 | 1 st transmission | | | | | | | |
| | | | | | AFWE87 | AFWE86 | AFWE85 | AFWE84 | AFWE83 | AFWE82 | AFWE81 | AFWE80 |
| | | | | | 2 nd transmission | | | | | | | |
| AFWE97 | | AFWE96 | AFWE95 | AFWE94 | AFWE93 | AFWE92 | AFWE91 | AFWE90 | | | | |
| 95h | | W | 0 | 16'h 1517 | 1 st transmission | | | | | | | |
| | | | | | AFWE107 | AFWE106 | AFWE105 | AFWE104 | AFWE103 | AFWE102 | AFWE101 | AFWE100 |
| | | | | | 2 nd transmission | | | | | | | |
| AFWE117 | | AFWE116 | AFWE115 | AFWE114 | AFWE113 | AFWE112 | AFWE111 | AFWE110 | | | | |
| 96h | | W | 0 | 16'h 191B | 1 st transmission | | | | | | | |
| | | | | | AFWE127 | AFWE126 | AFWE125 | AFWE124 | AFWE123 | AFWE122 | AFWE121 | AFWE120 |
| | | | | | 2 nd transmission | | | | | | | |
| AFWE137 | | AFWE136 | AFWE135 | AFWE134 | AFWE133 | AFWE132 | AFWE131 | AFWE130 | | | | |
| 97h | | W | 0 | 16'h 1D1F | 1 st transmission | | | | | | | |
| | | | | | AFWE147 | AFWE146 | AFWE145 | AFWE144 | AFWE143 | AFWE142 | AFWE141 | AFWE140 |
| | | | | | 2 nd transmission | | | | | | | |
| AFWE157 | | AFWE156 | AFWE155 | AFWE154 | AFWE153 | AFWE152 | AFWE151 | AFWE150 | | | | |
| 98h | | W | 0 | 16'h 2123 | 1 st transmission | | | | | | | |
| | | | | | AFWE167 | AFWE166 | AFWE165 | AFWE164 | AFWE163 | AFWE162 | AFWE161 | AFWE160 |
| | | | | | 2 nd transmission | | | | | | | |
| AFWE177 | | AFWE176 | AFWE175 | AFWE174 | AFWE173 | AFWE172 | AFWE171 | AFWE170 | | | | |
| 99h | | W | 0 | 16'h 2527 | 1 st transmission | | | | | | | |
| | | | | | AFWE187 | AFWE186 | AFWE185 | AFWE184 | AFWE183 | AFWE182 | AFWE181 | AFWE180 |
| | | | | | 2 nd transmission | | | | | | | |
| AFWE197 | | AFWE196 | AFWE195 | AFWE194 | AFWE193 | AFWE192 | AFWE191 | AFWE190 | | | | |
| 9Ah | | W | 0 | 16'h 292B | 1 st transmission | | | | | | | |
| | | | | | AFWE207 | AFWE206 | AFWE205 | AFWE204 | AFWE203 | AFWE202 | AFWE201 | AFWE200 |
| | | | | | 2 nd transmission | | | | | | | |
| AFWE217 | | AFWE216 | AFWE215 | AFWE214 | AFWE213 | AFWE212 | AFWE211 | AFWE210 | | | | |
| 9Bh | | W | 0 | 16'h 2D2F | 1 st transmission | | | | | | | |
| | | | | | AFWE227 | AFWE226 | AFWE225 | AFWE224 | AFWE223 | AFWE222 | AFWE221 | AFWE220 |
| | | | | | 2 nd transmission | | | | | | | |
| AFWE237 | | AFWE236 | AFWE235 | AFWE234 | AFWE233 | AFWE232 | AFWE231 | AFWE230 | | | | |
| 9Ch | | W | 0 | 16'h 3133 | 1 st transmission | | | | | | | |
| | | | | | AFWE247 | AFWE246 | AFWE245 | AFWE244 | AFWE243 | AFWE242 | AFWE241 | AFWE240 |
| | | | | | 2 nd transmission | | | | | | | |
| AFWE257 | | AFWE256 | AFWE255 | AFWE254 | AFWE253 | AFWE252 | AFWE251 | AFWE250 | | | | |
| 9Dh | | W | 0 | 16'h 3537 | 1 st transmission | | | | | | | |
| | | | | | AFWE267 | AFWE266 | AFWE265 | AFWE264 | AFWE263 | AFWE262 | AFWE261 | AFWE260 |
| | | | | | 2 nd transmission | | | | | | | |
| AFWE277 | | AFWE276 | AFWE275 | AFWE274 | AFWE273 | AFWE272 | AFWE271 | AFWE270 | | | | |
| 9Eh | | W | 0 | 16'h 393B | 1 st transmission | | | | | | | |
| | | | | | AFWE287 | AFWE286 | AFWE285 | AFWE284 | AFWE283 | AFWE282 | AFWE281 | AFWE280 |
| | | | | | 2 nd transmission | | | | | | | |
| AFWE297 | | AFWE296 | AFWE295 | AFWE294 | AFWE293 | AFWE292 | AFWE291 | AFWE290 | | | | |
| 9Fh | | W | 0 | 16'h 3D3F | 1 st transmission | | | | | | | |
| | | | | | AFWE307 | AFWE306 | AFWE305 | AFWE304 | AFWE303 | AFWE302 | AFWE301 | AFWE300 |
| | | | | | 2 nd transmission | | | | | | | |
| AFWE317 | | AFWE316 | AFWE315 | AFWE314 | AFWE313 | AFWE312 | AFWE311 | AFWE310 | | | | |

TL2796

960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout

Instruction for PenTile Processing * Note1

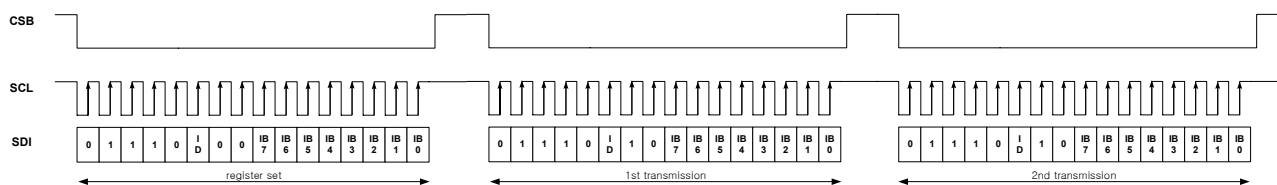
| Reg No. | Instruction | R/W | RS | Initial value | Code | | | | | | | |
|---------|-------------|-----|----|---------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | | | | | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
| A0h | PENTILE1 | W | 0 | 16'h0063 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | 0 | SFG | MSG | PTRB | SFRB1 | SFRB0 | MSRB | PARB |
| A1h | PENTILE2 | W | 0 | 16'h00C0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BYP5 |
| | | | | | DTMD | DTON | 0 | 0 | SID1 | SID0 | 0 | 0 |
| A2h | PENTILE3 | W | 0 | 16'h0032 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | MSTH 7 | MSTH 6 | MSTH 5 | MSTH 4 | MSTH 3 | MSTH 2 | MSTH 1 | MSTH 0 |
| A3h | PENTILE4 | W | 0 | 16'h0002 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | 0 | 0 | 0 | 0 | PATH 3 | PATH 2 | PATH 1 | PATH 0 |
| A4h | OR | W | 0 | 16'h0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | OR7 | OR6 | OR5 | OR4 | OR3 | OR2 | OR1 | OR0 |
| A5h | YR1 | W | 0 | 16'h122C | ΔYR27 | ΔYR26 | ΔYR25 | ΔYR24 | ΔYR23 | ΔYR22 | ΔYR21 | ΔYR20 |
| | | | | | ΔYR17 | ΔYR16 | ΔYR15 | ΔYR14 | ΔYR13 | ΔYR12 | ΔYR11 | ΔYR10 |
| A6h | YR2 | W | 0 | 16'h0A0C | ΔYR47 | ΔYR46 | ΔYR45 | ΔYR44 | ΔYR43 | ΔYR42 | ΔYR41 | ΔYR40 |
| | | | | | ΔYR37 | ΔYR36 | ΔYR35 | ΔYR34 | ΔYR33 | ΔYR32 | ΔYR31 | ΔYR30 |
| A7h | YR3 | W | 0 | 16'h0E10 | ΔYR67 | ΔYR66 | ΔYR65 | ΔYR64 | ΔYR63 | ΔYR62 | ΔYR61 | ΔYR60 |
| | | | | | ΔYR57 | ΔYR56 | ΔYR55 | ΔYR54 | ΔYR53 | ΔYR52 | ΔYR51 | ΔYR50 |
| A8h | YR4 | W | 0 | 16'h1317 | ΔYR87 | ΔYR86 | ΔYR85 | ΔYR84 | ΔYR83 | ΔYR82 | ΔYR81 | ΔYR80 |
| | | | | | ΔYR77 | ΔYR76 | ΔYR75 | ΔYR74 | ΔYR73 | ΔYR72 | ΔYR71 | ΔYR70 |
| A9h | YR5 | W | 0 | 16'h1A1F | ΔYR107 | ΔYR106 | ΔYR105 | ΔYR104 | ΔYR103 | ΔYR102 | ΔYR101 | ΔYR100 |
| | | | | | ΔYR97 | ΔYR96 | ΔYR95 | ΔYR94 | ΔYR93 | ΔYR92 | ΔYR91 | ΔYR90 |
| AAh | YR6 | W | 0 | 16'h242A | ΔYR127 | ΔYR126 | ΔYR125 | ΔYR124 | ΔYR123 | ΔYR122 | ΔYR121 | ΔYR120 |
| | | | | | ΔYR117 | ΔYR116 | ΔYR115 | ΔYR114 | ΔYR113 | ΔYR112 | ΔYR111 | ΔYR110 |
| ABh | YR7 | W | 0 | 16'h1B1F | ΔYR147 | ΔYR146 | ΔYR145 | ΔYR144 | ΔYR143 | ΔYR142 | ΔYR141 | ΔYR140 |
| | | | | | ΔYR137 | ΔYR136 | ΔYR135 | ΔYR134 | ΔYR133 | ΔYR132 | ΔYR131 | ΔYR130 |
| Ach | YR8 | W | 0 | 16'h171A | ΔYR167 | ΔYR166 | ΔYR165 | ΔYR164 | ΔYR163 | ΔYR162 | ΔYR161 | ΔYR160 |
| | | | | | ΔYR157 | ΔYR156 | ΔYR155 | ΔYR154 | ΔYR153 | ΔYR152 | ΔYR151 | ΔYR150 |
| ADh | YR9 | W | 0 | 16'h262B | ΔYR187 | ΔYR186 | ΔYR185 | ΔYR184 | ΔYR183 | ΔYR182 | ΔYR181 | ΔYR180 |
| | | | | | ΔYR177 | ΔYR176 | ΔYR175 | ΔYR174 | ΔYR173 | ΔYR172 | ΔYR171 | ΔYR170 |
| AEh | YR10 | W | 0 | 16'h2022 | ΔYR207 | ΔYR206 | ΔYR205 | ΔYR204 | ΔYR203 | ΔYR202 | ΔYR201 | ΔYR200 |
| | | | | | ΔYR197 | ΔYR196 | ΔYR195 | ΔYR194 | ΔYR193 | ΔYR192 | ΔYR191 | ΔYR190 |
| AFh | YR11 | W | 0 | 16'h343A | ΔYR227 | ΔYR226 | ΔYR225 | ΔYR224 | ΔYR223 | ΔYR222 | ΔYR221 | ΔYR220 |
| | | | | | ΔYR217 | ΔYR216 | ΔYR215 | ΔYR214 | ΔYR213 | ΔYR212 | ΔYR211 | ΔYR210 |
| B0h | YR12 | W | 0 | 16'h2C30 | ΔYR247 | ΔYR246 | ΔYR245 | ΔYR244 | ΔYR243 | ΔYR242 | ΔYR241 | ΔYR240 |
| | | | | | ΔYR237 | ΔYR236 | ΔYR235 | ΔYR234 | ΔYR233 | ΔYR232 | ΔYR231 | ΔYR230 |
| B1h | YR13 | W | 0 | 16'h2629 | ΔYR267 | ΔYR266 | ΔYR265 | ΔYR264 | ΔYR263 | ΔYR262 | ΔYR261 | ΔYR260 |
| | | | | | ΔYR257 | ΔYR256 | ΔYR255 | ΔYR254 | ΔYR253 | ΔYR252 | ΔYR251 | ΔYR250 |
| B2h | YR14 | W | 0 | 16'h2325 | ΔYR287 | ΔYR286 | ΔYR285 | ΔYR284 | ΔYR283 | ΔYR282 | ΔYR281 | ΔYR280 |
| | | | | | ΔYR277 | ΔYR276 | ΔYR275 | ΔYR274 | ΔYR273 | ΔYR272 | ΔYR271 | ΔYR270 |
| B3h | YR15 | W | 0 | 16'h2021 | ΔYR307 | ΔYR306 | ΔYR305 | ΔYR304 | ΔYR303 | ΔYR302 | ΔYR301 | ΔYR300 |
| | | | | | ΔYR297 | ΔYR296 | ΔYR295 | ΔYR294 | ΔYR293 | ΔYR292 | ΔYR291 | ΔYR290 |
| B4h | YR16 | W | 0 | 16'h1E1E | ΔYR327 | ΔYR326 | ΔYR325 | ΔYR324 | ΔYR323 | ΔYR322 | ΔYR321 | ΔYR320 |
| | | | | | ΔYR317 | ΔYR316 | ΔYR315 | ΔYR314 | ΔYR313 | ΔYR312 | ΔYR311 | ΔYR310 |
| B5h | XR1 | W | 0 | 16'h0000 | 0 | ΔXR42 | ΔXR41 | ΔXR40 | 0 | ΔXR32 | ΔXR31 | ΔXR30 |
| | | | | | 0 | ΔXR22 | ΔXR21 | ΔXR20 | 0 | ΔXR12 | ΔXR11 | ΔXR10 |
| B6h | XR2 | W | 0 | 16'h2211 | 0 | ΔXR82 | ΔXR81 | ΔXR80 | 0 | ΔXR72 | ΔXR71 | ΔXR70 |
| | | | | | 0 | ΔXR62 | ΔXR61 | ΔXR60 | 0 | ΔXR52 | ΔXR51 | ΔXR50 |
| B7h | XR3 | W | 0 | 16'h4433 | 0 | ΔXR122 | ΔXR121 | ΔXR120 | 0 | ΔXR112 | ΔXR111 | ΔXR110 |
| | | | | | 0 | ΔXR102 | ΔXR101 | ΔXR100 | 0 | ΔXR92 | ΔXR91 | ΔXR90 |
| B8h | XR4 | W | 0 | 16'h4444 | 0 | ΔXR162 | ΔXR161 | ΔXR160 | 0 | ΔXR152 | ΔXR151 | ΔXR150 |
| | | | | | 0 | ΔXR142 | ΔXR141 | ΔXR140 | 0 | ΔXR132 | ΔXR131 | ΔXR130 |
| B9h | XR5 | W | 0 | 16'h5555 | 0 | ΔXR202 | ΔXR201 | ΔXR200 | 0 | ΔXR192 | ΔXR191 | ΔXR190 |
| | | | | | 0 | ΔXR182 | ΔXR181 | ΔXR180 | 0 | ΔXR172 | ΔXR171 | ΔXR170 |
| Bah | XR6 | W | 0 | 16'h6666 | 0 | ΔXR242 | ΔXR241 | ΔXR240 | 0 | ΔXR232 | ΔXR231 | ΔXR230 |
| | | | | | 0 | ΔXR222 | ΔXR221 | ΔXR220 | 0 | ΔXR212 | ΔXR211 | ΔXR210 |
| BBh | XR7 | W | 0 | 16'h6666 | 0 | ΔXR282 | ΔXR281 | ΔXR280 | 0 | ΔXR272 | ΔXR271 | ΔXR270 |
| | | | | | 0 | ΔXR262 | ΔXR261 | ΔXR260 | 0 | ΔXR252 | ΔXR251 | ΔXR250 |
| BCh | XR8 | W | 0 | 16'h6666 | 0 | ΔXR322 | ΔXR321 | ΔXR320 | 0 | ΔXR312 | ΔXR311 | ΔXR310 |
| | | | | | 0 | ΔXR302 | ΔXR301 | ΔXR300 | 0 | ΔXR292 | ΔXR291 | ΔXR290 |
| BDh | OG | W | 0 | 16'h0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | OG7 | OG6 | OG5 | OG4 | OG3 | OG2 | OG1 | OG0 |
| BEh | YG1 | W | 0 | 16'h122C | ΔYG27 | ΔYG26 | ΔYG25 | ΔYG24 | ΔYG23 | ΔYG22 | ΔYG21 | ΔYG20 |
| | | | | | ΔYG17 | ΔYG16 | ΔYG15 | ΔYG14 | ΔYG13 | ΔYG12 | ΔYG11 | ΔYG10 |
| BFh | YG2 | W | 0 | 16'h0A0C | ΔYG47 | ΔYG46 | ΔYG45 | ΔYG44 | ΔYG43 | ΔYG42 | ΔYG41 | ΔYG40 |
| | | | | | ΔYG37 | ΔYG36 | ΔYG35 | ΔYG34 | ΔYG33 | ΔYG32 | ΔYG31 | ΔYG30 |
| C0h | YG3 | W | 0 | 16'h0E10 | ΔYG67 | ΔYG66 | ΔYG65 | ΔYG64 | ΔYG63 | ΔYG62 | ΔYG61 | ΔYG60 |
| | | | | | ΔYG57 | ΔYG56 | ΔYG55 | ΔYG54 | ΔYG53 | ΔYG52 | ΔYG51 | ΔYG50 |
| C1h | YG4 | W | 0 | 16'h1317 | ΔYG87 | ΔYG86 | ΔYG85 | ΔYG84 | ΔYG83 | ΔYG82 | ΔYG81 | ΔYG80 |
| | | | | | ΔYG77 | ΔYG76 | ΔYG75 | ΔYG74 | ΔYG73 | ΔYG72 | ΔYG71 | ΔYG70 |
| C2h | YG5 | W | 0 | 16'h1A1F | ΔYG107 | ΔYG106 | ΔYG105 | ΔYG104 | ΔYG103 | ΔYG102 | ΔYG101 | ΔYG100 |
| | | | | | ΔYG97 | ΔYG96 | ΔYG95 | ΔYG94 | ΔYG93 | ΔYG92 | ΔYG91 | ΔYG90 |
| C3h | YG6 | W | 0 | 16'h242A | ΔYG127 | ΔYG126 | ΔYG125 | ΔYG124 | ΔYG123 | ΔYG122 | ΔYG121 | ΔYG120 |
| | | | | | ΔYG117 | ΔYG116 | ΔYG115 | ΔYG114 | ΔYG113 | ΔYG112 | ΔYG111 | ΔYG110 |
| C4h | YG7 | W | 0 | 16'h1B1F | ΔYG147 | ΔYG146 | ΔYG145 | ΔYG144 | ΔYG143 | ΔYG142 | ΔYG141 | ΔYG140 |
| | | | | | ΔYG137 | ΔYG136 | ΔYG135 | ΔYG134 | ΔYG133 | ΔYG132 | ΔYG131 | ΔYG130 |
| C5h | YG8 | W | 0 | 16'h171A | ΔYG167 | ΔYG166 | ΔYG165 | ΔYG164 | ΔYG163 | ΔYG162 | ΔYG161 | ΔYG160 |
| | | | | | ΔYG157 | ΔYG156 | ΔYG155 | ΔYG154 | ΔYG153 | ΔYG152 | ΔYG151 | ΔYG150 |
| C6h | YG9 | W | 0 | 16'h262B | ΔYG187 | ΔYG186 | ΔYG185 | ΔYG184 | ΔYG183 | ΔYG182 | ΔYG181 | ΔYG180 |
| | | | | | ΔYG177 | ΔYG176 | ΔYG175 | ΔYG174 | ΔYG173 | ΔYG172 | ΔYG171 | ΔYG170 |
| C7h | YG10 | W | 0 | 16'h2022 | ΔYG207 | ΔYG206 | ΔYG205 | ΔYG204 | ΔYG203 | ΔYG202 | ΔYG201 | ΔYG200 |
| | | | | | ΔYG197 | ΔYG196 | ΔYG195 | ΔYG194 | ΔYG193 | ΔYG192 | ΔYG191 | ΔYG190 |

TL2796

960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout

| | | | | | | | | | | | | |
|-----|------------|---|---|----------|---------|---------|---------|---------|---------|---------|---------|---------|
| C8h | YG11 | W | 0 | 16'h343A | ΔYG22 7 | ΔYG22 6 | ΔYG22 5 | ΔYG22 4 | ΔYG22 3 | ΔYG22 2 | ΔYG22 1 | ΔYG22 0 |
| | | | | | ΔYG21 7 | ΔYG21 6 | ΔYG21 5 | ΔYG21 4 | ΔYG21 3 | ΔYG21 2 | ΔYG21 1 | ΔYG21 0 |
| C9h | YG12 | W | 0 | 16'h2C30 | ΔYG24 7 | ΔYG24 6 | ΔYG24 5 | ΔYG24 4 | ΔYG24 3 | ΔYG24 2 | ΔYG24 1 | ΔYG24 0 |
| | | | | | ΔYG23 7 | ΔYG23 6 | ΔYG23 5 | ΔYG23 4 | ΔYG23 3 | ΔYG23 2 | ΔYG23 1 | ΔYG23 0 |
| CAh | YG13 | W | 0 | 16'h2629 | ΔYG26 7 | ΔYG26 6 | ΔYG26 5 | ΔYG26 4 | ΔYG26 3 | ΔYG26 2 | ΔYG26 1 | ΔYG26 0 |
| | | | | | ΔYG25 7 | ΔYG25 6 | ΔYG25 5 | ΔYG25 4 | ΔYG25 3 | ΔYG25 2 | ΔYG25 1 | ΔYG25 0 |
| CBh | YG14 | W | 0 | 16'h2325 | ΔYG28 7 | ΔYG28 6 | ΔYG28 5 | ΔYG28 4 | ΔYG28 3 | ΔYG28 2 | ΔYG28 1 | ΔYG28 0 |
| | | | | | ΔYG27 7 | ΔYG27 6 | ΔYG27 5 | ΔYG27 4 | ΔYG27 3 | ΔYG27 2 | ΔYG27 1 | ΔYG27 0 |
| CCh | YG15 | W | 0 | 16'h2021 | ΔYG30 7 | ΔYG30 6 | ΔYG30 5 | ΔYG30 4 | ΔYG30 3 | ΔYG30 2 | ΔYG30 1 | ΔYG30 0 |
| | | | | | ΔYG29 7 | ΔYG29 6 | ΔYG29 5 | ΔYG29 4 | ΔYG29 3 | ΔYG29 2 | ΔYG29 1 | ΔYG29 0 |
| CDh | YG16 | W | 0 | 16'h1E1E | ΔYG32 7 | ΔYG32 6 | ΔYG32 5 | ΔYG32 4 | ΔYG32 3 | ΔYG32 2 | ΔYG32 1 | ΔYG32 0 |
| | | | | | ΔYG31 7 | ΔYG31 6 | ΔYG31 5 | ΔYG31 4 | ΔYG31 3 | ΔYG31 2 | ΔYG31 1 | ΔYG31 0 |
| CEh | XG1 | W | 0 | 16'h0000 | 0 | ΔXG2 | ΔXG41 | ΔXG40 | 0 | ΔXG32 | ΔXG31 | ΔXG30 |
| | | | | | 0 | ΔXG22 | ΔXG21 | ΔXG20 | 0 | ΔXG12 | ΔXG11 | ΔXG10 |
| CFh | XG2 | W | 0 | 16'h2211 | 0 | ΔXG82 | ΔXG81 | ΔXG80 | 0 | ΔXG72 | ΔXG71 | ΔXG70 |
| | | | | | 0 | ΔXG62 | ΔXG61 | ΔXG60 | 0 | ΔXG52 | ΔXG51 | ΔXG50 |
| D0h | XG3 | W | 0 | 16'h4433 | 0 | ΔXG122 | ΔXG121 | ΔXG120 | 0 | ΔXG112 | ΔXG111 | ΔXG110 |
| | | | | | 0 | ΔXG102 | ΔXG101 | ΔXG100 | 0 | ΔXG92 | ΔXG91 | ΔXG90 |
| D1h | XG4 | W | 0 | 16'h4444 | 0 | ΔXG162 | ΔXG161 | ΔXG160 | 0 | ΔXG152 | ΔXG151 | ΔXG150 |
| | | | | | 0 | ΔXG142 | ΔXG141 | ΔXG140 | 0 | ΔXG132 | ΔXG131 | ΔXG130 |
| D2h | XG5 | W | 0 | 16'h5555 | 0 | ΔXG202 | ΔXG201 | ΔXG200 | 0 | ΔXG192 | ΔXG191 | ΔXG190 |
| | | | | | 0 | ΔXG182 | ΔXG181 | ΔXG180 | 0 | ΔXG172 | ΔXG171 | ΔXG170 |
| D3h | XG6 | W | 0 | 16'h6666 | 0 | ΔXG242 | ΔXG241 | ΔXG240 | 0 | ΔXG232 | ΔXG231 | ΔXG230 |
| | | | | | 0 | ΔXG222 | ΔXG221 | ΔXG220 | 0 | ΔXG212 | ΔXG211 | ΔXG210 |
| D4h | XG7 | W | 0 | 16'h6666 | 0 | ΔXG282 | ΔXG281 | ΔXG280 | 0 | ΔXG272 | ΔXG271 | ΔXG270 |
| | | | | | 0 | ΔXG262 | ΔXG261 | ΔXG260 | 0 | ΔXG252 | ΔXG251 | ΔXG250 |
| D5h | XG8 | W | 0 | 16'h6666 | 0 | ΔXG322 | ΔXG321 | ΔXG320 | 0 | ΔXG312 | ΔXG311 | ΔXG310 |
| | | | | | 0 | ΔXG302 | ΔXG301 | ΔXG300 | 0 | ΔXG292 | ΔXG291 | ΔXG290 |
| D6h | OB | W | 0 | 16'h0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | OB7 | OB6 | OB5 | OB4 | OB3 | OB2 | OB1 | OB0 |
| D7h | YB1 | W | 0 | 16'h122C | ΔYB27 | ΔYB26 | ΔYB25 | ΔYB24 | ΔYB23 | ΔYB22 | ΔYB21 | ΔYB20 |
| | | | | | ΔYB17 | ΔYB16 | ΔYB15 | ΔYB14 | ΔYB13 | ΔYB12 | ΔYB11 | ΔYB10 |
| D8h | YB2 | W | 0 | 16'h0A0C | ΔYB47 | ΔYB46 | ΔYB45 | ΔYB44 | ΔYB43 | ΔYB42 | ΔYB41 | ΔYB40 |
| | | | | | ΔYB37 | ΔYB36 | ΔYB35 | ΔYB34 | ΔYB33 | ΔYB32 | ΔYB31 | ΔYB30 |
| D9h | YB3 | W | 0 | 16'h0E10 | ΔYB67 | ΔYB66 | ΔYB65 | ΔYB64 | ΔYB63 | ΔYB62 | ΔYB61 | ΔYB60 |
| | | | | | ΔYB57 | ΔYB56 | ΔYB55 | ΔYB54 | ΔYB53 | ΔYB52 | ΔYB51 | ΔYB50 |
| DAh | YB4 | W | 0 | 16'h1317 | ΔYB87 | ΔYB86 | ΔYB85 | ΔYB84 | ΔYB83 | ΔYB82 | ΔYB81 | ΔYB80 |
| | | | | | ΔYB77 | ΔYB76 | ΔYB75 | ΔYB74 | ΔYB73 | ΔYB72 | ΔYB71 | ΔYB70 |
| DBh | YB5 | W | 0 | 16'h1A1F | ΔYB107 | ΔYB106 | ΔYB105 | ΔYB104 | ΔYB103 | ΔYB102 | ΔYB101 | ΔYB100 |
| | | | | | ΔYB97 | ΔYB96 | ΔYB95 | ΔYB94 | ΔYB93 | ΔYB92 | ΔYB91 | ΔYB90 |
| DCh | YB6 | W | 0 | 16'h242A | ΔYB127 | ΔYB126 | ΔYB125 | ΔYB124 | ΔYB123 | ΔYB122 | ΔYB121 | ΔYB120 |
| | | | | | ΔYB117 | ΔYB116 | ΔYB115 | ΔYB114 | ΔYB113 | ΔYB112 | ΔYB111 | ΔYB110 |
| DDh | YB7 | W | 0 | 16'h1B1F | ΔYB147 | ΔYB146 | ΔYB145 | ΔYB144 | ΔYB143 | ΔYB142 | ΔYB141 | ΔYB140 |
| | | | | | ΔYB137 | ΔYB136 | ΔYB135 | ΔYB134 | ΔYB133 | ΔYB132 | ΔYB131 | ΔYB130 |
| DEh | YB8 | W | 0 | 16'h171A | ΔYB167 | ΔYB166 | ΔYB165 | ΔYB164 | ΔYB163 | ΔYB162 | ΔYB161 | ΔYB160 |
| | | | | | ΔYB157 | ΔYB156 | ΔYB155 | ΔYB154 | ΔYB153 | ΔYB152 | ΔYB151 | ΔYB150 |
| DFh | YB9 | W | 0 | 16'h262B | ΔYB187 | ΔYB186 | ΔYB185 | ΔYB184 | ΔYB183 | ΔYB182 | ΔYB181 | ΔYB180 |
| | | | | | ΔYB177 | ΔYB176 | ΔYB175 | ΔYB174 | ΔYB173 | ΔYB172 | ΔYB171 | ΔYB170 |
| E0h | YB10 | W | 0 | 16'h2022 | ΔYB207 | ΔYB206 | ΔYB205 | ΔYB204 | ΔYB203 | ΔYB202 | ΔYB201 | ΔYB200 |
| | | | | | ΔYB197 | ΔYB196 | ΔYB195 | ΔYB194 | ΔYB193 | ΔYB192 | ΔYB191 | ΔYB190 |
| E1h | YB11 | W | 0 | 16'h343A | ΔYB227 | ΔYB226 | ΔYB225 | ΔYB224 | ΔYB223 | ΔYB222 | ΔYB221 | ΔYB220 |
| | | | | | ΔYB217 | ΔYB216 | ΔYB215 | ΔYB214 | ΔYB213 | ΔYB212 | ΔYB211 | ΔYB210 |
| E2h | YB12 | W | 0 | 16'h2C30 | ΔYB247 | ΔYB246 | ΔYB245 | ΔYB244 | ΔYB243 | ΔYB242 | ΔYB241 | ΔYB240 |
| | | | | | ΔYB237 | ΔYB236 | ΔYB235 | ΔYB234 | ΔYB233 | ΔYB232 | ΔYB231 | ΔYB230 |
| E3h | YB13 | W | 0 | 16'h2629 | ΔYB267 | ΔYB266 | ΔYB265 | ΔYB264 | ΔYB263 | ΔYB262 | ΔYB261 | ΔYB260 |
| | | | | | ΔYB257 | ΔYB256 | ΔYB255 | ΔYB254 | ΔYB253 | ΔYB252 | ΔYB251 | ΔYB250 |
| E4h | YB14 | W | 0 | 16'h2325 | ΔYB287 | ΔYB286 | ΔYB285 | ΔYB284 | ΔYB283 | ΔYB282 | ΔYB281 | ΔYB280 |
| | | | | | ΔYB277 | ΔYB276 | ΔYB275 | ΔYB274 | ΔYB273 | ΔYB272 | ΔYB271 | ΔYB270 |
| E5h | YB15 | W | 0 | 16'h2021 | ΔYB307 | ΔYB306 | ΔYB305 | ΔYB304 | ΔYB303 | ΔYB302 | ΔYB301 | ΔYB300 |
| | | | | | ΔYB297 | ΔYB296 | ΔYB295 | ΔYB294 | ΔYB293 | ΔYB292 | ΔYB291 | ΔYB290 |
| E6h | YB16 | W | 0 | 16'h1E1E | ΔYB327 | ΔYB326 | ΔYB325 | ΔYB324 | ΔYB323 | ΔYB322 | ΔYB321 | ΔYB320 |
| | | | | | ΔYB317 | ΔYB316 | ΔYB315 | ΔYB314 | ΔYB313 | ΔYB312 | ΔYB311 | ΔYB310 |
| E7h | XB1 | W | 0 | 16'h0000 | 0 | ΔXB42 | ΔXB41 | ΔXB40 | 0 | ΔXB32 | ΔXB31 | ΔXB30 |
| | | | | | 0 | ΔXB22 | ΔXB21 | ΔXB20 | 0 | ΔXB12 | ΔXB11 | ΔXB10 |
| E8h | XB2 | W | 0 | 16'h2211 | 0 | ΔXB82 | ΔXB81 | ΔXB80 | 0 | ΔXB72 | ΔXB71 | ΔXB70 |
| | | | | | 0 | ΔXB62 | ΔXB61 | ΔXB60 | 0 | ΔXB52 | ΔXB51 | ΔXB50 |
| E9h | XB3 | W | 0 | 16'h4433 | 0 | ΔXB122 | ΔXB121 | ΔXB120 | 0 | ΔXB112 | ΔXB111 | ΔXB110 |
| | | | | | 0 | ΔXB102 | ΔXB101 | ΔXB100 | 0 | ΔXB92 | ΔXB91 | ΔXB90 |
| EAh | XB4 | W | 0 | 16'h4444 | 0 | ΔXB162 | ΔXB161 | ΔXB160 | 0 | ΔXB152 | ΔXB151 | ΔXB150 |
| | | | | | 0 | ΔXB142 | ΔXB141 | ΔXB140 | 0 | ΔXB132 | ΔXB131 | ΔXB130 |
| EBh | XB5 | W | 0 | 16'h5555 | 0 | ΔXB202 | ΔXB201 | ΔXB200 | 0 | ΔXB192 | ΔXB191 | ΔXB190 |
| | | | | | 0 | ΔXB182 | ΔXB181 | ΔXB180 | 0 | ΔXB172 | ΔXB171 | ΔXB170 |
| ECh | XB6 | W | 0 | 16'h6666 | 0 | ΔXB242 | ΔXB241 | ΔXB240 | 0 | ΔXB232 | ΔXB231 | ΔXB230 |
| | | | | | 0 | ΔXB222 | ΔXB221 | ΔXB220 | 0 | ΔXB212 | ΔXB211 | ΔXB210 |
| EDh | XB7 | W | 0 | 16'h6666 | 0 | ΔXB282 | ΔXB281 | ΔXB280 | 0 | ΔXB272 | ΔXB271 | ΔXB270 |
| | | | | | 0 | ΔXB262 | ΔXB261 | ΔXB260 | 0 | ΔXB252 | ΔXB251 | ΔXB250 |
| EEh | XB8 | W | 0 | 16'h6666 | 0 | ΔXB322 | ΔXB321 | ΔXB320 | 0 | ΔXB312 | ΔXB311 | ΔXB310 |
| | | | | | 0 | ΔXB302 | ΔXB301 | ΔXB300 | 0 | ΔXB292 | ΔXB291 | ΔXB290 |
| EFh | PENTILEKEY | W | 0 | 16'hXXXX | RSV DF | RSV DE | RSV DD | RSV DC | RSV DB | RSV DA | RSV D9 | RSV D8 |
| | | | | | RSV D7 | RSV D6 | RSV D5 | RSV D4 | RSV D3 | RSV D2 | RSV D1 | RSV D0 |

*Note1) This instruction need to transmission of two times.
Also these registers can't read out through the SDO pin.



Note2) Read operation is possible with only 3-pin SPI

6-1 Index (IR)

| | | | | | | | | | |
|---|---|-----|-----|-----|-----|-----|-----|-----|-----|
| w | 0 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|---|---|-----|-----|-----|-----|-----|-----|-----|-----|

The index instruction specifies indexes. It sets the register number in the range of 00h to EFh in hexadecimal form.

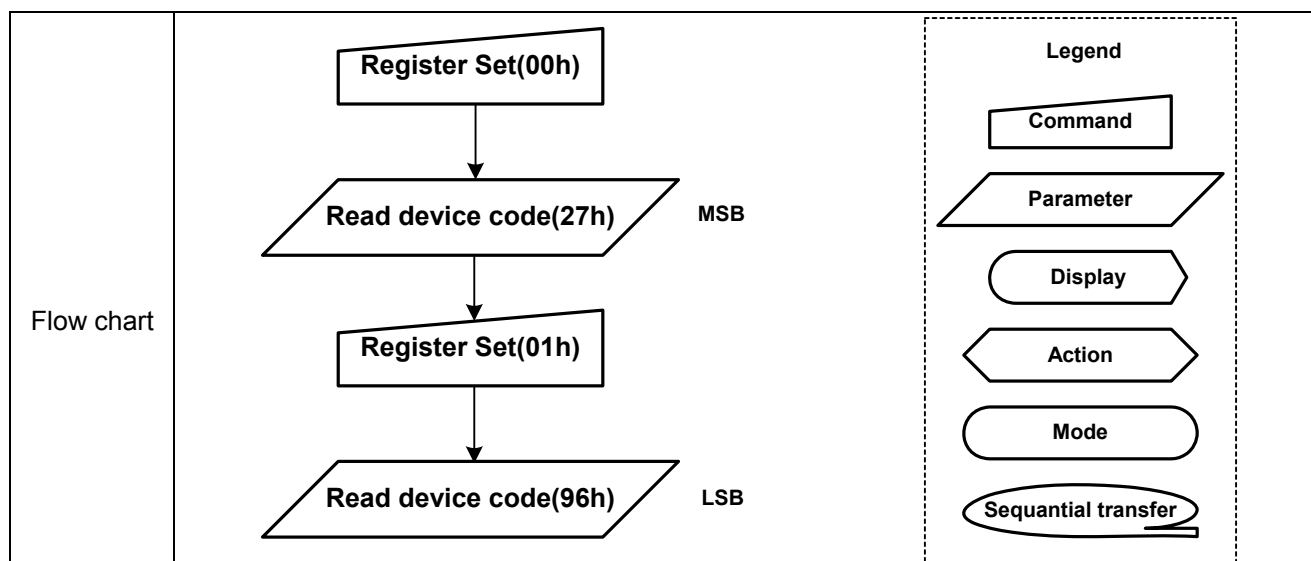
6-2 IC information Read (R00h ~ R02h)

| | | |
|---|---|---------------------------|
| R | 0 | Read data(IC information) |
|---|---|---------------------------|

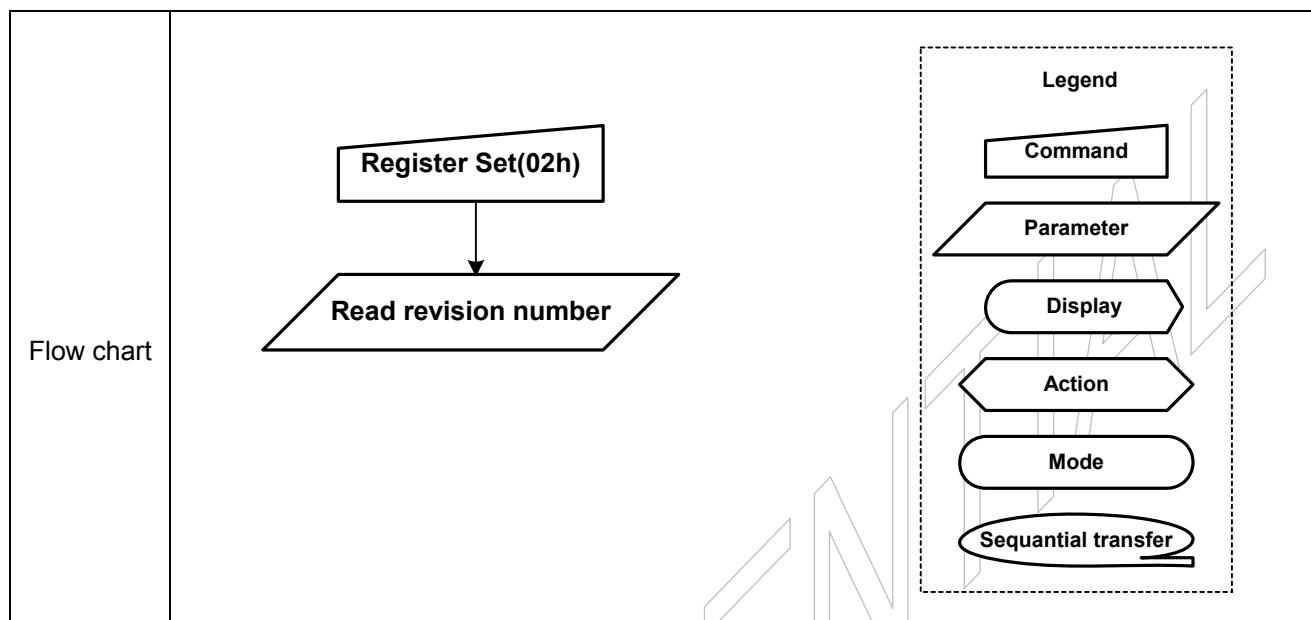
The status and instruction read for IC information.

The first and second word of reading data (R00h / R01h) is device code and the third reading data(R02h) is revision number.

- Sequence of Device code reading



- Sequence of Revision number reading



6-3 Oscillator control (R11h)

| R/W | RS | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|-----|-----|-----|-----|-----|------|-----|-----|
| W | 0 | 1 | 0 | 1 | 0 | 0 | EXTR | EXT | OSC |

OSC : Internal Oscillator On/Off control. When OSC bit set to “1”, internal oscillator is beginning oscillation.

OSC = 0 : Internal oscillator OFF. **(default)**

OSC = 1 : Internal oscillator ON.

EXT : External clock select bit.

EXT=0 : Select internal clock. **(default)**

EXT=1 : Select external clock.

EXTR : Select internal or external resistor for oscillator operation.

EXTR = 0 : Select internal resistor. **(default)**

EXTR = 1 : Select external resistor.

Note) If RESETB is “Low”, oscillator clock is fixed to VSS.

6-4. Display Control 1 (R12h / R13h)

| R/W | RS | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 0 | 0 | 0 | 0 | BP4 | BP3 | BP2 | BP1 | BP0 |
| W | 0 | 0 | 0 | 0 | FP4 | FP3 | FP2 | FP1 | FP0 |

FP4-0/BP4-0: Set the periods of blanking (the front and back porch), which are placed at the beginning and end of the display. FP4-0 is for a front porch and BP4-0 is for a back porch. When a front and back porch are set, the settings should meet the following conditions.

The back-porch (BP) will start on the falling edge of the VSYNC signal and display operation commences at the end of the back-porch period. The front-porch (FP) will start when data for the number of raster-rows specified. During the period between the completion of the front-porch and the next VSYNC signal, the display will remain blank.

| FP4 / BP4 | FP3 / BP3 | FP2 / BP2 | FP1 / BP1 | FP0 / BP0 | Number of lines for the Front / Back Porch |
|-----------|-----------|-----------|-----------|-----------|--|
| 0 | 0 | 0 | 0 | 0 | Setting disable |
| 0 | 0 | 0 | 0 | 1 | |
| 0 | 0 | 0 | 1 | 0 | |
| 0 | 0 | 0 | 1 | 1 | |
| 0 | 0 | 1 | 0 | 0 | 4 |
| 0 | 0 | 1 | 0 | 1 | 5 |
| 0 | 0 | 1 | 1 | 0 | 6 |
| 0 | 0 | 1 | 1 | 1 | 7 |
| 0 | 1 | 0 | 0 | 0 | 8 (default) |
| 0 | 1 | 0 | 0 | 1 | 9 |
| : | : | : | : | : | : |
| : | : | : | : | : | : |
| : | : | : | : | : | : |
| 1 | 1 | 1 | 0 | 0 | 28 |
| 1 | 1 | 1 | 0 | 1 | 29 |
| 1 | 1 | 1 | 1 | 0 | 30 |
| 1 | 1 | 1 | 1 | 1 | 31 |

6-5. Display Control 2 (R14h ~ R16h)

| R/W | RS | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|-----|-----|-----|-----|------|------|-----|-----|
| W | 0 | 0 | 0 | 0 | REV | 0 | 0 | D1 | D0 |
| W | 0 | 0 | 0 | 0 | SS | VSPL | HSPL | DPL | EPL |
| W | 0 | 0 | 0 | PT1 | PT0 | 0 | 0 | CM1 | CM0 |

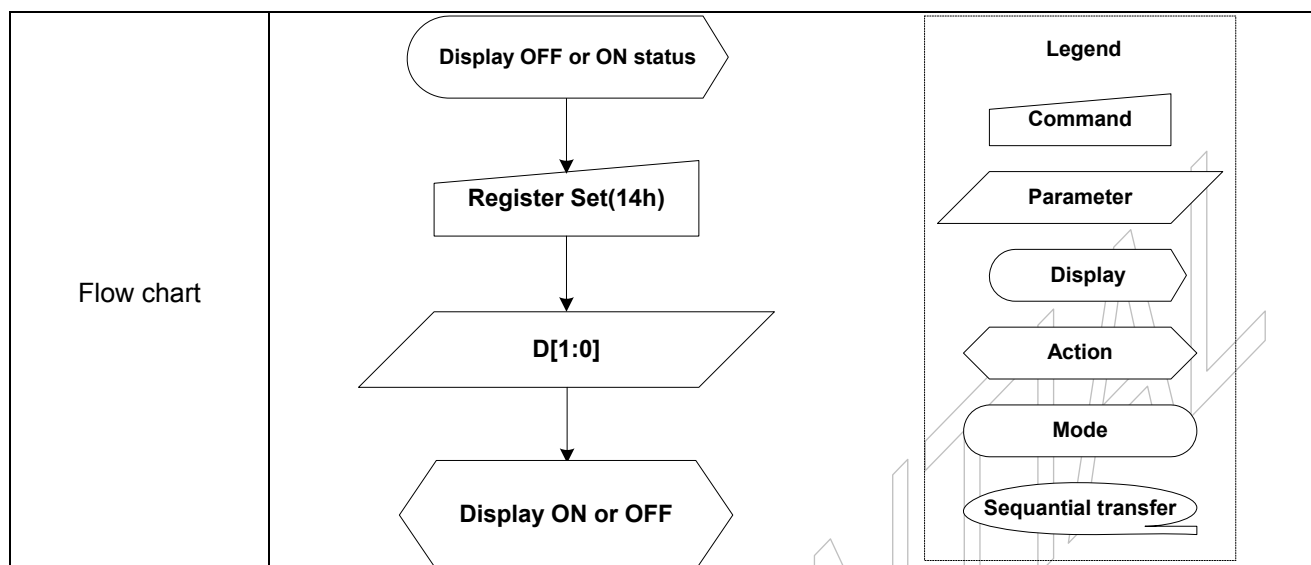
REV: Displays all character and graphics display sections with reversal when REV = 1. Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels.

| REV | Display Data (R / G / B) | Source Output in the Display Area |
|----------------|--------------------------|-----------------------------------|
| 0 (default) | 8'h00 | V0 |
| | 8'h01 | V1 |
| | : | : |
| | : | : |
| | 8'hFE | V254 |
| | 8'hFF | V255 |
| 1 | 8'h00 | V255 |
| | 8'h01 | V254 |
| | : | : |
| | : | : |
| | 8'hFE | V1 |
| | 8'hFF | V0 |

< REV Bit and Source Output Level of Displayed Area >

D1–0: When the D[1:0] set "00", "01" or "10", the source driver outputs have a V0 level. In this case the AMOLED display pattern has a black. When the D[1:0] set "11", source driver outputs have a 256 gray scale level(V0~V255) through source driver (S1~S960)

| D1 | D0 | Source output |
|----|----|---------------|
| 0 | 0 | V0 |
| 0 | 1 | V0 |
| 1 | 0 | V0 |
| 1 | 1 | V0~V255 |



SS: Selects the output shift direction of the source driver.

When SS = 0, S1 shifts to S960. **(default)**

When SS = 1, S960 shifts to S1.

Note) When SS = 1, the SID1-0(RA1h) bit is setting to "01".

VSPL: Invert the polarity of signal for VSYNC.

VSPL = 0: Active low. **(default)**

VSPL = 1: Active high

HSPL: Invert the polarity of signal for HSYNC.

HSPL = 0: Active low. **(default)**

HSPL = 1: Active high

DPL: Invert the polarity of signal for DOTCLK.

DPL = 0: Data are read in synchronization with the rising edge of the DOTCLK. **(default)**

DPL = 1: Data are read in synchronization with the falling edge of the DOTCLK

EPL: Selects the polarity of data enabling signal for using RGB interface.

| EPL | ENABLE | Display data |
|--------------------|--------|--------------|
| 0 (default) | 0 | Valid |
| | 1 | Invalid |
| 1 | 0 | Invalid |
| | 1 | Valid |

< Relationship between EPL, ENABLE >

Set the DPL/EPL bit for timing margin of input signal.

PT1-0: These bits set the source output of non-displayed region. The partial display operation is shown below.

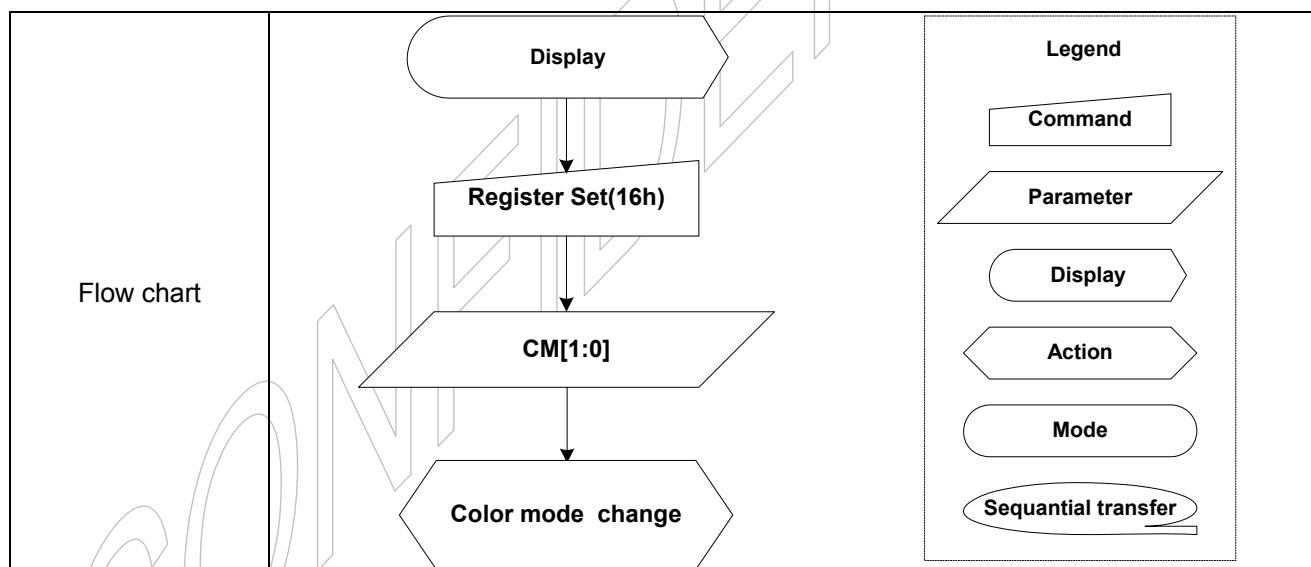
| PT1 | PT0 | REV = 0 | REV = 1 |
|-----|-----|-----------------|-----------------|
| 0 | 0 | V0 (default) | V255 |
| 0 | 1 | V255 | V0 |
| 1 | 0 | V0 | V255 |
| 1 | 1 | Setting disable | Setting disable |

< Source Output of non-Displayed Region >

CM1-0 : Color mode set. These bits assign the data bus for the display color.

| CM1 | CM0 | RGB Interface | Color mode | DB Pin |
|-----|-----|----------------------------|---------------|---------------------|
| 0 | 0 | 24-bit RGB interface | 16M (default) | DB23-0 |
| 0 | 1 | 18-bit RGB interface | 262K | DB23-18, 15-10, 7-2 |
| 1 | 0 | 16-bit RGB interface | 65K | DB23-19, 15-10, 7-3 |
| 1 | 1 | 24/18/16-bit RGB interface | 8 | DB23, 15, 7 |

Note) When setting CM1-0 = "11", all data bits about R, G and B internally connected to MSB of each.



6-6. Power Control 1 (R17h ~ R19h)

| R/W | RS | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|-----|------|------|------|-----|------|------|------|
| W | 0 | 0 | DC12 | DC11 | DC10 | 0 | DC02 | DC01 | DC00 |
| W | 0 | 0 | SAP2 | SAP1 | SAP0 | 0 | AP2 | AP1 | AP0 |
| W | 0 | 0 | 0 | 0 | 0 | 0 | GAP2 | GAP1 | GAP0 |

DC12-0 : Select the boosting frequency for the high voltage generation. If set the boosting frequency high, the efficiency of the boosting circuit will be improved. But the current consumption will increase.

DC02-0 : Select the boosting frequency for the medium voltage generation. If set the boosting frequency high, the efficiency of the boosting circuit will be improved. But the current consumption will increase.

DC1 setting (for High voltage)

| DC12-0 | Boosting clock |
|------------|------------------------------|
| 000 | DOTCLK x 64 |
| 001 | DOTCLK x 128 |
| 010 | DOTCLK x 256(default) |
| 011 | DOTCLK x 512 |
| 100 | DOTCLK x 1024 |
| 101 | DOTCLK x 2048 |
| 110 | Stop |
| 111 | Setting disable |

DC0 setting (for Medium voltage)

| DC02-0 | Boosting clock |
|------------|------------------------------|
| 000 | DOTCLK x 32 |
| 001 | DOTCLK x 64 |
| 010 | DOTCLK x 128(default) |
| 011 | DOTCLK x 256 |
| 100 | DOTCLK x 512 |
| 101 | DOTCLK x 1024 |
| 110 | Stop |
| 111 | Setting disable |

Note) It is necessary to find the best register setting between display quality and current consumption.

SAP2-0 : This instruction adjust the amount of fixed current in the operational amplifier for the source driver. When the amount of fixed current is large, AMOLED driving ability and the display quality become high, but the current consumption is increased. Also this instruction must consider about the display quality and the current consumption

| SAP2-0 | | | Amount of Current in Operational Amplifier |
|----------|----------|----------|--|
| 0 | 0 | 0 | Operation of the operational amplifier and step-up circuit stops |
| 0 | 0 | 1 | Small |
| 0 | 1 | 0 | Small or medium |
| 0 | 1 | 1 | Medium (default) |
| 1 | 0 | 0 | Medium or large |
| 1 | 0 | 1 | Large |
| 1 | 1 | 0 | Setting disabled |
| 1 | 1 | 1 | Setting disabled |

AP2-0 : This instruction adjust regular current flow rate of operation amplifier circuit of AMOLED driving power. If regular current flow rate of operation amplifier is set large, display quality is enhanced due to increased AMOLED driving capacity, while current consumption is also increased. It is necessary to adjust between display quality and current consumption.

| AP2-0 | | | Power op-amp current flow rate |
|----------|----------|----------|--|
| 0 | 0 | 0 | Operation of the operational amplifier halts |
| 0 | 0 | 1 | Small |
| 0 | 1 | 0 | Small or medium |
| 0 | 1 | 1 | Medium (default) |
| 1 | 0 | 0 | Medium or large |
| 1 | 0 | 1 | Large |
| 1 | 1 | 0 | Setting disabled |
| 1 | 1 | 1 | Setting disabled |

GAP2-0 : This instruction adjust regular current flow rate of gray scale op-amp. If gray scale op-amp current flow rate is set large, display quality is enhanced, but current consumption is increased. It is necessary to adjust between display quality and current consumption.

| GAP2-0 | | | Gray scale op-amp current flow rate |
|----------|----------|----------|--|
| 0 | 0 | 0 | Operation of the operational amplifier halts |
| 0 | 0 | 1 | Small |
| 0 | 1 | 0 | Small or medium |
| 0 | 1 | 1 | Medium (default) |
| 1 | 0 | 0 | Medium or large |
| 1 | 0 | 1 | Large |
| 1 | 1 | 0 | Setting disabled |
| 1 | 1 | 1 | Setting disabled |

6-7. Power Control 2 (R1Ah / R1Bh / R1Ch)

| R/W | RS | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|-------|-------|-------|-------|
| W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BT1 | BT0 |
| W | 0 | VGH3 | VGH2 | VGH1 | VGH0 | VGL3 | VGL2 | VGL1 | VGL0 |
| W | 0 | 0 | 0 | 0 | 0 | VINT3 | VINT2 | VINT1 | VINT0 |

BT1-0 : Control the boosting ratio of the DCDC converter circuits.

BT setting table

| BT1-0 | VLOUT1 | VLOUT2 | VLOUT3 |
|-------|-------------|-----------------------|------------------------|
| 00 | VCI1OUT x 2 | VCI1OUT x 3 (default) | VCI1OUT x -3 (default) |
| 01 | | | VCI1OUT x -4 |
| 10 | | VCI1OUT x 4 | VCI1OUT x -3 |
| 11 | | | VCI1OUT x -4 |

VGH3-0 : Set VGH(High Voltage Level for Gate).

| VGH3 | VGH2 | VGH1 | VGH0 | VGH Voltage Value |
|------|------|------|------|-------------------|
| 0 | 0 | 0 | 0 | 4.60V |
| 0 | 0 | 0 | 1 | 4.80V |
| 0 | 0 | 1 | 0 | 5.00V |
| 0 | 0 | 1 | 1 | 5.20V (default) |
| 0 | 1 | 0 | 0 | 5.40V |
| 0 | 1 | 0 | 1 | 5.60V |
| 0 | 1 | 1 | 0 | 5.80V |
| 0 | 1 | 1 | 1 | 6.00V |
| 1 | 0 | 0 | 0 | 6.20V |
| 1 | 0 | 0 | 1 | 6.40V |
| 1 | 0 | 1 | 0 | 6.60V |
| 1 | 0 | 1 | 1 | Setting disable |
| 1 | 1 | 0 | 0 | |
| 1 | 1 | 0 | 1 | |
| 1 | 1 | 1 | 0 | |
| 1 | 1 | 1 | 1 | |

< VGH Bits and VGH Voltage >

VGL3-0 : Set VGL(Low Voltage Level for Gate).

| VGL3 | VGL2 | VGL1 | VGL0 | VGL Voltage Value |
|----------|----------|----------|----------|-------------------------|
| 0 | 0 | 0 | 0 | -5.00V |
| 0 | 0 | 0 | 1 | -5.20V |
| 0 | 0 | 1 | 0 | -5.40V |
| 0 | 0 | 1 | 1 | -5.60V |
| 0 | 1 | 0 | 0 | -5.80V |
| 0 | 1 | 0 | 1 | -6.00V |
| 0 | 1 | 1 | 0 | -6.20V |
| 0 | 1 | 1 | 1 | -6.40V |
| 1 | 0 | 0 | 0 | -6.60V |
| 1 | 0 | 0 | 1 | -6.80V |
| 1 | 0 | 1 | 0 | -7.00V (default) |
| 1 | 0 | 1 | 1 | -7.20V |
| 1 | 1 | 0 | 0 | -7.40V |
| 1 | 1 | 0 | 1 | -7.60V |
| 1 | 1 | 1 | 0 | -7.80V |
| 1 | 1 | 1 | 1 | Setting disable |

< VGL Bits and VGL Voltage >

VINT3-0: Set VINT(control voltage of OLED Panel).

| VINT3 | VINT2 | VINT1 | VINT0 | VINT Voltage Value |
|----------|----------|----------|----------|-------------------------|
| 0 | 0 | 0 | 0 | -1.00V |
| 0 | 0 | 0 | 1 | -1.20V |
| 0 | 0 | 1 | 0 | -1.40V |
| 0 | 0 | 1 | 1 | -1.60V |
| 0 | 1 | 0 | 0 | -1.80V |
| 0 | 1 | 0 | 1 | -2.00V (default) |
| 0 | 1 | 1 | 0 | -2.20V |
| 0 | 1 | 1 | 1 | -2.40V |
| 1 | 0 | 0 | 0 | -2.60V |
| 1 | 0 | 0 | 1 | -2.80V |
| 1 | 0 | 1 | 0 | -3.00V |
| 1 | 0 | 1 | 1 | -3.20V |
| 1 | 1 | 0 | 0 | -3.40V |
| 1 | 1 | 0 | 1 | -3.60V |
| 1 | 1 | 1 | 0 | -3.80V |
| 1 | 1 | 1 | 1 | -4.00V |

< VINT Bits and VINT Voltage >

6-8. Power Control 3 (R1Dh)

| R/W | RS | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | STB |

STB: When STB set the “H” (**default**), the IC enters the standby mode, where display operation completely stops, halting all the internal operations.

This command has no effect when module is already in Standby In mode. Standby In mode can only be left by the Standby Out command (R1Dh).

It will be necessary to wait 200msec after sending Standby Out command (when in Standby In mode) before Standby In command can be sent. For details, see the Standby Mode ON/OFF flow.

6-9. VREF Control (R21h)

| R/W | RS | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|-----|-----|-----|-----|-----|--------|-----|-----|
| W | 0 | 0 | 0 | 0 | 0 | 0 | REF_MD | 0 | 0 |

REF_MD : Select CMOS or BJT type for VREF voltage generation. Internal power generation for AMOLED display based on the VREF voltage. When REF_MD = 1, VREF voltage is generation through BJT circuit. Default value of REF_MD is “0” and VREF voltage is generation through CMOS circuit.

6-10. Logic voltage control (R22h)

| R/W | RS | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|-----|-----|-----|-----|-----|------|------|------|
| W | 0 | 1 | 0 | 1 | 0 | 0 | SVL2 | SVL1 | SVL0 |

SVL2-0 : Internal logic voltage(VCCL) control(default : "100")

| VCC | | | | 2.4V | 2.5 V | 2.6 V | 2.7 V | 2.8 V | 2.9 V | 3.0 V |
|--------|---|---|----------------------|------|-------|-------|--------|-------|--------|-------|
| SVL2-0 | | | | | | | | | | |
| 0 | 0 | 0 | VCC x 0.45 | - | - | - | - | - | - | - |
| 0 | 0 | 1 | VCC x 0.50 | - | - | - | - | - | - | - |
| 0 | 1 | 0 | VCC x 0.55 | - | - | - | - | - | - | - |
| 0 | 1 | 1 | VCC x 0.60 | - | - | - | - | - | - | 1.8V |
| 1 | 0 | 0 | VCC x 0.65 (default) | - | - | - | - | 1.82V | 1.88 V | - |
| 1 | 0 | 1 | VCC x 0.70 | - | - | 1.82V | 1.89 V | - | - | - |
| 1 | 1 | 0 | VCC x 0.75 | 1.8V | 1.87V | - | - | - | - | - |
| 1 | 1 | 1 | VCC x 0.80 | - | - | - | - | - | - | - |

Note) We recommend VCCL voltage range by 1.75~1.9V, so you must change the SVL[2:0] value according to your VCC voltage level.

6-11. Power control 4 (R23h / R24h)

| R/W | RS | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|-----|------|------|------|------|------|------|------|
| W | 0 | 0 | 0 | 0 | 0 | 0 | VC2 | VC1 | VC0 |
| W | 0 | 0 | VRH2 | VRH1 | VRH0 | VRG3 | VRG2 | VRG1 | VRG0 |

VC2-0 : VCI1OUT setting

| VC2-0 | VCI1OUT |
|-------|----------------------|
| 0 0 0 | VCI X 0.98 (default) |
| 0 0 1 | VCI X 0.96 |
| 0 1 0 | VCI X 0.94 |
| 0 1 1 | VCI X 0.92 |
| 1 0 0 | VCI X 0.90 |
| 1 0 1 | VCI X 0.88 |
| 1 1 0 | VCI X 0.86 |
| 1 1 1 | VCI X 0.84 |

VRH2-0 : VREG2OUT setting

| VRH2-0 | VREG2OUT |
|--------|-----------------|
| 0 0 0 | 4.3 V |
| 0 0 1 | 4.4 V |
| 0 1 0 | 4.5 V |
| 0 1 1 | 4.6 V |
| 1 0 0 | 4.8 V |
| 1 0 1 | 5.0 V |
| 1 1 0 | 5.2 V |
| 1 1 1 | 5.4 V (default) |

VRG3-0 : VREG1OUT setting

| VRG3-0 | VREG1OUT |
|---------|-----------------|
| 0 0 0 0 | 3.5 V |
| 0 0 0 1 | 3.6 V |
| 0 0 1 0 | 3.7 V |
| 0 0 1 1 | 3.8 V |
| : | : |
| 0 1 1 1 | 4.2 V (default) |
| : | : |
| 1 1 0 1 | 4.8 V |
| 1 1 1 0 | 4.9 V |
| 1 1 1 1 | 5.0 V |

6-12. Display control 3 (R26h / R27h)

| R/W | RS | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|-----|-----|-----|-----|-----|-----|------|------|
| W | 0 | 1 | 0 | 1 | 0 | 0 | 0 | DMD1 | DMD0 |
| W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SOE | PCS |

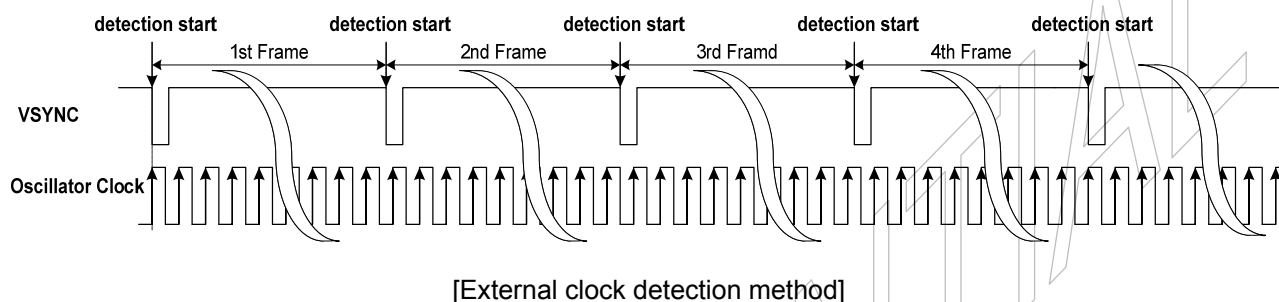
DMD1-0 : Reference clock selection for LTPS signal generation. When DMD1-0 set "00", LTPS timing clock for AMOLED use a DOTCLK. The LTPS timing clock is depend on the external clock frequency (frame frequency) and LTPS signal pulse width for AMOLDE is variable according to the external clock frequency.

If DMD1-0 = "01", external clock frequency(frame frequency) is automatically detected by internal oscillator clock and LTPS signal pulse width is fixed by SCWE register value, regardless of external clock frequency, or else LTPS signal for AMOLDE is generated by internal oscillator clock.

| DMD1 | DMD0 | Reference clock |
|------|------|--|
| 0 | 0 | DOTCLK (default) |
| 0 | 1 | DOTCLK(frame frequency auto detection) |
| 1 | 0 | Internal Oscillator |
| 1 | 1 | Setting disable |

- Auto detection method for frame frequency

| External clock frequency (Frame frequency) | IC operation frequency |
|---|------------------------|
| More than 56Hz | 60Hz operation |
| From 46Hz to 55Hz | 50Hz operation |
| Less than 45Hz | 40Hz operation |



If DMD1-0 = "01" or DMD1-0 = "10", this instruction is applied to the following LTPS signals, and pulse width of LTPS signals are not depend on the "Frame frequency" but depend on the "Oscillator frequency"

| Pad name | CMOS | Latch | PMOS-1 | PMOS-2 |
|----------|--------------|--------------|--------------|--------------|
| | GTCON = "00" | GTCON = "01" | GTCON = "10" | GTCON = "11" |
| FLM | X | X | O | O |
| CLK1 | X | O | O | O |
| CLK2 | X | O | O | O |
| CLK3 | O | O | O | O |
| CLK4 | O | O | X | X |
| EM_FLM | X | X | X | X |
| EM_CLK1 | X | X | X | X |
| EM_CLK1B | X | X | X | X |
| EM_CLK2 | X | X | X | X |
| EM_CLK2B | X | X | X | X |
| ESR | X | X | X | X |

X : not applied , O : applied

PCS : Select power sequence mode about AMOLED gate less signal for PMOS type. Gate less signal of each PMOS type have two power sequences modes. This command would be selected by sequence characteristic to AMOLED panel display. The timing for the gate less signals on/off is changed by this command.

PCS = 0 : power sequence mode 1 (default)

PCS = 1 : power sequence mode 2

SOE : Select the start type of Pentile. If the first display input data is transferred to R/G/B/G format of panel, set SOE=0. And if the first display input data is transferred to B/G/R/G format of panel, set SOE=1.

SOE = 0 : Transmission to R/G/B/G format with first display input data (default)

SOE = 1 : Transmission to B/G/R/G format with first display input data

6-13. Display control 4 (R28h / R29h)

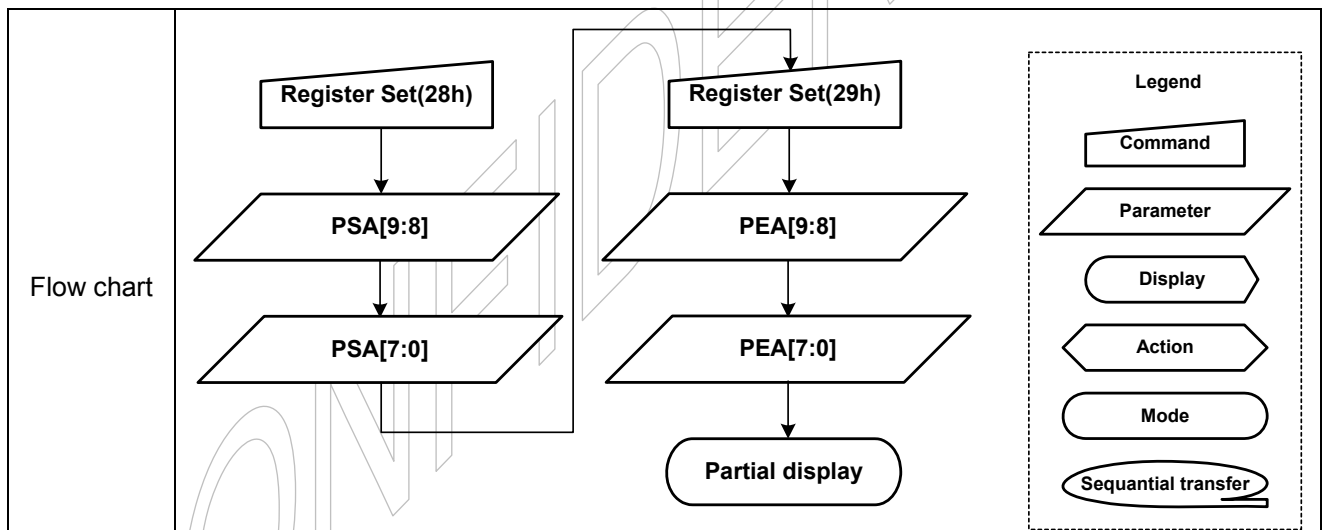
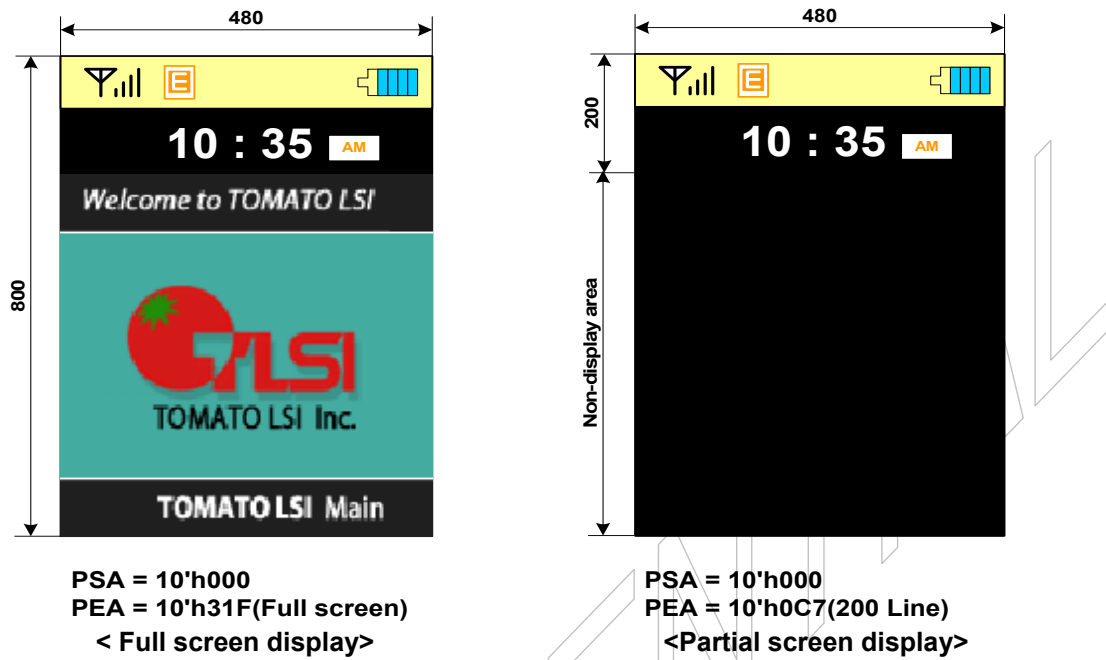
| R/W | RS | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|------|------|
| W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PSA9 | PSA8 |
| | | PSA7 | PSA6 | PSA5 | PSA4 | PSA3 | PSA2 | PSA1 | PSA0 |
| W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PEA9 | PEA8 |
| | | PEA7 | PEA6 | PEA5 | PEA4 | PEA3 | PEA2 | PEA1 | PEA0 |

PSA9-0 : This register set starting position for the partial area.

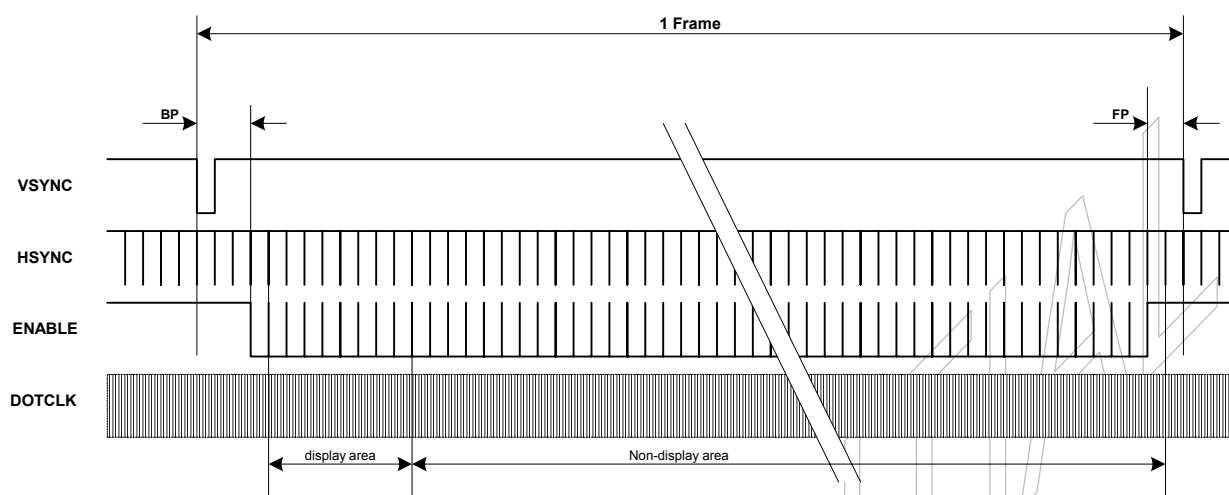
PEA9-0 : This register set ending position for the partial area.

| PSA9-0 | Starting position |
|----------------|---------------------|
| 10'h000 | G1 (default) |
| 10'h001 | G2 |
| 10'h002 | G3 |
| 10'h003 | G4 |
| 10'h004 | G5 |
| 10'h005 | G6 |
| 10'h006 | G7 |
| 10'h007 | G8 |
| 10'h008 | G9 |
| 10'h009 | G10 |
| : | : |
| : | : |
| : | : |
| : | : |
| : | : |
| : | : |
| 10'h31D | G798 |
| 10'h31E | G799 |
| 10'h31F | G800 |
| : | : |
| : | : |
| : | : |
| 10'h35E | G863 |
| 10'h35F | G864 |
| others | Setting disable |

| PEA9-0 | Ending position |
|----------------|-----------------------|
| 10'h000 | Setting disable |
| 10'h001 | |
| 10'h002 | |
| 10'h003 | |
| 10'h004 | |
| 10'h005 | |
| 10'h006 | |
| 10'h007 | |
| 10'h008 | G9 |
| 10'h009 | G10 |
| : | : |
| : | : |
| : | : |
| : | : |
| : | : |
| 10'h31D | G798 |
| 10'h31E | G799 |
| 10'h31F | G800 (default) |
| : | : |
| : | : |
| : | : |
| 10'h35E | G863 |
| 10'h35F | G864 |
| others | Setting disable |



Instruction setting method for partial display start/end line



Note 1) Minimum partial display area is 8-line($PEA - PSA \geq 8$)

Note 2) Source outputs about the Non-display area is fixed by PT[1:0] setting value.

6-14. Gate-less signal Control (R30h ~ R32h)

| R/W | RS | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|-----|-----|-----|-------|-------|-------|--------|--------|
| W | 0 | 0 | 0 | DL1 | DL0 | 0 | 0 | GTCON1 | GTCON0 |
| W | 0 | 0 | 0 | 0 | SCTE4 | SCTE3 | SCTE2 | SCTE1 | SCTE0 |
| W | 0 | 0 | 0 | 0 | SCWE4 | SCWE3 | SCWE2 | SCWE1 | SCWE0 |

DL1-0 : Selection display line. This register selects the total display line. A LTPS signals limited by DL register.

DL = 00 : 800 line display. **(default)**

DL = 01 : 854 line display.

DL = 10 : 864 line display.

DL = 11 : setting disable.

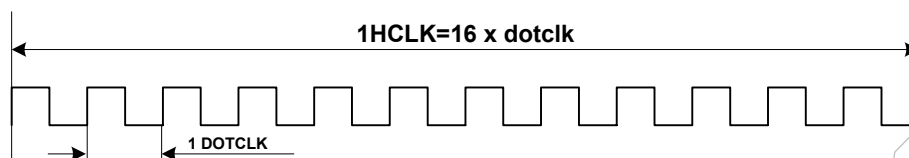
GTCON1-0 : These bits set the waveform of the gate-less signal for the AMOLED. The TL2796 support the four type waveform of gate-less signal for the AMOLED.

| GTCON1-0 | | LTPS Type | Gate-less signal Type |
|----------|----------|---------------|-------------------------|
| 0 | 0 | CMOS | Type A |
| 0 | 1 | Latch | Type B |
| 1 | 0 | PMOS-1 | Type C (default) |
| 1 | 1 | PMOS-2 | Type D |

| LTPS Mode PAD Name | CMOS | Latch | PMOS-1 | PMOS-2 |
|-----------------------|--------------|--------------|--------------|--------------|
| | GTCON = "00" | GTCON = "01" | GTCON = "10" | GTCON = "11" |
| FLM | FLM | FLM | FLM | FLM |
| SFTCLKB(CLK1) | SFTCLKB | CL1 | CLK1 | CLK1 |
| SFTCLK(CLK2) | SFTCLK | CL2 | CLK2 | CLK2 |
| SCLK2(CLK3) | SCLK2 | CL3 | CLK3 | CLK3 |
| SCLK1 | SCLK1 | CL4 | - | - |
| ESR | ESR | ESR | ESR | ESR |
| EM_CLK2B | - | - | EM_CLK2B | EM_CLK2B |
| EM_CLK2 | - | - | EM_CLK2 | EM_CLK2 |
| EM_CLK1B | ACL_CLKB | ACL_CLKB | EM_CLK1B | EM_CLK1B |
| EM_CLK1 | ACL_CLK | ACL_CLK | EM_CLK1 | EM_CLK1 |
| EM_FLM | ACL_FLM | ACL_FLM | EM_FLM | EM_FLM |

TL2796

**960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout**
SCTE4-0 : Specify the rising position of FLM, CLK1, CLK2 and CLK3

SCWE4-0 : Specify the pulse width of FLM, CLK1, CLK2 and CLK3


| SCTE4-0 | Rising delay Time |
|------------------|---------------------------|
| 0 0 0 0 0 | 0 x HCLK |
| 0 0 0 0 1 | 1 x HCLK |
| 0 0 0 1 0 | 2 x HCLK |
| 0 0 0 1 1 | 3 x HCLK |
| 0 0 1 0 0 | 4 x HCLK |
| 0 0 1 0 1 | 5 x HCLK |
| 0 0 1 1 0 | 6 x HCLK |
| 0 0 1 1 1 | 7 x HCLK |
| 0 1 0 0 0 | 8 x HCLK (default) |
| 0 1 0 0 1 | 9 x HCLK |
| 0 1 0 1 0 | 10 x HCLK |
| 0 1 0 1 1 | 11 x HCLK |
| 0 1 1 0 0 | 12 x HCLK |
| 0 1 1 0 1 | 13 x HCLK |
| 0 1 1 1 0 | 14 x HCLK |
| 0 1 1 1 1 | 15 x HCLK |
| 1 0 0 0 0 | 16 x HCLK |
| 1 0 0 0 1 | 17 x HCLK |
| 1 0 0 1 0 | 18 x HCLK |
| 1 0 0 1 1 | 19 x HCLK |
| 1 0 1 0 0 | 20 x HCLK |
| 1 0 1 0 1 | 21 x HCLK |
| 1 0 1 1 0 | 22 x HCLK |
| 1 0 1 1 1 | 23 x HCLK |
| 1 1 0 0 0 | 24 x HCLK |
| 1 1 0 0 1 | 25 x HCLK |
| 1 1 0 1 0 | 26 x HCLK |
| 1 1 0 1 1 | 27 x HCLK |
| 1 1 1 0 0 | 28 x HCLK |
| 1 1 1 0 1 | 29 x HCLK |
| 1 1 1 1 0 | 30 x HCLK |
| 1 1 1 1 1 | 31 x HCLK |

| SCWE4-0 | High Time |
|------------------|----------------------------|
| 0 0 0 0 0 | 0 x HCLK |
| 0 0 0 0 1 | 1 x HCLK |
| 0 0 0 1 0 | 2 x HCLK |
| 0 0 0 1 1 | 3 x HCLK |
| 0 0 1 0 0 | 4 x HCLK |
| 0 0 1 0 1 | 5 x HCLK |
| 0 0 1 1 0 | 6 x HCLK |
| 0 0 1 1 1 | 7 x HCLK |
| 0 1 0 0 0 | 8 x HCLK |
| 0 1 0 0 1 | 9 x HCLK |
| 0 1 0 1 0 | 10 x HCLK |
| 0 1 0 1 1 | 11 x HCLK |
| 0 1 1 0 0 | 12 x HCLK |
| 0 1 1 0 1 | 13 x HCLK |
| 0 1 1 1 0 | 14 x HCLK |
| 0 1 1 1 1 | 15 x HCLK |
| 1 0 0 0 0 | 16 x HCLK |
| 1 0 0 0 1 | 17 x HCLK |
| 1 0 0 1 0 | 18 x HCLK |
| 1 0 0 1 1 | 19 x HCLK |
| 1 0 1 0 0 | 20 x HCLK (default) |
| 1 0 1 0 1 | 21 x HCLK |
| 1 0 1 1 0 | 22 x HCLK |
| 1 0 1 1 1 | 23 x HCLK |
| 1 1 0 0 0 | 24 x HCLK |
| 1 1 0 0 1 | 25 x HCLK |
| 1 1 0 1 0 | 26 x HCLK |
| 1 1 0 1 1 | 27 x HCLK |
| 1 1 1 0 0 | 28 x HCLK |
| 1 1 1 0 1 | 29 x HCLK |
| 1 1 1 1 0 | 30 x HCLK |
| 1 1 1 1 1 | 31 x HCLK |

6-15. ACL Control (R35h)

| R/W | RS | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|-----|-----|-----|-------|-----|-----|-------|-------|
| W | 0 | 0 | 0 | 0 | ACLON | 0 | 0 | ACLM1 | ACLM0 |

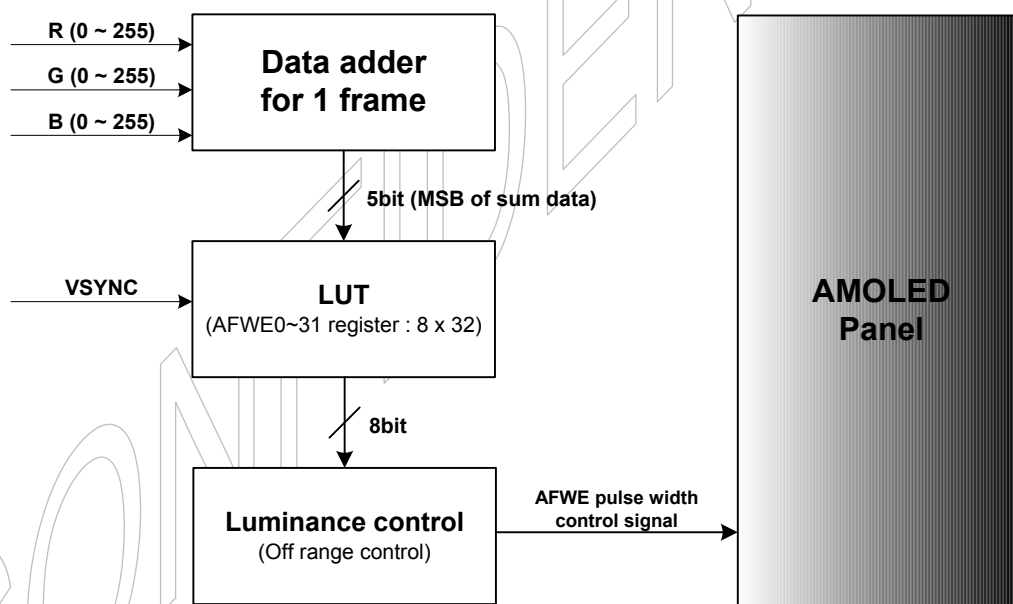
ACLON : ACL on/off control.

When ACLON = 0, ACL Off (default)

When ACLON = 1, ACL On.

ACLM1-0 : ACL control bit.

| ACLM1-0 | | Duty |
|---------|---|-------------|
| 0 | 0 | 1 (default) |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 6 |



6-16. ACL Pulse width control (R90h ~ R9Fh)

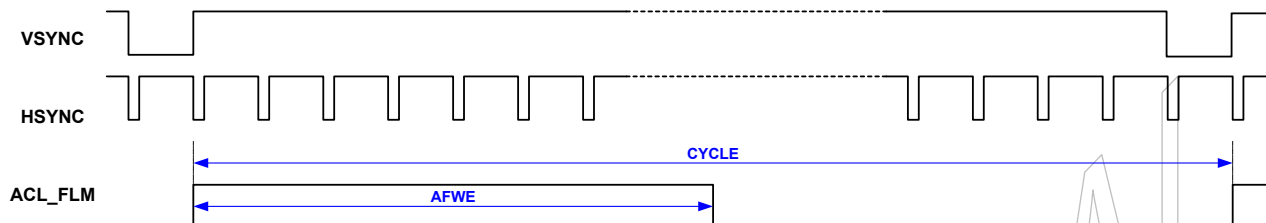
| R/W | RS | Reg No. | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| W | 0 | 90h | AFWE07 | AFWE06 | AFWE05 | AFWE04 | AFWE03 | AFWE02 | AFWE01 | AFWE00 |
| | | | AFWE17 | AFWE16 | AFWE15 | AFWE14 | AFWE13 | AFWE12 | AFWE11 | AFWE10 |
| | | 91h | AFWE27 | AFWE26 | AFWE25 | AFWE24 | AFWE23 | AFWE22 | AFWE21 | AFWE20 |
| | | | AFWE37 | AFWE36 | AFWE35 | AFWE34 | AFWE33 | AFWE32 | AFWE31 | AFWE30 |
| | | 92h | AFWE47 | AFWE46 | AFWE45 | AFWE44 | AFWE43 | AFWE42 | AFWE41 | AFWE40 |
| | | | AFWE57 | AFWE56 | AFWE55 | AFWE54 | AFWE53 | AFWE52 | AFWE51 | AFWE50 |
| | | 93h | AFWE67 | AFWE66 | AFWE65 | AFWE64 | AFWE63 | AFWE62 | AFWE61 | AFWE60 |
| | | | AFWE77 | AFWE76 | AFWE75 | AFWE74 | AFWE73 | AFWE72 | AFWE71 | AFWE70 |
| | | 94h | AFWE87 | AFWE86 | AFWE85 | AFWE84 | AFWE83 | AFWE82 | AFWE81 | AFWE80 |
| | | | AFWE97 | AFWE96 | AFWE95 | AFWE94 | AFWE93 | AFWE92 | AFWE91 | AFWE90 |
| | | 95h | AFWE107 | AFWE106 | AFWE105 | AFWE104 | AFWE103 | AFWE102 | AFWE101 | AFWE100 |
| | | | AFWE117 | AFWE116 | AFWE115 | AFWE114 | AFWE113 | AFWE112 | AFWE111 | AFWE110 |
| | | 96h | AFWE127 | AFWE126 | AFWE125 | AFWE124 | AFWE123 | AFWE122 | AFWE121 | AFWE120 |
| | | | AFWE137 | AFWE136 | AFWE135 | AFWE134 | AFWE133 | AFWE132 | AFWE131 | AFWE130 |
| | | 97h | AFWE147 | AFWE146 | AFWE145 | AFWE144 | AFWE143 | AFWE142 | AFWE141 | AFWE140 |
| | | | AFWE157 | AFWE156 | AFWE155 | AFWE154 | AFWE153 | AFWE152 | AFWE151 | AFWE150 |
| | | 98h | AFWE167 | AFWE166 | AFWE165 | AFWE164 | AFWE163 | AFWE162 | AFWE161 | AFWE160 |
| | | | AFWE177 | AFWE176 | AFWE175 | AFWE174 | AFWE173 | AFWE172 | AFWE171 | AFWE170 |
| | | 99h | AFWE187 | AFWE186 | AFWE185 | AFWE184 | AFWE183 | AFWE182 | AFWE181 | AFWE180 |
| | | | AFWE197 | AFWE196 | AFWE195 | AFWE194 | AFWE193 | AFWE192 | AFWE191 | AFWE190 |
| | | 9Ah | AFWE207 | AFWE206 | AFWE205 | AFWE204 | AFWE203 | AFWE202 | AFWE201 | AFWE200 |
| | | | AFWE217 | AFWE216 | AFWE215 | AFWE214 | AFWE213 | AFWE212 | AFWE211 | AFWE210 |
| | | 9Bh | AFWE227 | AFWE226 | AFWE225 | AFWE224 | AFWE223 | AFWE222 | AFWE221 | AFWE220 |
| | | | AFWE237 | AFWE236 | AFWE235 | AFWE234 | AFWE233 | AFWE232 | AFWE231 | AFWE230 |
| | | 9Ch | AFWE247 | AFWE246 | AFWE245 | AFWE244 | AFWE243 | AFWE242 | AFWE241 | AFWE240 |
| | | | AFWE257 | AFWE256 | AFWE255 | AFWE254 | AFWE253 | AFWE252 | AFWE251 | AFWE250 |
| | | 9Dh | AFWE267 | AFWE266 | AFWE265 | AFWE264 | AFWE263 | AFWE262 | AFWE261 | AFWE260 |
| | | | AFWE277 | AFWE276 | AFWE275 | AFWE274 | AFWE273 | AFWE272 | AFWE271 | AFWE270 |
| | | 9Eh | AFWE287 | AFWE286 | AFWE285 | AFWE284 | AFWE283 | AFWE282 | AFWE281 | AFWE280 |
| | | | AFWE297 | AFWE296 | AFWE295 | AFWE294 | AFWE293 | AFWE292 | AFWE291 | AFWE290 |
| | | 9Fh | AFWE307 | AFWE306 | AFWE305 | AFWE304 | AFWE303 | AFWE302 | AFWE301 | AFWE300 |
| | | | AFWE317 | AFWE316 | AFWE315 | AFWE314 | AFWE313 | AFWE312 | AFWE311 | AFWE310 |

| AFWE0~15 [7:0] | Initial value | Width(Off range) |
|----------------|---------------|------------------|
| AFWE0 | 01h | 2 x HSYNC |
| AFWE1 | 03h | 6 x HSYNC |
| AFWE2 | 05h | 10 x HSYNC |
| AFWE3 | 07h | 14 x HSYNC |
| AFWE4 | 09h | 18 x HSYNC |
| AFWE5 | 0Bh | 22 x HSYNC |
| AFWE6 | 0Dh | 26 x HSYNC |
| AFWE7 | 0Fh | 30 x HSYNC |
| AFWE8 | 11h | 34 x HSYNC |
| AFWE9 | 13h | 38 x HSYNC |
| AFWE10 | 15h | 42 x HSYNC |
| AFWE11 | 17h | 46 x HSYNC |
| AFWE12 | 19h | 50 x HSYNC |
| AFWE13 | 1Bh | 54 x HSYNC |
| AFWE14 | 1Dh | 58 x HSYNC |
| AFWE15 | 1Fh | 62 x HSYNC |

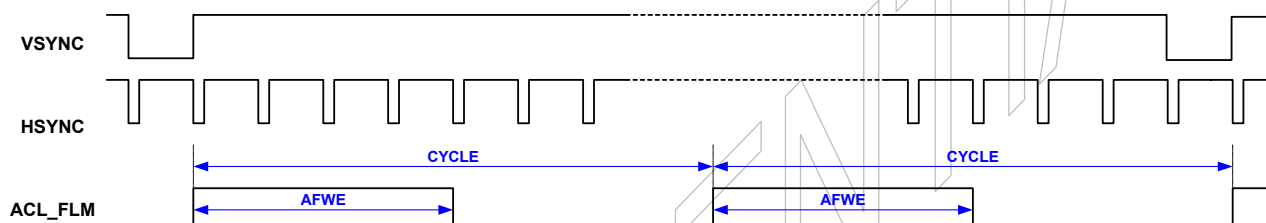
| AFWE16~31 [7:0] | Initial value | Width(Off range) |
|-----------------|---------------|------------------|
| AFWE16 | 21h | 66 x HSYNC |
| AFWE17 | 23h | 70 x HSYNC |
| AFWE18 | 25h | 74 x HSYNC |
| AFWE19 | 27h | 78 x HSYNC |
| AFWE20 | 29h | 82 x HSYNC |
| AFWE21 | 2Bh | 86 x HSYNC |
| AFWE22 | 2Dh | 90 x HSYNC |
| AFWE23 | 2Fh | 94 x HSYNC |
| AFWE24 | 31h | 98 x HSYNC |
| AFWE25 | 33h | 102 x HSYNC |
| AFWE25 | 35h | 106 x HSYNC |
| AFWE27 | 37h | 110 x HSYNC |
| AFWE28 | 39h | 114 x HSYNC |
| AFWE29 | 3Bh | 118 x HSYNC |
| AFWE30 | 3Dh | 122 x HSYNC |
| AFWE31 | 3Fh | 126 x HSYNC |

AFWE0-31 initial value

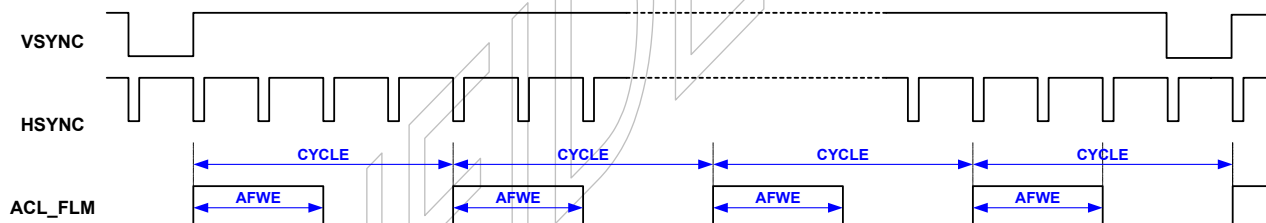
- 1-cycle Timing Diagram (ACLM1-0 = 2'b00)



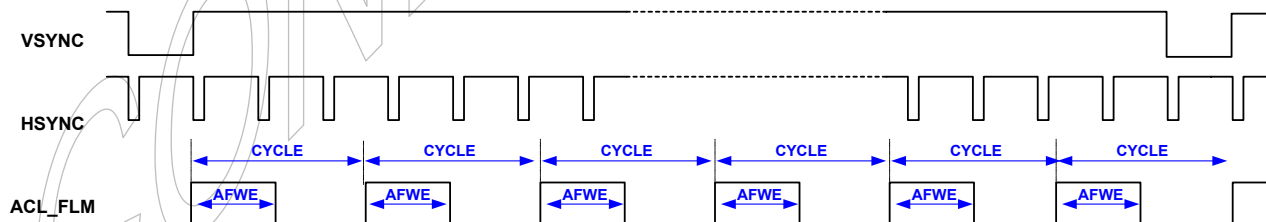
- 2-cycle Timing Diagram (ACLM1-0 = 2'b01)



- 4-cycle Timing Diagram (ACLM1-0 = 2'b10)



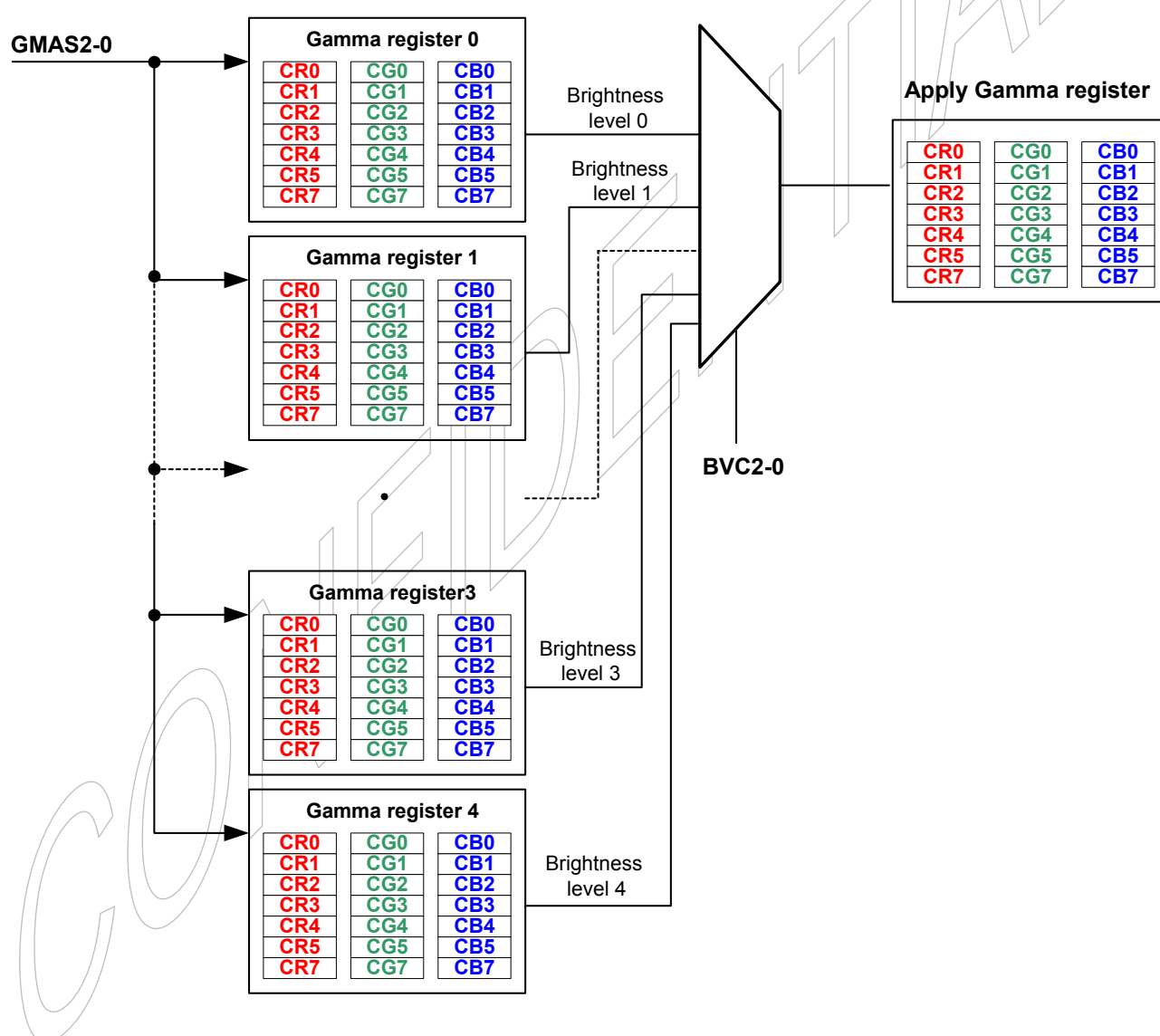
- 6-cycle Timing Diagram (ACLM1-0 = 2'b11)



6-17. Brightness control (R39h)

| R/W | RS | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|-----|------|------|------|-----|-------|-------|-------|
| W | 0 | 0 | BVC2 | BVC1 | BVC0 | 0 | GMAS2 | GMAS1 | GMAS0 |

TL2796 have five gamma register set for brightness control.



BVC2-0 : Display brightness control.

| BVC2-0 | | | Operation |
|--------|---|---|-------------------------------------|
| 0 | 0 | 0 | Brightness Level 0 |
| 0 | 0 | 1 | Brightness Level 1 |
| 0 | 1 | 0 | Brightness Level 2 |
| 0 | 1 | 1 | Brightness Level 3 |
| 1 | 0 | 0 | Brightness Level 4 (default) |
| 1 | 0 | 1 | Setting disable |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

GMAS2-0 : Gamma register selection for display brightness control.

| GMAS2-0 | | | Operation |
|---------|---|---|-----------------------------------|
| 0 | 0 | 0 | Gamma Register 0 |
| 0 | 0 | 1 | Gamma Register 1 |
| 0 | 1 | 0 | Gamma Register 2 |
| 0 | 1 | 1 | Gamma Register 3 |
| 1 | 0 | 0 | Gamma Register 4 (default) |
| 1 | 0 | 1 | Setting disable |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

6-18. Gamma adjustment for R-gray (R40h ~ R46h)

| R/W | RS | | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|-----|------|------|------|------|------|------|------|------|
| W | 0 | 40h | 0 | 0 | 0 | 0 | CR03 | CR02 | CR01 | CR00 |
| W | 0 | 41h | 0 | 0 | CR15 | CR14 | CR13 | CR12 | CR11 | CR10 |
| W | 0 | 42h | 0 | 0 | CR25 | CR24 | CR23 | CR22 | CR21 | CR20 |
| W | 0 | 43h | 0 | 0 | CR35 | CR34 | CR33 | CR32 | CR31 | CR30 |
| W | 0 | 44h | 0 | 0 | CR45 | CR44 | CR43 | CR42 | CR41 | CR40 |
| W | 0 | 45h | 0 | 0 | CR55 | CR54 | CR53 | CR52 | CR51 | CR50 |
| W | 0 | 46h | CR67 | CR66 | CR65 | CR64 | CR63 | CR62 | CR61 | CR60 |

CR0[3:0] : Gamma adjustment register for the R output (V0)**CR1[5:0]** : Gamma curve adjustment register for the R output (V5)**CR2[5:0]** : Gamma curve adjustment register for the R output (V15)**CR3[5:0]** : Gamma curve adjustment register for the R output (V31)**CR4[5:0]** : Gamma curve adjustment register for the R output (V63)**CR5[5:0]** : Gamma curve adjustment register for the R output (V127)**CR6[7:0]** : Gamma adjustment register for the R output (V255)

For details, see the Gamma Adjustment Function.

6-19. Gamma adjustment for G-gray (R50h ~ R56h)

| R/W | RS | | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|-----|------|------|------|------|------|------|------|------|
| W | 0 | 50h | 0 | 0 | 0 | 0 | CG03 | CG02 | CG01 | CG00 |
| W | 0 | 51h | 0 | 0 | CG15 | CG14 | CG13 | CG12 | CG11 | CG10 |
| W | 0 | 52h | 0 | 0 | CG25 | CG24 | CG23 | CG22 | CG21 | CG20 |
| W | 0 | 53h | 0 | 0 | CG35 | CG34 | CG33 | CG32 | CG31 | CG30 |
| W | 0 | 54h | 0 | 0 | CG45 | CG44 | CG43 | CG42 | CG41 | CG40 |
| W | 0 | 55h | 0 | 0 | CG55 | CG54 | CG53 | CG52 | CG51 | CG50 |
| W | 0 | 56h | CG67 | CG66 | CG65 | CG64 | CG63 | CG62 | CG61 | CG60 |

CG0[3:0] : Gamma adjustment register for the G output (V0)
CG1[5:0] : Gamma curve adjustment register for the G output (V5)
CG2[5:0] : Gamma curve adjustment register for the G output (V15)
CG3[5:0] : Gamma curve adjustment register for the G output (V31)
CG4[5:0] : Gamma curve adjustment register for the G output (V63)
CG5[5:0] : Gamma curve adjustment register for the G output (V127)
CG6[7:0] : Gamma adjustment register for the G output (V255)

6-20. Gamma adjustment for B-gray (R60h ~ R66h)

| R/W | | RS | | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|---|----|-----|------|------|------|------|------|------|------|------|
| W | 0 | | 60h | 0 | 0 | 0 | 0 | CB03 | CB02 | CB01 | CB00 |
| W | 0 | | 61h | 0 | 0 | CB15 | CB14 | CB13 | CB12 | CB11 | CB10 |
| W | 0 | | 62h | 0 | 0 | CB25 | CB24 | CB23 | CB22 | CB21 | CB20 |
| W | 0 | | 63h | 0 | 0 | CB35 | CB34 | CB33 | CB32 | CB31 | CB30 |
| W | 0 | | 64h | 0 | 0 | CB45 | CB44 | CB43 | CB42 | CB41 | CB40 |
| W | 0 | | 65h | 0 | 0 | CB55 | CB54 | CB53 | CB52 | CB51 | CB50 |
| W | 0 | | 66h | CB67 | CB66 | CB65 | CB64 | CB63 | CB62 | CB61 | CB60 |

CB0[3:0] : Gamma adjustment register for the B output (V0)
CB1[5:0] : Gamma curve adjustment register for the B output (V5)
CB2[5:0] : Gamma curve adjustment register for the B output (V15)
CB3[5:0] : Gamma curve adjustment register for the B output (V31)
CB4[5:0] : Gamma curve adjustment register for the B output (V63)
CB5[5:0] : Gamma curve adjustment register for the B output (V127)
CB6[7:0] : Gamma adjustment register for the B output (V255)

6-21. EEPROM Control (R07h / R70h ~ R82h)

| R/W | RS | | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|-----|-----|----------|----------|----------|----------|----------|----------|----------|
| W | 0 | 07h | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 |
| W | 0 | 70h | 0 | EV255_C2 | EV255_C1 | EV255_C0 | 0 | EV127_C2 | EV127_C1 | EV127_C0 |
| W | 0 | 71h | 0 | 0 | 0 | 0 | EV127_R3 | EV127_R2 | EV127_R1 | EV127_R0 |
| W | 0 | 72h | 0 | 0 | 0 | 0 | EV127_G3 | EV127_G2 | EV127_G1 | EV127_G0 |
| W | 0 | 73h | 0 | 0 | 0 | 0 | EV127_B3 | EV127_B2 | EV127_B1 | EV127_B0 |
| W | 0 | 74h | 0 | 0 | 0 | EV255_R4 | EV255_R3 | EV255_R2 | EV255_R1 | EV255_R0 |
| W | 0 | 75h | 0 | 0 | 0 | EV255_G4 | EV255_G3 | EV255_G2 | EV127_G1 | EV127_G0 |
| W | 0 | 76h | 0 | 0 | 0 | EV255_B4 | EV255_B3 | EV255_B2 | EV127_B1 | EV127_B0 |

The TL2796 has 27-bits internal EEPROM for gray scale adjustment.

Note) The register number R77h~R82h is reserved for internal voltage and oscillator clock adjustment.

EC[7:0] : EEPROM access enable. This instruction must set the "AAh" value for EEPROM Erase/Write/Read.

EV255_C2-0/EV127_C2-0 : Internal EEPROM control for V255/V127 gray scale level adjustment.

| EV127_C[2:0] EV255_C[2:0] | | | Operation |
|------------------------------|---|---|--|
| 0 | 0 | 0 | EEPROM can't access(but EV255_R/G/B, EV127_R/GB register value is valid) |
| 0 | 0 | 1 | Erase a data for V127 / V255 adjustment from EEPROM |
| 0 | 1 | 0 | Write to EEPROM for V127 / V255 adjustment. |
| 0 | 1 | 1 | Setting disable |
| 1 | 0 | 0 | Read from EEPROM for V127 / V255 adjustment. |
| 1 | 0 | 1 | Apply EEPROM data. (default) |
| 1 | 1 | 0 | Automatic Write/Read |
| 1 | 1 | 1 | Automatic Erase/Write/Read |

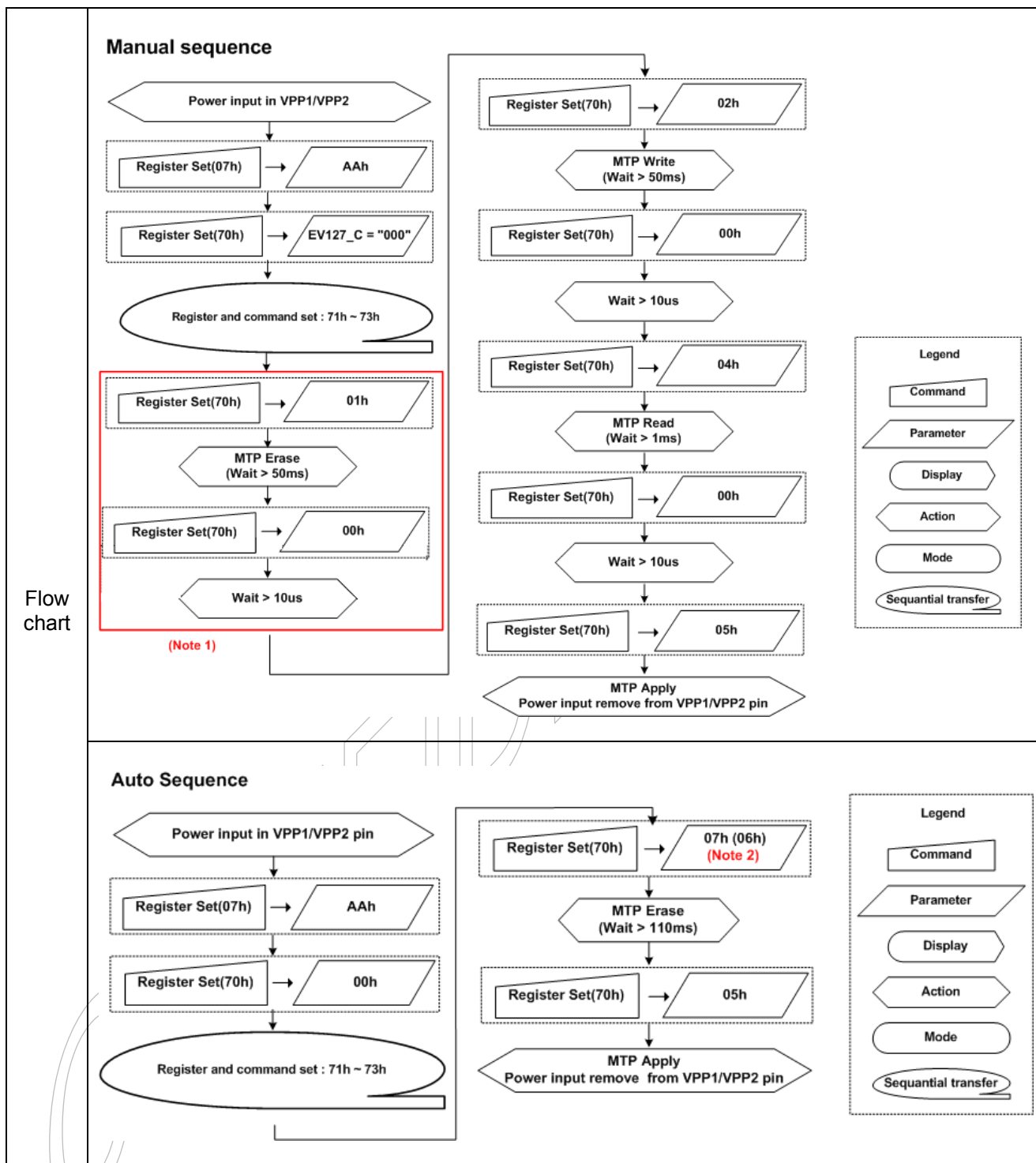
EV127_R3-0 / EV255_R4-0 : EEPROM writing value for adjustment the V127 / V255 level of R-gray scale.

EV127_G3-0 / EV255_G4-0 : EEPROM writing value for adjustment the V127 / V255 level of G-gray scale.

EV127_B3-0 / EV255_B4-0 : EEPROM writing value for adjustment the V127 / V255 level of B-gray scale.

| EV255[4:0] | | | | | Operation |
|------------|---|---|---|---|----------------------|
| 0 | 1 | 1 | 1 | 1 | + 15 |
| 0 | 1 | 1 | 1 | 0 | + 14 |
| 0 | 1 | 1 | 0 | 1 | + 13 |
| 0 | 1 | 1 | 0 | 0 | + 12 |
| : | : | : | : | : | : |
| 0 | 0 | 0 | 1 | 0 | + 2 |
| 0 | 0 | 0 | 0 | 1 | + 1 |
| 0 | 0 | 0 | 0 | 0 | + 0 (default) |
| 1 | 1 | 1 | 1 | 1 | - 1 |
| 1 | 1 | 1 | 1 | 0 | - 2 |
| 1 | 1 | 1 | 0 | 1 | - 3 |
| 1 | 1 | 1 | 0 | 0 | - 4 |
| : | : | : | : | : | : |
| 1 | 0 | 0 | 0 | 1 | - 15 |
| 1 | 0 | 0 | 0 | 0 | - 16 |

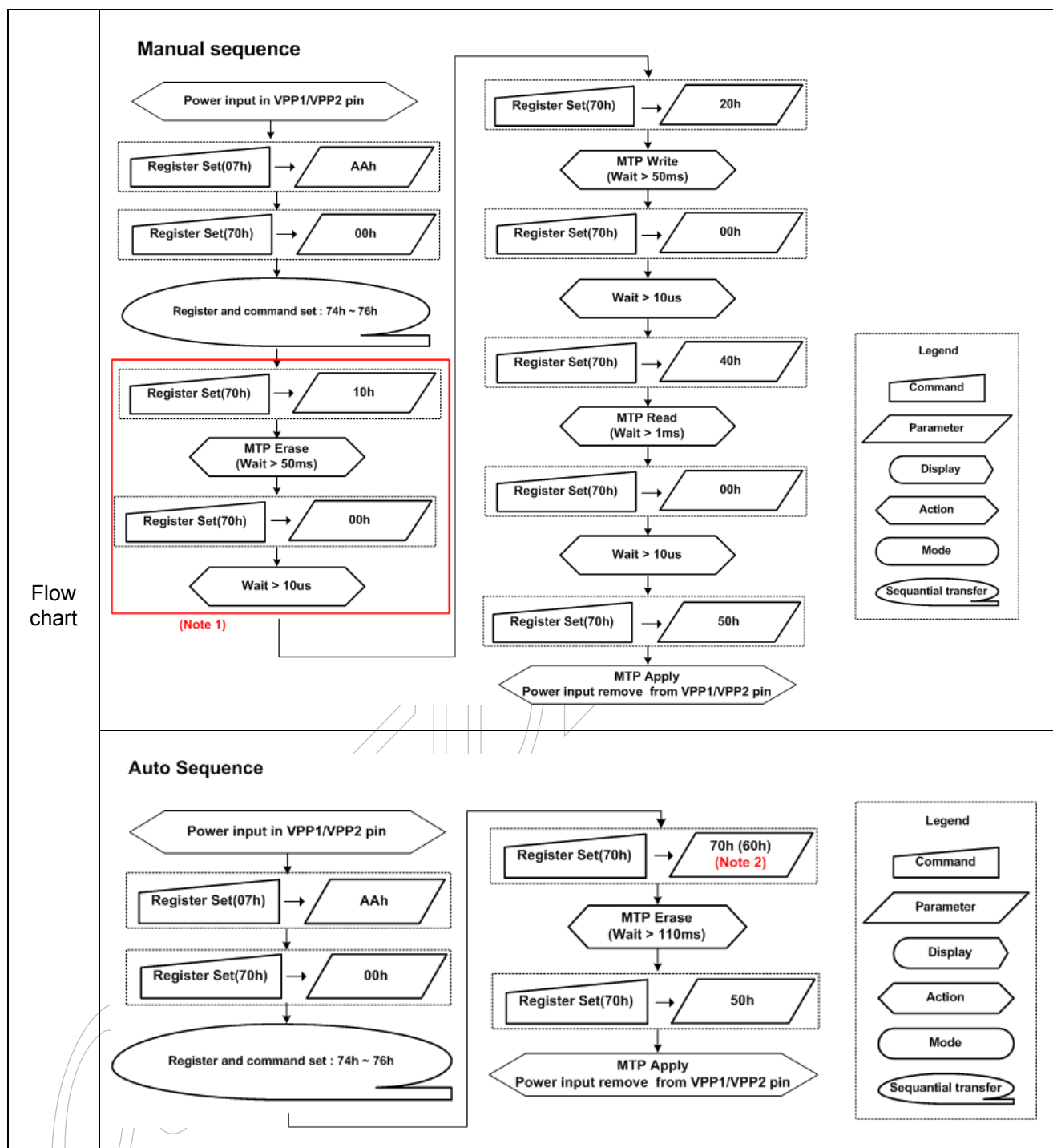
| EV127[3:0] | | | | Operation |
|------------|---|---|---|----------------------|
| 0 | 1 | 1 | 1 | + 7 |
| 0 | 1 | 1 | 0 | + 6 |
| 0 | 1 | 0 | 1 | + 5 |
| 0 | 1 | 0 | 0 | + 4 |
| 0 | 0 | 1 | 1 | + 3 |
| 0 | 0 | 1 | 0 | + 2 |
| 0 | 0 | 0 | 1 | + 1 |
| 0 | 0 | 0 | 0 | + 0 (default) |
| 1 | 1 | 1 | 1 | - 1 |
| 1 | 1 | 1 | 0 | - 2 |
| 1 | 1 | 0 | 1 | - 3 |
| 1 | 1 | 0 | 0 | - 4 |
| 1 | 0 | 1 | 1 | - 5 |
| 1 | 0 | 1 | 0 | - 6 |
| 1 | 0 | 0 | 1 | - 7 |
| 1 | 0 | 0 | 0 | - 8 |



Method for V127 gray scale level adjustment

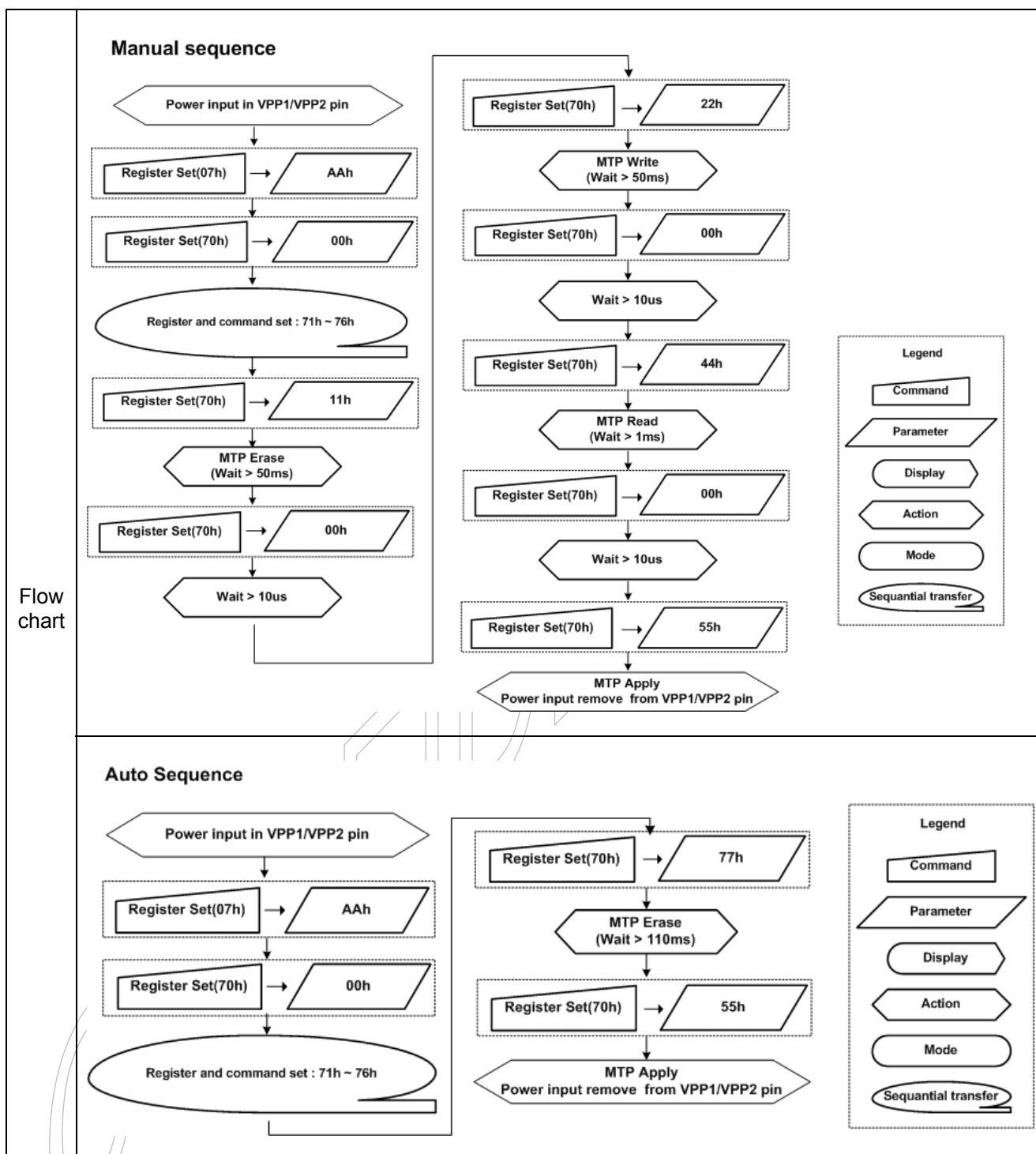
Note 1) If main program has been executed V255 voltage fitting before V127 voltage fitting, this process must not set.

Note 2) If main program has been executed V255 voltage fitting before V127 voltage fitting, this parameter must set "06"h



Note 1) If main program has been executed V127 voltage fitting before V255 voltage fitting, this process must not set.

Note 2) If main program has been executed V127 voltage fitting before V255 voltage fitting, this parameter must set "60"h



Method for V127/V255 gray scale level adjustment at one time

6-22. Instruction for PenTile Processing (RA0h ~ REFh)

PenTile Filters (PenTile 1, RA0h)

PARB : Determine if pattern adaptive filter is turned on to enhance the diagonal line and dot, which works only for red and blue sub-pixels.

| Bit | Bit Definition | Bit Value | Value Definition |
|------|--|-----------|------------------|
| PARB | This bit determines if pattern adaptive filter is enabled for red and blue sub-pixels. | 0 | OFF |
| | | 1 | ON, default |

MSRB : Determine if mixed saturated color adaptive filter is turned on to enhance the saturated color patterns, which is applied only to red and blue sub-pixels. If it is enabled, mixed saturated color pixels are compared against the pre-defined saturated color value in the mixed saturated threshold register, MSTH [15:0]. If it is disabled, the filter specified in SFRB [1:0] will be applied.

| Bit | Bit Definition | Bit Value | Value Definition |
|------|---|-----------|---|
| MSRB | This bit determines if mixed saturated color adaptive filter is applied to red and blue sub-pixels. | 0 | filter specified in SFRB [1:0]: DL, DS, D or B |
| | | 1 | DS filter for saturated color, and DL filter for non-saturated color, default |

SFRB [1:0] : Specify the fundamental filters for red and blue sub-pixels.

| Bit | Bit Definition | Bit Value | Value Definition |
|-----------|--|-----------|-------------------------------|
| SFRB[1:0] | These bits define the supported PenTile filters for red and blue sub-pixels. | 00 | DL sharpening filter, default |
| | | 01 | DS sharpening filter |
| | | 10 | D filter |
| | | 11 | B filter |

PTRB : Specify the pattern adaptive filter type for dot or diagonal patterns. For other patterns, the filter specified in SFRB [1:0] will be applied. It works only for red and blue sub-pixels.

| Bit | Bit Definition | Bit Value | Value Definition |
|------|---|-----------|---|
| PTRB | This bit defines the pattern adaptive filter type for dot and diagonal lines, which applied to red and blue sub-pixels. | 0 | D filter for dot, and B filter for diagonal line, default |
| | | 1 | B filter for dot and diagonal line |

MSG: Determine if mixed saturated color filter is turned on to enhance the saturated color patterns, which is applied only to green sub-pixels. This bit works exclusively with SFG bit. If it is enabled, mixed saturated colored pixels are compared against the value in the mixed saturated threshold register, MSTH [15:0].

| Bit | Bit Definition | Bit Value | Value Definition |
|-----|--|-----------|--|
| MSG | This bit determines if mixed saturated color adaptive filter is applied to green sub-pixels. | 0 | U filter |
| | | 1 | U filter for saturated color, and GL filter for non-saturated color, default |

SFG: Specify the fundamental filters for the green sub-pixel. This bit works exclusively with MSG bit and is superior to MSG bit.

| Bit | Bit Definition | Bit Value | Value Definition |
|-----|---|-----------|-------------------------------|
| SFG | This bit defines the supported PenTile sharpening filters for green sub-pixels. | 0 | U filter |
| | | 1 | GL sharpening filter, default |

PenTile Modes and Timing (PenTile 2, RA1h)

MD [1:0] : Specify the supported PenTile color mode as follows.

| Bit | Bit Definition | Bit Value | Value Definition |
|---------|---|-----------|----------------------------------|
| MD[1:0] | These bits define the supported PenTile color modes | 00 | PenTile full-color mode, default |
| | | 01 | PenTile 8-color mode |
| | | 10 | Reserved |
| | | 11 | Reserved |

SID [1:0]: It is assumed that the PenTile panel starts with R/G/B/G order and ends with B/G/R/G. The following table shows two possible directions. It is for SPR core processing.

| Bit | Bit Definition | Bit Value | Value Definition |
|----------|--|-----------|---|
| SID[1:0] | This bit indicates the shift direction of source & gate driver | 00 | Scanning upper left to lower right, default |
| | | 01 | Scanning upper right to lower left |
| | | 10 | Reserved |
| | | 11 | Reserved |

DT_ON: Determine if dithering function is on.

| Bit | Bit Definition | Bit Value | Value Definition |
|-------|--|-----------|--------------------------------|
| DT_ON | This bit determines if dithering function is on. | 0 | Dithering block is off |
| | | 1 | Dithering block is on, default |

DT_MD : Specify the type of dithering.

| Bit | Bit Definition | Bit Value | Value Definition |
|-------|--|-----------|-------------------------------------|
| DT_MD | This bit indicates the type of dithering function. | 0 | Spatial dithering only |
| | | 1 | Spatial-temporal dithering, default |

BYPS : Determine if all PenTile sub-system blocks are bypassed, which is for factory test-purpose only. If BYPS is set to "1", PID is recommended to be set to "0b00". It's because pre-rendered image starts with R/G/B/G order. For pre-rendered image, only red and green channels should be used and blue channel should be treated as dummy data.

| Bit | Bit Definition | Bit Value | Value Definition |
|------|--|-----------|------------------|
| BYPS | This bit determines if all PenTile sub-system blocks are bypassed. | 0 | Running. default |
| | | 1 | Bypassed |

MS Threshold Setting (PenTile 3, RA2h)

MSTH [7:0]: Specify the mixed saturation threshold in connection with MSRB and MSG bits in PenTile Filter register. If either MSRB or MSG bits is enabled, mixed saturated colored pixels are compared against this threshold value to determine if mixed saturated color adaptive filter is applied. The smaller number defines the more narrow saturated color range which starts from color value 255.

| Bit | Bit Definition | Bit Value | Value Definition |
|-----------|---|-----------|---|
| MSTH[7:0] | These bits define the mixed saturation threshold. | 0xXX | mixed saturation threshold value (default:0x0032) |

PA Threshold Setting (PenTile 4, RA3h)

PATH [3:0]: Specify the threshold value of pattern adaptive filter. The upper 4 bits of internal 11-bit data are used for this threshold. If PARB bit is enabled, pattern adaptive filter refers to this threshold value to compare with input red and blue pixel data.

Reducing this number, the pattern detective range reduces and it's getting more limited in terms of pattern recognition.

| Bit | Bit Definition | Bit Value | Value Definition |
|-----------|---|-----------|---|
| PATH[3:0] | These bits define the threshold value of pattern adaptive filter. | 0xX | threshold value of pattern adaptive filter (default:0x02) |

Gamma set (RA4h ~ REFh)

OR [7:0] : the initial offset value at Y coordinate of Red output gamma.

ΔYR_n [7:0] : $n=1\ldots32$, thirty-two sets of 8-bit DeltaY register are used to define delta value of each step at Y coordinate of Red output gamma table. Above 16-bit register includes two sets of 8-bit DeltaY register.

ΔXR_n [2:0] : $n=1\ldots32$, thirty-two sets of 3-bit DeltaX register are used to define delta value of each step (2, 4, 8, 16, 32, 64, 128 or 256) at X coordinate of Red output gamma table. Above 16-bit register includes four sets of 8-bit DeltaX register.

OG [7:0]: the initial offset value at Y coordinate of Green output gamma

ΔYG_n [7:0] : $n=1\ldots32$, thirty-two sets of 8-bit DeltaY register are used to define delta value of each step at Y coordinate of Green output gamma table. Above 16-bit register includes two sets of 8-bit DeltaY register.

ΔXG_n [2:0] : $n=1\ldots32$, thirty-two sets of 3-bit DeltaX register are used to define delta value of each step (2, 4, 8, 16, 32, 64, 128 or 256) at X coordinate of Green output gamma table. Above 16-bit register includes four sets of 8-bit DeltaX register.

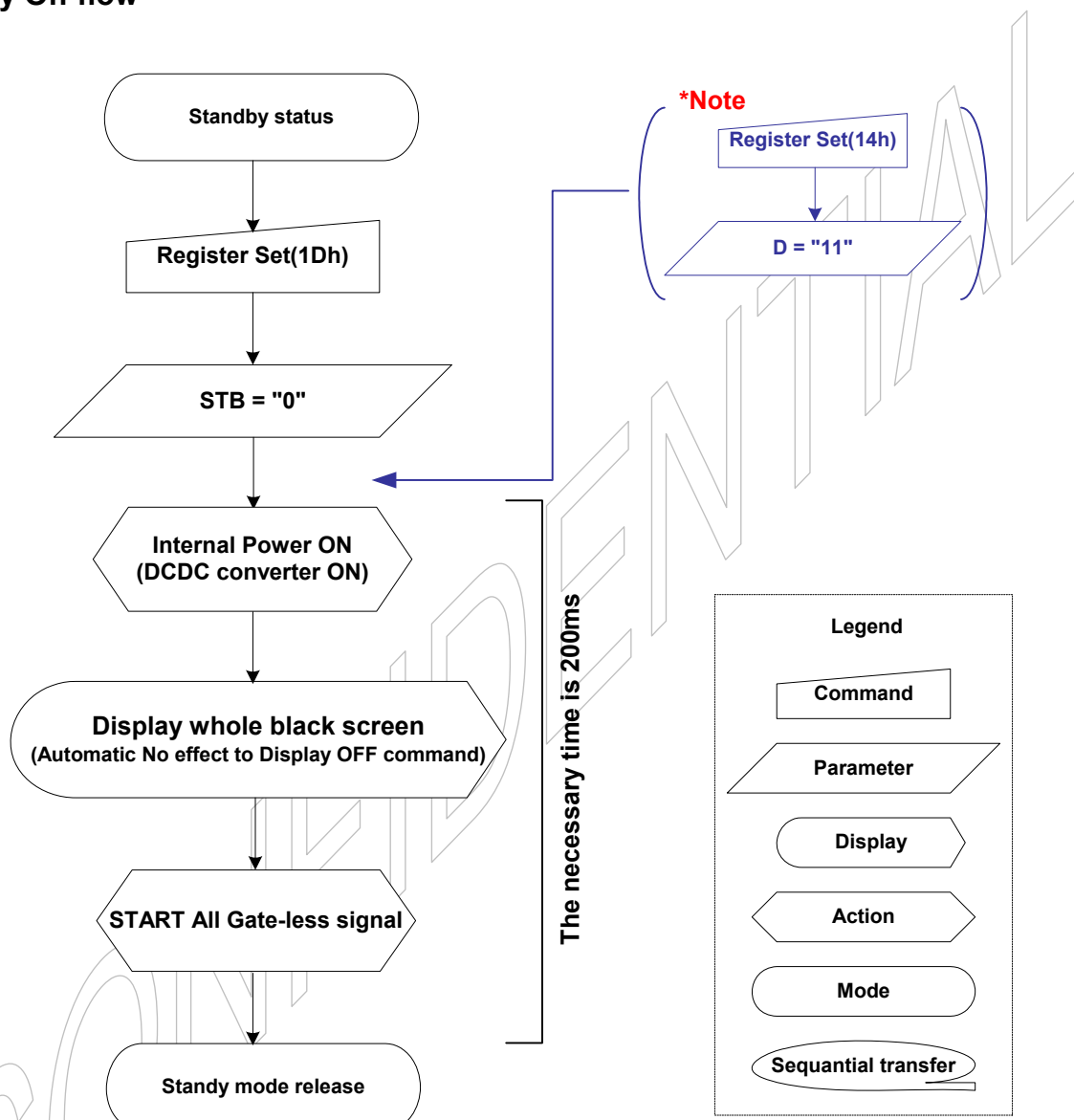
OB [7:0]: the initial offset value at Y coordinate of Blue output gamma.

ΔYB_n [7:0] : $n=1\ldots32$, thirty-two sets of 8-bit DeltaY register are used to define delta value of each step at Y coordinate of Blue output gamma table. Above 16-bit register includes two sets of 8-bit DeltaY register.

ΔXB_n [2:0] : $n=1\ldots32$, thirty-two sets of 3-bit DeltaX register are used to define delta value of each step (2, 4, 8, 16, 32, 64, 128 or 256) at X coordinate of Blue output gamma table. Above 16-bit register includes four sets of 8-bit DeltaX register.

7. INSTRUCTION SET UP FLOW

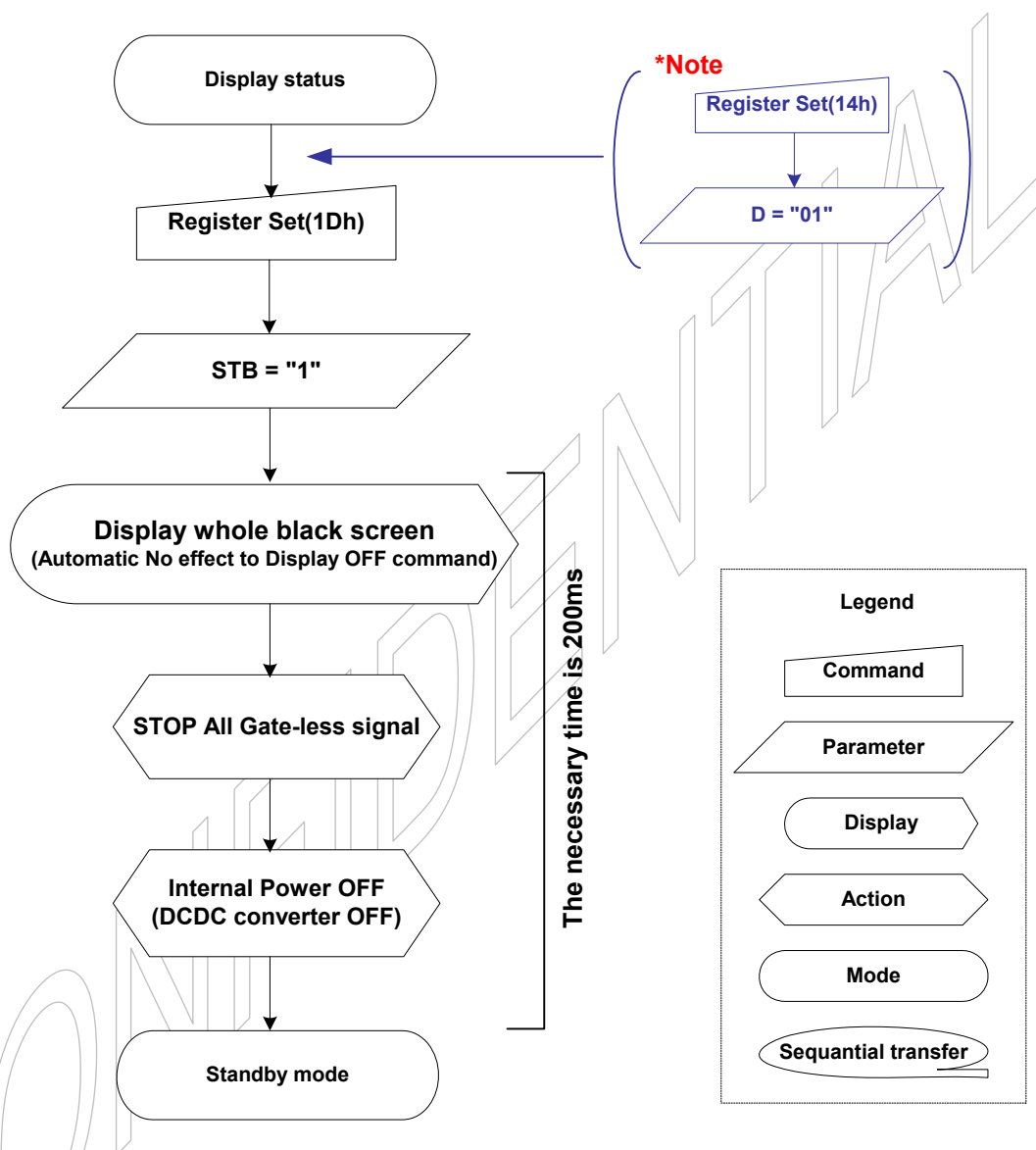
Standby Off flow



*Note) If D[1:0] don't changed at the "Standby On flow", the R14h register don't need to transmission at the "Standby Off flow". But, if D[1:0] set the "01" at the "Standby On flow", this register must be set.

Flow chart for Standby mode Release

Standby On flow



*Note) If R14h instruction don't transmission at this flow, source out internally operate like D[1:0] = "01" with STB ON(STB = 1) instruction for black display. But, internal register value about D[1:0] don't changed.

Flow chart for Standby mode Enter

Power Supply setting flow & Initial setting Flow

Power supplying should follow the sequence below. The settling time for oscillation circuit, step-up circuit, and operational amplifier depend on external resistor and capacitor.

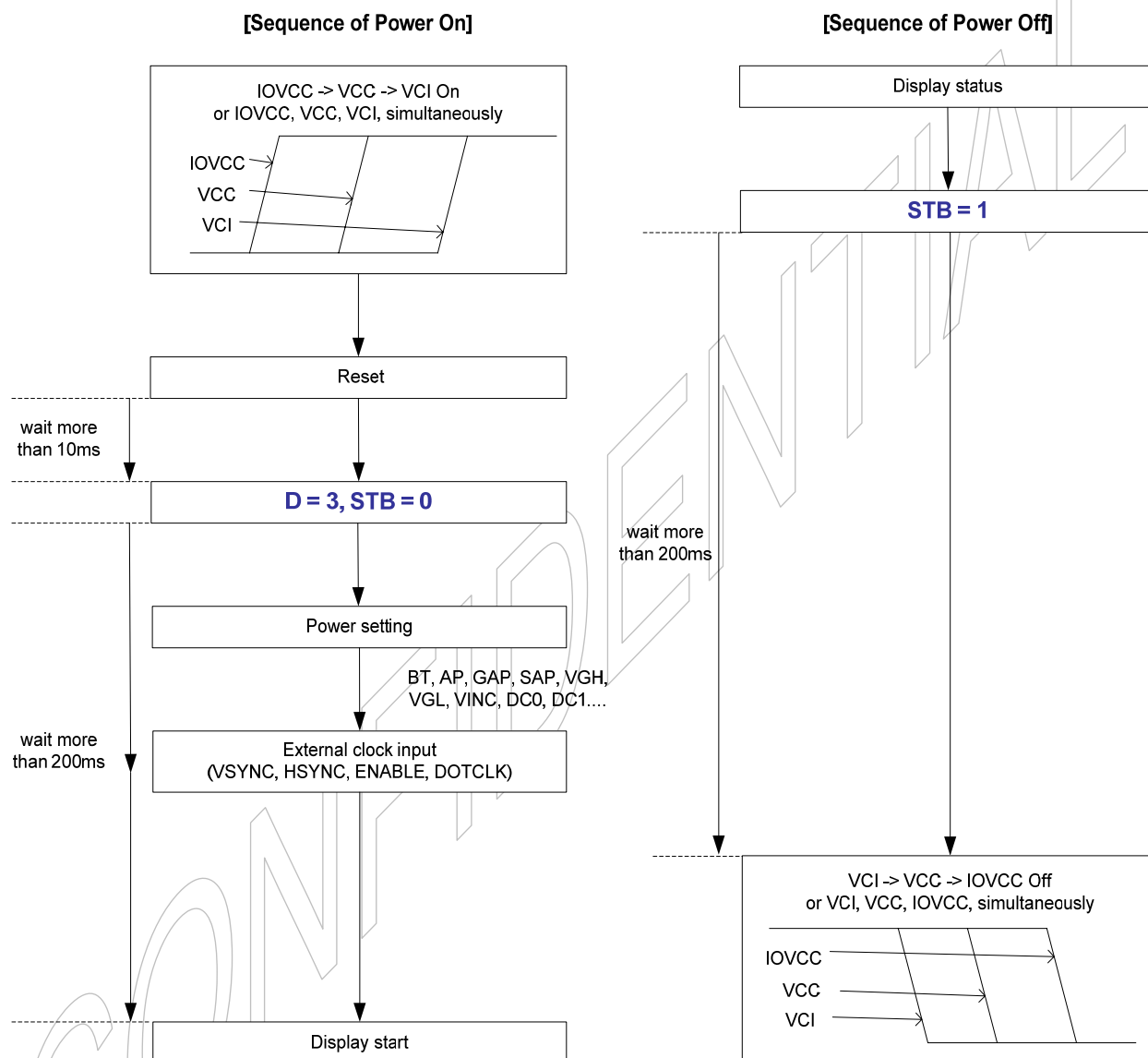


Figure Power Set Up Flow

8. SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Unit | Value | Note* |
|--|-----------------|------|------------------|-------|
| Power supply voltage (1) | VCC | V | -0.3 ~ +3.6 | 1,2 |
| Power supply voltage (2) | IOVCC | V | -0.3 ~ +3.6 | 1,2 |
| Power supply voltage for step-up circuit | VCI | V | -0.3 ~ +3.6 | 1,2 |
| AMOLED Power supply voltage range | VLOUT2 – VLOUT3 | V | 27 | 1,2 |
| Input voltage range | Vin | V | -0.5 ~ VCC + 0.5 | 1 |
| Operating temperature | Topr | °C | -40 ~ +85 | 1,3 |
| Storage temperature | Tstg | °C | -55 ~ +110 | 1 |

Note1) If the Driver is used above these absolute maximum ratings, it may become permanently damaged. Using the Driver within the following electrical characteristic limit is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the Driver will malfunction and cause poor reliability.

Note2) Indicate the voltage form VSS = 0V

Note3) DC characteristics and AC characteristics of shipping chips and shipping wafer are guaranteed at 85°C.

DC CHARACTERISTICS

DC Characteristics (VCC=2.4 to 3.3V, IOVCC=1.65 to 3.3V, Ta = +25°C)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Note |
|---|------|-----------------|---|-----------|------|-----------|------|------|
| Operating voltage | | IOVCC | - | 1.65 | - | 3.3 | V | *1 |
| | | VCC | - | 2.4 | - | 3.3 | | *1 |
| | | VCI | - | 2.5 | - | 3.3 | V | *1 |
| Logic input voltage | High | V _{IH} | - | 0.8xIOVCC | - | IOVCC | V | *2 |
| | Low | V _{IL} | - | -0.2 | - | 0.2xIOVCC | V | *2 |
| Logic output voltage | High | V _{OH} | IOH = -0.1mA | 0.8xIOVCC | - | IOVCC | V | *3 |
| | Low | V _{OL} | IOL = 0.1mA | -0.2 | - | 0.2xIOVCC | V | *3 |
| Input leakage current | | I _{IL} | Vin = VSS or IOVCC | -1.0 | - | 1.0 | uA | |
| Output leakage current | | I _{OL} | Vin = VSS or IOVCC | -3.0 | - | 3.0 | uA | |
| Operating frequency | | Fosc | Frame freq. = 60Hz Rf = 80KΩ, VCC=2.8V | 900 | 950 | 1000 | KHz | |
| 1 st step-up output efficiency | | VLOUT1 | ILOAD = 10mA | 85 | - | - | % | |
| 2 nd step-up output efficiency | | VLOUT2 | ILOAD = 1mA | 80 | - | - | % | |
| 3 rd step-up output efficiency | | VLOUT3 | ILOAD = 1mA | 80 | - | - | % | |

Note1) VSS = 0V

Note2) Applied pins : IM1-0, CSB, RS, SCL, DB23-0, SDI, ENABLE, VSYNC, HSYNC, ENABLE, DOTCLK, RESETB.

Note3) Applied pins : SDO, FSYNC

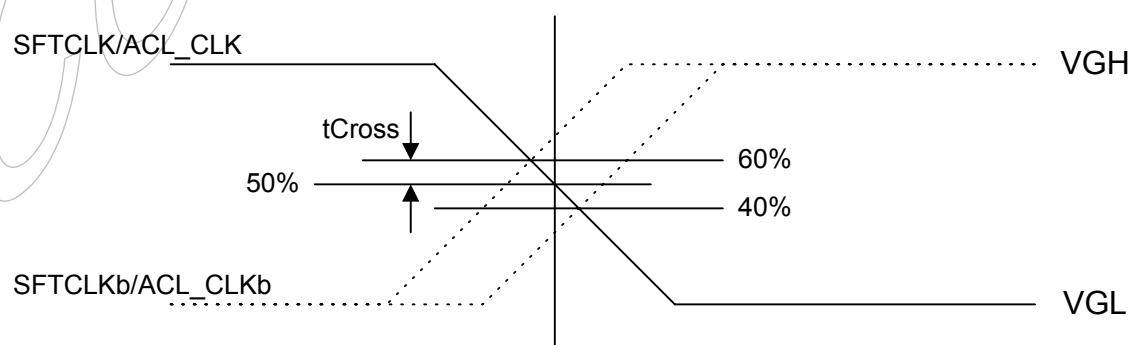
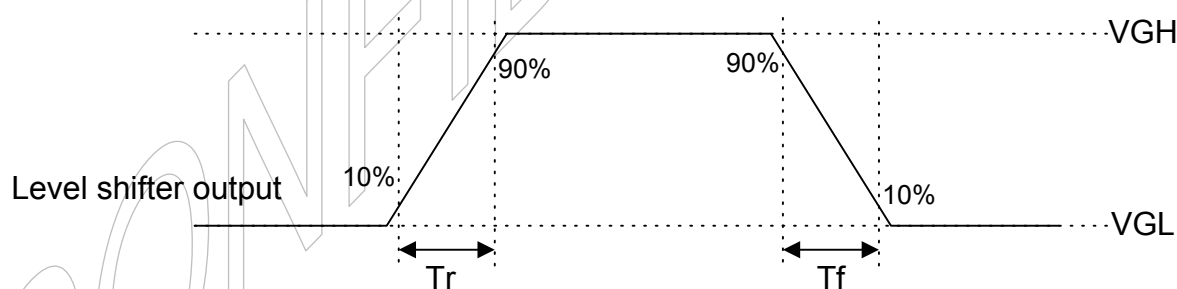
LOAD CONDITIONS

| Characteristic | Symbol | CONDITION | MIN | TYP | MAX | Unit | Note |
|--|--------|---|-------|-------|-------|------|------|
| VREG1OUT | | VCI = 2.5~3.3V Ta = +25°C | 4.185 | 4.200 | 4.215 | V | |
| Level shifter ON resistance | Ron | VGH = 6.0V VGL = -7.0V | 29 | - | 72 | kΩ | |
| Source driver high-level output current | IHOG | Vrx = 4.2V Vox = 3.5V | -180 | - | - | μA | |
| Source driver low-level output current | iLOG | Vrx = 1.0V Vox = 2.0V | - | - | 450 | μA | |
| Chip to chip source deviation | | When source output is 2V, mean value of total output | - | - | 15 | mV | |
| Output voltage deviation1 (pin to pin) | ΔVo1 | | - | - | 5 | mV | |
| Output voltage deviation2 (each gray) | ΔVo2 | | - | - | 5 | mV | |
| Source driver output voltage range | Vso | | 0.2 | - | 4.2 | V | |
| Source driver delay | tDD | | - | - | 5 | μs | |
| Current consumption during standby operation | Istb | Standby mode, VCC=VCI=IOVCC = 2.8V | - | 15 | 33 | μA | |
| Current consumption during normal operation | IVCC | VCC=IOVCC=VCI = 2.8V Ta = +25°C | - | - | 14 | mA | |
| | IVCI | Frame Frequency = 60Hz | - | - | 15 | mA | |

Driver load condition

- CMOS

| Signal | Load Condition | | Output Level | | Parameter | Symbol | Specification | | | Unit |
|-----------|----------------|-------|--------------|-----|----------------|--------|---------------|-----|------|------|
| | R(Ω) | C(pF) | High | Low | | | Min | Typ | Max | |
| ESR | 1420 | 65 | VGH | VGL | Rising/Falling | Tr/Tf | - | - | 2000 | ns |
| FLM | 1000 | 45 | VGH | VGL | Rising/Falling | Tr/Tf | - | - | 1000 | ns |
| SFTCLK/B | 1000 | 65 | VGH | VGL | Rising/Falling | Tr/Tf | - | - | 300 | ns |
| | | | | | Cross point | tCross | 40 | 50 | 60 | % |
| SCLK1/2 | 1000 | 65 | VGH | VGL | Rising/Falling | Tr/Tf | - | - | 300 | ns |
| ACL_FLM | 1000 | 45 | VGH | VGL | Rising/Falling | Tr/Tf | - | - | 1000 | ns |
| ACL_CLK/B | 1000 | 75 | VGH | VGL | Rising/Falling | Tr/Tf | - | - | 350 | ns |
| | | | | | Cross point | tCross | 40 | 50 | 60 | % |



- Latch

| Signal | Load Condition | | Output Level | | Parameter | Symbol | Specification | | | Unit |
|------------|----------------|-------|--------------|-----|----------------|--------|---------------|-----|------|------|
| | R(Ω) | C(pF) | High | Low | | | Min | Typ | Max | |
| ESR | 1420 | 65 | VGH | VGL | Rising/Falling | Tr/Tf | - | - | 2000 | ns |
| FLM | 1000 | 45 | VGH | VGL | Rising/Falling | Tr/Tf | - | - | 1000 | ns |
| CL 1/2/3/4 | 1000 | 50 | VGH | VGL | Rising/Falling | Tr/Tf | - | - | 1000 | ns |
| ACL_FLM | 1000 | 45 | VGH | VGL | Rising/Falling | Tr/Tf | - | - | 1000 | ns |
| ACL_CLK/B | 1000 | 75 | VGH | VGL | Rising/Falling | Tr/Tf | - | - | 350 | ns |
| | | | | | Cross point | tCross | 40 | 50 | 60 | % |

- PMOS1/2

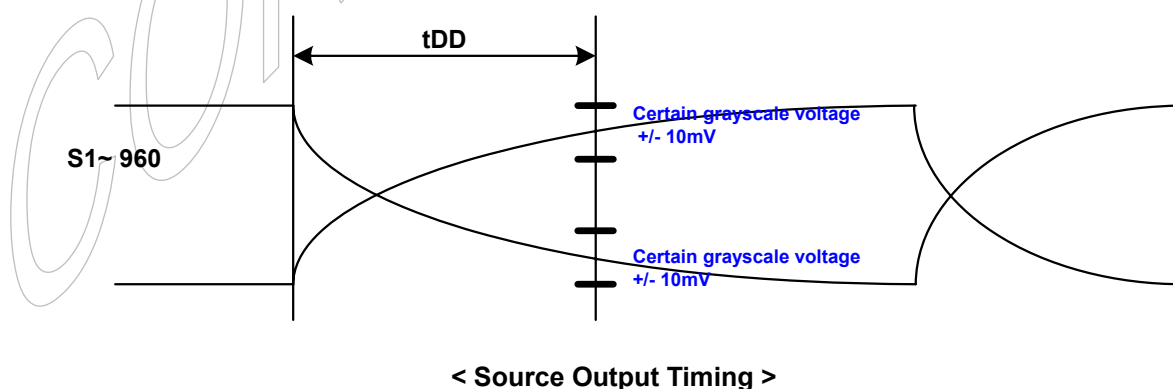
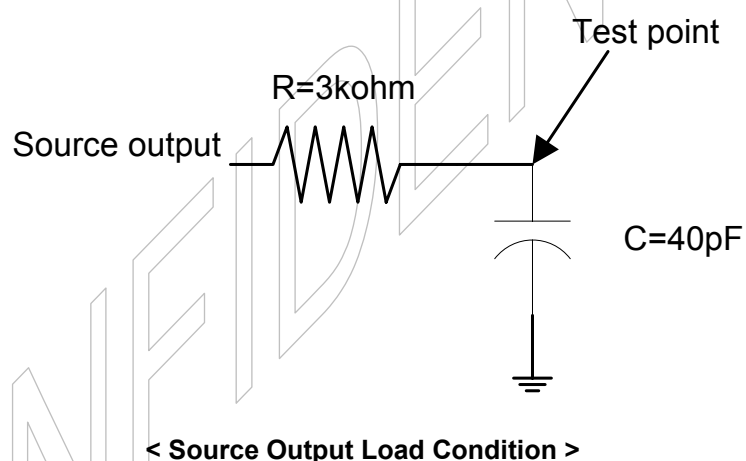
| Signal | Load Condition | | Output Level | | Parameter | Symbol | Specification | | | Unit |
|------------------------|----------------|-------|--------------|-----|----------------|--------|---------------|-----|------|------|
| | R(Ω) | C(pF) | High | Low | | | Min | Typ | Max | |
| FLM | 1000 | 45 | VGH | VGL | Rising/Falling | Tr/Tf | - | - | 1000 | ns |
| CLK1/2/3 | 1000 | 50 | VGH | VGL | Rising/Falling | Tr/Tf | - | - | 1000 | ns |
| EM_FLM | 1000 | 45 | VGH | VGL | Rising/Falling | Tr/Tf | - | - | 1000 | ns |
| EM_CLK1/B EM_CLK2/B | 1000 | 100 | VGH | VGL | Rising/Falling | Tr/Tf | - | - | 300 | ns |
| ESR | 1413 | 65 | VGH | VGL | Rising/Falling | Tr/Tf | - | - | 2000 | ns |

VGH/VGL/VINT Load condition

| Name | Range | Deviation | Interval | Current [max] |
|------|---------------|------------------------|----------|-------------------|
| VGH | 4.6V ~ 6.0V | Max $\pm 100\text{mV}$ | | 500 μA |
| VGL | -7.8V ~ -6.4V | Max $\pm 100\text{mV}$ | | 500 μA |
| VINT | -1.0V ~ -3.0V | Max $\pm 100\text{mV}$ | | Peak 3mA |

SOURCE OUTPUT

| Item | Symbol | Test Condition | Max |
|-----------------------------|--------|---|--------------|
| Driver output Delay time | tDD | - Grayscale of time to be reached by output level : $\pm 10\text{mV}$ - Load resistance R : min=1kohm max=3kohm - Load resistance C : min=30pF max=40pF | 5.0us / 4.0V |



VINT Source

Functions and conditions of VINT Output

- During 1H (=20 μ s, 1 horizontal line) time
- Peak current = 3mA
- VINT ripple(at saturation position) < 100mV
- VINT Saturation time < 7 μ s

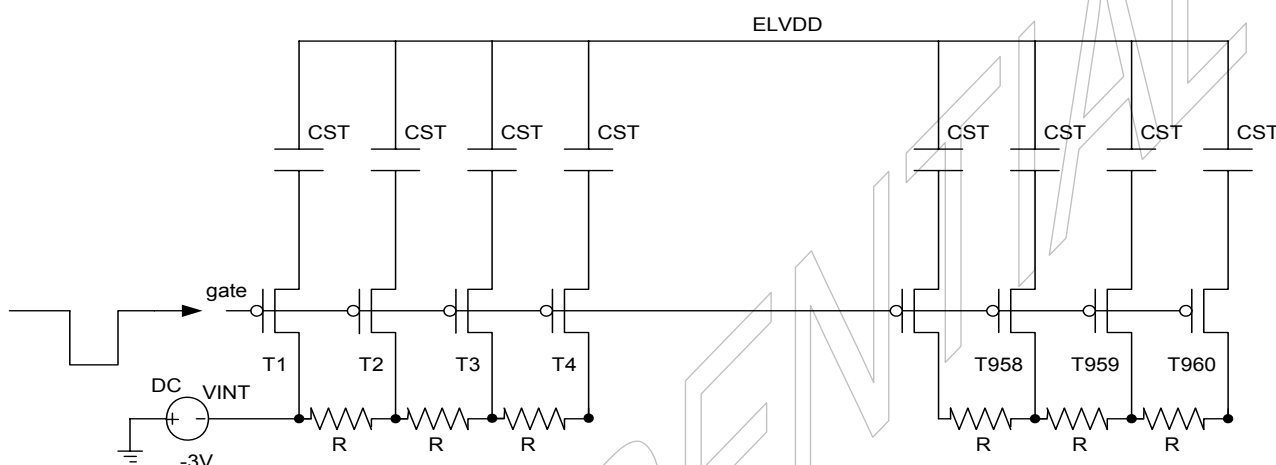


Figure VINT Source Load

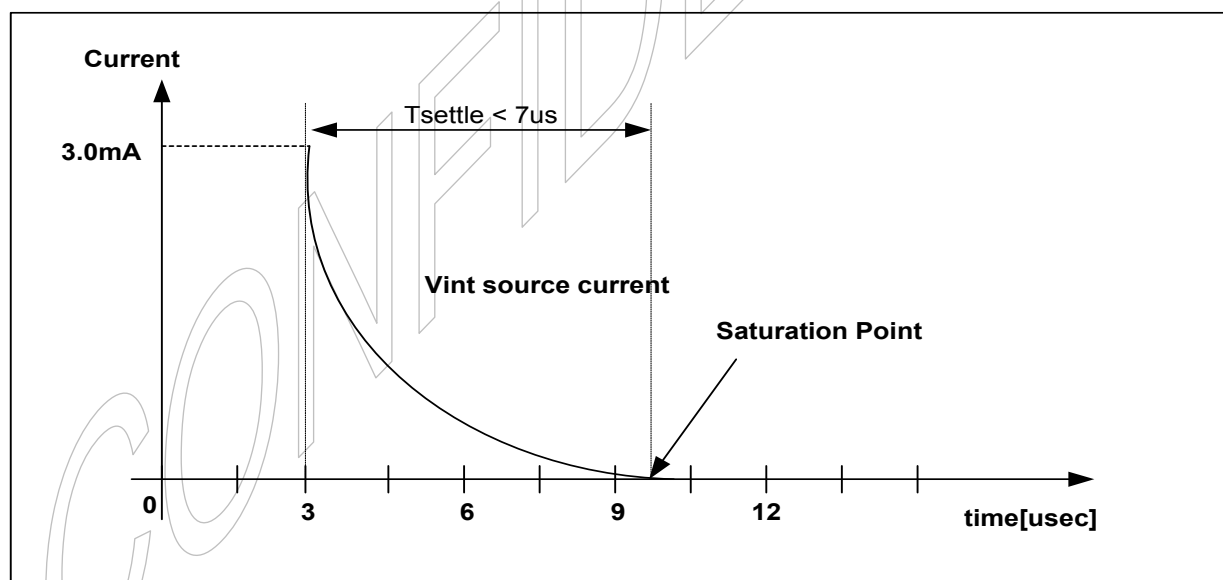
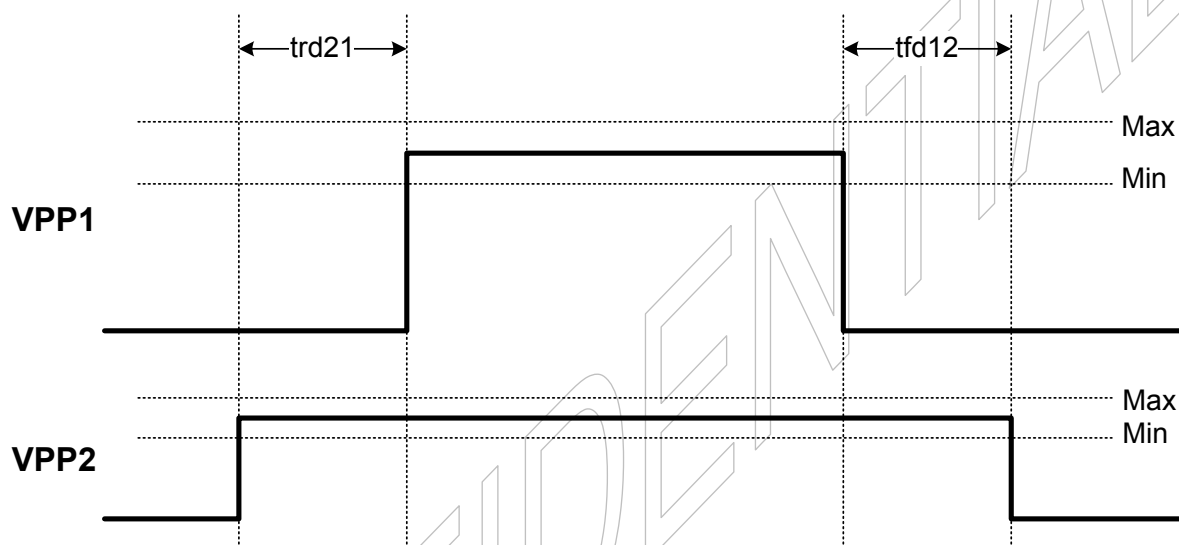


Figure Current Wave of VINT

MTP operation condition

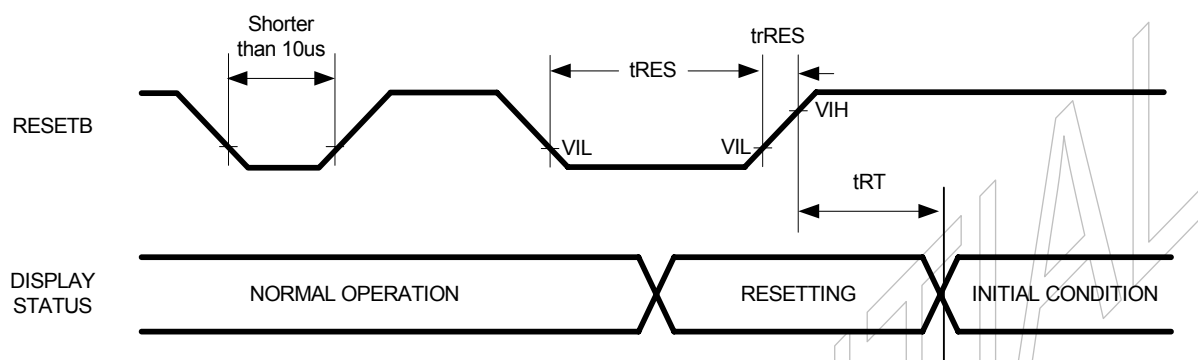
| Item | Symbol | Min. | Typ. | Max. | Unit |
|--------------------------|--------|------|-----------|------|------|
| VPP2 to VPP1 delay time | Trd21 | 1 | - | - | ms |
| VPP1 to VPP2 delay time | Tfd12 | 1 | - | - | ms |
| VPP1 input voltage range | - | 20 | 21 | 22 | V |
| VPP2 input voltage range | - | 4 | 5 | 6 | V |



-
- The diagram illustrates the timing relationships for the 24C02 I2C EEPROM. The signals shown are CSB (Chip Select), SCL (Serial Clock), SDI (Serial Data Input), and SDO (Serial Data Output). The diagram is divided into two sections: 'Start : S' and 'End : P'.
- Timing Parameters:**
- tCSU:** CSB setup time before SCL sampling.
 - tscr:** SCL setup time before data sampling.
 - tSCH:** SCL hold time after data sampling.
 - tSCYC:** SCL cycle time.
 - tscf:** SCL setup time before CSB sampling.
 - tSCL:** SCL hold time after CSB sampling.
 - tCH:** CSB hold time after SCL sampling.
 - tSISU:** SDI setup time before SCL sampling.
 - tSIH:** SDI hold time after SCL sampling.
 - tSOD:** SDO output delay time.
 - tSOH:** SDO output hold time.
- Signal Levels:**
- CSB:** VIH (High), VIL (Low).
 - SCL:** VIH (High), VIL (Low).
 - SDI:** VIH (High), VIL (Low).
 - SDO:** VOH (High), VOL (Low).

| Item | | Symbol | Min. | Typ. | Max. | Unit |
|-------------------------------------|--------------------|------------|------|------|------|------|
| Serial clock cycle time | Write (received) | tSCYC | 100 | - | - | ns |
| | Read (transmitted) | tSCYC | 350 | - | - | ns |
| Serial clock high-level pulse width | Write (received) | tSCH | 40 | - | - | ns |
| | Read (transmitted) | tSCH | 150 | - | - | ns |
| Serial clock low-level pulse width | Write (received) | tSCL | 40 | - | - | ns |
| | Read (transmitted) | tSCL | 150 | - | - | ns |
| Serial clock rise/fall time | | tSCr, tSCf | - | - | 20 | ns |
| Chip select set up time | | tCSU | 20 | - | - | ns |
| Chip select hold time | | tCH | 60 | - | - | ns |
| Serial input data set up time | | tSISU | 30 | - | - | ns |
| Serial input data hold time | | tSIH | 30 | - | - | ns |
| Serial output data delay time | | tSOD | - | - | 130 | ns |
| Serial output data hold time | | tSOH | 5 | - | - | ns |

• Reset Timing Characteristics



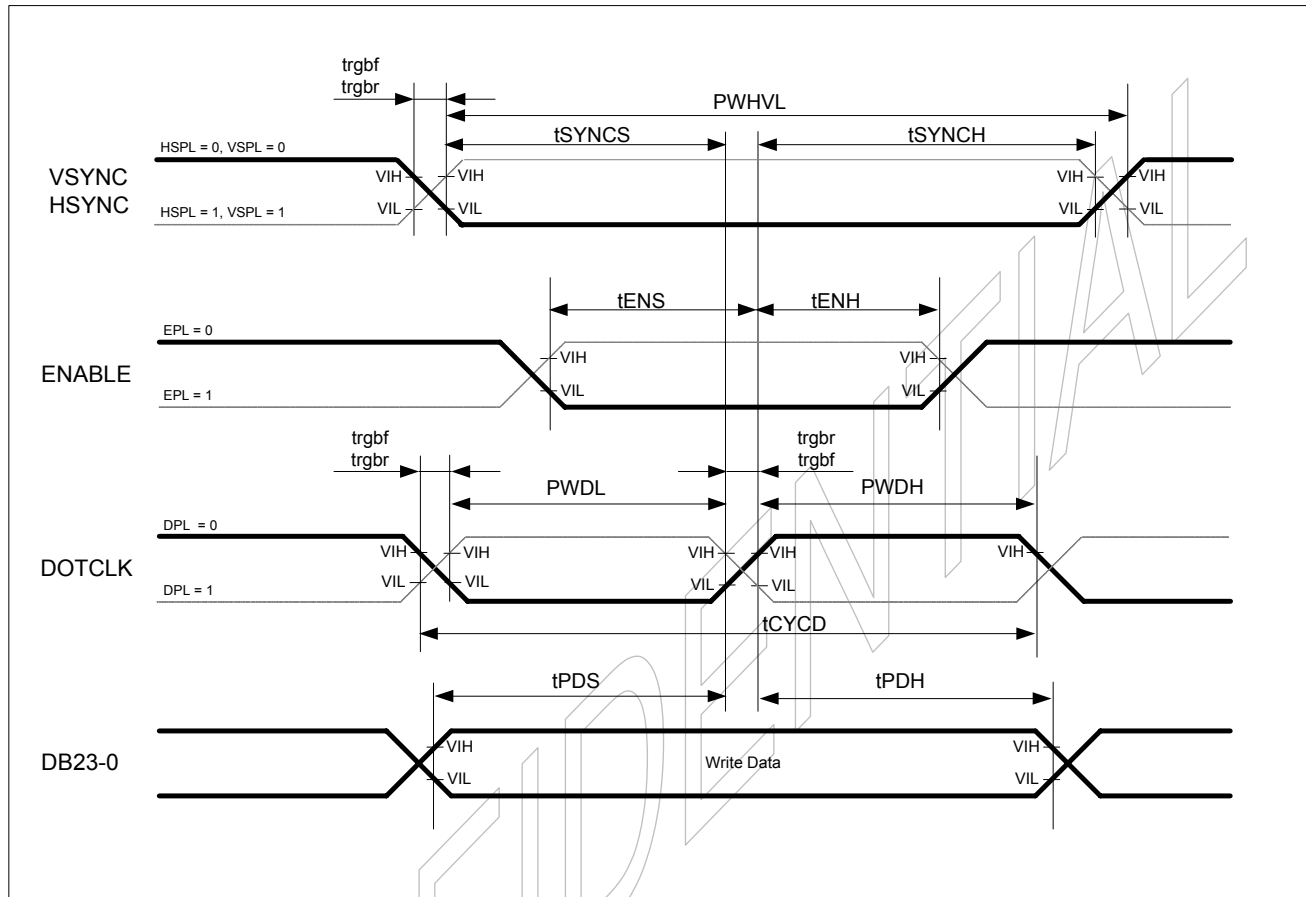
IOVCC=1.65 to 3.3V, VCC= 2.4 to 3.3V operation

| Item | Symbol | Unit | Min. | Typ. | Max. |
|-----------------------|------------|------|------|------|------|
| Reset low-level width | t_{RES} | us | 10 | - | - |
| Reset rise time | t_{rRES} | us | - | - | 2 |
| Reset cancel | t_{RT} | ms | | | 1 |

Reset description

| RESETB Pulse | Action |
|-------------------|----------------|
| Shorter than 10us | Reset rejected |
| Longer than 10us | Reset |

• RGB interface timing characteristics



RGB interface(16/18/24-bit), IOVCC=1.65 to 3.3V, VCC= 2.4 to 3.3V operation

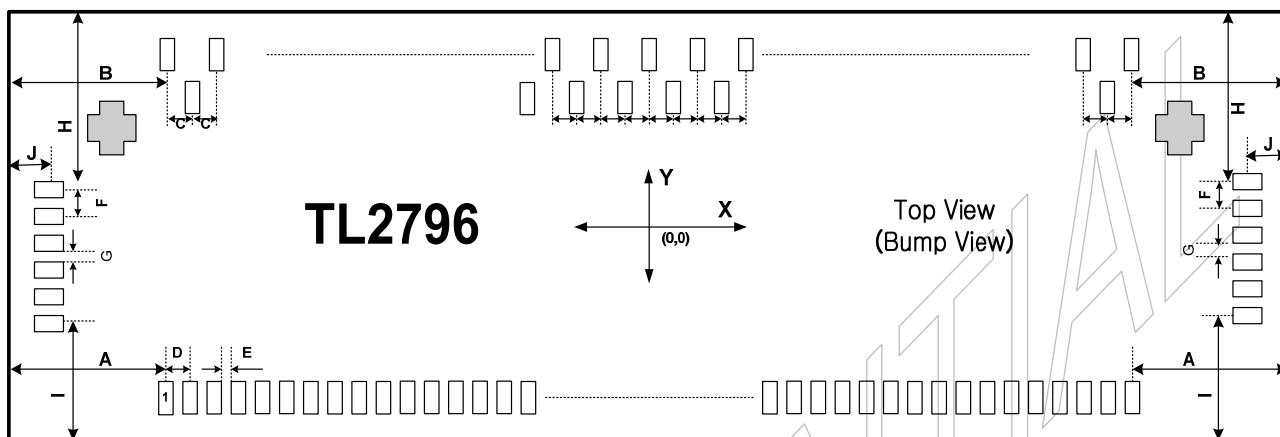
| Item | Symbol | Min. | Typ. | Max. | Unit |
|--|--------------|------|------|------|--------|
| VSYNC / HSYNC "Low" level pulse width | PWHVL | 1 | - | - | DOTCLK |
| VSYNC / HSYNC set up time | tSYNCS | 10 | - | - | ns |
| VSYNC / HSYNC hold time | tSYNCH | 10 | - | - | ns |
| ENABLE set up time | tENS | 10 | - | - | ns |
| ENABLE hold time | tENH | 10 | - | - | ns |
| DOTCLK "Low" level pulse width | PWDL | 10 | - | - | ns |
| DOTCLK "High" level pulse width | PWDH | 10 | - | - | ns |
| DOTCLK cycle time | tCYCD | 30 | - | - | ns |
| Data set up time | tPDS | 7 | - | - | ns |
| Data hold time | tPDH | 7 | - | - | ns |
| DOTCLK, VSYNC, HSYNC rising, falling time | trgbr, trgbf | - | - | 15 | ns |

Note 1) Above AC characteristics condition is in case of VCCL >= 1.8V irrespective of VCC.

TL2796

960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout

9. PAD CENTER COORDINATES



Pad Dimensions <Basis of Bump Pad>

[unit : um]

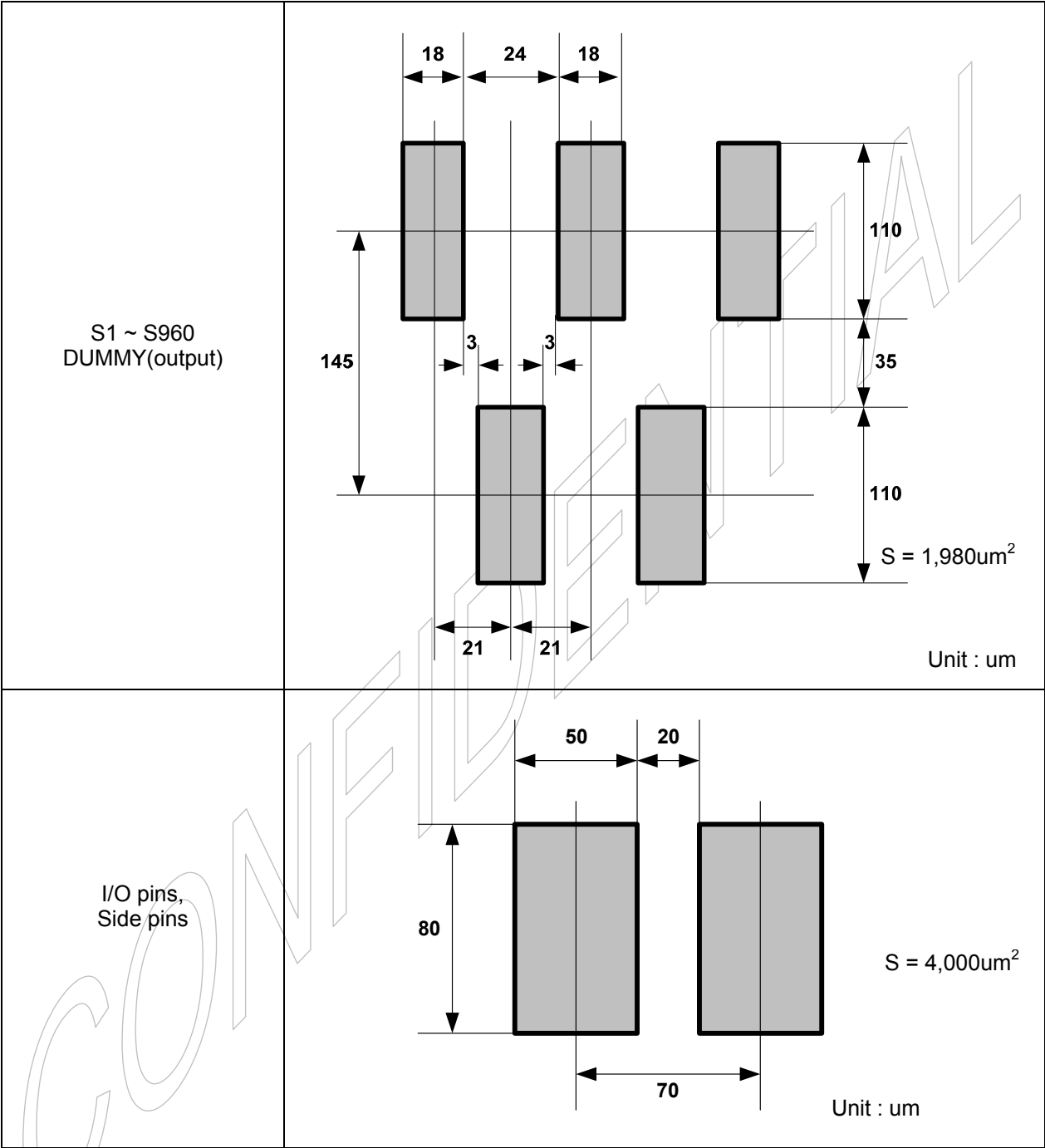
| Pad name | Pad number | X | Y |
|-------------------------|------------------------|----------|------|
| Chip Size (without S/L) | - | 21100 | 1000 |
| Chip Size (with S/L) | - | 21200 | 1100 |
| Input Pad | 1 ~ 294 | 50 | 80 |
| Side Pad | 295 ~ 300, 1280 ~ 1285 | 80 | 50 |
| Output Pad | 301 ~ 1279 | 18 | 110 |
| Bumped Pad Height | 1 ~ 1285 | 15 ± 3 | |
| Chip Thickness | - | 300 ± 20 | |

Chip Outline Dimensions <Basis of Bump Pad>

[unit : um]

| Symbol | Dimension | Symbol | Dimension |
|--------|-----------|--------|-----------|
| A | 295 | B | 281 |
| C | 21 | D | 70 |
| E | 20 | F | 70 |
| G | 20 | H | 370 |
| I | 280 | J | 55 |

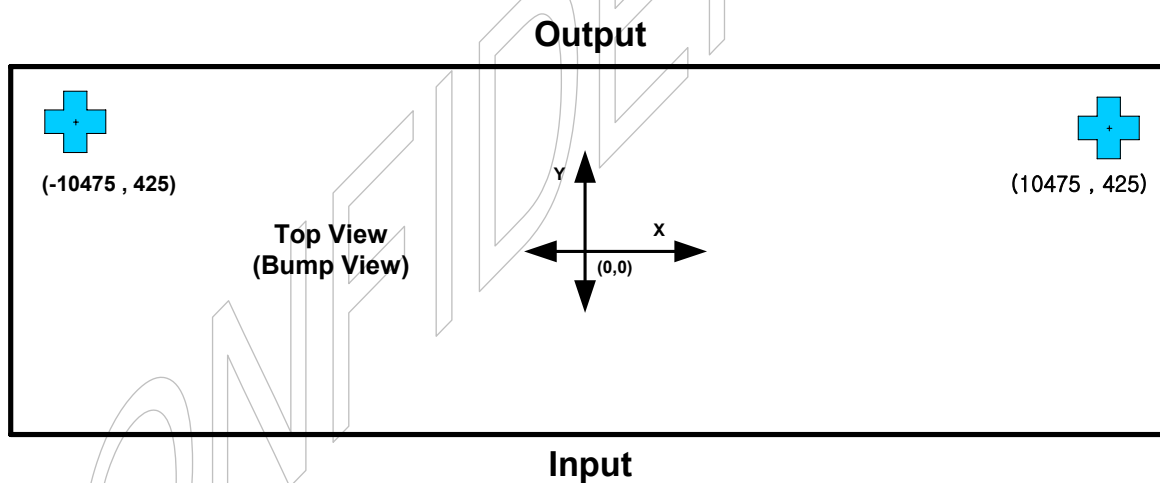
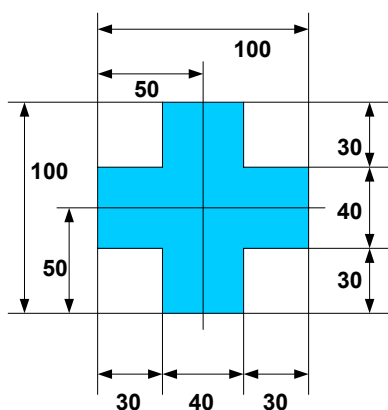
BUMP



TL2796

960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout

ALIGN KEY



 TL2796

**960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout**
PAD LOCATION

| Pin No | X | Y | Pad Name |
|--------|--------|------|-------------|
| 1 | -10255 | -445 | DUMMYR1 |
| 2 | -10185 | -445 | DUMMYR2 |
| 3 | -10115 | -445 | DUMMYR3 |
| 4 | -10045 | -445 | DUMMYS960 |
| 5 | -9975 | -445 | VINT |
| 6 | -9905 | -445 | VINT |
| 7 | -9835 | -445 | VINT |
| 8 | -9765 | -445 | VINT |
| 9 | -9695 | -445 | DUMMY |
| 10 | -9625 | -445 | VGL |
| 11 | -9555 | -445 | VGL |
| 12 | -9485 | -445 | VGL |
| 13 | -9415 | -445 | VGL |
| 14 | -9345 | -445 | DUMMY |
| 15 | -9275 | -445 | VGH |
| 16 | -9205 | -445 | VGH |
| 17 | -9135 | -445 | VGH |
| 18 | -9065 | -445 | VGH |
| 19 | -8995 | -445 | DUMMY |
| 20 | -8925 | -445 | VCI(ANALOG) |
| 21 | -8855 | -445 | VCI(ANALOG) |
| 22 | -8785 | -445 | VCI(ANALOG) |
| 23 | -8715 | -445 | VCI(ANALOG) |
| 24 | -8645 | -445 | VCI(ANALOG) |
| 25 | -8575 | -445 | VCI(ANALOG) |
| 26 | -8505 | -445 | VCI(ANALOG) |
| 27 | -8435 | -445 | VCI(ANALOG) |
| 28 | -8365 | -445 | VCI(ANALOG) |
| 29 | -8295 | -445 | VCI(HV) |
| 30 | -8225 | -445 | VCI(HV) |
| 31 | -8155 | -445 | VCI(HV) |
| 32 | -8085 | -445 | VCI(HV) |
| 33 | -8015 | -445 | VCI(HV) |
| 34 | -7945 | -445 | VCI(HV) |
| 35 | -7875 | -445 | DUMMY |
| 36 | -7805 | -445 | VSS(SDRV) |
| 37 | -7735 | -445 | VSS(SDRV) |
| 38 | -7665 | -445 | VSS(SDRV) |
| 39 | -7595 | -445 | VSS(SDRV) |
| 40 | -7525 | -445 | VSS(SDRV) |
| 41 | -7455 | -445 | VSS(SDRV) |
| 42 | -7385 | -445 | VSS(HV) |
| 43 | -7315 | -445 | VSS(HV) |
| 44 | -7245 | -445 | VSS(HV) |
| 45 | -7175 | -445 | VSS(HV) |
| 46 | -7105 | -445 | VSS(HV) |
| 47 | -7035 | -445 | VSS(HV) |
| 48 | -6965 | -445 | DUMMY |
| 49 | -6895 | -445 | C22M |
| 50 | -6825 | -445 | C22M |

| Pin No | X | Y | Pad Name |
|--------|-------|------|----------|
| 51 | -6755 | -445 | C22M |
| 52 | -6685 | -445 | C22M |
| 53 | -6615 | -445 | C22M |
| 54 | -6545 | -445 | C22M |
| 55 | -6475 | -445 | DUMMY |
| 56 | -6405 | -445 | C22P |
| 57 | -6335 | -445 | C22P |
| 58 | -6265 | -445 | C22P |
| 59 | -6195 | -445 | C22P |
| 60 | -6125 | -445 | C22P |
| 61 | -6055 | -445 | C22P |
| 62 | -5985 | -445 | DUMMY |
| 63 | -5915 | -445 | VLOUT3 |
| 64 | -5845 | -445 | VLOUT3 |
| 65 | -5775 | -445 | VLOUT3 |
| 66 | -5705 | -445 | VLOUT3 |
| 67 | -5635 | -445 | DUMMY |
| 68 | -5565 | -445 | C21M |
| 69 | -5495 | -445 | C21M |
| 70 | -5425 | -445 | C21M |
| 71 | -5355 | -445 | C21M |
| 72 | -5285 | -445 | C21M |
| 73 | -5215 | -445 | C21M |
| 74 | -5145 | -445 | DUMMY |
| 75 | -5075 | -445 | C21P |
| 76 | -5005 | -445 | C21P |
| 77 | -4935 | -445 | C21P |
| 78 | -4865 | -445 | C21P |
| 79 | -4795 | -445 | C21P |
| 80 | -4725 | -445 | C21P |
| 81 | -4655 | -445 | DUMMY |
| 82 | -4585 | -445 | VLOUT2 |
| 83 | -4515 | -445 | VLOUT2 |
| 84 | -4445 | -445 | VLOUT2 |
| 85 | -4375 | -445 | VLOUT2 |
| 86 | -4305 | -445 | DUMMY |
| 87 | -4235 | -445 | VREG1OUT |
| 88 | -4165 | -445 | VREG1OUT |
| 89 | -4095 | -445 | VREG1OUT |
| 90 | -4025 | -445 | VREG1OUT |
| 91 | -3955 | -445 | VREG1OUT |
| 92 | -3885 | -445 | VREG1OUT |
| 93 | -3815 | -445 | DUMMY |
| 94 | -3745 | -445 | VREG2OUT |
| 95 | -3675 | -445 | VREG2OUT |
| 96 | -3605 | -445 | VREG2OUT |
| 97 | -3535 | -445 | VREG2OUT |
| 98 | -3465 | -445 | VREG2OUT |
| 99 | -3395 | -445 | VREG2OUT |
| 100 | -3325 | -445 | DUMMY |

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**960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout**

| Pin No | X | Y | Pad Name |
|--------|-------|------|-------------|
| 101 | -3255 | -445 | EXT_MV(REF) |
| 102 | -3185 | -445 | EXT_MV(REF) |
| 103 | -3115 | -445 | DUMMY |
| 104 | -3045 | -445 | EXT_MV |
| 105 | -2975 | -445 | EXT_MV |
| 106 | -2905 | -445 | EXT_MV |
| 107 | -2835 | -445 | EXT_MV |
| 108 | -2765 | -445 | EXT_MV |
| 109 | -2695 | -445 | EXT_MV |
| 110 | -2625 | -445 | DUMMY |
| 111 | -2555 | -445 | VLOUT1 |
| 112 | -2485 | -445 | VLOUT1 |
| 113 | -2415 | -445 | VLOUT1 |
| 114 | -2345 | -445 | VLOUT1 |
| 115 | -2275 | -445 | VLOUT1 |
| 116 | -2205 | -445 | VLOUT1 |
| 117 | -2135 | -445 | DUMMY |
| 118 | -2065 | -445 | ATEST |
| 119 | -1995 | -445 | DUMMY |
| 120 | -1925 | -445 | VGS |
| 121 | -1855 | -445 | VGS |
| 122 | -1785 | -445 | DUMMY |
| 123 | -1715 | -445 | VSS(ANALOG) |
| 124 | -1645 | -445 | VSS(ANALOG) |
| 125 | -1575 | -445 | VSS(ANALOG) |
| 126 | -1505 | -445 | VSS(ANALOG) |
| 127 | -1435 | -445 | VSS(ANALOG) |
| 128 | -1365 | -445 | VSS(ANALOG) |
| 129 | -1295 | -445 | VSS(OSC) |
| 130 | -1225 | -445 | VSS(OSC) |
| 131 | -1155 | -445 | VSS(OSC) |
| 132 | -1085 | -445 | VSS(OSC) |
| 133 | -1015 | -445 | VSS(MV) |
| 134 | -945 | -445 | VSS(MV) |
| 135 | -875 | -445 | VSS(MV) |
| 136 | -805 | -445 | VSS(MV) |
| 137 | -735 | -445 | VSS(MV) |
| 138 | -665 | -445 | VSS(MV) |
| 139 | -595 | -445 | DUMMY |
| 140 | -525 | -445 | C12P |
| 141 | -455 | -445 | C12P |
| 142 | -385 | -445 | C12P |
| 143 | -315 | -445 | C12P |
| 144 | -245 | -445 | C12P |
| 145 | -175 | -445 | C12P |
| 146 | -105 | -445 | DUMMY |
| 147 | -35 | -445 | C12M |
| 148 | 35 | -445 | C12M |
| 149 | 105 | -445 | C12M |
| 150 | 175 | -445 | C12M |

| Pin No | X | Y | Pad Name |
|--------|------|------|----------|
| 151 | 245 | -445 | C12M |
| 152 | 315 | -445 | C12M |
| 153 | 385 | -445 | DUMMY |
| 154 | 455 | -445 | C11P |
| 155 | 525 | -445 | C11P |
| 156 | 595 | -445 | C11P |
| 157 | 665 | -445 | C11P |
| 158 | 735 | -445 | C11P |
| 159 | 805 | -445 | C11P |
| 160 | 875 | -445 | DUMMY |
| 161 | 945 | -445 | C11M |
| 162 | 1015 | -445 | C11M |
| 163 | 1085 | -445 | C11M |
| 164 | 1155 | -445 | C11M |
| 165 | 1225 | -445 | C11M |
| 166 | 1295 | -445 | C11M |
| 167 | 1365 | -445 | DUMMY |
| 168 | 1435 | -445 | VCI1OUT |
| 169 | 1505 | -445 | VCI1OUT |
| 170 | 1575 | -445 | DUMMY |
| 171 | 1645 | -445 | VCI1OUT |
| 172 | 1715 | -445 | VCI1OUT |
| 173 | 1785 | -445 | VCI1OUT |
| 174 | 1855 | -445 | VCI1OUT |
| 175 | 1925 | -445 | VCI1OUT |
| 176 | 1995 | -445 | VCI1OUT |
| 177 | 2065 | -445 | DUMMY |
| 178 | 2135 | -445 | OSC2 |
| 179 | 2205 | -445 | DUMMY |
| 180 | 2275 | -445 | OSC1 |
| 181 | 2345 | -445 | DUMMY |
| 182 | 2415 | -445 | VCI(MV) |
| 183 | 2485 | -445 | VCI(MV) |
| 184 | 2555 | -445 | VCI(MV) |
| 185 | 2625 | -445 | VCI(MV) |
| 186 | 2695 | -445 | VCI(MV) |
| 187 | 2765 | -445 | VCI(MV) |
| 188 | 2835 | -445 | VCC |
| 189 | 2905 | -445 | VCC |
| 190 | 2975 | -445 | VCC |
| 191 | 3045 | -445 | VCC |
| 192 | 3115 | -445 | VCC |
| 193 | 3185 | -445 | VCC |
| 194 | 3255 | -445 | VCI(MV) |
| 195 | 3325 | -445 | VCI(MV) |
| 196 | 3395 | -445 | VCI(MV) |
| 197 | 3465 | -445 | VCI(MV) |
| 198 | 3535 | -445 | VCI(MV) |
| 199 | 3605 | -445 | VCI(MV) |
| 200 | 3675 | -445 | IOVCC |

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**960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout**

| Pin No | X | Y | Pad Name |
|--------|------|------|----------|
| 201 | 3745 | -445 | IOVCC |
| 202 | 3815 | -445 | IOVCC |
| 203 | 3885 | -445 | IOVCC |
| 204 | 3955 | -445 | IOVCC |
| 205 | 4025 | -445 | IOVCC |
| 206 | 4095 | -445 | DUMMY |
| 207 | 4165 | -445 | VCCL |
| 208 | 4235 | -445 | VCCL |
| 209 | 4305 | -445 | VCCL |
| 210 | 4375 | -445 | VCCL |
| 211 | 4445 | -445 | VCCL |
| 212 | 4515 | -445 | VCCL |
| 213 | 4585 | -445 | DUMMY |
| 214 | 4655 | -445 | VPP1 |
| 215 | 4725 | -445 | VPP1 |
| 216 | 4795 | -445 | VPP2 |
| 217 | 4865 | -445 | VPP2 |
| 218 | 4935 | -445 | VPP3 |
| 219 | 5005 | -445 | VPP3 |
| 220 | 5075 | -445 | IOVSSDUM |
| 221 | 5145 | -445 | REGOFF |
| 222 | 5215 | -445 | IOVCCDUM |
| 223 | 5285 | -445 | RESETB |
| 224 | 5355 | -445 | FSYNC |
| 225 | 5425 | -445 | DUMMY |
| 226 | 5495 | -445 | DB0 |
| 227 | 5565 | -445 | DB1 |
| 228 | 5635 | -445 | DB2 |
| 229 | 5705 | -445 | DB3 |
| 230 | 5775 | -445 | DB4 |
| 231 | 5845 | -445 | DB5 |
| 232 | 5915 | -445 | DB6 |
| 233 | 5985 | -445 | DB7 |
| 234 | 6055 | -445 | DB8 |
| 235 | 6125 | -445 | DB9 |
| 236 | 6195 | -445 | DB10 |
| 237 | 6265 | -445 | DB11 |
| 238 | 6335 | -445 | DUMMY |
| 239 | 6405 | -445 | DB12 |
| 240 | 6475 | -445 | DB13 |
| 241 | 6545 | -445 | DB14 |
| 242 | 6615 | -445 | DB15 |
| 243 | 6685 | -445 | DB16 |
| 244 | 6755 | -445 | DB17 |
| 245 | 6825 | -445 | DB18 |
| 246 | 6895 | -445 | DB19 |
| 247 | 6965 | -445 | DB20 |
| 248 | 7035 | -445 | DB21 |
| 249 | 7105 | -445 | DB22 |
| 250 | 7175 | -445 | DB23 |

| Pin No | X | Y | Pad Name |
|--------|-------|------|------------|
| 251 | 7245 | -445 | IOVSS_S |
| 252 | 7315 | -445 | IOVSS_S |
| 253 | 7385 | -445 | DOTCLK |
| 254 | 7455 | -445 | DOTCLK |
| 255 | 7525 | -445 | IOVSS_S |
| 256 | 7595 | -445 | IOVSS_S |
| 257 | 7665 | -445 | HSYNC |
| 258 | 7735 | -445 | VSYN |
| 259 | 7805 | -445 | ENABLE |
| 260 | 7875 | -445 | SDO |
| 261 | 7945 | -445 | SDI |
| 262 | 8015 | -445 | SCL |
| 263 | 8085 | -445 | RS |
| 264 | 8155 | -445 | CSB |
| 265 | 8225 | -445 | IM0 |
| 266 | 8295 | -445 | IOVCCDUM |
| 267 | 8365 | -445 | IM1 |
| 268 | 8435 | -445 | IOVSSDUM |
| 269 | 8505 | -445 | IOVSS |
| 270 | 8575 | -445 | IOVSS |
| 271 | 8645 | -445 | IOVSS |
| 272 | 8715 | -445 | IOVSS |
| 273 | 8785 | -445 | IOVSS |
| 274 | 8855 | -445 | IOVSS |
| 275 | 8925 | -445 | VSS(LOGIC) |
| 276 | 8995 | -445 | VSS(LOGIC) |
| 277 | 9065 | -445 | VSS(LOGIC) |
| 278 | 9135 | -445 | VSS(LOGIC) |
| 279 | 9205 | -445 | VSS(LOGIC) |
| 280 | 9275 | -445 | VSS(LOGIC) |
| 281 | 9345 | -445 | VSS(SDRV) |
| 282 | 9415 | -445 | VSS(SDRV) |
| 283 | 9485 | -445 | VSS(SDRV) |
| 284 | 9555 | -445 | VSS(SDRV) |
| 285 | 9625 | -445 | VSS(SDRV) |
| 286 | 9695 | -445 | VSS(SDRV) |
| 287 | 9765 | -445 | DUMMY |
| 288 | 9835 | -445 | ELVDDON |
| 289 | 9905 | -445 | DUMMY |
| 290 | 9975 | -445 | VINT |
| 291 | 10045 | -445 | VINT |
| 292 | 10115 | -445 | VINT |
| 293 | 10185 | -445 | VINT |
| 294 | 10255 | -445 | DUMMYS1 |
| 295 | 10495 | -220 | EMFLM |
| 296 | 10495 | -150 | EMCLK1 |
| 297 | 10495 | -80 | EMCLK1B |
| 298 | 10495 | -10 | EMCLK2 |
| 299 | 10495 | 60 | EMCLK2B |
| 300 | 10495 | 130 | ESR |


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**960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout**

| Pin No | X | Y | Pad Name |
|--------|-------|-----|----------|
| 301 | 10269 | 431 | DUMMY |
| 302 | 10248 | 286 | DUMMY |
| 303 | 10227 | 431 | DUMMY |
| 304 | 10206 | 286 | DUMMY |
| 305 | 10185 | 431 | DUMMY |
| 306 | 10164 | 286 | DUMMY |
| 307 | 10143 | 431 | SOUT1 |
| 308 | 10122 | 286 | SOUT2 |
| 309 | 10101 | 431 | SOUT3 |
| 310 | 10080 | 286 | SOUT4 |
| 311 | 10059 | 431 | SOUT5 |
| 312 | 10038 | 286 | SOUT6 |
| 313 | 10017 | 431 | SOUT7 |
| 314 | 9996 | 286 | SOUT8 |
| 315 | 9975 | 431 | SOUT9 |
| 316 | 9954 | 286 | SOUT10 |
| 317 | 9933 | 431 | SOUT11 |
| 318 | 9912 | 286 | SOUT12 |
| 319 | 9891 | 431 | SOUT13 |
| 320 | 9870 | 286 | SOUT14 |
| 321 | 9849 | 431 | SOUT15 |
| 322 | 9828 | 286 | SOUT16 |
| 323 | 9807 | 431 | SOUT17 |
| 324 | 9786 | 286 | SOUT18 |
| 325 | 9765 | 431 | SOUT19 |
| 326 | 9744 | 286 | SOUT20 |
| 327 | 9723 | 431 | SOUT21 |
| 328 | 9702 | 286 | SOUT22 |
| 329 | 9681 | 431 | SOUT23 |
| 330 | 9660 | 286 | SOUT24 |
| 331 | 9639 | 431 | SOUT25 |
| 332 | 9618 | 286 | SOUT26 |
| 333 | 9597 | 431 | SOUT27 |
| 334 | 9576 | 286 | SOUT28 |
| 335 | 9555 | 431 | SOUT29 |
| 336 | 9534 | 286 | SOUT30 |
| 337 | 9513 | 431 | SOUT31 |
| 338 | 9492 | 286 | SOUT32 |
| 339 | 9471 | 431 | SOUT33 |
| 340 | 9450 | 286 | SOUT34 |
| 341 | 9429 | 431 | SOUT35 |
| 342 | 9408 | 286 | SOUT36 |
| 343 | 9387 | 431 | SOUT37 |
| 344 | 9366 | 286 | SOUT38 |
| 345 | 9345 | 431 | SOUT39 |
| 346 | 9324 | 286 | SOUT40 |
| 347 | 9303 | 431 | SOUT41 |
| 348 | 9282 | 286 | SOUT42 |
| 349 | 9261 | 431 | SOUT43 |
| 350 | 9240 | 286 | SOUT44 |

| Pin No | X | Y | Pad Name |
|--------|------|-----|----------|
| 351 | 9219 | 431 | SOUT45 |
| 352 | 9198 | 286 | SOUT46 |
| 353 | 9177 | 431 | SOUT47 |
| 354 | 9156 | 286 | SOUT48 |
| 355 | 9135 | 431 | SOUT49 |
| 356 | 9114 | 286 | SOUT50 |
| 357 | 9093 | 431 | SOUT51 |
| 358 | 9072 | 286 | SOUT52 |
| 359 | 9051 | 431 | SOUT53 |
| 360 | 9030 | 286 | SOUT54 |
| 361 | 9009 | 431 | SOUT55 |
| 362 | 8988 | 286 | SOUT56 |
| 363 | 8967 | 431 | SOUT57 |
| 364 | 8946 | 286 | SOUT58 |
| 365 | 8925 | 431 | SOUT59 |
| 366 | 8904 | 286 | SOUT60 |
| 367 | 8883 | 431 | SOUT61 |
| 368 | 8862 | 286 | SOUT62 |
| 369 | 8841 | 431 | SOUT63 |
| 370 | 8820 | 286 | SOUT64 |
| 371 | 8799 | 431 | SOUT65 |
| 372 | 8778 | 286 | SOUT66 |
| 373 | 8757 | 431 | SOUT67 |
| 374 | 8736 | 286 | SOUT68 |
| 375 | 8715 | 431 | SOUT69 |
| 376 | 8694 | 286 | SOUT70 |
| 377 | 8673 | 431 | SOUT71 |
| 378 | 8652 | 286 | SOUT72 |
| 379 | 8631 | 431 | SOUT73 |
| 380 | 8610 | 286 | SOUT74 |
| 381 | 8589 | 431 | SOUT75 |
| 382 | 8568 | 286 | SOUT76 |
| 383 | 8547 | 431 | SOUT77 |
| 384 | 8526 | 286 | SOUT78 |
| 385 | 8505 | 431 | SOUT79 |
| 386 | 8484 | 286 | SOUT80 |
| 387 | 8463 | 431 | SOUT81 |
| 388 | 8442 | 286 | SOUT82 |
| 389 | 8421 | 431 | SOUT83 |
| 390 | 8400 | 286 | SOUT84 |
| 391 | 8379 | 431 | SOUT85 |
| 392 | 8358 | 286 | SOUT86 |
| 393 | 8337 | 431 | SOUT87 |
| 394 | 8316 | 286 | SOUT88 |
| 395 | 8295 | 431 | SOUT89 |
| 396 | 8274 | 286 | SOUT90 |
| 397 | 8253 | 431 | SOUT91 |
| 398 | 8232 | 286 | SOUT92 |
| 399 | 8211 | 431 | SOUT93 |
| 400 | 8190 | 286 | SOUT94 |

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**960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout**

| Pin No | X | Y | Pad Name |
|--------|------|-----|----------|
| 401 | 8169 | 431 | SOUT95 |
| 402 | 8148 | 286 | SOUT96 |
| 403 | 8127 | 431 | SOUT97 |
| 404 | 8106 | 286 | SOUT98 |
| 405 | 8085 | 431 | SOUT99 |
| 406 | 8064 | 286 | SOUT100 |
| 407 | 8043 | 431 | SOUT101 |
| 408 | 8022 | 286 | SOUT102 |
| 409 | 8001 | 431 | SOUT103 |
| 410 | 7980 | 286 | SOUT104 |
| 411 | 7959 | 431 | SOUT105 |
| 412 | 7938 | 286 | SOUT106 |
| 413 | 7917 | 431 | SOUT107 |
| 414 | 7896 | 286 | SOUT108 |
| 415 | 7875 | 431 | SOUT109 |
| 416 | 7854 | 286 | SOUT110 |
| 417 | 7833 | 431 | SOUT111 |
| 418 | 7812 | 286 | SOUT112 |
| 419 | 7791 | 431 | SOUT113 |
| 420 | 7770 | 286 | SOUT114 |
| 421 | 7749 | 431 | SOUT115 |
| 422 | 7728 | 286 | SOUT116 |
| 423 | 7707 | 431 | SOUT117 |
| 424 | 7686 | 286 | SOUT118 |
| 425 | 7665 | 431 | SOUT119 |
| 426 | 7644 | 286 | SOUT120 |
| 427 | 7623 | 431 | SOUT121 |
| 428 | 7602 | 286 | SOUT122 |
| 429 | 7581 | 431 | SOUT123 |
| 430 | 7560 | 286 | SOUT124 |
| 431 | 7539 | 431 | SOUT125 |
| 432 | 7518 | 286 | SOUT126 |
| 433 | 7497 | 431 | SOUT127 |
| 434 | 7476 | 286 | SOUT128 |
| 435 | 7455 | 431 | SOUT129 |
| 436 | 7434 | 286 | SOUT130 |
| 437 | 7413 | 431 | SOUT131 |
| 438 | 7392 | 286 | SOUT132 |
| 439 | 7371 | 431 | SOUT133 |
| 440 | 7350 | 286 | SOUT134 |
| 441 | 7329 | 431 | SOUT135 |
| 442 | 7308 | 286 | SOUT136 |
| 443 | 7287 | 431 | SOUT137 |
| 444 | 7266 | 286 | SOUT138 |
| 445 | 7245 | 431 | SOUT139 |
| 446 | 7224 | 286 | SOUT140 |
| 447 | 7203 | 431 | SOUT141 |
| 448 | 7182 | 286 | SOUT142 |
| 449 | 7161 | 431 | SOUT143 |
| 450 | 7140 | 286 | SOUT144 |

| Pin No | X | Y | Pad Name |
|--------|------|-----|----------|
| 451 | 7119 | 431 | SOUT145 |
| 452 | 7098 | 286 | SOUT146 |
| 453 | 7077 | 431 | SOUT147 |
| 454 | 7056 | 286 | SOUT148 |
| 455 | 7035 | 431 | SOUT149 |
| 456 | 7014 | 286 | SOUT150 |
| 457 | 6993 | 431 | SOUT151 |
| 458 | 6972 | 286 | SOUT152 |
| 459 | 6951 | 431 | SOUT153 |
| 460 | 6930 | 286 | SOUT154 |
| 461 | 6909 | 431 | SOUT155 |
| 462 | 6888 | 286 | SOUT156 |
| 463 | 6867 | 431 | SOUT157 |
| 464 | 6846 | 286 | SOUT158 |
| 465 | 6825 | 431 | SOUT159 |
| 466 | 6804 | 286 | SOUT160 |
| 467 | 6783 | 431 | SOUT161 |
| 468 | 6762 | 286 | SOUT162 |
| 469 | 6741 | 431 | SOUT163 |
| 470 | 6720 | 286 | SOUT164 |
| 471 | 6699 | 431 | SOUT165 |
| 472 | 6678 | 286 | SOUT166 |
| 473 | 6657 | 431 | SOUT167 |
| 474 | 6636 | 286 | SOUT168 |
| 475 | 6615 | 431 | SOUT169 |
| 476 | 6594 | 286 | SOUT170 |
| 477 | 6573 | 431 | SOUT171 |
| 478 | 6552 | 286 | SOUT172 |
| 479 | 6531 | 431 | SOUT173 |
| 480 | 6510 | 286 | SOUT174 |
| 481 | 6489 | 431 | SOUT175 |
| 482 | 6468 | 286 | SOUT176 |
| 483 | 6447 | 431 | SOUT177 |
| 484 | 6426 | 286 | SOUT178 |
| 485 | 6405 | 431 | SOUT179 |
| 486 | 6384 | 286 | SOUT180 |
| 487 | 6363 | 431 | SOUT181 |
| 488 | 6342 | 286 | SOUT182 |
| 489 | 6321 | 431 | SOUT183 |
| 490 | 6300 | 286 | SOUT184 |
| 491 | 6279 | 431 | SOUT185 |
| 492 | 6258 | 286 | SOUT186 |
| 493 | 6237 | 431 | SOUT187 |
| 494 | 6216 | 286 | SOUT188 |
| 495 | 6195 | 431 | SOUT189 |
| 496 | 6174 | 286 | SOUT190 |
| 497 | 6153 | 431 | SOUT191 |
| 498 | 6132 | 286 | SOUT192 |
| 499 | 6111 | 431 | SOUT193 |
| 500 | 6090 | 286 | SOUT194 |


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**960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout**

| Pin No | X | Y | Pad Name |
|--------|------|-----|----------|
| 501 | 6069 | 431 | SOUT195 |
| 502 | 6048 | 286 | SOUT196 |
| 503 | 6027 | 431 | SOUT197 |
| 504 | 6006 | 286 | SOUT198 |
| 505 | 5985 | 431 | SOUT199 |
| 506 | 5964 | 286 | SOUT200 |
| 507 | 5943 | 431 | SOUT201 |
| 508 | 5922 | 286 | SOUT202 |
| 509 | 5901 | 431 | SOUT203 |
| 510 | 5880 | 286 | SOUT204 |
| 511 | 5859 | 431 | SOUT205 |
| 512 | 5838 | 286 | SOUT206 |
| 513 | 5817 | 431 | SOUT207 |
| 514 | 5796 | 286 | SOUT208 |
| 515 | 5775 | 431 | SOUT209 |
| 516 | 5754 | 286 | SOUT210 |
| 517 | 5733 | 431 | SOUT211 |
| 518 | 5712 | 286 | SOUT212 |
| 519 | 5691 | 431 | SOUT213 |
| 520 | 5670 | 286 | SOUT214 |
| 521 | 5649 | 431 | SOUT215 |
| 522 | 5628 | 286 | SOUT216 |
| 523 | 5607 | 431 | SOUT217 |
| 524 | 5586 | 286 | SOUT218 |
| 525 | 5565 | 431 | SOUT219 |
| 526 | 5544 | 286 | SOUT220 |
| 527 | 5523 | 431 | SOUT221 |
| 528 | 5502 | 286 | SOUT222 |
| 529 | 5481 | 431 | SOUT223 |
| 530 | 5460 | 286 | SOUT224 |
| 531 | 5439 | 431 | SOUT225 |
| 532 | 5418 | 286 | SOUT226 |
| 533 | 5397 | 431 | SOUT227 |
| 534 | 5376 | 286 | SOUT228 |
| 535 | 5355 | 431 | SOUT229 |
| 536 | 5334 | 286 | SOUT230 |
| 537 | 5313 | 431 | SOUT231 |
| 538 | 5292 | 286 | SOUT232 |
| 539 | 5271 | 431 | SOUT233 |
| 540 | 5250 | 286 | SOUT234 |
| 541 | 5229 | 431 | SOUT235 |
| 542 | 5208 | 286 | SOUT236 |
| 543 | 5187 | 431 | SOUT237 |
| 544 | 5166 | 286 | SOUT238 |
| 545 | 5145 | 431 | SOUT239 |
| 546 | 5124 | 286 | SOUT240 |
| 547 | 5103 | 431 | SOUT241 |
| 548 | 5082 | 286 | SOUT242 |
| 549 | 5061 | 431 | SOUT243 |
| 550 | 5040 | 286 | SOUT244 |

| Pin No | X | Y | Pad Name |
|--------|------|-----|----------|
| 551 | 5019 | 431 | SOUT245 |
| 552 | 4998 | 286 | SOUT246 |
| 553 | 4977 | 431 | SOUT247 |
| 554 | 4956 | 286 | SOUT248 |
| 555 | 4935 | 431 | SOUT249 |
| 556 | 4914 | 286 | SOUT250 |
| 557 | 4893 | 431 | SOUT251 |
| 558 | 4872 | 286 | SOUT252 |
| 559 | 4851 | 431 | SOUT253 |
| 560 | 4830 | 286 | SOUT254 |
| 561 | 4809 | 431 | SOUT255 |
| 562 | 4788 | 286 | SOUT256 |
| 563 | 4767 | 431 | SOUT257 |
| 564 | 4746 | 286 | SOUT258 |
| 565 | 4725 | 431 | SOUT259 |
| 566 | 4704 | 286 | SOUT260 |
| 567 | 4683 | 431 | SOUT261 |
| 568 | 4662 | 286 | SOUT262 |
| 569 | 4641 | 431 | SOUT263 |
| 570 | 4620 | 286 | SOUT264 |
| 571 | 4599 | 431 | SOUT265 |
| 572 | 4578 | 286 | SOUT266 |
| 573 | 4557 | 431 | SOUT267 |
| 574 | 4536 | 286 | SOUT268 |
| 575 | 4515 | 431 | SOUT269 |
| 576 | 4494 | 286 | SOUT270 |
| 577 | 4473 | 431 | SOUT271 |
| 578 | 4452 | 286 | SOUT272 |
| 579 | 4431 | 431 | SOUT273 |
| 580 | 4410 | 286 | SOUT274 |
| 581 | 4389 | 431 | SOUT275 |
| 582 | 4368 | 286 | SOUT276 |
| 583 | 4347 | 431 | SOUT277 |
| 584 | 4326 | 286 | SOUT278 |
| 585 | 4305 | 431 | SOUT279 |
| 586 | 4284 | 286 | SOUT280 |
| 587 | 4263 | 431 | SOUT281 |
| 588 | 4242 | 286 | SOUT282 |
| 589 | 4221 | 431 | SOUT283 |
| 590 | 4200 | 286 | SOUT284 |
| 591 | 4179 | 431 | SOUT285 |
| 592 | 4158 | 286 | SOUT286 |
| 593 | 4137 | 431 | SOUT287 |
| 594 | 4116 | 286 | SOUT288 |
| 595 | 4095 | 431 | SOUT289 |
| 596 | 4074 | 286 | SOUT290 |
| 597 | 4053 | 431 | SOUT291 |
| 598 | 4032 | 286 | SOUT292 |
| 599 | 4011 | 431 | SOUT293 |
| 600 | 3990 | 286 | SOUT294 |


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**960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout**

| Pin No | X | Y | Pad Name |
|--------|------|-----|----------|
| 601 | 3969 | 431 | SOUT295 |
| 602 | 3948 | 286 | SOUT296 |
| 603 | 3927 | 431 | SOUT297 |
| 604 | 3906 | 286 | SOUT298 |
| 605 | 3885 | 431 | SOUT299 |
| 606 | 3864 | 286 | SOUT300 |
| 607 | 3843 | 431 | SOUT301 |
| 608 | 3822 | 286 | SOUT302 |
| 609 | 3801 | 431 | SOUT303 |
| 610 | 3780 | 286 | SOUT304 |
| 611 | 3759 | 431 | SOUT305 |
| 612 | 3738 | 286 | SOUT306 |
| 613 | 3717 | 431 | SOUT307 |
| 614 | 3696 | 286 | SOUT308 |
| 615 | 3675 | 431 | SOUT309 |
| 616 | 3654 | 286 | SOUT310 |
| 617 | 3633 | 431 | SOUT311 |
| 618 | 3612 | 286 | SOUT312 |
| 619 | 3591 | 431 | SOUT313 |
| 620 | 3570 | 286 | SOUT314 |
| 621 | 3549 | 431 | SOUT315 |
| 622 | 3528 | 286 | SOUT316 |
| 623 | 3507 | 431 | SOUT317 |
| 624 | 3486 | 286 | SOUT318 |
| 625 | 3465 | 431 | SOUT319 |
| 626 | 3444 | 286 | SOUT320 |
| 627 | 3423 | 431 | SOUT321 |
| 628 | 3402 | 286 | SOUT322 |
| 629 | 3381 | 431 | SOUT323 |
| 630 | 3360 | 286 | SOUT324 |
| 631 | 3339 | 431 | SOUT325 |
| 632 | 3318 | 286 | SOUT326 |
| 633 | 3297 | 431 | SOUT327 |
| 634 | 3276 | 286 | SOUT328 |
| 635 | 3255 | 431 | SOUT329 |
| 636 | 3234 | 286 | SOUT330 |
| 637 | 3213 | 431 | SOUT331 |
| 638 | 3192 | 286 | SOUT332 |
| 639 | 3171 | 431 | SOUT333 |
| 640 | 3150 | 286 | SOUT334 |
| 641 | 3129 | 431 | SOUT335 |
| 642 | 3108 | 286 | SOUT336 |
| 643 | 3087 | 431 | SOUT337 |
| 644 | 3066 | 286 | SOUT338 |
| 645 | 3045 | 431 | SOUT339 |
| 646 | 3024 | 286 | SOUT340 |
| 647 | 3003 | 431 | SOUT341 |
| 648 | 2982 | 286 | SOUT342 |
| 649 | 2961 | 431 | SOUT343 |
| 650 | 2940 | 286 | SOUT344 |

| Pin No | X | Y | Pad Name |
|--------|------|-----|----------|
| 651 | 2919 | 431 | SOUT345 |
| 652 | 2898 | 286 | SOUT346 |
| 653 | 2877 | 431 | SOUT347 |
| 654 | 2856 | 286 | SOUT348 |
| 655 | 2835 | 431 | SOUT349 |
| 656 | 2814 | 286 | SOUT350 |
| 657 | 2793 | 431 | SOUT351 |
| 658 | 2772 | 286 | SOUT352 |
| 659 | 2751 | 431 | SOUT353 |
| 660 | 2730 | 286 | SOUT354 |
| 661 | 2709 | 431 | SOUT355 |
| 662 | 2688 | 286 | SOUT356 |
| 663 | 2667 | 431 | SOUT357 |
| 664 | 2646 | 286 | SOUT358 |
| 665 | 2625 | 431 | SOUT359 |
| 666 | 2604 | 286 | SOUT360 |
| 667 | 2583 | 431 | SOUT361 |
| 668 | 2562 | 286 | SOUT362 |
| 669 | 2541 | 431 | SOUT363 |
| 670 | 2520 | 286 | SOUT364 |
| 671 | 2499 | 431 | SOUT365 |
| 672 | 2478 | 286 | SOUT366 |
| 673 | 2457 | 431 | SOUT367 |
| 674 | 2436 | 286 | SOUT368 |
| 675 | 2415 | 431 | SOUT369 |
| 676 | 2394 | 286 | SOUT370 |
| 677 | 2373 | 431 | SOUT371 |
| 678 | 2352 | 286 | SOUT372 |
| 679 | 2331 | 431 | SOUT373 |
| 680 | 2310 | 286 | SOUT374 |
| 681 | 2289 | 431 | SOUT375 |
| 682 | 2268 | 286 | SOUT376 |
| 683 | 2247 | 431 | SOUT377 |
| 684 | 2226 | 286 | SOUT378 |
| 685 | 2205 | 431 | SOUT379 |
| 686 | 2184 | 286 | SOUT380 |
| 687 | 2163 | 431 | SOUT381 |
| 688 | 2142 | 286 | SOUT382 |
| 689 | 2121 | 431 | SOUT383 |
| 690 | 2100 | 286 | SOUT384 |
| 691 | 2079 | 431 | SOUT385 |
| 692 | 2058 | 286 | SOUT386 |
| 693 | 2037 | 431 | SOUT387 |
| 694 | 2016 | 286 | SOUT388 |
| 695 | 1995 | 431 | SOUT389 |
| 696 | 1974 | 286 | SOUT390 |
| 697 | 1953 | 431 | SOUT391 |
| 698 | 1932 | 286 | SOUT392 |
| 699 | 1911 | 431 | SOUT393 |
| 700 | 1890 | 286 | SOUT394 |

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**960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout**

| Pin No | X | Y | Pad Name |
|--------|------|-----|----------|
| 701 | 1869 | 431 | SOUT395 |
| 702 | 1848 | 286 | SOUT396 |
| 703 | 1827 | 431 | SOUT397 |
| 704 | 1806 | 286 | SOUT398 |
| 705 | 1785 | 431 | SOUT399 |
| 706 | 1764 | 286 | SOUT400 |
| 707 | 1743 | 431 | SOUT401 |
| 708 | 1722 | 286 | SOUT402 |
| 709 | 1701 | 431 | SOUT403 |
| 710 | 1680 | 286 | SOUT404 |
| 711 | 1659 | 431 | SOUT405 |
| 712 | 1638 | 286 | SOUT406 |
| 713 | 1617 | 431 | SOUT407 |
| 714 | 1596 | 286 | SOUT408 |
| 715 | 1575 | 431 | SOUT409 |
| 716 | 1554 | 286 | SOUT410 |
| 717 | 1533 | 431 | SOUT411 |
| 718 | 1512 | 286 | SOUT412 |
| 719 | 1491 | 431 | SOUT413 |
| 720 | 1470 | 286 | SOUT414 |
| 721 | 1449 | 431 | SOUT415 |
| 722 | 1428 | 286 | SOUT416 |
| 723 | 1407 | 431 | SOUT417 |
| 724 | 1386 | 286 | SOUT418 |
| 725 | 1365 | 431 | SOUT419 |
| 726 | 1344 | 286 | SOUT420 |
| 727 | 1323 | 431 | SOUT421 |
| 728 | 1302 | 286 | SOUT422 |
| 729 | 1281 | 431 | SOUT423 |
| 730 | 1260 | 286 | SOUT424 |
| 731 | 1239 | 431 | SOUT425 |
| 732 | 1218 | 286 | SOUT426 |
| 733 | 1197 | 431 | SOUT427 |
| 734 | 1176 | 286 | SOUT428 |
| 735 | 1155 | 431 | SOUT429 |
| 736 | 1134 | 286 | SOUT430 |
| 737 | 1113 | 431 | SOUT431 |
| 738 | 1092 | 286 | SOUT432 |
| 739 | 1071 | 431 | SOUT433 |
| 740 | 1050 | 286 | SOUT434 |
| 741 | 1029 | 431 | SOUT435 |
| 742 | 1008 | 286 | SOUT436 |
| 743 | 987 | 431 | SOUT437 |
| 744 | 966 | 286 | SOUT438 |
| 745 | 945 | 431 | SOUT439 |
| 746 | 924 | 286 | SOUT440 |
| 747 | 903 | 431 | SOUT441 |
| 748 | 882 | 286 | SOUT442 |
| 749 | 861 | 431 | SOUT443 |
| 750 | 840 | 286 | SOUT444 |

| Pin No | X | Y | Pad Name |
|--------|------|-----|----------|
| 751 | 819 | 431 | SOUT445 |
| 752 | 798 | 286 | SOUT446 |
| 753 | 777 | 431 | SOUT447 |
| 754 | 756 | 286 | SOUT448 |
| 755 | 735 | 431 | SOUT449 |
| 756 | 714 | 286 | SOUT450 |
| 757 | 693 | 431 | SOUT451 |
| 758 | 672 | 286 | SOUT452 |
| 759 | 651 | 431 | SOUT453 |
| 760 | 630 | 286 | SOUT454 |
| 761 | 609 | 431 | SOUT455 |
| 762 | 588 | 286 | SOUT456 |
| 763 | 567 | 431 | SOUT457 |
| 764 | 546 | 286 | SOUT458 |
| 765 | 525 | 431 | SOUT459 |
| 766 | 504 | 286 | SOUT460 |
| 767 | 483 | 431 | SOUT461 |
| 768 | 462 | 286 | SOUT462 |
| 769 | 441 | 431 | SOUT463 |
| 770 | 420 | 286 | SOUT464 |
| 771 | 399 | 431 | SOUT465 |
| 772 | 378 | 286 | SOUT466 |
| 773 | 357 | 431 | SOUT467 |
| 774 | 336 | 286 | SOUT468 |
| 775 | 315 | 431 | SOUT469 |
| 776 | 294 | 286 | SOUT470 |
| 777 | 273 | 431 | SOUT471 |
| 778 | 252 | 286 | SOUT472 |
| 779 | 231 | 431 | SOUT473 |
| 780 | 210 | 286 | SOUT474 |
| 781 | 189 | 431 | SOUT475 |
| 782 | 168 | 286 | SOUT476 |
| 783 | 147 | 431 | SOUT477 |
| 784 | 126 | 286 | SOUT478 |
| 785 | 105 | 431 | SOUT479 |
| 786 | 84 | 286 | SOUT480 |
| 787 | 63 | 431 | DUMMY |
| 788 | 42 | 286 | DUMMY |
| 789 | 21 | 431 | DUMMY |
| 790 | 0 | 286 | DUMMY |
| 791 | -21 | 431 | DUMMY |
| 792 | -42 | 286 | DUMMY |
| 793 | -63 | 431 | DUMMY |
| 794 | -84 | 286 | SOUT481 |
| 795 | -105 | 431 | SOUT482 |
| 796 | -126 | 286 | SOUT483 |
| 797 | -147 | 431 | SOUT484 |
| 798 | -168 | 286 | SOUT485 |
| 799 | -189 | 431 | SOUT486 |
| 800 | -210 | 286 | SOUT487 |

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**960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout**

| Pin No | X | Y | Pad Name |
|--------|-------|-----|----------|
| 801 | -231 | 431 | SOUT488 |
| 802 | -252 | 286 | SOUT489 |
| 803 | -273 | 431 | SOUT490 |
| 804 | -294 | 286 | SOUT491 |
| 805 | -315 | 431 | SOUT492 |
| 806 | -336 | 286 | SOUT493 |
| 807 | -357 | 431 | SOUT494 |
| 808 | -378 | 286 | SOUT495 |
| 809 | -399 | 431 | SOUT496 |
| 810 | -420 | 286 | SOUT497 |
| 811 | -441 | 431 | SOUT498 |
| 812 | -462 | 286 | SOUT499 |
| 813 | -483 | 431 | SOUT500 |
| 814 | -504 | 286 | SOUT501 |
| 815 | -525 | 431 | SOUT502 |
| 816 | -546 | 286 | SOUT503 |
| 817 | -567 | 431 | SOUT504 |
| 818 | -588 | 286 | SOUT505 |
| 819 | -609 | 431 | SOUT506 |
| 820 | -630 | 286 | SOUT507 |
| 821 | -651 | 431 | SOUT508 |
| 822 | -672 | 286 | SOUT509 |
| 823 | -693 | 431 | SOUT510 |
| 824 | -714 | 286 | SOUT511 |
| 825 | -735 | 431 | SOUT512 |
| 826 | -756 | 286 | SOUT513 |
| 827 | -777 | 431 | SOUT514 |
| 828 | -798 | 286 | SOUT515 |
| 829 | -819 | 431 | SOUT516 |
| 830 | -840 | 286 | SOUT517 |
| 831 | -861 | 431 | SOUT518 |
| 832 | -882 | 286 | SOUT519 |
| 833 | -903 | 431 | SOUT520 |
| 834 | -924 | 286 | SOUT521 |
| 835 | -945 | 431 | SOUT522 |
| 836 | -966 | 286 | SOUT523 |
| 837 | -987 | 431 | SOUT524 |
| 838 | -1008 | 286 | SOUT525 |
| 839 | -1029 | 431 | SOUT526 |
| 840 | -1050 | 286 | SOUT527 |
| 841 | -1071 | 431 | SOUT528 |
| 842 | -1092 | 286 | SOUT529 |
| 843 | -1113 | 431 | SOUT530 |
| 844 | -1134 | 286 | SOUT531 |
| 845 | -1155 | 431 | SOUT532 |
| 846 | -1176 | 286 | SOUT533 |
| 847 | -1197 | 431 | SOUT534 |
| 848 | -1218 | 286 | SOUT535 |
| 849 | -1239 | 431 | SOUT536 |
| 850 | -1260 | 286 | SOUT537 |

| Pin No | X | Y | Pad Name |
|--------|-------|-----|----------|
| 851 | -1281 | 431 | SOUT538 |
| 852 | -1302 | 286 | SOUT539 |
| 853 | -1323 | 431 | SOUT540 |
| 854 | -1344 | 286 | SOUT541 |
| 855 | -1365 | 431 | SOUT542 |
| 856 | -1386 | 286 | SOUT543 |
| 857 | -1407 | 431 | SOUT544 |
| 858 | -1428 | 286 | SOUT545 |
| 859 | -1449 | 431 | SOUT546 |
| 860 | -1470 | 286 | SOUT547 |
| 861 | -1491 | 431 | SOUT548 |
| 862 | -1512 | 286 | SOUT549 |
| 863 | -1533 | 431 | SOUT550 |
| 864 | -1554 | 286 | SOUT551 |
| 865 | -1575 | 431 | SOUT552 |
| 866 | -1596 | 286 | SOUT553 |
| 867 | -1617 | 431 | SOUT554 |
| 868 | -1638 | 286 | SOUT555 |
| 869 | -1659 | 431 | SOUT556 |
| 870 | -1680 | 286 | SOUT557 |
| 871 | -1701 | 431 | SOUT558 |
| 872 | -1722 | 286 | SOUT559 |
| 873 | -1743 | 431 | SOUT560 |
| 874 | -1764 | 286 | SOUT561 |
| 875 | -1785 | 431 | SOUT562 |
| 876 | -1806 | 286 | SOUT563 |
| 877 | -1827 | 431 | SOUT564 |
| 878 | -1848 | 286 | SOUT565 |
| 879 | -1869 | 431 | SOUT566 |
| 880 | -1890 | 286 | SOUT567 |
| 881 | -1911 | 431 | SOUT568 |
| 882 | -1932 | 286 | SOUT569 |
| 883 | -1953 | 431 | SOUT570 |
| 884 | -1974 | 286 | SOUT571 |
| 885 | -1995 | 431 | SOUT572 |
| 886 | -2016 | 286 | SOUT573 |
| 887 | -2037 | 431 | SOUT574 |
| 888 | -2058 | 286 | SOUT575 |
| 889 | -2079 | 431 | SOUT576 |
| 890 | -2100 | 286 | SOUT577 |
| 891 | -2121 | 431 | SOUT578 |
| 892 | -2142 | 286 | SOUT579 |
| 893 | -2163 | 431 | SOUT580 |
| 894 | -2184 | 286 | SOUT581 |
| 895 | -2205 | 431 | SOUT582 |
| 896 | -2226 | 286 | SOUT583 |
| 897 | -2247 | 431 | SOUT584 |
| 898 | -2268 | 286 | SOUT585 |
| 899 | -2289 | 431 | SOUT586 |
| 900 | -2310 | 286 | SOUT587 |


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**960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout**

| Pin No | X | Y | Pad Name |
|--------|-------|-----|----------|
| 901 | -2331 | 431 | SOUT588 |
| 902 | -2352 | 286 | SOUT589 |
| 903 | -2373 | 431 | SOUT590 |
| 904 | -2394 | 286 | SOUT591 |
| 905 | -2415 | 431 | SOUT592 |
| 906 | -2436 | 286 | SOUT593 |
| 907 | -2457 | 431 | SOUT594 |
| 908 | -2478 | 286 | SOUT595 |
| 909 | -2499 | 431 | SOUT596 |
| 910 | -2520 | 286 | SOUT597 |
| 911 | -2541 | 431 | SOUT598 |
| 912 | -2562 | 286 | SOUT599 |
| 913 | -2583 | 431 | SOUT600 |
| 914 | -2604 | 286 | SOUT601 |
| 915 | -2625 | 431 | SOUT602 |
| 916 | -2646 | 286 | SOUT603 |
| 917 | -2667 | 431 | SOUT604 |
| 918 | -2688 | 286 | SOUT605 |
| 919 | -2709 | 431 | SOUT606 |
| 920 | -2730 | 286 | SOUT607 |
| 921 | -2751 | 431 | SOUT608 |
| 922 | -2772 | 286 | SOUT609 |
| 923 | -2793 | 431 | SOUT610 |
| 924 | -2814 | 286 | SOUT611 |
| 925 | -2835 | 431 | SOUT612 |
| 926 | -2856 | 286 | SOUT613 |
| 927 | -2877 | 431 | SOUT614 |
| 928 | -2898 | 286 | SOUT615 |
| 929 | -2919 | 431 | SOUT616 |
| 930 | -2940 | 286 | SOUT617 |
| 931 | -2961 | 431 | SOUT618 |
| 932 | -2982 | 286 | SOUT619 |
| 933 | -3003 | 431 | SOUT620 |
| 934 | -3024 | 286 | SOUT621 |
| 935 | -3045 | 431 | SOUT622 |
| 936 | -3066 | 286 | SOUT623 |
| 937 | -3087 | 431 | SOUT624 |
| 938 | -3108 | 286 | SOUT625 |
| 939 | -3129 | 431 | SOUT626 |
| 940 | -3150 | 286 | SOUT627 |
| 941 | -3171 | 431 | SOUT628 |
| 942 | -3192 | 286 | SOUT629 |
| 943 | -3213 | 431 | SOUT630 |
| 944 | -3234 | 286 | SOUT631 |
| 945 | -3255 | 431 | SOUT632 |
| 946 | -3276 | 286 | SOUT633 |
| 947 | -3297 | 431 | SOUT634 |
| 948 | -3318 | 286 | SOUT635 |
| 949 | -3339 | 431 | SOUT636 |
| 950 | -3360 | 286 | SOUT637 |

| Pin No | X | Y | Pad Name |
|--------|-------|-----|----------|
| 951 | -3381 | 431 | SOUT638 |
| 952 | -3402 | 286 | SOUT639 |
| 953 | -3423 | 431 | SOUT640 |
| 954 | -3444 | 286 | SOUT641 |
| 955 | -3465 | 431 | SOUT642 |
| 956 | -3486 | 286 | SOUT643 |
| 957 | -3507 | 431 | SOUT644 |
| 958 | -3528 | 286 | SOUT645 |
| 959 | -3549 | 431 | SOUT646 |
| 960 | -3570 | 286 | SOUT647 |
| 961 | -3591 | 431 | SOUT648 |
| 962 | -3612 | 286 | SOUT649 |
| 963 | -3633 | 431 | SOUT650 |
| 964 | -3654 | 286 | SOUT651 |
| 965 | -3675 | 431 | SOUT652 |
| 966 | -3696 | 286 | SOUT653 |
| 967 | -3717 | 431 | SOUT654 |
| 968 | -3738 | 286 | SOUT655 |
| 969 | -3759 | 431 | SOUT656 |
| 970 | -3780 | 286 | SOUT657 |
| 971 | -3801 | 431 | SOUT658 |
| 972 | -3822 | 286 | SOUT659 |
| 973 | -3843 | 431 | SOUT660 |
| 974 | -3864 | 286 | SOUT661 |
| 975 | -3885 | 431 | SOUT662 |
| 976 | -3906 | 286 | SOUT663 |
| 977 | -3927 | 431 | SOUT664 |
| 978 | -3948 | 286 | SOUT665 |
| 979 | -3969 | 431 | SOUT666 |
| 980 | -3990 | 286 | SOUT667 |
| 981 | -4011 | 431 | SOUT668 |
| 982 | -4032 | 286 | SOUT669 |
| 983 | -4053 | 431 | SOUT670 |
| 984 | -4074 | 286 | SOUT671 |
| 985 | -4095 | 431 | SOUT672 |
| 986 | -4116 | 286 | SOUT673 |
| 987 | -4137 | 431 | SOUT674 |
| 988 | -4158 | 286 | SOUT675 |
| 989 | -4179 | 431 | SOUT676 |
| 990 | -4200 | 286 | SOUT677 |
| 991 | -4221 | 431 | SOUT678 |
| 992 | -4242 | 286 | SOUT679 |
| 993 | -4263 | 431 | SOUT680 |
| 994 | -4284 | 286 | SOUT681 |
| 995 | -4305 | 431 | SOUT682 |
| 996 | -4326 | 286 | SOUT683 |
| 997 | -4347 | 431 | SOUT684 |
| 998 | -4368 | 286 | SOUT685 |
| 999 | -4389 | 431 | SOUT686 |
| 1000 | -4410 | 286 | SOUT687 |

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**960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout**

| Pin No | X | Y | Pad Name |
|--------|-------|-----|----------|
| 1001 | -4431 | 431 | SOUT688 |
| 1002 | -4452 | 286 | SOUT689 |
| 1003 | -4473 | 431 | SOUT690 |
| 1004 | -4494 | 286 | SOUT691 |
| 1005 | -4515 | 431 | SOUT692 |
| 1006 | -4536 | 286 | SOUT693 |
| 1007 | -4557 | 431 | SOUT694 |
| 1008 | -4578 | 286 | SOUT695 |
| 1009 | -4599 | 431 | SOUT696 |
| 1010 | -4620 | 286 | SOUT697 |
| 1011 | -4641 | 431 | SOUT698 |
| 1012 | -4662 | 286 | SOUT699 |
| 1013 | -4683 | 431 | SOUT700 |
| 1014 | -4704 | 286 | SOUT701 |
| 1015 | -4725 | 431 | SOUT702 |
| 1016 | -4746 | 286 | SOUT703 |
| 1017 | -4767 | 431 | SOUT704 |
| 1018 | -4788 | 286 | SOUT705 |
| 1019 | -4809 | 431 | SOUT706 |
| 1020 | -4830 | 286 | SOUT707 |
| 1021 | -4851 | 431 | SOUT708 |
| 1022 | -4872 | 286 | SOUT709 |
| 1023 | -4893 | 431 | SOUT710 |
| 1024 | -4914 | 286 | SOUT711 |
| 1025 | -4935 | 431 | SOUT712 |
| 1026 | -4956 | 286 | SOUT713 |
| 1027 | -4977 | 431 | SOUT714 |
| 1028 | -4998 | 286 | SOUT715 |
| 1029 | -5019 | 431 | SOUT716 |
| 1030 | -5040 | 286 | SOUT717 |
| 1031 | -5061 | 431 | SOUT718 |
| 1032 | -5082 | 286 | SOUT719 |
| 1033 | -5103 | 431 | SOUT720 |
| 1034 | -5124 | 286 | SOUT721 |
| 1035 | -5145 | 431 | SOUT722 |
| 1036 | -5166 | 286 | SOUT723 |
| 1037 | -5187 | 431 | SOUT724 |
| 1038 | -5208 | 286 | SOUT725 |
| 1039 | -5229 | 431 | SOUT726 |
| 1040 | -5250 | 286 | SOUT727 |
| 1041 | -5271 | 431 | SOUT728 |
| 1042 | -5292 | 286 | SOUT729 |
| 1043 | -5313 | 431 | SOUT730 |
| 1044 | -5334 | 286 | SOUT731 |
| 1045 | -5355 | 431 | SOUT732 |
| 1046 | -5376 | 286 | SOUT733 |
| 1047 | -5397 | 431 | SOUT734 |
| 1048 | -5418 | 286 | SOUT735 |
| 1049 | -5439 | 431 | SOUT736 |
| 1050 | -5460 | 286 | SOUT737 |

| Pin No | X | Y | Pad Name |
|--------|-------|-----|----------|
| 1051 | -5481 | 431 | SOUT738 |
| 1052 | -5502 | 286 | SOUT739 |
| 1053 | -5523 | 431 | SOUT740 |
| 1054 | -5544 | 286 | SOUT741 |
| 1055 | -5565 | 431 | SOUT742 |
| 1056 | -5586 | 286 | SOUT743 |
| 1057 | -5607 | 431 | SOUT744 |
| 1058 | -5628 | 286 | SOUT745 |
| 1059 | -5649 | 431 | SOUT746 |
| 1060 | -5670 | 286 | SOUT747 |
| 1061 | -5691 | 431 | SOUT748 |
| 1062 | -5712 | 286 | SOUT749 |
| 1063 | -5733 | 431 | SOUT750 |
| 1064 | -5754 | 286 | SOUT751 |
| 1065 | -5775 | 431 | SOUT752 |
| 1066 | -5796 | 286 | SOUT753 |
| 1067 | -5817 | 431 | SOUT754 |
| 1068 | -5838 | 286 | SOUT755 |
| 1069 | -5859 | 431 | SOUT756 |
| 1070 | -5880 | 286 | SOUT757 |
| 1071 | -5901 | 431 | SOUT758 |
| 1072 | -5922 | 286 | SOUT759 |
| 1073 | -5943 | 431 | SOUT760 |
| 1074 | -5964 | 286 | SOUT761 |
| 1075 | -5985 | 431 | SOUT762 |
| 1076 | -6006 | 286 | SOUT763 |
| 1077 | -6027 | 431 | SOUT764 |
| 1078 | -6048 | 286 | SOUT765 |
| 1079 | -6069 | 431 | SOUT766 |
| 1080 | -6090 | 286 | SOUT767 |
| 1081 | -6111 | 431 | SOUT768 |
| 1082 | -6132 | 286 | SOUT769 |
| 1083 | -6153 | 431 | SOUT770 |
| 1084 | -6174 | 286 | SOUT771 |
| 1085 | -6195 | 431 | SOUT772 |
| 1086 | -6216 | 286 | SOUT773 |
| 1087 | -6237 | 431 | SOUT774 |
| 1088 | -6258 | 286 | SOUT775 |
| 1089 | -6279 | 431 | SOUT776 |
| 1090 | -6300 | 286 | SOUT777 |
| 1091 | -6321 | 431 | SOUT778 |
| 1092 | -6342 | 286 | SOUT779 |
| 1093 | -6363 | 431 | SOUT780 |
| 1094 | -6384 | 286 | SOUT781 |
| 1095 | -6405 | 431 | SOUT782 |
| 1096 | -6426 | 286 | SOUT783 |
| 1097 | -6447 | 431 | SOUT784 |
| 1098 | -6468 | 286 | SOUT785 |
| 1099 | -6489 | 431 | SOUT786 |
| 1100 | -6510 | 286 | SOUT787 |


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**960-channel source driver with power circuit for
16M colors gate-IC-less AMOLED with PenTile Layout**

| Pin No | X | Y | Pad Name |
|--------|-------|-----|----------|
| 1101 | -6531 | 431 | SOUT788 |
| 1102 | -6552 | 286 | SOUT789 |
| 1103 | -6573 | 431 | SOUT790 |
| 1104 | -6594 | 286 | SOUT791 |
| 1105 | -6615 | 431 | SOUT792 |
| 1106 | -6636 | 286 | SOUT793 |
| 1107 | -6657 | 431 | SOUT794 |
| 1108 | -6678 | 286 | SOUT795 |
| 1109 | -6699 | 431 | SOUT796 |
| 1110 | -6720 | 286 | SOUT797 |
| 1111 | -6741 | 431 | SOUT798 |
| 1112 | -6762 | 286 | SOUT799 |
| 1113 | -6783 | 431 | SOUT800 |
| 1114 | -6804 | 286 | SOUT801 |
| 1115 | -6825 | 431 | SOUT802 |
| 1116 | -6846 | 286 | SOUT803 |
| 1117 | -6867 | 431 | SOUT804 |
| 1118 | -6888 | 286 | SOUT805 |
| 1119 | -6909 | 431 | SOUT806 |
| 1120 | -6930 | 286 | SOUT807 |
| 1121 | -6951 | 431 | SOUT808 |
| 1122 | -6972 | 286 | SOUT809 |
| 1123 | -6993 | 431 | SOUT810 |
| 1124 | -7014 | 286 | SOUT811 |
| 1125 | -7035 | 431 | SOUT812 |
| 1126 | -7056 | 286 | SOUT813 |
| 1127 | -7077 | 431 | SOUT814 |
| 1128 | -7098 | 286 | SOUT815 |
| 1129 | -7119 | 431 | SOUT816 |
| 1130 | -7140 | 286 | SOUT817 |
| 1131 | -7161 | 431 | SOUT818 |
| 1132 | -7182 | 286 | SOUT819 |
| 1133 | -7203 | 431 | SOUT820 |
| 1134 | -7224 | 286 | SOUT821 |
| 1135 | -7245 | 431 | SOUT822 |
| 1136 | -7266 | 286 | SOUT823 |
| 1137 | -7287 | 431 | SOUT824 |
| 1138 | -7308 | 286 | SOUT825 |
| 1139 | -7329 | 431 | SOUT826 |
| 1140 | -7350 | 286 | SOUT827 |
| 1141 | -7371 | 431 | SOUT828 |
| 1142 | -7392 | 286 | SOUT829 |
| 1143 | -7413 | 431 | SOUT830 |
| 1144 | -7434 | 286 | SOUT831 |
| 1145 | -7455 | 431 | SOUT832 |
| 1146 | -7476 | 286 | SOUT833 |
| 1147 | -7497 | 431 | SOUT834 |
| 1148 | -7518 | 286 | SOUT835 |
| 1149 | -7539 | 431 | SOUT836 |
| 1150 | -7560 | 286 | SOUT837 |

| Pin No | X | Y | Pad Name |
|--------|-------|-----|----------|
| 1151 | -7581 | 431 | SOUT838 |
| 1152 | -7602 | 286 | SOUT839 |
| 1153 | -7623 | 431 | SOUT840 |
| 1154 | -7644 | 286 | SOUT841 |
| 1155 | -7665 | 431 | SOUT842 |
| 1156 | -7686 | 286 | SOUT843 |
| 1157 | -7707 | 431 | SOUT844 |
| 1158 | -7728 | 286 | SOUT845 |
| 1159 | -7749 | 431 | SOUT846 |
| 1160 | -7770 | 286 | SOUT847 |
| 1161 | -7791 | 431 | SOUT848 |
| 1162 | -7812 | 286 | SOUT849 |
| 1163 | -7833 | 431 | SOUT850 |
| 1164 | -7854 | 286 | SOUT851 |
| 1165 | -7875 | 431 | SOUT852 |
| 1166 | -7896 | 286 | SOUT853 |
| 1167 | -7917 | 431 | SOUT854 |
| 1168 | -7938 | 286 | SOUT855 |
| 1169 | -7959 | 431 | SOUT856 |
| 1170 | -7980 | 286 | SOUT857 |
| 1171 | -8001 | 431 | SOUT858 |
| 1172 | -8022 | 286 | SOUT859 |
| 1173 | -8043 | 431 | SOUT860 |
| 1174 | -8064 | 286 | SOUT861 |
| 1175 | -8085 | 431 | SOUT862 |
| 1176 | -8106 | 286 | SOUT863 |
| 1177 | -8127 | 431 | SOUT864 |
| 1178 | -8148 | 286 | SOUT865 |
| 1179 | -8169 | 431 | SOUT866 |
| 1180 | -8190 | 286 | SOUT867 |
| 1181 | -8211 | 431 | SOUT868 |
| 1182 | -8232 | 286 | SOUT869 |
| 1183 | -8253 | 431 | SOUT870 |
| 1184 | -8274 | 286 | SOUT871 |
| 1185 | -8295 | 431 | SOUT872 |
| 1186 | -8316 | 286 | SOUT873 |
| 1187 | -8337 | 431 | SOUT874 |
| 1188 | -8358 | 286 | SOUT875 |
| 1189 | -8379 | 431 | SOUT876 |
| 1190 | -8400 | 286 | SOUT877 |
| 1191 | -8421 | 431 | SOUT878 |
| 1192 | -8442 | 286 | SOUT879 |
| 1193 | -8463 | 431 | SOUT880 |
| 1194 | -8484 | 286 | SOUT881 |
| 1195 | -8505 | 431 | SOUT882 |
| 1196 | -8526 | 286 | SOUT883 |
| 1197 | -8547 | 431 | SOUT884 |
| 1198 | -8568 | 286 | SOUT885 |
| 1199 | -8589 | 431 | SOUT886 |
| 1200 | -8610 | 286 | SOUT887 |

TL2796

[illegible]

Revision History

| Rev | Date | Contents | Page |
|-----|------------|---------------------------------|------|
| 1.0 | 2007.07.10 | Delete Preliminary version. | - |
| 1.1 | 2009.01.19 | Add SOE bit in R27h instruction | P48 |

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