ESP32-A1S Specification

Version V2.3

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Formulation / Revision / Abolition of CV

Version	Date	Formulation / Revision	Make	Verify
V2.2	2019.11.01	First development		
V2.3	2021.06.09	Update data		

content

1. Product overview

ESP32-A1S is a Wi-Fi+BT voice module developed by Shenzhen Anxinke Technology Co., Ltd. The module's core processor chip ESP32 integrates 2.4 GHz Wi-Fi and Bluetooth dual mode, and the module also integrates ES8388 voice codec chip, PSRAM and Flash chip. It can be widely used in offline voice products and various IoT hardware terminal occasions.

ESP32 chip has industry-leading low-power performance and radio frequency performance, supports Wi-Fi IEEE802.11b/g/n protocol and Bluetooth V4.2 complete standard, including traditional Bluetooth (BR/EDR) and low energy Bluetooth (BLE) . The chip is equipped with an Xtensa® 32-bit LX6 dual-core processor with a computing power of up to 600 MIPS and a working frequency of up to 240 MHz. Support secondary development without using other microcontrollers or processors. The chip has built-in 520 KB SRAM, 448 KB ROM, 16KB RTC SRAM, and 1 Kbit eFuse. The chip supports a variety of low power consumption working states, which can meet the power consumption requirements of various application scenarios.

ES8388 is a low-power, cost-effective audio codec chip. It integrates 2 ADCs and 2 DACs, microphone amplifiers, headphone amplifiers, etc., which can be widely used in various home smart devices, smart audio, story machine solutions And so on, is the ideal solution for voice products.

The ESP32-A1S module provides a wealth of peripheral interfaces, including UART, PWM, SPI, I2S, I2C, ADC, DAC, SDIO and multiple GPIOs.

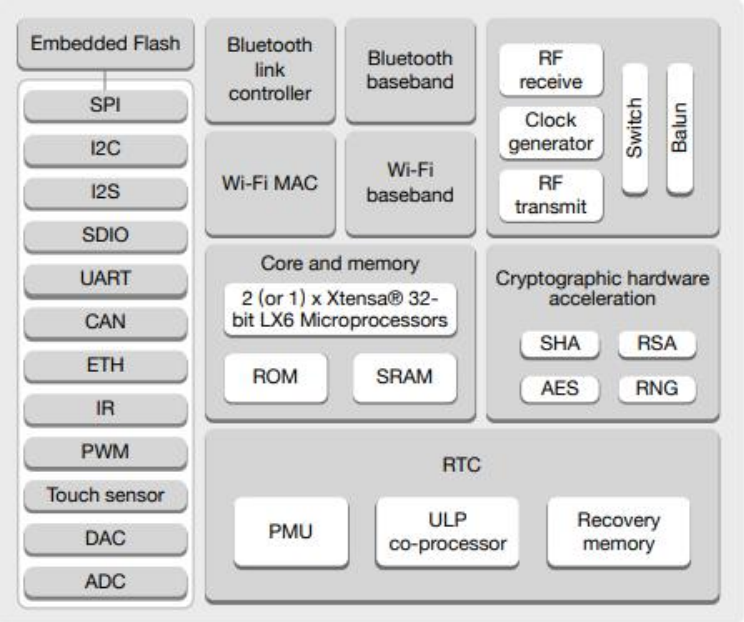

Figure 1 Main chip architecture diagram

1.1. Features

- Support Wi-Fi 802.11b/g/n, 1T1R mode data rate up to 150Mbps
- Support Bluetooth V4.2 complete standard, including traditional Bluetooth (BR/EDR) and low energy Bluetooth (BLE)
  Support standard Class-1, Class-2 and Class-3
- Xtensa® 32-bit LX6 dual-core processor, computing power up to 600 MIPS
- The chip has built-in 520 KB SRAM, 448 KB ROM, 16KB RTC SRAM, and 1 Kbit eFuse
- Support 2 audio input and 2 audio output, integrated microphone amplifier and headphone amplifier
- Support UART/GPIO/ADC/DAC/PWM/I2C/I2S interface
- Integrate 64Mb PSRAM
- Using SMD-38 package
- General AT commands can be used quickly
- Support secondary development, integrated Windows and Linux development environment

2. Main parameters

List 1 Main parameter description

Model	ESP32-A1S
Package	SMD-38
Size	31.5*19.0*3.1(±0.2)mm
Antenna	Onboard PCB antenna / compatible with IPEX antenna interface
Spectrum range	2400 ~ 2483.5MHz
Operating temperature	-40 ℃ ~ 85 ℃
Storage environment	-40 ℃ ~ 125 ℃ , < 90%RH
Power supply	Supply voltage 3.0V ~ 3.6V, supply current >500mA
Interface	UART/GPIO/ADC/PWM/I2C/I2S/microphone/headphone/speaker
Serial port rate	Support 110 ~ 4608000 bps, the default is 115200 bps
WiFi	802.11b/g/n
Bluetooth	Bluetooth 4.2 BR/EDR and BLE standards
Safety	WEP/WPA-PSK/WPA2-PSK

2.1.Electrical parameters

The ESP32-A1S module is an electrostatic sensitive device, and special precautions must be taken when handling it.

Figure 2 ESD Anti-static mark

2.2. Electrical characteristics

List 2 Main parameter description

Parameters		Condition	Min	Typical	Max	Unit
Voltage		VDD	3.0	3.3	3.6	V
I/O	V_{IL}/V_{IH}	-	-0.3/0.75VDD	-	0.25VDD/VDD+0.3	V
	V_{OL}/V_{OH}	-	N/0.8VIO	-	0.1VIO/N	V

2.3. WIFI RF performance

List 3 Main parameter description

Description	Typical	Unit
Working frequency	2400 - 2483.5	MHz
Output Power		
11n mode HT40, PA output power is	13±2	dBm
11n mode HT20, PA output power is	13±2	dBm
In 11g mode, the PA output power is	14±2	dBm
In 11b mode, PA output power is	18±2	dBm
Receiving sensitivity		
CCK, 1 Mbps	≤-96	dBm
CCK, 11 Mbps	≤-88	dBm
6 Mbps (1/2 BPSK)	≤-92	dBm
54 Mbps (3/4 64-QAM)	≤-74	dBm
HT20 (MCS7)	≤-72	dBm
HT40 (MCS7)	≤-70	dBm

2.4. Bluetooth（BR）RF performance

List 4 Main parameter description

Description	Typical	Unit
Output Power		
Transmit power	Typical 8±2	dBm
Receiving sensitivity Bluetooth low energy 1M		
Sensitivity@0.1%BER	≤-89	dBm

2.5. Bluetooth（EDR）RF performance

List 5 Main parameter description

Description	Typical	Unit
Output Power		
Transmit power	Typical 8±2	dBm
Receiving sensitivity Bluetooth low energy 1M		
Sensitivity@0.01%BER	≤-89	dBm

2.6. BLE RF performance

List 6 Main parameter description

Description	Typical	Unit
Output Power		
Transmit power	Typical 8±2	dBm
Receiving sensitivity Bluetooth low energy 1M		
Sensitivity@30.8%PER	≤-94	dBm

2.7. Power consumption

The following power consumption data is based on 3.3V power supply, 25°C

ambient temperature, and measured with an internal voltage regulator.

- All measurements are done at the antenna interface without SAW filter.
- All emission data is based on 50% duty cycle, measured in continuous emission mode.

List 7 Main parameter description

Mode	Min	Typical	Max	Unit
Transmit 802.11b, CCK 1Mbps, POUT=+19.5dBm	-	240	-	mA
Transmission 802.11g, OFDM 54Mbps, POUT = +16dBm	-	190	-	mA
Transmit 802.11n, MCS7, POUT = +14dBm	-	180	-	mA
Receive 802.11b, the packet length is 1024 bytes	-	95	-	mA
Receive 802.11g, the packet length is 1024 bytes	-	95	-	mA
Receive 802.11n, the packet length is 1024 bytes	-	93	-	mA
Modem-Sleep①	-	20	-	mA
Light-Sleep②	-	130	-	μA
Deep-Sleep③	-	5	-	μA
Power Off	-	1	-	μA

3. Dimensions

Figure 3 Module appearance diagram (rendered diagram is for reference only, the actual product shall prevail)

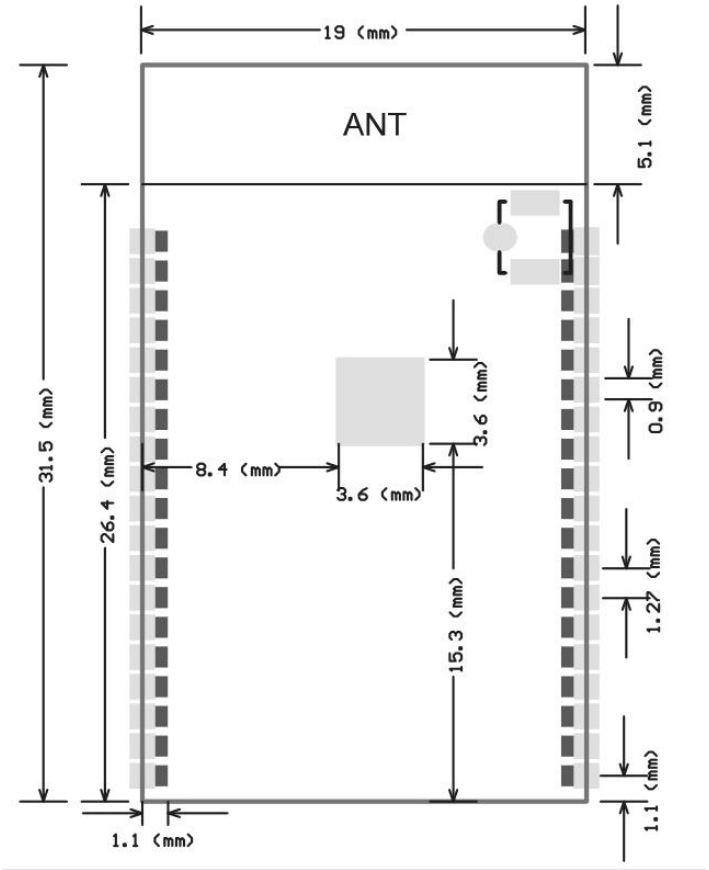

Figure 4 Module size chart

4. PIN definition

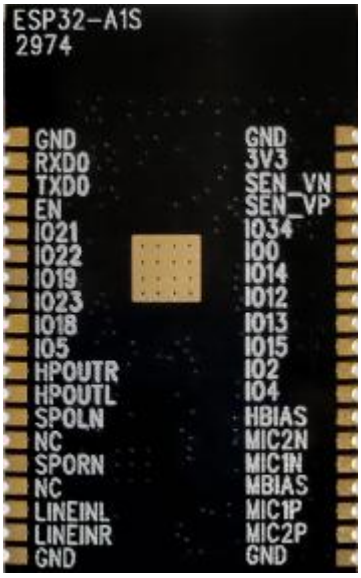

图 **5** 管脚示意图

The ESP32-A1S module has a total of 38 interfaces. As shown in the pin diagram, the pin function definition table is the interface definition.

List 8 ESP32-A1S Pin function definition table

No.	Name	Function Description
1	GND	Grounded
2	3V3	Power supply, recommended 3.3V, greater than 500mA
3	SENSOR_VN	GPI39, SENSOR_VN, ADC1_CH3, ADC_H, RTC_GPIO3
4	SENSOR_VP	GPI36, SENSOR_VP, ADC_H, ADC1_CH0, RTC_GPIO0
5	IO34	GPI34, ADC1_CH6, RTC_GPIO4
6	IO0	GPIO0, ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK
7	IO14	GPIO14, ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2
8	IO12	GPIO12, ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3
9	IO13	GPIO13, ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER
10	IO15	GPIO15, ADC2_CH3, TOUCH3, MTDO, HSPICS0,

		RTC_GPIO13, HS2_CMD, SD_CMD, EMAC_RXD3
11	IO2	GPIO2, ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SD_DATA0
12	IO4	GPIO4, ADC2_CH0, TOUCH0, RTC_GPIO10, HSPIHD, HS2_DATA1, SD_DATA1, EMAC_TX_ER
13	HBIAS	Pull up to AVCC by internal 1K resistor
14	MIC2N	Audio chip RIN2 channel
15	MIC1N	Audio chip RIN1 channel
16	MBIAS	Pull up to AVCC by internal 1K resistor
17	MIC1P	Audio chip LIN1 channel
18	MIC2P	Audio chip LIN2 channel
19	GND	Grounded
20	GND	Grounded
21	LINEINR	Audio chip RIN2 channel
22	LINEINL	Audio chip LIN2 channel
23	NC	NC, suspended handling
24	SPORN	Audio chip ROUT1 channel
25	NC	NC, suspended handling
26	SPOLN	Audio chip LOUT1 channel
27	HPOUTL	Audio chip LOUT2 channel
28	HPOUTR	Audio chip ROUT2 channel
29	IO5	GPIO5, HS1_DATA6, VSPICS0, EMAC_RX_CLK
30	IO18	GPIO18, HS1_DATA7, VSPICLK
31	IO23	GPIO23, HS1_STROBE, VSPID
32	IO19	GPIO19, VSPIQ, U0CTS, EMAC_TXD0
33	IO22	GPIO22, VSPIWP, U0RTS, EMAC_TXD1
34	IO21	GPIO21, VSPIHD, EMAC_TX_EN
35	EN	Enable the chip, high level is effective.

36	TXD0	GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2
37	RXD0	GPIO3, U0RXD, CLK_OUT2
38	GND	Grounded

List 9 Module startup mode description

System startup mode			
PIN	Default	SPI boot mode	Download start mode
GPIO 0	pull up	1	0
GPIO 2	drop down	Irrelevant	0

Note: Some pins have been internally pulled up, please refer to the schematic

5. Schematic diagram

5.1. Module schematic

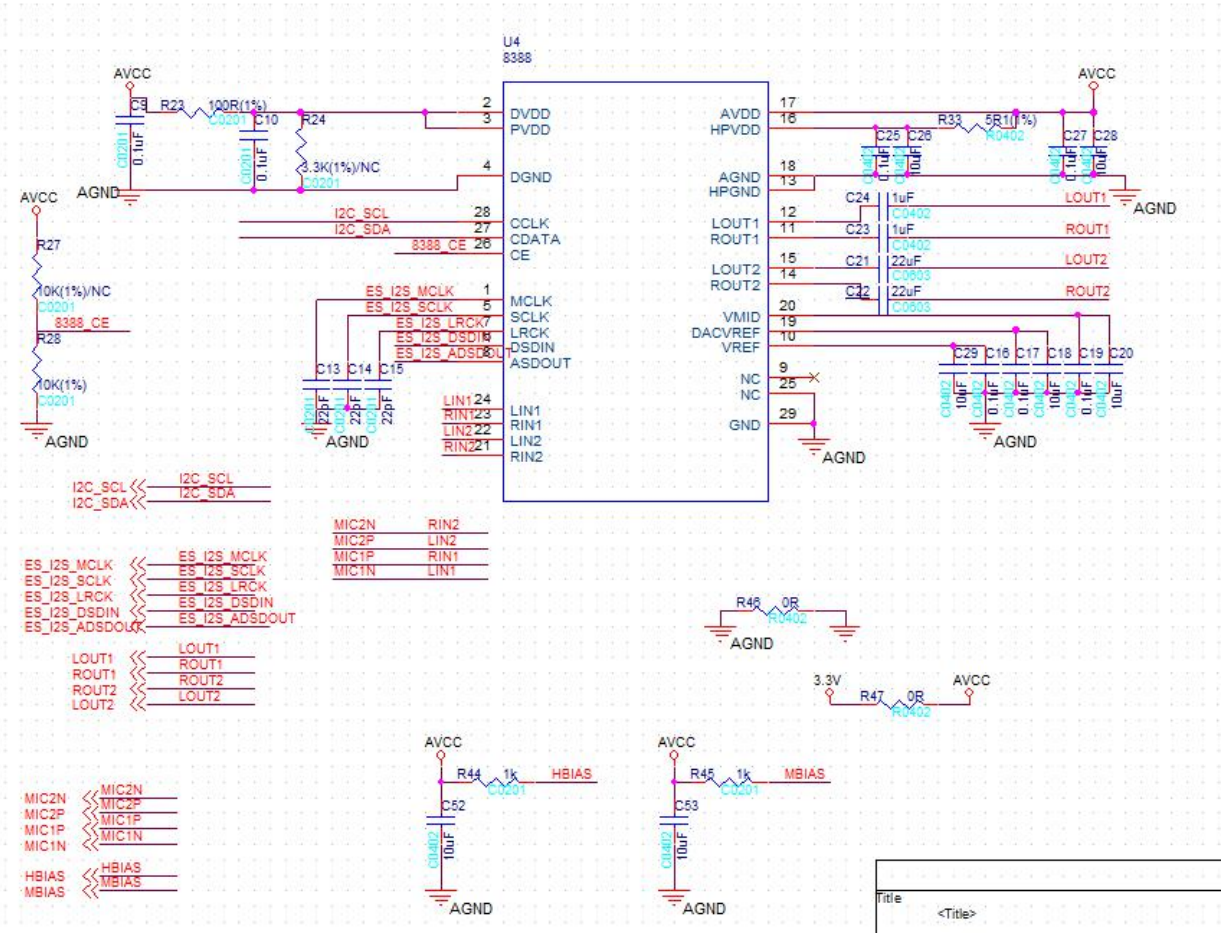

Figure 6 Audio part schematic

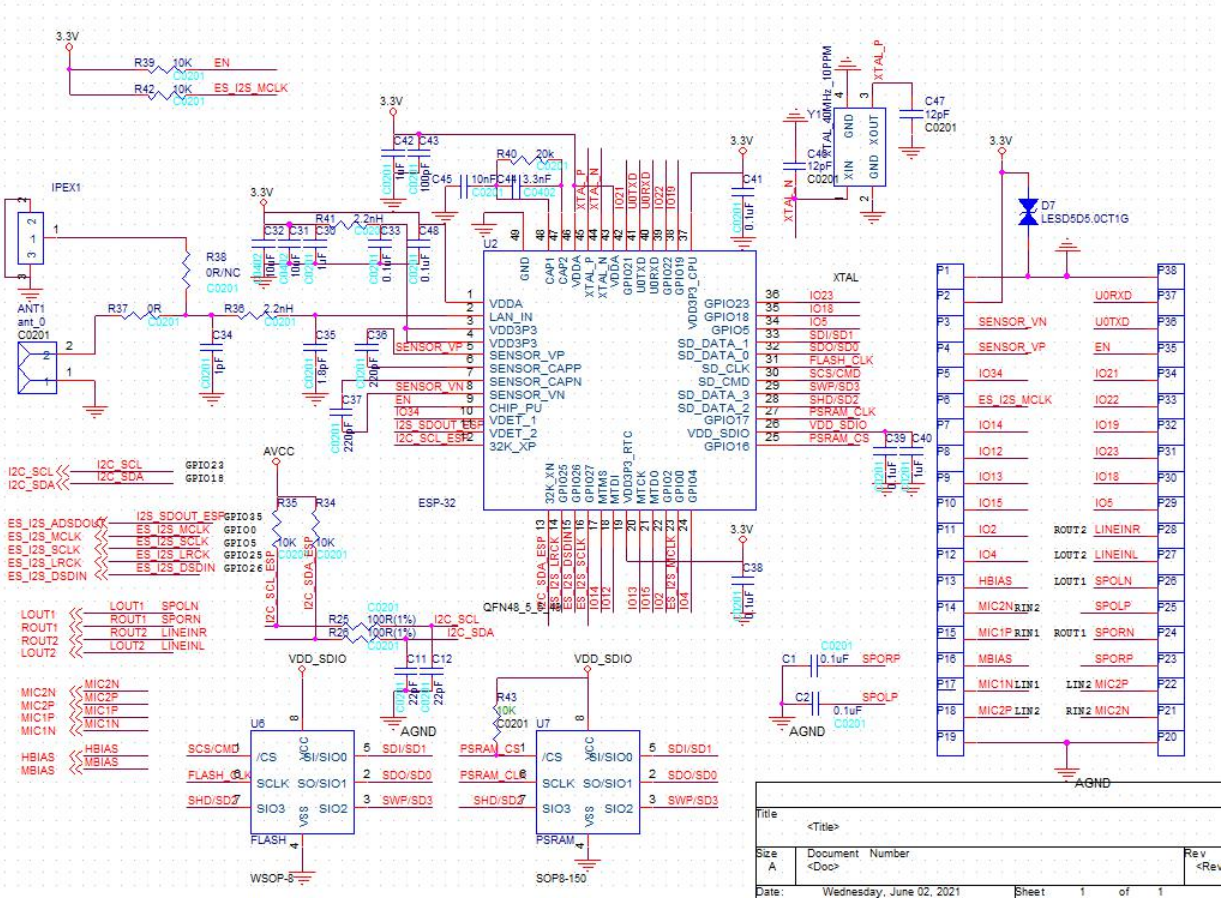

Figure 7 Schematic diagram of the main chip

5.2. Application circuit diagram

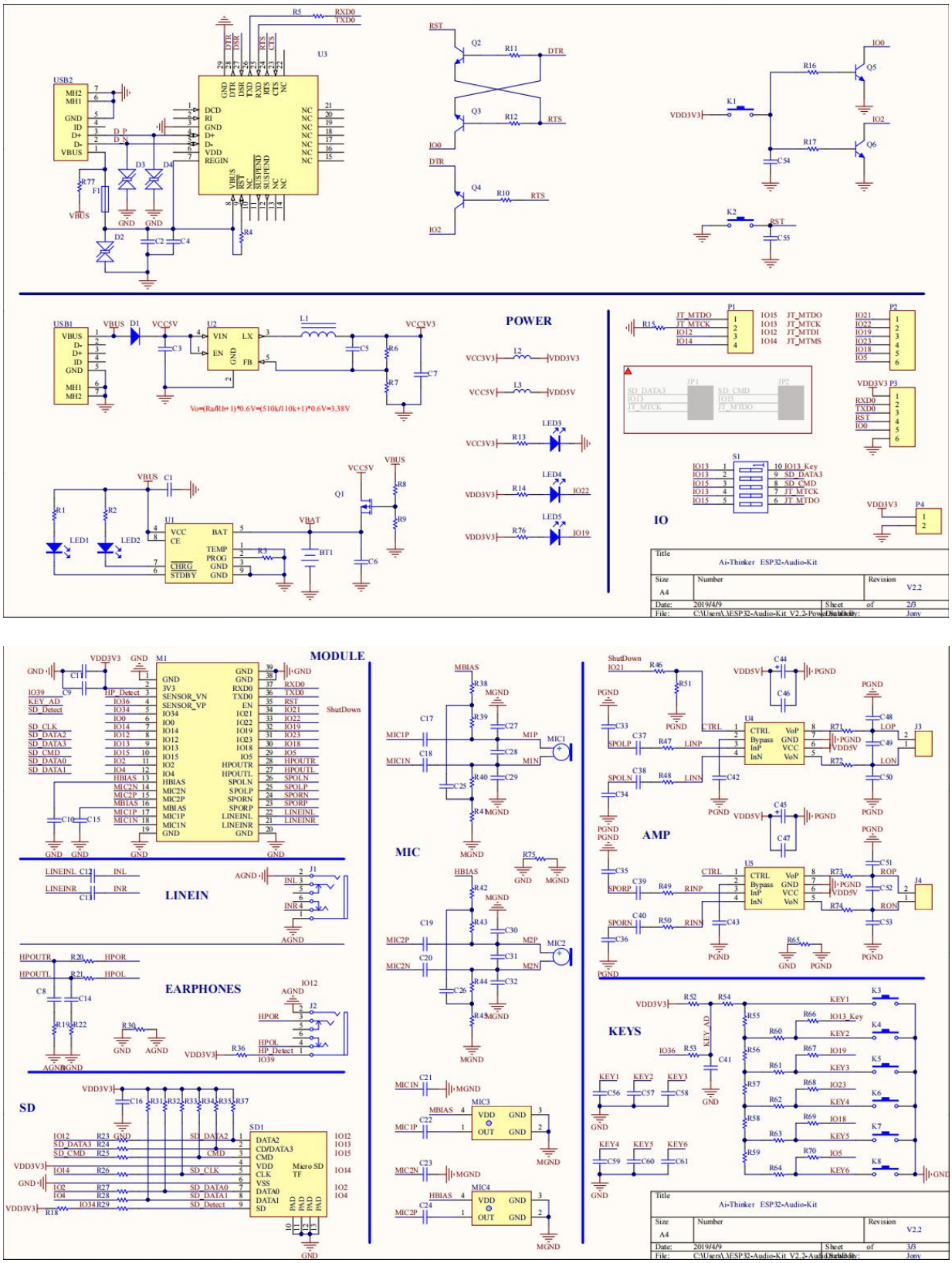

Figure 8 Application circuit diagram

6. Design guide

6.1. Antenna layout requirements

（1）、For the installation position on the motherboard, the following two methods are recommended：
Solution 1: Put the module on the edge of the main board, and the antenna area extends out of the edge of the main board.
Solution 2: Put the module on the edge of the motherboard, and hollow out an area at the antenna position on the edge of the motherboard.
（2）、In order to meet the performance of the on-board antenna, it is forbidden to place metal parts around the antenna, away from high-frequency components.

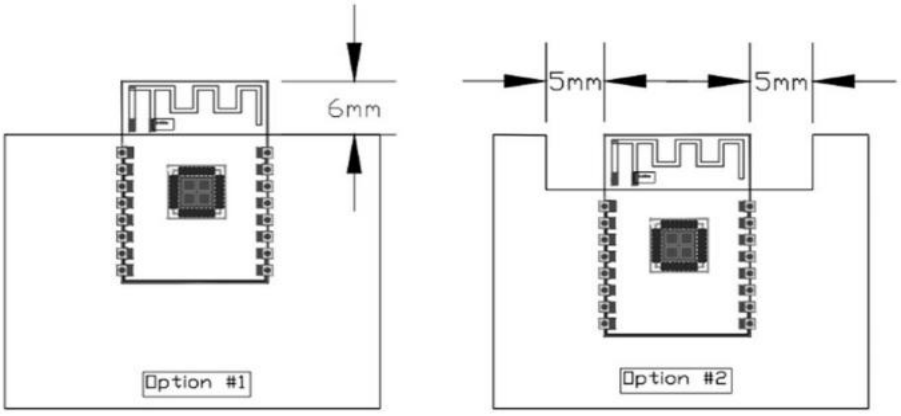

Figure 9　Schematic diagram of antenna layout

6.2. Power supply

（1）、Recommend 3.3V voltage, peak current above 500mA
（2）、It is recommended to use LDO for power supply; if DC-DC is used, the ripple is recommended to be controlled within 30mV.
（3）、It is recommended to reserve the position of the dynamic response capacitor for the DC-DC power supply circuit to optimize the output ripple when the load changes greatly.
（4）、It is recommended to add ESD devices to the 3.3V power interface.

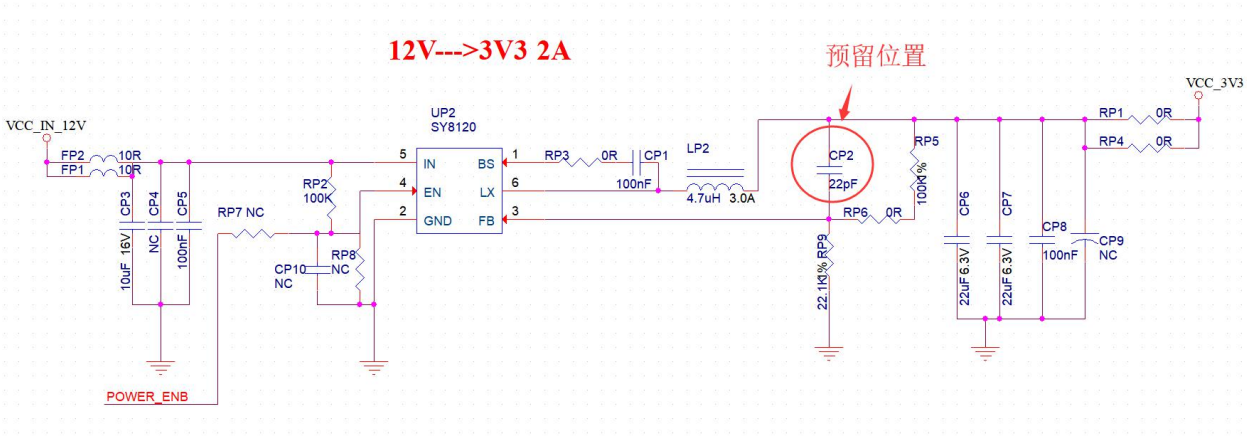

Figure 10 DC-DC Step-down circuit diagram

6.3. Use of GPIO port

（1）、There are some GPIO ports on the periphery of the module. If you need to use it, it is recommended to connect a 10-100 ohm resistor in series with the IO port. This can suppress overshoot and make the levels on both sides more stable. It is helpful for EMI and ESD.

（2）、For the pull-up and pull-down of special IO ports, please refer to the instructions in the specification, which will affect the startup configuration of the module.

（3）、The IO port of the module is 3.3V. If the main control and the IO level of the module do not match, a level conversion circuit needs to be added.

（4）、If the IO port is directly connected to a peripheral interface or terminal such as a header, it is recommended to reserve an ESD device near the terminal on the IO trace.

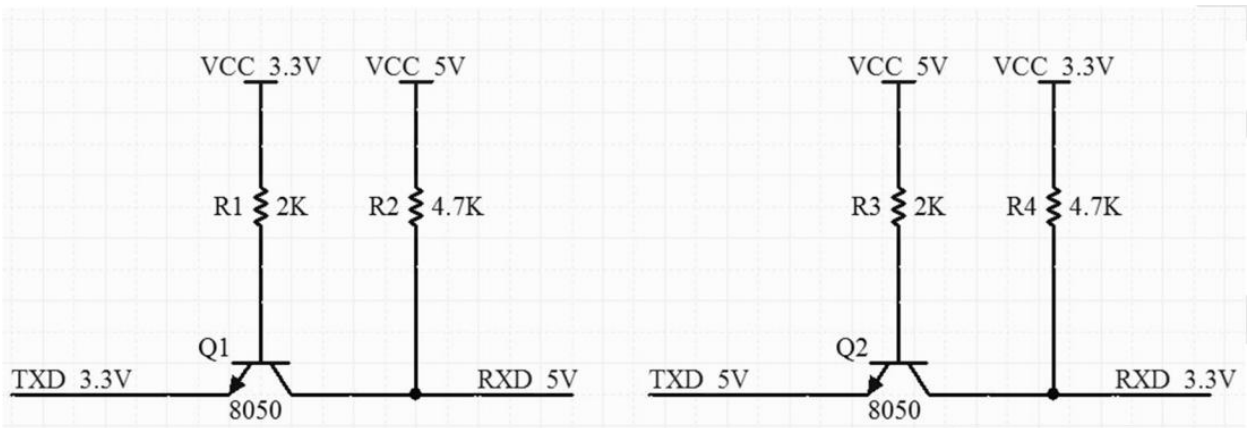

Figure 11 Level conversion circuit

7. Reflow solder curve

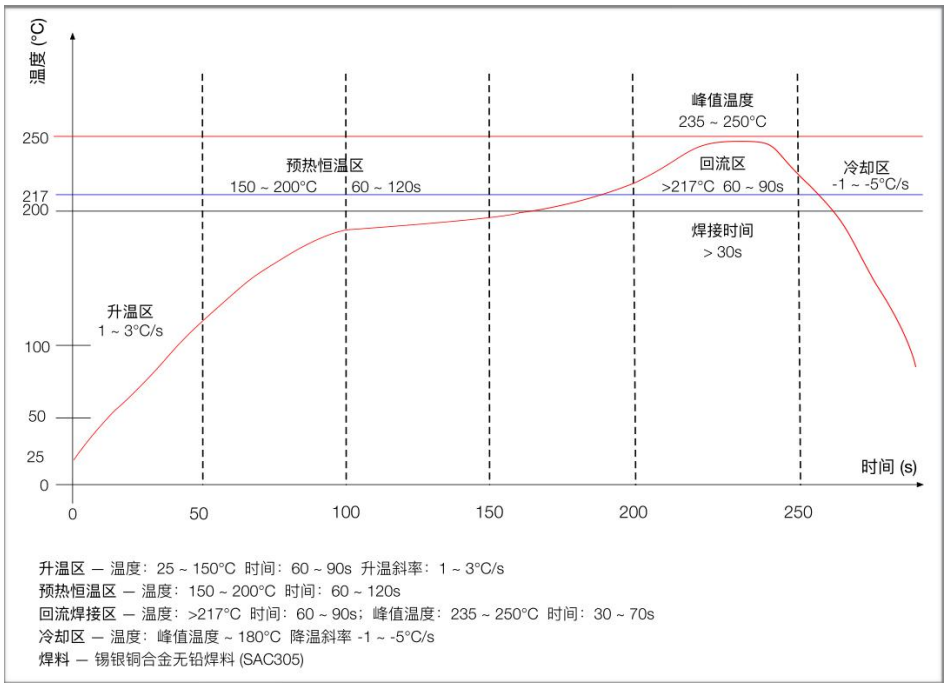

Figure 12 Reflow solder curve

8. Packaging

As shown in the figure below, the packaging of ESP32-A1S is braid.

Figure 13　tape package