

## Stereo CODEC with 1W Stereo Class D Speaker Drivers and Headphone Drivers for Portable Audio Applications

### DESCRIPTION

The WM8960 is a low power, high quality stereo codec designed for portable digital audio applications.

Stereo class D speaker drivers provide 1W per channel into 8Ω loads with a 5V supply. Low leakage, excellent PSRR and pop/click suppression mechanisms also allow direct battery connection to the speaker supply. Flexible speaker boost settings allow speaker output power to be maximised while minimising other analogue supply currents.

A highly flexible input configuration for up to three stereo sources is integrated, with a complete microphone interface. External component requirements are drastically reduced as no separate microphone, speaker or headphone amplifiers are required. Advanced on-chip digital signal processing performs automatic level control for the microphone or line input.

Stereo 24-bit sigma-delta ADCs and DACs are used with low power over-sampling digital interpolation and decimation filters and a flexible digital audio interface.

The master clock can be input directly or generated internally by an onboard PLL, supporting most commonly-used clocking schemes.

The WM8960 operates at analogue supply voltages down to 2.7V, although the digital supplies can operate at voltages down to 1.71V to save power. The speaker supply can operate at up to 5.5V, providing 1W per channel into 8Ω loads. Unused functions can be disabled using software control to save power.

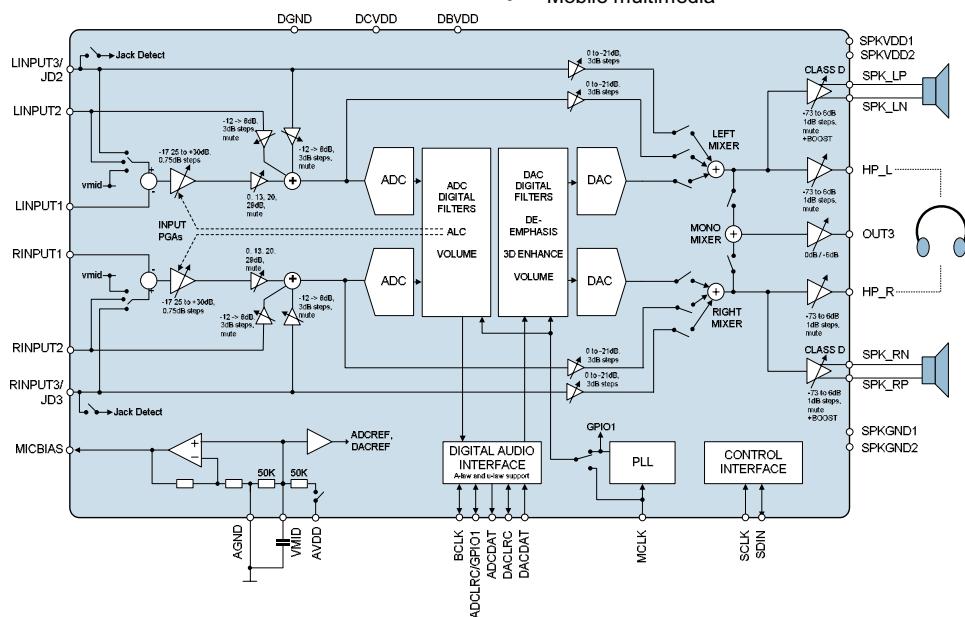
The WM8960 is supplied in a very small and thin 5x5mm QFN package, ideal for use in hand-held and portable systems.

### FEATURES

- DAC SNR 98dB ('A' weighted), THD -84dB at 48kHz, 3.3V
- ADC SNR 94dB ('A' weighted), THD -82dB at 48kHz, 3.3V
- Pop and click suppression
- 3D Enhancement
- Stereo Class D Speaker Driver
  - <0.1% THD with 1W per channel into 8Ω BTL speakers
  - 70dB PSRR @217Hz
  - 87% efficiency (1W output)
  - Flexible internal switching clock
- On-chip Headphone Driver
  - 40mW output power into 16Ω at 3.3V
  - Capless mode support
  - THD -75dB at 20mW, SNR 90dB with 16Ω load
- Microphone Interface
  - Pseudo differential for high noise immunity
  - Integrated low noise MICBIAS
  - Programmable ALC / Limiter & Noise Gate
- Low Power Consumption
  - 10mW headphone playback (2.7V / 1.8V supplies)
  - 20mW record and playback (2.7V / 1.8V supplies)
- Low Supply Voltages
  - Analogue 2.7V to 3.6V (Speaker supply up to 5.5V)
  - Digital core and I/O: 1.71V to 3.6V
- On-chip PLL provides flexible clocking scheme
- Sample rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48
- 5x5x0.9mm QFN package

### APPLICATIONS

- Games consoles
- Portable media / DVD players
- Mobile multimedia



## 用于便携式音频应用的带1W立体声D类扬声器驱动器和耳机驱动器的立体声编解码器

### 描述

WM8960是一款低功耗、高质量的立体声编解码器，专为便携式数字音频应用而设计。

立体声D类扬声器驱动器在5V电源下可向8Ω负载提供每通道1W的功率。低漏电、出色的电源抑制比（PSRR）以及爆音/咔嗒声抑制机制也允许直接将电池连接到扬声器电源。灵活的扬声器增强设置可以在最大化扬声器输出功率的同时，最小化其他模拟电源电流。

集成了高度灵活的输入配置，支持多达三个立体声源，并带有完整的麦克风接口。

由于不需要单独的麦克风、扬声器或耳机放大器，外部组件需求大幅减少。先进的片上数字信号处理技术可对麦克风或线路输入进行自动电平控制。

采用立体声24位Σ-Δ ADC和DAC，配备低功耗过采样数字插值和抽取滤波器，以及灵活的数字音频接口。

主时钟可以直接输入，也可以通过板载PLL内部生成，支持大多数常用的时钟方案。

WM8960的模拟电源电压可低至2.7V，而数字电源电压可低至1.71V以节省功耗。扬声器电源电压最高可达5.5V，可在8Ω负载下提供每通道1W的功率。未使用的功能可以通过软件控制禁用以节省功耗。

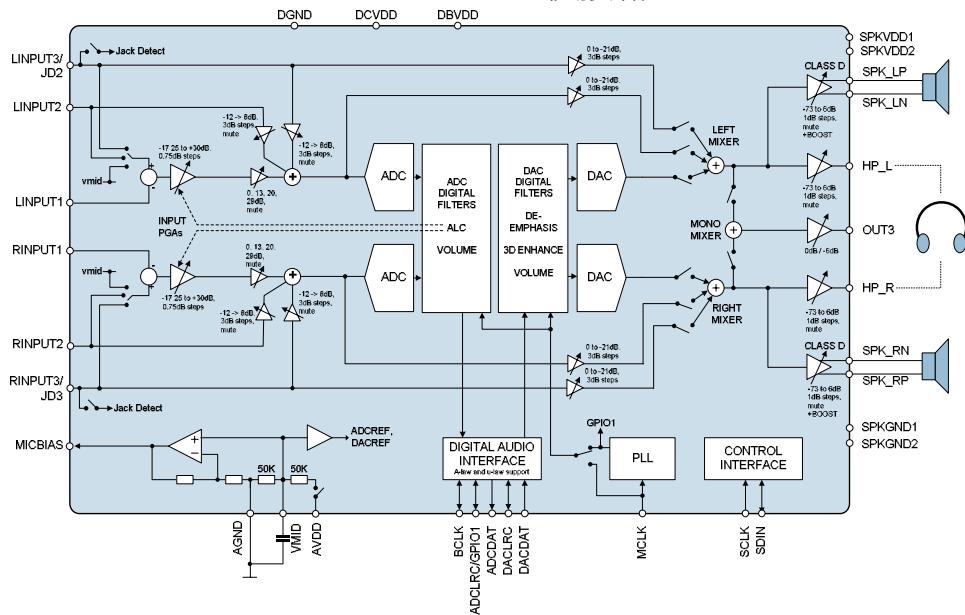
WM8960采用非常小巧的5x5mm QFN封装，非常适合用于手持和便携式系统。

### 特性

- DAC信噪比98dB（A'加权），总谐波失真-84dB，48kHz，3.3V
- ADC信噪比94dB（A'加权），总谐波失真-82dB，48kHz，3.3V
- 爆音和咔嗒声抑制
- 3D增强
- 立体声D类扬声器驱动器
  - <0.1%总谐波失真，每通道1W输出至8ΩBTL扬声器
  - 70dB电源抑制比@217Hz
  - 87%效率（1W输出）
  - 灵活的内部切换时钟
- 片上耳机驱动器
  - 40mW输出功率至16Ω，3.3V
  - 无电容模式支持
  - 总谐波失真-75dB，20mW，信噪比90dB，16Ω负载
- 麦克风接口
  - 伪差分以提高抗噪能力
  - 集成低噪声麦克风偏置
  - 可编程ALC/限幅器与噪声门
- 低功耗
  - 10mW 耳机播放（2.7V / 1.8V 供电）
  - 20mW 录音和播放（2.7V / 1.8V 供电）
- 低供电电压
  - 模拟 2.7V 至 3.6V（扬声器供电最高 5.5V）
  - 数字核心和 I/O：1.71V 至 3.6V
- 片上 PLL 提供灵活的时钟方案
- 采样率：8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48
- 5x5x0.9mm QFN 封装

### 应用

- 游戏机
- 便携式媒体 / DVD 播放器
- 移动多媒体

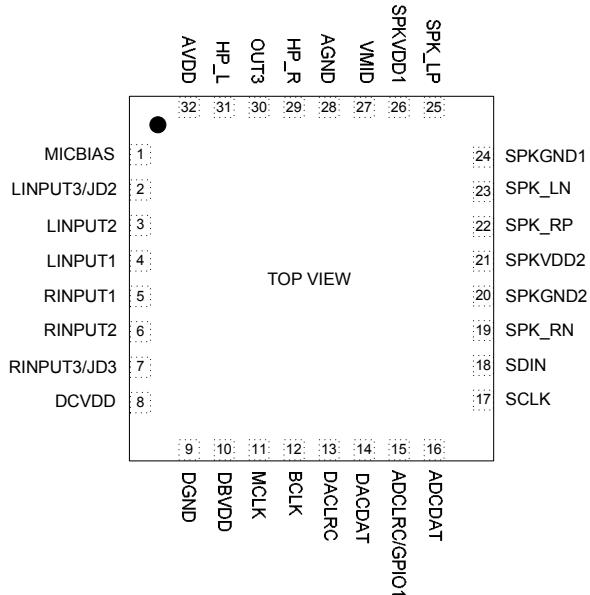


**TABLE OF CONTENTS**

<b>DESCRIPTION .....</b>	<b>1</b>
<b>FEATURES.....</b>	<b>1</b>
<b>APPLICATIONS .....</b>	<b>1</b>
<b>TABLE OF CONTENTS .....</b>	<b>2</b>
<b>PIN CONFIGURATION.....</b>	<b>3</b>
<b>ORDERING INFORMATION .....</b>	<b>3</b>
<b>PIN DESCRIPTION .....</b>	<b>4</b>
<b>ABSOLUTE MAXIMUM RATINGS.....</b>	<b>5</b>
<b>RECOMMENDED OPERATING CONDITIONS .....</b>	<b>5</b>
<b>ELECTRICAL CHARACTERISTICS .....</b>	<b>6</b>
<b>OUTPUT PGA GAIN.....</b>	<b>10</b>
<b>TYPICAL POWER CONSUMPTION .....</b>	<b>11</b>
<b>SIGNAL TIMING REQUIREMENTS .....</b>	<b>12</b>
SYSTEM CLOCK TIMING.....	12
AUDIO INTERFACE TIMING – MASTER MODE .....	12
AUDIO INTERFACE TIMING – SLAVE MODE .....	13
CONTROL INTERFACE TIMING – 2-WIRE MODE .....	14
<b>INTERNAL POWER ON RESET CIRCUIT .....</b>	<b>15</b>
<b>DEVICE DESCRIPTION.....</b>	<b>17</b>
INTRODUCTION.....	17
INPUT SIGNAL PATH.....	18
ANALOGUE TO DIGITAL CONVERTER (ADC) .....	25
AUTOMATIC LEVEL CONTROL (ALC) .....	27
OUTPUT SIGNAL PATH.....	30
ANALOGUE OUTPUTS .....	36
ENABLING THE OUTPUTS .....	40
HEADPHONE OUTPUT .....	40
CLASS D SPEAKER OUTPUTS .....	41
VOLUME UPDATES .....	42
HEADPHONE JACK DETECT .....	44
THERMAL SHUTDOWN .....	45
GENERAL PURPOSE INPUT/OUTPUT .....	46
DIGITAL AUDIO INTERFACE .....	47
AUDIO INTERFACE CONTROL .....	51
CLOCKING AND SAMPLE RATES .....	55
CONTROL INTERFACE .....	62
POWER MANAGEMENT .....	62
<b>REGISTER MAP.....</b>	<b>66</b>
REGISTER BITS BY ADDRESS .....	67
<b>DIGITAL FILTER CHARACTERISTICS .....</b>	<b>81</b>
ADC FILTER RESPONSES .....	81
DAC FILTER RESPONSES .....	82
DE-EMPHASIS FILTER RESPONSES .....	83
<b>APPLICATIONS INFORMATION .....</b>	<b>84</b>
RECOMMENDED EXTERNAL COMPONENTS.....	84
<b>IMPORTANT NOTICE .....</b>	<b>88</b>
ADDRESS:.....	88

## 目录

<b>描述</b>	1
<b>特性</b>	1
<b>应用</b>	1
<b>目录</b>	2
引脚配置	3
订购信息	3
引脚描述	4
绝对最大额定值	5
推荐工作条件	5
电气特性	6
输出PGA增益	10
典型功耗	11
<b>信号时序要求</b>	12
系统时钟时序	12
音频接口时序 – 主模式	12
音频接口时序 – 从模式	13
控制接口时序 – 2线模式	14
<b>内部上电复位电路</b>	15
<b>设备描述</b>	17
介绍	17
输入信号路径	18
模数转换器 (ADC)	25
自动电平控制 (ALC)	27
输出信号路径	30
模拟输出	36
启用输出	40
耳机输出	40
D类扬声器输出	41
音量更新	42
耳机插孔检测	44
热关机	45
通用输入/输出	46
数字音频接口	47
音频接口控制	51
时钟和采样率	55
控制接口	62
电源管理	62
<b>寄存器映射</b>	66
按地址的寄存器位	67
<b>数字滤波器特性</b>	81
ADC滤波器响应	81
DAC滤波器响应	82
去加重滤波器响应	83
<b>应用信息</b>	84
推荐外部组件	84
<b>重要通知</b>	88
地址：	88

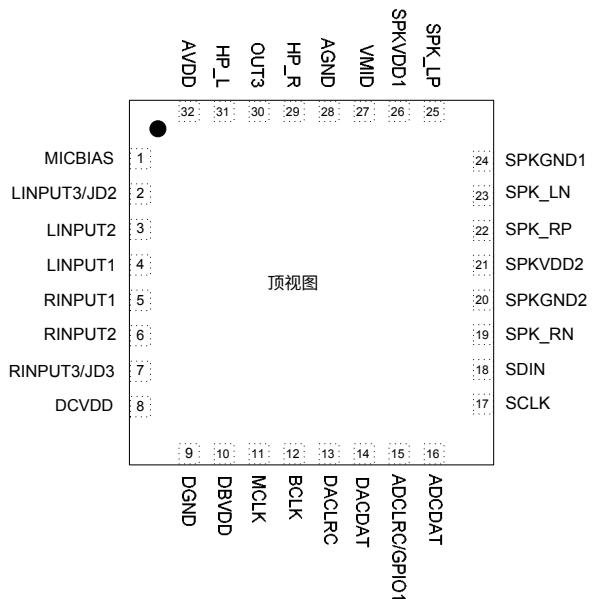
**PIN CONFIGURATION****ORDERING INFORMATION**

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8960GEFL/V	-40°C to +85°C	32-pin QFN (5x5x0.9mm) (Pb-free)	MSL3	260°C
WM8960GEFL/RV	-40°C to +85°C	32-pin QFN (5x5x0.9mm) (Pb-free, Tape and reel)	MSL3	260°C

**Note:**

Reel quantity = 3500

## 引脚配置



## 订购信息

订购代码	温度范围	封装	湿度敏感等级	峰值焊接温度
WM8960GEFL/V	-40°C 至 +85°C	32引脚QFN (5x5x0.9mm) (无铅)	MSL3	260°C
WM8960GEFL/RV	-40°C 至 +85°C	32引脚QFN封装 (5x5x0.9mm) (无铅, 卷带包装)	MSL3	260°C

注意：

每卷数量 = 3500

**PIN DESCRIPTION**

PIN NO	NAME	TYPE	DESCRIPTION
1	MICBIAS	Analogue Output	Microphone bias
2	LINPUT3 / JD2	Analogue Input	Left channel line input / Left channel positive differential MIC input / Jack detect input pin
3	LINPUT2	Analogue Input	Left channel line input / Left channel positive differential MIC input
4	LINPUT1	Analogue Input	Left channel single-ended MIC input / Left channel negative differential MIC input
5	RINPUT1	Analogue Input	Right channel single-ended MIC input / Right channel negative differential MIC input
6	RINPUT2	Analogue Input	Right channel line input / Right channel positive differential MIC input
7	RINPUT3 / JD3	Analogue Input	Right channel line input / Right channel positive differential MIC input / Jack detect input pin
8	DCVDD	Supply	Digital core supply
9	DGND	Supply	Digital ground (Return path for both DCVDD and DBVDD)
10	DBVDD	Supply	Digital buffer (I/O) supply
11	MCLK	Digital Input	Master clock
12	BCLK	Digital Input / Output	Audio interface bit clock
13	DACLRC	Digital Input / Output	Audio interface DAC left / right clock
14	DACDAT	Digital Input	DAC digital audio data
15	ADCLRC / GPIO1	Digital Input / Output	Audio interface ADC left / right clock / GPIO1 pin
16	ADCDAT	Digital Output	ADC digital audio data
17	SCLK	Digital Input	Control interface clock input
18	SDIN	Digital Input/Output	Control interface data input / 2-wire acknowledge output
19	SPK_RN	Analogue Output	Right speaker negative output
20	SPKGND2	Supply	Ground for speaker drivers 2
21	SPKVDD2	Supply	Supply for speaker drivers 2
22	SPK_RP	Analogue Output	Right speaker positive output
23	SPK_LN	Analogue Output	Left speaker negative output
24	SPKGND1	Supply	Ground for speaker drivers 1
25	SPK_LP	Analogue Output	Left speaker positive output
26	SPKVDD1	Supply	Supply for speaker drivers 1
27	VMID	Analogue Output	Midrail voltage decoupling capacitor
28	AGND	Supply	Analogue ground (Return path for AVDD)
29	HP_R	Analogue Output	Right output (Line or headphone)
30	OUT3	Analogue Output	Mono, left, right or buffered midrail output for capless mode
31	HP_L	Analogue Output	Left output (Line or headphone)
32	AVDD	Supply	Analogue supply
33	GND_PADDLE		Die Paddle (Note 1)

**Note:**

1. It is recommended that the QFN ground paddle should be connected to analogue ground on the application PCB.
2. Refer to the application note WAN\_0118 on "Guidelines on How to Use QFN Packages and Create Associated PCB Footprints"

## 引脚描述

引脚编号	名称	类型	描述
1	MICBIAS	模拟输出	麦克风偏置
2	LINPUT3 / JD2	模拟输入	左声道线路输入 / 左声道正差分麦克风输入 / 插孔检测输入引脚
3	LINPUT2	模拟输入	左声道线路输入 / 左声道正差分麦克风输入
4	LINPUT1	模拟输入	左声道单端麦克风输入 / 左声道负差分麦克风输入
5	RINPUT1	模拟输入	右声道单端麦克风输入 / 右声道负差分麦克风输入
6	RINPUT2	模拟输入	右声道线路输入 / 右声道正差分麦克风输入
7	RINPUT3 / JD3	模拟输入	右声道线路输入 / 右声道正差分麦克风输入 / 插孔检测输入引脚
8	DCVDD	电源	数字核心电源
9	DGND	电源	数字地 (DCVDD 和 DBVDD 的返回路径)
10	DBVDD	电源	数字缓冲器 (I/O) 电源
11	MCLK	数字输入	主时钟
12	BCLK	数字输入 / 输出	音频接口位时钟
13	DACLRC	数字输入 / 输出	音频接口 DAC 左 / 右时钟
14	DACDAT	数字输入	DAC 数字音频数据
15	ADCLRC / GPIO1	数字输入 / 输出	音频接口 ADC 左 / 右时钟 / GPIO1 引脚
16	ADCDAT	数字输出	ADC 数字音频数据
17	SCLK	数字输入	控制接口时钟输入
18	SDIN	数字输入 / 输出	控制接口数据输入 / 2 线确认输出
19	SPK_RN	模拟输出	右扬声器负输出
20	SPKGND2	电源	扬声器驱动器 2 的地
21	SPKVDD2	电源	扬声器驱动器 2 的电源
22	SPK_RP	模拟输出	右扬声器正输出
23	SPK_LN	模拟输出	左扬声器负输出
24	SPKGND1	电源	扬声器驱动器 1 的地
25	SPK_LP	模拟输出	左扬声器正输出
26	SPKVDD1	电源	扬声器驱动器 1 的电源
27	VMID	模拟输出	中轨电压去耦电容
28	AGND	电源	模拟地 (AVDD 的返回路径)
29	HP_R	模拟输出	右声道输出 (线路或耳机)
30	OUT3	模拟输出	单声道、左声道、右声道或缓冲中轨输出 (适用于无电容模式)
31	HP_L	模拟输出	左声道输出 (线路或耳机)
32	AVDD	电源	模拟电源
33	GND_PADDLE		芯片焊盘 (注1)

### 注意：

1. 建议将QFN接地焊盘连接到应用PCB的模拟地。
2. 请参考应用笔记WAN\_0118《如何使用QFN封装并创建相关PCB焊盘布局的指南》

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (excluding SPKVDD1 and SPKVDD2)	-0.3V	+4.5V
SPKVDD1, SPKVDD2	-0.3V	+7V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T <sub>A</sub>	-40°C	+85°C
Storage temperature after soldering	-65°C	+150°C

### Notes

- Analogue, digital and speaker grounds must always be within 0.3V of each other.
- All digital and analogue supplies are completely independent from each other (i.e. not internally connected).
- DCVDD must be less than or equal to AVDD and DBVDD.
- AVDD must be less than or equal to SPKVDD1 and SPKVDD2.
- SPKVDD1 and SPKVDD2 must be high enough to support the peak output voltage when using DCGAIN and ACGAIN functions, to avoid output waveform clipping. Peak output voltage is AVDD\*(DCGAIN+ACGAIN)/2.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	1.71		3.6	V
Digital supply range (Buffer)	DBVDD	1.71		3.6	V
Analogue supplies range	AVDD	2.7		3.6	V
Speaker supply range	SPKVDD1, SPKVDD2	2.7		5.5	V
Ground	DGND, AGND, SPKGND1, SPKGND2		0		V

## 绝对最大额定值

绝对最大额定值仅为应力额定值。持续在或超过这些极限条件下操作可能会导致设备永久性损坏。设备的功能操作极限和保证性能规格在电气特性中给出，并在指定的测试条件下进行。



静电敏感设备。该设备采用CMOS工艺制造，因此通常容易受到过高静电电压的损害。在操作和存储该设备时，必须采取适当的静电防护措施。

Wolfson根据IPC/JEDEC J-STD-020B标准对其封装类型进行湿度敏感性测试，以确定表面贴装组装前的可接受存储条件。这些等级为：

MSL1 = 在<30°C / 85%相对湿度下，无限期存储。通常不存储在防潮袋中。

MSL2 = 在<30°C / 60%相对湿度下，袋外存储1年。提供防潮袋包装。

MSL3 = 在<30°C / 60%相对湿度下，袋外存储168小时。提供防潮袋包装。

各封装类型的湿度敏感等级参数详见订购信息章节。

条件	最小值	最大值
供电电压（SPKVDD1和SPKVDD2除外）	-0.3V	+4.5V
SPKVDD1、SPKVDD2	-0.3V	+7V
数字输入电压范围	DGND -0.3V	DBVDD +0.3V
模拟输入电压范围	AGND -0.3V	AVDD +0.3V
工作温度范围，T <sub>A</sub>	-40°C	+85°C
焊接后存储温度	-65°C	+150°C

### 注释

1. 模拟地、数字地和扬声器地之间的电位差必须始终保持在0.3V范围内。
2. 所有数字和模拟电源均完全相互独立（即内部无连接）。
3. DCVDD必须小于或等于AVDD和DBVDD。
4. AVDD必须小于或等于SPKVDD1和SPKVDD2。
5. 当使用DCGAIN和ACGAIN功能时，SPKVDD1和SPKVDD2的电压必须足够高以支持峰值输出电压，避免输出波形削波。峰值输出电压计算公式为AVDD\*(DCGAIN+ACGAIN)/2。

## 推荐工作条件

参数	符号	最小值	典型值	最大值	单位
数字电源范围（核心）	DCVDD	1.71		3.6	伏特
数字电源范围（缓冲）	DBVDD	1.71		3.6	伏特
模拟电源范围	AVDD	2.7		3.6	伏特
扬声器电源范围	SPKVDD1、SPKVDD2	2.7		5.5	伏特
地	DGND, AGND, SPKGND1, SPKGND2		0		伏特

## ELECTRICAL CHARACTERISTICS

### Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = SPKVDD1 = SPKVDD2 = 3.3V, TA = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Analogue Inputs (LINPUT1, RINPUT1, LINPUT2, LINPUT3, RINPUT2, RINPUT3)</b>						
Full-scale Input Signal Level – note this changes in proportion to AVDD	V <sub>INFS</sub>	L/RINPUT1 Single-ended or differential MIC		1.0 0		Vrms dBV
		L/RINPUT2/3 Differential MIC		0.5 -6		Vrms dBV
		L/RINPUT2/3 Boost or bypass path		0.5 -6		Vrms dBV
		L/RINPUT3 Boost + bypass path		0.5 -6		Vrms dBV
Mic PGA equivalent input noise		0 to 20kHz, +30dB gain	150			uV
Input resistance (Note that input boost and bypass path resistances will be seen in parallel with PGA input resistance when these paths are enabled)	R <sub>INPUT1</sub>	+30dB PGA gain Differential or single-ended MIC configuration		3		kΩ
	R <sub>INPUT1</sub>	0dB PGA gain Differential or single-ended MIC configuration		49		kΩ
	R <sub>INPUT1</sub>	-17.25dB PGA gain Differential or single-ended MIC configuration		87		kΩ
	R <sub>INPUT2</sub> , R <sub>INPUT3</sub>	(Constant for all gains) Differential MIC configuration		85		kΩ
	R <sub>INPUT2</sub> , R <sub>INPUT3</sub>	Max boost gain L/RINPUT2/3 to boost		7.5		kΩ
	R <sub>INPUT2</sub> , R <sub>INPUT3</sub>	0dB boost gain L/RINPUT2/3 to boost		13		kΩ
	R <sub>INPUT2</sub> , R <sub>INPUT3</sub>	Min boost gain L/RINPUT2/3 to boost		37		kΩ
	R <sub>INPUT3</sub>	Max bypass gain L/RINPUT2/3 to bypass		20		kΩ
	R <sub>INPUT3</sub>	Min bypass gain L/RINPUT2/3 to bypass		224		kΩ
Input capacitance			10			pF
<b>MIC Programmable Gain Amplifier (PGA)</b>						
Programmable Gain Min				-17.25		dB
Programmable Gain Max				30		dB
Programmable Gain Step Size		Guaranteed monotonic		0.75		dB
Mute Attenuation		LMIC2B = 0 and RMIC2B = 0		90		dB
<b>Selectable Input Gain Boost</b>						
Gain Boost Steps		Input from PGA		0, 13, 20, 29, MUTE		dB
		Input from L/RINPUT2 or L/RINPUT3		-12, -9, -6, -3 0, 3, 6, MUTE		dB

## 电气特性

### 测试条件

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = SPKVDD1 = SPKVDD2 = 3.3V, TA = +25°C, 1千赫信号, 采样频率 = 48千赫, PGA增益 = 0分贝, 24位音频数据 (除非另有说明)。

参数	符号	测试条件	最小值	典型值	最大值	单位
<b>模拟输入接口 (LINPUT1、RINPUT1、LINPUT2、LINPUT3、RINPUT2、RINPUT3)</b>						
满量程输入信号电平 - 注意该值随AVDD成比例变化	V <sub>INFS</sub>	L/RINPUT1 单端或差分麦克风	1.0	0		Vrms dBV
		L/RINPUT2/3 差分麦克风	0	.5 -6		Vrms dBV
		L/RINPUT2/3 升压或旁路路径	0	.5 -6		Vrms dBV
		L/RINPUT3 升压+旁路路径	0	.5 -6		Vrms dBV
麦克风PGA等效输入噪声		0至20千赫 +30分贝增益		150		微伏
输入电阻 (注意 : 当启用输入升压和旁路 路径时, 其电阻会与PGA输入 电阻并联)	R <sub>INPUT1</sub>	+30dB PGA增益 差分或单端麦克风 配置		3		kΩ
	R <sub>INPUT1</sub>	0dB PGA增益 差分或单端麦克风 配置		49		kΩ
	R <sub>INPUT1</sub>	-17.25dB PGA增益 差分或单端麦克风 配置		87		kΩ
	R <sub>INPUT2</sub> , R <sub>INPUT3</sub>	(所有增益恒定) 差分麦克风 配置		85		kΩ
	R <sub>INPUT2</sub> , R <sub>INPUT3</sub>	最大升压增益 L/RINPUT2/3至升压电路		7.5		kΩ
	R <sub>INPUT2</sub> , R <sub>INPUT3</sub>	0dB升压增益 L/RINPUT2/3至升压电路		13		kΩ
	R <sub>INPUT2</sub> , R <sub>INPUT3</sub>	最小升压增益 L/RINPUT2/3至升压电路		37		kΩ
	R <sub>INPUT3</sub>	最大旁路增益 L/RINPUT2/3至旁路路径		20		kΩ
	R <sub>INPUT3</sub>	最小旁路增益 L/RINPUT2/3至旁路路径		224		kΩ
输入电容				10		pF
<b>麦克风可编程增益放大器 (PGA)</b>						
可编程增益最小值				-17.25		分贝
可编程增益最大值				30		分贝
可编程增益步长		保证单调性		0.75		分贝
静音衰减		LMIC2B = 0 且 RMIC2B = 0		90		分贝
<b>可选输入增益提升</b>						
增益提升步进		来自PGA的输入		0, 13, 20, 29、静音控制		分贝
		来自L/RINPUT2或 L/RINPUT3的输入		-12, -9, -6, -3 0, 3, 6, 静音控制		分贝

**Test Conditions**

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = SPKVDD1 = SPKVDD2 = 3.3V, TA = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Analogue Inputs (LINPUT2, RINPUT2, LINPUT3, RINPUT3) to ADC out</b>						
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 3.3V	94			dB
		AVDD = 2.7V	93			
Total Harmonic Distortion Plus Noise	THD+N	-3dBFS input, AVDD = 3.3V	-86			dB %
		-3dBFS input, AVDD = 2.7V	0.005	-80		
Total Harmonic Distortion	THD	-3dBFS input, AVDD = 3.3V	-89			dB %
		-3dBFS input, AVDD = 2.7V	TBD			
ADC Channel Separation		1kHz full scale signal into ADC via L/RINPUT1, MIC amp (single-ended) and boost	90			dB
		1kHz full scale signal into ADC via L/RINPUT1/2, MIC amp (pseudo- differential) and boost	90			dB
		1kHz full scale signal into ADC via L/RINPUT2 and boost	90			dB
		1kHz full scale signal into ADC via L/RINPUT3 and boost	90			dB
Line Input / MIC Separation (Quiescent input to ADC via boost; Output on ADC; 1kHz on L/RINPUT3 to HP out via bypass path)		Single-ended MIC input on L/RINPUT1	90			dB
		Differential MIC input using L/RINPUT2	90			dB
Boost / Bypass Separation (Quiescent L/RINPUT3 to HP outputs via bypass)		1kHz on LINPUT2 to ADC via boost only	90			dB
		1kHz on LINPUT1 to ADC via single-ended MIC PGA & boost	90			dB
Channel Matching		1kHz signal	0.2			dB
<b>Headphone Outputs (HP_L, HP_R)</b>						
0dB Full scale output voltage			AVDD/3.3			Vrms
Mute attenuation		1kHz, full scale signal	90			dB
Channel Separation		L/RINPUT3 to headphone outputs via bypass	85			dB
<b>DAC to Line-Out (HP_L, HP_R or OUT3 with 10kΩ / 50pF load)</b>						
Signal to Noise Ratio (A-weighted)	SNR	AVDD=3.3V	99			dB
		AVDD=2.7V	98			
Total Harmonic Distortion Plus Noise	THD+N	AVDD=3.3V	-85			dB
		AVDD=2.7V	-90			
Total Harmonic Distortion	THD	AVDD=3.3V	-87			dB
		AVDD=2.7V	-92			
Channel Separation		1kHz full scale signal	110			dB

**测试条件**

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = SPKVDD1 = SPKVDD2 = 3.3V, TA = +25°C, 1千赫信号, 采样频率 = 48千赫, PGA增益 = 0分贝, 24位音频数据 (除非另有说明)。

参数	符号	测试条件	最小值	典型值	最大值	单位
<b>模拟输入接口 (LINPUT2、RINPUT2、LINPUT3、RINPUT3) 至ADC输出</b>						
信噪比 (A加权)	信噪比	AVDD = 3.3V	94			分贝
		AVDD = 2.7V	93			
总谐波失真加噪声	THD+N	输入-3dBFS, AVDD = 3.3V	-86	0.005		分贝 %
		-3dBFS输入, AVDD = 2.7V	-80			
总谐波失真	THD	输入-3dBFS, AVDD = 3.3V	-89			分贝 %
		-3dBFS输入, AVDD = 2.7V		待确定		
模数转换器通道分离度		1千赫满幅信号输入至 通过左/右输入1的模数转换器, 麦克风 放大器 (单端) 与升压 电路	90			分贝
		1千赫满幅信号通过左/右 输入1/2, 麦克风放大 器 (伪差分) 和升 压电路输入至模数转换	90			分贝
		1千赫满幅信号通过左/右 输入2和升压电路输入至 模数转换器	90			分贝
		1千赫满幅信号通过左/右 输入3和升压电路输入至 模数转换器	90			分贝
线路输入/麦克风分离度 (通过升压电路输入至模数转换器的静态输入; 模数转换器输出; 1千赫信号经左/右输入3通过旁路路径 输出至耳机接口)		L/RINPUT1上的单端麦 克风输入	90			分贝
		使用L/RINPUT2的差 分麦克风输入	90			分贝
升压/旁路分离 (静态左/右 输入3通过旁路至耳机输出)		左输入2的1千赫信号输入至模数转换器 仅通过升压电路	90			分贝
		LINPUT1上的1千赫信号至模数转换器 通过单端麦克风 <small>可编程增益放大器与升压电路</small>	90			分贝
通道匹配		1千赫信号	0.2			分贝
<b>耳机输出 (HP_L, HP_R)</b>						
0分贝满量程输出电压			AVDD/3.3			伏有效值
静音控制衰减		1千赫满幅信号	90			分贝
通道分离度		左/右输入3至耳机 通过旁路输出	85			分贝
<b>数模转换器至线路输出 (HP_L、HP_R或OUT3, 带10kΩ/50pF负载)</b>						
信噪比 (A加权)	信噪比	AVDD=3.3伏	99			分贝
		AVDD=2.7伏	98			
总谐波失真加噪声	THD+N	AVDD=3.3伏	-85			分贝
		AVDD=2.7伏	-90			
总谐波失真	THD	AVDD=3.3伏	-87			分贝
		AVDD=2.7伏	-92			
通道分离度		1千赫满幅信号	110			分贝

**Test Conditions**

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = SPKVDD1 = SPKVDD2 = 3.3V, TA = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Headphone Output (HP_L, HP_R, using capacitors unless otherwise specified)</b>						
Output Power per channel	P <sub>O</sub>	Output power is very closely correlated with THD; see below.				
Total Harmonic Distortion Plus Noise	THD+N	AVDD=2.7V, R <sub>L</sub> =32Ω P <sub>O</sub> =5mW	0.013			% dB
		AVDD=2.7V, R <sub>L</sub> =16Ω P <sub>O</sub> =5mW	0.018			
		AVDD=3.3V, R <sub>L</sub> =32Ω, P <sub>O</sub> =20mW	0.025			
		AVDD=3.3V, R <sub>L</sub> =16Ω, P <sub>O</sub> =20mW	0.032			
		AVDD=2.7V, R <sub>L</sub> =32Ω P <sub>O</sub> =5mW; Capless mode	0.013			
		AVDD=2.7V, R <sub>L</sub> =16Ω P <sub>O</sub> =5mW; Capless mode	0.018			
		AVDD=3.3V, R <sub>L</sub> =32Ω, P <sub>O</sub> =20mW; Capless mode	0.025			
		AVDD=3.3V, R <sub>L</sub> =16Ω, P <sub>O</sub> =20mW; Capless mode	0.032			
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 3.3V	92	99		dB
		AVDD = 2.7V		98		
		AVDD = 3.3V; Capless mode	92	99		
		AVDD = 2.7V; Capless mode		98		
<b>Speaker Outputs (DAC to SPK_LP, SPK_LN, SPK_RP, SPK_RN with 8Ω bridge tied load)</b>						
Output Power	P <sub>O</sub>	Output power is very closely correlated with THD; see below				
Total Harmonic Distortion Plus Noise (DAC to speaker outputs)	THD+N	P <sub>O</sub> =200mW, R <sub>L</sub> = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V	0.01			% dB
		P <sub>O</sub> =320mW, R <sub>L</sub> = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V	0.03			
		P <sub>O</sub> =500mW, R <sub>L</sub> = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=3.3V	0.011			
		P <sub>O</sub> =1W, R <sub>L</sub> = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=3.3V	0.03			

**测试条件**

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = SPKVDD1 = SPKVDD2 = 3.3V, TA = +25°C, 1千赫信号, 采样频率 = 48千赫, P GA增益 = 0分贝, 24位音频数据 (除非另有说明)。

参数	符号	测试条件	最小值	典型值	最大值	单位	
<b>耳机输出 (HP_L、HP_R, 除非另有说明, 否则使用电容器)</b>							
每通道输出功率	P <sub>O</sub>	输出功率与总谐波失真 (THD) 密切相关; 详见下文说明					
总谐波失真加噪声	THD+N	AVDD=2.7V, R <sub>L</sub> =32Ω P <sub>O</sub> =5毫瓦	0.013		-78	% 分贝	
		AVDD=2.7V, R <sub>L</sub> =16Ω P <sub>O</sub> =5毫瓦	0.018		-75		
		AVDD=3.3V, R <sub>L</sub> =32Ω, P <sub>O</sub> =20毫瓦	0.025		-72		
		AVDD=3.3V, R <sub>L</sub> =16Ω, P <sub>O</sub> =20毫瓦	0.032		-70		
		AVDD=2.7V, R <sub>L</sub> =32Ω P <sub>O</sub> =5毫瓦; 无电容模式	0.013		-78		
		AVDD=2.7V, R <sub>L</sub> =16Ω P <sub>O</sub> =5毫瓦; 无电容模式	0.018		-75		
		AVDD=3.3V, R <sub>L</sub> =32Ω, o=20毫瓦; 无电容模式	0.025		-72		
		AVDD=3.3V, R <sub>L</sub> =16Ω, o=20毫瓦; 无电容模式	0.032		-70		
信噪比 (A加权)	信噪比	AVDD = 3.3V	92	99		分贝	
		AVDD = 2.7V		98			
		AVDD = 3.3V; 无电容模式	92	99			
		AVDD = 2.7V; 无电容模式		98			
<b>扬声器输出 (DAC至SPK_LP、SPK_LN、SPK_RP、SPK_RN, 采用8Ω桥接负载)</b>							
输出功率	P <sub>O</sub>	输出功率与总谐波失真 (THD) 密切相关; 详见下文说明					
总谐波失真加噪声 (DAC至扬声器输出)	THD+N	P <sub>O</sub> =200mW, R <sub>L</sub> = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V	0	.0 -80	1	% 分贝	
		P <sub>O</sub> =320mW, R <sub>L</sub> = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V	0	.0 -72	3		
		P <sub>O</sub> =500mW, R <sub>L</sub> = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=3.3V		0.011 -79			
		P <sub>O</sub> =1瓦, R <sub>L</sub> = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=3.3V	0	.0 -71	3		

**Test Conditions**

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = SPKVDD1 = SPKVDD2 = 3.3V, TA = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total Harmonic Distortion Plus Noise (LINPUT3 and RINPUT3 to speaker outputs)	THD+N	Po =200mW, RL = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V		0.01 -80		% dB
		Po =320mW, RL = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V		0.03 -72		% dB
		Po =500mW, RL = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=3.3V		0.011 -79		% dB
		Po =1W, RL = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=3.3V		0.03 -71		% dB
Signal to Noise Ratio (A-weighted) (DAC to speaker outputs)	SNR	SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V; RL = 8Ω, ref=2.0Vrms		90		dB
		SPKVDD1=SPKVDD2 =5V; AVDD=3.3V; RL = 8Ω, ref=2.8Vrms		92		dB
Signal to Noise Ratio (A-weighted) (LINPUT3 and RINPUT3 to speaker outputs)	SNR	SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V; RL = 8Ω, ref=2.0Vrms		90		dB
		SPKVDD1=SPKVDD2 =5V; AVDD=3.3V; RL = 8Ω, ref=2.8Vrms		92		dB
Speaker Supply Leakage current	ISPKVDD	SPKVDD1=SPKVDD2 =5V; All other supplies disconnected		1		uA
		SPKVDD1=SPKVDD2 =5V; All other supplies 0V		1		uA
Power Supply Rejection Ratio (100mV ripple on SPKVDD1/SPKVDD2 @217Hz)	PSRR	DAC to speaker playback		80		dB
		L/RINPUT3 to speaker playback		80		dB
<b>Analogue Reference Levels</b>						
Midrail Reference Voltage	VMID		-3%	AVDD/2	+3%	V
Buffered Reference Voltage	VREF		-3%	AVDD/2	+3%	V
<b>Microphone Bias</b>						
Bias Voltage	VMICBIAS	3mA load current MBSEL=1	-5%	0.9×AVDD	+ 5%	V
		3mA load current MBSEL=0	-5%	0.65×AVDD	+ 5%	V
Bias Current Source	IMICBIAS				3	mA
Output Noise Voltage	Vn	1K to 20kHz		15		nV/√Hz
<b>Digital Input / Output</b>						
Input HIGH Level	V <sub>IH</sub>		0.7×DBVDD			V
Input LOW Level	V <sub>IL</sub>				0.3×DBVDD	V
Output HIGH Level	V <sub>OH</sub>	I <sub>OL</sub> =1mA	0.9×DBVDD			V
Output LOW Level	V <sub>OL</sub>	I <sub>OH</sub> =-1mA			0.1×DBVDD	V
Input capacitance				10		pF
Input leakage			-0.9		0.9	uA

**测试条件**

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = SPKVDD1 = SPKVDD2 = 3.3V, TA = +25°C, 1千赫信号, 采样频率 = 48千赫, P GA增益 = 0分贝, 24位音频数据 (除非另有说明)。

参数	符号	测试条件	最小值	典型值	最大值	单位
总谐波失真加噪声 (左输入3和右输入3至扬声器输出)	THD+N	P <sub>O</sub> =200mW, R <sub>L</sub> = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V	0	.0 -80	1	% 分贝
		P <sub>O</sub> =320mW, R <sub>L</sub> = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V	0	.0 -72	3	% 分贝
		P <sub>O</sub> =500mW, R <sub>L</sub> = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=3.3V		0.011 -79		% 分贝
		P <sub>O</sub> =1瓦, R <sub>L</sub> = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=3.3V	0	.0 -71	3	% 分贝
信噪比 (A加权) (DAC至扬声器输出)	信噪比	SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V; R <sub>L</sub> = 8Ω, 参考=2.0V有效值		90		分贝
		SPKVDD1=SPKVDD2 =5V; AVDD=3.3V; R <sub>L</sub> = 8Ω, 参考=2.8V有效值		92		分贝
信噪比 (A加权) (左输入3和右输入3至扬声器输出)	信噪比	SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V; R <sub>L</sub> = 8Ω, 参考=2.0V有效值		90		分贝
		SPKVDD1=SPKVDD2 =5V; AVDD=3.3V; R <sub>L</sub> = 8Ω, 参考=2.8V有效值		92		分贝
扬声器供电漏电流	I <sub>SPKVDD</sub>	SPKVDD1=SPKVDD2 =5V; 所有其他电源断开连接		1		微安
		SPKVDD1=SPKVDD2 =5V; 所有其他电源0V		1		微安
电源抑制比 (SPKVDD1/SPK VDD2上100mV 纹波 @217Hz)	电源抑制比	DAC至扬声器回放		80		分贝
		左/右输入3至扬声器回放		80		分贝
<b>模拟参考电平</b>						
中轨参考电压	VMID		-3%	AVDD/2	+3%	伏特
缓冲参考电压	VREF		-3%	AVDD/2	+3%	伏特
<b>麦克风偏置</b>						
偏置电压	V <sub>MICBIAS</sub>	3mA负载电流 MBSEL=1	-5%	0.9×AVDD	+ 5%	伏特
		3mA负载电流 MBSEL=0	-5%	0.65×AVDD	+ 5%	伏特
偏置电流源	I <sub>MICBIAS</sub>				3	mA
输出噪声电压	V <sub>n</sub>	1千赫至20千赫		15		nV/√Hz
<b>数字输入 / 输出</b>						
输入高电平	V <sub>IH</sub>	.7	×DBVDD			伏特
输入低电平 0	V <sub>IL</sub>	.3			×DBVDD	伏特
输出高电平	V <sub>OH</sub>	I <sub>OL</sub> =1mA	0.9×DBVDD			伏特
输出低电平	V <sub>OL</sub>	I <sub>OH</sub> =-1mA			0.1×DBVDD	伏特
输入电容				10		pF
输入漏电流			-0.9		0.9	微安

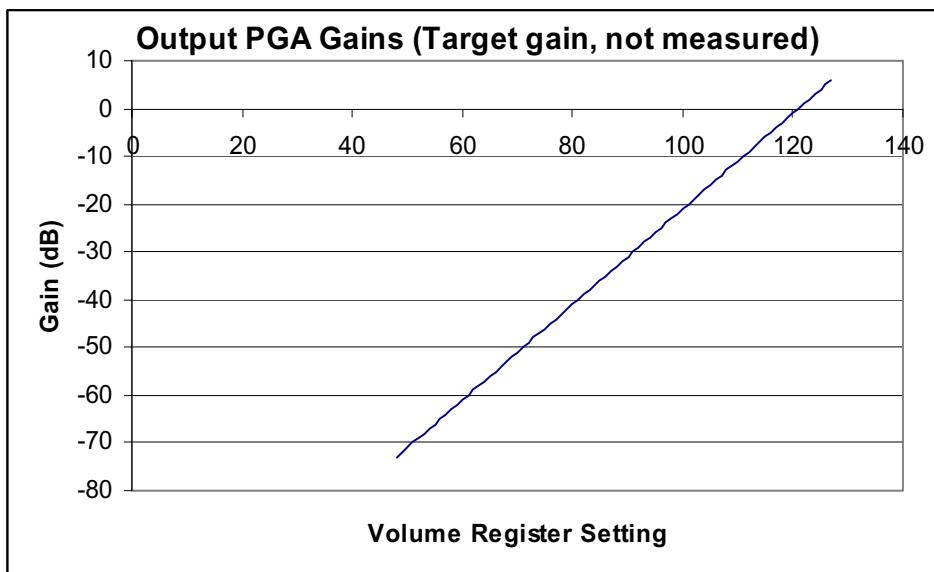
**OUTPUT PGA GAIN**

Figure 1 Output PGA Gains (LOUT1VOL, ROUT1VOL, SPKLVOL, SPKRVOL)

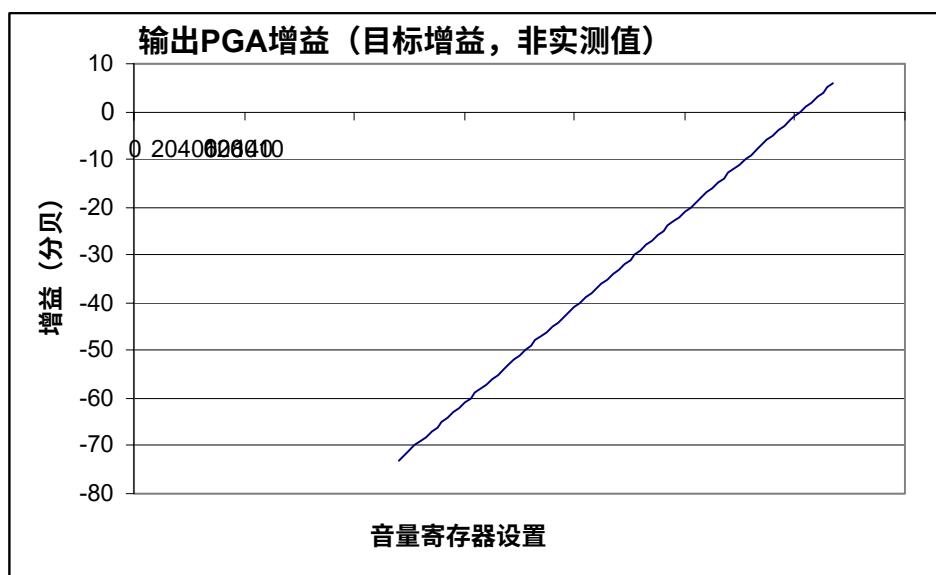
**输出PGA增益**

图1 输出PGA增益（左输出1音量，右输出1音量，左扬声器音量，右扬声器音量）

## TYPICAL POWER CONSUMPTION

Mode	AVDD (V)	SPKVDD (V)	DBVDD (V)	DCVDD (V)	I <sub>AVDD</sub> (mA)	I <sub>SPKVDD</sub> (mA)	I <sub>DBVDD</sub> (mA)	I <sub>DCVDD</sub> (mA)	Total (mW)
Off (Default state at power-up, no clocks)	2.7	2.7	1.71	1.71	0.0314	0	0	0	0.085
	3	3	1.8	1.8	0.0326	0	0	0	0.098
	3.3	3.3	3.3	1.8	0.033	0	0	0	0.109
	3.6	5.5	3.6	3.6	0.0345	0	0	0	0.124
Off (Thermal sensor disabled, no clocks)	2.7	2.7	1.71	1.71	0.0086	0	0	0	0.023
	3	3	1.8	1.8	0.0092	0	0	0	0.028
	3.3	3.3	3.3	1.8	0.0096	0	0	0	0.032
	3.6	5.5	3.6	3.6	0.0102	0	0	0	0.037
Sleep (Thermal sensor enabled, VMID enabled using 250k VMID resistors)	2.7	2.7	1.71	1.71	0.0537	0	0	0	0.145
	3	3	1.8	1.8	0.0621	0	0	0	0.186
	3.3	3.3	3.3	1.8	0.0674	0	0	0	0.222
	3.6	5.5	3.6	3.6	0.0728	0	0	0	0.262
Stereo line record @8kHz (No signal)	2.7	2.7	1.71	1.71	4.8	0	0.049	0.81	14.429
	3	3	1.8	1.8	5.1	0	0.05	0.86	16.938
	3.3	3.3	3.3	1.8	5.5	0	0.11	0.88	20.097
	3.6	5.5	3.6	3.6	5.8	0	0.11	2.2	29.196
Stereo line record @16kHz (No signal)	2.7	2.7	1.71	1.71	5.8	0	0.09	1.33	18.088
	3	3	1.8	1.8	6.2	0	0.09	1.4	21.282
	3.3	3.3	3.3	1.8	6.5	0	0.18	1.41	24.582
	3.6	5.5	3.6	3.6	6.9	0	0.2	3.6	38.520
Stereo line record @44.1kHz (No signal)	2.7	2.7	1.71	1.71	5.93	0	0.02	3.1	21.346
	3	3	1.8	1.8	6.3	0	0.02	3.3	24.876
	3.3	3.3	3.3	1.8	6.8	0	0.04	3.3	28.512
	3.6	5.5	3.6	3.6	7.1	0	0.05	8.7	57.060
Stereo line record @44.1kHz, PLL enabled, MCLK=12MHz, no signal, master mode	2.7	2.7	1.71	1.71	6.4	0	0.25	3.5	23.693
	3	3	1.8	1.8	6.9	0	0.26	3.78	27.972
	3.3	3.3	3.3	1.8	7.5	0	0.5	3.8	33.240
	3.6	5.5	3.6	3.6	7.9	0	0.54	9.6	64.944
DAC Playback to 16Ohm headphones @44.1kHz, (no signal)	2.7	2.7	1.71	1.71	3.869	0	0.0029	3.38	16.231
	3	3	1.8	1.8	4.35	0	0.0031	3.6	19.536
	3.3	3.3	3.3	1.8	4.8	0	0.0098	3.78	22.676
	3.6	5.5	3.6	3.6	5.33	0	0.0145	9.4	53.080
DAC Playback to 16Ohm headphones @44.1kHz, (white noise 1Vrms)	2.7	2.7	1.71	1.71	19.6	0	0.003	3.6	59.081
	3	3	1.8	1.8	22.1	0	0.004	3.9	73.327
	3.3	3.3	3.3	1.8	23.8	0	0.012	3.9	85.600
	3.6	5.5	3.6	3.6	26	0	0.02	9.9	129.312
DAC Playback to 16Ohm headphones @44.1kHz, (1kHz tone 100mVrms)	2.7	2.7	1.71	1.71	7.8	0	0.003	3.5	27.050
	3	3	1.8	1.8	8.9	0	0.004	3.8	33.547
	3.3	3.3	3.3	1.8	9.6	0	0.012	3.8	38.560
	3.6	5.5	3.6	3.6	10.5	0	0.014	9.5	72.050
DAC Playback to 16Ohm headphones @44.1kHz, PLL enabled, MCLK=12MHz (no signal), master mode	2.7	2.7	1.71	1.71	4.77	0	0.23	3.7	19.599
	3	3	1.8	1.8	5.4	0	0.25	3.9	23.670
	3.3	3.3	3.3	1.8	6.04	0	0.46	3.9	28.470
	3.6	5.5	3.6	3.6	6.6	0	0.49	10.1	61.884
DAC Playback to 8Ohm speakers @44.1kHz (no signal)	2.7	2.7	1.71	1.71	5.1	1.4	0.0032	3.57	23.660
	3.3	3.3	3.3	1.8	6.3	1.79	0.01	3.84	33.642
	3.3	5	3.3	1.8	6.3	2.9	0.01	3.8	42.163
	3.3	5.5	3.3	1.8	6.9	3.2	0.0132	9.8	58.054
DAC Playback to 8Ohm speakers @44.1kHz (1kHz tone, full scale)	2.7	2.7	1.71	1.71	5.1	240	0.0032	3.57	667.880
	3.3	3.3	3.3	1.8	6.3	304	0.01	3.84	1030.935
	3.3	5	3.3	1.8	6.3	450	0.01	3.8	2277.663
	3.3	5.5	3.3	1.8	6.9	486	0.0132	9.8	2713.454
DAC Playback to 8Ohm speakers @44.1kHz (white noise, 1Vrms)	2.7	2.7	1.71	1.71	5.1	48	0.0032	3.57	149.480
	3.3	3.3	3.3	1.8	6.3	56	0.01	3.84	212.535
	3.3	5	3.3	1.8	6.3	82	0.01	3.8	437.663
	3.3	5.5	3.3	1.8	6.9	90	0.0132	9.8	535.454
DAC Playback to mono speaker @44.1kHz (1kHz tone, full scale)	2.7	2.7	1.71	1.71	3	125	0.0034	3.63	351.813
	3.3	3.3	3.3	1.8	3.77	154	0.0126	3.89	527.685
	3.3	5	3.3	1.8	3.79	229	0.0126	3.7	1164.209
	3.6	5.5	3.6	3.6	4.2	250	0.0163	9.7	1425.099
Stereo line record @8kHz and stereo DAC playback to line output (load = 10kOhm) @48kHz	2.7	2.7	1.71	1.71	8.64	0	0.009	4.5	31.038
	3	3	1.8	1.8	9.44	0	0.01	4.7	36.798
	3.3	3.3	3.3	1.8	10.24	0	0.025	4.7	42.335
	3.6	5.5	3.6	3.6	11.032	0	0.03	11.732	82.058

**Notes:**

- Power in the load is included.

## 典型功耗

工作模式	AVDD (伏)	SPKVDD (伏)	DBVDD (伏)	DCVDD (伏)	IAVDD (毫安)	ISPKVDD (毫安)	IDBVDD (毫安)	IDCVDD (毫安)	总功耗 (毫瓦)
关闭 (上电默认状态, 无时钟)	2.7	2.7	1.71	1.71	0.0314	0	0	0	0.085
	3	3	1.8	1.8	0.0326	0	0	0	0.098
	3.3	3.3	3.3	1.8	0.033	0	0	0	0.109
	3.6	5.5	3.6	3.6	0.0345	0	0	0	0.124
关闭 (热敏传感器禁用, 无时钟)	2.7	2.7	1.71	1.71	0.0086	0	0	0	0.023
	3	3	1.8	1.8	0.0092	0	0	0	0.028
	3.3	3.3	3.3	1.8	0.0096	0	0	0	0.032
	3.6	5.5	3.6	3.6	0.0102	0	0	0	0.037
睡眠 (热敏传感器启用, VMID启用 使用250k VMID电阻)	2.7	2.7	1.71	1.71	0.0537	0	0	0	0.145
	3	3	1.8	1.8	0.0621	0	0	0	0.186
	3.3	3.3	3.3	1.8	0.0674	0	0	0	0.222
	3.6	5.5	3.6	3.6	0.0728	0	0	0	0.262
立体声线路录音@8千赫 (无信号)	2.7	2.7	1.71	1.71	4.8	0	0.049	0.81	14.429
	3	3	1.8	1.8	5.1	0	0.05	0.86	16.938
	3.3	3.3	3.3	1.8	5.5	0	0.11	0.88	20.097
	3.6	5.5	3.6	3.6	5.8	.11	0.22	29.196	
立体声线路录音@16千赫 (无信号)	2.7	2.7	1.71	1.71	5.8	0	0.09	1.33	18.088
	3	3	1.8	1.8	6.2	0	0.09	1.4	21.282
	3.3	3.3	3.3	1.8	6.5	.18	0.41	24.582	
	3.6	5.5	3.6	3.6	6.9	.2	0.36	38.520	
立体声线路录音@44.1千赫 (无信号)	2.7	2.7	1.71	1.71	5.93	0	0.02	3.1	21.346
	3	3	1.8	1.8	6.3	0	0.02	3.3	24.876
	3.3	3.3	3.3	1.8	6.8	0	0.04	3.3	28.512
	3.6	5.5	3.6	3.6	7.1	0	0.05	8.7	57.060
立体声线路录音@44.1千赫, 锁相环启用, MCLK=12MHz, 无信号, 主模式	2.7	2.7	1.71	1.71	6.4	.25	0.0	3.5	23.693
	3	3	1.8	1.8	6.9	.26	0.0	3.78	27.972
	3.3	3.3	3.3	1.8	7.5	.5	0.0	3.8	33.240
	3.6	5.5	3.6	3.6	7.9	.54	0.0	9.6	64.944
DAC播放至16欧姆耳机@44.1千赫, (无信号)	2.7	2.7	1.71	1.71	3.869	0	0.0029	3.38	16.231
	3	3	1.8	1.8	4.35	0	0.0031	3.6	19.536
	3.3	3.3	3.3	1.8	4.8	0	0.0098	3.78	22.676
	3.6	5.5	3.6	3.6	5.33	0	0.0145	9.4	53.080
DAC播放至16欧姆耳机@44.1千赫 (白噪声1伏有效值)	2.7	2.7	1.71	1.71	19.6	0	0.003	3.6	59.081
	3	3	1.8	1.8	22.1	0	0.004	3.9	73.327
	3.3	3.3	3.3	1.8	23.8	0	0.012	3.9	85.600
	3.6	5.5	3.6	3.6	26	0	0.02	9.9	129.312
DAC播放至16欧姆耳机@44.1千赫 (1千赫音调10 0毫伏有效值)	2.7	2.7	1.71	1.71	7.8	0	0.003	3.5	27.050
	3	3	1.8	1.8	8.9	0	0.004	3.8	33.547
	3.3	3.3	3.3	1.8	9.6	0	0.012	3.8	38.560
	3.6	5.5	3.6	3.6	10.5	0	0.014	9.5	72.050
DAC播放至16欧姆耳机@44.1千赫, 启用锁相环, MCLK=12MHz (无信号), 主模式	2.7	2.7	1.71	1.71	4.77	.23	0.0	3.7	19.599
	3	3	1.8	1.8	5.4	.25	0.0	3.9	23.670
	3.3	3.3	3.3	1.8	6.04	0	0.46	3.9	28.470
	3.6	5.5	3.6	3.6	6.6	0	0.49	10.1	61.884
DAC播放至8欧姆扬声器@44.1千赫 (无信号)	2.7	2.7	1.71	1.71	5.1	1.4	0.0032	3.57	23.660
	3.3	3.3	3.3	1.8	6.3	1.79	0.01	3.84	33.642
	3.3	5	3.3	1.8	6.3	2.9	0.01	3.8	42.163
	3.3	5.5	3.3	1.8	6.9	3.2	0.0132	9.8	58.054
DAC播放至8欧姆扬声器@44.1千赫 (1千赫音调, 满量程)	2.7	2.7	1.71	1.71	5.1	240	0.0032	3.57	667.880
	3.3	3.3	3.3	1.8	6.3	304	0.01	3.84	1030.935
	3.3	5	3.3	1.8	6.3	450	0.01	3.8	2277.663
	3.3	5.5	3.3	1.8	6.9	486	0.0132	9.8	2713.454
DAC播放至8欧姆扬声器@44.1千赫 (白噪声, 1伏 有效值)	2.7	2.7	1.71	1.71	5.1	48	0.0032	3.57	149.480
	3.3	3.3	3.3	1.8	6.3	56	0.01	3.84	212.535
	3.3	5	3.3	1.8	6.3	82	0.01	3.8	437.663
	3.3	5.5	3.3	1.8	6.9	90	0.0132	9.8	535.454
DAC播放至单声道扬声器@44.1千赫 (1千赫音调 , 满量程)	2.7	2.7	1.71	1.71	3	125	0.0034	3.63	351.813
	3.3	3.3	3.3	1.8	3.77	154	0.0126	3.89	527.685
	3.3	5	3.3	1.8	3.79	229	0.0126	3.7	1164.209
	3.3	5.5	3.6	3.6	4.2	250	0.0163	9.7	1425.099
立体声线路录音@8千赫与立体声DAC播放 至线路输出 (负载=10千欧) @48千赫	2.7	2.7	1.71	1.71	8.64	0	0.009	4.5	31.038
	3	3	1.8	1.8	9.44	0	0.01	4.7	36.798
	3.3	3.3	3.3	1.8	10.24	0	0.025	4.7	42.335
	3.6	5.5	3.6	3.6	11.032	0	0.03	11.732	82.058

### 注释:

- 包含负载中的功耗。

## SIGNAL TIMING REQUIREMENTS

### SYSTEM CLOCK TIMING

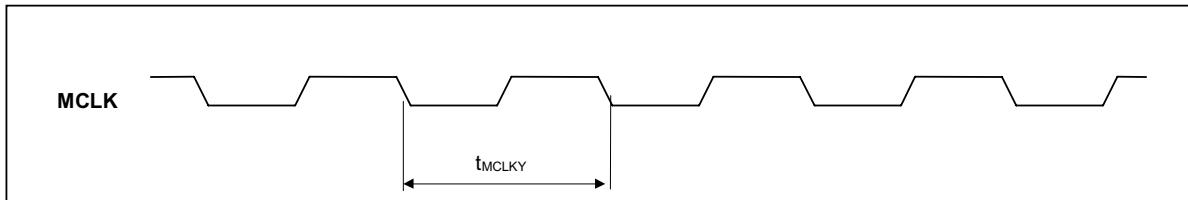


Figure 2 System Clock Timing Requirements

#### Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD1=SPKVDD2=3.3V, DGND=AGND=SPKGND1=SPKGND2=0V,  $T_A = +25^\circ\text{C}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
<b>System Clock Timing Information</b>						
MCLK cycle time	$T_{MCLKY}$		33.33			ns
MCLK duty cycle	$T_{MCLKDS}$		60:40		40:60	

### AUDIO INTERFACE TIMING – MASTER MODE

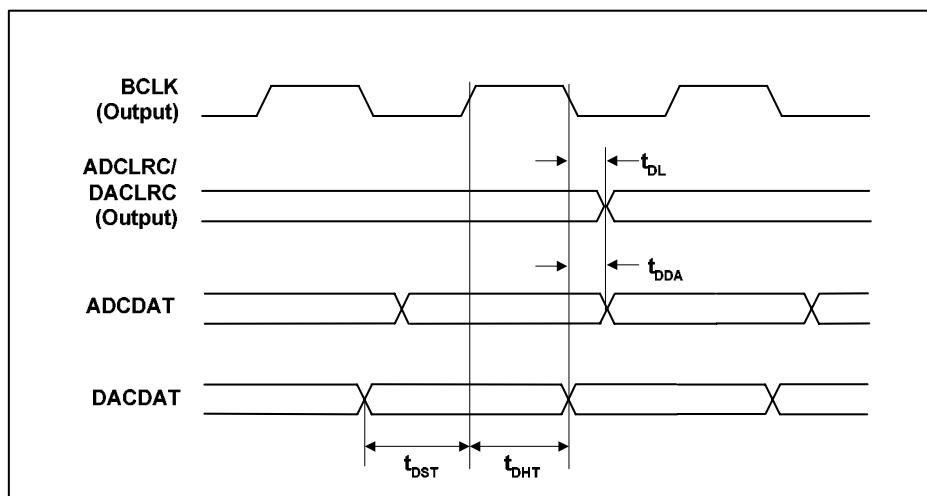


Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)

## 信号时序要求

### 系统时钟时序

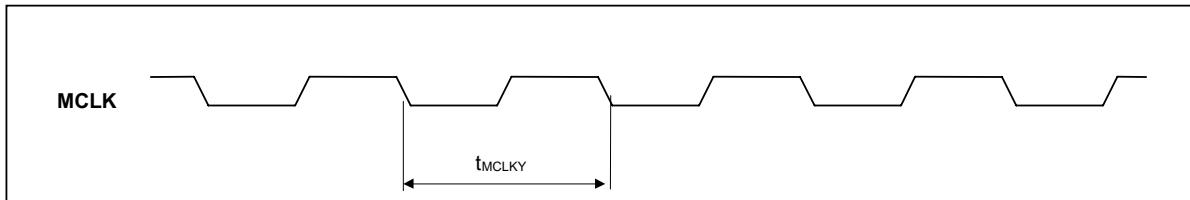


图2 系统时钟时序要求

#### 测试条件

DCVDD=1.8V, DBVDD=AVDD=SPKVDD1=SPKVDD2=3.3V, DGND=AGND=SPKGND1=SPKGND2=0V,  $T_A = +25^\circ\text{C}$

参数	符号	条件	最小值	典型值	最大值	单位
<b>系统时钟时序信息</b>						
MCLK周期时间	$T_{MCLKY}$		33.33			ns
MCLK占空比	$T_{MCLKDS}$		60:40		40:60	

### 音频接口时序 - 主模式

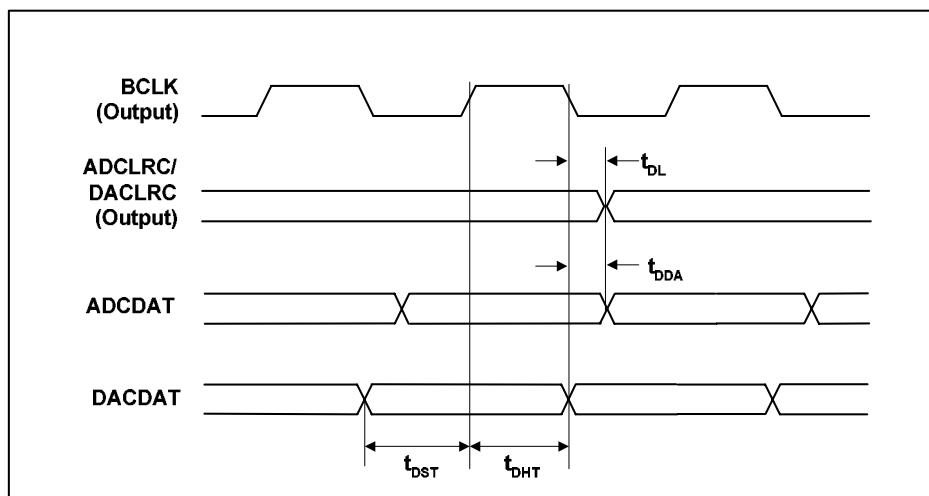


图2 数字音频数据时序 - 主模式（见控制接口）

**Test Conditions**

DCVDD=1.8V, DBVDD=AVDD=SPKVDD1=SPKVDD2=3.3V, DGND=AGND=SPKGND1=SPKGND2=0V, TA=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
<b>Audio Data Input Timing Information</b>					
ADCLRC/DACLRC propagation delay from BCLK falling edge	t <sub>DL</sub>			10	ns
ADCDAT propagation delay from BCLK falling edge	t <sub>DDA</sub>			10	ns
DACDAT setup time to BCLK rising edge	t <sub>DST</sub>	10			ns
DACDAT hold time from BCLK rising edge	t <sub>DHT</sub>	10			ns

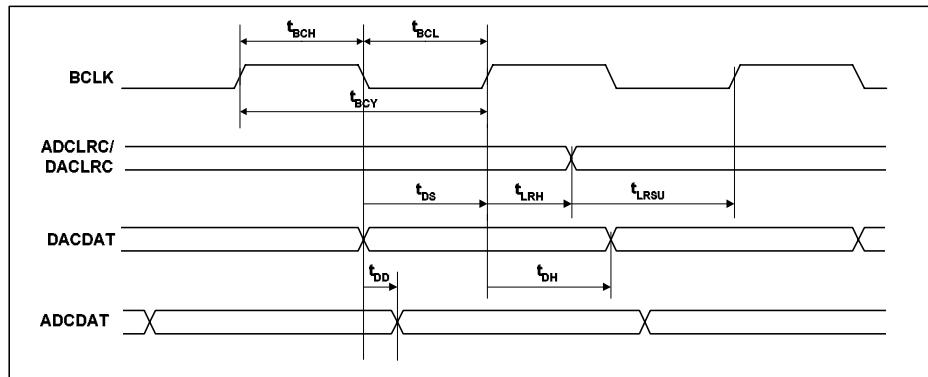
**AUDIO INTERFACE TIMING – SLAVE MODE**

Figure 3 Digital Audio Data Timing – Slave Mode

**Test Conditions**

DCVDD=1.8V, DBVDD=AVDD=SPKVDD1=SPKVDD2=3.3V, DGND=AGND=SPKGND1=SPKGND2=0V, TA=+25°C, Slave Mode, fs=48kHz, MCLK= 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
<b>Audio Data Input Timing Information</b>					
BCLK cycle time	t <sub>BCY</sub>	50			ns
BCLK pulse width high	t <sub>BCH</sub>	20			ns
BCLK pulse width low	t <sub>BCL</sub>	20			ns
ADCLRC/DACLRC set-up time to BCLK rising edge	t <sub>LRSU</sub>	10			ns
ADCLRC/DACLRC hold time from BCLK rising edge	t <sub>LRH</sub>	10			ns
DACDAT hold time from BCLK rising edge	t <sub>DH</sub>	10			ns
ADCDAT propagation delay from BCLK falling edge	t <sub>DD</sub>			10	ns
DACDAT set-up time to BCLK rising edge	t <sub>DS</sub>	10			ns

**Note:**

BCLK period should always be greater than or equal to MCLK period.

**测试条件**

DCVDD=1.8V, DBVDD=AVDD=SPKVDD1=SPKVDD2=3.3V, DGND=AGND=SPKGND1=SPKGND2=0V,  $T_A=+25^\circ\text{C}$ , 从模式,  $f_s=48\text{kHz}$ , MCLK=256fs, 24位数据, 除非另有说明。

参数	符号	最小值	典型值	最大值	单位
<b>音频数据输入时序信息</b>					
ADCLRC/DACLRC从BCLK下降沿的传播延迟	$t_{DQ}$	ns			
ADCDAT从BCLK下降沿的传播延迟	$t_{DDA0}$	ns			
DACDAT相对于BCLK上升沿的建立时间	$t_{DST}$	10 ns			
DACDAT相对于BCLK上升沿的保持时间	$t_{DHT}$	10 ns			

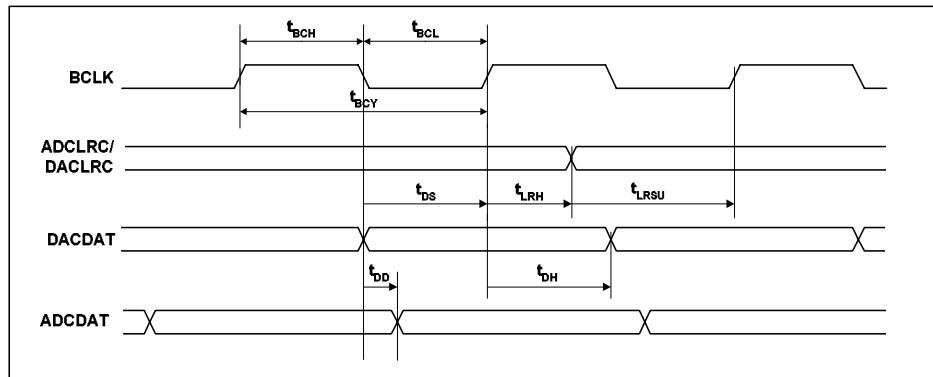
**音频接口时序 - 从模式**

图3 数字音频数据时序 - 从模式

**测试条件**

DCVDD=1.8伏, DBVDD=AVDD=SPKVDD1=SPKVDD2=3.3伏, DGND=AGND=SPKGND1=SPKGND2=0伏,  $T_A=+25$ 摄氏度, 从模式, 采样频率=48千赫, MCLK=256倍采样频率, 24位数据, 特殊说明除外。

参数	符号	最小值	典型值	最大值	单位
<b>音频数据输入时序信息</b>					
BCLK周期时间	$t_{BCY}$	50 ns			
BCLK高电平脉冲宽度	$t_{BCH}$	20 ns			
BCLK低电平脉冲宽度	$t_{BCL}$	20 ns			
ADCLRC/DACLRC相对BCLK上升沿的建立时间	$t_{LRSU}$	10 ns			
ADCLRC/DACLRC相对BCLK上升沿的保持时间	$t_{LRH}$	10 ns			
DACDAT相对于BCLK上升沿的保持时间	$t_{DH}$	10 ns			
ADCDAT从BCLK下降沿的传播延迟	$t_{DD}$	10 ns			
DACDAT相对BCLK上升沿的建立时间	$t_{DS}$	10 ns			

**注意：**

BCLK周期应始终大于或等于MCLK周期。

## CONTROL INTERFACE TIMING – 2-WIRE MODE

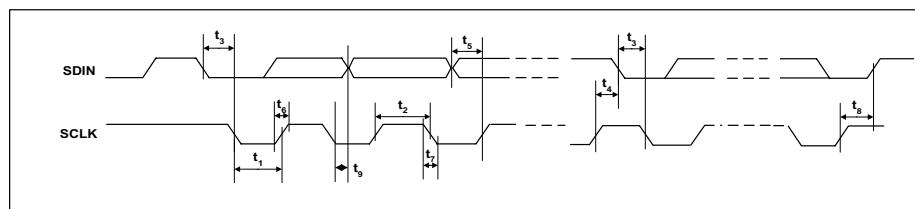


Figure 4 Control Interface Timing – 2-Wire Serial Control Mode

## Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD1=SPKVDD2=3.3V, DGND=AGND=SPKGND1=SPKGND2=0V, TA=+25°C, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
<b>Program Register Input Information</b>					
SCLK Frequency				526	kHz
SCLK Low Pulse-Width	t <sub>1</sub>	1.3			us
SCLK High Pulse-Width	t <sub>2</sub>	600			ns
Hold Time (Start Condition)	t <sub>3</sub>	600			ns
Setup Time (Start Condition)	t <sub>4</sub>	600			ns
Data Setup Time	t <sub>5</sub>	100			ns
SDIN, SCLK Rise Time	t <sub>6</sub>			300	ns
SDIN, SCLK Fall Time	t <sub>7</sub>			300	ns
Setup Time (Stop Condition)	t <sub>8</sub>	600			ns
Data Hold Time	t <sub>9</sub>			900	ns
Pulse width of spikes that will be suppressed	t <sub>ps</sub>	0		5	ns

## 控制接口时序 - 2线模式

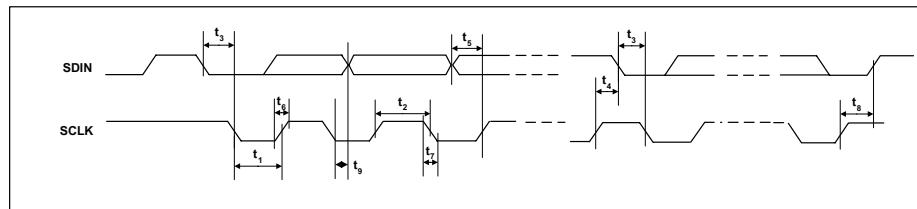


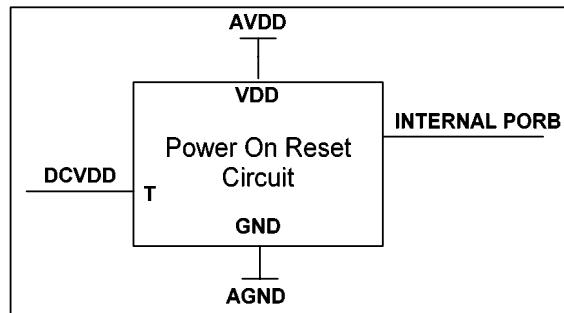
图4 控制接口时序 - 2线串行控制模式

### 测试条件

DCVDD=1.8V, DBVDD=AVDD=SPKVDD1=SPKVDD2=3.3V, DGND=AGND=SPKGND1=SPKGND2=0V, TA=+25°C, 从模式, fs=48kHz, MCLK = 256倍采样频率, 24位数据, 除非另有说明。

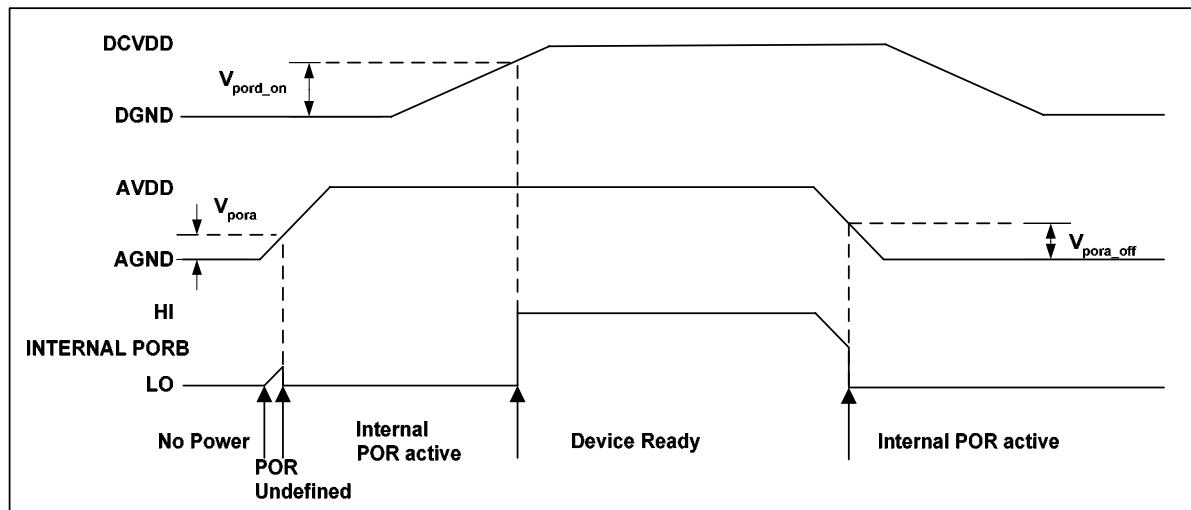
参数	符号	最小值	典型值	最大值	单位
<b>编程寄存器输入信息</b>					
SCLK时钟频率				526	千赫
SCLK低电平脉冲宽度	t <sub>1</sub>	1.3			微秒
SCLK高电平脉冲宽度	t <sub>2</sub>	60	ns		
保持时间 (起始条件)	t <sub>3</sub>	60	ns		
建立时间 (起始条件)	t <sub>4</sub>	60	ns		
数据建立时间	t <sub>5</sub>	10	ns		
SDIN、SCLK上升时间	30	t <sub>6</sub>	0	ns	
SDIN、SCLK下降时间	30	t <sub>7</sub>	0	ns	
建立时间 (停止条件)		t <sub>8</sub>	60	ns	
数据保持时间	90	t <sub>9</sub>	0	ns	
可抑制的尖峰脉冲宽度		t <sub>10</sub>	0	5	ns

## INTERNAL POWER ON RESET CIRCUIT



**Figure 5 Internal Power on Reset Circuit Schematic**

The WM8960 includes an internal Power-On-Reset Circuit, as shown in Figure 5, which is used to reset the digital logic into a default state after power up. The POR circuit is powered from AVDD and monitors DCVDD. It asserts PORB low if AVDD or DCVDD is below a minimum threshold.



**Figure 6 Typical Power up sequence where AVDD is Powered before DCVDD**

Figure 6 shows a typical power-up sequence where AVDD comes up first. When AVDD goes above the minimum threshold,  $V_{pora}$ , there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Now AVDD is at full supply level. Next DCVDD rises to  $V_{por\_on}$  and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold  $V_{pora\_off}$ .

## 内部上电复位电路

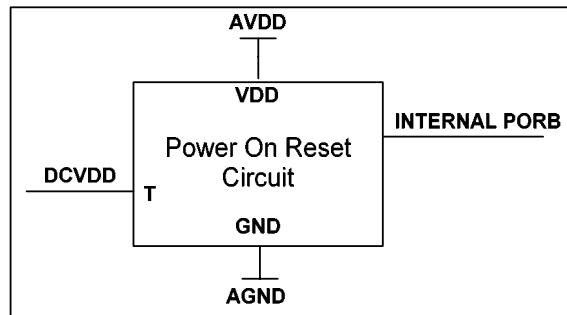


图5 内部上电复位电路原理图

WM8960集成了内部上电复位电路(如图5所示)，该电路用于在电源上电后将数字逻辑复位至默认状态。该POR电路由AVDD供电并监测DCVDD电压。当AVDD或DCVDD低于最小阈值时，会将PORB信号拉低。

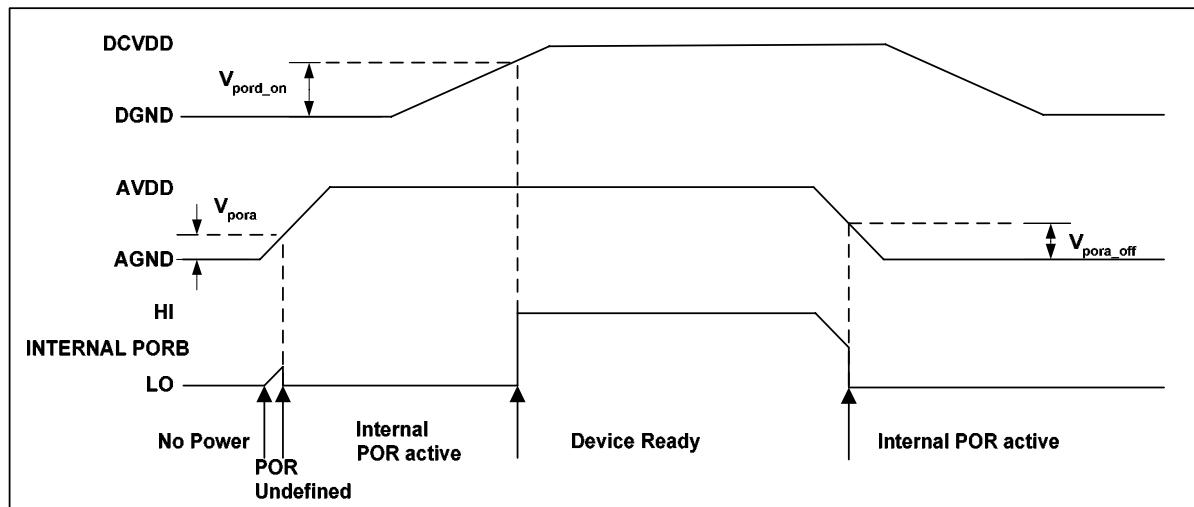
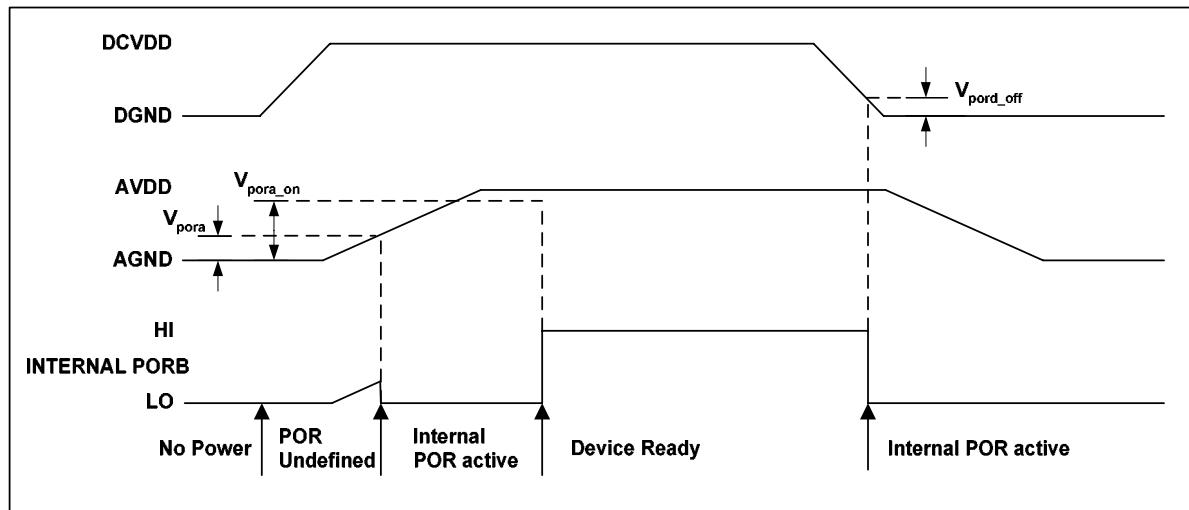


图6 AVDD先于DCVDD供电的典型上电时序

图6展示了AVDD优先上电的典型时序。当AVDD超过最小阈值 $V_{pora}$ 时，电路将确保PORB保持低电平，芯片处于复位状态。在此状态下，所有控制接口的写入操作均被忽略。当AVDD达到完整供电电平后，DCVDD继续上升至 $V_{porb\_on}$ 时PORB信号释放为高电平，此时所有寄存器恢复默认状态，控制接口的写入操作方可正常进行。

在掉电过程中，当AVDD首先下降时，每当AVDD低于最小阈值 $V_{pora\_off}$ 时，上电复位信号PORB将被拉低。



**Figure 7 Typical Power up Sequence where DCVDD is Powered before AVDD**

Figure 7 shows a typical power-up sequence where DCVDD comes up first. First it is assumed that DCVDD is already up to specified operating voltage. When AVDD goes above the minimum threshold,  $V_{\text{pora}}$ , there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD rises to  $V_{\text{pora\_on}}$ , PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DCVDD falls first, PORB is asserted low whenever DCVDD drops below the minimum threshold  $V_{\text{pord\_off}}$ .

SYMBOL	MIN	TYP	MAX	UNIT
$V_{\text{pora}}$	0.4	0.6	0.8	V
$V_{\text{pora\_on}}$	0.9	1.2	1.6	V
$V_{\text{pora\_off}}$	0.4	0.6	0.8	V
$V_{\text{pord\_on}}$	0.5	0.7	0.9	V
$V_{\text{pord\_off}}$	0.4	0.6	0.8	V

**Table 1 Typical POR Operation (typical values, not tested)**

**Notes:**

1. If AVDD and DCVDD suffer a brown-out (i.e. drop below the minimum recommended operating level but do not go below  $V_{\text{pora\_off}}$  or  $V_{\text{pord\_off}}$ ) then the chip will not reset and will resume normal operation when the voltage is back to the recommended level again.
2. The chip will enter reset at power down when AVDD or DCVDD falls below  $V_{\text{pora\_off}}$  or  $V_{\text{pord\_off}}$ . This may be important if the supply is turned on and off frequently by a power management system.
3. The minimum  $t_{\text{por}}$  period is maintained even if DCVDD and AVDD have zero rise time. This specification is guaranteed by design rather than test.

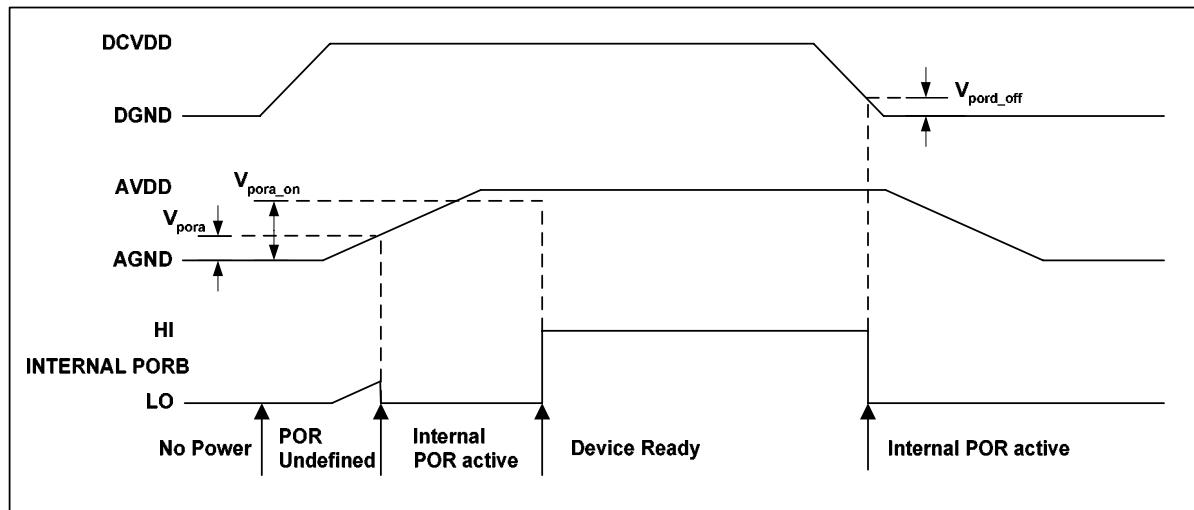


图7 典型上电时序 (DCVDD先于AVDD上电)

图7展示了典型的DCVDD先上电的时序过程。首先假设DCVDD已达到规定工作电压。当AVDD超过最小阈值 $V_{pora}$ 时，电路具备足够电压以确保上电复位信号PORB保持低电平，芯片处于复位状态。在此状态下，所有对控制接口的写入操作均被忽略。当AVDD升至 $V_{pora\_on}$ 时，PORB信号释放为高电平，所有寄存器恢复默认状态，此时可对控制接口进行写入操作。

在掉电过程中，当DCVDD首先下降时，每当DCVDD低于最小阈值 $V_{pord\_off}$ 时，上电复位信号PORB将被拉低。

符号	最小值	典型值	最大值	单位
$V_{pora}$	0.4	0.6	0.8	伏特
$V_{pora\_on}$	0.9	1.2	1.6	伏特
$V_{pora\_off}$	0.4	0.6	0.8	伏特
$V_{pord\_on}$	0.5	0.7	0.9	伏特
$V_{pord\_off}$	0.4	0.6	0.8	伏特

表1 典型上电复位操作 (典型值, 未经测试)

#### 注释：

- 若AVDD和DCVDD发生电压跌落（即电压降至最低推荐工作电平以下但未低于 $V_{pora\_off}$ 或 $V_{pord\_off}$ ），则芯片不会复位，当电压恢复至推荐电平时将恢复正常工作。
- 当AVDD或DCVDD低于 $V_{pora\_off}$ 或 $V_{pord\_off}$ 时，芯片将在断电时进入复位状态。对于需要电源管理系统频繁开关供电的场景，此特性尤为重要。
- 即使DCVDD和AVDD的上升时间为零，仍会维持最小 $t_{por}$ 周期。该规格通过设计保证而非测试验证。

## DEVICE DESCRIPTION

### INTRODUCTION

The WM8960 is a low power audio codec offering a combination of high quality audio, advanced features, low power and small size. These characteristics make it ideal for portable digital audio applications with stereo speaker and headphone outputs such as games consoles, portable media players and multimedia phones.

Stereo class D speaker drivers can provide >1W per channel into 8Ω loads. BTL configuration provides high power output and excellent PSRR. Low leakage and pop/click suppression mechanisms allow direct battery connection, reducing component count and power consumption in portable battery-powered applications. Highly flexible speaker boost settings provide fully internal level-shifting of analogue output signals, allowing speaker output power to be maximised while minimising other analogue supply currents, and requiring no additional components.

A flexible input configuration includes support for two stereo microphone interfaces (single-ended or pseudo-differential) and additional stereo line inputs. Up to three stereo analogue input sources are available, removing the need for external analogue switches in many applications. Boost amplifiers are available for additional gain on the microphone inputs and a programmable gain amplifier with a mixed signal automatic level control (ALC) keeps the recording volume constant.

The stereo ADC and DAC are of hi-fi quality using a 24-bit, low-order oversampling architecture to deliver optimum performance. A flexible clocking arrangement supports mixed ADC and DAC sample rates.

The DAC output signal can be mixed with analogue input signals from the line inputs or bypass paths. This mix is available on speaker and headphone/line outputs.

The WM8960 has a configurable digital audio interface where ADC data can be read and digital audio playback data fed to the DAC. It supports a number of audio data formats including I<sup>2</sup>S, DSP Mode (a burst mode in which frame sync plus two data packed words are transmitted), MSB-First, left justified and MSB-First, right justified, and can operate in master or slave modes. In PCM mode A-law and μ-law companding is supported.

The SYSCLK (system clock) provides clocking for the ADCs, DACs, DSP core, class D outputs and the digital audio interface. SYSCLK can be derived directly from the MCLK pin or via an integrated PLL, providing flexibility to support a wide range of clocking schemes. All MCLK frequencies typically used in portable systems are supported for sample rates between 8kHz and 48kHz. A flexible switching clock for the class D speaker drivers (synchronous with the audio DSP clocks for best performance) is also derived from SYSCLK.

To allow full software control over all its features, the WM8960 uses a 2 wire control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. Unused circuitry can be disabled via software to save power, while low leakage currents extend standby and off time in portable battery-powered applications.

## 器件描述

### 引言

WM8960是一款低功耗音频编解码器，集高音质、先进功能、低功耗和小尺寸于一体。这些特性使其成为便携式数字音频应用的理想选择，尤其适用于需要立体声扬声器和耳机输出的场景，如游戏机、便携媒体播放器和多媒体手机。

立体声D类扬声器驱动器可向 $8\Omega$ 负载提供每通道>1瓦的输出功率。BTL配置可实现高功率输出和优异的电源抑制比(PSRR)。低泄漏电流与爆破音/咔嗒声抑制机制允许直接连接电池，在便携式电池供电应用中有效减少元件数量并降低功耗。高度灵活的扬声器升压设置可对模拟输出信号进行完全内部电平转换，在最大限度提升扬声器输出功率的同时最小化其他模拟供电电流，且无需额外元件。

灵活的输入配置支持两个立体声麦克风接口（单端或伪差分）及额外立体声线路输入。最多可支持三路立体声模拟输入源，省去了许多应用中对外部模拟开关的需求。麦克风输入配备升压放大器可提供额外增益，带混合信号自动电平控制(ALC)的可编程增益放大器能保持录制音量恒定。

立体声模数转换器(ADC)和数模转换器(DAC)采用24位低阶过采样架构，提供高保真音质。灵活的时钟配置支持混合ADC和DAC采样率，可输出最佳性能表现。

数模转换器(DAC)输出信号可与来自线路输入或旁路路径的模拟输入信号进行混合。该混合信号可通过扬声器输出和耳机/线路输出接口获取。

WM8960配备可配置数字音频接口，支持读取模数转换器(ADC)数据并向DAC输送数字音频回放数据。该器件支持多种音频数据格式，包括I<sup>2</sup>S、DSP模式(一种突发传输模式，可同步传输帧信号和两个数据包字)、MSB优先左对齐、MSB优先右对齐格式，并能工作在主从模式。在PCM模式下支持A律和μ律压扩技术。

系统时钟(SYSCLK)为模数转换器、数模转换器、DSP内核、D类输出和数字音频接口提供时钟信号。SYSCLK可直接源自MCLK引脚，或通过集成锁相环(PLL)生成，这种设计可灵活支持多种时钟方案。器件支持便携式系统常用的所有MCLK频率，可覆盖8千赫至48千赫的采样率范围。D类扬声器驱动器使用的灵活可变的开关时钟(与音频DSP时钟同步以实现最佳性能)同样源自SYSCLK。

为实现所有功能的完整软件控制，WM8960采用双线控制接口。该接口与各类行业标准微处理器、控制器和数字信号处理器完全兼容，是理想的配套方案。通过软件可禁用未使用电路以节省功耗，而低漏电流特性可延长便携式电池供电应用的待机时间和关机时长。

## INPUT SIGNAL PATH

The WM8960 has three flexible stereo analogue input channels which can be configured as line inputs, differential microphone inputs or single-ended microphone inputs. Line inputs and microphone PGA outputs can be routed to the hi-fi ADCs or directly to the output mixers via a bypass path.

### MICROPHONE INPUTS

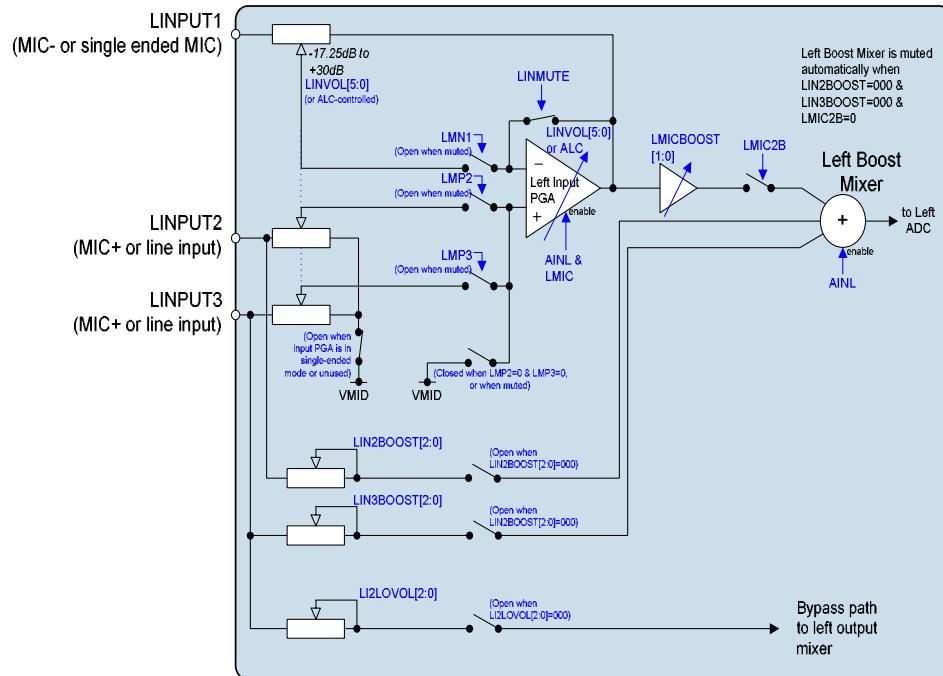
Differential microphones can be connected between LINPUT1 and LINPUT2 or LINPUT3, and between RINPUT1 and RINPUT2 or RINPUT3. Alternatively single-ended microphones can be connected to LINPUT1 or RINPUT1.

In single-ended microphone input configuration the microphone signal should be input to LINPUT1 or RINPUT1 and the internal non-inverting input of the input PGA should be switched to VMID.

In differential mode the larger signal should be input to LINPUT2 or LINPUT3 on the left channel, or RINPUT2 or RINPUT3 on the right channel. The smaller (e.g. noisy ground connection) should be input to LINPUT1 or RINPUT1.

The gain of the microphone PGAs can be controlled directly via software, or using the ALC / Limiter.

The inputs LINPUT2, RINPUT2, LINPUT3 and RINPUT3 should not be connected to the boost mixer or bypass path while operating as the non-inverting input in differential microphone configuration.



## 输入信号路径

WM8960配备三个灵活的立体声模拟输入通道，可配置为线路输入、差分麦克风输入或单端麦克风输入。线路输入和麦克风可编程增益放大器输出既可路由至高保真模数转换器，也可通过旁路路径直接输出至混音器。

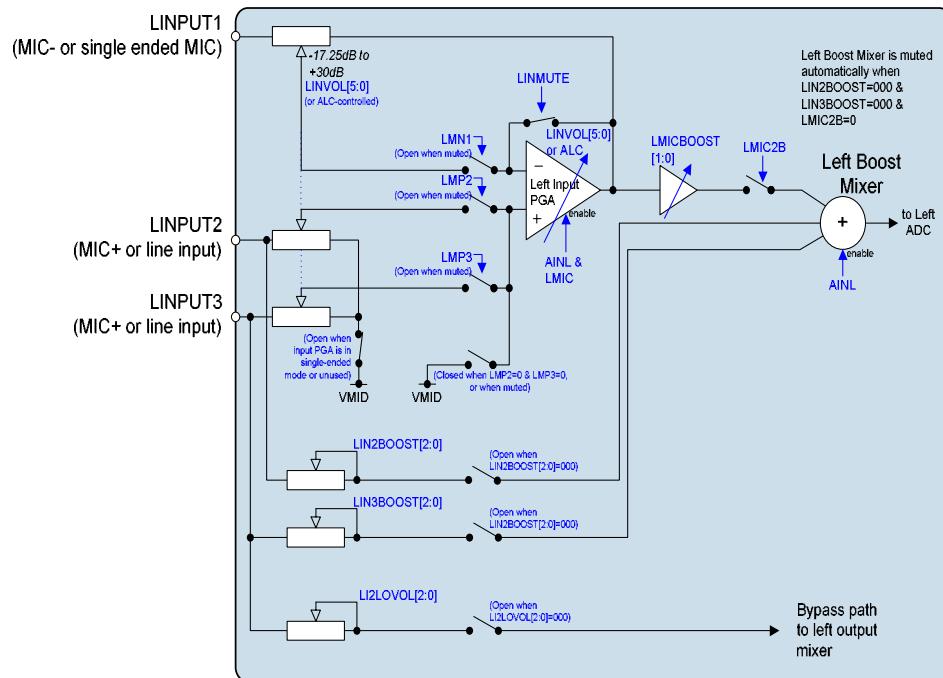
### 麦克风输入

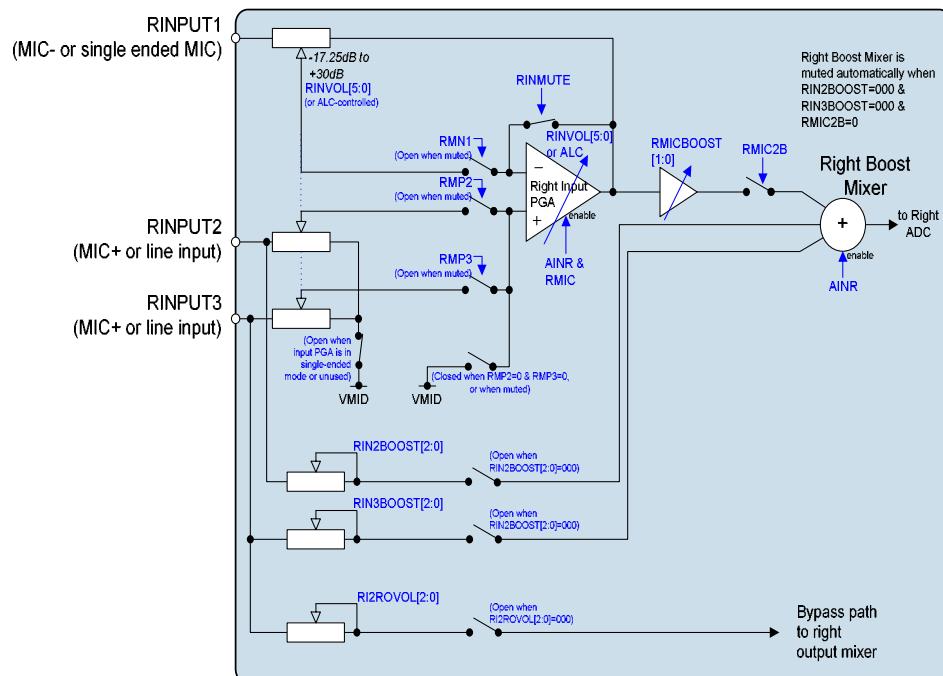
差分麦克风可连接于左通道的LINPUT1与LINPUT2/LINPUT3之间，或右通道的RINPUT1与RINPUT2/RINPUT3之间。单端麦克风亦可连接至LINPUT1或RINPUT1。

在单端麦克风输入配置中，麦克风信号应输入至LINPUT1或RINPUT1，同时需将输入可编程增益放大器的内部同相输入端切换至VMID。差分模式下，较大信号应输入左通道的LINPUT2/LINPU

T3或右通道的RINPUT2/RINPUT3，较小信号（如含噪声的地端）则应输入LINPUT1或RINPUT1。

麦克风可编程增益放大器(PGA)的增益可通过软件直接控制，或使用ALC/限幅器进行控制。当作为差分麦克风配置中的同相输入端工作时，输入信号LINPUT2、RINPUT2、LINPUT3和RINPUT3不应连接到升压混频器或旁路路径。



**Figure 8 Microphone Input PGA Circuit**

The input PGAs and boost mixers are enabled by the AINL and AINR register bits. The microphone PGAs can be also be disabled independently of the boost mixer to save power, using LMIC and RMIC register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power Management (1)	5	AINL	0	Left channel input PGA and boost stage enable 0 = PGA disabled, boost disabled 1 = PGA enabled (if LMIC = 1), boost enabled
	4	AINR	0	Right channel input PGA and boost stage enable 0 = PGA disabled, boost disabled 1 = PGA enabled (if LMIC = 1), boost enabled
R47 (2Fh) Power Management (3)	5	LMIC	0	Left channel input PGA enable 0 = PGA disabled 1 = PGA enabled (if AINL = 1)
	4	RMIC	0	Right channel input PGA enable 0 = PGA disabled 1 = PGA enabled (if AINR = 1)

**Table 2 Input PGA and Boost Enable Register Settings**

The input PGAs can be configured as differential inputs, using LINPUT1/LINPUT2 or LINPUT1/LINPUT3, and RINPUT1/RINPUT2 or RINPUT1/RINPUT3. The input impedance to these non-inverting inputs is constant in this configuration. Differential configuration is controlled by LMP2, LMP3, RMP2 and RMP3 as shown in Table 3.

When single-ended configuration is selected, the non-inverting input of the PGA is connected to VMID.

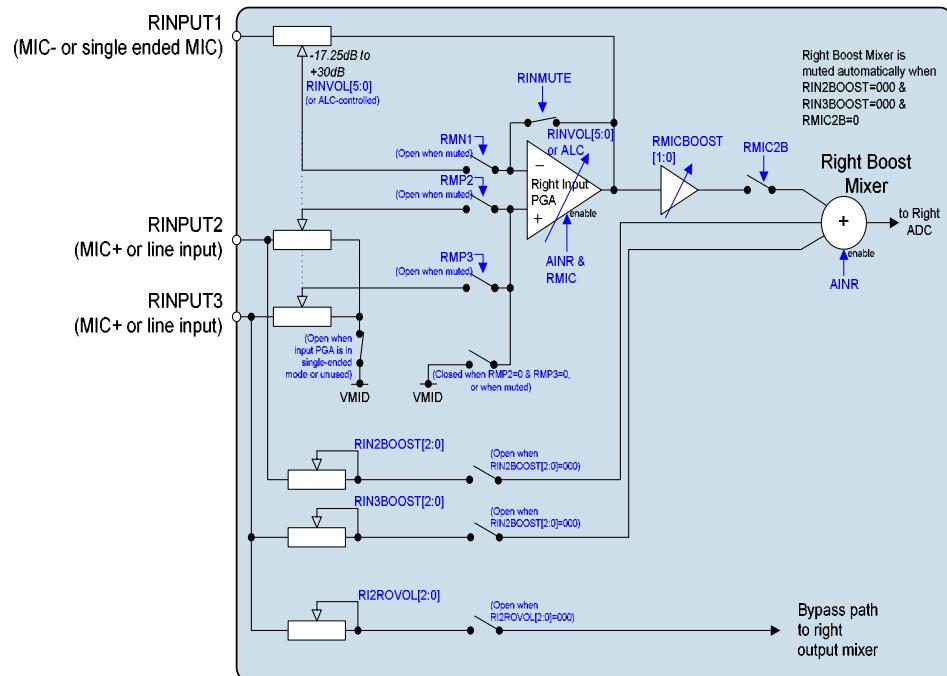


图8 麦克风输入可编程增益放大器电路

输入PGA和升压混频器通过AINL和AINR寄存器位使能。为节省功耗，也可通过LMIC和RMIC寄存器位单独禁用麦克风PGA（不影响升压混频器）。

寄存器地址	位	标签	默认值	描述
R25 (19h) 电源管理 (1)	5	AINL	0	左声道输入PGA及升压级使能 0 = PGA禁用，升压禁用 1 = PGA使能（当LMIC=1时），升压使能
	4	AINR	0	右声道输入PGA及升压级使能 0 = PGA禁用，升压禁用 1 = PGA使能（当LMIC=1时），升压使能
R47 (2Fh) 电源管理 (3)	5	左麦克风输入控制	0	左声道输入PGA使能 0 = PGA禁用 1 = 启用PGA（当AINL = 1时）
	4	右麦克风输入控制	0	右声道输入PGA使能 0 = PGA禁用 1 = 启用PGA（当AINR = 1时）

表2 输入PGA及升压使能寄存器设置

输入PGA可配置为差分输入模式，使用LINPUT1/LINPUT2或LINPUT1/LINPUT3，以及RINPUT1/RINPUT2或RINPUT1/RINPUT3。在此配置中，这些同相输入端的输入阻抗保持恒定。差分配置由LMP2、LMP3、RMP2和RMP3控制，如表3所示。

当选择单端配置时，PGA的同相输入端将连接至VMID。

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) ADCL Input Signal Path	3	LMIC2B	0	Connect Left Input PGA to Left Input Boost mixer 0 = Not connected 1 = Connected
	6	LMP2	0	Connect LINPUT2 to non-inverting input of Left Input PGA 0 = LINPUT2 not connected to PGA 1 = LINPUT2 connected to PGA (Constant input impedance)
	7	LMP3	0	Connect LINPUT3 to non-inverting input of Left Input PGA 0 = LINPUT3 not connected to PGA 1 = LINPUT3 connected to PGA (Constant input impedance)
	8	LMN1	1	Connect LINPUT1 to inverting input of Left Input PGA 0 = LINPUT1 not connected to PGA 1 = LINPUT1 connected to PGA
R33 (21h) ADCR Input Signal Path	3	RMIC2B	0	Connect Right Input PGA to Right Input Boost mixer 0 = Not connected 1 = Connected
	6	RMP2	0	Connect RINPUT2 to non-inverting input of Right Input PGA 0 = RINPUT2 not connected to PGA 1 = RINPUT2 connected to PGA (Constant input impedance)
	7	RMP3	0	Connect RINPUT3 to non-inverting input of Right Input PGA 0 = RINPUT3 not connected to PGA 1 = RINPUT3 connected to PGA (Constant input impedance)
	8	RMN1	1	Connect RINPUT1 to inverting input of Right Input PGA 0 = RINPUT1 not connected to PGA 1 = RINPUT1 connected to PGA

Table 3 Input PGA Control

### INPUT PGA VOLUME CONTROLS

The input PGAs have a gain range from -17.25dB to +30dB in 0.75dB steps. The gains from the inverting inputs (LINPUT1 and RINPUT1) to the PGA outputs and from the non-inverting inputs (LINPUT2/RINPUT2 and LINPUT3/RINPUT3) to the PGA output are always common in differential configuration and controlled by the register bits LINVOL[5:0] and RINVOL[5:0].

When the Automatic Level Control (ALC) is enabled the input PGA gains are controlled automatically and the LINVOL and RINVOL bits should not be used.

The left and right input PGAs can be independently muted using the LINMUTE and RINMUTE register bits.

To allow simultaneous volume updates of left and right channels, PGA gains are not altered until a 1 is written to the IPVU bit.

To prevent "zipper noise", a zero-cross function is provided, so that when enabled, volume updates will not take place until a zero-crossing is detected. In the event of a long period without zero-crossings, a timeout function is available. When this function is enabled (using the TOEN register bit), the volume will update automatically after a timeout. The timeout period is set by TOCLKSEL. Note that SYSCLK must be running to use this function.

寄存器地址	位	标签	默认值	描述
R32 (20h) ADCL输入 信号路径	3	左麦克风输入控制2B	0	将左输入PGA连接至左输入升压混频器 0 = 未连接 1 = 已连接
	6	左麦克风路径2	0	将LINPUT2连接至左输入PGA的同相输入端 0 = LINPUT2未连接到PGA 1 = LINPUT2连接到PGA (恒定输入阻抗)
	7	LMP3	0	将LINPUT3连接至左输入PGA的同相输入端 0 = LINPUT3未连接到PGA 1 = LINPUT3连接到PGA (恒定输入阻抗)
	8	LMN1	1	将LINPUT1连接至左输入PGA的反相输入端 0 = LINPUT1未连接到PGA 1 = LINPUT1连接到PGA
R33 (21h) ADCR 输入 信号路径	3	RMIC2B	0	将右输入PGA连接至右输入升压混频器 0 = 未连接 1 = 已连接
	6	RMP2	0	将RINPUT2连接至右输入PGA的同相输入端 0 = RINPUT2 未连接到PGA 1 = RINPUT2连接到PGA (恒定输入阻抗)
	7	RMP3	0	将RINPUT3连接至右输入PGA的同相输入端 0 = RINPUT3 未连接到PGA 1 = RINPUT3 连接至 PGA (恒定输入阻抗)
	8	RMN1	1	将 RINPUT1 连接至右输入 PGA 的反相输入端 0 = RINPUT1 未连接至 PGA 1 = RINPUT1 连接至 PGA

表3 输入PGA控制

### 输入PGA音量控制

输入可编程增益放大器(PGA)的增益范围从-17.25分贝到+30分贝，步进为0.75分贝。在差分配置中，从反相输入(LINPUT1和RINPUT1)到PGA输出端的增益，以及从同相输入(LINPUT2/RINPUT2和LINPUT3/RINPUT3)到PGA输出端的增益始终是共用的，并由寄存器位LINVOL[5:0]和RINVOL[5:0]控制。

当启用自动电平控制(ALC)时，输入PGA增益将自动控制，此时不应再使用LINVOL和RINVOL位进行调节。

左右输入端的可编程增益放大器(PGA)可通过LINMUTE和RINMUTE寄存器位实现独立静音控制。

为实现左右声道音量的同步更新，PGA增益值将在IPVU位写入1后才会生效。

为防止'拉链噪声'，芯片提供过零检测功能。当使能该功能时，音量更新操作将延迟至信号过零点执行。若长时间未检测到过零点，可通过启用超时功能(设置TOEN寄存器位)实现强制更新。超时周期由T\_OCLKSEL设定。注意：此功能需SYSCLK处于运行状态。

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Left Channel PGA	8	IPVU	N/A	Input PGA Volume Update Writing a 1 to this bit will cause left and right input PGA volumes to be updated (LINVOL and RINVOL)
	7	LINMUTE	1	Left Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IPVU must be set to un-mute.
	6	LIZC	0	Left Input PGA Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	LINVOL [5:0]	010111 ( 0dB )	Left Input PGA Volume Control 111111 = +30dB 111110 = +29.25dB .. 0.75dB steps down to 000000 = -17.25dB
R1 (01h) Right Channel PGA	8	IPVU	N/A	Input PGA Volume Update Writing a 1 to this bit will cause left and right input PGA volumes to be updated (LINVOL and RINVOL)
	7	RINMUTE	1	Right Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IPVU must be set to un-mute.
	6	RIZC	0	Right Input PGA Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	RINVOL [5:0]	010111 ( 0dB )	Right Input PGA Volume Control 111111 = +30dB 111110 = +29.25dB .. 0.75dB steps down to 000000 = -17.25dB
R23 (17h) Additional Control (1)	0	TOEN	0	Timeout Enable (Also enables jack detect debounce clock) 0 = Timeout disabled 1 = Timeout enabled
	1	TOCLKSEL	0	Slow Clock Selection (Used for volume update timeouts and for jack detect debounce) 0 = SYSCLK / $2^{21}$ (Slower Response) 1 = SYSCLK / $2^{19}$ (Faster Response)

**Table 4 Input PGA Volume Control**

See "Volume Updates" for more information on volume update bits, zero cross and timeout operation.

### LINE INPUTS

Two pairs of stereo line inputs (LINPUT2 / RINPUT2 and LINPUT3 / RINPUT3) are available as analogue inputs into the ADC path. LINPUT3 and RINPUT3 can also be input directly to the output mixers via the bypass paths.

See "Output Signal Path" for more information on the bypass paths.

寄存器地址	位	标签	默认值	描述
R0 (00h) 左声道 可编程增益放大器	8	IPVU	不适用	输入可编程增益放大器音量更新 向该位写入1将使左右输入可编程增益放大器音量更新（左输入音量和右输入音量）
	7	线路静音	1	左输入PGA模拟静音控制 1 = 启用静音 0 = 禁用静音控制 注意：必须设置IPVU以取消静音
	6	左输入零交叉检测	0	左输入可编程增益放大器零交叉检测器 1 = 仅在零交叉时改变增益 0 = 立即改变增益
	5:0	左输入音量 [5:0]	010111 (0分贝)	左输入可编程增益放大器音量控制 111111 = +30分贝 111110 = +29.25分贝 ... 以0.75分贝步进递减至 000000 = -17.25分贝
R1 (01h) 右声道 可编程增益放大器	8	IPVU	不适用	输入可编程增益放大器音量更新 向该位写入1将使左右输入可编程增益放大器音量更新（左输入音量和右输入音量）
	7	右输入静音	1	右输入可编程增益放大器模拟静音 1 = 启用静音 0 = 禁用静音控制 注意：必须设置IPVU以取消静音
	6	右输入零交叉检测	0	右输入可编程增益放大器零交叉检测器 1 = 仅在零交叉时改变增益 0 = 立即改变增益
	5:0	右输入音量 [5:0]	010111 (0分贝)	右输入可编程增益放大器音量控制 111111 = +30分贝 111110 = +29.25分贝 ... 以0.75分贝步进递减至 000000 = -17.25分贝
R23 (17h) 附加控制位 (1)	0	超时使能	0	超时功能使能（同时启用插孔检测消抖时钟）0 = 关闭超时功能 1 = 启用超时功能
	1	慢时钟选择	0	慢时钟选择（用于音量更新超时和插孔检测去抖）0 = SYSCLK / 2 <sup>21</sup> （响应较慢）1 = SYSCLK / 2 <sup>19</sup> （响应较快）

表4 输入PGA音量控制

有关音量更新位、零交叉和超时操作的详细信息，请参阅“音量更新”章节。

### 线路输入接口

ADC通路提供两对立体声线路输入（LINPUT2/RINPUT2 和 LINPUT3/RINPUT3）作为模拟输入接口。LINPUT3和RINPUT3也可通过旁路路径直接输入至输出混频器。

旁路路径的详细信息请参阅“输出信号路径”章节。

**INPUT BOOST**

The input path to the ADCs is via a boost stage, which can mix signals from the microphone PGAs and the line inputs.

The boost stage can provide up to +29dB additional gain from the microphone PGA output to the ADC input, providing a total maximum available analogue gain of +59dB from microphone to ADC. The microphone PGA path to the boost mixer is muted using LINMUTE and RINMUTE as shown in Table 4. Microphone PGA to boost gain settings are shown in Table 5.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) ADCL Signal path	5:4	LMICBOOST [1:0]	00	Left Channel Input PGA Boost Gain 00 = +0dB 01 = +13dB 10 = +20dB 11 = +29dB
R33 (21h) ADCR Signal path	5:4	RMICBOOST [1:0]	00	Right Channel Input PGA Boost Gain 00 = +0dB 01 = +13dB 10 = +20dB 11 = +29dB

**Table 5 Microphone PGA Boost Control**

For line inputs, -12dB to +6dB gain is available on the boost mixer, with mute control, as shown in Table 6.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R43 (2Bh) Input Boost Mixer 1	6:4	LIN3BOOST [2:0]	000	LINPUT3 to Boost Mixer gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB
	3:1	LIN2BOOST [2:0]	000	LINPUT2 to Boost Mixer gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB
R44 (2Ch) Input Boost Mixer 2	6:4	RIN3BOOST [2:0]	000	RINPUT3 to Boost Mixer gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB
	3:1	RIN2BOOST [2:0]	000	RINPUT2 to Boost Mixer gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB

**Table 6 Line Input Boost Control**

When all three input paths to the boost mixer are disabled, the boost mixer will automatically be muted.

### 输入升压电路

ADC的输入路径通过升压级实现，可混合来自麦克风PGA和线路输入接口的信号。

升压级可从麦克风可编程增益放大器输出端至模数转换器输入端提供最高+29分贝的额外增益，使麦克风至模数转换器的总最大模拟增益达到+59分贝。如表4所示，通过LINMUTE和RINMUTE可对通往升压混频器的麦克风PGA路径进行静音控制。麦克风PGA至升压级的增益设置详见表5。

寄存器地址	位	标签	默认值	描述
R32 (20h) ADCL信号路径	5:4	LMICBOOST [1:0]	00	左声道输入PGA升压增益 00 = +0分贝 01 = +13分贝 10 = +20分贝 11 = +29分贝
R33 (21h) ADCR信号路径	5:4	RMICBOOST [1:0]	00	右声道输入PGA升压增益 00 = +0分贝 01 = +13分贝 10 = +20分贝 11 = +29分贝

表5 麦克风可编程增益放大器升压控制

对于线路输入，升压混频器可提供-12分贝至+6分贝的增益范围，并配有如表6所示的静音控制功能。

寄存器地址	位	标签	默认值	描述
R43 (2Bh) 输入升压混频器1	6:4	左输入3升压控制 [2:0]	000	左输入3至升压混频器增益 000 = 静音 001 = -12分贝 ...以3分贝为步进递增至 111 = +6分贝
	3:1	左输入2升压控制 [2:0]	000	左输入2至升压混频器增益 000 = 静音 001 = -12分贝 ...以3分贝为步进递增至 111 = +6分贝
R44 (2Ch) 输入升压混频器2	6:4	右输入3升压控制 [2:0]	000	右输入3至升压混频器增益 000 = 静音 001 = -12分贝 ...以3分贝为步进递增至 111 = +6分贝
	3:1	右输入2升压控制 [2:0]	000	右输入2至升压混频器增益 000 = 静音 001 = -12分贝 ...以3分贝为步进递增至 111 = +6分贝

表6 线路输入升压控制

当所有三个输入路径至升压混频器均被禁用时，升压混频器将自动进入静音状态。

### MICROPHONE BIASING CIRCUIT

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. Refer to the Applications Information section for recommended external components. The MICBIAS voltage can be altered via the MBSEL register bit. When MBSEL=0, MICBIAS=0.9\*AVDD and when MBSEL=1, MICBIAS=0.65\*AVDD. The output can be enabled or disabled using the MICB control bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power management (1)	1	MICB	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON
R48 (30h) Additional Control (4)	0	MBSEL	0	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.65 * AVDD

Table 7 Microphone Bias Control

The internal MICBIAS circuitry is shown in Figure 9. The maximum source current capability for MICBIAS is 3mA. The external biasing resistors therefore must be large enough to limit the MICBIAS current to 3mA.

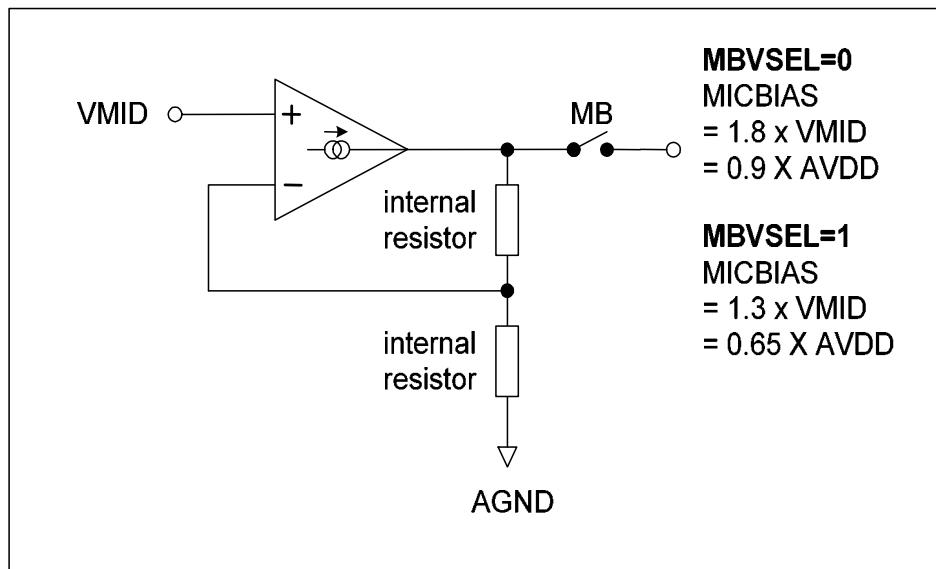


Figure 9 Microphone Bias Schematic

### 麦克风偏置电路

MICBIAS输出提供了一个适用于驻极体麦克风及相关外部电阻偏置网络的低噪声参考电压。推荐使用的外部元件请参阅应用信息章节。MICBIAS电压可通过MBSEL寄存器位进行调节：当MBSEL=0时，MICBIAS=0.9\*AVDD；当MBSEL=1时，MICBIAS=0.65\*AVDD。该输出可通过MICB控制位启用或禁用。

寄存器地址	位	标签	默认值	描述
R25 (19h) 电源管理 (1)	1	MICB	0	麦克风偏置使能 0 = 关闭（高阻输出） 1 = 开启
R48 (30h) 附加控制(4)	0	MBSEL	0	麦克风偏置电压控制 0 = 0.9 * AVDD 1 = 0.65 * AVDD

表7 麦克风偏置控制

内部MICBIAS电路结构如图9所示。MICBIAS的最大源电流能力为3mA，因此外部偏置电阻必须足够大以将MICBIAS电流限制在3mA以内。

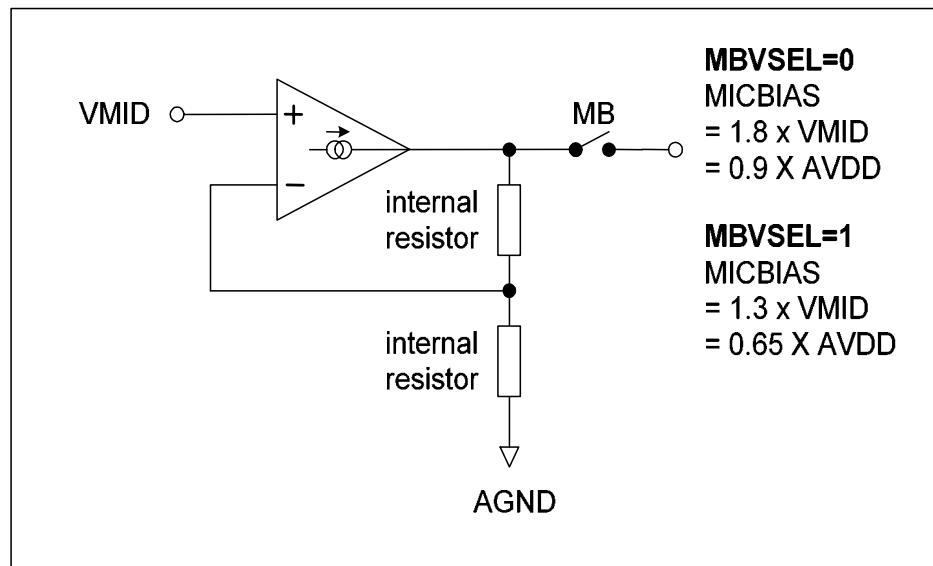


图9 麦克风偏置电路示意图

## EXAMPLE INPUT CONFIGURATIONS

Some example input configurations are shown below.

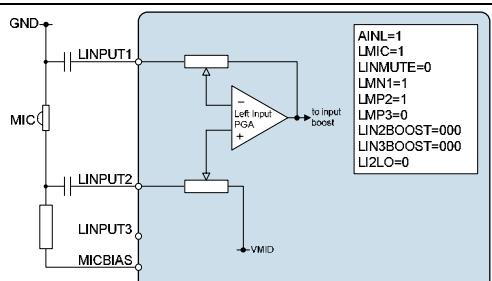
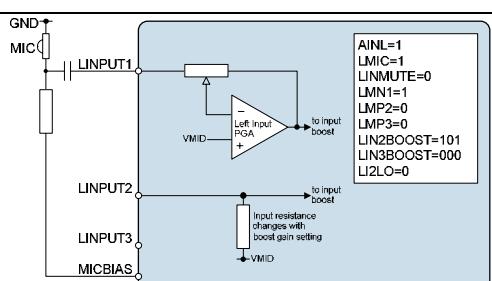
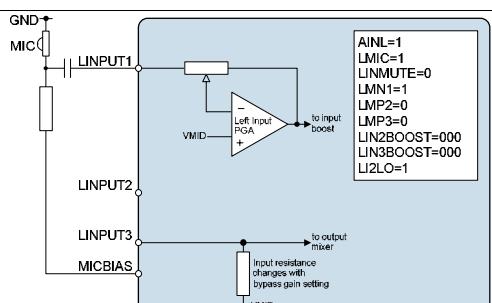
 <pre> AINL=1 LMIC=1 LINMUTE=0 LMN1=1 LMP2=1 LMP3=0 LIN2BOOST=000 LIN3BOOST=000 LI2LO=0 </pre>	<p>Pseudo-differential MIC configuration on left channel using LINPUT1 as ground connection and LINPUT2 as signal input. LINPUT3 unused.</p>
 <pre> AINL=1 LMIC=1 LINMUTE=0 LMN1=1 LMP2=0 LMP3=0 LIN2BOOST=101 LIN3BOOST=000 LI2LO=0 </pre>	<p>Single-ended MIC configuration on left channel. LINPUT2 used as additional input to boost stage. LINPUT3 unused.</p>
 <pre> AINL=1 LMIC=1 LINMUTE=0 LMN1=1 LMP2=0 LMP3=0 LIN2BOOST=000 LIN3BOOST=000 LI2LO=1 </pre>	<p>Single-ended MIC configuration on left channel. LINPUT3 used as input to bypass path. LINPUT2 unused.</p>

Figure 10 Example Microphone Input Configurations (See also "Recommended External Components")

## 输入配置示例

以下展示了一些输入配置的示例。

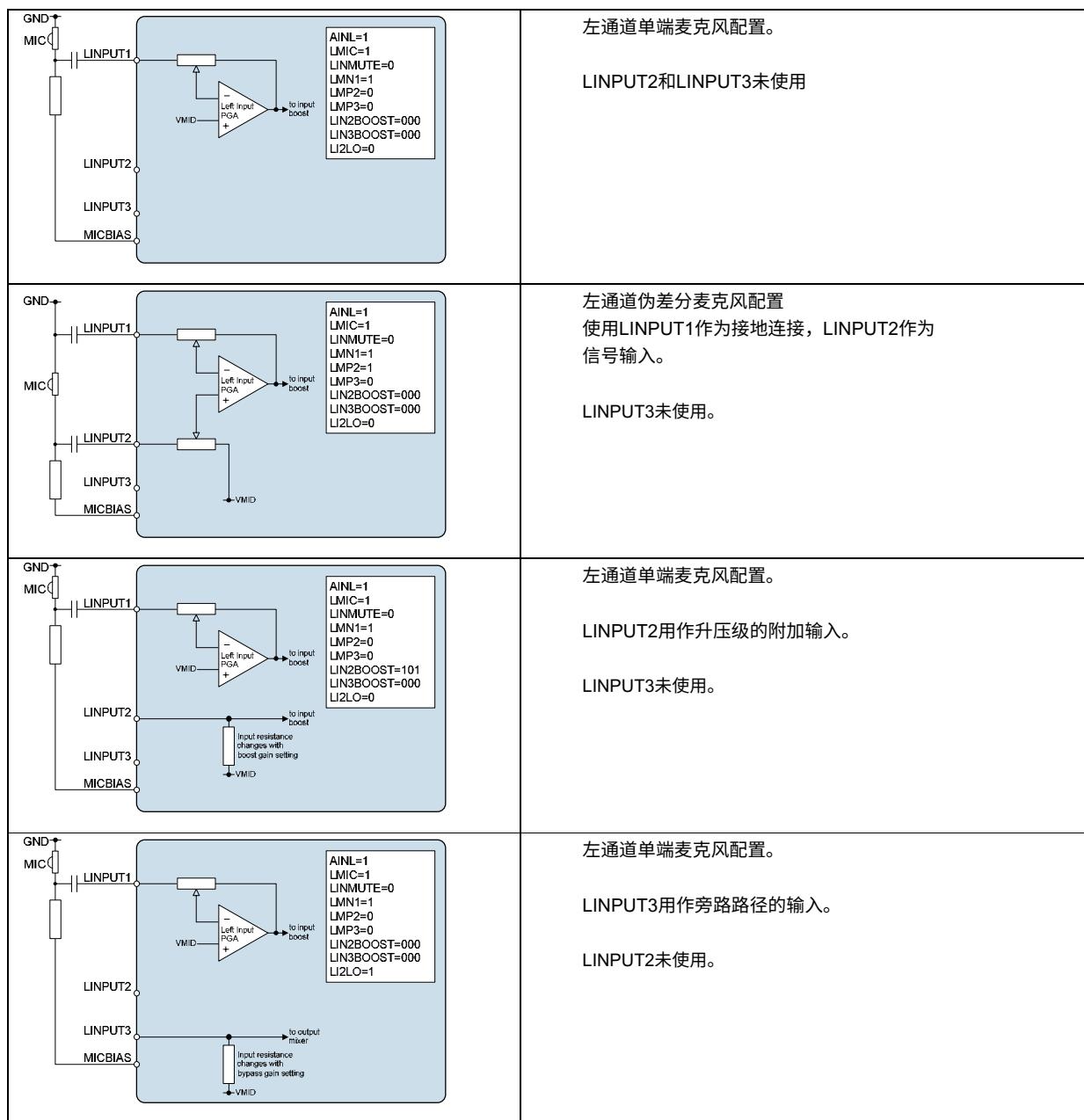


图10 麦克风输入配置示例（另请参见“推荐外部元件”）

## ANALOGUE TO DIGITAL CONVERTER (ADC)

The WM8960 uses stereo 24-bit, 64x oversampled sigma-delta ADCs. The use of multi-bit feedback and high oversampling rates reduce the effects of jitter and high frequency noise. The ADC Full Scale input level is proportional to AVDD. With a 3.3V supply voltage, the full scale level is  $1.0V_{rms}$ . Any voltage greater than full scale may overload the ADC and cause distortion.

The ADCs are enabled by the ADCL/R register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power management (2)	3	ADCL	0	Enable ADC left channel: 0 = ADC disabled 1 = ADC enabled
	2	ADCR	0	Enable ADC right channel: 0 = ADC disabled 1 = ADC enabled

Table 8 ADC Enable Control

The polarity of the output signal can be changed under software control using the ADCPOL[1:0] register bits. The DATSEL bits are used to select which channel is used for the left and right ADC data.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC Control (1)	6:5	ADCPOL[1:0]	00	ADC polarity control: 00 = Polarity not inverted 01 = ADC L inverted 10 = ADC R inverted 11 = ADC L and R inverted
R23 (17h) Additional Control (1)	3:2	DATSEL [1:0]	00	ADC Data Output Select 00: left data = left ADC; right data = right ADC 01: left data = left ADC; right data = left ADC 10: left data = right ADC; right data = right ADC 11: left data = right ADC; right data = left ADC

Table 9 ADC Control

## DIGITAL ADC VOLUME CONTROL

The output of the ADCs can be digitally amplified or attenuated over a range from  $-97dB$  to  $+30dB$  in  $0.5dB$  steps. The volume of each channel can be controlled separately. The gain for a given eight-bit code X is given by:

$$0.5 \times (X-195) \text{ dB} \text{ for } 1 \leq X \leq 255; \quad \text{MUTE for } X=0$$

The ADCVU control bit controls the loading of digital volume control data. When ADCVU is set to 0, the LADCVOL or RADCVOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when ADCVU is set to 1. This makes it possible to update the gain of both channels simultaneously.

## 模数转换器 (ADC)

WM8960采用立体声24位、64倍过采样Σ-Δ架构模数转换器。该器件通过多位反馈架构和高过采样率有效降低时钟抖动和高频噪声的影响。ADC的满量程输入电平与AVDD成比例关系。当供电电压为3.3V时，满量程电平为1.0V有效值。超过满量程的输入电压可能导致ADC过载并引发失真。

模数转换器通过ADCL/R寄存器位启用。

寄存器地址	位	标签	默认值	描述
R25 (19h) 电源 管理(2)	3	ADCL	0	启用左通道模数转换器： 0 = 模数转换器禁用 1 = 模数转换器启用
	2	ADCR	0	启用右通道模数转换器： 0 = 模数转换器禁用 1 = 模数转换器启用

表8 模数转换器启用控制

输出信号的极性可通过ADCPOL[1:0]寄存器位进行软件控制。DATSEL位用于选择左右通道的模数转换器数据源。

寄存器地址	位	标签	默认值	描述
R5 (05h) 模数 转换器和数模 转换器控制(1)	6:5	ADCPOL[1:0]	00	模数转换器极性控制： 00 = 极性未反相 01 = 左通道模数转换器反相 10 = 右通道模数转换器反相 11 = 左右通道模数转换器均反相
R23 (17h) 附加控制(1)	3:2	DATSEL [1:0]	00	ADC数据输出选择 00: 左数据=左ADC； 右数据=右ADC 01: 左数据=左ADC； 右数据=左ADC 10: 左数据=右ADC； 右数据=右ADC 11: 左数据=右ADC； 右数据=左ADC

表9 ADC控制

### 数字ADC音量控制

ADC的输出可通过数字方式在-97dB至+30dB范围内以0.5dB步进进行放大或衰减。各声道音量可独立控制，八位编码X对应的增益计算公式为：

$$0.5 \times (X-195) \text{ dB} \quad (\text{当 } 1 \leq X \leq 255 \text{ 时}) \quad \text{静音控制 (X=0时生效)}$$

ADCVU控制位用于管理数字音量控制数据的加载。当ADCVU设为0时，LADCVOL或RADCVOL控制数据将载入对应控制寄存器但不会实际改变数字增益设置。当ADCVU设为1时，左右声道增益设置将同步更新，从而实现双通道增益的同步调节。

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (15h) Left ADC Digital Volume	7:0	LADCVOL [7:0]	11000011 ( 0dB )	Left ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -97dB 0000 0010 = -96.5dB ... 0.5dB steps up to 1111 1111 = +30dB
	8	ADCVU	0	ADC Volume Update 0 = Store LADCVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LADCVOL, right = intermediate latch)
R22 (16h) Right ADC Digital Volume	7:0	RADCVOL [7:0]	11000011 ( 0dB )	Right ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -97dB 0000 0010 = -96.5dB ... 0.5dB steps up to 1111 1111 = +30dB
	8	ADCVU	0	ADC Volume Update 0 = Store RADCVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = RADCVOL)

**Table 10 ADC Digital Volume Control****ADC DIGITAL FILTERS**

The ADC filters perform true 24-bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface.

**HIGH PASS FILTER**

A digital high pass filter is applied by default to the ADC path to remove DC offsets. This filter can be disabled using the ADCHPD register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC Control (1)	0	ADCHPD	0	ADC High Pass Filter Disable 0 = Enable high pass filter on left and right channels 1 = Disable high pass filter on left and right channels

**Table 11 ADC High Pass Filter**

The high pass filter characteristics are shown in the Digital Filter Characteristics section.

寄存器地址	位	标签	默认值	描述
R21 (15h) 左ADC 数字音量	7:0	左ADC音量 [7:0]	11000011 (0分贝)	左ADC数字音量控制 0000 0000 = 数字静音 0000 0001 = -97分贝 0000 0010 = -96.5分贝 ... 以0.5分贝为步进递增至 1111 1111 = +30分贝
	8	ADC音量更新	0	ADC音量更新控制 0 = 将LADCVOL存储至中间锁存器(不改变增益) 1 = 更新左 右声道增益(左=LADCVOL, 右=中间锁存器)
R22 (16h) 右ADC 数字音量	7:0	右ADC音量 [7:0]	11000011 (0分贝)	右ADC数字音量控制 0000 0000 = 数字静音 0000 0001 = -97分贝 0000 0010 = -96.5分贝 ... 以0.5分贝为步进递增至 1111 1111 = +30分贝
	8	ADC音量更新	0	ADC音量更新 0 = 将 右ADC音量存入中间锁存器 (不改 变增益) 1 = 更新左右 声道增益 (左=中间锁存器值, 右=RADCVOL值)

表10 ADC数字音量控制

**ADC数字滤波器**

ADC滤波器执行真正的24位信号处理，将来自ADC的原始多位过采样数据转换为正确的采样频率，以便通过数字音频接口输出。

**高通滤波器**

默认在ADC路径中应用数字高通滤波器以消除直流偏移。可通过ADCHPD寄存器位禁用此滤波器。

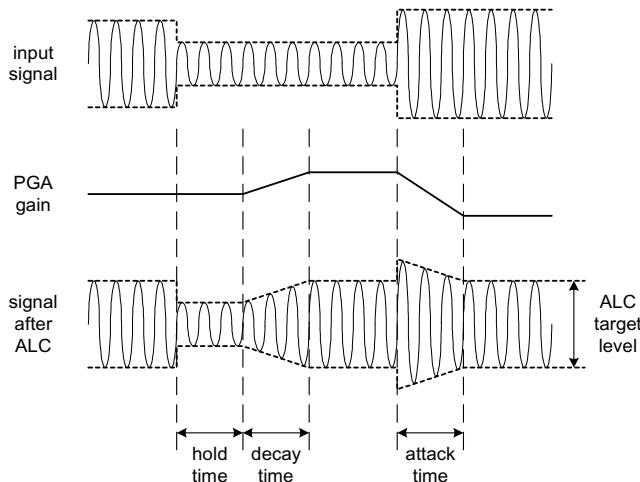
寄存器地址	位	标签	默认值	描述
R5 (05h) 模数转换器和数模转换器控制(1)	0	ADCHPD	0	ADC高通滤波器禁用 0 = 启用 左右声道的高通滤波器  1 = 禁用左右声道高通滤波器

表11 ADC高通滤波器

高通滤波器特性详见数字滤波器特性章节。

## AUTOMATIC LEVEL CONTROL (ALC)

The WM8960 has an automatic level control that aims to keep a constant recording volume irrespective of the input signal level. This is achieved by continuously adjusting the PGA gain so that the signal level at the ADC input remains constant. A digital peak detector monitors the ADC output and changes the PGA gain if necessary. Note that when the ALC function is enabled, the settings of registers 0 and 1 (LINVOL, IPVU, LIZC, LINMUTE, RINVOL, RIZC and RINMUTE) are ignored.



**Figure 11 ALC Operation**

The ALC function is enabled using the ALCSEL control bits. When enabled, the recording volume can be programmed between -1.5dB and -22.5dB (relative to ADC full scale) using the ALCL register bits. An upper limit for the PGA gain can be imposed by setting the MAXGAIN control bits.

HLD, DCY and ATK control the hold, decay and attack times, respectively:

**Hold** time is the time delay between the peak level detected being below target and the PGA gain beginning to ramp up. It can be programmed in power-of-two ( $2^n$ ) steps, e.g. 2.67ms, 5.33ms, 10.67ms etc. up to 43.7s. Alternatively, the hold time can also be set to zero. The hold time only applies to gain ramp-up, there is no delay before ramping the gain down when the signal level is above target.

**Decay** (Gain Ramp-Up) Time is the time that it takes for the PGA gain to ramp up across 90% of its range (e.g. from -15B up to 27.75dB). The time it takes for the recording level to return to its target value therefore depends on both the decay time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the decay time. The decay time can be programmed in power-of-two ( $2^n$ ) steps, from 24ms, 48ms, 96ms, etc. to 24.58s.

**Attack** (Gain Ramp-Down) Time is the time that it takes for the PGA gain to ramp down across 90% of its range (e.g. from 27.75dB down to -15B gain). The time it takes for the recording level to return to its target value therefore depends on both the attack time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the attack time. The attack time can be programmed in power-of-two ( $2^n$ ) steps, from 6ms, 12ms, 24ms, etc. to 6.14s.

When operating in stereo, the peak detector takes the maximum of left and right channel peak values, and any new gain setting is applied to both left and right PGAs, so that the stereo image is preserved. However, the ALC function can also be enabled on one channel only. In this case, only one PGA is controlled by the ALC mechanism, while the other channel runs independently with its PGA gain set through the control register.

When one ADC channel is unused, the peak detector disregards that channel.

## 自动电平控制(ALC)

WM8960具有自动电平控制功能，旨在无论输入信号电平如何变化都能保持恒定的录音音量。该功能通过持续调整PGA增益，使ADC输入端的信号电平保持恒定来实现。数字峰值检测器会监测ADC输出，并在必要时改变PGA增益。请注意，当启用ALC功能时，寄存器0和1（左输入音量、IPVU、LIZC、左输入静音、右输入音量、RIZC及右输入静音）的设置将被忽略。

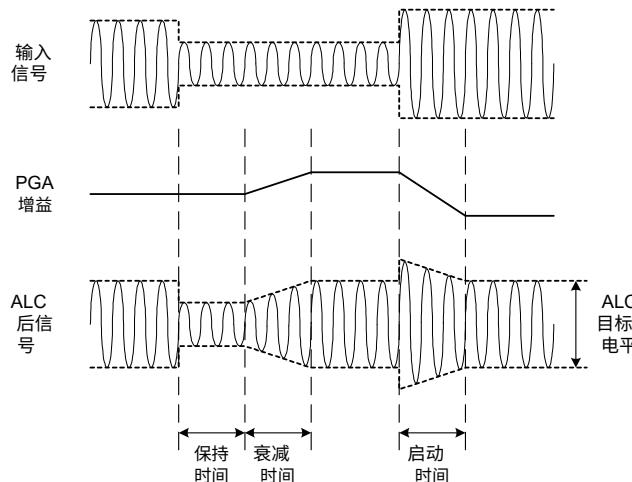


图11 ALC操作原理

ALC功能通过ALCSEL控制位启用。启用后，可使用ALCL寄存器位将录音音量编程设置为-1.5分贝至-22.5分贝（相对于ADC满量程）。通过设置MAXGAIN控制位可为PGA增益设置上限。

HLD、DCY和ATK分别控制保持时间、衰减时间和启动时间：

保持时间是指从检测到峰值电平低于目标值到PGA增益开始上升之间的时间延迟。该时间可通过2的幂次方（ $2^n$ ）步进进行编程设置，例如2.67毫秒、5.33毫秒、10.67毫秒等，最高可达43.7秒。此外，保持时间也可设置为零。需注意保持时间仅适用于增益上升过程，当信号电平超过目标值时，增益下降前不会有任何延迟。

衰减（增益上升）时间指PGA增益在其90%范围内完成上升所需的时间（例如从-15dB升至27.75dB）。录音电平恢复至目标值所需的时间取决于衰减时间和所需的增益调节量。若增益调节幅度较小，实际耗时将短于衰减时间。该衰减时间可通过2的幂次方（ $2^n$ ）步进编程设置，范围涵盖24毫秒、48毫秒、96毫秒等，最高可达24.58秒。

建立（增益衰减）时间是指PGA增益在其量程的90%范围内完成下降所需的时间（例如从27.75dB增益下降至-15B增益）。因此录音电平恢复到目标值所需的时间既取决于建立时间，也取决于所需的增益调整量。若增益调整幅度较小，所需时间将短于建立时间。建立时间可通过2的幂次方（ $2^n$ ）步进进行编程设置，范围从6ms、12ms、24ms等直至6.14秒。

在立体声工作模式下，峰值检测器会取左右声道峰值中的最大值，新的增益设置将同时应用于左右声道的可编程增益放大器，从而保持立体声场的一致性。然而，ALC功能也可仅在单声道启用。在此情况下，仅一个PGA受ALC机制控制，另一声道则独立运行，其PGA增益通过控制寄存器进行设置。

当某个ADC通道未被使用时，峰值检测器将忽略该通道。

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R17 (11h) ALC Control (1)	8:7	ALCSEL [1:0]	00 (OFF)	ALC Function Select 00 = ALC off (PGA gain set by register) 01 = Right channel only 10 = Left channel only 11 = Stereo (PGA registers unused) Note: ensure that LINVOL and RINVOL settings (reg. 0 and 1) are the same before entering this mode.
	6:4	MAXGAIN [2:0]	111 (+30dB)	Set Maximum Gain of PGA 111 : +30dB 110 : +24dB ....(-6dB steps) 001 : -6dB 000 : -12dB
	3:0	ALCL [3:0]	1011 (-12dB)	ALC Target (Sets signal level at ADC input) 0000 = -22.5dB FS 0001 = -21.0dB FS ... (1.5dB steps) 1101 = -3.0dB FS 1110 = -1.5dB FS 1111 = -1.5dB FS
R18 (12h) ALC Control (2)	6:4	MINGAIN [2:0]	000	Set Minimum Gain of PGA 000 = -17.25dB 001 = -11.25dB 010 = -5.25dB 011 = +0.75dB 100 = +6.75dB 101 = +12.75dB 110 = +18.75dB 111 = +24.75dB
	3:0	HLD [3:0]	0000 (0ms)	ALC hold time before gain is increased. 0000 = 0ms 0001 = 2.67ms 0010 = 5.33ms ... (time doubles with every step) 1111 = 43.691s
R19 (13h) ALC Control (3)	8	ALCMODE	0	Determines the ALC mode of operation: 0 = ALC mode 1 = Limiter mode
	7:4	DCY [3:0]	0011 (192ms)	ALC decay (gain ramp-up) time 0000 = 24ms 0001 = 48ms 0010 = 96ms ... (time doubles with every step) 1010 or higher = 24.58s
	3:0	ATK [3:0]	0010 (24ms)	ALC attack (gain ramp-down) time 0000 = 6ms 0001 = 12ms 0010 = 24ms ... (time doubles with every step) 1010 or higher = 6.14s

寄存器地址	位	标签	默认值	描述
R17 (11h) ALC控制 (1)	8:7	ALCSEL [1:0]	00 (关闭)	ALC功能选择 00 = ALC关闭 (PGA增益由寄存器设置) 01 = 仅右声道 10 = 仅左声道 11 = 立体声模式 (PGA寄存器未使用) 注意: 进入此模式前需确保LINVOL和RINVOL设置 (寄存器0和1) 相同。
	6:4	MAXGAIN [2:0]	111 (+30分贝)	设置PGA最大增益 111 : +30dB 110 : +24dB ...(-6dB步进) 001 : -6dB 000 : -12dB
	3:0	ALCL [3:0]	1011 (-12分贝)	ALC目标值 (设置ADC输入端的信号电平) 0000 = -22.5d B FS 0001 = -21.0dB FS ... (1.5dB步进) 1 101 = -3.0dB FS 111 0 = -1.5dB FS 1111 = -1.5dB FS
R18 (12h) ALC控制 (2)	6:4	MINGAIN [2:0]	000	设置PGA最小增益 000 = -17.25dB 001 = -11.25dB 010 = -5.25dB 011 = +0.75dB 100 = +6.75dB 101 = +12.75dB 110 = +18.75dB 111 = +24.75dB
	3:0	HLD [3:0]	0000 (0毫秒)	增益提升前ALC保持时间 0000 = 0毫秒 0001 = 2.67毫秒 0010 = 5.33毫秒 ... (每步时间加倍) 1111 = 43.691秒
R19 (13h) ALC控制 (3)	8	ALCMODE	0	确定ALC的工作模式: 0 = ALC模式 1 = 限幅器模式
	7:4	DCY [3:0]	0011 (192毫秒)	ALC衰减 (增益上升) 时间 0000 = 24毫秒 0001 = 48毫秒 0010 = 96毫秒 ... (每步时间加倍) 1010 或更高值 = 24.58秒
	3:0	ATK [3:0]	0010 (24毫秒)	ALC启动 (增益下降) 时间 0000 = 6毫秒 0001 = 12毫秒 0010 = 24毫秒 ... (每步时间加倍) 1010 或更高值 = 6.14秒

R27 (1Bh) Additional Control (3)	2:0	ADC_ALC_SR [2:0]	000	ALC Sample Rate 000 = 44.1k / 48k 001 = 32k 010 = 22.05k / 24k 011 = 16k 100 = 11.25k / 12k 101 = 8k 110 and 111 = Reserved
--	-----	---------------------	-----	--

**Table 12 ALC Control****ALC SAMPLE RATE CONTROL**

The register bits ADC\_ALC\_SR must be set correctly to ensure that the ALC attack, decay and hold times are correct for the chosen sample rate as shown in Table 12.

**PEAK LIMITER**

To prevent clipping when a large signal occurs just after a period of quiet, the ALC circuit includes a limiter function. If the ADC input signal exceeds 87.5% of full scale (-1.16dB), the PGA gain is ramped down at the maximum attack rate (as when ATK = 0000), until the signal level falls below 87.5% of full scale. This function is automatically enabled whenever the ALC is enabled.

**Note:**

If ATK = 0000, then the limiter makes no difference to the operation of the ALC. It is designed to prevent clipping when long attack times are used.

**NOISE GATE**

When the signal is very quiet and consists mainly of noise, the ALC function may cause "noise pumping", i.e. loud hissing noise during silence periods. The WM8960 has a noise gate function that prevents noise pumping by comparing the signal level at the input pins against a noise gate threshold, NGTH. The noise gate cuts in when:

- Signal level at ADC [dB] < NGTH [dB] + PGA gain [dB] + Mic Boost gain [dB]

This is equivalent to:

- Signal level at input pin [dB] < NGTH [dB]

The PGA gain will then be held constant (preventing it from ramping up as it normally would when the signal is quiet).

The table below summarises the noise gate control register. The NGTH control bits set the noise gate threshold with respect to the ADC full-scale range. The threshold is adjusted in 1.5dB steps. Levels at the extremes of the range may cause inappropriate operation, so care should be taken with set-up of the function. Note that the noise gate only works in conjunction with the ALC function, and always operates on the same channel(s) as the ALC (left, right, both, or none).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 (14h) Noise Gate Control	7:3	NGTH [4:0]	00000	Noise gate threshold 00000 -76.5dBfs 00001 -75dBfs ... 1.5 dB steps 11110 -31.5dBfs 11111 -30dBfs
	0	NGAT	0	Noise gate function enable 0 = disable 1 = enable

**Table 13 Noise Gate Control**

R27 (1Bh) 附加 控制 (3)	2:0	ADC_ALC_SR [2:0]	000	ALC采样率 000 = 44.1k / 48k 001 = 32k 010 = 22.05k / 24k 011 = 16k 100 = 11.25k / 12k 101 = 8k 110 和 111 = 保留
---------------------------	-----	---------------------	-----	---

表12 ALC控制

**ALC采样率控制**

必须正确设置寄存器位ADC\_ALC\_SR，以确保如表12所示，针对所选采样率的ALC启动、衰减和保持时间参数准确无误。

**峰值限幅器**

为防止在静音段后突现强信号时发生削波，ALC电路包含限幅器功能。当模数转换器输入信号超过满量程的87.5% (-1.16分贝) 时，PGA增益会以最大恢复速率（即ATK=0000时的速率）逐步降低，直至信号电平回落至满量程87.5%以下。该功能在启用ALC时自动激活。

**注意：**

当ATK=0000时，限幅器不会改变自动电平控制的工作模式。该功能专为使用较长恢复时间时防止削波而设计。

**噪声门**

当信号非常微弱且主要由噪声构成时，自动电平控制功能可能引发"噪声泵"效应，即在静默期间产生显著嘶嘶声。WM8960配备噪声门功能，通过将输入引脚信号电平与噪声门阈值(NGTH)进行对比，可有效防止噪声泵效应。噪声门在以下条件触发：

- 模数转换器处的信号电平[分贝] < 噪声门限阈值[分贝] + 可编程增益放大器增益[分贝] + 麦克风升压增益[分贝]

这等效于：

- 输入引脚处的信号电平[分贝] < 噪声门限阈值[分贝]

此时可编程增益放大器增益将保持恒定（防止在信号静默时像常规情况那样逐步提升）。

下表总结了噪声门控制寄存器。NGTH控制位设置相对于模数转换器满量程范围的噪声门限阈值。阈值以1.5分贝步进进行调整。

范围极值处的电平可能导致功能异常，因此需谨慎设置该功能。需注意噪声门仅与自动电平控制功能协同工作，且始终作用于与自动电平控制相同的声道（左、右、双声道或无）。

寄存器地址	位	标签	默认值	描述
R20 (14h) 噪声门 控制	7:3	NGTH [4:0]	00000	噪声门限阈值 00000 -76.5dBfs 00001 -75dBfs ... 1.5分贝步进 11110 -31.5dBfs 11111 -30dBfs
	0	NGAT	0	噪声门功能使能 0 = 禁用 1 = 启用

表13 噪声门控制

## OUTPUT SIGNAL PATH

The hi-fi DACs and DAC digital filters are enabled by register bits DACL and DACR. The mixers and output drivers can be separately enabled by individual control bits (see Analogue Outputs). Thus it is possible to utilise the analogue mixing and amplification provided by the WM8960, irrespective of whether the DACs are enabled or not.

The WM8960 DACs receive digital input data on the DACDAT pin. The digital filter block processes the data to provide the following functions:

- § Digital volume control with soft mute and soft un-mute
- § Mono mix
- § 3D stereo enhancement
- § De-emphasis
- § Sigma-delta modulation

High performance sigma-delta 24-bit audio DAC converts the digital data into an analogue signal.

The analogue outputs from the DACs can then be mixed with the analogue line inputs and the ADC analogue inputs. This mix is fed to the output drivers for headphone or speaker output. OUT3 can provide a mono mix of left and right mixers or a pseudo-ground for capless headphone drive.

## DIGITAL PLAYBACK (DAC) PATH

Digital data is passed to the WM8960 via the flexible audio interface to the hi-fi DACs. The DACs are enabled by the DACL and DACR register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R26 (1Ah) Power Management (2)	8	DACL	0	Left Channel DAC Enable 0 = DAC disabled 1 = DAC enabled
	7	DACR	0	Right Channel DAC Enable 0 = DAC disabled 1 = DAC enabled

Table 14 DAC Enable Control

### DIGITAL DAC VOLUME CONTROL

The signal volume from each DAC can be controlled digitally, in the same way as the ADC volume (see Digital ADC Volume Control). The gain and attenuation range is -127dB to 0dB in 0.5dB steps. The level of attenuation for an eight-bit code X is given by:

$$0.5 \times (X-255) \text{ dB} \quad \text{for } 1 \leq X \leq 255; \quad \text{MUTE for } X = 0$$

The DACVU control bit controls the loading of digital volume control data. When DACVU is set to 0, the LDACVOL or RDACVOL control data is loaded into an intermediate register, but the actual gain does not change. Both left and right gain settings are updated simultaneously when DACVU is set to 1.

See "Volume Updates" for more information on volume update bits.

## 输出信号路径

高保真数模转换器(DACs)及其数字滤波器通过寄存器位DACL和DSCR启用。混音器和输出驱动器可通过独立控制位单独启用（参见模拟输出接口）。因此无论DAC是否启用，均可利用WM8960提供的模拟混音和放大功能。

WM8960的数模转换器通过DACDAT引脚接收数字输入数据。数字滤波器模块对数据进行处理，提供以下功能：

- § 带软静音和软解除静音功能的数字音量控制
- § 单声道混音
- § 3D立体声增强
- § 去加重处理
- § Σ-Δ调制

高性能Σ-Δ型24位音频数模转换器将数字数据转换为模拟信号

DAC输出的模拟信号可与线路输入的模拟信号及ADC模拟输入信号进行混合。该混合信号被送至输出驱动器，用于耳机或扬声器输出。OUT3可提供左右声道混音器的单声道混合信号，或为无电容耳机驱动提供伪接地参考。

### 数字播放 (DAC) 路径

数字数据通过灵活音频接口传输至WM8960的高保真数模转换器。通过设置DACL和DSCR寄存器位可启用数模转换器。

寄存器地址	位	标签	默认值	描述
R26 (1A h) 电 源管理 (2)	8	左声道数模转换器	0	左声道数模转换器使能 0 = 禁用DAC 1 = 启用DAC
	7	右声道数模转换器	0	右声道数模转换器使能 0 = 禁用DAC 1 = 启用DAC

表14 DAC使能控制

### 数字DAC音量控制

每个DAC的信号音量可通过数字方式控制，其控制方式与ADC音量类似（参见数字ADC音量控制）。增益与衰减范围为-127分贝至0分贝，步进精度为0.5分贝。  
八位代码X对应的衰减量计算公式如下：

$$0.5 \times (X-255) \text{ 分贝} \quad (\text{当 } 1 \leq X \leq 255 \text{ 时}) \quad \text{静音控制 (X=0时生效)}$$

DACVU控制位用于管理数字音量控制数据的加载。当DACVU设为0时，LDACVOL或RDACVOL控制数据将存入中间寄存器但实际增益不变。当DACVU设为1时，左右声道增益设置将同步更新。

有关音量更新位的更多信息，请参见“音量更新”章节。

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) Left Channel Digital Volume	8	DACVU	0	DAC Volume Update 0 = Store LDACVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LDACVOL, right = intermediate latch)
	7:0	LDACVOL [7:0]	11111111 ( 0dB )	Left DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB
R11 (0Bh) Right Channel Digital Volume	8	DACVU	0	DAC Volume Update 0 = Store RDACVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = RDACVOL)
	7:0	RDACVOL [7:0]	11111111 ( 0dB )	Right DAC Digital Volume Control similar to LDACVOL

Table 15 Digital Volume Control

**DAC SOFT MUTE AND SOFT UN-MUTE**

The WM8960 also has a soft mute function, which, when enabled, gradually attenuates the volume of the digital signal to zero. When soft mute is disabled, the gain will either gradually ramp back up to the digital gain setting, or return instantly to the digital gain setting, depending on the DACSMM register bit.

The DAC is soft-muted by default. To play back an audio signal, this function must first be disabled by setting the DACMU bit to zero.

DACSMM would typically be enabled when using soft mute during playback of audio data so that when soft mute is then disabled, the sudden volume increase will not create pop noise by jumping immediately to the previous volume level (e.g. resuming playback after pausing during a track).

DACSMM would typically be disabled when un-muting at the start of a digital music file, so that the first part of the track is not attenuated (e.g. when starting playback of a new track, or resuming playback after pausing between tracks).

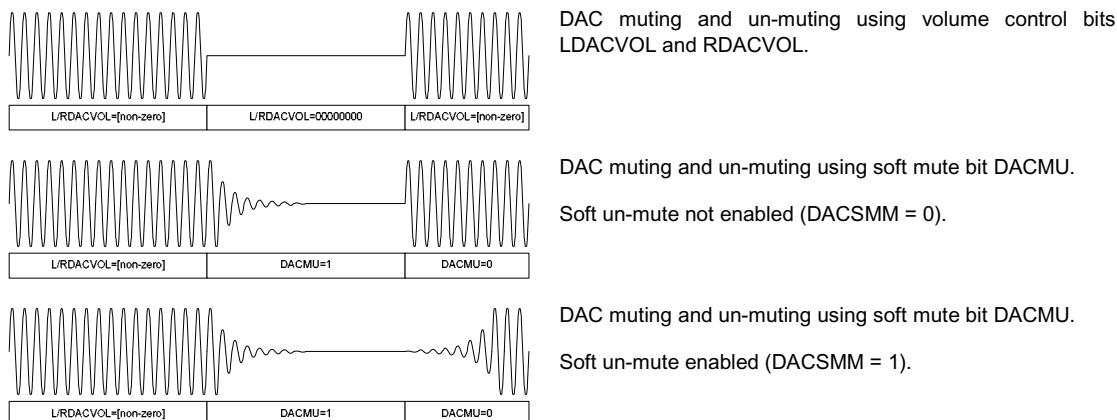


Figure 12 DAC Mute Control

The volume ramp rate during soft mute and un-mute is controlled by the DACMR bit. Ramp rates of fs/32 and fs/2 are selectable as shown in Table 16 (fs = DAC sample rate).

寄存器地址	位	标签	默认值	描述
R10 (0Ah) 左声道 数字音量	8	DACVU	0	DAC音量更新 0 = 将 LDACVOL存储至中间锁存器（无增益变化） 1 = 更新左右声道增益（左=LDACVOL，右=中间锁存器）
	7:0	左DAC音量 [7:0]	11111111 (0分贝)	左DAC数字音量控制 0000 0000 = 数字静音 0000 0001 = -127分贝 0000 0010 = -126.5分贝 ... 以0.5分贝为步进递增至 1111 1111 = 0分贝
R11 (0Bh) 右声道 数字音量	8	DACVU	0	DAC音量更新 0 = 将 RDACVOL存储至中间锁存器（无增益变化） 1 = 更新左右声道增益（左=中间锁存器，右=RDACVOL）
	7:0	右DAC音量 [7:0]	11111111 (0分贝)	右DAC数字音量控制与LDAC音量类似

表15 数字音量控制

**DAC软静音与软解除静音**

WM8960还具备软静音功能，启用时会将数字信号的音量逐渐衰减至零。当禁用软静音时，增益将根据DACSMM寄存器位的设置，或逐渐恢复至数字增益设定值，或立即跳转回数字增益设定值。

数模转换器默认处于软静音状态。要播放音频信号，需首先通过将DACMU位设为零来禁用此功能。

在音频数据播放期间使用软静音时，通常应启用DACSMM模块。这样当后续解除软静音时，可避免因音量突然跳升至先前水平（例如在曲目暂停后恢复播放时）产生爆音噪声。

在数字音乐文件开始播放时取消静音操作，DACSMM（数模转换器模拟电源管理模块）通常会被禁用，以避免音轨起始部分被衰减（例如在开始播放新曲目时，或在曲目间暂停后恢复播放时）。

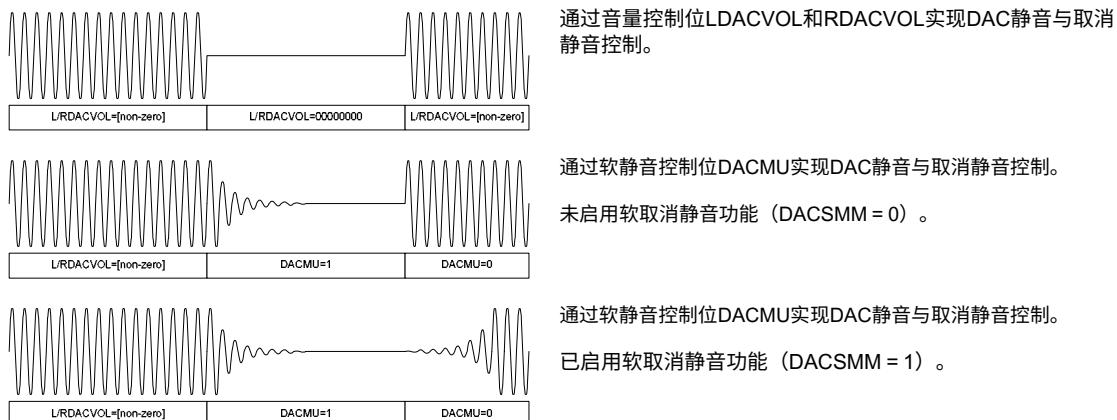


图12 DAC静音控制

软静音和取消静音过程中的音量渐变速率由DACMR位控制。可选择fs/32和fs/2两种渐变速率（如表16所示，其中fs表示DAC采样率）。

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC Control (1)	3	DACMU	1	Digital Soft Mute 1 = Mute 0 = No mute (signal active)
R6 (06h) ADC and DAC Control (2)	3	DACSMM	0	DAC Soft Mute Mode 0 = Disabling soft-mute (DACMU=0) will cause the volume to change immediately to the LDACVOL / RDACVOL settings 1 = Disabling soft-mute (DACMU=0) will cause the volume to ramp up gradually to the LDACVOL / RDACVOL settings
	2	DACMR	0	DAC Soft Mute Ramp Rate 0 = Fast ramp (fs/2 at fs=48k, providing maximum delay of 10.7ms) 1 = Slow ramp (fs/32 at fs=48k, providing maximum delay of 171ms)

Table 16 DAC Soft-Mute Control

**DAC DE-EMPHASIS**

Digital de-emphasis can be applied to the DAC playback data (e.g. when the data comes from a CD with pre-emphasis used in the recording). De-emphasis filtering is available for sample rates of 48kHz, 44.1kHz and 32kHz.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC Control (1)	2:1	DEEMPH [1:0]	00	De-Emphasis Control 11 = 48kHz sample rate 10 = 44.1kHz sample rate 01 = 32kHz sample rate 00 = No de-emphasis

Table 17 DAC De-Emphasis Control

**DAC OUTPUT PHASE AND MONO MIXING**

The digital audio data is converted to oversampled bit streams in the on-chip, true 24-bit digital interpolation filters. The bitstream data enters two multi-bit, sigma-delta DACs, which convert them to high quality analogue audio signals. The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a Dynamic Element Matching technique for high linearity and low distortion.

In normal operation, the left and right channel digital audio data is converted to analogue in two separate DACs. There is a mono-mix mode where the two audio channels are mixed together digitally and then converted to analogue using only one DAC, while the other DAC is switched off. The mono-mix signal can be selected to appear on both analogue output channels. The mono mix is automatically attenuated by 6dB to prevent clipping.

The DAC output defaults to non-inverted. Setting DACPOL[0] bit will invert the left DAC output phase and setting DACPOL[1] bit will invert the right DAC output phase.

寄存器地址	位	标签	默认值	描述
R5 (05h) 模数转换器和数模转换器控制(1)	3	数模转换器静音控制单元	1	数字软静音 1 = 静音 0 = 非静音（信号激活）
R6 (06h) ADC与DAC控制寄存器(2)	3	数模转换器模拟电源管理模块	0	DAC软静音模式 0 = 禁用软静音 (DACMU=0) 时，音量将立即切换至LDAC音量/右DAC音量设置 1 = 禁用软静音 (DACMU=0) 时，音量将逐步渐变至LDAC音量/右DAC音量设置
	2	DAC主控右声道	0	DAC软静音斜坡速率 0 = 快速斜坡（在48kHz采样率下为fs/2, 最大延迟10.7ms） 1 = 慢速斜坡（在48kHz采样率下为fs/32, 最大延迟171ms）

表16 DAC软静音控制

**DAC去加重功能**

可对DAC回放数据应用数字去加重处理（例如处理来自采用预加重录音的CD数据时）。去加重滤波器支持48kHz、44.1kHz和32kHz三种采样率。

寄存器地址	位	标签	默认值	描述
R5 (05h) 模数转换器和数模转换器控制(1)	2:1	DEEMPH [1:0]	00	去加重控制 11 = 48千赫采样率 10 = 44.1千赫采样率 01 = 32千赫采样率 00 = 无去加重

表17 DAC去加重控制

**DAC输出相位与单声道混合**

数字音频数据通过片内真正的24位数字插值滤波器转换为过采样比特流。该比特流数据进入两个多位Σ-Δ数模转换器，将其转换为高质量模拟音频信号。多位DAC架构可降低高频噪声和对时钟抖动的敏感性，同时采用动态元件匹配技术实现高线性度和低失真。

在正常操作中，左右声道数字音频数据通过两个独立的DAC进行数模转换。单声道混合模式下，两个音频通道先进行数字混合，然后仅使用一个DAC进行转换（另一个DAC关闭）。混合后的单声道信号可选择同时输出到两个模拟输出通道，并自动衰减6分贝以防止削波。

DAC输出默认为非反相。设置DACPOL[0]位将使左声道数模转换器(DACL)输出相位反相，设置DACPOL[1]位将使右声道数模转换器(DACR)输出相位反相。

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) ADC and DAC Control (2)	6:5	DACPOL[1:0]	00	DAC Polarity Control: 00 = Polarity not inverted 01 = DAC L inverted 10 = DAC R inverted 11 = DAC L and R inverted
R23 (17h) Additional Control (1)	4	DMONOMIX	0	DAC Mono Mix 0 = Stereo 1 = Mono (Mono MIX output on enabled DACs)

**Table 18 DAC Mono Mix and Phase Invert Select****3D STEREO ENHANCEMENT**

The WM8960 has a digital 3D enhancement option to artificially increase the separation between the left and right channels. This effect can only be used for playback, not for record.

The 3D enhancement function is activated by the 3DEN bit, and the 3DDEPTH setting controls the degree of stereo expansion. Additionally, one of four filter characteristics can be selected for the 3D processing, using the 3DUC and 3DLC control bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16 (10h) 3D enhance	6	3DUC	0	Upper Cut-Off Frequency 0 = High (Recommended for $fs \geq 32\text{kHz}$ ) 1 = Low (Recommended for $fs < 32\text{kHz}$ )
	5	3DLC	0	Lower Cut-Off Frequency 0 = Low (Recommended for $fs \geq 32\text{kHz}$ ) 1 = High (Recommended for $fs < 32\text{kHz}$ )
	4:1	3DDEPTH [3:0]	0000	3D Stereo Depth 0000 = 0% (minimum 3D effect) 0001 = 6.67% ... 1110 = 93.3% 1111 = 100% (maximum 3D effect)
	0	3DEN	0	3D Stereo Enhancement Enable 0 = Disabled 1 = Enabled

**Table 19 3D Stereo Enhancement Function**

When 3D enhancement is enabled it may be necessary to attenuate the signal by 6dB to avoid limiting. This is a user-selectable function, enabled by setting DACDIV2.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC control (1)	7	DACDIV2	0	DAC 6dB attenuate enable 0 = disabled (0dB) 1 = -6dB enabled

**Table 20 DAC 6dB Attenuation Select**

寄存器地址	位	标签	默认值	描述
R6 (06h) ADC与DAC 控制寄存器(2)	6:5	DACPOL[1:0]	00	DAC极性控制： 00 = 极性未反相 01=左DAC反相 10=右DAC反相 11=左右DAC均反相
R23 (17h) 附加 控制位 (1)	4	DMONOMIX	0	DAC单声道混音 0=立体声 1=单声道（在启用的DAC上输出单声道混音）

表18 DAC单声道混音及相位反转选择

**3D立体声增强**

WM8960具有数字3D增强选项，可人工扩展左右声道间的分离度。此效果仅适用于播放模式，不可用于录音场景。

通过3DEN位激活3D增强功能，3DEPTH设置控制立体声扩展程度。此外，可使用3DUC和3DLC控制位从四种滤波器特性中选择一种用于3D处理。

寄存器地址	位	标签	默认值	描述
R16 (10h) 3D增强	6	3DUC	0	上截止频率 0 = 高（建议用于采样频率 $\geq$ 32kHz） 1 = 低（建议用于采样频率 $<$ 32kHz）
	5	3DLC	0	下截止频率 0 = 低（建议用于采样频率 $\geq$ 32kHz） 1 = 高（建议用于采样频率 $<$ 32kHz）
	4:1	3D深度 [3:0]	0000	3D立体声深度 0000 = 0%（最小3D效果） 0001 = 6.67% ... 1110 = 93.3% 1111 = 100%（最大3D效果）
	0	3D使能	0	3D立体声增强使能 0 = 禁用 1 = 启用

表19 3D立体声增强功能

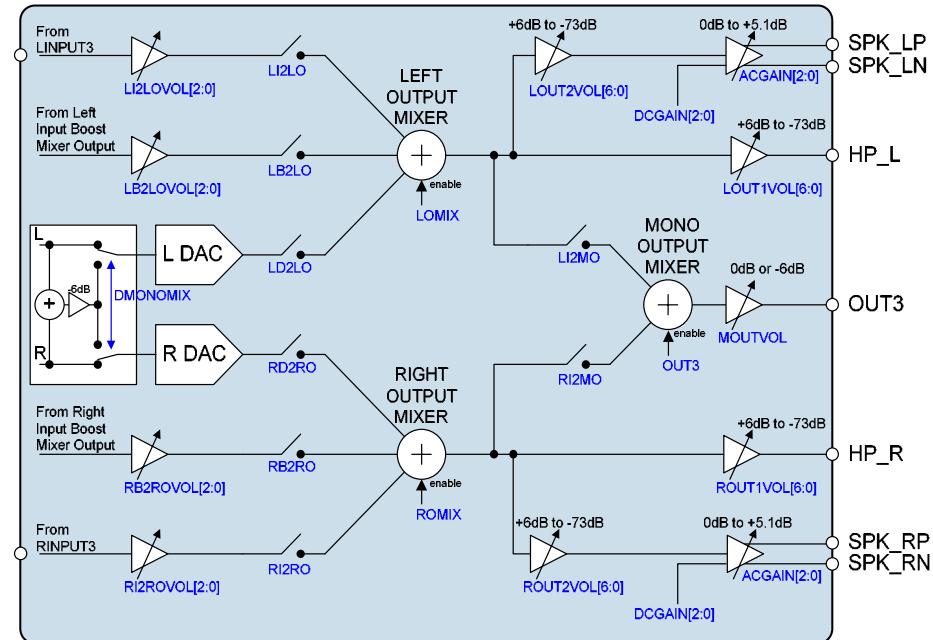
启用3D增强功能时，可能需要将信号衰减6分贝以避免限幅。这是用户可选功能，通过设置DACDIV2启用。

寄存器地址	位	标签	默认值	描述
R5 (05h) 模数转换器和数模转换器 控制 (1)	7	DACDIV2	0	DAC 6分贝衰减启用 0 = 禁用（0分贝） 1 = 启用-6分贝衰减

表20 DAC 6分贝衰减选择

## OUTPUT MIXERS

Left and right analogue mixers allow the DAC output and analogue bypass paths to be mixed. Programmable attenuation and mute is available on the analogue bypass paths from LINPUT3, RINPUT3 and from the input boost mixers as shown in Figure 13. A mono mix of left and right output mixers is also available on OUT3.



**Figure 13 Output Mixer Path**

Left and right mixers are enabled by the LOMIX and ROMIX register bits. The mono mixer is enabled by OUT3 register bit, which also enables the OUT3 driver.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 (2Fh) Power Management (3)	3	LOMIX	0	Left Output Mixer Enable Control 0 = Disabled 1 = Enabled
	4	ROMIX	0	Right Output Mixer Enable Control 0 = Disabled 1 = Enabled
R26 (1Ah) Power Management (2)	1	OUT3	0	Mono Output and Mono Mixer Enable Control 0 = Mono mixer and output disabled 1 = Mono mixer and output enabled

**Table 21 Output Mixer Enable Control**

Inputs to the mixers from the DAC and bypass paths can be individually muted. The bypass paths have programmable attenuation as shown in Table 22. To prevent pop noise, it is recommended not to change volume levels of these paths during playback.

### 输出混频器

左右模拟混频器允许将DAC输出和模拟旁路路径进行混合。

如图13所示，来自左输入3、右输入3以及输入升压混频器的模拟旁路路径可进行可编程衰减和静音控制。左右输出混频器的单声道混合信号也可通过OUT3输出。

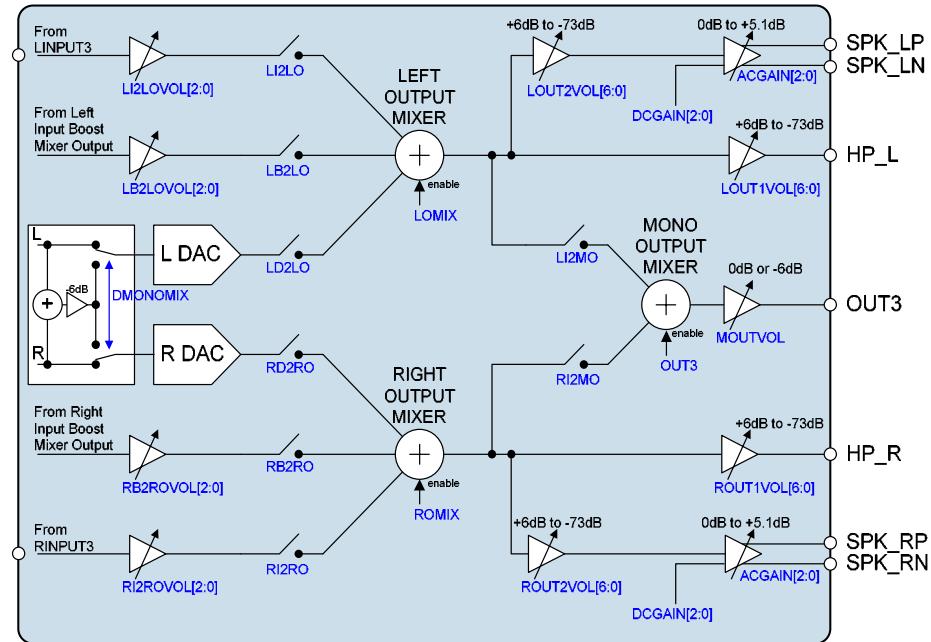


图13 输出混频器路径

通过LOMIX和ROMIX寄存器位启用左右混频器。OUT3寄存器位可启用单声道混频器，同时激活OUT3驱动器。

寄存器地址	位	标签	默认值	描述
R47 (2Fh) 电源管理(3)	3	LOMIX	0	左声道输出混频器启用控制 0 = 禁用 1 = 启用
	4	ROMIX	0	右声道输出混频器启用控制 0 = 禁用 1 = 启用
R26 (1Ah) 电源管理(2)	1	OUT3	0	单声道输出及单声道混频器启用控制 0 = 单声道混频器及输出禁用 1 = 单声道混频器及输出启用

表21 输出混频器使能控制

来自DAC和旁路路径的混频器输入可单独静音。如表22所示，旁路路径具有可编程衰减功能。为防止爆音噪声，建议在播放期间不要更改这些路径的音量等级。

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R34 (22h) Left Output Mixer Control	8	LD2LO	0	Left DAC to Left Output Mixer 0 = Disable (Mute) 1 = Enable Path
	7	LI2LO	0	LINPUT3 to Left Output Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	LI2LOVOL [2:0]	101 (-15dB)	LINPUT3 to Left Output Mixer Volume 000 = 0dB ...(3dB steps) 111 = -21dB
R45 (2Dh) Bypass (1)	7	LB2LO	0	Left Input Boost Mixer to Left Output Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	LB2LOVOL [2:0]	101 (-15dB)	Left Input Boost Mixer to Left Output Mixer Volume 000 = 0dB ...(3dB steps) 111 = -21dB
	8	RD2RO	0	Right DAC to Right Output Mixer 0 = Disable (Mute) 1 = Enable Path
R37 (25h) Right Output Mixer Control	7	RI2RO	0	RINPUT3 to Right Output Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	RI2ROVOL [2:0]	101 (-15dB)	RINPUT3 to Right Output Mixer Volume 000 = 0dB ...(3dB steps) 111 = -21dB
	7	RB2RO	0	Right Input Boost Mixer to Right Output Mixer 0 = Disable (Mute) 1 = Enable Path
R46 (2Eh) Bypass (2)	6:4	RB2ROVOL [2:0]	101 (-15dB)	Right Input Boost Mixer to Right Output Mixer Volume 000 = 0dB ...(3dB steps) 111 = -21dB

**Table 22 Left and Right Output Mixer Mute and Volume Control**

The mono output mixer can output, left, right, left+right or a buffered VMID. 0dB or 6dB attenuation is selectable using MOUTVOL register bit. It is recommended to attenuate a mono mix of left and right channels by 6dB in order to prevent clipping. This attenuation control (MOUTVOL) should not be modified while OUT3 is enabled as this may cause an audible click noise.

寄存器地址	位	标签	默认值	描述
R34 (22h) 左声道输出 混频器控制	8	LD2LO	0	左DAC至左声道输出混频器 0 = 禁用 (静音) 1 = 启用路径
	7	LI2LO	0	LINPUT3至左声道输出混频器 0 = 禁用 (静音) 1 = 启用路径
	6:4	左输入3至左输出混频器音量 [2:0]	101 (-15dB)	LINPUT3至左声道输出混频器音量 000 = 0dB ... (3dB步进) 111 = -21dB
R45 (2Dh) 旁路控制(1)	7	LB2LO	0	左输入升压混频器至左声道输出 混频器 0 = 禁用 (静音) 1 = 启用路径
	6:4	LB2LOVOL [2:0]	101 (-15dB)	左输入升压混频器至左声道输出混频器音量 000 = 0分贝 ... (3分贝步进) 111 = -21分贝
R37 (25h) 右输出混频器控制	8	RD2RO	0	右DAC至右输出混频器 0 = 禁用 (静音) 1 = 启用路径
	7	RI2RO	0	右输入3至右输出混频器 0 = 禁用 (静音) 1 = 启用路径
	6:4	RI2ROVOL [2:0]	101 (-15dB)	右输入3至右输出混频器音量 000 = 0分贝 ... (3分贝步进) 111 = -21分贝
R46 (2Eh) 旁路(2)	7	RB2RO	0	右输入升压混频器至右输出混频器 0 = 禁用 (静音) 1 = 启用路径
	6:4	RB2ROVOL [2:0]	101 (-15dB)	右输入升压混频器至右输出混频器音量 000 = 0分贝 .. . (3分贝 步进) 111 = -21分贝

表22 左右输出混频器静音及音量控制

单声道输出混音器可输出左声道、右声道、左+右声道混合信号或缓冲后的VMID信号。通过MOUTVOL寄存器位可选择0分贝或6分贝衰减。建议对左右声道的混合信号采用6分贝衰减以防止信号削波。在OUT3启用状态下请勿修改此衰减控制(MOUTVOL)，否则可能产生可闻的咔嗒噪声。

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R38 (26h) Mono Out Mix (1)	7	L2MO	0	Left Output Mixer to Mono Output Mixer Control 0 = Left channel mix disabled 1 = Left channel mix enabled
R39 (27h) Mono Out Mix (2)	7	R2MO	0	Right Output Mixer to Mono Output Mixer Control 0 = Right channel mix disabled 1 = Right channel mix enabled
R42 (2Ah) Mono Out Volume	6	MOUTVOL	1	Mono Output Mixer Volume Control 0 = 0dB 1 = -6dB

**Table 23 Output Mixer Enable Control**

When left and right inputs to the mono mixer are both disabled, the mono mixer will output VMID.

## ANALOGUE OUTPUTS

### HP\_L AND HP\_R OUTPUTS

The HP\_L and HP\_R pins can drive a 16Ω or 32Ω headphone or a line output (see Headphone Output and Line Output sections, respectively). The signal volume on HP\_L and HP\_R can be independently adjusted under software control by writing to LOUT1VOL and ROUT1VOL, respectively. Note that gains over 0dB may cause clipping if the signal is large. Any gain setting below 0101111 (minimum) mutes the output driver. The corresponding output pin remains at the same DC level (the reference voltage on the VREF pin), so that no click noise is produced when muting or un-muting.

A zero cross detect on the analogue output may also be enabled when changing the gain setting to minimize audible clicks and zipper noise as the gain updates. If zero cross is enabled a timeout is also available to update the gain if a zero cross does not occur. This function may be enabled by setting TOEN in register R23 (17h). The timeout period is set by TOCLKSEL. Note: SYSCLK must be enabled to use this function.

寄存器地址	位	标签	默认值	描述
R38 (26h) 单声道输出混频器 (1)	7	L2MO	0	左声道输出混频器至单声道输出混频器控制 0 = 左声道混频禁用 1 = 左声道混频启用
R39 (27h) 单声道输出混频器 (2)	7	R2MO	0	右输出混频器至单声道输出混频器控制 0 = 右声道混音禁用 1 = 右声道混频启用
R42 (2Ah) 单声道输出音量	6	主输出音量	1	单声道输出混频器音量控制 0 = 0分贝 1 = -6分贝

表23 输出混频器使能控制

当单声道混频器的左右输入均被禁用时，混频器将输出VMID电压。

## 模拟输出

### HP\_L与HP\_R输出

HP\_L和HP\_R引脚可驱动16Ω或32Ω耳机或线路输出（分别参见耳机输出和线路输出章节）。通过软件分别写入LOUT1VOL（左输出1音量）和ROUT1VOL（右输出1音量）寄存器，可独立调节HP\_L和HP\_R的信号音量。注意：若信号幅度较大，超过0分贝的增益可能导致削波。任何低于0101111（最小值）的增益设置将静音输出驱动。对应输出引脚保持相同直流电平（VREF引脚参考电压），从而实现静音/取消静音时的无爆音操作。

在改变增益设置时，可启用模拟输出的零交叉检测功能以最小化增益更新时的可闻咔嗒声和拉链噪声。若启用零交叉检测，当未检测到零交叉时可设置超时强制更新增益。此功能可通过设置R23（17h）寄存器中的TOEN位启用。超时周期由TOCLKSEL设置。注意：使用此功能需使能SYSCLK。

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) LOUT1 Volume	8	OUT1VU	0	Headphone Volume Update 0 = Store LOUT1VOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LOUT1VOL, right = intermediate latch)
	7	LO1ZC	0	Left zero cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	6:0	LOUT1VOL [6:0]	0000000 (MUTE)	LOUT1 Volume 1111111 = +6dB ... 1dB steps down to 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE
R3 (03h) ROUT1 Volume	8	OUT1VU	0	Headphone Volume Update 0 = Store ROUT1VOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = ROUT1VOL)
	7	RO1ZC	0	Right zero cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	6:0	ROUT1VOL [6:0]	0000000 (MUTE)	ROUT1 Volume Similar to LOUT1VOL

**Table 24 LOUT1/ROUT1 Volume Control**

See "Volume Updates" for more information on volume update bits, zero cross and timeout operation.

#### CLASS D SPEAKER OUTPUTS

The SPK\_LP/SPK\_LN and SPK\_RP/SPK\_RN output pins are class D speaker drivers. Each pair is independently controlled and can drive an 8Ω BTL speaker (see Speaker Output section). Output mixer volume is relative to AVDD, while an additional boost stage is available to accommodate higher SPKVDD1/SPKVDD2 supply voltages. This allows AVDD to be run at a lower voltage to save power, while maximum output power can be delivered to the load, utilising the full range of SPKVDD1/SPKVDD2. Note that the BTL speaker connection provides an additional +6dB gain at the output.

寄存器地址	位	标签	默认值	描述
R2 (02h) 左输出1 音量	8	OUT1VU	0	耳机音量更新 0 = 将左输出1音量存储在中间锁存器（无增益变化）1 = 更新左右声道增益（左声道=左输出1音量，右声道=中间锁存器值）
	7	LO1ZC	0	左声道零交叉使能 0 = 立即改变增益 1 = 仅在零交叉时改变增益
	6:0	LOUT1VOL [6:0]	0000000 (静音)	左输出1音量 1 111111 = +6分贝 ... 以1分贝为步长 递减至0110000 = -73分贝 0101111至0000000 = 模拟静音
R3 (03h) 右输出1 音量	8	OUT1VU	0	耳机音量更新 0 = 将右输出1音量存储至中间锁存器（无增益变化）1 = 更新左右声道增益（左声道=中间锁存器值，右声道=右输出1音量值）
	7	RO1ZC	0	右声道零交叉使能 0 = 立即改变增益 1 = 仅在零交叉时改变增益
	6:0	右输出1音量 [6:0]	0000000 (静音)	右输出1音量 与左输出1音量控制类似

表24 左输出1/右输出1音量控制

有关音量更新位、零交叉和超时操作的详细信息，请参阅“音量更新”章节。

#### D类扬声器输出

SPK\_LP/SPK\_LN和SPK\_RP/SPK\_RN输出引脚为D类扬声器驱动器。每对输出可独立控制，能够驱动8ΩBTL扬声器（详见扬声器输出章节）。输出混音器音量以AVDD为基准，同时配置额外升压级以适配更高的SPKVDD1/SPKVDD2供电电压。这使得AVDD可在更低电压下运行以节省功耗，同时利用SPKVDD1/SPKVDD2的全电压范围向负载提供最大输出功率。需注意BTL扬声器连接方式可在输出端提供额外的+6dB增益。

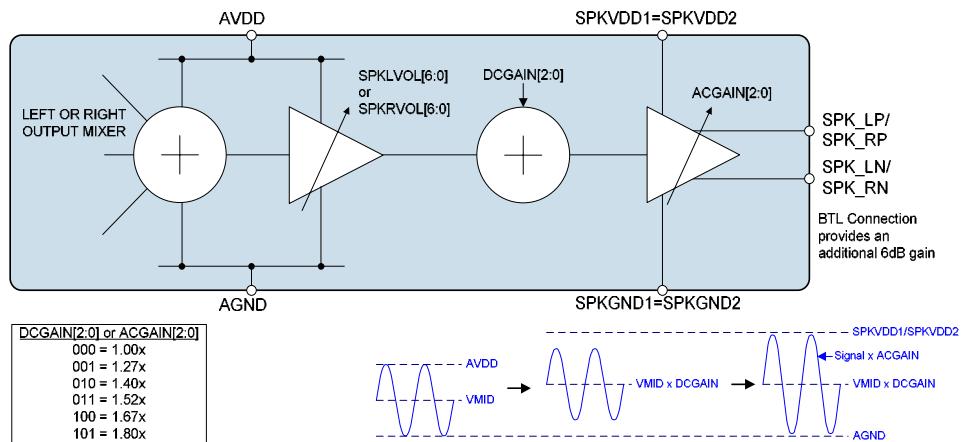


Figure 14 Speaker Boost Operation

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h) Left Speaker Volume	6:0	SPKLVOL [6:0]	0000000 (MUTE)	SPK_LP/SPK_LN Volume 1111111 = +6dB ... 1dB steps down to 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE
	7	SPKLZC	0	Left Speaker Zero Cross Enable 1 = Change gain on zero cross only 0 = Change gain immediately
	8	SPKVU	0	Speaker Volume Update 0 = Store SPKLVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = SPKLVOL, right = intermediate latch)
R41 (29h) Right Speaker Volume	6:0	SPKRVOL [6:0]	0000000 (MUTE)	SPK_RP/SPK_RN Volume 1111111 = +6dB ... 1dB steps down to 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE
	7	SPKRZC	0	Right Speaker Zero Cross Enable 1 = Change gain on zero cross only 0 = Change gain immediately
	8	SPKVU	0	Speaker Volume Update 0 = Store SPKRVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = SPKRVOL)
R51 (33h) Class D Control (3)	5:3	DCGAIN [2:0]	000 (1.0x)	DC Speaker Boost (Boosts speaker DC output level by up to 1.8 x on left and right channels) 000 = 1.00x boost (+0dB) 001 = 1.27x boost (+2.1dB) 010 = 1.40x boost (+2.9dB) 011 = 1.52x boost (+3.6dB) 100 = 1.67x boost (+4.5dB) 101 = 1.8x boost (+5.1dB) 110 to 111 = Reserved

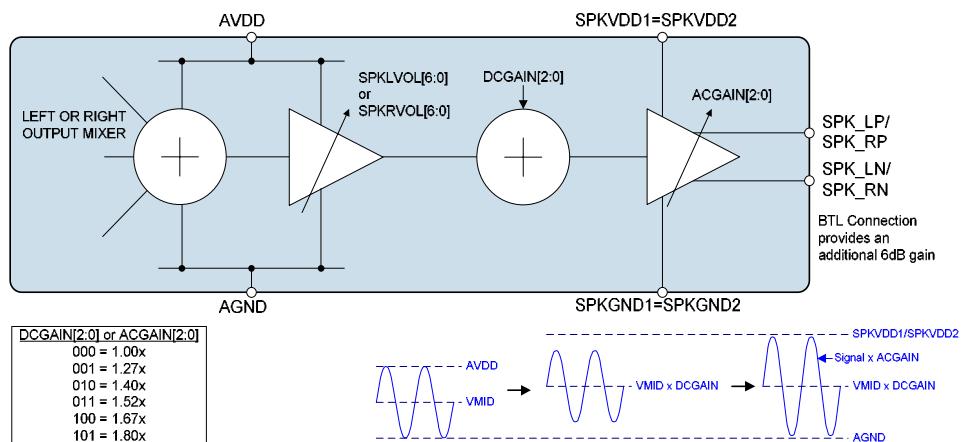


图14 扬声器升压操作

寄存器地址	位	标签	默认值	描述
R40 (28h) 左扬声器音量	6:0	左扬声器音量 [6:0]	0000000 (静音)	SPK_LP/SPK_LN 音量 1111111 = +6分贝 ... 以1分贝步进递减至 0110000 = -73分贝 0101111 至 0000000 = 模拟静音控制
	7	SPKLZC	0	左扬声器零交叉使能 1 = 仅在零交叉时改变增益 0 = 立即改变增益
	8	SPKVU	0	扬声器音量更新 0 = 将 S PKLVOL 存储至中间锁存器 (不改 变增益) 1 = 更新左右 声道增益 (左=SPKLVOL, 右=中间锁 存器)
R41 (29h) 右扬声器音量	6:0	SPKRVOL [6:0]	0000000 (静音)	SPK_RP/SPK_RN 音量 1111111 = +6分贝 ... 以1分贝步进递减至 0110000 = -73分贝 0101111 至 0000000 = 模拟静音控制
	7	SPKRZC	0	右扬声器零交叉使能 1 = 仅在零交叉时改变增益 0 = 立即改变增益
	8	SPKVU	0	扬声器音量更新控制 0 = 将右扬声器音量存储到中间锁存器 (不改变增益) 1 = 更 新左右声道增益 (左声道=中间锁存器 值, 右声道=当前右扬声器音量 值)
R51 (33h) D类控制寄存器(3)	5:3	直流增益控制 [2:0]	000 (1.0倍)	直流扬声器升压 (提升左右声道直流输出电平, 最高1.8倍) 000 = 1.00倍升压 (+0分贝) 001 = 1.27倍升压 (+2.1分贝) 010 = 1.40倍升压 (+2.9分贝) 011 = 1.52倍升压 (+3.6分贝) 100 = 1.67倍升压 (+4.5分贝) 101 = 1.8倍升压 (+5.1分贝) 1 10至111 = 保留值

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2:0	ACGAIN [2:0]	000 (1.0x)	AC Speaker Boost (Boosts speaker AC output signal by up to 1.8 x on left and right channels) 000 = 1.00x boost (+0dB) 001 = 1.27x boost (+2.1dB) 010 = 1.40x boost (+2.9dB) 011 = 1.52x boost (+3.6dB) 100 = 1.67x boost (+4.5dB) 101 = 1.8x boost (+5.1dB) 110 to 111 = Reserved

**Table 25 SPK\_L/SPK\_R Volume and Speaker Boost Control**

To prevent pop noise, DCGAIN and ACGAIN should not be modified while the speaker outputs are enabled.

To avoid clipping at speaker ground, ACGAIN should not be greater than DCGAIN.

To avoid clipping at speaker supply, SPKVDD1 and SPKVDD2 must be high enough to support the peak output voltage when using DCGAIN and ACGAIN functions. The peak output voltage is  $AVDD^*(DCGAIN+ACGAIN)/2$ .

DCGAIN should normally be set to the same value as ACGAIN.

See "Volume Updates" for more information on volume update bits, zero cross and timeout operation.

See "Class D Speaker Outputs" for more information on class D speaker operation.

### OUT3 OUTPUT

The OUT3 pin can drive a  $16\Omega$  or  $32\Omega$  headphone or a line output or be used as a pseudo-ground for capless headphone drive (see Headphone Output section). It can also drive out a mono mix of left and right output mixers (See Output Signal Path).

寄存器地址	位	标签	默认值	描述
	2:0	交流增益控制 [2:0]	000 (1.0倍)	交流扬声器升压 (提升左右声道交流输出信号, 最高1.8倍) 000 = 1.00倍升压 (+0分贝) 001 = 1.27倍升压 (+2.1分贝) 010 = 1.40倍升压 (+2.9分贝) 011 = 1.52倍升压 (+3.6分贝) 100 = 1.67倍升压 (+4.5分贝) 101 = 1.8倍升压 (+5.1分贝) 1至111 = 保留值

表25 SPK\_L/SPK\_R音量及扬声器升压电路控制

为防止爆音噪声, 在启用扬声器输出时不应修改直流增益控制(DCGAIN)和交流增益(ACGAIN)。

为避免扬声器接地端出现削波, 交流增益(ACGAIN)不应大于直流增益控制(DCGAIN)。

为避免扬声器供电端出现削波, 当使用直流增益控制(DCGAIN)和交流增益(ACGAIN)功能时, SPKVDD1和SPKVDD2必须足够高以支持峰值输出电压。峰值输出电压为AVDD\*(DCGAIN+ACGAIN)/2。

直流增益控制(DCGAIN)通常应设置为与交流增益(ACGAIN)相同的值。

有关音量更新位、零交叉和超时操作的详细信息, 请参阅"音量更新"章节。

有关D类扬声器工作的更多信息, 请参见「D类扬声器输出」章节。

### OUT3输出

OUT3引脚可驱动16Ω或32Ω耳机或线路输出, 也可用作无电容耳机驱动的伪地 (参见耳机输出部分)。该引脚还可输出左右声道混频后的单声道信号 (参见输出信号路径)。

## ENABLING THE OUTPUTS

Each analogue output of the WM8960 can be independently enabled or disabled. The analogue mixer associated with each output is powered on or off along with the output pin. All outputs are disabled by default. To save power, unused outputs should remain disabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R26 (1Ah) Power Management (2)	6	LOUT1	0	LOUT1 Output Enable
	5	ROUT1	0	ROUT1 Output Enable
	4	SPKL	0	SPK_LP and SPK_LN Volume Control Enable
	3	SPKR	0	SPK_RP and SPK_RN Volume Control Enable
	1	OUT3	0	OUT3 Enable
R49 (31h) Class D Control (1)	7:6	SPK_OP_EN [1:0]	00	Enable Class D Speaker Outputs 00 = Off 01 = Left speaker only 10 = Right speaker only 11 = Left and right speakers enabled
Note: All "Enable" bits are 1 = ON, 0 = OFF				

Table 26 Analogue Output Control

The speaker output enable bits SPK\_OP\_EN[1:0] should not be enabled until there is a valid switching clock to drive the class D outputs. This means that SYCLK must be active, and DCLKDIV set to an appropriate value to produce a class D clock of between 700kHz and 800kHz for best performance (See "Class D Speaker Outputs" and "Clocking and Sample Rates" sections for more information).

Whenever an analogue output is disabled, it remains connected to VREF through a resistor. This helps to prevent pop noise when the output is re-enabled. The resistance between VREF and each output can be controlled using the VROI bit in register 27. If a high impedance is desired for disabled outputs, VROI can then be set to 1, increasing the resistance to about 20kΩ.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R27 (1Bh) Additional (1)	6	VROI	0	VREF to Analogue Output Resistance (Disabled Outputs) 0 = 500Ω VMID to output 1 = 20kΩ VMID to output

Table 27 Disabled Outputs to VREF Resistance

## HEADPHONE OUTPUT

Analogue outputs HP\_L/HP\_R, and OUT3, can drive a 16Ω or 32Ω headphone load, either through DC blocking capacitors, or DC coupled without any capacitor.

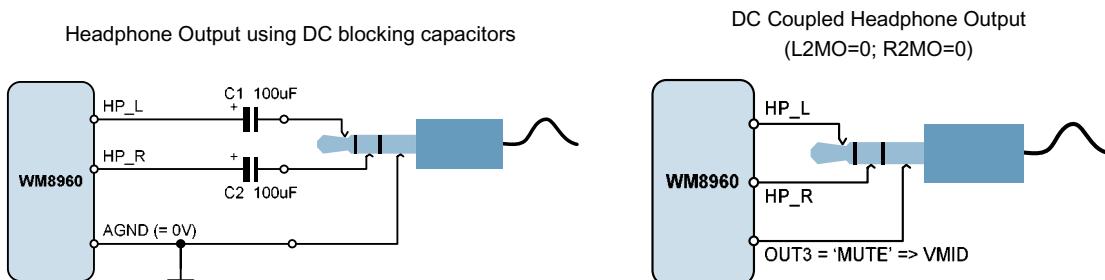


Figure 15 Recommended Headphone Output Configurations

## 启用输出通道

WM8960的每个模拟输出均可独立启用或禁用。与各输出通道关联的模拟混音器会随输出引脚同步开启或关闭。所有输出默认处于禁用状态。为节省功耗，未使用的输出应保持禁用状态。

寄存器地址	位	标签	默认值	描述
R26 (1Ah) 电源管理(2)	6	左输出1	0	LOUT1输出使能
	5	右输出1	0	ROUT1输出使能
	4	SPKL	0	SPK_LP和SPK_LN音量控制启用
	3	SPKR	0	SPK_RP和SPK_RN音量控制启用
	1	OUT3	0	OUT3使能
R49 (31h) D类功放 控制寄存器(1)	7:6	SPK_OP_EN [1:0]	00	启用D类扬声器输出 00 = 关闭 01 = 仅左声道扬声器 10 = 仅右声道扬声器 11 = 左右声道扬声器均启用
注意：所有「使能」位定义均为 1 = 开启，0 = 关闭				

表26 模拟输出控制

扬声器输出使能位SPK\_OP\_EN[1:0]在未获得有效开关时钟驱动D类输出前不应启用。这意味着SYSC\_LK必须处于激活状态，且DCLKDIV需设置为适当值以产生700kHz至800kHz的D类时钟来获得最佳性能（更多信息请参阅“D类扬声器输出”及“时钟与采样率”章节）。

当模拟输出被禁用时，其仍通过电阻器保持与VREF的连接。这有助于防止输出重新启用时产生爆音噪声。可通过寄存器27中的VROI位控制VREF与各输出端之间的电阻值。若希望禁用输出呈现高阻抗状态，可将VROI设为1，此时电阻值将增至约20kΩ。

寄存器地址	位	标签	默认值	描述
R27 (1Bh) 附加(1)	6	VROI	0	VREF至模拟输出电阻 (禁用输出) 0 = 500Ω VMID至输出 1 = 20kΩ VMID至输出

表27 禁用输出至VREF电阻值

## 耳机输出

模拟输出HP\_L/HP\_R和OUT3可驱动16Ω或32Ω的耳机负载，既可通过隔直电容器连接，也可无需电容器直接进行直流耦合。

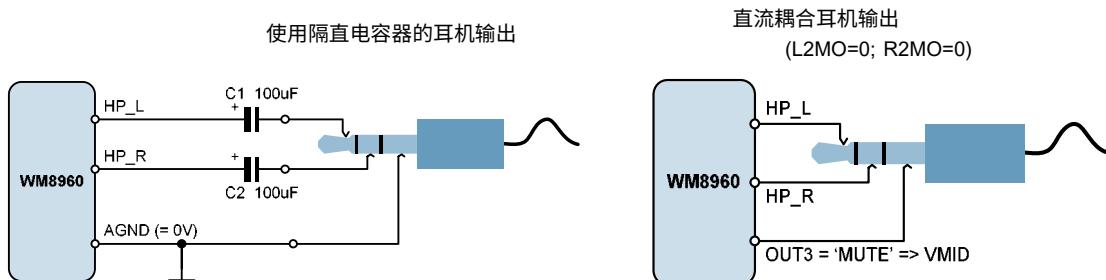


图15 推荐耳机输出配置方案

When DC blocking capacitors are used, then their capacitance and the load resistance together determine the lower cut-off frequency,  $f_c$ . Increasing the capacitance lowers  $f_c$ , improving the bass response. Smaller capacitance values will diminish the bass response. Assuming a  $32\Omega$  load and  $C_1, C_2 = 100\mu F$ :

$$f_c = 1 / 2\pi R_L C_1 = 1 / (2\pi \times 32\Omega \times 100\mu F) = 50 \text{ Hz}$$

In the DC coupled configuration, the headphone "ground" is connected to the OUT3 pin, which must be enabled by setting OUT3 = 1 and muted by setting L2MO=0 and R2MO=0. As the OUT3 pin produces a DC voltage of AVDD/2 (=VREF), there is no DC offset between HP\_L/HP\_R and OUT3, and therefore no DC blocking capacitors are required. This saves space and material cost in portable applications.

It is recommended to connect the DC coupled headphone outputs only to headphones, and not to the line input of another device. Although the built-in short circuit protection will prevent any damage to the headphone outputs, such a connection may be noisy, and may not function properly if the other device is grounded.

## CLASS D SPEAKER OUTPUTS

The class D speaker outputs SPK\_LN/SPK\_LP and SPK\_RN/SPK\_RP can drive 1W into  $8\Omega$  BTL speakers. Class D outputs reduce power consumption and maximise efficiency by reducing power dissipated in the output drivers, delivering most of the power directly to the load. This is achieved by pulse width modulation (PWM) of a high frequency square wave, allowing the audio signal level to be set by controlling the pulse width. The frequency of the output waveform is controlled by DCLKDIV, and is derived from SYSCLK.

When the speakers are close to the device (typically less than about 100mm), the internal filtering effects of the speaker can be used. Where signals are routed over longer distances, it is recommended to use additional passive filtering, positioned close to the WM8960, to reduce EMI. See "Applications Information" for more information on EMI reduction.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Clocking (2)	8:6	DCLKDIV	111	Controls clock division from SYSCLK to generate suitable class D clock. 000 = SYSCLK / 1.5 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16
R49 (31h) Class D Control (1)	7:6	SPK_OP_EN [1:0]	00	Enable Class D Speaker Outputs 00 = Off 01 = Left speaker only 10 = Right speaker only 11 = Left and right speakers enabled

Table 28 Class D Control Registers

The class D outputs require a PWM switching clock, which is derived from SYSCLK. This clock should not be altered or disabled while the class D outputs are enabled.

See "Clocking and Sample Rates" for more information.

当使用隔直电容器时，其电容值与负载电阻共同决定低频截止频率 $f_c$ 。增大电容可降低 $f_c$ ，改善低频响应。较小电容值会减弱低频响应。假设 $32\Omega$ 负载且 $C_1 = C_2 = 100\mu F$ 时：

$$f_c = 1 / 2\pi R_L C_1 = 1 / (2\pi \times 32\Omega \times 100\mu F) = 50 \text{ 赫兹}$$

在直流耦合配置中，耳机'地端'连接至OUT3引脚，该引脚需通过设置OUT3=1使能，并通过设定L2MO=0和R2MO=0实现静音控制。由于OUT3引脚会产生AVDD/2(=VREF)的直流电压，HP\_L/HP\_R与OUT3之间不存在直流偏置，因此无需使用隔直电容器。这一特性为便携式应用节省了空间与物料成本。

建议仅将直流耦合耳机输出连接至耳机设备，而非其他设备的线路输入。虽然内置短路保护可防止耳机输出端受损，但此类连接可能产生噪声，且当其他设备接地时可能导致功能异常。

## D类扬声器输出

D类扬声器输出SPK\_LN/SPK\_LP和SPK\_RN/SPK\_RP可驱动 $8\Omega$ 桥接式负载(BTL)扬声器实现1瓦输出功率。通过采用脉宽调制(PWM)技术对高频方波进行调制，D类输出可降低功耗并最大化效率，其原理是通过控制脉冲宽度来设定音频信号电平，从而将大部分功率直接传输至负载而非消耗在输出驱动器中。输出波形频率由数字时钟分频器(DCLKDIV)控制，该时钟源自主系统时钟(SYSCLK)。

当扬声器与设备距离较近时(通常小于约100毫米)，可利用扬声器自身的内部滤波特性。若信号传输距离较长，建议在靠近WM8960的位置增加无源滤波器以降低电磁干扰(EMI)。更多关于EMI抑制的具体措施，请参阅"应用信息"章节。

寄存器地址	位	标签	默认值	描述
R8 (08h) 时钟设置(2)	8:6	数字时钟分频器	111	控制从SYSCLK分频以生成合适的D类时钟。 000 = SYSCLK / 1.5 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16
R49 (31h) D类功放 控制寄存器(1)	7:6	SPK_OP_EN [1:0]	00	启用D类扬声器输出 00 = 关闭 01 = 仅左声道扬声器 10 = 仅右声道扬声器 11 = 左右声道扬声器均启用

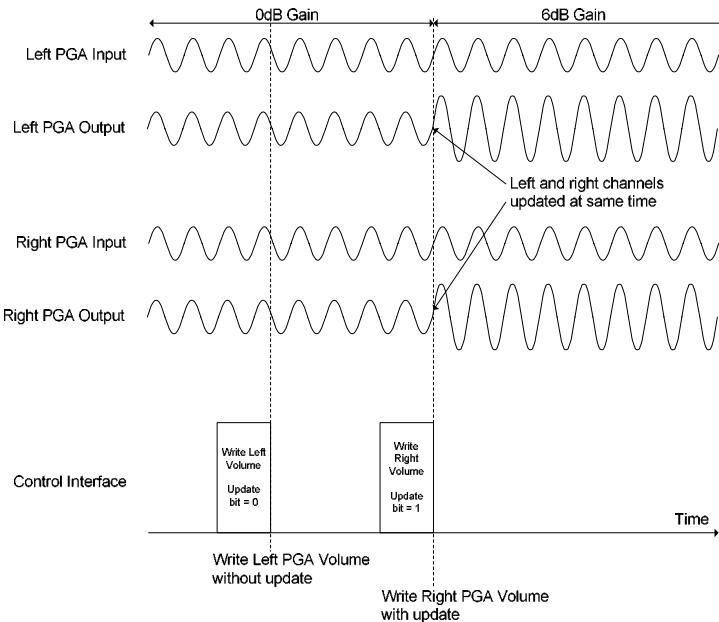
表28 D类控制寄存器

D类输出需要基于SYSCLK生成的PWM开关时钟。在D类输出使能状态下，不得修改或禁用此时钟。

更多信息请参见"时钟与采样率"章节。

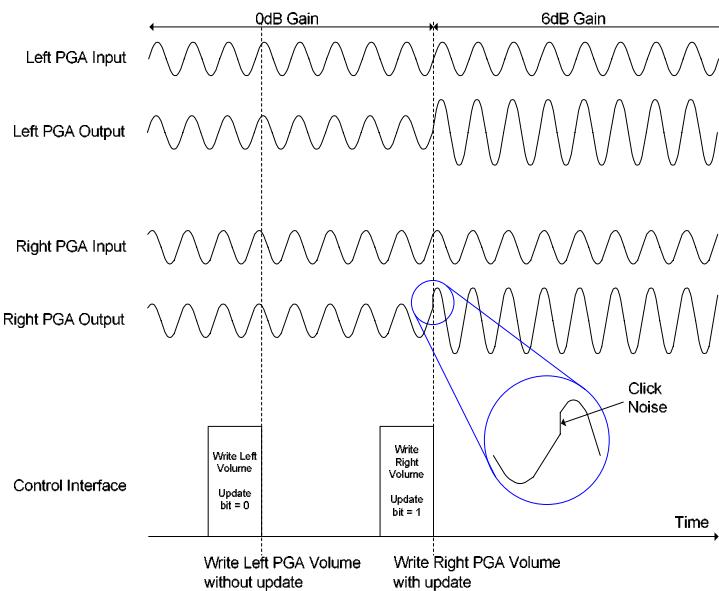
## VOLUME UPDATES

Volume settings will not be applied to input or output PGAs until a '1' is written to one of the update bits (IPVU, OUT1VU, SPKVU bits). This is to allow left and right channels to be updated at the same time, as shown in Figure 16.



**Figure 16 Simultaneous Left and Right Volume Updates**

If the volume is adjusted while the signal is a non-zero value, an audible click can occur as shown in Figure 17.



**Figure 17 Click Noise During Volume Update**

In order to prevent this click noise, a zero cross function is provided. When enabled, this will cause the PGA volume to update only when a zero crossing occurs, minimising click noise as shown in Figure 18.

## 音量更新机制

音量设置需在对应更新位(IPVU/OUT1VU/SPKVU)写入'1'后才会应用于输入/输出的可编程增益放大器。此机制可确保左右声道同步更新，具体时序如图16所示。

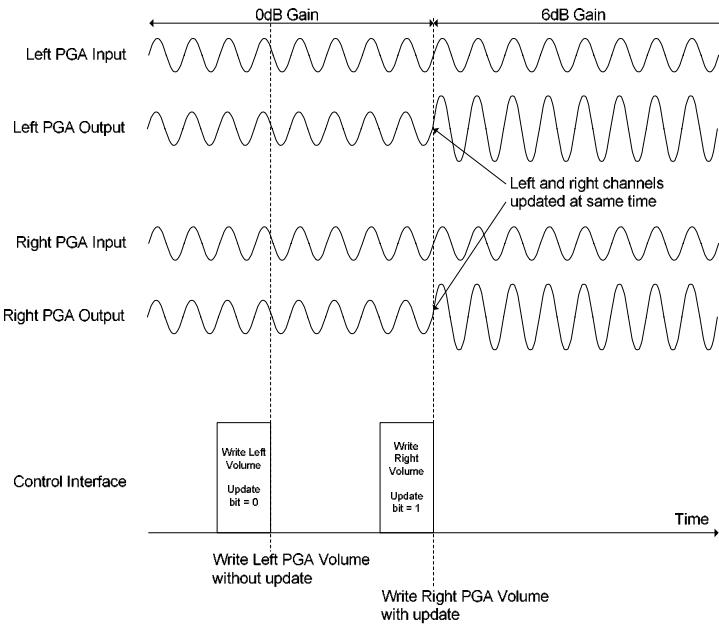


图16 左右声道音量同步更新

当信号处于非零值时进行音量调节，可能产生如图17所示的可闻咔嗒声。

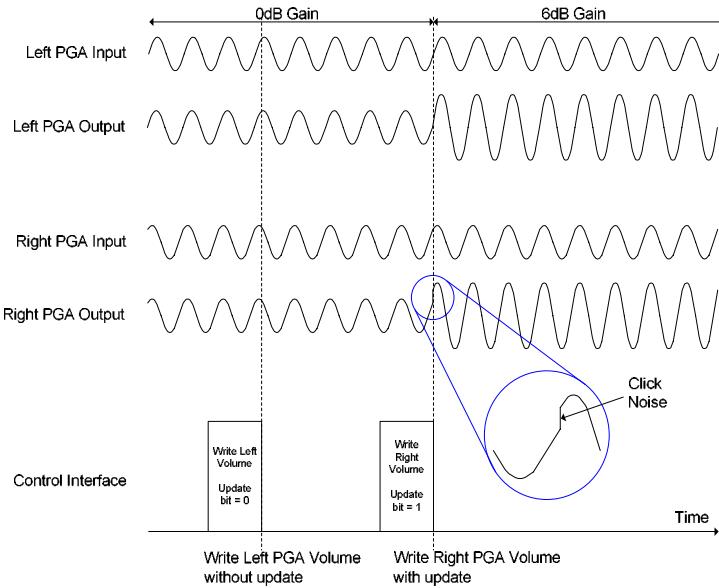
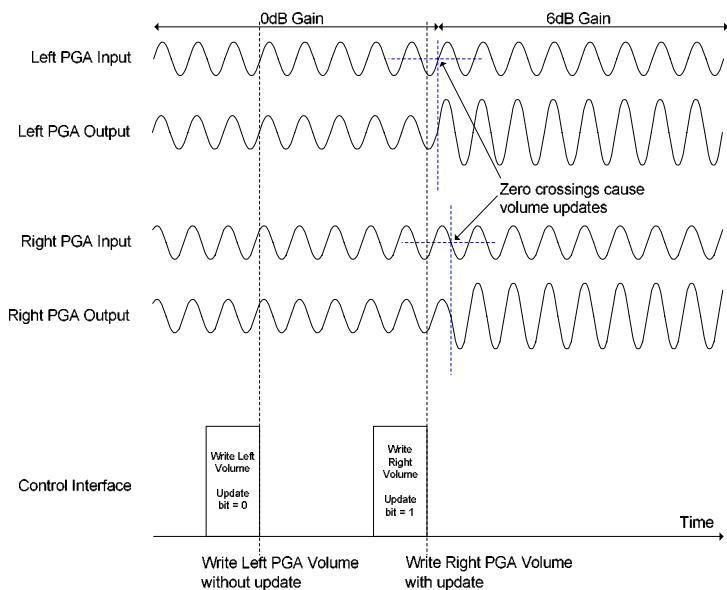
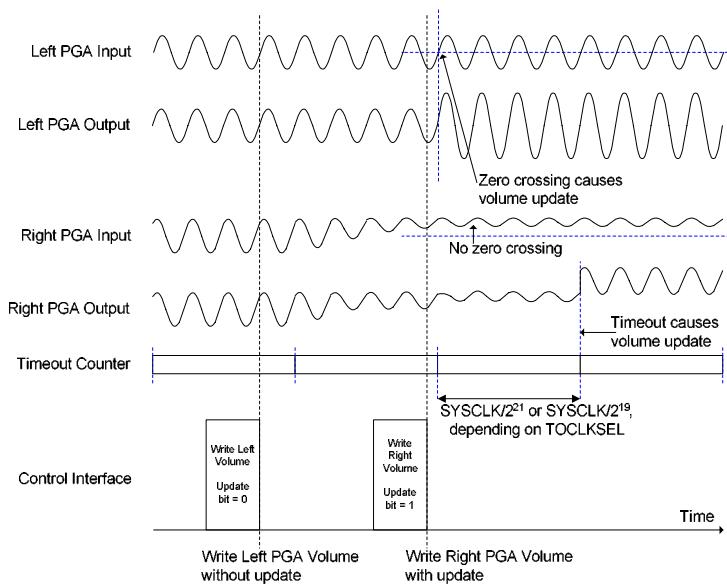


图17 音量更新期间的咔嗒噪声

为防止此类咔嗒噪声，本器件提供过零检测功能。启用该功能后，PGA可编程增益放大器仅在信号过零时更新音量值，如图18所示可有效抑制咔嗒噪声。

**Figure 18 Volume Update Using Zero Cross Detection**

If there is a long period where no zero-crossing occurs, a timeout circuit in the WM8960 will automatically update the volume. The volume updates will occur between one and two timeout periods, depending on when the volume update bit is set as shown in Figure 19. The TOEN register bit must be set to enable this timeout function. The timeout period is set by TOCLKSEL.

**Figure 19 Volume Update after Timeout**

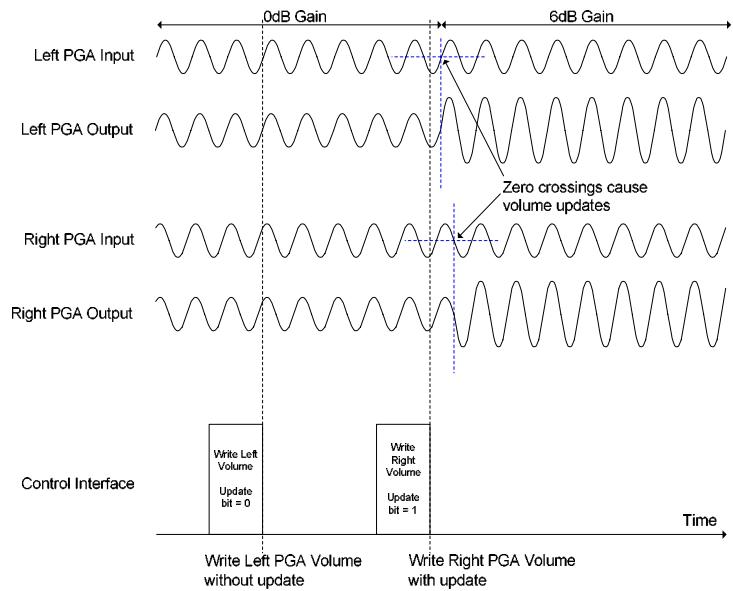


图18 采用过零检测的音量更新

若长时间未出现过零信号，WM8960内置的超时电路将自动执行音量更新。如图19所示，音量更新将在一到两个超时周期内完成（具体取决于音量更新位的设置时序）。需设置TOEN寄存器位使能此超时功能，超时周期由TOCLKSEL设定。

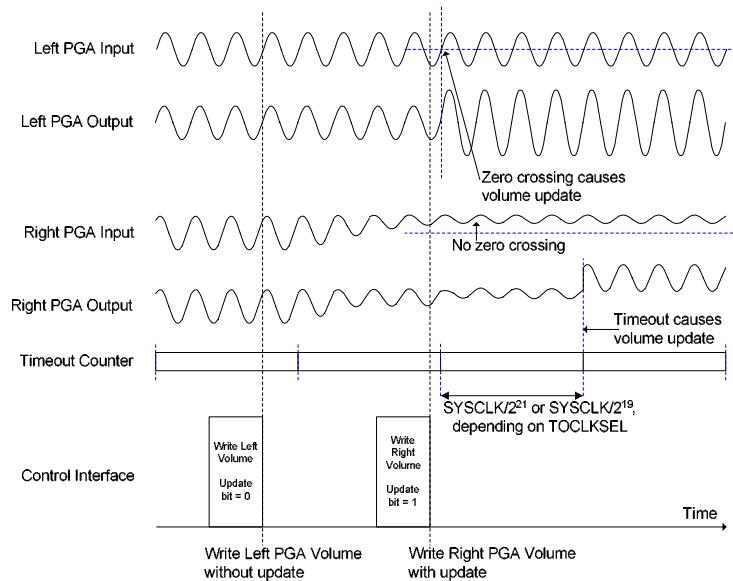


图19 超时后的音量更新

## HEADPHONE JACK DETECT

The ADCLRC/GPIO1, LINPUT3/JD2 and RINPUT3/JD3 pins can be selected as headphone jack detect inputs to automatically disable the speaker output and enable the headphone output e.g. when a headphone is plugged into a jack socket. In this mode, enabled by setting HPSWEN, the headphone detect input pin switches between headphone and speaker outputs (e.g. when the pin is connected to a mechanical switch in the headphone socket to detect plug-in). The HPSEL[1:0] bits select the input pin used for this function. The HPSWPOL bit reverses the pin's polarity. Note that the LOUT1, ROUT1, SPKL and SPKR bits in register 26 must also be set for headphone and speaker output (see Table 29 and Table 30).

TOEN must also be set to enable the clock which is used for de-bouncing the jack detect input. TOCLKSEL selects a fast or slow de-bounce period. Note that SYCLK must be enabled to use this function.

When using capless mode, the OUT3CAP bit should be enabled so that OUT3 is enabled/disabled at the same time as HP\_L and HP\_R to prevent pop noise.

The debounced headphone detect signal can also be output to the ADCLRC/GPIO1 pin (See GPIO section). This function is not available when using GPIO1 as an input or as ADCLRC.

When using the ADCLRC/GPIO1 pin as a headphone detect input, the ALRCGPIO register bit needs to be set to 1. In this mode, DACLRC is used for both ADC and DAC frame clocks. (See GPIO section for more information)

### Note:

When LINPUT3 or RINPUT3 is used as the headphone detect input, the thresholds become CMOS levels (0.3 AVDD / 0.7 AVDD).

HPSWEN	HPSWPOL	HEADPHONE DETECT PIN (LINPUT3/JD2, RINPUT3/JD3 OR ADCLRC/GPIO1)	L/ROUT1 (AND OUT3 IN CAPLESS MODE) (REG. 26)	SPKL/R (REG. 26)	HEADPHONE ENABLED (AND OUT3 IN CAPLESS MODE)	SPEAKER ENABLED
0	X	X	0	0	no	no
0	X	X	0	1	no	yes
0	X	X	1	0	yes	no
0	X	X	1	1	yes	yes
1	0	0	X	0	no	no
1	0	0	X	1	no	yes
1	0	1	0	X	no	no
1	0	1	1	X	yes	no
1	1	0	0	X	no	no
1	1	0	1	X	yes	no
1	1	1	X	0	no	no
1	1	1	X	1	no	yes

Table 29 Headphone Jack Detect Operation

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) Additional Control (2)	6	HPSWEN	0	Headphone Switch Enable 0 = Headphone switch disabled 1 = Headphone switch enabled
	5	HPSWPOL	0	Headphone Switch Polarity 0 = HPDETECT high = headphone 1 = HPDETECT high = speaker

## 耳机插孔检测

ADCLRC/GPIO1、LINPUT3/JD2和RINPUT3/JD3引脚可配置为耳机插孔检测输入，用于在检测到耳机插入插孔时自动禁用扬声器输出并启用耳机输出（例如当耳机插入插孔插座时）。通过设置HPSWE N使能该模式后，耳机检测输入引脚将在耳机和扬声器输出之间切换（例如当引脚连接至耳机插座中的机械开关以检测插入状态时）。HPSEL[1:0]位用于选择实现此功能的输入引脚，HPSWPOL位可反转引脚的极性。需注意，寄存器26中的LOUT1、ROUT1、SPKL和SPKR位也必须设置才能启用耳机和扬声器输出（参见表29和表30）。

同时必须设置TOEN以启用用于对插孔检测输入进行去抖动的时钟信号。  
TOCLKSEL选择快速或慢速去抖周期。注意使用此功能时必须启用SYSCLK时钟。

当使用无电容模式时，应启用OUT3CAP位以使OUT3与HP\_L和HP\_R同步启用/禁用，从而防止爆音噪声的产生。

经过去抖处理的耳机检测信号也可输出至ADCLRC/GPIO1引脚（详见GPIO章节）。当GPIO1作为输入或用作ADCLRC时，此功能不可用。

当将ADCLRC/GPIO1引脚用作耳机检测输入时，需将ALRCGPIO寄存器位设置为1。在此模式下，ADCLRC将同时用作ADC和DAC的帧时钟（更多信息请参考GPIO章节）。

### 注意：

当使用LINPUT3或RINPUT3作为耳机检测输入时，其阈值将转为CMOS电平（0.3 AVDD / 0.7 AVDD）。

耳机开关使能	耳机开关极性	耳机检测引脚 (左输入3/J D2、右输入3/J D3 或 ADCLRC/ 通用输入输出端口)	左/右输出1 (及无电容模 式下的OUT3) (寄存器26)	左/右扬声器 (寄存器26)	耳机已启用 (及无电容 模式下的OUT 3)	扬声器已 启用
0	X	X	0	0	否	否
0	X	X	0	1	否	是
0	X	X	1	0	是	否
0	X	X	1	1	是	是
1	0	0	X	0	否	否
1	0	0	X	1	否	是
1	0	1	0	X	否	否
1	0	1	1	X	是	否
1	1	0	0	X	否	否
1	1	0	1	X	是	否
1	1	1	X	0	否	否
1	1	1	X	1	否	是

表29 耳机插孔检测操作

寄存器 地址	位	标签	默认值	描述
R24 (18h) 附加控制 寄存器(2)	6	耳机开关使能	0	耳机开关使能 0 = 耳机开关禁用 1 = 耳机开关使能
	5	耳机开关极性	0	耳机开关极性 0 = HPDETECT高电平表示耳机 1 = HPDETECT高电平表示扬声器

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R27 (1Bh) Additional Control (3)	3	OUT3CAP	0	Capless Mode Headphone Switch Enable 0 = OUT3 unaffected by jack detect events 1 = OUT3 enabled and disabled together with HP_L and HP_R in response to jack detect events
R48 (30h) Additional Control (4)	3:2	HPSEL[1:0]	00	Headphone Switch Input Select 0X = GPIO1 used for jack detect input (Requires ADCLRC pin to be configured as a GPIO) 10 = JD2 used for jack detect input 11 = JD3 used for jack detect input
R23 (17h) Additional Control (1)	0	TOEN	0	Slow Clock Enable (Must be enabled for jack detect de-bounce) 0 = Slow Clock Disabled 1 = Slow Clock Enabled
	1	TOCLKSEL	0	Slow Clock Selection (Used for volume update timeouts and for jack detect debounce) 0 = SYSCLK / $2^{21}$ (Slower Response) 1 = SYSCLK / $2^{19}$ (Faster Response)

Table 30 Headphone Jack Detect

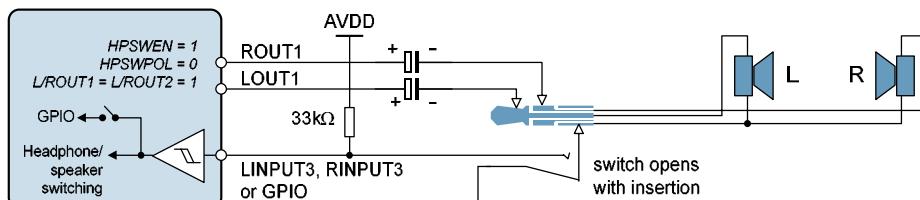


Figure 20 Example Headset Detection Circuit Using Normally-Open Switch

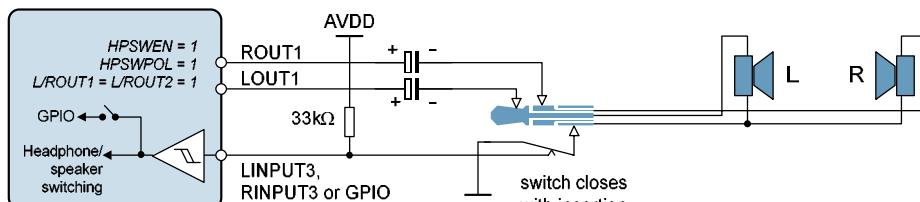


Figure 21 Example Headset Detection Circuit Using Normally-Closed Switch

## THERMAL SHUTDOWN

The speaker and headphone outputs can drive very large currents. To protect the WM8960 from overheating a thermal shutdown circuit is included and is enabled by default. If the device temperature reaches approximately 150°C and the thermal shutdown circuit is enabled (TSDEN = 1; TSENSEN = 1) the speaker and headphone amplifiers (HP\_L, HP\_R, SPK\_LP, SPK\_LN, SPK\_RP, SPK\_RN and OUT3) will be disabled. This feature can be disabled to save power when the device is in standby mode.

TSENSEN must be set to 1 to enable the temperature sensor when using the TSSEN thermal shutdown function. The output of the temperature sensor can also be output to the GPIO1 pin.

寄存器地址	位	标签	默认值	描述
R27 (1Bh) 附加控制 (3)	3	OUT3电容	0	无电容模式耳机开关使能 0 = OUT3 不受插孔检测事件影响 1 = OUT3 随 HP_L 和 HP_R 根据插孔检测事件同步启用/禁用
R48 (30h) 附加控制 (4)	3:2	HPSEL[1:0]	00	耳机开关输入选择 0X = 使用 GPIO1 作为插孔检测输入 (需将 ADCLR_C 引脚配置为 GPIO) 10 = 使用 JD2 作为插孔检测输入 11 = 使用 JD3 作为插孔检测输入
R23 (17h) 附加控制位 (1)	0	超时使能	0	慢时钟使能 (必须启用以实现插孔检测去抖动) 0 = 慢时钟禁用 1 = 慢时钟使能
	1	慢时钟选择	0	慢时钟选择 (用于音量更新超时和插孔检测去抖动) 0 = SYSCLK / 2 <sup>21</sup> (响应较慢) 1 = SYSCLK / 2 <sup>19</sup> (响应较快)

表30 耳机插孔检测

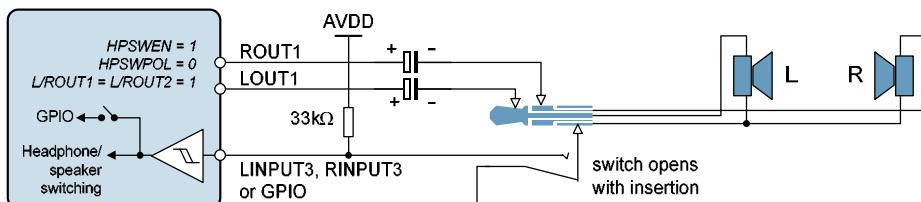


图20 使用常开开关的耳机检测电路示例

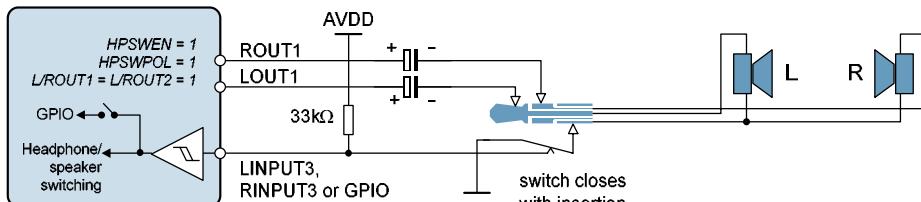


图21 使用常闭开关的耳机检测电路示例

## 热关断保护

扬声器和耳机输出端可驱动极大电流。为防止WM8960过热，芯片默认启用热关断保护电路。当器件温度达到约150°C且热关断保护电路启用时 (TSDEN = 1; TSENSEN = 1)，扬声器和耳机放大器 (HP\_L、HP\_R、SPK\_LP、SPK\_LN、SPK\_RP、SPK\_RN及OUT3) 将被禁用。当器件处于待机模式时，可通过禁用此功能以节省功耗。

使用TSDEN热关断功能时，必须将TSENSEN设为1以启用温度传感器。温度传感器的输出也可通过通用输入输出端口1引脚输出。

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	8	TSDEN	1	Thermal Shutdown Enable 0 = Thermal shutdown disabled 1 = Thermal shutdown enabled (TSENSEN must be enabled for this function to work)
R48 (30h) Additional Control (4)	1	TSENSEN	1	Temperature Sensor Enable 0 = Temperature sensor disabled 1 = Temperature sensor enabled

**Table 31 Thermal Shutdown****GENERAL PURPOSE INPUT/OUTPUT**

The WM8960 has three dual purpose input/output pins.

- LINPUT3/JD2: Analogue input or headphone detect input.
- RINPUT3/JD3: Analogue input or headphone detect input.
- ADCLRC/GPIO1: ADC left/right frame clock or GPIO pin.

The ADCLRC/GPIO1 pin can be configured as a left/right frame clock for the ADC, a headphone detect input, or one of a number of GPIO output functions as shown in Table 32.

The default configuration for the LINPUT3 and RINPUT2 pins is to be analogue inputs. The default configuration for the ADCLRC/GPIO1 pin is to be the ADC left/right frame clock.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h) Audio Interface (2)	6	ALRCGPIO	0	ADCLRC/GPIO1 Pin Function Select 0 = ADCLRC frame clock for ADC 1 = GPIO pin
R48 (30h) Additional Control (4)	6:4	GPIOSEL [2:0]	000	ADCLRC/GPIO1 GPIO Function Select: 000 = Jack detect input 001 = Reserved 010 = Temperature ok 011 = Debounced jack detect output 100 = SYSCLK output 101 = PLL lock 110 = Logic 0 111 = Logic 1
	7	GPIOPOL	0	GPIO Polarity Invert 0 = Non inverted 1 = Inverted
R52 (34h) Clocking (2)	8:6	OPCLKDIV [2:0]	000	SYSCLK Output to GPIO Clock Division ratio 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 5.5 101 = SYSCLK / 6

**Table 32 GPIO Control**

Slow clock must be enabled (TOEN = 1) when using the jack detect function. This slow clock is used to debounce the jack detect input. The debounce period can be selected using TOCLKSEL.

The temperature sensor must be enabled for the "Temperature ok" GPIO output to function properly.

For further details of the Jack detect operation see the Headphone Switch section.

寄存器地址	位	标签	默认值	描述
R23 (17h) 附加控制位 (1)	8	TSDEN	1	热关断使能 0 = 禁用热关断保护 1 = 启用热关断保护 (此功能需同时启用TSENSEN方可生效)
R48 (30h) 附加控制 (4)	1	TSENSEN	1	温度传感器使能 0 = 温度传感器禁用 1 = 温度传感器启用

表31 热关机

## 通用输入/输出

WM8960具有三个双功能输入/输出引脚。

- LINPUT3/JD2：模拟输入或耳机检测输入。
- RINPUT3/JD3：模拟输入或耳机检测输入。
- ADCLRC/GPIO1：ADC左/右帧时钟或GPIO引脚。

ADCLRC/GPIO1引脚可配置为ADC的左右帧时钟、耳机检测输入或表32所示的多项GPIO输出功能之一。

LINPUT3和RINPUT2引脚的默认配置为模拟输入。ADCLRC/GPIO1引脚的默认配置为ADC左右帧时钟。

寄存器地址	位	标签	默认值	描述
R9 (09h) 音频接口寄存器(2)	6	ALRCGPIO	0	ADCLRC/GPIO1引脚功能选择 0 = ADC的ADCLRC帧时钟 1 = 通用输入输出引脚
R48 (30h) 附加控制 (4)	6:4	GPIO选择 [2:0]	000	ADCLRC/GPIO1 GPIO功能选择： 000 = 插孔检测输入 001 = 保留 010 = 温度正常 011 = 去抖动后的插孔检测输出 100 = 系统时钟输出 101 = PLL锁定 110 = 逻辑0 111 = 逻辑1
	7	GPIO极性	0	GPIO极性反转 0 = 不反转 1 = 反转
R52 (34h) 时钟配置(2)	8:6	输出时钟分频 [2:0]	000	系统时钟输出至GPIO的分频比 000 = 系统 时钟 001 = 系统时钟/2 010 = 系统时钟/3 011 = 系统时钟/4 100 = 系统时钟/5.5 101 = 系统时钟/6

表32 GPIO控制

使用插孔检测功能时必须启用慢时钟 (TOEN = 1)。该慢时钟用于对插孔检测输入进行去抖动处理。去抖动周期可通过TOCLKSEL选择。要使“温度正常”GPIO输出正常工作，必须启用温度传感器。

有关插孔检测操作的更多详细信息，请参阅耳机开关部分。

## DIGITAL AUDIO INTERFACE

The digital audio interface is used for inputting DAC data into the WM8960 and outputting ADC data from it. It uses five pins:

- ADCDAT: ADC data output
- ADCLRC: ADC data alignment clock
- DACDAT: DAC data input
- DAACLRC: DAC data alignment clock
- BCLK: Bit clock, for synchronisation

The clock signals BCLK, ADCLRC and DAACLRC can be outputs when the WM8960 operates as a master, or inputs when it is a slave (see Master and Slave Mode Operation, below).

ADCLRC can also be configured as a GPIO pin. In this case, the ADC will use DAACLRC as a frame clock. The ADCLRC/GPIO1 pin function should not be modified while the ADC is enabled.

Four different audio data formats are supported:

- Left justified
- Right justified
- I<sup>2</sup>S
- DSP mode

All four of these modes are MSB first. They are described in Audio Data Formats, below. Refer to the Electrical Characteristic section for timing information.

## MASTER AND SLAVE MODE OPERATION

The WM8960 can be configured as either a master or slave mode device. As a master device the WM8960 generates BCLK, ADCLRC and DAACLRC and thus controls sequencing of the data transfer on ADCDAT and DACDAT. In slave mode, the WM8960 responds with data to clocks it receives over the digital audio interface. The mode can be selected by writing to the MS bit. Master and slave modes are illustrated below.

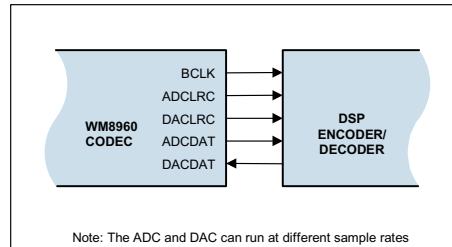


Figure 22 Master Mode

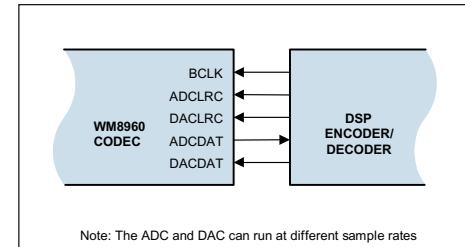


Figure 23 Slave Mode

## OPERATION WITH ADCLRC AS GPIO

When ALRCGPIO=1, the DAACLRC pin is used as a frame clock for ADCs and DACs as shown below. The ADCs and DACs must operate at the same sample rate in this mode. See Table 32 for details of GPIO pin configuration.

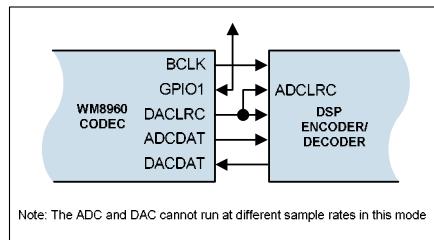


Figure 24 Master Mode with ADCLRC as GPIO

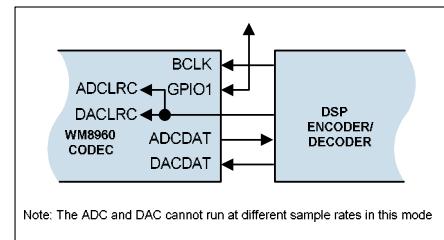


Figure 25 Slave Mode with ADCLRC as GPIO

## 数字音频接口

数字音频接口用于将DAC数据输入WM8960并从中输出ADC数据。该接口使用五个引脚：

- ADCDAT: ADC数据输出
- ADCLRC: ADC数据对齐时钟
- DACDAT: DAC数据输入
- DAACLRC: DAC数据对齐时钟
- BCLK: 位时钟（用于同步）

当WM8960作为主设备工作时，时钟信号BCLK、ADCLRC和DAACLRC可作为输出；当作为从设备工作时则作为输入（详见下文主从模式操作）。

ADCLRC也可配置为GPIO引脚。在此配置下，ADC将使用DAACLRC作为帧时钟。在ADC启用状态下不应修改ADCLRC/GPIO1引脚功能。

支持四种不同的音频数据格式：

- 左对齐格式
- 右对齐格式
- I<sup>2</sup>S
- DSP模式

所有四种模式均采用最高有效位优先(MSB first)传输方式，具体描述详见下文'音频数据格式'章节。时序信息请参考'电气特性'章节。

### 主从模式操作

WM8960可配置为主设备或从设备。作为主设备时，WM8960生成BCLK、ADCLRC和DAACLRC时钟信号，从而控制ADCDAT和DACPAT数据传输的时序。在从模式下，WM8960通过数字音频接口接收外部时钟信号进行数据同步。工作模式可通过设置MS位进行选择。主从模式操作示意图如下所示。

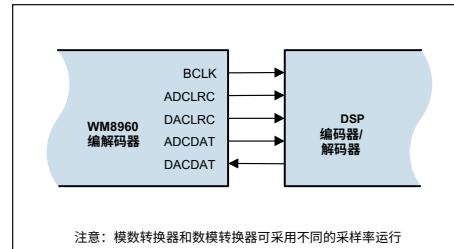


图22 主模式

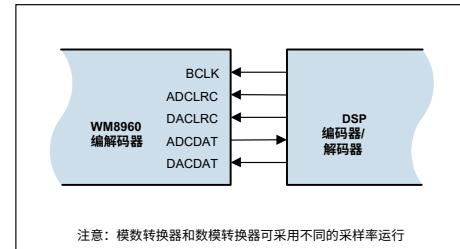


图23 从模式

### ADCLRC作为GPIO的操作模式

当ALRCGPIO=1时，DAACLRC引脚将作为模数转换器(ADC)和数模转换器(DAC)的帧同步时钟使用（如下所示）。在此模式下，ADC和DAC必须保持相同的采样率。GPIO引脚配置详情请参见表32。

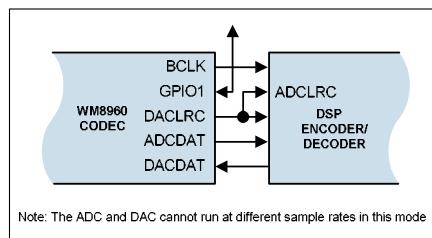


图24 将ADCLRC作为GPIO的主模式

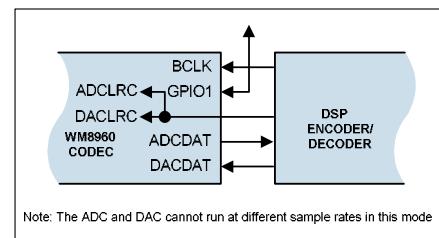


图25 将ADCLRC作为GPIO的从模式

### BCLK DIVIDE

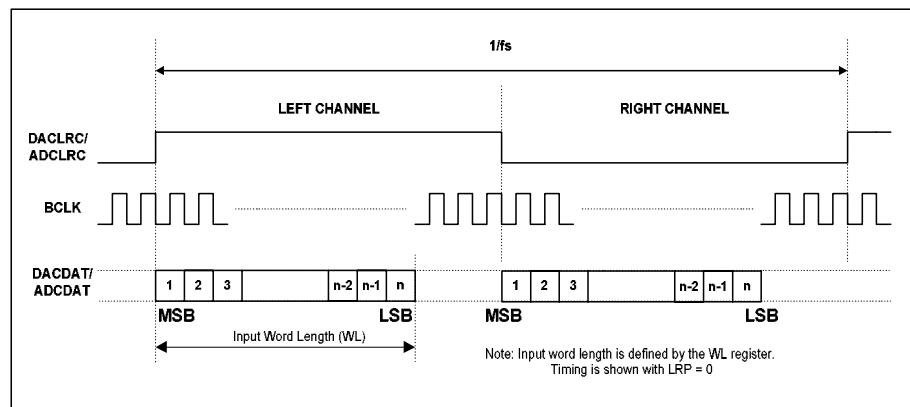
The BCLK frequency in master mode is controlled by BCLKDIV[3:0]. When the ADCs and DACs are operating at different sample rates, BCLKDIV must be set appropriately to support the data rate of whichever is the faster.

Internal clock divide and phase control mechanisms ensure that the BCLK, ADCLRC and DACLR RC edges will occur in a predictable and repeatable position relative to each other and to the data for a given combination of DAC sample rate, ADC sample rate and BCLKDIV settings.

See Clocking and Sample Rates section for more information.

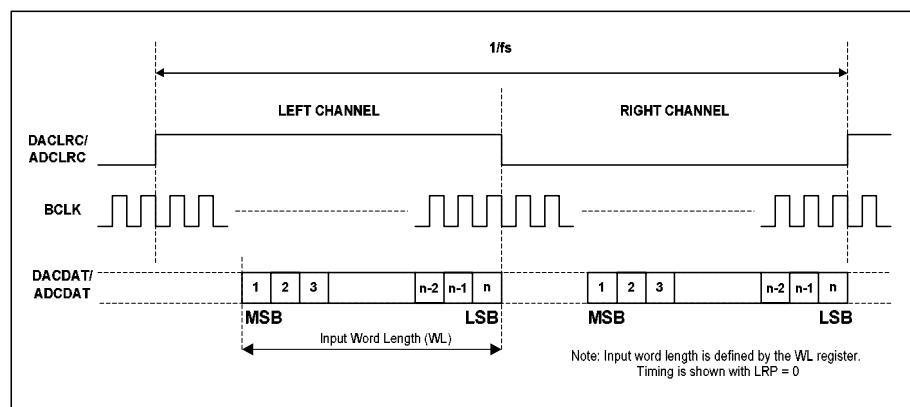
### AUDIO DATA FORMATS

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.



**Figure 26 Left Justified Audio Interface (assuming n-bit word length)**

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.



**Figure 27 Right Justified Audio Interface (assuming n-bit word length)**

In I<sup>2</sup>S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

### BCLK 分频

主模式下的BCLK频率由BCLKDIV[3:0]控制。当模数转换器和数模转换器工作在不同采样率时，必须适当设置BCLKDIV以支持较高速率的数据传输。

内部时钟分频和相位控制机制确保在任何给定的数模转换器采样率、模数转换器采样率和BCLKDIV设置组合下，BCLK、ADCLRC和DACLRC的边沿将保持可预测且可重复的相对时序关系，并与数据对齐。

更多信息请参阅时钟与采样率章节。

### 音频数据格式

在左对齐模式下，MSB（最高有效位）在LRCLK跳变后的第一个BCLK上升沿有效。随后按顺序传输其他位直至LSB（最低有效位）。根据字长、BCLK频率和采样率的不同，在每次LRCLK跳变前可能存在未使用的BCLK周期。

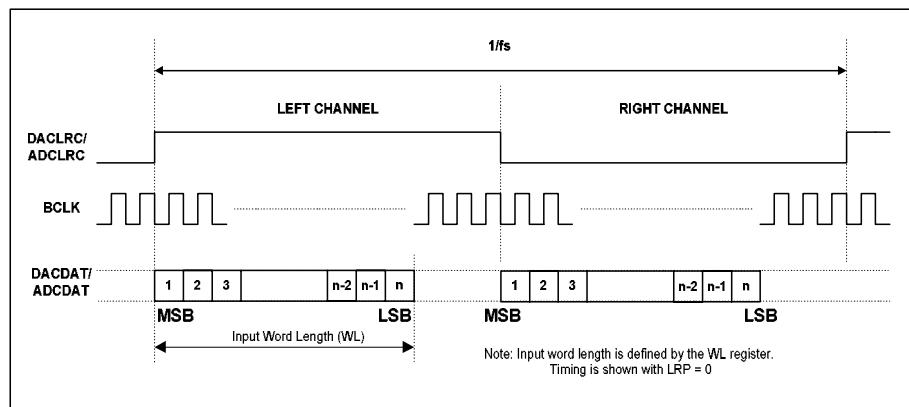


图26 左对齐音频接口（假设字长为n位）

在右对齐模式下，最低有效位（LSB）在LRCLK转换前的最后一个BCLK上升沿有效。其余所有位均在此之前传输（最高有效位优先）。根据字长、BCLK频率和采样率的不同，在每次LRCLK转换后可能存在未使用的BCLK周期。

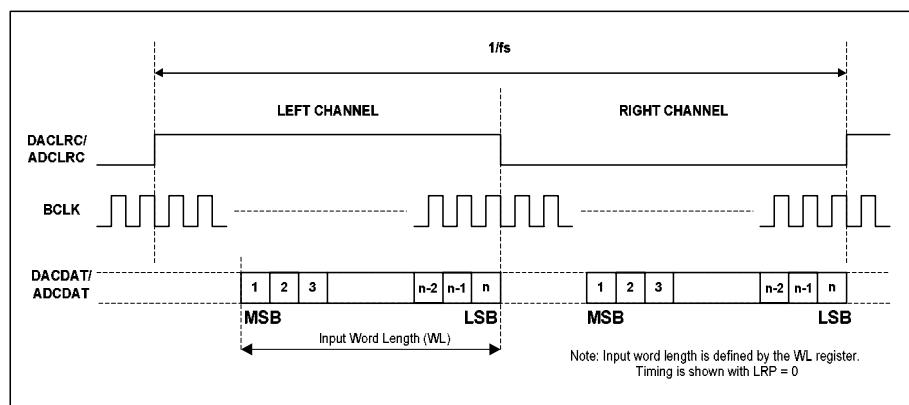
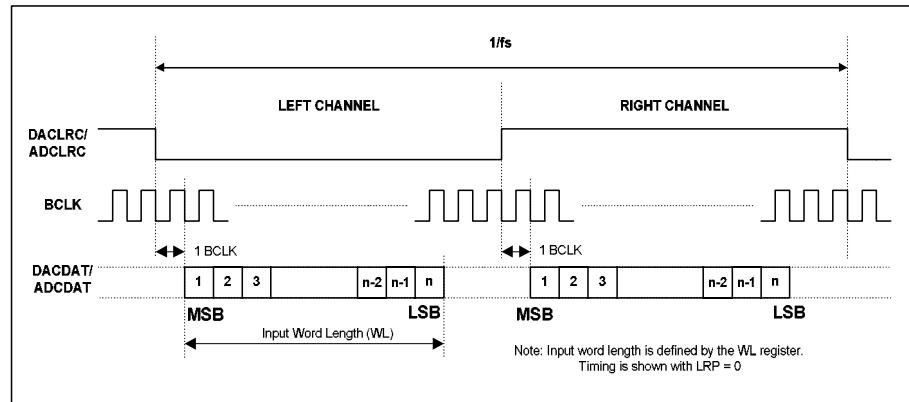


图27 右对齐音频接口（假设字长为n位）

在<sup>2</sup>S模式下，最高有效位（MSB）在LRCLK转换后的第二个BCLK上升沿有效。随后按顺序传输至最低有效位（LSB）。根据字长、BCLK频率和采样率的不同，在一个样本的LSB与下一个样本的MSB之间可能存在未使用的BCLK周期。

Figure 28 I<sup>2</sup>S Justified Audio Interface (assuming n-bit word length)

In DSP/PCM mode, the left channel MSB is available on either the 1<sup>st</sup> (mode B) or 2<sup>nd</sup> (mode A) rising edge of BCLK (selectable by LRP) following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRC output will resemble the frame pulse shown in Figure 29 and Figure 30. In device slave mode, Figure 31 and Figure 32, it is possible to use any length of frame pulse less than  $1/f_s$ , providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

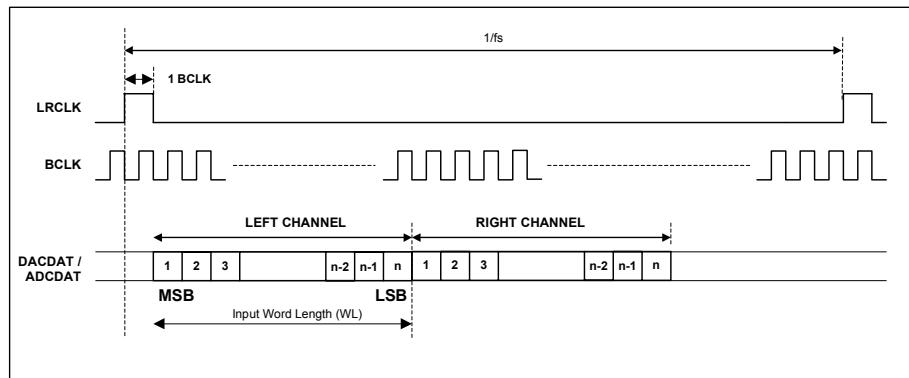


Figure 29 DSP/PCM Mode Audio Interface (mode A, LRP=0, Master)

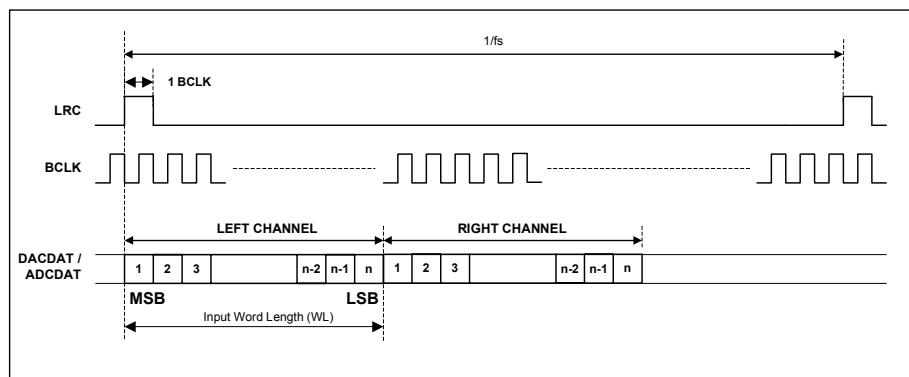
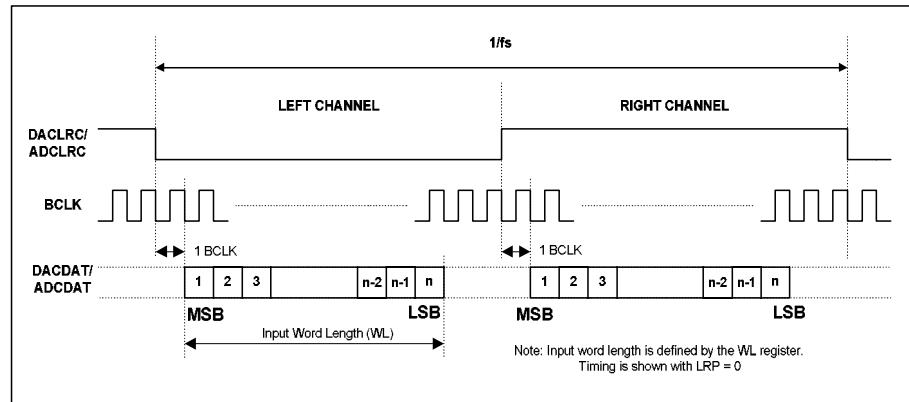


Figure 30 DSP/PCM Mode Audio Interface (mode B, LRP=1, Master)

图28 I<sup>2</sup>S对齐音频接口（假设字长为n位）

在DSP/PCM模式下，左声道最高有效位（MSB）在LRC上升沿后的第1个（模式B）或第2个（模式A）BCLK上升沿有效（通过LRP选择）。右声道数据紧接左声道数据。根据字长、BCLK频率和采样率的不同，在右声道数据的LSB与下一个采样点之间可能存在未使用的BCLK周期。

在设备主模式中，LRC输出将类似于图29和图30所示的帧脉冲。在设备从模式中（图31和图32），可使用任何长度小于1/采样频率的帧脉冲，前提是帧脉冲的下降沿需在下一帧脉冲上升沿前至少一个BCLK周期发生。

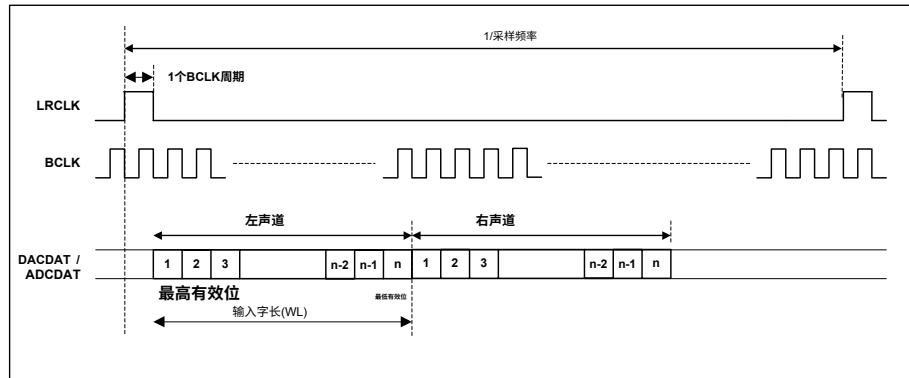


图29 DSP/PCM模式音频接口（模式A, LRP=0, 主模式）

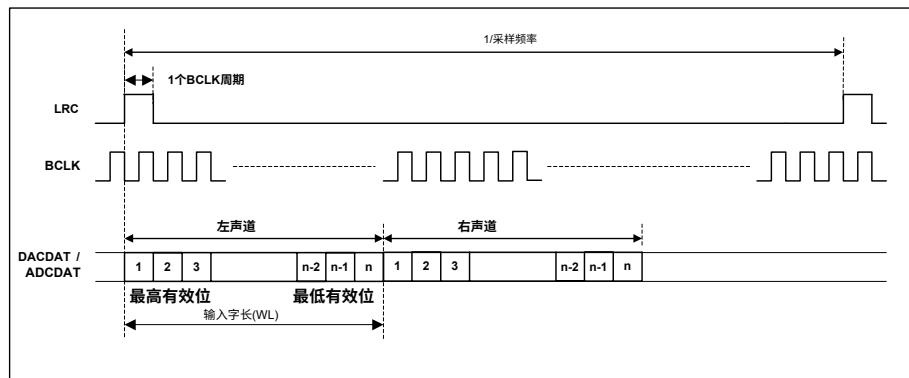


图30 DSP/PCM模式音频接口（模式B, LRP=1, 主模式）

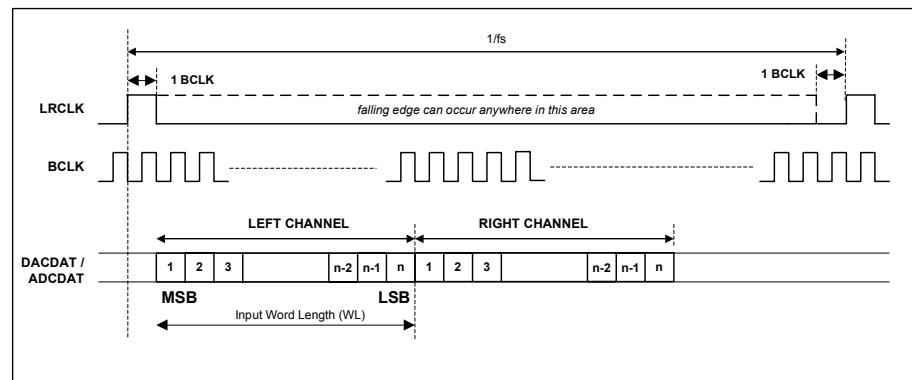


Figure 31 DSP/PCM Mode Audio Interface (mode A, LRP=0, Slave)

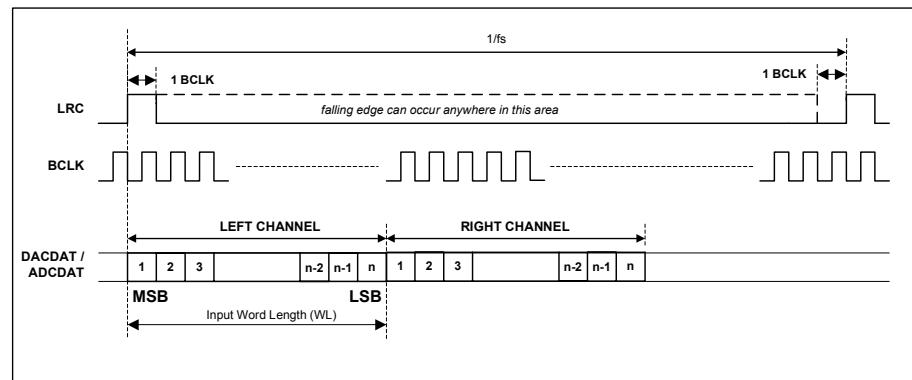


Figure 32 DSP/PCM Mode Audio Interface (mode B, LRP=1, Slave)

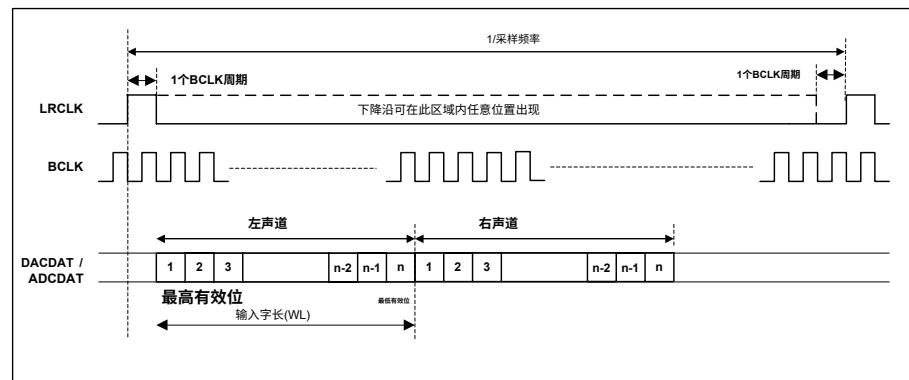


图31 DSP/PCM模式音频接口（模式A，LRP=0，从模式）

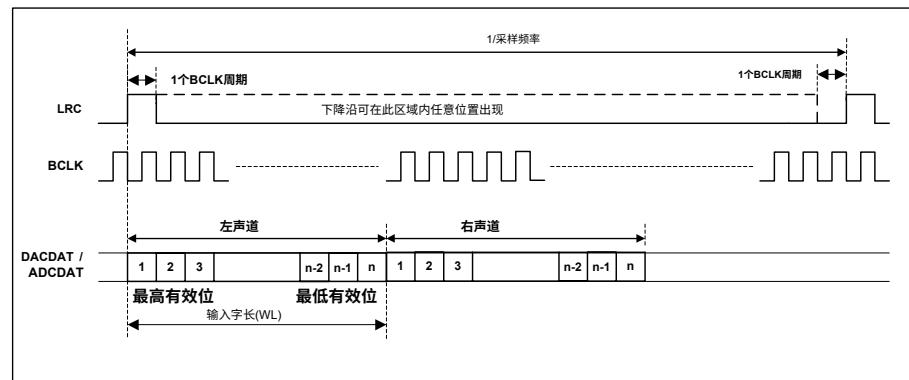


图32 DSP/PCM模式音频接口（模式B，LRP=1，从模式）

## AUDIO INTERFACE CONTROL

The register bits controlling audio format, word length and master / slave mode are summarised in Table 33. MS selects audio interface operation in master or slave mode. In Master mode BCLK, ADCLRC and DACLRC are outputs. The frequency of ADCLRC and DACLRC is set by the bits ADCDIV and DACDIV and the frequency of BCLK is set by the bits BCLKDIV (See "Clocking and Sample Rates"). In Slave mode BCLK, ADCLRC and DACLRC are inputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) Digital Audio Interface Format	8	ALRSWAP	0	Left/Right ADC channel swap 1 = Swap left and right ADC data in audio interface 0 = Output left and right data as normal
	7	BCLKINV	0	BCLK invert bit (for master and slave modes) 0 = BCLK not inverted 1 = BCLK inverted
	6	MS	0	Master / Slave Mode Control 0 = Enable slave mode 1 = Enable master mode
	5	DLRSWAP	0	Left/Right DAC Channel Swap 0 = Output left and right data as normal 1 = Swap left and right DAC data in audio interface
	4	LRP	0	Right, left and I <sup>2</sup> S modes – LRCLK polarity 0 = normal LRCLK polarity 1 = invert LRCLK polarity
	3:2	WL[1:0]	10	DSP Mode – mode A/B select 0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A) 1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B)
	1:0	FORMAT[1:0]	10	Audio Data Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits (see Note)

Table 33 Audio Data Format Control

**Note:** Right Justified mode does not support 32-bit data.

## 音频接口控制

表33总结了控制音频格式、字长和主/从模式的寄存器位。MS位用于选择音频接口的主/从模式操作。在主模式下，BCLK、ADCLRC和DACLRC为输出信号。ADCLRC和DACLRC的频率由ADCDIV和DADIV位设置，BCLK的频率由BCLKDIV位设置（参见“时钟与采样率”章节）。在从模式下，BCLK、A DCLRC和DACLRC为输入信号。

寄存器地址	位	标签	默认值	描述
R7 (07h) 数字音频 接口 格式	8	ALRSWAP	0	左右ADC通道交换 1 = 在音频 接口中交换左右ADC数据 0 = 正常输出左右声道数据
	7	BCLKINV	0	BCLK反相位（适用于主/从模式）0 = BCL K不反相 1 = BCLK反相
	6	MS	0	主/从模式控制 0 = 启用从模式 1 = 启用主模式
	5	DLRSWAP	0	左/右DAC通道交换 0 = 正常输出左右声道数据 1 = 在音频接口中交换左右DAC数 据
	4	LRP	0	右、左和I <sup>2</sup> S模式 – LRCLK 极性 0 = LRCLK极性正常 1 = 反转LRCLK极性  DSP模式 - 模式A/B选择 0 = 在LRC上升沿后的第2个BCLK上升沿获 取MSB（模式A） 1 = 在LRC上升沿 后的第1个BCLK上升沿获取MSB（模式 B）
	3:2	WL[1:0]	10	音频数据字长 00 = 16位 01 = 20位 10 = 24位 11 = 32位（参见注释）
	1:0	FORMAT[1:0]	10	音频数据格式选择 00 = 右对齐 01 = 左对齐 10 = I <sup>2</sup> S 格式 11 = DSP 模式

表33 音频数据格式控制

注：右对齐模式不支持32位数据。

### AUDIO INTERFACE OUTPUT TRISTATE

Register bit TRIS, register 24(18h) bit[3] can be used to tristate the ADCDAT pin and switch ADCLRC, DACLRC and BCLK to inputs. In Slave mode (MS=0) ADCLRC, DACLRC and BCLK are by default configured as inputs and only ADCDAT will be tri-stated, (see Table 34).

When the ADCLRC/GPIO1 pin is configured as a GPIO, this pin will not be tristated by the TRIS register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) Additional Control (2)	3	TRIS	0	Tristates ADCDAT and switches ADCLRC, DACLRC and BCLK to inputs. 0 = ADCDAT is an output; ADCLRC, DACLRC and BCLK are inputs (slave mode) or outputs (master mode) 1 = ADCDAT is tristated; DACLRC and BCLK are inputs; ADCLRC is an input (when not configured as a GPIO)

Table 34 Tri-stating the Audio Interface

### MASTER MODE ADCLRC AND DACLRC ENABLE

In master mode, by default ADCLRC clock generator is disabled and will output a logic 0 when the ADCs are both disabled and DACLRC clock generator is disabled and will output a logic 0 when the DACs are both disabled.

Register bit LRCM, register 24 (18h) bit[2] changes the control so that the ADCLRC and DACLRC clock generators are both disabled only when both ADCs and both DACs are disabled. This enables the user to use e.g. ADCLRC for both ADC and DAC LRCLK and disable the ADC when DAC only operation is required, (see Table 35).

When ADCLRC is configured as a GPIO (using ALRCGPIO), DACLRC is used for the ADCs and the DACs and will only be disabled in master mode when both ADCs and both DACs are disabled.

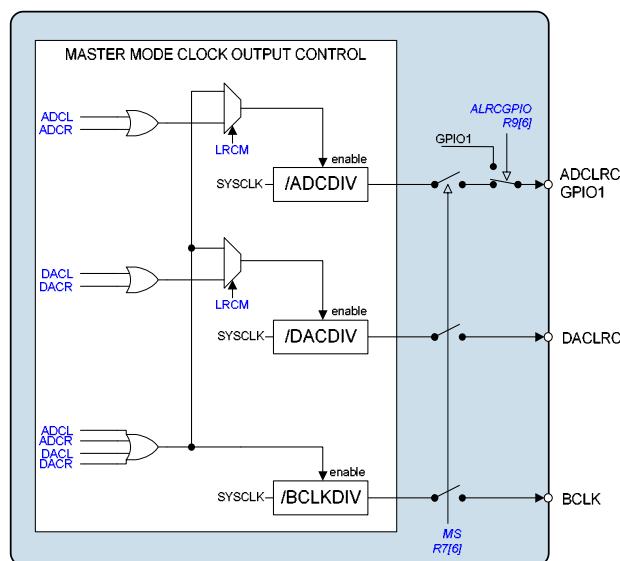


Figure 33 Master Mode Clock Ouput Control

### 音频接口输出三态控制

寄存器位TRIS（寄存器24(18h)位[3]）可用于将ADCDAT引脚设为高阻态，并将ADCLRC、DACLRC和BCLK切换为输入。在从模式（MS=0）下，ADCLRC、DACLRC和BCLK默认配置为输入，仅ADCDAT会被设为高阻态（参见表34）。

当ADCLRC/GPIO1引脚配置为GPIO时，TRIS寄存器位不会使该引脚进入高阻态。

寄存器地址	位	标签	默认值	描述
R24 (18h) 附加控制 寄存器(2)	3	TRIS	0	<p>将ADCDAT设为高阻态，并将ADCLRC、DACLRC和BCLK切换为输入。 0 = ADCDAT为输出；ADCLRC、DACLRC和BCLK作为输入（从模式）或输出（主模式） 1 = ADCDAT处于三态；DACLRC和BCLK作为输入；ADCLRC作为输入（当未配置为GPIO时）</p>

表34 音频接口三态控制

### 主模式ADCLRC与DACLRC使能

在主模式下，默认情况下当两个ADC均被禁用时ADCLRC时钟发生器将被禁用并输出逻辑0；当两个DAC均被禁用时DACLRC时钟发生器将被禁用并输出逻辑0。

寄存器位LRCM（寄存器24 (18h) bit[2]）可修改控制逻辑，使得仅当两个ADC和两个DAC均被禁用时，ADCLRC和DACLRC时钟发生器才会同时禁用。这允许用户使用例如ADCLRC同时作为ADC和DAC的LRCLK，并在仅需DAC操作时禁用ADC（参见表35）。

当ADCLRC被配置为GPIO（使用ALRCGPIO）时，DACLRC将同时用于ADC和DAC，且在主模式下仅当两个ADC和两个DAC均被禁用时才会被禁用。

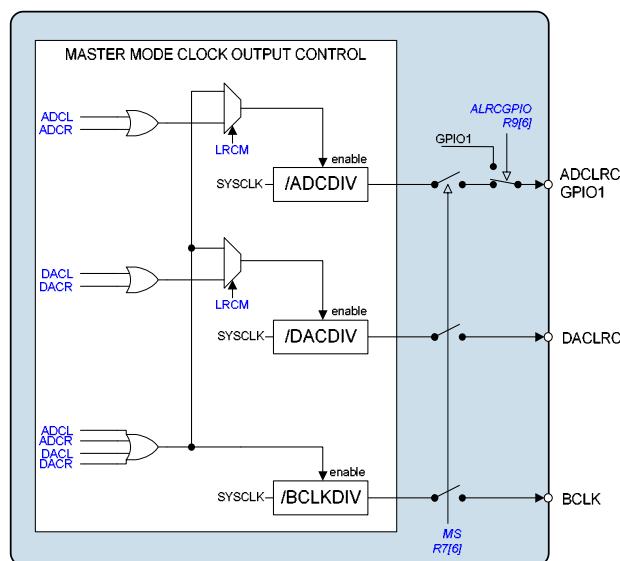


图33 主模式时钟输出控制

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) Additional Control (2)	2	LRCM	0	Selects disable mode for ADCLRC and DACLRC (Master mode) 0 = ADCLRC disabled when ADC (Left and Right) disabled; DACLRC disabled when DAC (Left and Right) disabled. 1 = ADCLRC and DACLRC disabled only when ADC (Left and Right) and DAC (Left and Right) are disabled.

Table 35 ADCLRC/DACLRC Enable

### COMPANDING

The WM8960 supports A-law and  $\mu$ -law companding on both transmit (ADC) and receive (DAC) sides. Companding can be enabled on the DAC or ADC audio interfaces by writing the appropriate value to the DACCOMP or ADCCOMP register bits respectively.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h) Audio Interface (2)	2:1	ADCCOMP	00	ADC companding 00 = off 01 = reserved 10 = $\mu$ -law 11 = A-law
	4:3	DACCOMP	00	DAC companding 00 = off 01 = reserved 10 = $\mu$ -law 11 = A-law
	5	WL8	0	0 = off 1 = device operates in 8-bit mode.

Table 36 Companding Control

Companding involves using a piecewise linear approximation of the following equations (as set out by ITU-T G.711 standard) for data compression:

$\mu$ -law (where  $\mu=255$  for the U.S. and Japan):

$$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu) \quad -1 \leq x \leq 1$$

A-law (where  $A=87.6$  for Europe):

$$F(x) = A|x| / (1 + \ln A) \quad \} \text{ for } x \geq 1/A$$

$$F(x) = (1 + \ln A|x|) / (1 + \ln A) \quad \} \text{ for } 1/A \leq x \leq 1$$

The compounded data is also inverted as recommended by the G.711 standard (all 8 bits are inverted for  $\mu$ -law, all even data bits are inverted for A-law). The data will be transmitted as the first 8 MSB's of data.

Companding converts 13 bits ( $\mu$ -law) or 12 bits (A-law) to 8 bits using non-linear quantization. The input data range is separated into 8 levels, allowing low amplitude signals better precision than that of high amplitude signals. This is to exploit the operation of the human auditory system, where louder sounds do not require as much resolution as quieter sounds. The compounded signal is an 8-bit word containing sign (1-bit), exponent (3-bits) and mantissa (4-bits).

Setting the WL8 register bit allows the device to operate with 8-bit data. In this mode it is possible to use 8 BCLK cycles per LRC frame. When using DSP mode B, this allows 8-bit data words to be output consecutively every 8 BCLK cycles and can be used with 8-bit data words using the A-law and u-law companding functions.

寄存器地址	位	标签	默认值	描述
R24 (18h) 附加控制 寄存器(2)	2	LRCM	0	选择ADCLRC和DACLRC的禁用模式（主模式） 0 = 当ADC（左右声道）禁用时ADCLRC禁用；当DAC（左右声道）禁用时DACLRC禁用 1 = 仅当ADC（左右声道）和DAC（左右声道）同时禁用时，ADCLRC和DACLRC才会禁用

表35 ADCLRC/DACLRC使能控制

**压扩**

WM8960支持在发送（ADC）和接收（DAC）端使用A律和μ律压扩技术。通过向DACCOMP或ADCCOMP寄存器位写入相应值，可分别在DAC或ADC音频接口启用压扩功能。

寄存器地址	位	标签	默认值	描述
R9 (09h) 音频接口 寄存器(2)	2:1	ADCCOMP	00	ADC压扩 00 = 关闭 01 = 保留 10 = μ律 11 = A律
	4:3	DACCOMP	00	DAC压扩 00 = 关闭 01 = 保留 10 = μ律 11 = A律
	5	WL8	0	0 = 关闭 1 = 设备工作于8位模式。

表36 压扩控制

压扩采用基于ITU-T G.711标准规定的分段线性近似方程进行数据压缩：

μ-law（其中  $\mu = 255$ ，适用于美国和日本）：

$$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu) \quad -1 \leq x \leq 1$$

A-law（其中  $A=87.6$ ，适用于欧洲）：

$$F(x) = A|x| / (1 + \ln A) \quad \} \text{ 当 } x \leq 1/A \text{ 时}$$

$$F(x) = (1 + \ln A|x|) / (1 + \ln A) \quad \} \text{ 当 } 1/A \leq x \leq 1 \text{ 时}$$

根据G.711标准建议，压扩数据需进行取反处理（μ-law所有8位数据取反，A-law偶数位数据取反）。数据将以8位最高有效位(MSB)形式传输。

压扩技术通过非线性量化将13位（μ律）或12位（A律）信号转换为8位。输入数据范围被划分为8个层级，使低幅度信号能获得比高幅度信号更高的精度。这利用了人类听觉系统的特性：较响声音不需要像弱声音那样高的解析度。压扩后的信号为8位字，包含符号位（1位）、指数位（3位）和尾数位（4位）。

设置WL8寄存器位可使器件工作在8位数据模式。此模式下每个LRC帧可使用8个BCLK周期。当采用DSP模式时，可实现每8个BCLK周期连续输出8位数据字，并可与使用A律和μ律压扩功能的8位数据字配合使用。

BIT7	BIT[6:4]	BIT[3:0]
SIGN	EXPONENT	MANTISSA

Table 37 8-bit Companded Word Composition

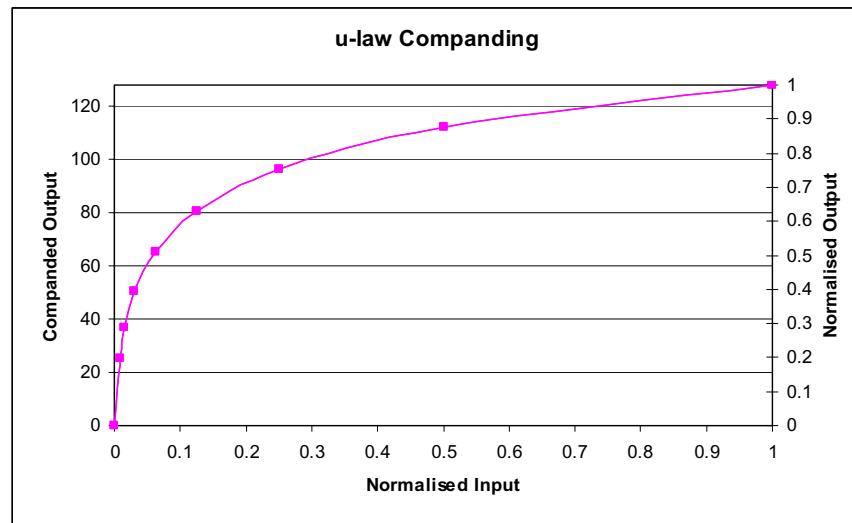
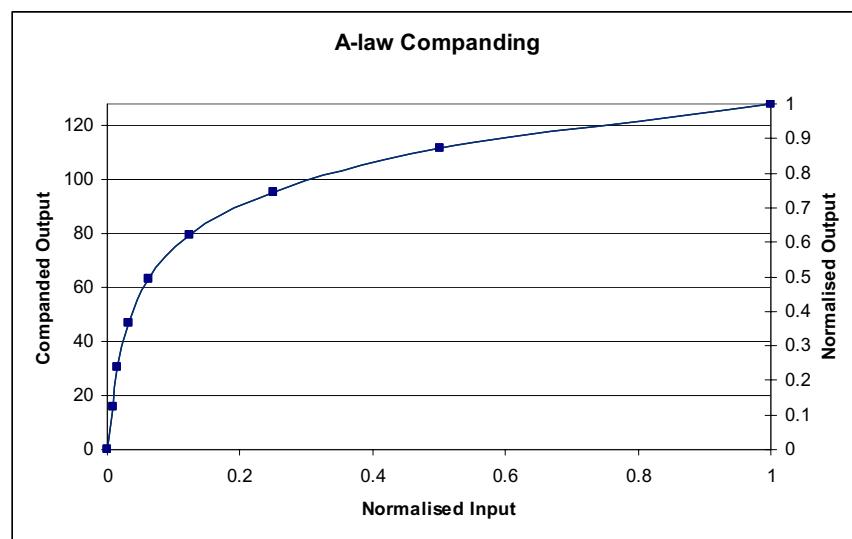
Figure 34  $\mu$ -Law Companding

Figure 35 A-Law Companding

BIT7	BIT[6:4]	BIT[3:0]
符号位	指数部分	尾数部分

表37 8位压扩字组成结构

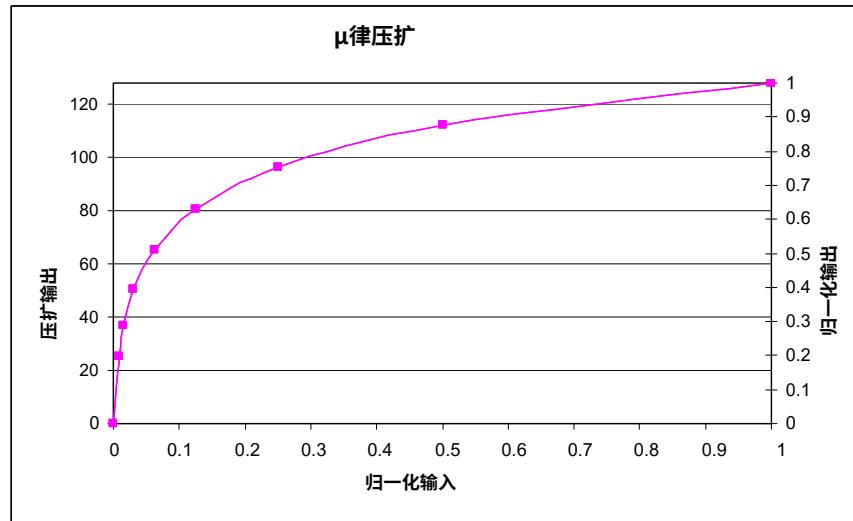


图34 μ律压扩特性

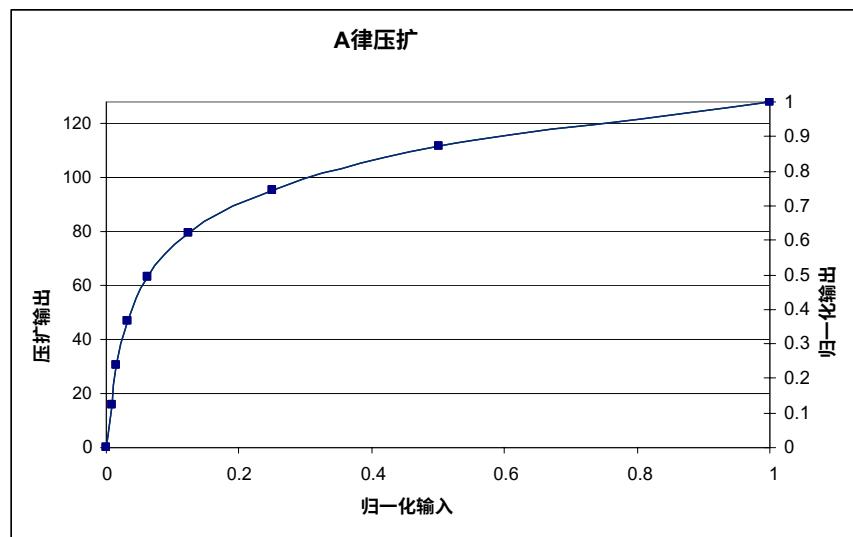


图35 A律压扩特性

## LOOPBACK

Setting the LOOPBACK register bit enables digital loopback. When this bit is set the output data from the ADC audio interface is fed directly into the DAC data input.

The ADCs and DACs must both use DA CLR when loopback is enabled. This is enabled by setting register bit ALRCGPIO = 1.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 Audio Interface	0	LOOPBACK	0	Digital Loopback Function 0 = No loopback. 1 = Loopback enabled, ADC data output is fed directly into DAC data input.

Table 38 Loopback Control

## CLOCKING AND SAMPLE RATES

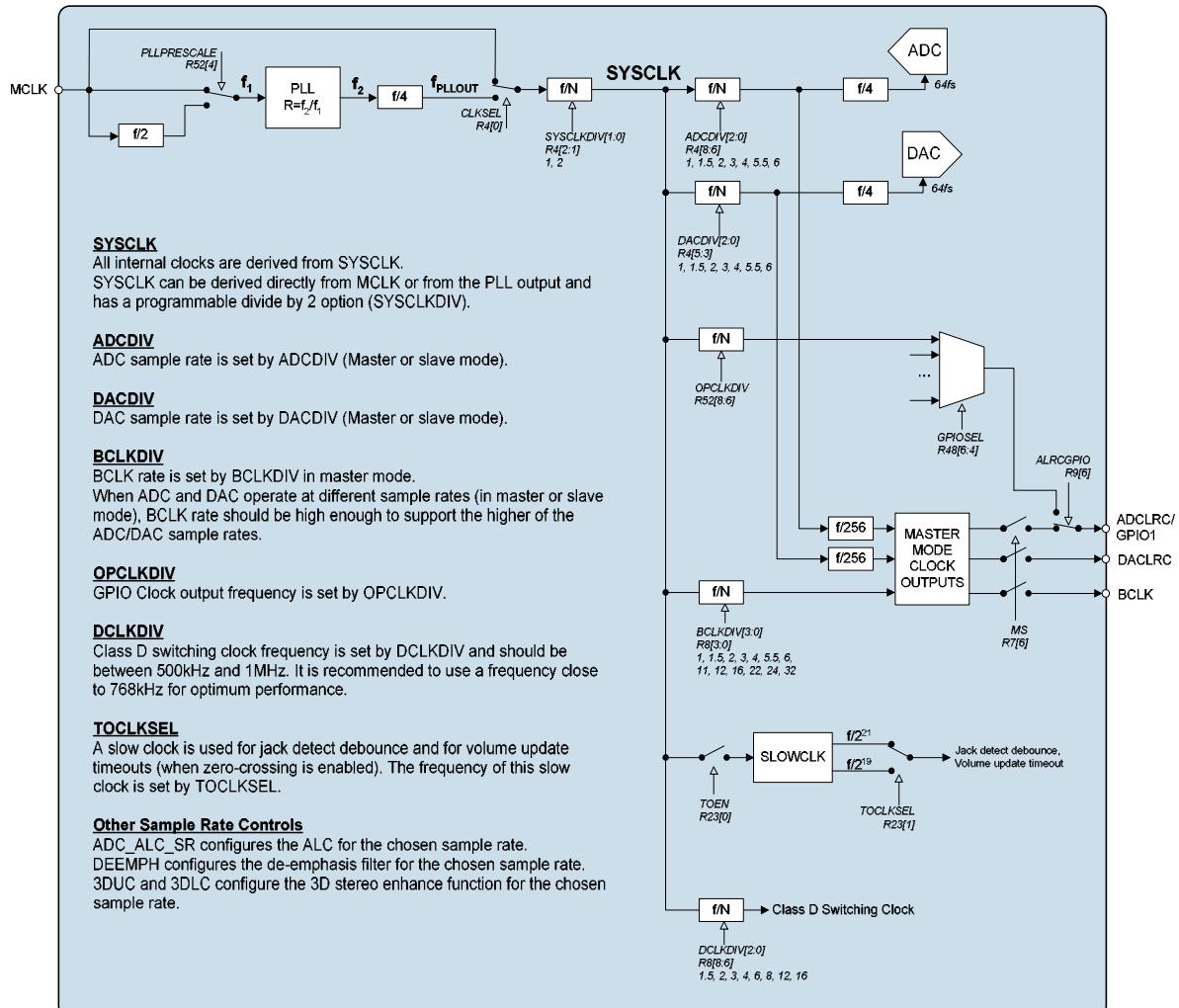


Figure 36 Clocking Scheme

Clocks for the ADCs and DACs, the DSP core functions, the digital audio interface and the class D outputs are all derived from SYSCLK as shown in Figure 36.

### 数字回环

设置LOOPBACK寄存器位可启用数字回环功能。当该位置位时，模数转换器(ADC)音频接口的输出数据将直接馈入数模转换器(DAC)的数据输入端。

当启用回环功能时，模数转换器(ADC)和数模转换器(DAC)必须同时使用DACLRC信号。可通过设置寄存器位ALRCGPIO=1来启用此功能。

寄存器地址	位	标签	默认值	描述
R9 音频 接口	0	数字回环	0	数字回环功能 0 = 禁用回环 1 = 启用环回模式，ADC数据输出直接馈入DAC数据输入。

表38 环回控制

### 时钟与采样率

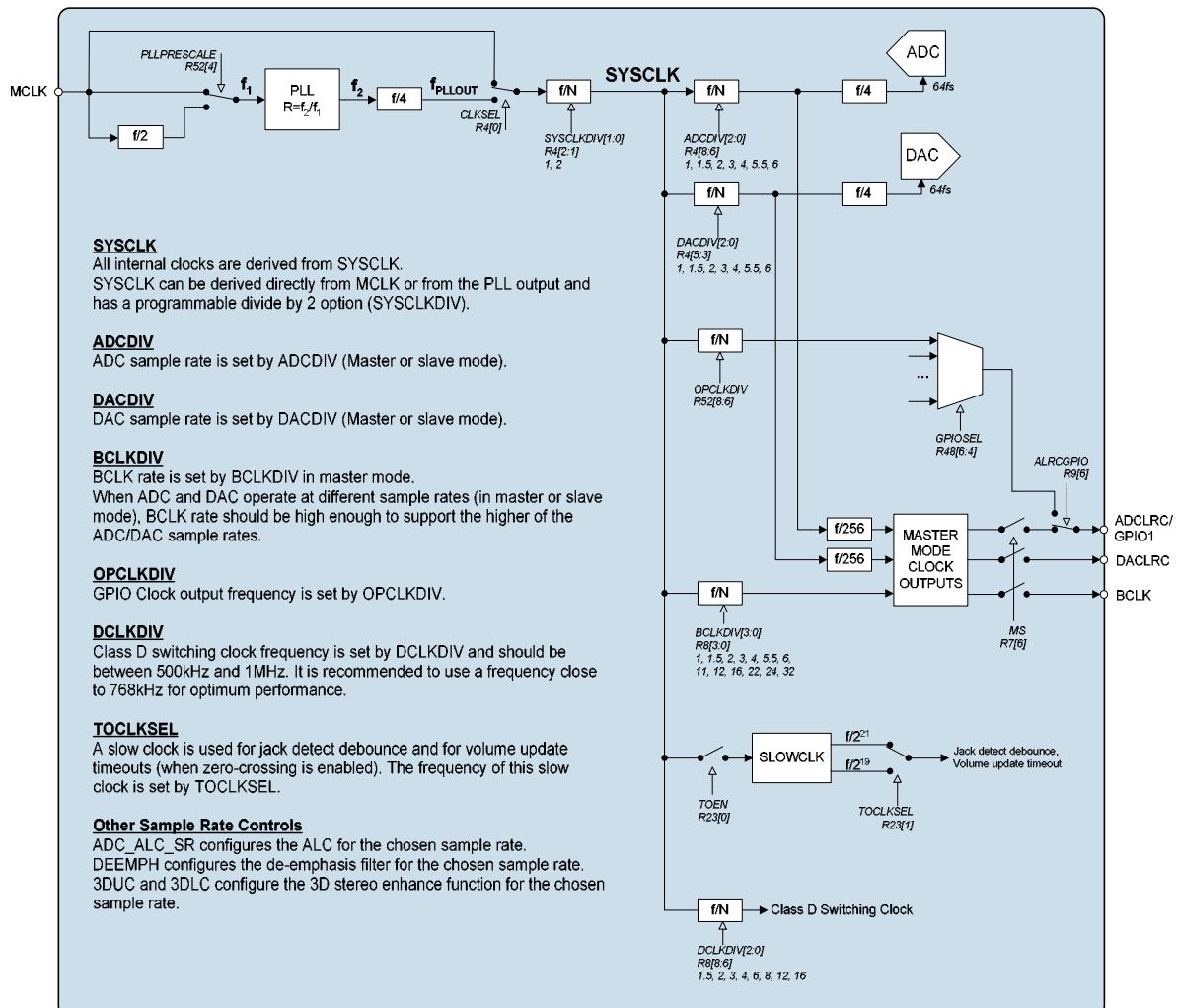


图36 时钟方案

如[图36]所示，ADC和DAC的时钟、DSP核心功能、数字音频接口以及D类输出的时钟均源自SYSCLK。

SYSCLK can either be derived directly from MCLK, or generated from a PLL using MCLK as a reference. The clock source is selected by CLKSEL. Many commonly-used audio sample rates can be derived directly from MCLK, while the PLL provides additional flexibility.

The ADC and DAC sample rates are independently selectable, relative to SYSCLK, using ADCDIV and DACDIV. In master mode, BCLK is also derived from SYSCLK via a programmable clock divide (BCLKDIV).

When the ADCLRC/GPIO1 pin is configured as a GPIO, a clock derived from SYSCLK can be output on this pin to provide clocking for other parts of the system. The frequency of this output clock is set by OPCLKDIV.

A slow clock derived from SYSCLK is used to de-bounce the headphone detect function, and to set the timeout period for volume updates when zero-cross functions are used. This clock is enabled by TOEN and its frequency is set by TOCLKSEL.

The class D outputs require a clock, and this is also derived from SYSCLK via a programmable divider (DCLKDIV) as shown in Figure 36. The class D switching clock should be set between 700kHz and 800kHz.

**The class D switching clock should not be disabled when the speaker outputs are active, as this would prevent the speaker outputs from functioning. The class D switching clock frequency should not be altered while the speaker outputs are active as this may generate an audible click.**

Table 39 shows the clocking and sample rate controls for MCLK input, BITCLK output (in master mode), ADCs, DACs, class D outputs and GPIO clock output. Refer to Table 40 for example clocking configurations.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h) Clocking (1)	8:6	ADCDIV [2:0]	000	ADC Sample rate divider (Also determines ADCLRC in master mode) 000 = SYSCLK / (1.0 * 256) 001 = SYSCLK / (1.5 * 256) 010 = SYSCLK / (2 * 256) 011 = SYSCLK / (3 * 256) 100 = SYSCLK / (4 * 256) 101 = SYSCLK / (5.5 * 256) 110 = SYSCLK / (6 * 256) 111 = Reserved
	5:3	DACDIV [2:0]	000	DAC Sample rate divider (Also determines DACLRC in master mode) 000 = SYSCLK / (1.0 * 256) 001 = SYSCLK / (1.5 * 256) 010 = SYSCLK / (2 * 256) 011 = SYSCLK / (3 * 256) 100 = SYSCLK / (4 * 256) 101 = SYSCLK / (5.5 * 256) 110 = SYSCLK / (6 * 256) 111 = Reserved
	2:1	SYCLKDIV [1:0]	00	SYSCLK Pre-divider. Clock source (MCLK or PLL output) will be divided by this value to generate SYSCLK. 00 = Divide SYSCLK by 1 01 = Reserved 10 = Divide SYSCLK by 2 11 = Reserved
	0	CLKSEL	0	SYSCLK selection 0 = SYSCLK derived from MCLK 1 = SYSCLK derived from PLL output

SYSCLK可直接源自MCLK，或通过以MCLK为参考的锁相环(PLL)生成。时钟源由CLKSEL选择。许多常用音频采样率可直接从MCLK派生，而PLL提供了额外的灵活性。

通过ADCDIV和DACDIV可独立设置ADC与DAC相对于SYSCLK的采样率。在主模式下，BCLK也通过可编程时钟分频器(BCLKDIV)从SYSCLK派生。

当ADCLRC/GPIO1引脚配置为通用输入输出端口时，可从该引脚输出源自SYSCLK的时钟信号，为系统其他部分提供时钟基准。该输出时钟频率由OPCLKDIV设置。

系统时钟(SYSCLK)分频产生的低速时钟用于耳机检测功能的去抖动处理，并在使用零交叉功能时设置音量更新的超时期限。该时钟通过TOEN使能，其频率由TOCLKSEL设定。

D类输出需要时钟信号，该时钟同样通过可编程分频器(DCLKDIV)从SYSCLK分频获得，如图36所示。D类开关时钟频率应设置在700kHz至800kHz之间。

**当扬声器输出处于激活状态时，不得禁用D类开关时钟，否则将导致扬声器输出功能失效。同时应避免在扬声器工作期间调整D类开关时钟频率，否则可能产生可闻的咔嗒声。**

表39列出了MCLK输入、主模式下的BITCLK输出、模数转换器(ADC)、数模转换器(DAC)、D类输出以及GPIO时钟输出的时钟与采样率控制参数。具体时钟配置示例请参考表40。

寄存器地址	位	标签	默认值	描述
R4 (04h) 时钟设置 (1)	8:6	ADCDIV [2:0]	000	ADC采样率分频器（在主机模式下也决定ADCLRC）000 = SYSCL K / (1.0 * 256) 001 = SYSCL K / (1.5 * 256) 010 = SYSCL K / (2 * 256) 011 = SYSCL K / (3 * 256) 100 = SYSCL K / (4 * 256) 101 = SYSCL K / (5.5 * 256) 110 = SYSCL K / (6 * 256) 111 = 保留值
	5:3	DACDIV [2:0]	000	DAC采样率分频器（在主机模式下也决定DACLRC）000 = SYSCL K / (1.0 * 256) 001 = SYSCL K / (1.5 * 256) 010 = SYSCL K / (2 * 256) 011 = SYSCL K / (3 * 256) 100 = SYSCL K / (4 * 256) 101 = SYSCL K / (5.5 * 256) 110 = SYSCL K / (6 * 256) 111 = 保留值
	2:1	SYSCLKDIV [1:0]	00	SYSCLK预分频器。时钟源(MCLK或PLL输出)将除以该值以生成SYSCLK。 00 = SYSCLK分频比为1 01 = 保留 10 = SYSCLK分频比为2 11 = 保留
	0	CLKSEL	0	SYSCLK选择 0 = SYSCLK源自MCLK 1 = SYSCLK源自PLL输出

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Clocking (2)	8:6	DCLKDIV	111	Class D switching clock divider. 000 = SYSCLK / 1.5 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16
	3:0	BCLKDIV[3:0]	0000	BCLK Frequency (Master Mode) 0000 = SYSCLK 0001 = SYSCLK / 1.5 0010 = SYSCLK / 2 0011 = SYSCLK / 3 0100 = SYSCLK / 4 0101 = SYSCLK / 5.5 0110 = SYSCLK / 6 0111 = SYSCLK / 8 1000 = SYSCLK / 11 1001 = SYSCLK / 12 1010 = SYSCLK / 16 1011 = SYSCLK / 22 1100 = SYSCLK / 24 1101 to 1111 = SYSCLK / 32

Table 39 ADC, DAC and BCLK Control

SYSCLK (=MCLK OR PLL OUTPUT) (MHz)	ADCDIV OR DACDIV	ADC / DAC SAMPLE RATE (kHz)
12.288	000 (=1)	48
	001 (=1.5)	32
	010 (=2)	24
	011 (=3)	16
	100 (=4)	12
	101 (=5.5)	(Not used)
	110 (=6)	8
	111	Reserved
11.2896	000 (=1)	44.1
	001 (=1.5)	(Not used)
	010 (=2)	22.05
	011 (=3)	(Not used)
	100 (=4)	11.025
	101 (=5.5)	8.018
	110 (=6)	(Not used)
	111	Reserved
2.048	000 (=1)	8
	001 (=1.5)	(Not used)
	010 (=2)	(Not used)
	011 (=3)	(Not used)
	100 (=4)	(Not used)
	101 (=5.5)	(Not used)
	110 (=6)	(Not used)
	111	Reserved

Table 40 ADC and DAC Sample Rates

寄存器地址	位	标签	默认值	描述
R8 (08h) 时钟设置(2)	8:6	数字时钟分频器	111	D类开关时钟分频器。 000 = SYSCLK / 1.5 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16
	3:0	BCLKDIV[3:0]	0000	BCLK频率 (主模式) 0000 = SYSCLK 0001 = SYSCLK / 1.5 0010 = SYSCLK / 2 0011 = SYSCLK / 3 0100 = SYSCLK / 4 0101 = SYSCLK / 5.5 0110 = SYSCLK / 6 0111 = SYSCLK / 8 1000 = SYSCLK / 11 1001 = SYSCLK / 12 1010 = SYSCLK / 16 1011 = SYSCLK / 22 1100 = SYSCLK / 24 1101至1111 = SYSCLK / 32

表39 ADC、DAC和BCLK控制

SYSCLK (=MCLK或PLL输出) (MHz)	ADCDIV或 DACDIV	ADC/DAC采样 速率 (kHz)
12.288	000 (=1)	48
	001 (=1.5)	32
	010 (=2)	24
	011 (=3)	16
	100 (=4)	12
	101 (=5.5)	(未使用)
	110 (=6)	8
	111	保留
11.2896	000 (=1)	44.1
	001 (=1.5)	(未使用)
	010 (=2)	22.05
	011 (=3)	(未使用)
	100 (=4)	11.025
	101 (=5.5)	8.018
	110 (=6)	(未使用)
	111	保留
2.048	000 (=1)	8
	001 (=1.5)	(未使用)
	010 (=2)	(未使用)
	011 (=3)	(未使用)
	100 (=4)	(未使用)
	101 (=5.5)	(未使用)
	110 (=6)	(未使用)
	111	保留

表40 ADC和DAC采样率

Although the ADC and DAC can run at different sample rates, they share the same bit clock pin BCLK.

When operating in master mode, register bits BCLKDIV[3:0] should be set to an appropriate value to ensure that there are sufficient BCLK cycles to transfer the complete data word from the ADCs and to the DACs.

When operating in slave mode, the host device must provide sufficient BCLK cycles to transfer complete data words to the ADCs and DACs.

Table 41 shows the maximum word lengths supported for a given SYSCLK and BCLKDIV, assuming that either the ADCs or DACs are running at maximum rate (i.e. ADCDIV[2:0]=000 or DACDIV[2:0]=000).

SYSCLK (=MCLK OR PLL OUTPUT) (MHz)	BCLKDIV[3:0]	BCLK RATE (MASTER MODE) (MHz)	MAXIMUM WORD LENGTH (AT MAXIMUM ADC OR DAC SAMPLE RATE)
12.288	0000 (=1)	12.288	32
	0001 (=1.5)	8.192	32
	0010 (=2)	6.144	32
	0011 (=3)	4.096	32
	0100 (=4)	3.072	32
	0101 (=5.5)	2.2341818	20
	0110 (=6)	2.048	20
	0111 (=8)	1.536	16
	1000 (=11)	1.117091	8
	1001 (=12)	1.024	8
	1010 (=16)	0.768	8
	1011 (=22)	0.558545	N/A
	1100 (=24)	0.512	N/A
	1101 (=32)	0.384	N/A
	1110 (=32)	0.384	N/A
	1111 (=32)	0.384	N/A
11.2896	0000 (=1)	11.2896	32
	0001 (=1.5)	7.5264	32
	0010 (=2)	5.6448	32
	0011 (=3)	3.7632	32
	0100 (=4)	2.8224	32
	0101 (=5.5)	2.052655	20
	0110 (=6)	1.8816	20
	0111 (=8)	1.4112	16
	1000 (=11)	1.026327	8
	1001 (=12)	0.9408	8
	1010 (=16)	0.7056	8
	1011 (=22)	0.513164	N/A
	1100 (=24)	0.4704	N/A
	1101 (=32)	0.3528	N/A
	1110 (=32)	0.3528	N/A
	1111 (=32)	0.3528	N/A

Table 41 BCLK Divider in Master Mode

#### OTHER SAMPLE RATE CONTROL BITS

The ALC, de-emphasis filter and 3D stereo enhance functions all need to be configured for the chosen sample rate when in use, as shown in Table 42.

ADC\_ALC\_SR should be configured to match the chosen ADC sample rate.

DEEMPH, 3DUC and 3DUC should be configured to match the chosen DAC sample rate.

尽管ADC和DAC可以工作在不同的采样率下，但它们共享同一个位时钟引脚BCLK。

当工作在主模式时，应设置寄存器位BCLKDIV[3:0]为适当值，以确保有足够的BCLK周期来传输来自ADC的完整数据字至DAC。

当工作在从模式时，主机设备必须提供足够的BCLK周期来传输完整数据字至ADC和DAC。

表41显示了在给定SYSCLK和BCLKDIV条件下支持的最大字长（假设ADC或DAC以最高速率运行，即ADCDIV[2:0]=000或DADCDIV[2:0]=000）。

SYSCLK (=MCLK或PLL输出) (MHz)	BCLKDIV[3:0]	BCLK速率 (主模式) (MHz)	最大字长 (在最大 ADC 或 DAC 采样率下)
12.288	0000 (=1)	12.288	32
	0001 (=1.5)	8.192	32
	0010 (=2)	6.144	32
	0011 (=3)	4.096	32
	0100 (=4)	3.072	32
	0101 (=5.5)	2.2341818	20
	0110 (=6)	2.048	20
	0111 (=8)	1.536	16
	1000 (=11)	1.117091	8
	1001 (=12)	1.024	8
	1010 (=16)	0.768	8
	1011 (=22)	0.558545	不适用
	1100 (=24)	0.512	不适用
	1101 (=32)	0.384	不适用
	1110 (=32)	0.384	不适用
	1111 (=32)	0.384	不适用
11.2896	0000 (=1)	11.2896	32
	0001 (=1.5)	7.5264	32
	0010 (=2)	5.6448	32
	0011 (=3)	3.7632	32
	0100 (=4)	2.8224	32
	0101 (=5.5)	2.052655	20
	0110 (=6)	1.8816	20
	0111 (=8)	1.4112	16
	1000 (=11)	1.026327	8
	1001 (=12)	0.9408	8
	1010 (=16)	0.7056	8
	1011 (=22)	0.513164	不适用
	1100 (=24)	0.4704	不适用
	1101 (=32)	0.3528	不适用
	1110 (=32)	0.3528	不适用
	1111 (=32)	0.3528	不适用

表41 主模式下的BCLK分频器

#### 其他采样率控制位

如表42所示，使用时应根据所选采样率为ALC、去加重滤波器和3D立体声增强功能进行配置。

应配置ADC\_ALC\_SR以匹配所选ADC采样率。

DEEMPH、3DUC及3DUC应配置为匹配所选DAC采样率。

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R27 (1Bh) Additional Control (3)	2:0	ADC_ALC_SR [2:0]	000	ALC Sample Rate 000 = 44.1k / 48k 001 = 32k 010 = 22.05k / 24k 011 = 16k 100 = 11.25k / 12k 101 = 8k 110 and 111 = Reserved
R5 (05h) ADC and DAC Control (1)	2:1	DEEMPH [1:0]	00	De-Emphasis Control 11 = 48kHz sample rate 10 = 44.1kHz sample rate 01 = 32kHz sample rate 00 = No de-emphasis
R16 (10h) 3D Enhance	6	3DUC	0	Upper Cut-Off Frequency 0 = High (Recommended for $f_s \geq 32\text{kHz}$ ) 1 = Low (Recommended for $f_s < 32\text{kHz}$ )
	5	3DLC	0	Lower Cut-Off Frequency 0 = Low (Recommended for $f_s \geq 32\text{kHz}$ ) 1 = High (Recommended for $f_s < 32\text{kHz}$ )

**Table 42 Additional Sample Rate Controls****PLL**

The integrated PLL can be used to generate SYSCLK for the WM8960 or provide clocking for external devices via the GPIO1 pin.

The PLL is enabled by the PLLEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R26 (1Ah) Power management (2)	0	PLLEN	0	PLL Enable 0 = PLL off 1 = PLL on
R52 (34h) PLL (1)	5	SDM	0	Enable Integer Mode 0 = Integer mode 1 = Fractional mode

**Table 43 PLLEN Control Bit**

The PLL frequency ratio  $R = f_2/f_1$  (See Figure 36) can be set using the register bits PLLK and PLLN:

$$\text{PLLN} = \text{int } R$$

$$\text{PLLK} = \text{int } (2^{24} (R - \text{PLLN}))$$

**EXAMPLE:**

MCLK=12MHz, required clock = 12.288MHz.

R should be chosen to ensure  $5 < \text{PLLN} < 13$ . There is a fixed divide by 4 in the PLL and a selectable divide by N after the PLL which should be set to divide by 2 to meet this requirement.

Enabling the divide by 2 sets the required  $f_2 = 4 \times 2 \times 12.288\text{MHz} = 98.304\text{MHz}$ .

$$R = 98.304 / 12 = 8.192$$

$$\text{PLLN} = \text{int } R = 8$$

$$k = \text{int } (2^{24} \times (8.192 - 8)) = 3221225 = 3126E9h$$

寄存器地址	位	标签	默认值	描述
R27 (1Bh) 附加控制 (3)	2:0	ADC_ALC_SR [2:0]	000	ALC采样率 000 = 44.1k / 48k 001 = 32k 010 = 22.05k / 24k 011 = 16k 100 = 11.25k / 12k 101 = 8k 110 和 111 = 保留
R5 (05h) 模数 转换器和数模 转换器控制(1)	2:1	DEEMPH [1:0]	00	去加重控制 11 = 48千赫采样率 10 = 44.1千赫采样率 01 = 32千赫采样率 00 = 无去加重
R16 (10h) 3D增强	6	3DUC	0	上截止频率 0 = 高 (建议用于 采样频率 $\geq$ 32kHz) 1 = 低 (建议用于 采样频率<32kHz)
	5	3DLC	0	下截止频率 0 = 低 (建议用于 采样频率 $\geq$ 32kHz) 1 = 高 (建议用于 采样频率<32kHz)

表42 附加采样率控制

**PLL**

集成锁相环可用于为WM8960生成SYSCLK，或通过GPIO1引脚为外部设备提供时钟信号。

通过PLLEN寄存器位使能锁相环。

寄存器地址	位	标签	默认值	描述
R26 (1Ah) 电源管理 (2)	0	PLLEN	0	锁相环使能 0 = 关闭锁相环 1 = 开启锁相环
R52 (34h) 锁相环 (1)	5	SDM	0	启用整数模式 0 = 整数模式 1 = 分数模式

表43 PLLEN控制位

锁相环频率比  $R = f_2/f_1$  (参见图36) 可通过寄存器位PLLK和PLLN进行设置：

PLLN = 取R的整数部分

PLLK = 取( $2^{24}(R-PLLN)$ )的整数部分

**示例：**

MCLK=12MHz, 所需时钟频率=12.288MHz。

应选择R以确保 $5 < PLLN < 13$ 。锁相环中存在固定的4分频电路，且在锁相环之后有一个可配置的N分频电路，需将其设置为2分频以满足此要求。

启用2分频后得到所需 $f_2 = 4 \times 2 \times 12.288\text{MHz} = 98.304\text{MHz}$ 。

$$R = 98.304 / 12 = 8.192$$

PLLN=取R的整数部分=8

$$k = \text{int} (2^{24} \times (8.192 - 8)) = 3221225 = 3126E9h$$

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R52 (34h) PLL N value	4	PLLPRESCALE	0	Divide MCLK by 2 before input to PLL 0 = Divide by 1 1 = Divide by 2
	3:0	PLLN	8h	Integer (N) part of PLL input/output frequency ratio. Use values greater than 5 and less than 13.
R53 (35h) PLL K value (1)	5:0	PLLK [23:16]	31h	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).
R54 (36h) PLL K Value (2)	8:0	PLLK [15:8]	26h	
R55 (37h) PLL K Value (3)	8:0	PLLK [7:0]	E9h	

**Table 44 PLL Frequency Ratio Control**

The PLL performs best when  $f_2$  is between 90MHz and 100MHz. Its stability peaks at N=8. Some example settings are shown in Table 45.

MCLK (MHz) (f1)	DESIRED OUTPUT (SYSCLK) (MHz)	f2 (MHz)	PRESCALE DIVIDE (PLLPRESCALE)	POSTSCALE DIVIDE (SYSCLKDIV[1:0])	FIXED POST-DIVIDE	R	N	K
12	11.2896	90.3168	1	2	4	7.5264	7h	86C226h
12	12.288	98.304	1	2	4	8.192	8h	3126E8h
13	11.2896	90.3168	1	2	4	6.947446	6h	F28BD4h
13	12.288	98.304	1	2	4	7.561846	7h	8FD525h
14.4	11.2896	90.3168	1	2	4	6.272	6h	45A1CAh
14.4	12.288	98.304	1	2	4	6.826667	6h	D3A06Eh
19.2	11.2896	90.3168	2	2	4	9.408	9h	6872AFh
19.2	12.288	98.304	2	2	4	10.24	Ah	3D70A3h
19.68	11.2896	90.3168	2	2	4	9.178537	9h	2DB492h
19.68	12.288	98.304	2	2	4	9.990243	9h	FD809Fh
19.8	11.2896	90.3168	2	2	4	9.122909	9h	1F76F7h
19.8	12.288	98.304	2	2	4	9.929697	9h	EE009Eh
24	11.2896	90.3168	2	2	4	7.5264	7h	86C226h
24	12.288	98.304	2	2	4	8.192	8h	3126E8h
26	11.2896	90.3168	2	2	4	6.947446	6h	F28BD4h
26	12.288	98.304	2	2	4	7.561846	7h	8FD525h
27	11.2896	90.3168	2	2	4	6.690133	6h	B0AC93h
27	12.288	98.304	2	2	4	7.281778	7h	482296h

**Table 45 PLL Frequency Examples**

寄存器地址	位	标签	默认值	描述
R52 (34h) 锁相环N值	4	锁相环预分频器	0	在输入至锁相环前将MCLK分频2分 频 0=1分频 1=2分频
	3:0	锁相环N值	8h	锁相环输入/输出频率比的整数(N)部分。取值应大于5且小于13。
R53 (35h) 锁相环K值(1)	5:0	PLLK [23:16]	31h	锁相环输入/输出频率比的小数(K)部分 (按24位二进制数处理)。
R54 (36h) 锁相环K值(2)	8:0	PLLK [15:8]	26h	
R55 (37h) 锁相环K值(3)	8:0	PLLK [7:0]	E9h	

表44 锁相环频率比控制

当f2处于90MHz至100MHz之间时，锁相环性能最佳。其稳定性在N=8时达到峰值。部分示例设置如表格45所示。

MCLK (MHz) (f1)	期望输出 (SYSCLK) (MHz)	f2 (MHz)	预分频除数 (PLL_PRESCALE)	后分频除数 (SYSCLKDIV[1:0])	固定后分频	R	N	K
12	11.2896	90.3168	1	2	4	7.5264	7h	86C226h
12	12.288	98.304	1	2	4	8.192	8h	3126E8h
13	11.2896	90.3168	1	2	4	6.947446	6h	F28BD4h
13	12.288	98.304	1	2	4	7.561846	7h	8FD525h
14.4	11.2896	90.3168	1	2	4	6.272	6h	45A1CAh
14.4	12.288	98.304	1	2	4	6.826667	6h	D3A06Eh
19.2	11.2896	90.3168	2	2	4	9.408	9h	6872AFh
19.2	12.288	98.304	2	2	4	10.24	Ah	3D70A3h
19.68	11.2896	90.3168	2	2	4	9.178537	9h	2DB492h
19.68	12.288	98.304	2	2	4	9.990243	9h	FD809Fh
19.8	11.2896	90.3168	2	2	4	9.122909	9h	1F76F7h
19.8	12.288	98.304	2	2	4	9.929697	9h	EE009Eh
24	11.2896	90.3168	2	2	4	7.5264	7h	86C226h
24	12.288	98.304	2	2	4	8.192	8h	3126E8h
26	11.2896	90.3168	2	2	4	6.947446	6h	F28BD4h
26	12.288	98.304	2	2	4	7.561846	7h	8FD525h
27	11.2896	90.3168	2	2	4	6.690133	6h	B0AC93h
27	12.288	98.304	2	2	4	7.281778	7h	482296h

表45 锁相环频率示例

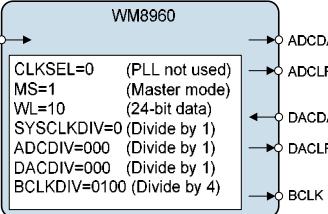
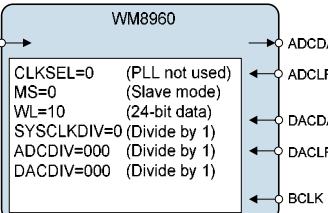
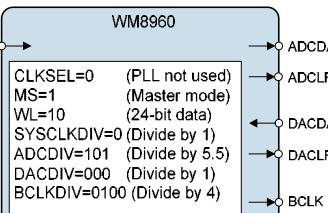
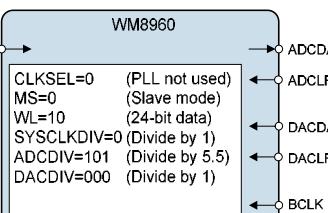
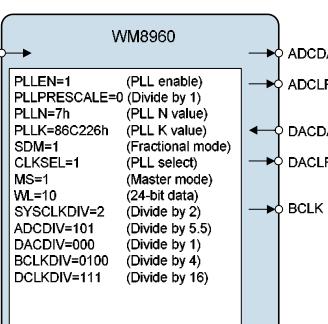
	Device running in master mode with 24-bit data MCLK input at 12.288MHz ADC and DAC running at fs=48kHz BCLK running at 64fs
	Device running in slave mode with 24-bit data MCLK input at 12.288MHz ADC and DAC running at fs=48kHz BCLK supplied from host at 64fs in this example
	Device running in master mode with 24-bit data MCLK input at 11.2896MHz ADC running at fs=8.018kHz DAC running at fs=44.1kHz BCLK running at 64fs (relative to DAC sample rate, as DAC is operating at a higher sample rate than ADC)
	Device running in slave mode with 24-bit data MCLK input at 11.2896MHz ADC running at fs=8.018kHz DAC running at fs=44.1kHz BCLK supplied from host at 64fs in this example (relative to DAC sample rate, as DAC is operating at a higher sample rate than ADC)
	Device running in master mode with 24-bit data MCLK input at 12MHz PLL Enabled and configured for SYSCLK=11.2896MHz ADC running at fs=8.018kHz DAC running at fs=44.1kHz BCLK running at 64fs (relative to DAC sample rate, as DAC is operating at a higher sample rate than ADC) Class D clocks running at 705.6kHz

Table 46 Example Clocking Schemes

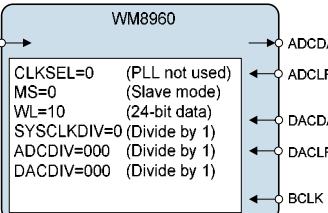
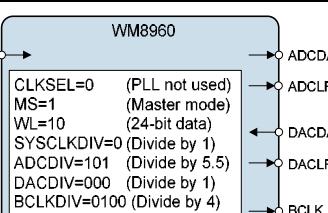
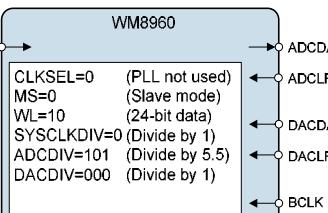
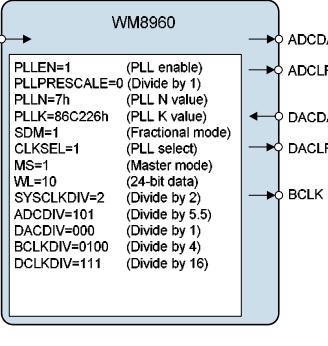
 <p>WM8960</p> <p>CLKSEL=0 (PLL not used) MS=0 (Slave mode) WL=10 (24-bit data) SYSCLKDIV=0 (Divide by 1) ADCDIV=000 (Divide by 1) DACDIV=000 (Divide by 1)</p> <p>ADCDAT ADC fs = 48kHz ADCLRC DACDAT DAC fs = 48kHz DACLRC BCLK Bit clock = 3.072MHz</p>	设备以从模式运行，采用24位数据 MCLK输入为12.288MHz ADC和DAC以fs=48千赫运行 本示例中BCLK由主机提供64倍采样频率时钟
 <p>WM8960</p> <p>CLKSEL=0 (PLL not used) MS=1 (Master mode) WL=10 (24-bit data) SYSCLKDIV=0 (Divide by 1) ADCDIV=101 (Divide by 5.5) DACDIV=000 (Divide by 1) BCLKDIV=0100 (Divide by 4)</p> <p>ADCDAT ADC fs = 8.018kHz ADCLRC DACDAT DAC fs = 44.1kHz DACLRC BCLK Bit clock = 2.8224MHz</p>	设备以主模式运行，采用24位数据 MCLK输入为11.2896MHz ADC以fs=8.018千赫运行 DAC以fs=44.1千赫运行 BCLK运行于64倍采样频率（相对于DAC采样率，因DAC工作于比ADC更高的采样率）
 <p>WM8960</p> <p>CLKSEL=0 (PLL not used) MS=0 (Slave mode) WL=10 (24-bit data) SYSCLKDIV=0 (Divide by 1) ADCDIV=101 (Divide by 5.5) DACDIV=000 (Divide by 1)</p> <p>ADCDAT ADC fs = 8.018kHz ADCLRC DACDAT DAC fs = 44.1kHz DACLRC BCLK Bit clock = 2.8224MHz</p>	设备以从模式运行，使用24位数据 MCLK输入频率为11.2896MHz 模数转换器(ADC)工作频率为fs=8.018kHz 数模转换器(DAC)工作频率为fs=44.1kHz 本示例中由主机提供64倍采样频率的BCLK（相对于DAC采样率，因DAC工作频率高于ADC）
 <p>WM8960</p> <p>PLLEN=1 (PLL enable) PLLPRSCALE=0 (Divide by 1) PLLN=7h (PLL N value) PLLK=86C226h (PLL K value) SDM=1 (Fractional mode) CLKSEL=1 (PLL select) MS=1 (Master mode) WL=10 (24-bit data) SYSCLKDIV=2 (Divide by 2) ADCDIV=101 (Divide by 5.5) DACDIV=000 (Divide by 1) BCLKDIV=0100 (Divide by 4) DCLKDIV=111 (Divide by 16)</p> <p>ADCDAT ADC fs = 8.018kHz ADCLRC DACDAT DAC fs = 44.1kHz DACLRC BCLK Bit clock = 2.8224MHz</p>	设备以主模式运行，使用24位数据 MCLK输入频率为12MHz 启用并配置锁相环(PLL)以实现SYSCLK=11.2896MHz 模数转换器(ADC)工作频率为fs=8.018kHz 数模转换器(DAC)工作频率为fs=44.1kHz BCLK运行于64倍采样频率（相对于DAC采样率，因DAC工作频率高于ADC），D类时钟运行频率为705.6kHz

表46 时钟方案示例

## CONTROL INTERFACE

### 2-WIRE SERIAL CONTROL INTERFACE

The WM8960 is controlled by writing to registers through a 2-wire serial control interface. A control word consists of 16 bits. The first 7 bits (B15 to B9) are address bits that select which control register is accessed. The remaining 9 bits (B8 to B0) are data bits, corresponding to the 9 bits in each control register. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 7-bit address of each register in the WM8960).

The device address is 0011010 (**0x34h**).

The WM8960 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8960 and the R/W bit is '0', indicating a write, then the WM8960 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1', the WM8960 returns to the idle condition and wait for a new start condition and valid address.

Once the WM8960 has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the WM8960 register address plus the first bit of register data). The WM8960 then acknowledges the first data byte by pulling SDIN low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the WM8960 acknowledges again by pulling SDIN low.

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high. After receiving a complete address and data sequence the WM8960 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device jumps to the idle condition.

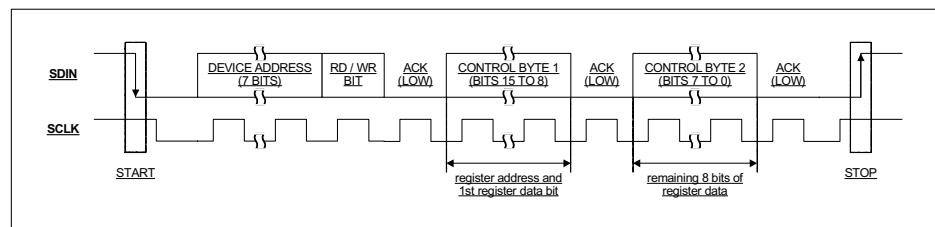


Figure 37 2-Wire Serial Control Interface

## POWER MANAGEMENT

The WM8960 has three control registers that allow users to select which functions are active. For minimum power consumption, unused functions should be disabled. To avoid any pop or click noise, it is important to enable or disable functions in the correct order (see Applications Information). VMIDSEL is the enable for the Vmid reference, which defaults to disabled and can be enabled as a 2x50k $\Omega$  potential divider or, for low power maintenance of Vref when all other blocks are disabled, as a 2x250k $\Omega$  potential divider.

## 控制接口

### 双线制串行控制接口

WM8960通过双线制串行控制接口进行寄存器写入操作。控制字由16位组成：前7位（B15至B9）为地址位，用于选择目标控制寄存器；剩余9位（B8至B0）为数据位，对应各控制寄存器的9个配置位。同一总线可控制多个设备，每个设备拥有唯一的7位地址（注意：此地址不同于WM8960内部寄存器的7位地址）。

设备地址为0011010（0x34h）。

WM8960仅作为从设备工作。控制器通过在SCLK保持高电平时SDIN出现从高到低的跳变来指示数据传输开始，这表示后续将跟随设备地址和数据。双线总线上所有设备都会响应起始条件，并在SDIN上移入接下来的8位数据（7位地址+读/写位，最高位优先）。如果接收到的设备地址与WM8960地址匹配且R/W位为'0'（表示写操作），则WM8960会在下一个时钟脉冲将SDIN拉低（ACK）作为响应。如果地址不匹配或R/W位为'1'，WM8960将返回空闲状态并等待新的起始条件和有效地址。

当WM8960确认正确地址后，控制器发送第一个控制数据字节（B15至B8，即WM8960寄存器地址加寄存器数据的首比特）。随后WM8960通过将SDIN拉低一个时钟脉冲来确认第一个数据字节。控制器接着发送第二个控制数据字节（B7至B0，即寄存器数据的剩余8位），WM8960会再次通过拉低SDIN进行确认。

当SCLK保持高电平时，SDIN端出现从低到高的跳变即表示数据传输完成。

在接收完整的地址和数据序列后，WM8960将返回空闲状态并等待下一个起始条件。若在数据传输过程中检测到非时序的起始或停止条件（即SCLK为高时SDIN发生变化），器件将立即跳转至空闲状态。

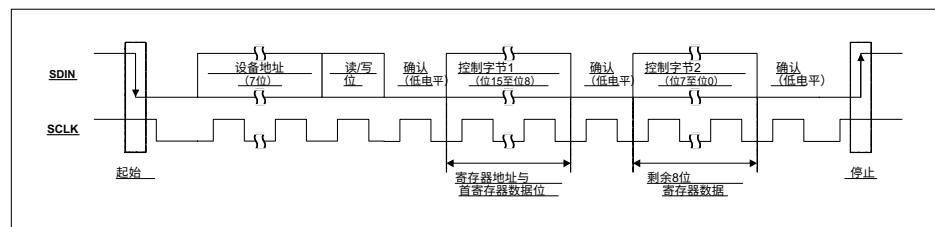


图37 双线串行控制接口

## 电源管理

WM8960包含三个控制寄存器用于选择启用功能模块。为达到最低功耗，建议禁用未使用功能。为避免爆音干扰，需按特定顺序启用/禁用功能（详见应用说明）。VMIDSEL是Vmid参考电压的使能控制位，默认禁用，可配置为 $2 \times 50\text{k}\Omega$ 电位分压模式，或当其他模块均禁用时采用 $2 \times 250\text{k}\Omega$ 电位分压模式以低功耗维持Vref。

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power Management (1)	8:7	VMIDSEL	00	Vmid Divider Enable and Select 00 = Vmid disabled (for OFF mode) 01 = 2 x 50kΩ divider enabled (for playback / record) 10 = 2 x 250kΩ divider enabled (for low-power standby) 11 = 2 x 5kΩ divider enabled (for fast start-up)
	6	VREF	0	VREF (necessary for all other functions) 0 = Power down 1 = Power up
	5	AINL	0	Analogue Input PGA and Boost Left 0 = Power down 1 = Power up (Note: LMIC must also be set to enable the PGA)
	4	AINR	0	Analogue Input PGA and Boost Right 0 = Power down 1 = Power up (Note: RMIC must also be set to enable the PGA)
	3	ADCL	0	ADC Left 0 = Power down 1 = Power up
	2	ADCR	0	ADC Right 0 = Power down 1 = Power up
	1	MICB	0	MICBIAS 0 = Power down 1 = Power up
	0	DIGENB	0	Master Clock Disable 0 = Master clock enabled 1 = Master clock disabled

寄存器地址	位	标签	默认值	描述
R25 (19h) 电源管理 (1)	8:7	VMID选择	00	VMID分压器使能与选择 00 = 禁用VMID (用于关机模式) 01 = 2 x 50kΩ分压器启用 (用于播放/录音) 10 = 2 x 250kΩ分压器启用 (用于低功耗待机) 11 = 启用2×5kΩ分压器 (用于快速启动)
	6	VREF	0	VREF (所有其他功能必需) 0 = 断电 1 = 上电
	5	AINL	0	左声道模拟输入PGA与升压电路 0 = 断电 1 = 上电 (注意：必须同时设置LMIC以启用PGA)
	4	AINR	0	右声道模拟输入PGA与升压电路 0 = 断电 1 = 上电 (注意：必须同时设置RMIC以启用PGA)
	3	ADCL	0	左声道ADC 0 = 断电 1 = 上电
	2	ADCR	0	右声道ADC 0 = 断电 1 = 上电
	1	MICB	0	麦克风偏置 0 = 断电 1 = 上电
	0	数字使能	0	主时钟禁用 0 = 主时钟启用 1 = 主时钟禁用

R26 (1Ah) Power Management (2)	8	DACL	0	DAC Left 0 = Power down 1 = Power up
	7	DACR	0	DAC Right 0 = Power down 1 = Power up
	6	LOUT1	0	LOUT1 Output Buffer 0 = Power down 1 = Power up
	5	ROUT1	0	ROUT1 Output Buffer 0 = Power down 1 = Power up
	4	SPKL	0	SPK_LP/SPK_LN Output PGA. 0 = Power down 1 = Power up (Note: Speaker output also requires SPK_OP_EN[0] to be set)
	3	SPKR	0	SPK_RP/SPK_RN Output PGA
				0 = Power down 1 = Power up (Note: Speaker output also requires SPK_OP_EN[1] to be set)
	1	OUT3	0	OUT3 Output Buffer 0 = Power down 1 = Power up
	0	PLL_EN	0	PLL Enable 0 = Power down 1 = Power up
R47 (2Fh) Power Management (3)	5	LMIC		Left Input PGA Enable 0 = Power down 1 = Power up (Note: PGA also requires AINL to be set)
	4	RMIC		Right Input PGA Enable 0 = Power down 1 = Power up (Note: PGA also requires AINR to be set)
	3	LOMIX		Left Output Mixer Enable 0 = Power down 1 = Power up
	2	ROMIX		Right Output Mixer Enable 0 = Power down 1 = Power up

Table 47 Power Management

R26 (1Ah) 电源 管理(2)	8	左声道数模转换器	0	左声道数模转换器 0 = 关闭电源 1 = 上电
	7	右声道数模转换器	0	右声道数模转换器 0 = 关闭电源 1 = 上电
	6	左输出1	0	左输出1缓冲器 0 = 关闭电源 1 = 上电
	5	右输出1	0	右输出1缓冲器 0 = 关闭电源 1 = 上电
	4	SPKL	0	SPK_LP/SPK_LN输出可编程增益放大器 0 = 关闭电源 1 = 上电 (注意：扬声器输出还需设置 SPK_OP_EN[0])
	3	SPKR	0	SPK_RP/SPK_RN输出可编程增益放大器  0 = 关闭电源 1 = 上电 (注意：扬声器输出还需设置 SPK_OP_EN[1])
	1	OUT3	0	OUT3输出缓冲器 0 = 关闭电源 1 = 上电
	0	锁相环使能	0	锁相环启用 0 = 关闭电源 1 = 上电
R47 (2Fh) 电源 管理 (3)	5	左麦克风输入控制		左声道输入可编程增益放大器使能 0 = 关闭电源 1 = 上电 (注意：需同时设置AINL)
	4	右麦克风输入控制		右声道输入可编程增益放大器使能 0 = 关闭电源 1 = 上电 (注意：需同时设置AINR)
	3	LOMIX		左声道输出混频器使能 0 = 关闭电源 1 = 上电
	2	ROMIX		右输出混频器使能 0 = 关闭电源 1 = 上电

表47 电源管理

### STOPPING THE MASTER CLOCK

In order to minimise power consumed in the digital core of the WM8960, the master clock may be stopped in Standby and OFF modes. If this cannot be done externally at the clock source, the DIGENB bit (R25, bit 0) can be set to stop the MCLK signal from propagating into the device core. In Standby mode, setting DIGENB will typically provide an additional power saving on DCVDD of 20uA. However, since setting DIGENB has no effect on the power consumption of other system components external to the WM8960, it is preferable to disable the master clock at its source wherever possible.

**MCLK should not be stopped while the class D outputs are enabled, as this would prevent the outputs from functioning.**

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Additional Control (1)	0	DIGENB	0	Master clock disable 0 = Master clock enabled 1 = Master clock disabled

Table 48 Enabling the Master Clock

**NOTE:** Before DIGENB can be set, the control bits ADCL, ADCR, DACL and DACR must be set to zero and a waiting time of 1ms must be observed. Any failure to follow this procedure may prevent DACs and ADCs from re-starting correctly.

### SAVING POWER AT HIGHER SUPPLY VOLTAGE

The AVDD supply of the WM8960 can operate between 2.7V and 3.6V. By default, all analogue circuitry on the device is optimized to run at 3.3V. This set-up is also good for all other supply voltages down to 2.7V. At lower voltages, performance can be improved by increasing the bias current by setting VSEL[1:0] = 01. If low power operation is preferred the bias current can be left at the default setting. This is controlled as shown below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	7:6	VSEL [1:0]	11	Analogue Bias Optimisation 00 = Reserved 01 = Increased bias current optimized for AVDD=2.7V 1X = Lowest bias current, optimized for AVDD=3.3V

Table 49 Bias Optimisation

### 停止主时钟

为最大限度降低WM8960数字核心的功耗，在待机模式和关闭模式下可停止主时钟。若无法在时钟源外部实现此操作，可通过设置DIGENB位（R25，位0）来阻止MCLK信号传入器件核心。在待机模式下，设置DIGENB通常可额外节省DCVDD端20微安的功耗。

然而，由于设置DIGENB对WM8960外部其他系统组件的功耗无影响，因此建议尽可能在时钟源处禁用主时钟。

**启用D类输出时不应停止MCLK，否则将导致输出功能失效。**

寄存器地址	位	标签	默认值	描述
R25 (19h) 附加控制 (1)	0	数字使能	0	主时钟禁用控制 0 = 主时钟启用 1 = 主时钟禁用

表48 主时钟启用方法

**注意：**在设置DIGENB之前，必须将控制位ADCL、ADCR、DACL和DSCR设置为零，并保持1ms的等待时间。如未遵循此流程，可能导致数模转换器(DACs)和模数转换器(ADCs)无法正确重启。

### 在较高电源电压下节省功耗

WM8960的AVDD供电可在2.7V至3.6V范围内工作。默认情况下，器件上的所有模拟电路均优化为3.3V运行。此配置同样适用于低至2.7V的其他供电电压。在较低电压下，通过设置VSEL[1:0]=01增加偏置电流可提升性能。若优先考虑低功耗运行，可保持偏置电流的默认设置。具体控制方式如下所示。

寄存器地址	位	标签	默认值	描述
R23 (17h) 附加 控制位 (1)	7:6	VSEL [1:0]	11	模拟偏置优化 00 = 保留 01 = 增强偏置电流优化方案（适用于AVDD=2.7V） 1X = 最低偏置电流配置（优化用于AVDD=3.3V）

表49 偏置优化设置

## REGISTER MAP

REGISTER	remarks	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	default
R0 (00h)	Left Input volume	IPVU	LINMUTE	LIZC			LINVOL[5:0]				0_1001_0111
R1 (01h)	Right Input volume	IPVU	RINMUTE	RIZC			RINVOL[5:0]				0_1001_0111
R2 (02h)	ROUT1 volume	OUT1VU	LO1ZC			LOUT1VOL[6:0]					0_0000_0000
R3 (03h)	ROUT1 volume	OUT1VU	RO1ZC			ROUT1VOL[6:0]					0_0000_0000
R4 (04h)	Clocking (1)		ADCDIV[2:0]		DACDIV[2:0]		SYSCLKDIV[1:0]		CLKSEL		0_0000_0000
R5 (05h)	ADC & DAC Control (CTR1)	0	DACDIV2	ADCPOL[1:0]	0	DACMU	DEEMPH[1:0]		ADCHPD		0_0000_1000
R6 (06h)	ADC & DAC Control (CTR2)	0	0	DACPOL[1:0]	0	DACSMM	DACMR	DACSLOPE	0		0_0000_0000
R7 (07h)	Audio Interface	ALRswap	BCLKINV	MS	DLRSWAP	LRP	WL[1:0]		FORMAT[1:0]		0_0000_1010
R8 (08h)	Clocking (2)		DCLKDIV[2:0]	0	0		BCLKDIV[3:0]				1_1100_0000
R9 (09h)	Audio Interface	0	0	ALRCGPIO	WL8	DACCOMP[1:0]	ADCCOMP[1:0]		LOOPBACK		0_0000_0000
R10 (0Ah)	Left DAC volume	DACVU				LDACVOL[7:0]					0_1111_1111
R11 (0Bh)	Right DAC volume	DACVU				RDACVOL[7:0]					0_1111_1111
R12 (0Ch)	Reserved	0	0	0	0	0	0	0	0		0_0000_0000
R13 (0Dh)	Reserved	0	0	0	0	0	0	0	0		0_0000_0000
R14 (0Eh)	Reserved	0	0	0	0	0	0	0	0		0_0000_0000
R15 (0Fh)	Reset				writing to this register resets all registers to their default state						not reset
R16 (10h)	3D control	0	0	3DUC	3DLC		3DDEPTH[3:0]		3DEN		0_0000_0000
R17 (11h)	ALC1		ALCSEL[1:0]		MAGXGAIN[2:0]		ALCL[3:0]				0_0111_1011
R18 (12h)	ALC2	1	0		MINGAIN[2:0]		HLD[3:0]				1_0000_0000
R19 (13h)	ALC3		ALCMODE		DCY[3:0]		ATK[3:0]				0_0011_0010
R20 (14h)	Noise Gate	0			NGTH[4:0]		0	0	NGAT		0_0000_0000
R21 (15h)	Left ADC volume	ADCVU				LADCVOL[7:0]					0_1100_0011
R22 (16h)	Right ADC volume	ADCVU				RADCVOL[7:0]					0_1100_0011
R23 (17h)	Additional control(1)	TSDEN	VSEL[1:0]	0	DMONOMIX	DATSEL[1:0]	TOCLKSEL	TOEN			1_1100_0000
R24 (18h)	Additional control(2)	0	0	HPSWEN	HPSWPOL	0	TRIS	LRCM	0	0	0_0000_0000
R25 (19h)	Pwr Mgmt (1)		VMIDSEL[1:0]	VREF	AINL	AINR	ADCL	ADCR	MICB	DIGENB	0_0000_0000
R26 (1Ah)	Pwr Mgmt (2)	DACL	DACR	LOUT1	ROUT1	SPKL	SPKR	0	OUT3	PLL_EN	0_0000_0000
R27 (1Bh)	Additional Control (3)	0	0	VROI	0	0	OUT3CAP		ADC_ALC_SR[2:0]		0_0000_0000
R28 (1Ch)	Anti-pop 1	0	POBCTRL	0	0	BUFDOPEN	BUFIOEN	SOFT_ST	0	HPSTBY	0_0000_0000
R29 (1Dh)	Anti-pop 2	0	0	DISOP	DRES[1:0]	0	0	0	0		0_0000_0000
R30 (1Eh)	Reserved	0	0	0	0	0	0	0	0		0_0000_0000
R31 (1Fh)	Reserved	0	0	0	0	0	0	0	0		0_0000_0000
R32 (20h)	ADCL signal path	LMN1	LMP3	LMP2	LMICBOOST[1:0]	LMIC2B	0	0	0		1_0000_0000
R33 (21h)	ADCR signal path	RMN1	RMP3	RMP2	RMICBOOST[1:0]	RMIC2B	0	0	0		1_0000_0000
R34 (22h)	Left out Mix (1)	LD2LO	LI2LO	LI2LOVOL[2:0]	0	0	0	0	0		0_0101_0000
R35 (23h)	Reserved	0	0	1	0	1	0	0	0		0_0101_0000
R36 (24h)	Reserved	0	0	1	0	1	0	0	0		0_0101_0000
R37 (25h)	Right out Mix (2)	RD2RO	RI2RO	RI2ROVOL[2:0]	0	0	0	0	0		0_0101_0000
R38 (26h)	Mono out Mix (1)	0	L2MO	0	0	0	0	0	0		0_0000_0000
R39 (27h)	Mono out Mix (2)	0	R2MO	0	0	0	0	0	0		0_0000_0000
R40 (28h)	LOUT2 volume	SPKVU	SPKLZC			SPKLVOL[6:0]					0_0000_0000
R41 (29h)	ROUT2 volume	SPKVU	SPKRZC			SPKRVOL[6:0]					0_0000_0000
R42 (2Ah)	MONOOUT volume	0	0	MOUTVOL	0	0	0	0	0		0_0100_0000
R43 (2Bh)	Input boost mixer (1)	0	0		LIN3BOOST[2:0]		LIN2BOOST[2:0]				0_0000_0000
R44 (2Ch)	Input boost mixer (2)	0	0		RIN3BOOST[2:0]		RIN2BOOST[2:0]				0_0000_0000
R45 (2Dh)	Bypass (1)	0	LB2LO	LB2LOVOL[2:0]	0	0	0	0	0		0_0101_0000
R46 (2Eh)	Bypass (2)	0	RB2RO	RB2ROVOL[2:0]	0	0	0	0	0		0_0101_0000
R47 (2Fh)	Pwr Mgmt (3)	0	0	LMIC	RMIC	LOMIX	ROMIX	0	0		0_0000_0000
R48 (30h)	Additional Control (4)	0	GPIOPOL	GPIOSEL[2:0]		HPSEL[1:0]	TSENSEN	MBSEL			0_0000_0010
R49 (31h)	Class D Control (1)	0	SPK_OP_EN[1:0]	1	1	0	1	1	1		0_0011_0111
R50 (32h)	Reserved	0	0	1	0	0	1	1	0		0_0100_1101
R51 (33h)	Class D Control (3)	0	1	0	DCGAIN[2:0]		ACGAIN[2:0]				0_1000_0000
R52 (34h)	PLL N		OPCLKDIV[2:0]	SDM	PLLRESCALE		PLLN[3:0]				0_0000_1000
R53 (35h)	PLL K 1	0				PLLK[23:16]					0_0011_0001
R54 (36h)	PLL K 2	0				PLLK[15:8]					0_0010_0110
R55 (37h)	PLL K 3	0				PLLK[7:0]					0_1110_1001

## 寄存器映射表

寄存器	备注	位[8]	位[7]	位[6]	位[5]	位[4]	位[3]	位[2]	位[1]	位[0]	默认值
R0 (00h)	左输入音量	IPVU	线路静音	左输入麦克风检测			左输入音量[5:0]				0_1001_0111
R1 (01h)	右输入音量	IPVU	右输入静音	右输入麦克风检测			右输入音量[5:0]				0_1001_0111
R2 (02h)	左输出1音量	OUT1VU	LO1ZC				左输出1音量[6:0]				0_0000_0000
R3 (03h)	右输出1音量	OUT1VU	RO1ZC				右输出1音量[6:0]				0_0000_0000
R4 (04h)	时钟配置(1)		模数转换器分频器[2:0]		数模转换器分频器[2:0]		系统时钟分频器[1:0]	CLKSEL			0_0000_0000
R5 (05h)	模数转换器与数模转换器控制 (CTR1)	0	DACDIV2	ADCPOL[1:0]	0	0	去加重[1:0]	ADCHPD			0_0000_1000
R6 (06h)	模数转换器与数模转换器控制 (CTR2)	0	0	DACPOL[1:0]	0	0	DAC主控右声道	DACSLOPE	0		0_0000_0000
R7 (07h)	音频接口	ALRSWAP	BCLKINV	MS	DLRSWAP	LRP	WL[1:0]		FORMAT[1:0]		0_0000_1010
R8 (08h)	时钟配置(2)		数字时钟分频器[2:0]	0	0		BCLKDIV[3:0]				1_1100_0000
R9 (09h)	音频接口	0	0	ALRCGPIO	WL8		DAC补偿[1:0]	模数转换器补偿[1:0]	数字回环		0_0000_0000
R10 (0Ah)	左DAC音量	DACVU					LDAC音量[7:0]				0_1111_1111
R11 (0Bh)	右DAC音量	DACVU					右DAC音量[7:0]				0_1111_1111
R12 (0Ch)	保留	0	0	0	0	0	0	0	0		0_0000_0000
R13 (0Dh)	保留	0	0	0	0	0	0	0	0		0_0000_0000
R14 (0Eh)	保留	0	0	0	0	0	0	0	0		0_0000_0000
R15 (0Fh)	复位						写入该寄存器会将所有寄存器重置为默认状态				非复位
R16 (10h)	3D控制	0	0	3DUC	3DLC		3D深度[3:0]		3D使能		0_0000_0000
R17 (11h)	ALC1		自动电平控制选择[1:0]		最大增益[2:0]			自动电平控制电平[3:0]			0_0111_1011
R18 (12h)	ALC2	1	0		最小增益[2:0]			保持时间[3:0]			1_0000_0000
R19 (13h)	ALC3		ALCMODE		衰减时间[3:0]			启动时间[3:0]			0_0011_0010
R20 (14h)	噪声门	0			噪声门限[4:0]		0	0	NGAT		0_0000_0000
R21 (15h)	左模数转换器音量	ADC音量更新			左ADC音量[7:0]						0_1100_0011
R22 (16h)	右模数转换器音量	ADC音量更新			右ADC音量[7:0]						0_1100_0011
R23 (17h)	附加控制(1)		TSD电压选择[1:0]			0DMONOMIX 数据选择[1:0]		KSEDC	超时使能		1_1100_0000
R24 (18h)	附加	控制(2)	HRSWEN	耳机开关极性	0	TRIS	LRCM	0	0		0_0000_0000
R25 (19h)	电源管理(1)		VMD选择[1:0]	VREF	AINL	AINR	ADCL	ADCR	MICB	数字使能	0_0000_0000
R26 (1Ah)	电源管理	(2)			右声道数模转换器	左输出1	右输出1	SPKL	SPKR	LL_ENOO	JT0_0000_0B00
R27 (1Bh)	附加	控制	(3)	0ROI	0	OUT3电容			模数转换器自动电平控制采样率[2:0]		0_0000_0000
R28 (1Ch)	抗爆音	1	OPOBCTRL	0 0	BUFDOPEN	BUFOEN	SOFT_ST	0	HPSTBY		0_0000_0000
R29 (1Dh)	防爆音2	0	0	DISOP	驱动电阻选择[1:0]	0	0	0	0		0_0000_0000
R30 (1Eh)	保留	0	0	0	0	0	0	0	0		0_0000_0000
R31 (0_0 (1Fh))	0 保留 0	0	0	0 00000000							
R32 (20h)	ADCL信号路径	LMN1	LMP3	左麦克风路径2	左麦克风输入控制升压电路[1:0]	左麦克风输入控制升压电容[2:0]	0	0	0		1_0000_0000
R33 (21h)	ADCR信号路径	RMN1	RMP3	RMP2	右麦克风输入控制升压电路[1:0]	RMIC2B	0	0	0		1_0000_0000
R34 (22h)	左输出混音器(1)	LD2LO	LI2LO	左I2L输出音量[2:0]	0	0	0	0	0		0_0101_0000
R35 (23h)	保留	0	0	1_001	10 01_0	0000					
R36 (24h)	保留	0	0	1_001	10 01_0	0000					
R37 (25h)	右输出混音(2)	RD2RO	RI2RO		右I2R输出音量[2:0]	0	0	0	0		0_0101_0000
R38 (26h)	单声道输出混音(1)	0	L2MO	0	0	0	0	0	0		0_0000_0000
R39 (27h)	单声道输出混音(2)	0	R2MO	0	0	0	0	0	0		0_0000_0000
R40 (28h)	左输出2音量	SPKVU	SPKLZC		左扬声器音量[6:0]						0_0000_0000
R41 (29h)	右输出2音量	SPKVU	SPKRZC		右扬声器音量[6:0]						0_0000_0000
R42 (2Ah)	单声道输出	音量		主输出音量	0	0	0	0	0		0_0100_0000
R43 (2Bh)	输入	升压电路	混音器	(1) 左输入3升压电路[2:0]	00		左输入2升压电路[2:0]		0		0_0000_0000
R44 (2Ch)	输入	升压电路	混音器	(2) 右输入3升压电路[2:0]	00		右输入2升压电路[2:0]		0		0_0000_0000
R45 (2Dh)	旁路(1)	0	LB2LO	LB2LOVOL[2:0]	0	0	0	0	0		0_0101_0000
R46 (2Eh)	旁路(2)	0	RB2RO	右B2R输出音量[2:0]	0	0	0	0	0		0_0101_0000
R47 (2Fh)	电源管理(3)	0	0	0	0	右麦克风输入控制	右麦克风输入控制	LOMIX	ROMIX	0	0_0000_0000
R48 (30h)	附加控制(4)	0	GPIO极性	GPIO选择[2:0]		HPSEL[1:0]		TSENSEN	MBSEL		0_0000_0010
R49 (31h)	D类控制(1)	0	SPK_OPE_N[1:0]	1 1	0	1	1	1	1	1	0_0011_0111
R50 (32h)	保留	0	0	1	0	0	1	1	0	1	0_0100_1101
R51 (33h)	类别	D	控制	(3)	增益控制[2:0]	0		交流增益[2:0]			0_1000_0000
R52 (34h)	锁相环N		OPCLKDIV[2:0]	SDM	锁相环重缩放			PLLNN[3:0]			0_0000_1000
R53 (35h)	锁相环K1	0				锁相环K值[23:16]					0_0011_0001
R54 (36h)	锁相环K2	0			PLLK[15:8]						0_0010_0110
R55 (37h)	锁相环K3	0			PLLK[7:0]						0_1110_1001

**REGISTER BITS BY ADDRESS**

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R0 (00h) Left Input Volume	8	IPVU	N/A	Input PGA Volume Update Writing a 1 to this bit will cause left and right input PGA volumes to be updated (LINVOL and RINVOL)	Input Signal Path
	7	LINMUTE	1	Left Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IPVU must be set to un-mute.	Input Signal Path
	6	LIZC	0	Left Input PGA Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately	Input Signal Path
	5:0	LINVOL[5:0]	010111	Left Input PGA Volume Control 111111 = +30dB 111110 = +29.25dB .. 0.75dB steps down to 000000 = -17.25dB	Input Signal Path
R1 (01h) Right Input Volume	8	IPVU	N/A	Input PGA Volume Update Writing a 1 to this bit will cause left and right input PGA volumes to be updated (LINVOL and RINVOL)	Input Signal Path
	7	RINMUTE	1	Right Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IPVU must be set to un-mute.	Input Signal Path
	6	RIZC	0	Right Input PGA Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately	Input Signal Path
	5:0	RINVOL[5:0]	010111	Right Input PGA Volume Control 111111 = +30dB 111110 = +29.25dB .. 0.75dB steps down to 000000 = -17.25dB	Input Signal Path
R2 (02h) LOUT1 Volume	8	OUT1VU	N/A	Headphone Output PGA Volume Update Writing a 1 to this bit will cause left and right headphone output volumes to be updated (LOUT1VOL and ROUT1VOL)	Analogue Outputs
	7	LO1ZC	0	Left Headphone Output Zero Cross Enable 0 = Change gain immediately 1 = Change gain on zero cross only	Analogue Outputs
	6:0	LOUT1VOL[6:0]	0000000	LOUT1 Volume 1111111 = +6dB .. 1dB steps down to 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE	Analogue Outputs
R3 (03h) ROUT1 Volume	8	OUT1VU	N/A	Headphone Output PGA Volume Update Writing a 1 to this bit will cause left and right headphone output volumes to be updated (LOUT1VOL and ROUT1VOL)	Analogue Outputs
	7	RO1ZC	0	Right Headphone Output Zero Cross Enable 0 = Change gain immediately 1 = Change gain on zero cross only	Analogue Outputs

### 按地址排列的寄存器位

寄存器地址	位	标签	默认值	描述	参见
R0 (00h) 左输入音量	8	IPVU	不适用	输入PGA音量更新 向此位 写入1将触发左右输入PGA音量更新（左输入音量和右输入音量）	输入信号路径
	7	线路静音	1	左输入PGA模拟静音控制 1 = 启用静音 0 = 禁用静音控制 注意：必须设置IPVU以取消静音	输入信号路径
	6	左输入零交叉检测	0	左输入可编程增益放大器零交叉检测器 1 = 仅在零交叉时改变增益 0 = 立即改变增益	输入信号路径
	5:0	左输入音量[5:0]	010111	左输入可编程增益放大器音量控制 111111 = +30分贝 111110 = +29.25分贝 ... 以0.75分贝步进递减至 000000 = -17.25分贝	输入信号路径
R1 (01h) 右输入音量	8	IPVU	不适用	输入PGA音量更新 向此位 写入1将触发左右输入PGA音量更新（左输入音量和右输入音量）	输入信号路径
	7	右输入静音	1	右输入可编程增益放大器模拟静音 1 = 启用静音 0 = 禁用静音控制 注意：必须设置IPVU以取消静音	输入信号路径
	6	右输入零交叉检测	0	右输入可编程增益放大器过零检测器 1 = 仅在过零时改变增益 0 = 立即改变增益	输入信号路径
	5:0	右输入音量[5:0]	010111	右输入可编程增益放大器音量控制 111111 = +30分贝 111110 = +29.25分贝 ... 以0.75分贝步进递减至 000000 = -17.25分贝	输入信号路径
R2 (02h) 左输出1音量	8	OUT1VU	不适用	耳机输出可编程增益放大器音量更新 向该位写入1将使左右耳机输出音量更新（左输出1音量和右输出1音量）	模拟输出
	7	LO1ZC	0	左耳机输出过零使能 0 = 立即改变增益 1 = 仅在零交叉时改变增益	模拟输出
	6:0	左输出1音量[6:0]	0000000	左输出1音量 1111111 = +6分贝 ... 以1分贝为步进递减至 0110000 = -73分贝 0101111 至 0000000 = 模拟静音控制	模拟输出
R3 (03h) 右输出1音量	8	OUT1VU	不适用	耳机输出可编程增益放大器音量更新 向该位写入1将使左右耳机输出音量更新（左输出1音量和右输出1音量）	模拟输出
	7	RO1ZC	0	右耳机输出零交叉使能 0 = 立即改变增益 1 = 仅在零交叉时改变增益	模拟输出

# WM8960

Preliminary Technical Data

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6:0	ROUT1VOL[6:0]	0000000	ROUT1 Volume 1111111 = +6dB ... 1dB steps down to 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE	Analogue Outputs
R4 (04h) Clocking (1)	8:6	ADCDIV[2:0]	000	ADC Sample rate divider (Also determines ADCLRC in master mode) 000 = SYSCLK / (1.0 * 256) 001 = SYSCLK / (1.5 * 256) 010 = SYSCLK / (2 * 256) 011 = SYSCLK / (3 * 256) 100 = SYSCLK / (4 * 256) 101 = SYSCLK / (5.5 * 256) 110 = SYSCLK / (6 * 256) 111 = Reserved	Clocking and Sample Rates
	5:3	DACDIV[2:0]	000	DAC Sample rate divider (Also determines DACLRC in master mode) 000 = SYSCLK / (1.0 * 256) 001 = SYSCLK / (1.5 * 256) 010 = SYSCLK / (2 * 256) 011 = SYSCLK / (3 * 256) 100 = SYSCLK / (4 * 256) 101 = SYSCLK / (5.5 * 256) 110 = SYSCLK / (6 * 256) 111 = Reserved	Clocking and Sample Rates
	2:1	SYSCLKDIV[1:0]	00	SYSCLK Pre-divider. Clock source (MCLK or PLL output) will be divided by this value to generate SYSCLK. 00 = Divide SYSCLK by 1 01 = Reserved 10 = Divide SYSCLK by 2 11 = Reserved	Clocking and Sample Rates
	0	CLKSEL	0	SYSCLK Selection 0 = SYSCLK derived from MCLK 1 = SYSCLK derived from PLL output	Clocking and Sample Rates
R5 (05h) ADC and DAC Control (1)	8		0	Reserved	
	7	DACDIV2	0	DAC 6dB Attenuate Enable 0 = Disabled (0dB) 1 = -6dB Enabled	Output Signal Path
	6:5	ADCPOL[1:0]	00	ADC polarity control: 00 = Polarity not inverted 01 = ADC L inverted 10 = ADC R inverted 11 = ADC L and R inverted	Analogue to Digital Converter
	4		0	Reserved	
	3	DACMU	1	DAC Digital Soft Mute 1 = Mute 0 = No mute (signal active)	Output Signal Path
	2:1	DEEMPH[1:0]	00	De-emphasis Control 11 = 48kHz sample rate 10 = 44.1kHz sample rate 01 = 32kHz sample rate 00 = No de-emphasis	Output Signal Path

寄存器地址	位	标签	默认值	描述	参见
	6:0	右输出1音量[6:0]	0000000	右输出1音量 1111111 = +6分贝 ... 以1分贝为步进递减至 0110000 = -73分贝 0101111 至 0000000 = 模拟静音控制	模拟输出
R4 (04h) 时钟配置 (1)	8:6	模数转换器分频器[2:0]	000	模数转换器采样率分频器 (主模式下也决定ADCLRC) 000 = SYS CLK / (1.0 * 256) 001 = SYS CLK / (1.5 * 256) 010 = SYS CLK / (2 * 256) 011 = SYS CLK / (3 * 256) 100 = SYS CLK / (4 * 256) 101 = SYS CLK / (5.5 * 256) 110 = SYS CLK / (6 * 256) 111 = 保留	时钟与采样率
	5:3	数模转换器分频器[2:0]	000	DAC采样率分频器 (主模式下同时决定DA CLRC) 000 = SYSCLK/(1 .0*256) 001 = SYSCLK/(1.5 *256) 010 = SYSCLK/(2*256) 011 = SYSCLK/(3*256) 100 = SYSCLK/(4*256) 101 = SYSCLK/(5.5*256) 110 = SYSCLK/(6*256) 111 = 保留	时钟与采样率
	2:1	系统时钟分频器[1:0]	00	系统时钟预分频器。时钟源 (MCLK或锁相环输出) 将通过此值分频以生成SYSCLK。0 = SYSCLK分频比为1 01 = 保留 10 = SYSCLK分频比为2 11 = 保留	时钟与采样率
	0	CLKSEL	0	系统时钟选择 0 = SYSCLK源自MCLK 1 = SYSCLK源自PLL输出	时钟与采样率
R5 (05h) 模数转换器与 数模转换器 控制 (1)	8		0	保留	
	7	DACDIV2	0	数模转换器6分贝衰减启用 0 = 禁用 (0分贝) 1 = 启用-6分贝衰减	输出信号路径
	6:5	ADCPOL[1:0]	00	模数转换器极性控制: 00 = 极性未反相 01 = 左通道模数转换器反相 10 = 右通道模数转换器反相 11 = 左右通道模数转换器均反相	模数转换器
	4		0	保留	
	3	数模转换器静音控制单元	1	数模转换器数字软静音 1 = 静音 0 = 非静音 (信号激活)	输出信号路径
	2:1	去加重[1:0]	00	去加重控制 11 = 48千赫采样率 10 = 44.1千赫采样率 01 = 32千赫采样率 00 = 无去加重	输出信号路径

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	ADCHPD	0	ADC High Pass Filter Disable 0 = Enable high pass filter on left and right channels 1 = Disable high pass filter on left and right channels	Analogue to Digital Converter
R6 (06h) ADC and DAC Control (2)	8:7		00	Reserved	
	6:5	DACPOL[1:0]	00	DAC polarity control: 00 = Polarity not inverted 01 = DAC L inverted 10 = DAC R inverted 11 = DAC L and R inverted	Output Signal Path
	4		0	Reserved	
	3	DACSMM	0	DAC Soft Mute Mode 0 = Disabling soft-mute (DACMU=0) will cause the volume to change immediately to the LDACVOL / RDACVOL settings 1 = Disabling soft-mute (DACMU=0) will cause the volume to ramp up gradually to the LDACVOL / RDACVOL settings	Output Signal Path
	2	DACMR	0	DAC Soft Mute Ramp Rate 0 = Fast ramp (24kHz at fs=48k, providing maximum delay of 10.7ms) 1 = Slow ramp (1.5kHz at fs=48k, providing maximum delay of 171ms)	Output Signal Path
	1	DACSLOPE	0	Selects DAC filter characteristics 0 = Normal mode 1 = Sloping stopband	Output Signal Path
	0		0	Reserved	
	8	ALRSWAP	0	Left/Right ADC Channel Swap 1 = Swap left and right ADC data in audio interface 0 = Output left and right data as normal	Audio Interface Control
R7 (07h) Audio Interface	7	BCLKINV	0	BCLK invert bit (for master and slave modes) 0 = BCLK not inverted 1 = BCLK inverted	Audio Interface Control
	6	MS	0	Master / Slave Mode Control 0 = Enable slave mode 1 = Enable master mode	Audio Interface Control
	5	DLRSWAP	0	Left/Right DAC Channel Swap 0 = Output left and right data as normal 1 = Swap left and right DAC data in audio interface	Audio Interface Control
	4	LRP	0	Right, left and I <sup>2</sup> S modes – LRCLK polarity 0 = normal LRCLK polarity 1 = invert LRCLK polarity	Audio Interface Control
				DSP Mode – mode A/B select 0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A) 1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B)	
	3:2	WL[1:0]	10	Audio Data Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits (see Note)	Audio Interface Control

寄存器地址	位	标签	默认值	描述	参见
	0	ADCHPD	0	模数转换器高通滤波器禁用 0 = 启用左右声道高通滤波器 1 = 禁用左右声道高通滤波器	模数转换器
R6 (06h) ADC与DAC控制(2)	8:7		00	保留	
	6:5	DACPOL[1:0]	00	数模转换器极性控制： 00 = 极性未反相 01=左DAC反相 10=右DAC反相 11=左右DAC均反相	输出信号路径
	4		0	保留	
	3	数模转换器模拟电源管理模块	0	数模转换器软静音模式 0 = 禁用软静音 (DACMU=0) 将导致音量立即切换至LDAC音量/右DAC音量设置 1 = 禁用软静音 (DACMU=0) 将导致音量渐增强至LDAC音量/右DAC音量设置	输出信号路径
	2	DAC主控右声道	0	DAC软静音斜坡速率 0 = 快速斜坡 (在fs=48k时24kHz, 提供最大10.7ms延迟) 1 = 慢速斜坡 (在fs=48k时1.5kHz, 提供最大171ms延迟)	输出信号路径
	1	DACSLOPE	0	选择DAC滤波器特性 0 = 正常模式 1 = 倾斜阻带	输出信号路径
	0		保留		
R7 (07h) 音频接口	8	ALRSWAP	0	左/右ADC通道交换 1 = 在音频接口中交换左右ADC数据 0 = 正常输出左右声道数据	音频接口控制
	7	BCLKINV	0	BCLK反相位控制位 (主从模式适用) 0 = BCLK不反相 1 = BCLK反相	音频接口控制
	6	MS	0	主/从模式控制 0 = 启用从模式 1 = 启用主模式	音频接口控制
	5	DLRSWAP	0	左/右DAC通道交换 0 = 正常输出左右声道数据 1 = 在音频接口中交换左右DAC数据	音频接口控制
	4	LRP	0	右、左和I <sup>2</sup> S模式 - LRCLK极性 0 = 正常LRCLK极性 1 = 反转LRCLK极性  DSP模式 - 模式A/B选择 0 = M SB在LRC上升沿后的第二个BCLK上升沿有效 (模式A) 1 = MSB在LRC上升沿后的第一个BCLK上升沿有效 (模式B)	音频接口控制
	3:2	WL[1:0]	10	音频数据字长 00 = 16位 01 = 20位 10 = 24位 11 = 32位 (参见注释)	音频接口控制

# WM8960

Preliminary Technical Data

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1:0	FORMAT[1:0]	10	00 = Right justified 01 = Left justified 10 = I <sup>2</sup> S Format 11 = DSP Mode	Audio Interface Control
R8 (08h) Clocking (2)	8:6	DCLKDIV[2:0]	111	Class D switching clock divider. 000 = SYSCLK / 1.5 (Not recommended) 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16	Class D Speaker Outputs; Clocking and Sample Rates
	5:4		00	Reserved	
	3:0	BCLKDIV[3:0]	0000	BCLK Frequency (Master Mode) 0000 = SYSCLK 0001 = SYSCLK / 1.5 0010 = SYSCLK / 2 0011 = SYSCLK / 3 0100 = SYSCLK / 4 0101 = SYSCLK / 5.5 0110 = SYSCLK / 6 0111 = SYSCLK / 8 1000 = SYSCLK / 11 1001 = SYSCLK / 12 1010 = SYSCLK / 16 1011 = SYSCLK / 22 1100 = SYSCLK / 24 1101 to 1111 = SYSCLK / 32	Clocking and Sample Rates
R9 (09h) Audio Interface	8:7		00	Reserved	
	6	ALRCGPIO	0	ADCLRC/GPIO1 Pin Function Select 0 = ADCLRC frame clock for ADC 1 = GPIO pin	General Purpose Input / Output; Digital Audio Interface
	5	WL8	0	8-Bit Word Length Select (Used with companding) 0 = Off 1 = Device operates in 8-bit mode.	Audio Interface Control
	4:3	DACCOMP[1:0]	00	DAC companding 00 = off 01 = reserved 10 = μ-law 11 = A-law	Audio Interface Control
	2:1	ADCCOMP[1:0]	00	ADC companding 00 = off 01 = reserved 10 = μ-law 11 = A-law	Audio Interface Control
	0	LOOPBACK	0	Digital Loopback Function 0 = No loopback. 1 = Loopback enabled, ADC data output is fed directly into DAC data input.	Audio Interface Control

寄存器地址	位	标签	默认值	描述	参见
	1:0	FORMAT[1:0]	10	00 = 右对齐 01 = 左对齐 10 = I <sup>2</sup> S 格式 11 = DSP 模式	音频接口控制
R8 (08h) 时钟 (2)	8:6	数字时钟分频器[2:0]	111	D类开关时钟分频器。 000 = SYSCLK / 1.5 (不建议使用) 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16	D类扬声器输出; 时钟与采样率
	5:4		00	保留	
	3:0	BCLKDIV[3:0]	0000	BCLK频率 (主模式) 0000 = SYSCLK 0001 = SYSCLK / 1.5 0010 = SYSCLK / 2 0011 = SYSCLK / 3 0100 = SYSCLK / 4 0101 = SYSCLK / 5.5 0110 = SYSCLK / 6 0111 = SYSCLK / 8 1000 = SYSCLK / 11 1001 = SYSCLK / 12 1010 = SYSCLK / 16 1011 = SYSCLK / 22 1100 = SYSCLK / 24 1101至1111 = SYSCLK / 32	时钟与采样率
R9 (09h) 音频接口	8:7		00	保留	
	6	ALRCGPIO	0	ADCLRC/GPIO1引脚功能选择 0 = ADC的ADCLRC帧时钟 1 = 通用输入输出引脚	通用输入/ 输出; 数字音频接口
	5	WL8	0	8位字长选择 (用于压扩) 0 = 关闭  1 = 设备工作在8位模式	音频接口控制
	4:3	DAC补偿[1:0]	00	DAC压扩 00 = 关闭 01 = 保留 10 = μ律 11 = A律	音频接口控制
	2:1	模数转换器补偿[1:0]	00	ADC压扩 00 = 关闭 01 = 保留 10 = μ律 11 = A律	音频接口控制
	0	数字回环	0	数字回环功能 0 = 禁用回环 1 = 启用回环模式, ADC数据输出直接馈入DAC数据输入	音频接口控制

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R10 (0Ah) Left DAC Volume	8	DACVU	N/A	DAC Volume Update Writing a 1 to this bit will cause left and right DAC volumes to be updated (LDACVOL and RDACVOL)	Output Signal Path
	7:0	LDACVOL[7:0]	11111111	Left DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB	Output Signal Path
R11 (0Bh) Right DAC Volume	8	DACVU	N/A	DAC Volume Update Writing a 1 to this bit will cause left and right DAC volumes to be updated (LDACVOL and RDACVOL)	Output Signal Path
	7:0	RDACVOL[7:0]	11111111	Right DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB	Output Signal Path
R12 (0Ch)	8:0		00000000	Reserved	
R13 (0Dh)	8:0		00000000	Reserved	
R14 (0Eh)	8:0		00000000	Reserved	
R15 (0Fh) Reset	8:0	Reset	N/A	Writing to this register resets all registers to their default state.	
R16 {10h} 3D Control	8		0	Reserved	
	7		0	Reserved	
	6	3DUC	0	3D Enhance Filter Upper Cut-Off Frequency 0 = High (Recommended for $fs \geq 32\text{kHz}$ ) 1 = Low (Recommended for $fs < 32\text{kHz}$ )	Output Signal Path
	5	3DLC	0	3D Enhance Filter Lower Cut-Off Frequency 0 = Low (Recommended for $fs \geq 32\text{kHz}$ ) 1 = High (Recommended for $fs < 32\text{kHz}$ )	Output Signal Path
	4:1	3DDEPTH[3:0]	0000	3D Stereo Depth 0000 = 0% (minimum 3D effect) 0001 = 6.67% .... 1110 = 93.3% 1111 = 100% (maximum 3D effect)	Output Signal Path
	0	3DEN	0	3D Stereo Enhancement Enable 0 = Disabled 1 = Enabled	Output Signal Path
R17 (11h) ALC (1)	8:7	ALCSEL[1:0]	00	ALC Function Select 00 = ALC off (PGA gain set by register) 01 = Right channel only 10 = Left channel only 11 = Stereo (PGA registers unused) Note: ensure that LINVOL and RINVOL settings (reg. 0 and 1) are the same before entering this mode.	Automatic Level Control

寄存器地址	位	标签	默认值	描述	参见
R10 (0Ah) 左通道DAC音量控制	8	DACVU	不适用	DAC音量更新 向该位写入1将更新左右DAC音量 (LDACVOL和RDACVOL)	输出信号路径
	7:0	LDAC音量[7:0]	11111111	左DAC数字音量控制 0000 0000 = 数字静音 0000 0001 = -127分贝 0000 0010 = -126.5分贝 ... 以0.5分贝为步进递增至 1111 1111 = 0分贝	输出信号路径
R11 (0Bh) 右通道DAC音量控制	8	DACVU	不适用	DAC音量更新 向该位写入1将更新左右DAC音量 (LDACVOL和RDACVOL)	输出信号路径
	7:0	右DAC音量[7:0]	11111111	右通道DAC数字音量控制 0000 0000 = 数字静音 0000 0001 = -127分贝 0000 0010 = -126.5分贝 ... 每步0.5分贝递增至 1111 1111 = 0分贝	输出信号路径
R12 (0Ch)	8:0		00000000	保留	
R13 (0Dh)	8:0		00000000	保留	
R14 (0Eh)	8:0		00000000	保留	
R15 (0Fh) 复位寄存器	8:0	复位	不适用	向该寄存器写入数据将使所有寄存器恢复默认状态	
R16 (10h) 3D控制寄存器	8		0	保留	
	7		0	保留	
	6	3DUC	0	3D增强滤波器上限截止频率 0 = 高频模式 (建议用于采样频率≥32kHz) 1 = 低频模式 (建议用于采样频率<32kHz)	输出信号路径
	5	3DLC	0	3D增强滤波器下限截止频率 0 = 低频模式 (建议用于采样频率≥32kHz) 1 = 高频模式 (建议用于采样频率<32kHz)	输出信号路径
	4:1	3D深度[3:0]	0000	3D立体声深度 0000 = 0% (最小3D效果) 0001 = 6.67% ... 1110 = 93.3% 1111 = 100% (最大3D效果)	输出信号路径
	0	3D使能	0	3D立体声增强使能 0 = 禁用 1 = 启用	输出信号路径
R17 (11h) 自动电平控制(1)	8:7	自动电平控制选择[1:0]	00	ALC功能选择 00 = ALC关闭 (PGA增益由寄存器设置) 01 = 仅右声道 10 = 仅左声道 11 = 立体声模式 (PGA寄存器未使用) 注意： 进入此模式前需确保LINVOL和RINVOL设置 (寄存器0和1) 保持一致	自动电平控制

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6:4	MAXGAIN[2:0]	0000	Set Maximum Gain of PGA (During ALC operation) 111 : +30dB 110 : +24dB ....(-6dB steps) 001 : -6dB 000 : -12dB	Automatic Level Control
	3:0	ALCL[3:0]	1011	ALC Target (Sets signal level at ADC input) 0000 = -22.5dB FS 0001 = -21.0dB FS ... (1.5dB steps) 1101 = -3.0dB FS 1110 = -1.5dB FS 1111 = -1.5dB FS	Automatic Level Control
R18 (12h)	8		1	Reserved	
ALC (2)	7		0	Reserved	
	6:4	MINGAIN[2:0]	000	Set Minimum Gain of PGA (During ALC operation) 000 = -17.25dB 001 = -11.25dB 010 = -5.25dB 011 = +0.75dB 100 = +6.75dB 101 = +12.75dB 110 = +18.75dB 111 = +24.75dB	Automatic Level Control
	3:0	HLD[3:0]	0000	ALC hold time before gain is increased. 0000 = 0ms 0001 = 2.67ms 0010 = 5.33ms ... (time doubles with every step) 1111 = 43.691s	Automatic Level Control
R19 (13h)	8	ALCMODE	0	Determines the ALC mode of operation: 0 = ALC mode 1 = Limiter mode	Automatic Level Control
ALC (3)	7:4	DCY[3:0]	0011	ALC decay (gain ramp-up) time 0000 = 24ms 0001 = 48ms 0010 = 96ms ... (time doubles with every step) 1010 or higher = 24.58s	Automatic Level Control
3:0	ATK[3:0]	0010	ALC attack (gain ramp-down) time 0000 = 6ms 0001 = 12ms 0010 = 24ms ... (time doubles with every step) 1010 or higher = 6.14s	Automatic Level Control	
R20 (14h)	8		0	Reserved	
Noise Gate	7:3	NGTH[4:0]	00000	Noise gate threshold 00000 -76.5dBfs 00001 -75dBfs ... 1.5 dB steps 11110 -31.5dBfs 11111 -30dBfs	Automatic Level Control
	2:1		00	Reserved	

寄存器地址	位	标签	默认值	描述	参见
	6:4	最大增益[2:0]	0000	设置PGA最大增益 (ALC工作时) 111 : +30分贝 1 10 : +24分贝 ... (每步-6分贝) 001 : -6分贝 000 : -12分贝	自动电平控制
	3:0	自动电平控制电平[3:0]	1011	ALC目标值 (设置模数转换器输入信号电平) 0000 = -22.5分贝 FS 0001 = -21.0分贝 FS ... (1.5分贝步进) 1101 = -3.0分贝 FS 1110 = -1.5分贝 FS 1111 = -1.5分贝 FS	自动电平控制
R18 (12h) ALC (2)	8		1	保留	
	7		0	保留	
	6:4	最小增益[2:0]	000	设置PGA最小增益 (ALC工作时) 000 = -17.25分贝 001 = -11.25分贝 010 = -5.25分贝 011 = +0.75分贝 100 = +6.75分贝 101 = +12.75分贝 110 = +18.75分贝 11 = +24.75分贝	自动电平控制
	3:0	保持时间[3:0]	0000	增益提升前ALC保持时间 0000 = 0毫秒 0001 = 2.67毫秒 0010 = 5.33毫秒 ... (每步时间加倍) 1111 = 43.691秒	自动电平控制
	8	ALCMODE	0	确定ALC的工作模式： 0 = ALC模式 1 = 限幅器模式	自动电平控制
R19 (13h) 自动电平控制 (3)	7:4	衰减时间[3:0]	0011	ALC衰减 (增益上升) 时间 0000 = 24毫秒 0001 = 48毫秒 0010 = 96毫秒 ... (每步时间加倍) 1010 或更高值 = 24.58秒	自动电平控制
	3:0	启动时间[3:0]	0010	ALC启动 (增益下降) 时间 0000 = 6毫秒 0001 = 12毫秒 0010 = 24毫秒 ... (每步时间加倍) 1010 或更高值 = 6.14秒	自动电平控制
	8		0	保留	
R20 (14h) 噪声门	7:3	噪声门限[4:0]	00000	噪声门限阈值 00000 = -76.5dBfs 00001 = -75dBfs ... 1.5分贝步进 11110 = -31.5dBfs 11111 = -30dBfs	自动电平控制
	2:1		00	保留	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	NGAT	0	Noise gate function enable 0 = disable 1 = enable	Automatic Level Control
R21 (15h) Left ADC Volume	8	ADCVU	N/A	ADC Volume Update Writing a 1 to this bit will cause left and right ADC volumes to be updated (LADCVOL and RADCVOL)	Analogue to Digital Converter
	7:0	LADCVOL[7:0]	11000011	Left ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -97dB 0000 0010 = -96.5dB ... 0.5dB steps up to 1111 1111 = +30dB	Analogue to Digital Converter
R22 (16h) Right ADC Volume	8	ADCVU	N/A	ADC Volume Update Writing a 1 to this bit will cause left and right ADC volumes to be updated (LADCVOL and RADCVOL)	Analogue to Digital Converter
	7:0	RADCVOL[7:0]	11000011	Right ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -97dB 0000 0010 = -96.5dB ... 0.5dB steps up to 1111 1111 = +30dB	Analogue to Digital Converter
R23 (17h) Additional Control (1)	8	TSDEN	1	Thermal Shutdown Enable 0 = Thermal shutdown disabled 1 = Thermal shutdown enabled (TSENSE must be enabled for this function to work)	Thermal Shutdown
	7:6	VSEL[1:0]	11	Analogue Bias Optimisation 00 = Reserved 01 = Increased bias current optimized for AVDD=2.7V 1X = Lowest bias current, optimized for AVDD=3.3V	Power Management
	5		0	Reserved	
	4	DMONOMIX	0	DAC Mono Mix 0 = Stereo 1 = Mono (Mono MIX output on enabled DACs)	Output Signal Path
	3:2	DATSEL[1:0]	00	ADC Data Output Select 00: left data = left ADC; right data = right ADC 01: left data = left ADC; right data = left ADC 10: left data = right ADC; right data = right ADC 11: left data = right ADC; right data = left ADC	Analogue to Digital Converter
	1	TOCLKSEL	0	Slow Clock Select (Used for volume update timeouts and for jack detect debounce) 0 = SYSCLK / 2 <sup>21</sup> (Slower Response) 1 = SYSCLK / 2 <sup>19</sup> (Faster Response)	Volume Updates; Headphone Jack Detect
	0	TOEN	0	Enables Slow Clock for Volume Update Timeout and Jack Detect Debounce 0 = Slow clock disabled 1 = Slow clock enabled	Volume Updates; Headphone Jack Detect
	8:7		00	Reserved	
	6	HPSWEN	0	Headphone Switch Enable 0 = Headphone switch disabled 1 = Headphone switch enabled	Headphone Jack Detect
R24 (18h) Additional Control (2)					

寄存器地址	位	标签	默认值	描述	参见
	0	NGAT	0	噪声门功能使能 0 = 禁用 1 = 启用	自动电平控制
R21 (15h) 左ADC音量	8	ADC音量更新	不适用	ADC 音量更新 向该位写入1将更新左右ADC音量 (LADCVOL和RADCVOL)	模数转换器
	7:0	左ADC音量[7:0]	11000011	左ADC数字音量控制 0000 0000 = 数字静音 0000 0001 = -97分贝 0000 0010 = -96.5分贝 ... 以0.5分贝为步进递增至 1111 1111 = +30分贝	模数转换器
R22 (16h) 右ADC音量	8	ADC音量更新	不适用	ADC 音量更新 向该位写入1将更新左右ADC音量 (LADCVOL和RADCVOL)	模数转换器
	7:0	右ADC音量[7:0]	11000011	右ADC数字音量控制 0000 0000 = 数字静音 0000 0001 = -97分贝 0000 0010 = -96.5分贝 ... 以0.5分贝为步进递增至 1111 1111 = +30分贝	模数转换器
R23 (17h) 附加控制位(1)	8	TSDEN	1	热关断使能 0 = 禁用热关断保护 1 = 启用热关断 (需同时启用TSENSEN才能使此功能生效)	热关断
	7:6	电压选择[1:0]	11	模拟偏置优化 00 = 保留 01 = 增强偏置电流优化方案 (适用于AVDD=2.7V) 1X = 最低偏置电流配置 (优化用于AVDD=3.3V)	电源管理
	5		0	保留	
	4	DMONOMIX	0	DAC单声道混音 0=立体声 1 = 单声道 (在启用的DAC上输出单声道混合信号)	输出信号路径
	3:2	数据选择[1:0]	00	ADC数据输出选择 00: 左数据=左ADC; 右数据=右ADC 01: 左数据=左ADC; 右数据=左ADC 10: 左数据=右ADC; 右数据=右ADC 11: 左数据=右ADC; 右数据=左ADC	模数转换器
	1	慢时钟选择	0	慢时钟选择 (用于音量更新超时和插孔检测去抖) 0 = SYSCLK / 2 <sup>21</sup> (响应较慢) 1 = SYSCLK / 2 <sup>19</sup> (响应较快)	音量更新; 耳机插孔检测
	0	超时使能	0	启用慢时钟用于音量更新超时和插孔检测防抖 0 = 慢时钟禁用 1 = 慢时钟启用	音量更新; 耳机插孔检测
	8:7		00	保留	
	6	耳机开关使能	0	耳机开关使能 0 = 耳机开关禁用 1 = 耳机开关使能	耳机插孔检测
R24 (18h) 附加控制寄存器(2)					

# WM8960

Preliminary Technical Data

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	5	HPSWPOL	0	Headphone Switch Polarity 0 = HPDETECT high = headphone 1 = HPDETECT high = speaker	Headphone Jack Detect
	4			Reserved	
	3	TRIS	0	Tristates ADCDAT and switches ADCLRC, DACLRC and BCLK to inputs. 0 = ADCDAT is an output; ADCLRC, DACLRC and BCLK are inputs (slave mode) or outputs (master mode) 1 = ADCDAT is tristated; DACLRC and BCLK are inputs; ADCLRC is an input (when not configured as a GPIO)	Audio Interface Control
	2	LCRM	0	Selects disable mode for ADCLRC and DACLRC (Master mode) 0 = ADCLRC disabled when ADC (Left and Right) disabled; DACLRC disabled when DAC (Left and Right) disabled. 1 = ADCLRC and DACLRC disabled only when ADC (Left and Right) and DAC (Left and Right) are disabled.	Audio Interface Control
	1:0		0	Reserved	
R25 (19h) Power Mgmt (1)	8:7	VMDSEL[1:0]	00	Vmid Divider Enable and Select 00 = Vmid disabled (for OFF mode) 01 = 2 x 50kΩ divider enabled (for playback / record) 10 = 2 x 250kΩ divider enabled (for low-power standby) 11 = 2 x 5kΩ divider enabled (for fast start-up)	Power Management
	6	VREF	0	VREF (necessary for all other functions) 0 = Power down 1 = Power up	Power Management
	5	AINL	0	Analogue in PGA Left 0 = Power down 1 = Power up	Power Management
	4	AINR	0	Analogue in PGA Right 0 = Power down 1 = Power up	Power Management
	3	ADCL	0	ADC Left 0 = Power down 1 = Power up	Power Management
	2	ADCR	0	ADC Right 0 = Power down 1 = Power up	Power Management
	1	MICB	0	MICBIAS 0 = Power down 1 = Power up	Power Management
	0	DIGENB	0	Master Clock Disable 0 = Master clock enabled 1 = Master clock disabled	Power Management
R26 (1Ah) Power Mgmt (2)	8	DACL	0	DAC Left 0 = Power down 1 = Power up	Power Management
	7	DACR	0	DAC Right 0 = Power down 1 = Power up	Power Management

寄存器地址	位	标签	默认值	描述	参见
R25 (19h) 电源管理 (1)	5	耳机开关极性	0	耳机开关极性 0 = HPDETECT高电平表示耳机 1 = HPDETECT高电平表示扬声器	耳机插孔检测
	4			保留	
	3	TRIS	0	将ADCDAT设为高阻态，并将ADCLRC、DACLRC和BCLK切换为输入。 0 = ADCDAT为输出；ADCLRC、DACLRC和BCLK作为输入（从模式）或输出（主模式）  1 = ADCDAT处于三态；DACLRC和BCLK作为输入；ADCLRC作为输入（当未配置为GPIO时）	音频接口控制
	2	LRCM	0	选择ADCLRC和DACLRC的禁用模式（主模式） 0 = 当ADC（左右声道）禁用时ADCLRC禁用；当DAC（左右声道）禁用时DACLRC禁用 1 = 仅当ADC（左右）和DAC（左右）禁用时，ADCLRC和DACLRC才禁用	音频接口控制
	1:0		0	保留	
	8:7	VMID选择[1:0]	00	VMID分压器使能与选择 00 = 禁用VMID（用于关机模式） 01 = 启用 $2 \times 50\text{k}\Omega$ 分压器（用于播放/录制） 10 = 启用 $2 \times 250\text{k}\Omega$ 分压器（用于低功耗待机） 11 = 启用 $2 \times 5\text{k}\Omega$ 分压器（用于快速启动）	电源管理
	6	VREF	0	VREF（所有其他功能必需） 0 = 断电 1 = 上电	电源管理
	5	AINL	0	左声道模拟输入PGA 0 = 断电 1 = 上电	电源管理
	4	AINR	0	右声道模拟输入PGA 0 = 断电 1 = 上电	电源管理
	3	ADCL	0	左声道ADC 0 = 断电 1 = 上电	电源管理
	2	ADCR	0	右声道ADC 0 = 断电 1 = 上电	电源管理
	1	MICB	0	麦克风偏置 0 = 断电 1 = 上电	电源管理
	0	数字使能	0	主时钟禁用 0 = 主时钟启用 1 = 主时钟禁用	电源管理
R26 (1Ah) 电源管理 (2)	8	左声道数模转换器	0	左声道数模转换器 0 = 关闭电源 1 = 上电	电源管理
	7	右声道数模转换器	0	右声道数模转换器 0 = 关闭电源 1 = 上电	电源管理

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R27 (1Bh) Additional Control (3)	6	LOUT1	0	LOUT1 Output Buffer 0 = Power down 1 = Power up	Power Management
	5	ROUT1	0	ROUT1 Output Buffer 0 = Power down 1 = Power up	Power Management
	4	SPKL	0	SPK_LP/SPK_LN Output Buffers 0 = Power down 1 = Power up	Power Management
	3	SPKR	0	SPK_RP/SPK_RN Output Buffers 0 = Power down 1 = Power up	Power Management
	2		0	Reserved	
	1	OUT3	0	OUT3 Output Buffer 0 = Power down 1 = Power up	Power Management
	0	PLL_EN	0	PLL Enable 0 = Power down 1 = Power up	Power Management
	8:7		00	Reserved	
R28 (1Ch) Anti-Pop 1	6	VROI	0	VREF to Analogue Output Resistance (Disabled Outputs) 0 = 500Ω VMID to output 1 = 20kΩ VMID to output	Enabling the Outputs
	5		0	Reserved	
	4		0	Reserved	
	3	OUT3CAP	0	Capless Mode Headphone Switch Enable 0 = OUT3 unaffected by jack detect events 1 = OUT3 enabled and disabled together with HP_L and HP_R in response to jack detect events	Headphone Jack Detect
	2:0	ADC_ALC_SR	000	ALC Sample Rate 000 = 44.1k / 48k 001 = 32k 010 = 22.05k / 24k 011 = 16k 100 = 11.25k / 12k 101 = 8k 110 and 111 = Reserved	Automatic Level Control
	8		0	Reserved	
	7	POBCTRL	0	Selects the bias current source for output amplifiers and VMID buffer 0 = VMID / R bias 1 = VGS / R bias	
	6:5		00	Reserved	
	4	BUFDOPEN	0	Enables the VGS / R current generator 0 = Disabled 1 = Enabled	
	3	BUFIOEN	0	Enables the VGS / R current generator and the analogue input and output bias 0 = Disabled 1 = Enabled	
	2	SOFT_ST	0	Enables VMID soft start 0 = Disabled 1 = Enabled	

寄存器地址	位	标签	默认值	描述	参见
R27 (1Bh) 附加控制 (3)	6	左输出1	0	左输出1缓冲器 0 = 关闭电源 1 = 上电	电源管理
	5	右输出1	0	右输出1缓冲器 0 = 关闭电源 1 = 上电	电源管理
	4	SPKL	0	SPK_LP/SPK_LN输出缓冲器 0 = 断电 1 = 上电	电源管理
	3	SPKR	0	SPK_RP/SPK_RN输出缓冲器 0 = 断电 1 = 上电	电源管理
	2		0	保留	
	1	OUT3	0	OUT3输出缓冲器 0 = 关闭电源 1 = 上电	电源管理
	0	锁相环使能	0	锁相环启用 0 = 关闭电源 1 = 上电	电源管理
	8:7		00	保留	
R28 (1Ch) 防爆音1	6	VROI	0	VREF至模拟输出电阻 (禁用输出) 0 = 500ΩVM ID至输出 1 = 20kΩVMID至输出	启用输出端
	5		0	保留	
	4		0	保留	
	3	OUT3电容	0	无电容模式耳机开关使能 0 = OUT3不受插孔检测事件影响 1 = OUT3随HP_L和HP_R根据插孔检测事件同步启用/禁用	耳机插孔检测
	2:0	模数转换器_自动电平控制_采样率	000	ALC采样率 000 = 44.1k / 48k 001 = 32k 010 = 22.05k / 24k 011 = 16k 100 = 11.25k / 12k 101 = 8k 110 和 111 = 保留	自动电平控制
	8		0	保留	
	7	电源开关控制	0	选择输出放大器和VMID缓冲器的偏置电 流源 0 = VMID/R偏置  1 = VGS/R偏置	
	6:5		00	保留	
	4	BUFDOPEN	0	启用VGS/R电流发生器 0 = 禁用 1 = 启用	
	3	BUFIOEN	0	启用VGS/R电流发生器及模拟输入输出偏置 0 = 禁用  1 = 启用	
	2	SOFT_ST	0	启用VMID软启动 0 = 禁用 1 = 启用	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1		0	Reserved	
	0	HPSTBY	0	Headphone Amplifier Standby 0 = Standby mode disabled (Normal operation) 1 = Standby mode enabled	
R29 (1Dh)	8:7		00	Reserved	
Anti-pop 2	6	DISOP	0	Discharges the DC-blocking headphone capacitors on HP_L and HP_R 0 = Disabled 1 = Enabled	
	5:4	DRES[1:0]	00	DRES determines the value of the resistors used to discharge the DC-blocking headphone capacitors when DISOP=1 DRES[1:0]      Resistance (Ohms) 0            0      400 0            1      200 1            0      600 1            1      150	
	3:0		0000	Reserved	
R30 (1Eh)	8:0		000000000	Reserved	
R31 (1Fh)	8:0		000000000	Reserved	
R32 (20h)	8	LMN1	1	Connect LINPUT1 to inverting input of Left Input PGA 0 = LINPUT1 not connected to PGA 1 = LINPUT1 connected to PGA	Input Signal Path
ADCL Signal Path	7	LMP3	0	Connect LINPUT3 to non-inverting input of Left Input PGA 0 = LINPUT3 not connected to PGA 1 = LINPUT3 connected to PGA (Constant input impedance)	Input Signal Path
	6	LMP2	0	Connect LINPUT2 to non-inverting input of Left Input PGA 0 = LINPUT2 not connected to PGA 1 = LINPUT2 connected to PGA (Constant input impedance)	Input Signal Path
	5:4	LMICBOOST[1:0]	00	Left Channel Input PGA Boost Gain 00 = +0dB 01 = +13dB 10 = +20dB 11 = +29dB	Input Signal Path
	3	LMIC2B	0	Connect Left Input PGA to Left Input Boost Mixer 0 = Not connected 1 = Connected	Input Signal Path
	2:0		000	Reserved	
R33 (21h)	8	RMN1	1	Connect RINPUT1 to inverting input of Right Input PGA 0 = RINPUT1 not connected to PGA 1 = RINPUT1 connected to PGA	Input Signal Path
ADCR Signal Path	7	RMP3	0	Connect RINPUT3 to non-inverting input of Right Input PGA 0 = RINPUT3 not connected to PGA 1 = RINPUT3 connected to PGA (Constant input impedance)	Input Signal Path

寄存器地址	位	标签	默认值	描述	参见
	1		0	保留	
	0	HPSTBY	0	耳机放大器待机 0 = 禁用待机模式（正常操作） 1 = 启用待机模式	
R29 (1Dh) 防爆音2	8:7		00	保留	
	6	DISOP	0	对HP_L和HP_R的直流阻隔耳机电容进行放电 0 = 禁用  1 = 启用	
	5:4	驱动电阻选择[1:0]	00	当DISOP=1时，DRES[1:0]用于确定直流隔直耳机电容放电电阻的阻值  电阻值（欧姆） 0 0 40 0 0 1 20 0 1 0 600 1 1 150	
	3:0		0000	保留	
R30 (1Eh)	8:0		000000000	保留	
R31 (1Fh)	8:0		000000000	保留	
R32 (20h) ADCL 信号 路径	8	LMN1	1	将LINPUT1连接至左输入PGA的反相输入  0 = LINPUT1未连接到PGA 1 = LINPUT1连接到PGA	输入信号路 径
	7	LMP3	0	将LINPUT3连接至左输入PGA的同相输入  0 = LINPUT3未连接到PGA 1 = LINPUT3连接至PGA（恒定输入阻抗）	输入信号路 径
	6	左麦克风路径2	0	将LINPUT2连接至左输入PGA的同相输入  0 = LINPUT2未连接到PGA 1 = LINPUT2连接至PGA（恒定输入阻抗）	输入信号路 径
	5:4	左麦克风输入控制升压电路[1:0]	00	左声道输入PGA升压增益 00 = +0分贝 01 = +13分贝 10 = +20分贝 11 = +29分贝	输入信号路 径
	3	左麦克风输入控制2B	0	将左输入可编程增益放大器连接至左输入升压混频器 0 = 未连接 1 = 已连接	输入信号路 径
	2:0		000	保留	
R33 (21h) ADCR 信号 路径	8	RMN1	1	将RINPUT1连接至右输入PGA的反相输入  0 = RINPUT1 未连接至 PGA 1 = RINPUT1 连接至 PGA	输入信号路 径
	7	RMP3	0	将RINPUT3连接至右输入PGA的同相输入  0 = RINPUT3未连接至可编程增益放大器 1 = RINPUT3连接至可编程增益放大器（恒定输入阻抗）	输入信号路 径

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R34 (22h) Left Out Mix	6	RMP2	0	Connect RINPUT2 to non-inverting input of Right Input PGA 0 = RINPUT2 not connected to PGA 1 = RINPUT2 connected to PGA (Constant input impedance)	Input Signal Path
	5:4	RMICBOOST[1:0]	00	Right Channel Input PGA Boost Gain 00 = +0dB 01 = +13dB 10 = +20dB 11 = +29dB	Input Signal Path
	3	RMIC2B	0	Connect Right Input PGA to Right Input Boost Mixer 0 = Not connected 1 = Connected	Input Signal Path
	2:0		000	Reserved	
R35 (23h)	8	LD2LO	0	Left DAC to Left Output Mixer 0 = Disable (Mute) 1 = Enable Path	Output Signal Path
	7	LI2LO	0	LINPUT3 to Left Output Mixer 0 = Disable (Mute) 1 = Enable Path	Output Signal Path
	6:4	LI2LOVOL[2:0]	101	LINPUT3 to Left Output Mixer Volume 000 = 0dB ...(3dB steps) 111 = -21dB	Output Signal Path
	3:0		0000	Reserved	
R36 (24h)	8:0		001010000	Reserved	
R37 (25h) Right Out Mix	8	RD2RO	0	Right DAC to Right Output Mixer 0 = Disable (Mute) 1 = Enable Path	Output Signal Path
7	RI2RO	0	RINPUT3 to Right Output Mixer 0 = Disable (Mute) 1 = Enable Path	Output Signal Path	
6:4	RI2ROVOL[2:0]	101	RINPUT3 to Right Output Mixer Volume 000 = 0dB ...(3dB steps) 111 = -21dB	Output Signal Path	
3:0		0000	Reserved		
R38 (26h) Mono Out Mix (1)	8		0	Reserved	
	7	L2MO	0	Left Output Mixer to Mono Output Mixer Control 0 = Left channel mix disabled 1 = Left channel mix enabled	Output Signal Path
	6:0		0000000	Reserved	
R39 (27h) Mono Out Mix (2)	8		0	Reserved	
	7	R2MO	0	Right Output Mixer to Mono Output Mixer Control 0 = Right channel mix disabled 1 = Right channel mix enabled	Output Signal Path
	6:0		0000000	Reserved	
R40 (28h) Left Speaker Volume	8	SPKVU	N/A	Speaker Volume Update Writing a 1 to this bit will cause left and right speaker volumes to be updated (SPKLVOL and SPKRVOL)	Analogue Outputs

寄存器地址	位	标签	默认值	描述	参见
	6	RMP2	0	将RINPUT2连接至右输入可编程增益放大器的同相输入端 0 = RINPUT2未连接至可编程增益放大器 1 = RINPUT2连接至可编程增益放大器（恒定输入阻抗）	输入信号路径
	5:4	右麦克风输入控制升压电路[1:0]	00	右声道输入可编程增益放大器升压增益 00 = +0分贝 01 = +13分贝 10 = +20分贝 11 = +29分贝	输入信号路径
	3	RMIC2B	0	将右输入可编程增益放大器连接至右输入升压混频器 0 = 未连接 1 = 已连接	输入信号路径
	2:0		000	保留	
R34 (22h) 左声道输出混频	8	LD2LO	0	左DAC至左声道输出混频器 0 = 禁用（静音） 1 = 启用路径	输出信号路径
	7	LI2LO	0	LINPUT3至左声道输出混频器 0 = 禁用（静音） 1 = 启用路径	输出信号路径
	6:4	左I2L输出音量[2:0]	101	LINPUT3至左声道输出混频器音量 000 = 0dB ... (3dB步进) 111 = -21dB	输出信号路径
	3:0		0000	保留	
R35 (23h)	8:0		001010000	保留	
R36 (24h)	8:0		001010000	保留	
R37 (25h) 右声道输出混频	8	RD2RO	0	右DAC至右输出混频器 0 = 禁用（静音） 1 = 启用路径	输出信号路径
	7	RI2RO	0	右输入3至右输出混频器 0 = 禁用（静音） 1 = 启用路径	输出信号路径
	6:4	右I2R输出音量[2:0]	101	右输入3至右输出混频器音量 000 = 0分贝 ... (3分贝步进) 111 = -21分贝	输出信号路径
	3:0		0000	保留	
R38 (26h) 单声道输出混频 (1)	8		0	保留	
	7	L2MO	0	左声道输出混频器至单声道输出混频器控制 0 = 左声道混频禁用 1 = 左声道混频启用	输出信号路径
	6:0		0000000	保留	
R39 (27h) 单声道输出混频 (2)	8		0	保留	
	7	R2MO	0	右声道输出混频器至单声道输出混频器控制 0 = 右声道混频禁用 1 = 右声道混频启用	输出信号路径
	6:0		0000000	保留	
R40 (28h) 左声道扬声器音量	8	SPKVU	不适用	扬声器音量更新 向该位写入1将使左右扬声器音量更新（SPKLVOL和SPKRVOL）	模拟输出

# WM8960

Preliminary Technical Data

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	7	SPKLZC	0	Left Speaker Zero Cross Enable 1 = Change gain on zero cross only 0 = Change gain immediately	Analogue Outputs
	6:0	SPKLVOL[6:0]	0000000	SPK_LP/SPK_LN Volume 1111111 = +6dB ... 1dB steps down to 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE	Analogue Outputs
R41 (29h) Right Speaker Volume	8	SPKVU	N/A	Speaker Volume Update Writing a 1 to this bit will cause left and right speaker volumes to be updated (SPKLVOL and SPKRVOL)	Analogue Outputs
	7	SPKRZC	0	Right Speaker Zero Cross Enable 1 = Change gain on zero cross only 0 = Change gain immediately	Analogue Outputs
	6:0	SPKRVOL[6:0]	0000000	SPK_RP/SPK_RN Volume 1111111 = +6dB ... 1dB steps down to 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE	Analogue Outputs
	8:7		00	Reserved	
R42 (2Ah) OUT3 Volume	6	MOUTVOL	1	Mono Output Mixer Volume Control 0 = 0dB 1 = -6dB	Output Signal Path
	5:0		000000	Reserved	
	8:7		00	Reserved	
R43 (2Bh) Left Input Boost Mixer	6:4	LIN3BOOST[2:0]	000	LINPUT3 to Boost Mixer Gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB	Input Signal Path
	3:1	LIN2BOOST[2:0]	000	LINPUT2 to Boost Mixer Gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB	Input Signal Path
	0		0	Reserved	
	8:7		00	Reserved	
R44 (2Ch) Right Input Boost Mixer	6:4	RIN3BOOST[2:0]	000	RINPUT3 to Boost Mixer Gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB	Input Signal Path
	3:1	RIN2BOOST[2:0]	000	RINPUT2 to Boost Mixer Gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB	Input Signal Path
	0		0	Reserved	
	8:7		00	Reserved	
R45 (2Dh) Left Bypass	7	LB2LO	0	Left Input Boost Mixer to Left Output Mixer 0 = Disable (Mute) 1 = Enable Path	Output Signal Path

# WM8960

初步技术数据

寄存器地址	位	标签	默认值	描述	参见
	7	SPKLZC	0	左扬声器零交叉使能 1 = 仅在零交叉时改变增益 0 = 立即改变增益	模拟输出
	6:0	左扬声器音量[6:0]	0000000	SPK_LP/SPK_LN 音量 1111111 = +6分贝 ... 以1分贝步进递减至 0110000 = -73分贝 0101111 至 0000000 = 模拟静音控制	模拟输出
R41 (29h) 右扬声器音量	8	SPKVU	不适用	扬声器音量更新 向该位写入1将使左右扬声器音量更新 (SPKLVOL和SPKRVOL)	模拟输出
	7	SPKRZC	0	右扬声器零交叉使能 1 = 仅在零交叉时改变增益 0 = 立即改变增益	模拟输出
	6:0	右扬声器音量[6:0]	0000000	SPK_RP/SPK_RN 音量 1111111 = +6分贝 ... 以1分贝步进递减至 0110000 = -73分贝 0101111 至 0000000 = 模拟静音控制	模拟输出
	5:0		00	保留	
R42 (2Ah) OUT3 音量	6	主输出音量	1	单声道输出混频器音量控制 0 = 0分贝 1 = -6分贝	输出信号路径
	5:0		000000	保留	
	4:0		00	保留	
R43 (2Bh) 左输入升压混频器	6:4	左输入3升压电路[2:0]	000	LINPUT3至升压混频器增益 000 = 静音 001 = -12dB ... 每级3dB递增至 111 = +6dB	输入信号路径
	3:1	左输入2升压电路[2:0]	000	LINPUT2至升压混频器增益 000 = 静音 001 = -12dB ... 每级3dB递增至 111 = +6dB	输入信号路径
	2:0		0	保留	
	1:0		00	保留	
R44 (2Ch) 右输入升压混频器	6:4	右输入3升压电路[2:0]	000	RINPUT3至升压混频器增益 000 = 静音 001 = -12dB ... 每级3dB递增至 111 = +6dB	输入信号路径
	3:1	右输入2升压电路[2:0]	000	RINPUT2至升压混频器增益 000 = 静音 001 = -12dB ... 每级3dB递增至 111 = +6dB	输入信号路径
	2:0		0	保留	
	1:0		00	保留	
R45 (2Dh) 左声道旁路	7	LB2LO	0	左声道输入升压混频器至左声道输出混频器 0 = 禁用 (静音) 1 = 启用路径	输出信号路径
	6		0	保留	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6:4	LB2LOVOL[2:0]	101	Left Input Boost Mixer to Left Output Mixer Volume 000 = 0dB ... (3dB steps) 111 = -21dB	Output Signal Path
	3:0		0000	Reserved	
R46 (2Eh) Right Bypass	8		0	Reserved	
	7	RB2RO	0	Right Input Boost Mixer to Right Output Mixer 0 = Disable (Mute) 1 = Enable Path	Output Signal Path
	6:4	RB2ROVOL[2:0]	101	Right Input Boost Mixer to Right Output Mixer Volume 000 = 0dB ... (3dB steps) 111 = -21dB	Output Signal Path
	3:0		0000	Reserved	
R47 (2Fh) Power Mgmt (3)	8:6		000	Reserved	
	5	LMIC	0	Left Channel Input PGA Enable 0 = PGA disabled 1 = PGA enabled (if AINL = 1)	Input Signal Path
	4	RMIC	0	Right Channel Input PGA Enable 0 = PGA disabled 1 = PGA enabled (if AINR = 1)	Input Signal Path
	3	LOMIX	0	Left Output Mixer Enable Control 0 = Disabled 1 = Enabled	Output Signal Path
	2	ROMIX	0	Right Output Mixer Enable Control 0 = Disabled 1 = Enabled	Output Signal Path
	1:0		00	Reserved	
R48 (30h) Additional Control (4)	8		0	Reserved	
	7	GPIOPOL	0	GPIO Polarity Invert 0 = Non inverted 1 = Inverted	General Purpose Input / Output
	6:4	GPIOSEL[2:0]	000	ADCLRC/GPIO1 GPIO Function Select: 000 = Jack detect input 001 = Reserved 010 = Temperature ok 011 = Debounced jack detect output 100 = SYSCLK output 101 = PLL lock 110 = Logic 0 111 = Logic 1	General Purpose Input / Output
	3:2	HPSEL[1:0]	00	Headphone Switch Input Select 0X = GPIO1 used for jack detect input (Requires ADCLRC pin to be configured as a GPIO) 10 = JD2 used for jack detect input 11 = JD3 used for jack detect input	Headphone Jack Detect
	1	TSENSEN	1	Temperature Sensor Enable 0 = Temperature sensor disabled 1 = Temperature sensor enabled	Thermal Shutdown
	0	MBSEL	0	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.65 * AVDD	Input Signal Path

寄存器地址	位	标签	默认值	描述	参见
	6:4	LB2LOVOL[2:0]	101	左声道输入升压混频器至左声道输出混频器 混音器音量 000 = 0分贝 ... (3分贝步进) 111 = -21分贝	输出信号路径
	3:0		0000	保留	
R46 (2Eh) 右声道旁路	8		0	保留	
	7	RB2RO	0	右声道输入升压混频器至右声道输出混频器 0 = 禁用 (静音) 1 = 启用路径	输出信号路径
	6:4	右B2R输出音量[2:0]	101	右声道输入升压混频器至右声道输出混频器 混音器音量 000 = 0分贝 ... (3分贝步进) 111 = -21分贝	输出信号路径
	3:0		0000	保留	
R47 (2Fh) 电源管理 (3)	8:6		000	保留	
	5	左麦克风输入控制	0	左声道输入可编程增益放大器使能 0 = PGA禁用 1 = 启用PGA (当AINL = 1时)	输入信号路径
	4	右麦克风输入控制	0	右声道输入可编程增益放大器使能 0 = PGA禁用 1 = 启用PGA (当AINR = 1时)	输入信号路径
	3	LOMIX	0	左声道输出混频器启用控制 0 = 禁用 1 = 启用	输出信号路径
	2	ROMIX	0	右声道输出混频器启用控制 0 = 禁用 1 = 启用	输出信号路径
	1:0		00	保留	
	8		0	保留	
R48 (30h) 附加控制 (4)	7	GPIO极性	0	GPIO极性反转 0 = 不反转 1 = 反转	通用用途输入/输出
	6:4	GPIO选择[2:0]	000	ADCLRC/GPIO1 GPIO功能选择： 000 = 插孔检测输入 001 = 保留 010 = 温度正常 011 = 去抖动后的插孔检测输出 100 = 系统时钟输出 101 = PLL锁定 110 = 逻辑0 111 = 逻辑1	通用用途输入/输出
	3:2	HPSEL[1:0]	00	耳机开关输入选择 0X = 通用输入 输出端口1用于插孔检测输入 (需将ADCLRC引脚配置为GPIO) 10 = JD2用于插孔检测输入 11 = 使用 JD3 作为插孔检测输入	耳机插孔检测
	1	TSENSEN	1	温度传感器使能 0 = 温度传感器禁用 1 = 温度传感器启用	热关断
	0	MBSEL	0	麦克风偏置电压控制 0 = 0.9 * AVDD 1 = 0.65 * AVDD	输入信号路径

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R49 (31h) Class D Control (1)	8		0	Reserved	
	7:6	SPK_OP_EN[1:0]	00	Enable Class D Speaker Outputs 00 = Off 01 = Left speaker only 10 = Right speaker only 11 = Left and right speakers enabled	Enabling the Outputs
	5:0		110111	Reserved	
R50 (32h)	8:0		001001101	Reserved	
R51 (33h) Class D Control (2)	8:6		010	Reserved	
	5:3	DCGAIN[2:0]	000	DC Speaker Boost (Boosts speaker DC output level by up to 1.8 x on left and right channels) 000 = 1.00x boost (+0dB) 001 = 1.27x boost (+2.1dB) 010 = 1.40x boost (+2.9dB) 011 = 1.52x boost (+3.6dB) 100 = 1.67x boost (+4.5dB) 101 = 1.8x boost (+5.1dB) 110 to 111 = Reserved	Analogue Outputs
	2:0	ACGAIN[2:0]	000	AC Speaker Boost (Boosts speaker AC output signal by up to 1.8 x on left and right channels) 000 = 1.00x boost (+0dB) 001 = 1.27x boost (+2.1dB) 010 = 1.40x boost (+2.9dB) 011 = 1.52x boost (+3.6dB) 100 = 1.67x boost (+4.5dB) 101 = 1.8x boost (+5.1dB) 110 to 111 = Reserved	Analogue Outputs
	8:6	OPCLKDIV[2:0]	000	SYSCLK Output to GPIO Clock Division ratio 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 5.5 101 = SYSCLK / 6	General Purpose Input / Output
R52 (34h) PLL (1)	5	SDM	0	Enable Integer Mode 0 = Integer mode 1 = Fractional mode	Clocking and Sample Rates
	4	PLLPRESCALE	0	Divide MCLK by 2 before input to PLL 0 = Divide by 1 1 = Divide by 2	Clocking and Sample Rates
	3:0	PLLN[3:0]	1000	Integer (N) part of PLL input/output frequency ratio. Use values greater than 5 and less than 13.	Clocking and Sample Rates
	8		0	Reserved	
R53 (35h) PLL (2)	7:0	PLLK[23:16]	00110001	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).	Clocking and Sample Rates
	8		0	Reserved	
R54 (36h) PLL (3)	7:0	PLLK[15:8]	00100110	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).	Clocking and Sample Rates
	8		0	Reserved	
R55 (37h) PLL (4)	7:0	PLLK[7:0]	11101001	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).	Clocking and Sample Rates
	8		0	Reserved	

# WM8960

初步技术数据

寄存器地址	位	标签	默认值	描述	参见
R49 (31h) D类功放 控制寄存器(1)	8		0	保留	
	7:6	SPK_OP_EN[1:0]	00	启用D类扬声器输出 00 = 关闭 01 = 仅左声道扬声器 10 = 仅右声道扬声器 11 = 左右声道扬声器均启用	启用 输出端
	5:0		110111	保留	
R50 (32h)	8:0		001001101	保留	
R51 (33h) D类 控制 (2)	8:6		010	保留	
	5:3	直流增益控制[2:0]	000	直流扬声器升压 (左右声道扬声器直流输出电平最高提升1.8倍) 000 = 1.00倍升压 (+0分贝) 001 = 1.27倍升压 (+2.1分贝) 010 = 1.40倍升压 (+2.9分贝) 011 = 1.52倍升压 (+3.6分贝) 100 = 1.67倍升压 (+4.5分贝) 101 = 1.8倍升压 (+5.1分贝) 110至111 = 保留	模拟输出
	2:0	交流增益[2:0]	000	交流扬声器升压 (左右声道交流输出信号最大可提升1.8倍) 000 = 1.00倍升压 (+0分贝) 001 = 1.27倍升压 (+2.1分贝) 010 = 1.40倍升压 (+2.9分贝) 011 = 1.52倍升压 (+3.6分贝) 100 = 1.67倍升压 (+4.5分贝) 101 = 1.8倍升压 (+5.1分贝) 110至111 = 保留	模拟输出
R52 (34h) 锁相环 (1)	8:6	OPCLKDIV[2:0]	000	SYSCLK输出至GPIO时钟分频比 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 5.5 101 = SYSCLK / 6	通用 用途输入/ 输出
	5	SDM	0	启用整数模式 0 = 整数模式 1 = 分数模式	时钟与采样率
	4	锁相环预分频器	0	MCLK输入至锁相环(PLL)前的二分频 0 = 分频比1 1=2分频	时钟与采样率
	3:0	PLLN[3:0]	1000	PLL输入/输出频率比的整数部分(N)。取值应大于5且小于13。	时钟与采样率
R53 (35h) PLL (2)	8		0	保留	
	7:0	锁相环K值[23:16]	00110001	PLL1输入/输出频率比的小数部分(K) (视为一个24位二进制数)。	时钟与采样率
R54 (36h) PLL (3)	8		0	保留	
	7:0	PLLK[15:8]	00100110	PLL1输入/输出频率比的小数部分(K) (视为一个24位二进制数)。	时钟与采样率
R55 (37h) PLL (4)	8		0	保留	
	7:0	PLLK[7:0]	11101001	PLL1输入/输出频率比的小数部分(K) (视为一个24位二进制数)。	时钟与采样率

## DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ADC Filter</b>					
Passband	+/- 0.05dB	0		0.454 fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.546s			
Stopband Attenuation	f > 0.546 fs	-60			dB
<b>DAC Normal Filter</b>					
Passband	+/- 0.03dB	0		0.454 fs	
	-6dB		0.5 fs		
Passband Ripple	0.454 fs			+/- 0.03	dB
Stopband		0.546 fs			
Stopband Attenuation	F > 0.546 fs	-50			dB
<b>DAC Sloping Stopband Filter</b>					
Passband	+/- 0.03dB	0		0.25 fs	
	+/- 1dB	0.25 fs		0.454 fs	
	-6dB		0.5 fs		
Passband Ripple	0.25 fs			+/- 0.03	dB
Stopband 1		0.546 fs		0.7 fs	
Stopband 1 Attenuation	f > 0.546 fs	-60			dB
Stopband 2		0.7 fs		1.4 fs	
Stopband 2 Attenuation	f > 0.7 fs	-85			dB
Stopband 3		1.4 fs			
Stopband 3 Attenuation	F > 1.4 fs	-55			dB

DAC FILTERS		ADC FILTERS	
Mode	Group Delay	Mode	Group Delay
Normal	18 / fs	Normal	18 / fs
Sloping Stopband	18 / fs		

## ADC FILTER RESPONSES

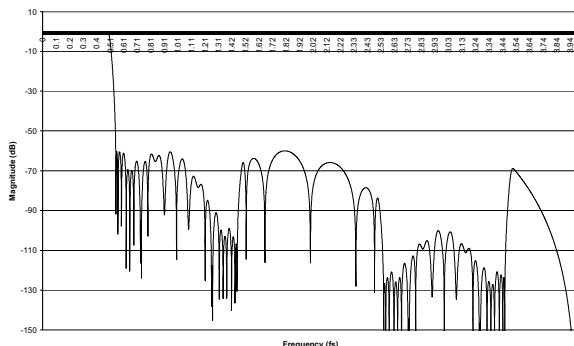


Figure 38 ADC Digital Filter Frequency Response

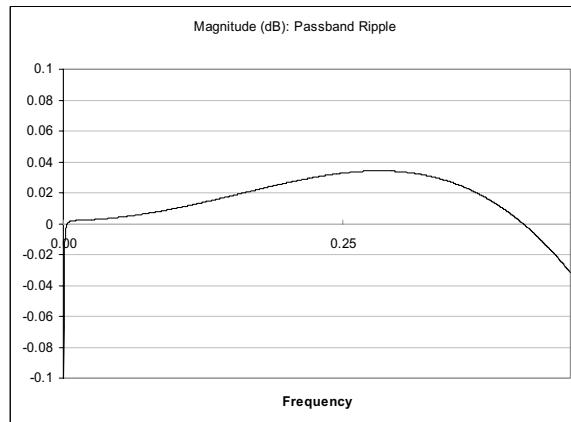


Figure 39 ADC Digital Filter Ripple

## 数字滤波器特性

参数	测试条件	最小值	典型值	最大值	单位
<b>ADC滤波器</b>					
通带	+/- 0.05分贝	0		0.454倍采样频率	
	-6分贝		0.5倍采样频率		
通带波纹				+/- 0.05	分贝
阻带		0.546倍采样频率			
阻带衰减	f > 0.546倍采样频率	-60			分贝
<b>DAC标准滤波器</b>					
通带	±0.03分贝	0		0.454倍采样频率	
	-6分贝		0.5倍采样频率		
通带波纹	0.454倍采样频率			+/- 0.03	分贝
阻带		0.546倍采样频率			
阻带衰减	F > 0.546倍采样频率	-50			分贝
<b>数模转换器斜坡阻带滤波器</b>					
通带	±0.03分贝	0		0.25倍采样频率	
	±1分贝	0.25倍采样频率		0.454倍采样频率	
	-6分贝		0.5倍采样频率		
通带波纹	0.25倍采样频率			+/- 0.03	分贝
阻带1		0.546倍采样频率		0.7倍采样频率	
阻带1衰减	f > 0.546倍采样频率	-60			分贝
阻带2		0.7倍采样频率		1.4倍采样频率	
阻带2衰减	f > 0.7倍采样频率	-85			分贝
阻带3		1.4倍采样频率			
阻带3衰减	F > 1.4倍采样频率	-55			分贝

数模转换器滤波器		模数转换器滤波器	
工作模式	群延迟	工作模式	群延迟
正常模式	18 / fs	正常模式	18 / fs
倾斜阻带模式	18 / fs		

## 模数转换器滤波器响应

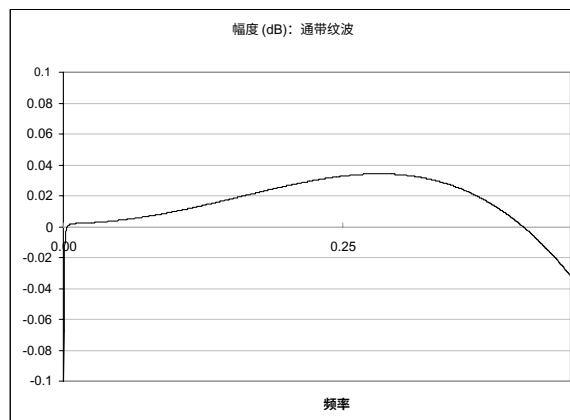
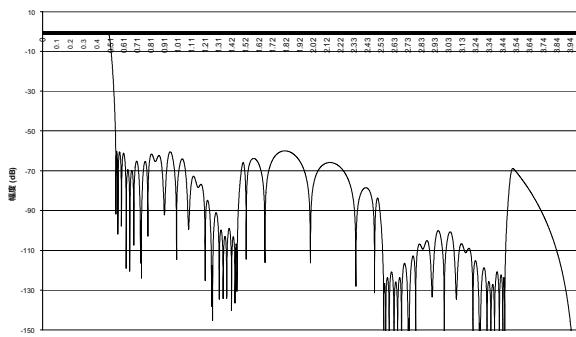


图38 模数转换器数字滤波器频率响应

图39 模数转换器数字滤波器纹波

## DAC FILTER RESPONSES

### DAC STOPBAND ATTENUATION

The DAC digital filter type is selected by the DACSLOPE register bit as shown in Table 50.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) ADC and DAC Control (2)	1	DACSLOPE	0	Selects DAC filter characteristics 0 = Normal mode 1 = Sloping stopband mode

Table 50 DAC Filter Selection

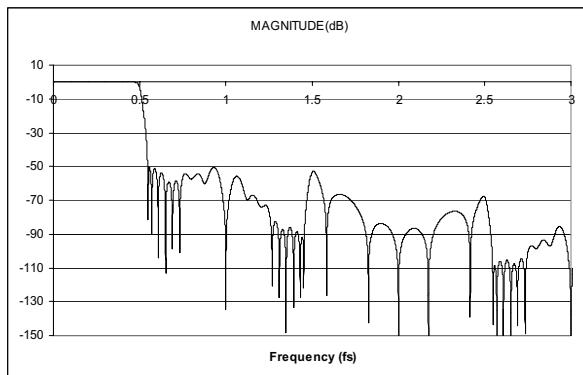


Figure 40 DAC Digital Filter Frequency Response (Normal Mode)

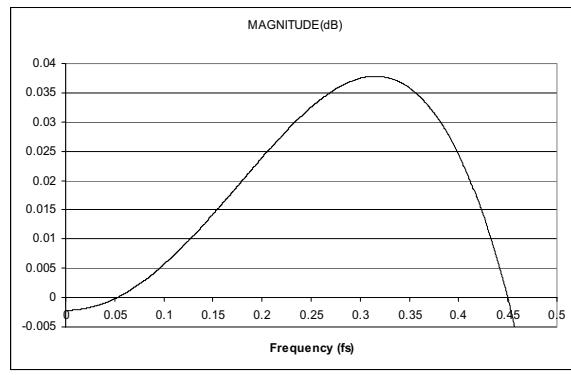


Figure 41 DAC Digital Filter Ripple (Normal Mode)

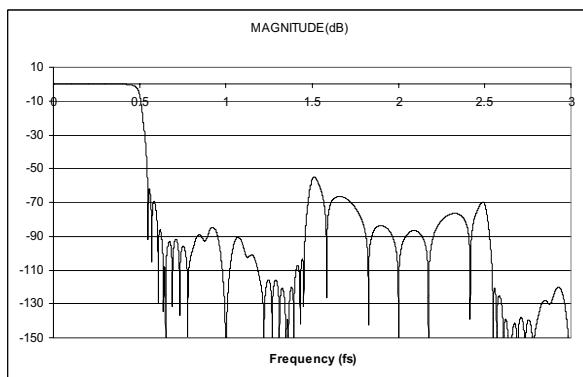


Figure 42 DAC Digital Filter Frequency Response (Sloping Stopband Mode)

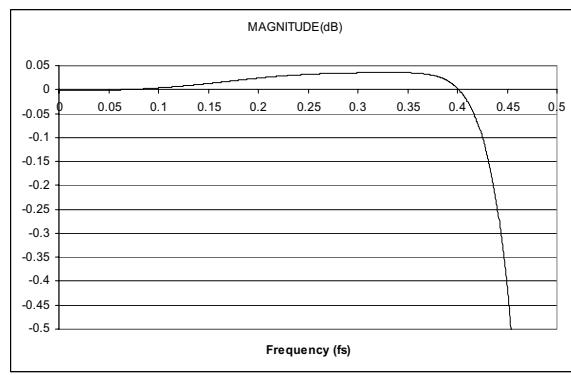


Figure 43 DAC Digital Filter Ripple (Sloping Stopband Mode)

## 数模转换器滤波器响应

### 数模转换器阻带衰减

数模转换器数字滤波器类型通过DACSLOPE寄存器位选择，如表50所示。

寄存器地址	位	标签	默认值	描述
R6 (06h) ADC与DAC 控制寄存器(2)	1	DACSLOPE	0	选择DAC滤波器特性 0 = 正常模式 1 = 倾斜阻带模式

表50 数模转换器滤波器选择

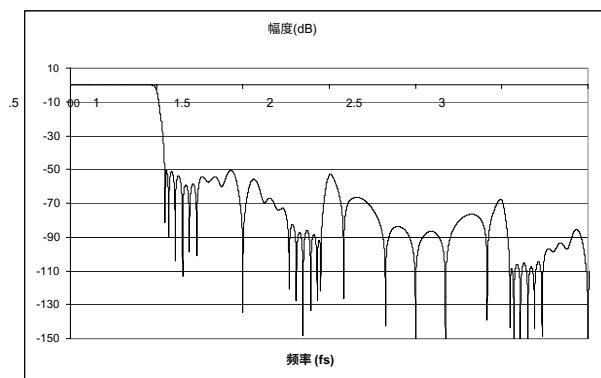


图40 DAC数字滤波器频率响应（正常模式）

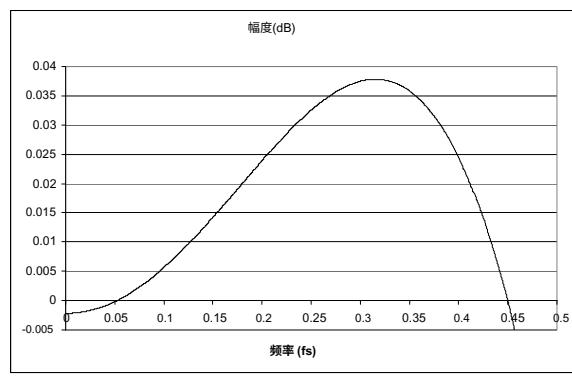


图41 DAC数字滤波器纹波（正常模式）

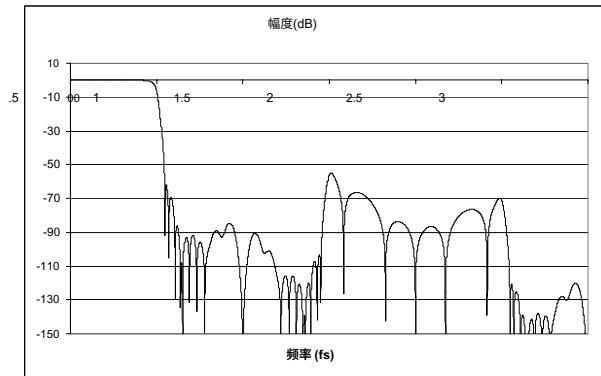


图42 DAC数字滤波器频率响应（斜降阻带模式）

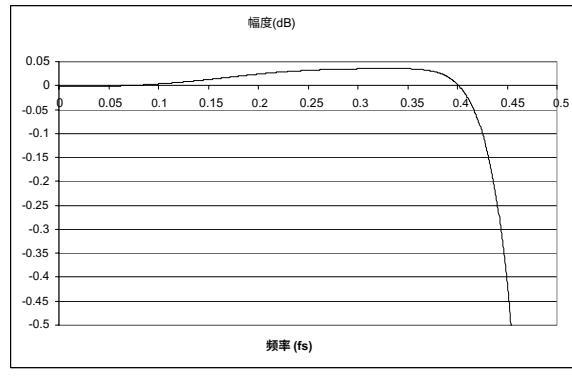


图43 DAC数字滤波器纹波（斜降阻带模式）

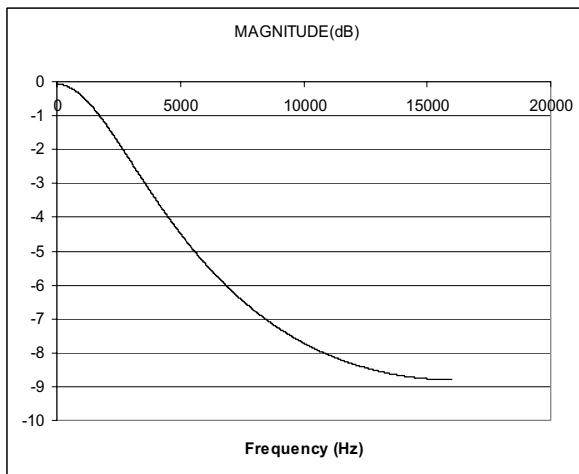
**DE-EMPHASIS FILTER RESPONSES**

Figure 44 De-Emphasis Digital Filter Response (32kHz)

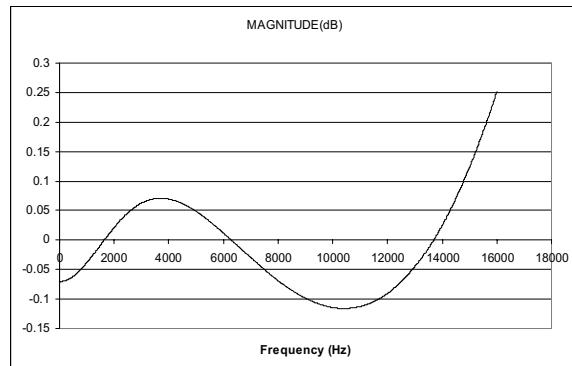


Figure 45 De-Emphasis Error (32kHz)

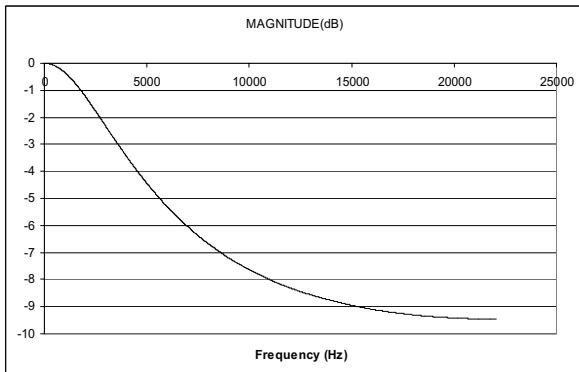


Figure 46 De-Emphasis Digital Filter Response (44.1kHz)

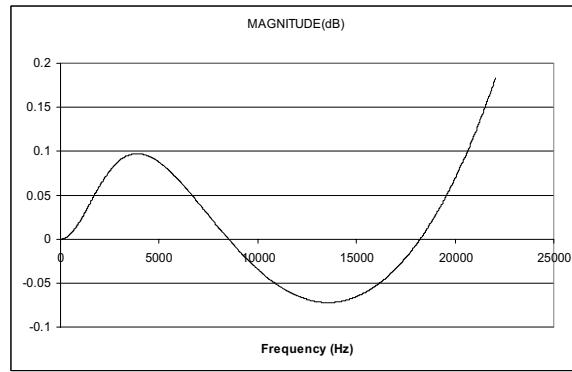


Figure 47 De-Emphasis Error (44.1kHz)

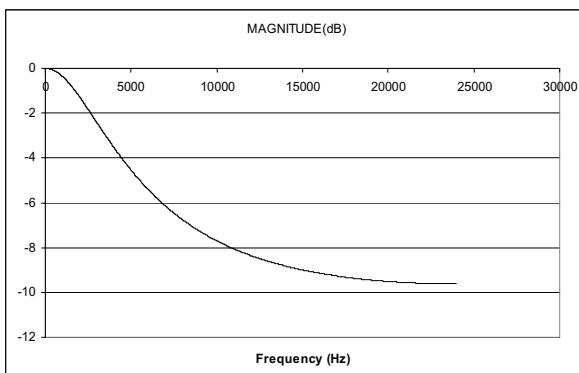


Figure 48 De-Emphasis Digital Filter Response (48kHz)

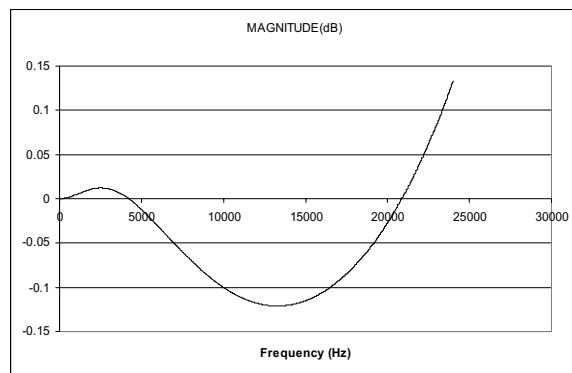


Figure 49 De-Emphasis Error (48kHz)

## 去加重滤波器响应

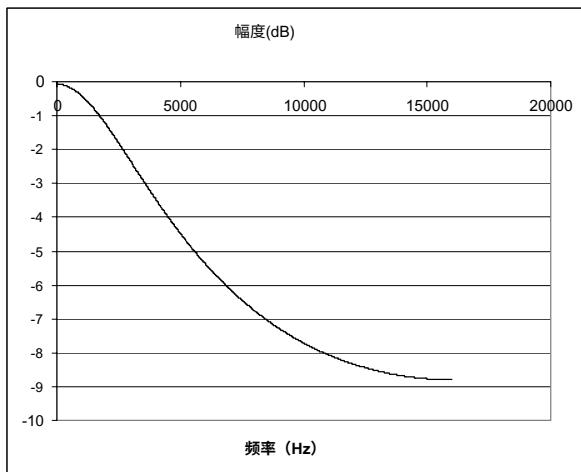


图44 去加重数字滤波器响应 (32千赫)

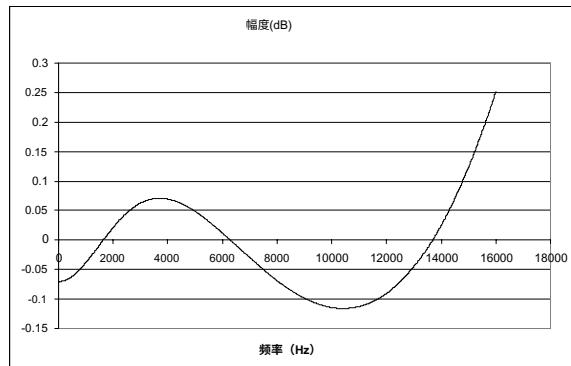


图45 去加重误差 (32千赫)

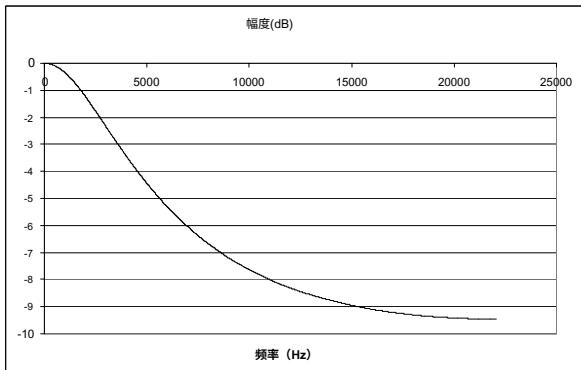


图46 去加重数字滤波器响应 (44.1千赫)

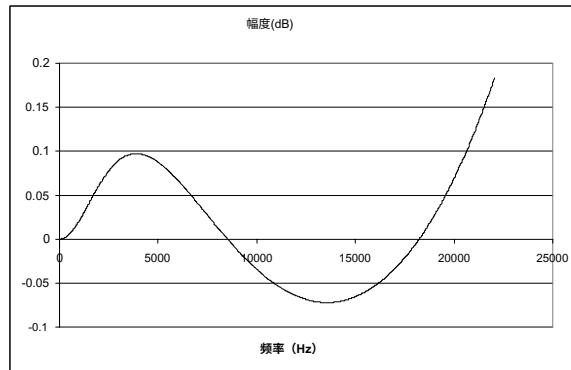


图47 去加重误差 (44.1千赫)

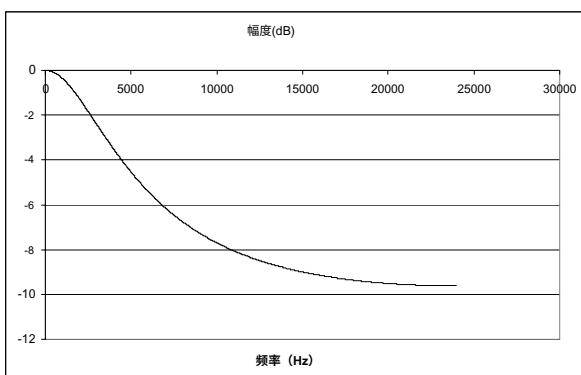


图48 去加重数字滤波器响应 (48千赫)

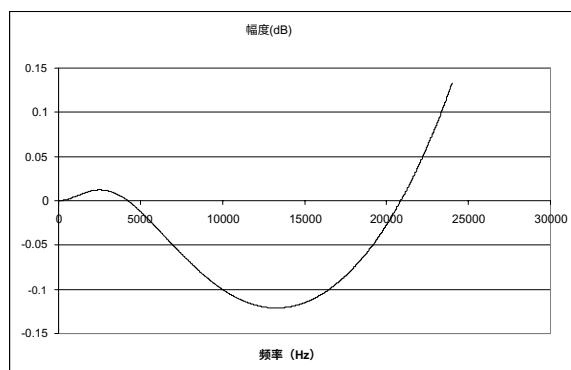
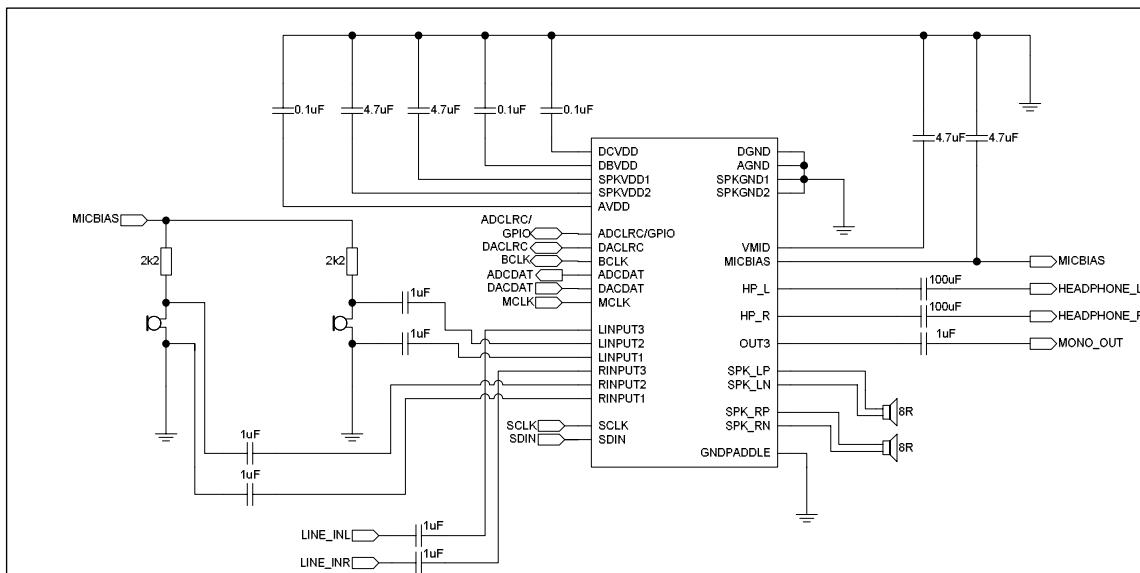


图49 去加重误差 (48千赫)

## APPLICATIONS INFORMATION

### RECOMMENDED EXTERNAL COMPONENTS



#### Notes:

1. AGND and DGND should be connected as close to the WM8960 as possible.
2. Supply decoupling capacitors on DCVDD, DBVDD, SPKVDD and AVDD should be positioned as close to the WM8960 as possible.
3. Capacitor types should be carefully chosen. Capacitors with very low ESR are recommended for optimum performance.
4. Microphone common mode noise performance can be improved by adding resistors from the microphone negative terminal to ground.
5. The speakers should be connected as close as possible to the WM8960. When this is not possible, filtering should be placed on the speaker outputs close to the WM8960.

## SPEAKER SELECTION

For filterless operation, it is important to select a speaker with appropriate internal inductance. The internal inductance and the speaker's load resistance create a low-pass filter with a cut-off frequency of:

$$f_c = R_L / 2\pi L$$

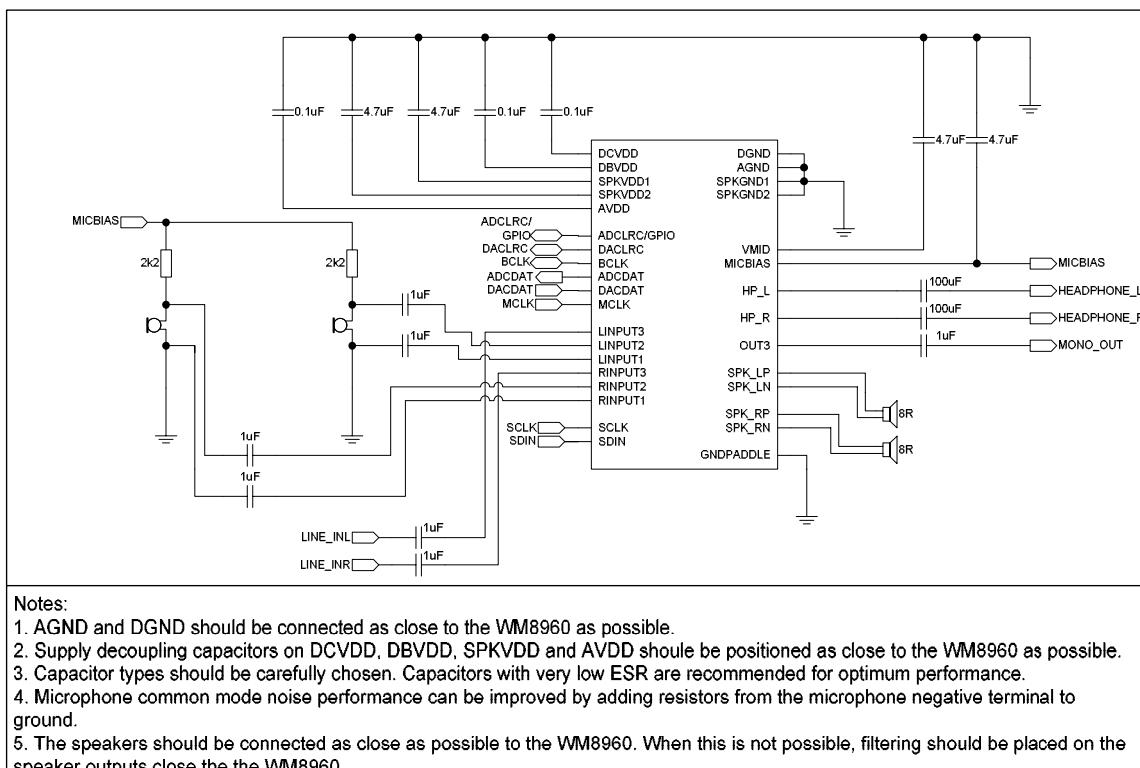
e.g. for an 8Ω speaker and required cut-off frequency of 20kHz, the speaker should be chosen to have an inductance of:

$$L = R_L / 2\pi f_c = 8\Omega / 2\pi * 20\text{kHz} = 64\mu\text{H}$$

8Ω speakers typically have an inductance in the range 20μH to 100μH. Care should be taken to ensure that the cut-off frequency of the speaker's internal filtering is low enough to prevent speaker damage. The class D outputs of the WM8960 operate at much higher frequencies than is recommended for most speakers, and the cut-off frequency of the filter should be low enough to protect the speaker.

## 应用信息

### 推荐外部元件



### 扬声器选择

对于无滤波器操作，选择具有适当内部电感的扬声器至关重要。扬声器的内部电感与负载电阻会形成截止频率为以下的低通滤波器：

$$f_c = R_L / 2\pi L$$

例如，对于8Ω扬声器和要求的20kHz截止频率，应选择电感量为：

$$L = R_L / 2\pi f_c = 8\Omega / 2\pi * 20\text{kHz} = 64\mu\text{H}$$

8Ω扬声器的典型电感量范围为20μH至100μH。需特别注意确保扬声器内部滤波器的截止频率足够低以防止损坏。WM8960的D类输出工作频率远高于大多数扬声器的推荐值，滤波器的截止频率应足够低以保护扬声器。

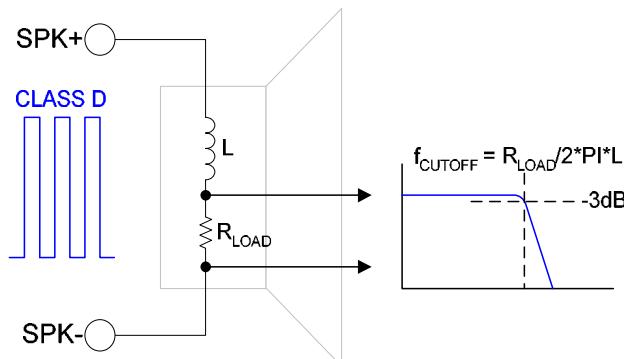


Figure 50 Speaker Equivalent Circuit

### PCB LAYOUT CONSIDERATIONS

The efficiency of the speaker drivers is affected by the series resistance between the WM8960 and the speaker (e.g. inductor ESR) as shown in Figure 51. This resistance should be as low as possible to maximise efficiency.

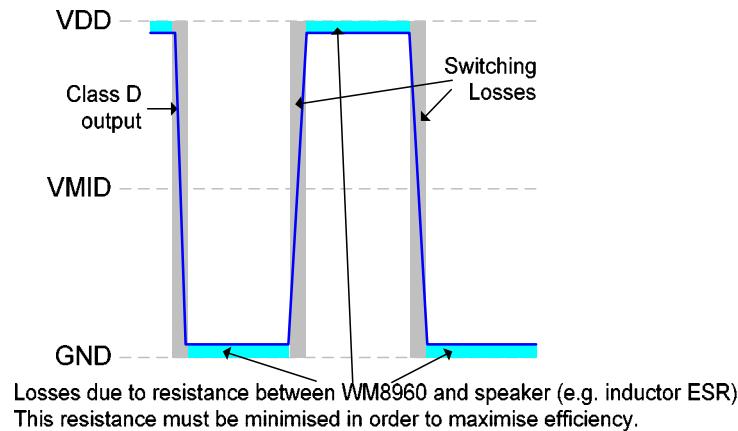


Figure 51 Speaker Connection Losses

The distance between the WM8960 and the speakers should be kept to a minimum to reduce series resistance, and also to reduce EMI. Further reductions in EMI can be achieved by additional passive filtering and/or shielding as shown in Figure 52. When additional passive filtering is used, low ESR components should be chosen to minimise series resistance between the WM8960 and the speaker, maximising efficiency.

LC passive filtering will usually be effective at reducing EMI at frequencies up to around 30MHz. To reduce emissions at higher frequencies, ferrite beads placed as close to the device as possible will be more effective.

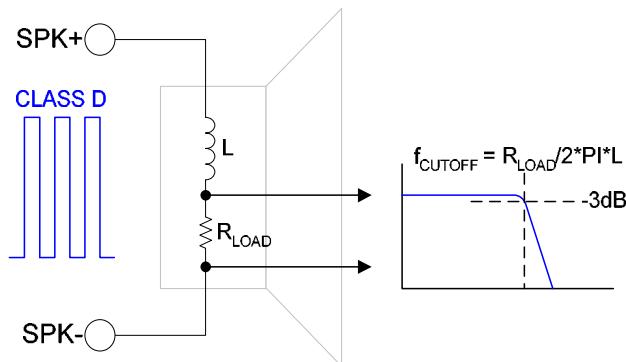


图50 扬声器等效电路

**PCB布局注意事项**

如51图所示，扬声器驱动器的效率受WM8960与扬声器之间串联电阻（例如电感器ESR）的影响。该电阻应尽可能低以最大化效率。

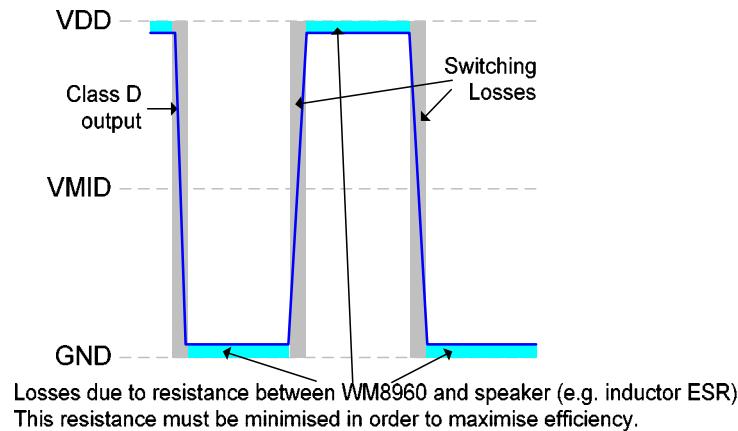


图51 扬声器连接损耗

应尽量缩短WM8960与扬声器之间的距离以降低串联电阻，同时减少电磁干扰。如图52所示，可通过增加无源滤波和/或屏蔽措施进一步降低电磁干扰。当使用额外无源滤波时，应选择低ESR元件以最小化WM8960与扬声器之间的串联电阻，从而实现效率最大化。

LC无源滤波通常可有效抑制30MHz以下的电磁干扰。为降低更高频率的辐射，应尽可能靠近器件放置铁氧体磁珠以获得更好的抑制效果。

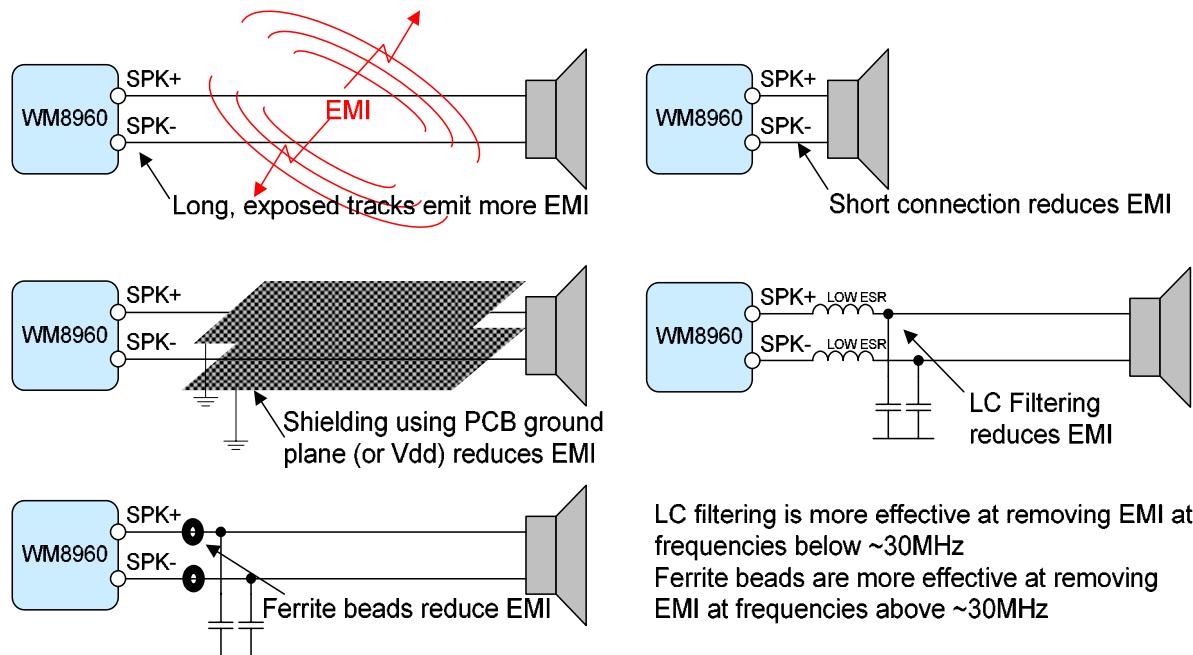


Figure 52 EMI Reduction Techniques

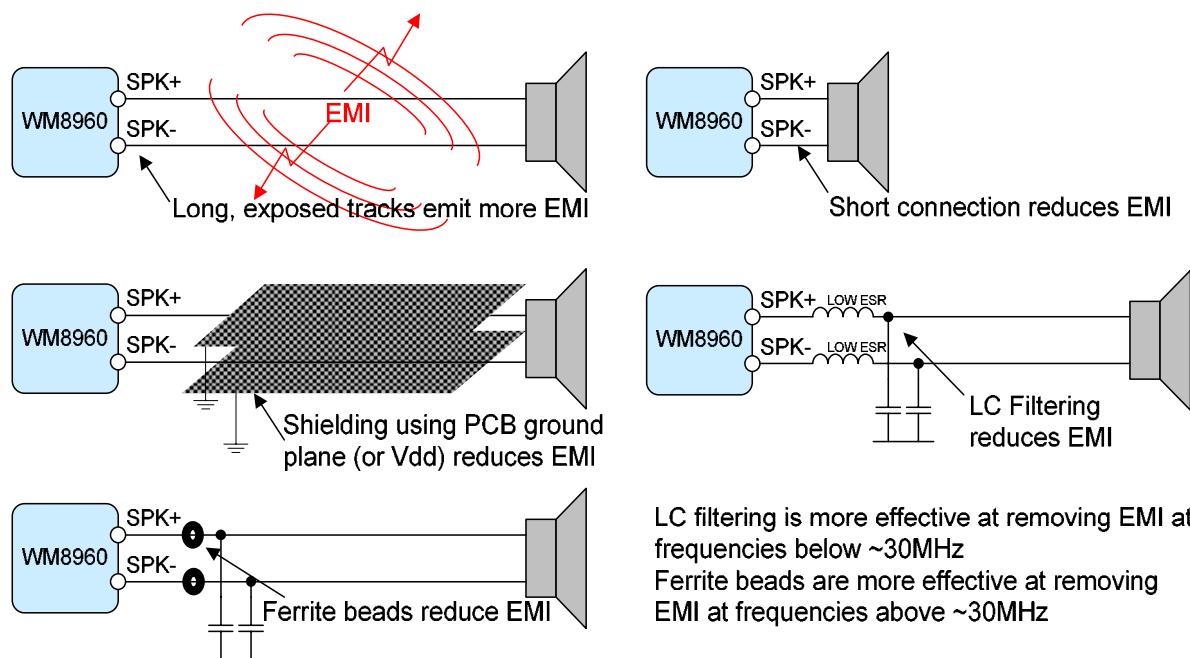
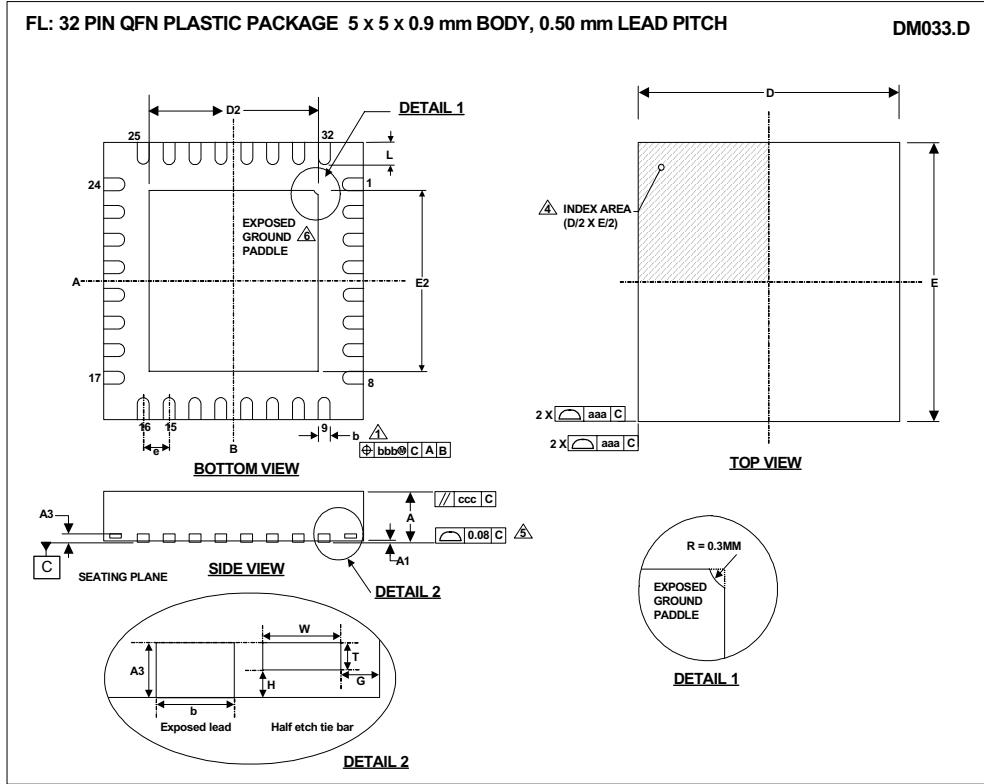


图52 电磁干扰抑制技术

## PACKAGE DIMENSIONS

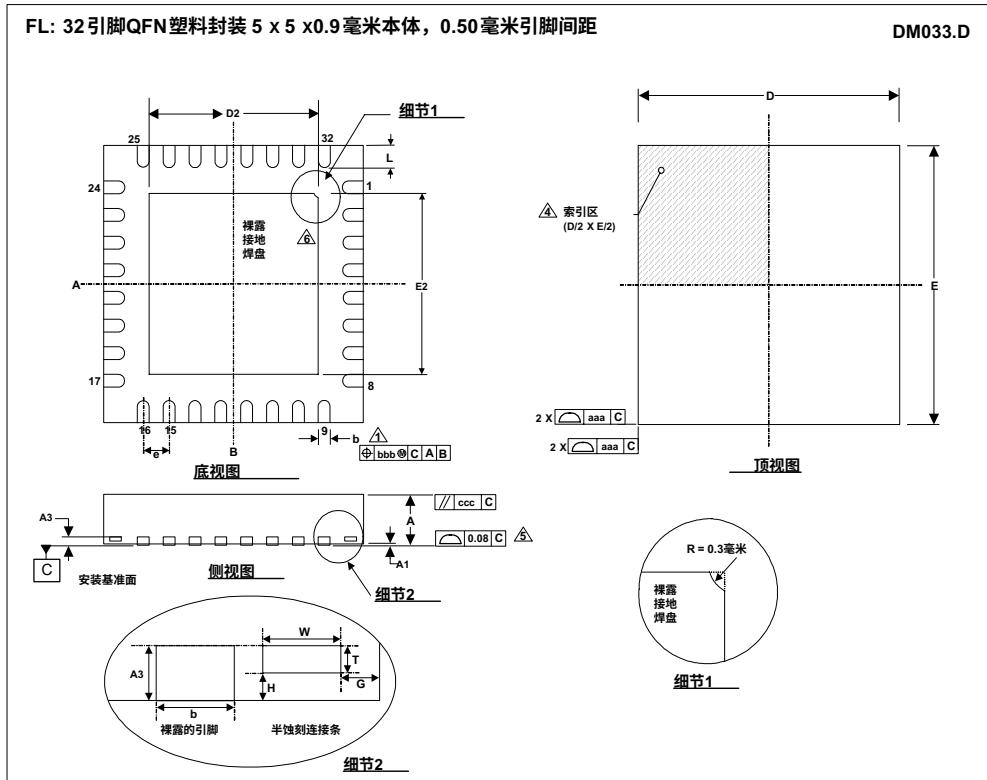


Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0	0.02	0.05	
A3		0.20 REF		
b	0.18	0.25	0.30	1
D		5.00		
D2	3.30	3.45	3.55	2
E		5.00		
E2	3.30	3.45	3.55	2
e		0.50 BSC		
G		0.213		
H		0.1		
L	0.30	0.40	0.50	
T		0.1		
W		0.2		
<b>Tolerances of Form and Position</b>				
aaa	0.15			
bbb	0.10			
ccc	0.10			
REF:	JEDEC, MO-220, VARIATION VHHD-5.			

## NOTES:

1. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
2. FALLS WITHIN JEDEC, MO-220, VARIATION VHHD-5.
3. ALL DIMENSIONS ARE IN MILLIMETRES.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-002.
5. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
6. REFER TO APPLICATION NOTE WM-0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.
7. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

## 封装尺寸



符号	尺寸(毫米)			
	最小值	公称值	最大值	注释
A	0.80	0.90	1.00	
A1	0	0.02	0.05	
A3		0.20 参考		
b	0.18	0.25	0.30	1
D		5.00		
D2	3.30	3.45	3.55	2
E		5.00		
E2	3.30	3.45	3.55	2
e		0.50 基本		
G		0.213		
H		0.1		
L	0.30	0.40	0.50	
T		0.1		
W		0.2		
形位公差				
aaa	0.15			
bbb	0.10			
ccc	0.10			
参考:	JEDEC标准 MO-220 版本VHHD-5			

注意：  
 1. 尺寸b适用于金属化端子，测量位置为距端子尖端0.15 mm至0.30 mm之间的区域。  
 2. 符合JEDEC标准MO-220 VHHD-5型封装规格。  
 3. 所有尺寸单位为毫米(mm)。  
 4. 第1号端子标识符及端子1引脚规则应符合JEDEC 95-1 SPP-002标准。  
 5. 共面性要求同时适用于外露散热焊盘和端子。  
 6. 有关PCB封装布局和QFN封装焊接的更多信息，请参考应用说明WAN\_0118。  
 7. 本图纸如有更改，恕不另行通知。

## IMPORTANT NOTICE

Wolfson Microelectronics plc ("Wolfson") products and services are sold subject to Wolfson's terms and conditions of sale, delivery and payment supplied at the time of order acknowledgement.

Wolfson warrants performance of its products to the specifications in effect at the date of shipment. Wolfson reserves the right to make changes to its products and specifications or to discontinue any product or service without notice. Customers should therefore obtain the latest version of relevant information from Wolfson to verify that the information is current.

Testing and other quality control techniques are utilised to the extent Wolfson deems necessary to support its warranty. Specific testing of all parameters of each device is not necessarily performed unless required by law or regulation.

In order to minimise risks associated with customer applications, the customer must use adequate design and operating safeguards to minimise inherent or procedural hazards. Wolfson is not liable for applications assistance or customer product design. The customer is solely responsible for its selection and use of Wolfson products. Wolfson is not liable for such selection or use nor for use of any circuitry other than circuitry entirely embodied in a Wolfson product.

Wolfson's products are not intended for use in life support systems, appliances, nuclear systems or systems where malfunction can reasonably be expected to result in personal injury, death or severe property or environmental damage. Any use of products by the customer for such purposes is at the customer's own risk.

Wolfson does not grant any licence (express or implied) under any patent right, copyright, mask work right or other intellectual property right of Wolfson covering or relating to any combination, machine, or process in which its products or services might be or are used. Any provision or publication of any third party's products or services does not constitute Wolfson's approval, licence, warranty or endorsement thereof. Any third party trade marks contained in this document belong to the respective third party owner.

Reproduction of information from Wolfson datasheets is permissible only if reproduction is without alteration and is accompanied by all associated copyright, proprietary and other notices (including this notice) and conditions. Wolfson is not liable for any unauthorised alteration of such information or for any reliance placed thereon.

Any representations made, warranties given, and/or liabilities accepted by any person which differ from those contained in this datasheet or in Wolfson's standard terms and conditions of sale, delivery and payment are made, given and/or accepted at that person's own risk. Wolfson is not liable for any such representations, warranties or liabilities or for any reliance placed thereon by any person.

## ADDRESS:

Wolfson Microelectronics plc

26 Westfield Road

Edinburgh

EH11 2QB

United Kingdom

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: [sales@wolfsonmicro.com](mailto:sales@wolfsonmicro.com)

## 重要声明

沃夫森微电子有限公司 ("Wolfson") 的产品和服务销售均以订单确认时提供的销售条款、交付条件和支付条款为准。

沃夫森保证其产品性能符合发货当日有效之规格要求。沃夫森保留对其产品和规格进行变更或随时终止任何产品或服务的权利。因此客户应从沃夫森获取最新版技术资料以确保信息的时效性。

沃夫森将根据其质量保证要求实施必要的测试和其他质量控制措施。  
除非法律或法规要求，否则无需对每个器件的所有参数进行专项测试。

为降低客户应用风险，客户须采用合理的设计方案和操作保护措施来减小系统固有风险和操作风险。沃夫森不承担应用技术支持及客户产品设计责任。客户对其沃夫森产品的选型和使用承担全责，沃夫森对产品选型、使用以及非完全采用沃夫森产品电路的应用概不负责。

Wolfson产品不适用于生命维持系统、家用电器、核系统或其他可合理预见设备故障会导致人身伤害、死亡、重大财产损失或环境破坏的系统。  
客户将产品用于此类用途时需自行承担风险。

对于覆盖或涉及任何组合、机器或工艺（可能使用或正在使用Wolfson产品或服务的场景）的专利权、版权、掩膜作品权或其他Wolfson知识产权，Wolfson不授予任何明示或暗示的许可。对任何第三方产品或服务的提供或发布，不构成Wolfson的认可、许可、担保或背书。本文档所含第三方商标归相应第三方所有者所有。

仅在不作任何更改且完整保留所有相关版权声明、专有声明、其他通知（含本声明）及条款的前提下，允许复制Wolfson数据手册中的信息。Wolfson对任何未经授权的信息修改行为以及由此产生的依赖后果概不负责。

任何个人所作的任何与本数据手册或Wolfson销售、交付及付款标准条款条件下载明内容存在差异的陈述、提供的担保及/或承担的责任，均应由该个人自行承担风险。Wolfson不对任何此类陈述、担保或责任承担任何责任，亦不对任何个人对此产生的依赖承担责任。

## 地址：

欧胜微电子有限公司 英国爱

丁堡西田路26号（

邮编：EH

11 2QB)

电话 :: +44 (0)131 272 7000

传真 :: +44 (0)131 272 7001

电邮 :: [sales@wolfsonmicro.com](mailto:sales@wolfsonmicro.com)