

AMOLED Power Solution

1 General Description

The BV6802/A is a highly integrated power solution for AMOLED Display application, which uses a single-inductor-bipolar-output (SIBO) converter and three linear low-dropout regulators (LDO) to generate two positive and one negative voltage outputs. It does not need an extra charge pump circuit to generate the negative voltage output so that external capacitors required by the charge pump circuit can be eliminated and the pcb space can be achieved with very small.

The output voltages can be adjusted by SWIRE pin. Compared with the scheme of generating negative voltage by a charge pump circuit, the best energy conversion efficiency can only be obtained near the negative voltage ratio provided by its charge pump circuit. This SIBO architecture can provide a stable high conversion efficiency throughout the entire negative voltage adjusting range. Therefore, this solution can provide the optimal negative voltage output value according to different brightness requirements to reduce the power consumption of the AMOLED display significantly. This is the best solution that can optimize the solution form factor as well as display power consumption.

With its input voltage range from 2.9V to 5.5V, BV6802/A is optimized for products powered by single-cell batteries with output currents up to 80mA. The BV6802/A is available in the WL-CSP-16B 1.64mm x 1.64mm package.

2 Features

- Input Voltage Range: 2.9V to 5.5V
- Positive Output Voltage AVDD: 2.6V to 3.5V (BV6802 Default is 2.8V \pm 1%) (BV6802A Default is 3.3V \pm 1%)
- Positive Output Voltage OVDD Range: 2.6V to 5.3V (Default is 4.6V \pm 1%)
- Negative Output Voltage OVSS Range: -0.6V to -4.7V (Default is -2.4V \pm 1%)
- Low Quiescent Current: 70 μ A
- AVDD Max. Loading is 20mA, OVDD and OVSS Max. loading is 100mA
- Low Output Ripple
- Built-in Internal Soft start
- UVLO, UVP, SCP, OCP, OTP, and SSP protection

3 Applications

- Wearable AMOLED Product

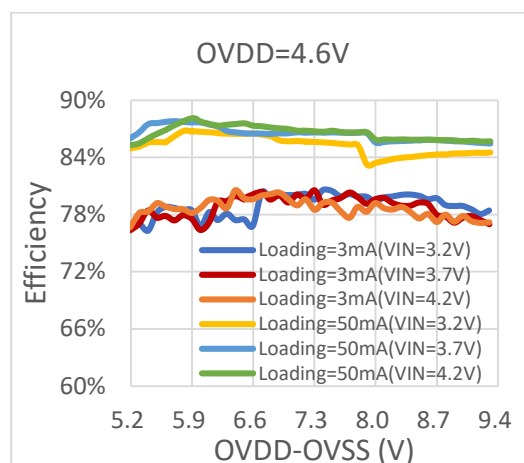
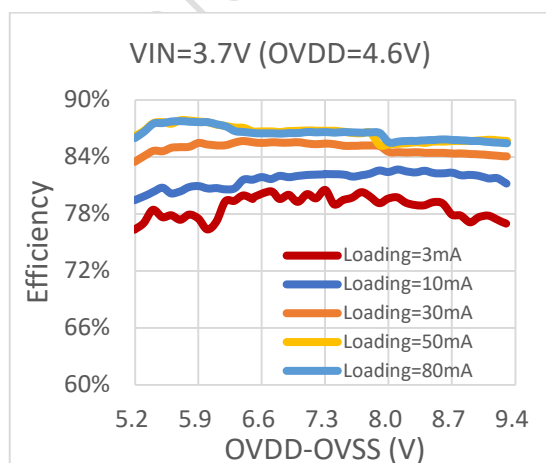
4 Ordering Information

BV6802(A)W

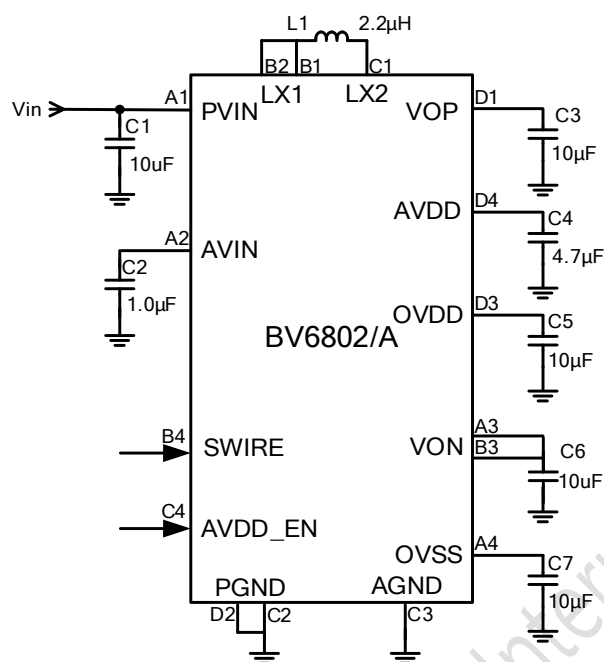
Package Type
W: WL-CSP-16B 1.64mmx1.64mm
Default: AVDD is 2.8V.
A: AVDD is 3.3V

Note:

Bravotek products are RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020Package Information



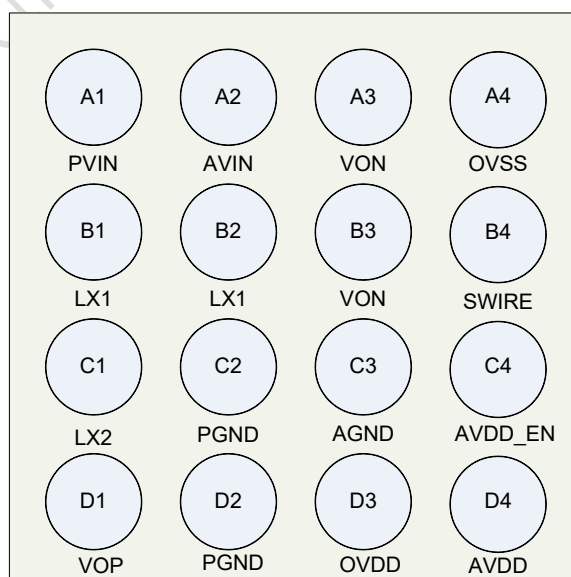
5 Application Circuit



Selectable Model

Model	Output Voltage
BV6802	AVDD(VCI)=2.8V, OVDD(ELVDD)=4.6V, OVSS(ELVSS)=-2.4V
BV6802A	AVDD(VCI)=3.3V, OVDD(ELVDD)=4.6V, OVSS(ELVSS)=-2.4V

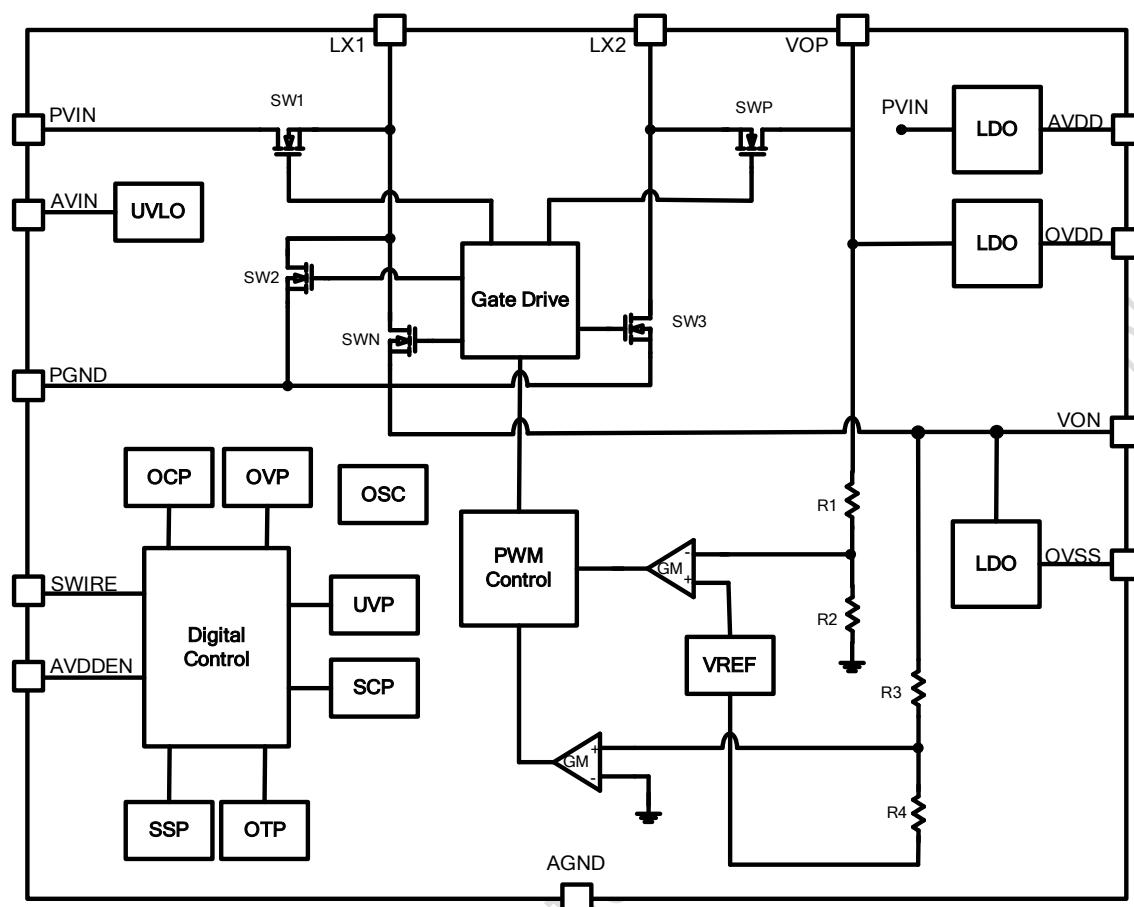
6 Pin Configuration and Function



Top View

Pin	Name	Function
A1	PVIN	Power Input for SIBO
A2	AVIN	Analog Power Input for IC
A3, B3	VON	SIBO Negative Output.
A4	OVSS	OVSS LDO Output
B1, B2	LX1	LX1 switching node for SIBO
B4	SWIRE	SWIRE Control Interface
C1	LX2	LX2 switching node for SIBO
C2, D2	PGND	Power Ground
C3	AGND	Analog Ground
C4	AVDD_EN	Enable for AVDD
D1	VOP	SIBO Positive Output
D3	OVDD	OVDD LDO Output
D4	AVDD	AVDD LDO Output

7 Functional Block Diagram



8 Absolute Maximum Ratings

- Supply Input Voltage: AVIN, PVIN to ANGND, PGND-0.3V to 6.0V
- VOP, AVDD, OVDD, SWIRE, AVDDEN to AGND, PGND-0.3V to 6.0V
- VON, OVSS to ANGND, PGND-6.0V to 0.3V
- Power Dissipation, PD@ TA=25°C
 WL-CSP-16B 1.96W
- Package Thermal Resistance
 WL-CSP-16B, θ_{JA} 51°C/W
- Lead Temperature (Soldering, 10sec.) 260°C
- Junction Temperature 150°C
- Storage Temperature -65°C to 150°C
- ESD Susceptibility
 HBM(Human Body Model) 2KV
 MM(Machine Model) 200V

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9 Recommended Operating Conditions

- BV6802 Supply Input Voltage2.9V to 5.5V
- BV6802A Supply Input Voltage3.4V to 5.5V
- Junction Temperature Range-40°C to 125°C
- Ambient Temperature Range-40°C to 85°C

Note:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The device is not guaranteed to function outside its recommended operating conditions.

10 Components Selection

10.1 Inductor

Reference	Value	Component supplier	Package	Isat / DCR
L1	2.2uH	ALPS GLULK2R201A	2.5mm x 2.0mm x 1.0mm	1.8A / 85mΩ

10.2 Capacitors

Reference	Value	Component supplier	Package
C1, C3, C5, C7, C6	10uF/6.3V	GRM188R60J106ME84	0603
C4	4.7uF/6.3V	GRM188R60J475KE19	0603
C2	1uF/6.3V	GRM155R60J105ME19	0402

11 Electrical Characteristics

$V_{IN}=3.7V$, $AVDD=2.8V$ or $3.3V$, $OVDD=4.6V$, $OVSS=-2.4V$, $T_A=25^{\circ}C$, unless otherwise specified.						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Power Supply						
Input Supply Voltage	V_{IN}	BV6802	2.9	3.7	5.5	V
		BV6802A	3.4	3.7	5.5	V
Quiescent Current	I_Q	SWIRE=High, AVDD_EN=High, measured into VIN pin. No load	-	70	-	μA
Standby Current	$I_{Standby}$	AVDD_EN =High and SWIRE = low	-	20		μA
Shutdown Current	I_{SHDN}	AVDD_EN and SWIRE = low	-	0.1	1	μA
Under-Voltage Lockout Threshold	V_{UVLOH}	VIN Rising	--	2.75	2.85	V
	V_{UVLOL}	VIN falling	--	2.5	2.6	V
Thermal Shutdown	T_{SD}		--	140	--	°C

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Thermal Shutdown Hysteresis	ΔT_{SD}		--	10	--	°C
SWIRE						
SWIRE Logical High-Level Voltage	V_{SRH}	$V_{IN}=2.9V$ to $5.5V$	1.2	-	-	V
SWIRE Logic Low-Level Voltage	V_{SRL}	$V_{IN}=2.9V$ to $5.5V$	0	-	0.4	V
SWIRE Turn-off Detection	T_{OFF_DLY}		300	-	-	μs
SWIRE Signal Stop Indicate Time	T_{STOP}		300	-	-	μs
SWIRE Rising Time	T_r		-	-	200	ns
SWIRE Falling Time	T_f		-	-	200	ns
Clocked SWIRE High	T_{ON}		2	-	20	μs
Clocked SWIRE Low	T_{OFF}		2	-	20	μs
Input Clocked SWIRE Frequency	F_{SWIRE}		25	-	250	KHz
AVDDEN						
AVDD Enable Input Voltage	V_{IH}	$V_{IN}=2.9V$ to $5.5V$	1.2	-	-	V
	V_{IL}	$V_{IN}=2.9V$ to $5.5V$	0	-	0.4	V
SIBO						
Positive Output Voltage Range	V_{OP}		2.7	-	5.4	V
Negative Output Voltage Range	V_{ON}		-4.8	-	-0.7	V
Switching Frequency	F_{SW}		1.2	1.5	1.8	MHz
Over Current Protection	I_{OCP}			0.75		A
AVDD LDO						
Positive Output Voltage Range	V_{AVDD_RANGE}	BV6802	2.6	2.8	3.5	V
		BV6802A	2.6	3.3	3.5	V
Positive Output Voltage Accuracy	V_{AVDD_ACC}		-1	-	1	%
Output Current Capability	I_{AVDD}		-	10	20	mA
Line Regulation	V_{AVDD_LINE}	$V_{IN}=2.9$ to $5.5V$, $I_{AVDD}=1mA$	-	2	5	mV
Load Regulation	V_{AVDD_LOAD}	$I_{AVDD} = 0$ to $10mA$	-	2	5	mV
Output Ripple	V_{AVDD_RIPPLE}	$I_{AVDD} = 5mA$	-	-	10	mV
Current Limit	I_{AVDD_LIMIT}		-	30	50	mA
Discharge Resistance	R_{AVDD_RDIS}			100		Ω
Under Voltage Protection				80		%
UVP Detection Time				1.35		ms
OVDD LDO						
Positive Output Voltage Range	V_{OVDD_RANGE}		2.6	4.6	5.3	V
Positive Output Voltage Accuracy	V_{OVDD_ACC}		-1	-	1	%
Output Current Capability	I_{OVDD}		-	80	100	mA

BV6802/A

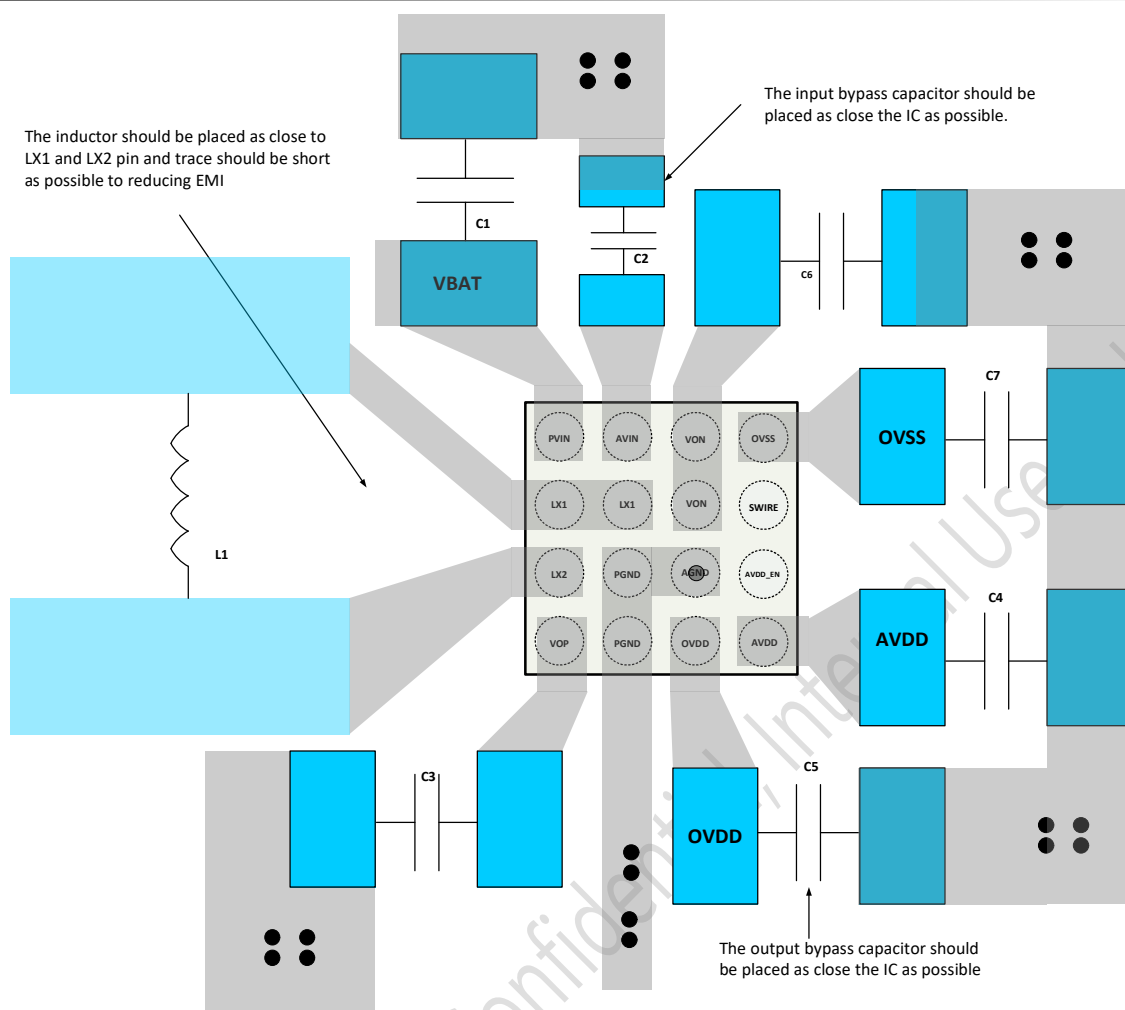
Line Regulation	V _{OVDD_LINE}	V _{IN} =2.9 to 5.5V, I _{OVDD} =1mA	-	2	5	mV
Load Regulation	V _{OVDD_LOAD}	I _{OVDD} = 0 to 10mA	-	2	5	mV
Output Ripple	V _{OVDD_RIPPLE}	I _{OVDD} = 30mA	-	-	10	mV
Current Limit	I _{OVDD_LIMIT}		-	150	200	mA
Discharge Resistance	R _{OVDD_RDIS}		-	100	-	Ω
Under Voltage Protection				80		%
UVP Detection Time				1.35		ms
OVSS LDO						
Negative Output Voltage Range	V _{OVSS_RANGE}		-4.7	-2.4	-0.6	V
Negative Output Voltage Accuracy	V _{OVSS_ACC}		-1	-	1	%
Output Current Capability	I _{OVSS}		-	80	100	mA
Line Regulation	V _{OVSS_LINE}	V _{IN} =2.9 to 5.5V, I _{OVSS} =1mA	-	2	5	mV
Load Regulation	V _{OVSS_LOAD}	I _{OVSS} = 0 to 10mA	-	2	5	mV
Output Ripple	V _{OVSS_RIPPLE}	I _{OVSS} = 30mA	-	-	10	mV
Current Limit	I _{OVSS_LIMIT}		-	150	200	mA
Discharge Resistance	R _{OVSS_RDIS}			100		Ω
Under Voltage Protection				80		%
UVP Detection Time				1.35		ms

12 Layout Guidelines

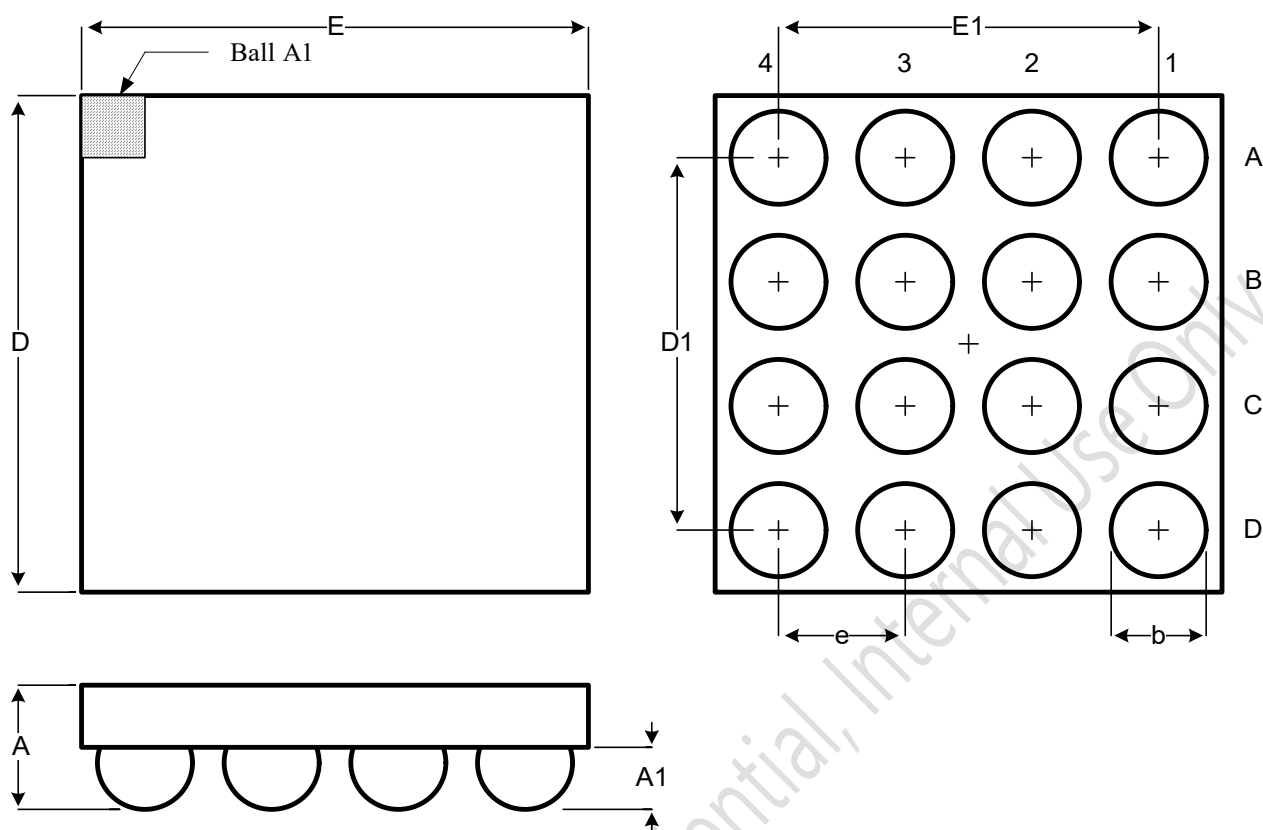
For the best performance of the BV6802/A, the basic principles listed should be strictly followed.

- Place C1 and C2 as close as possible to the PVIN and AVIN pins respectively.
- Place C3 and C6 as close as possible to the VOP and VON pins respectively
- Place C4, C5 and C7 as close as possible to the AVDD, OVDD and OVSS pins respectively
- Place L1 as close as possible to the LX1 and LX2 pins
- For good regulation, the traces should be wide and short especially for the high current output loop

BV6802/A



13 Outline Dimension



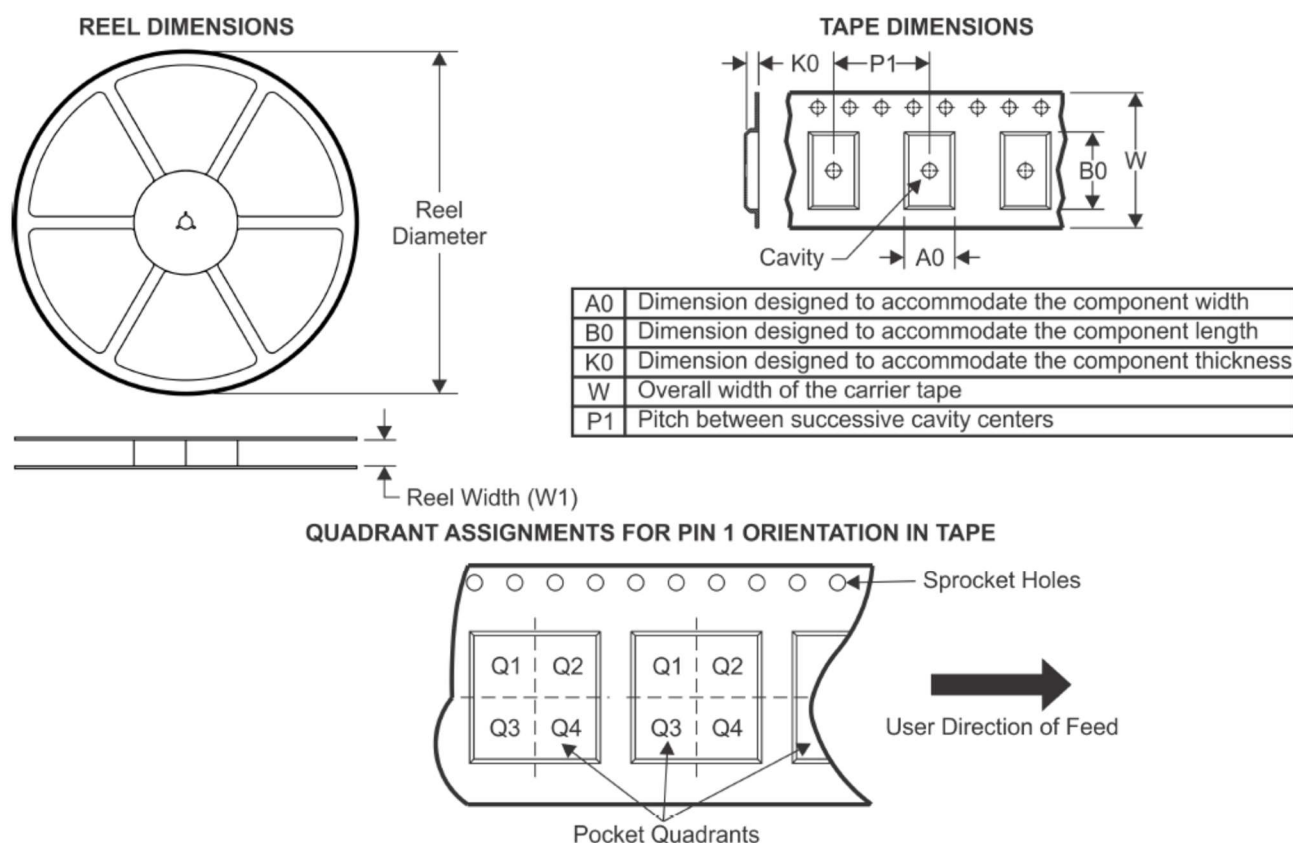
Symbol	Dimensions(mm)		Dimensions(inch)	
	Min.	Max.	Min.	Max.
A	0.527	0.621	0.021	0.024
A1	0.175	0.213	0.007	0.008
b	0.228	0.308	0.009	0.012
D	1.620	1.660	1.552	0.065
D1	1.200		0.047	
E	1.620	1.660	0.064	0.065
E1	1.200		0.047	
e	0.400		0.016	

14 Packaging Information

Orderable Device	Status ⁽¹⁾	Package Type	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ⁽⁴⁾
BV6802W	ACTIVE	WLCSP	16	3,000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-1 YEAR	-40 to 85	6802
BV6802AW	ACTIVE	WLCSP	16	3,000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-1 YEAR	-40 to 85	6802A

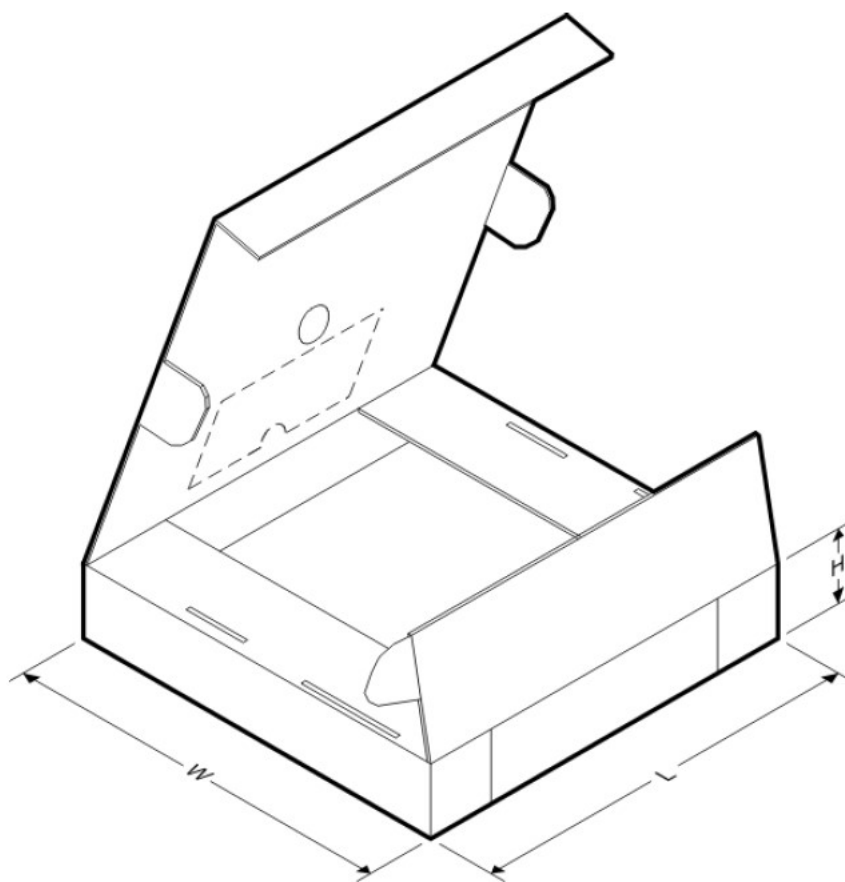
- The status is to reflect current situation in marketing.
ACTIVE: The product currently is on sale.
LAST TIME BUY in EOL: Bravotekcorp announced this product will be discontinued. Only last time buy supported within a half of a year.
SAMPLES BY REQUEST: The product is still in developing. Samples may or may not be available.
OBSOLETE: Bravotekcorp has terminated the production of this product.
- Green: Bravotekcorp defines that the product follow JS709B low halogen requirements of <= 1,000 ppm.
RoHS: Bravotekcorp defines that the product follows current EU RoHS requirements.
- MSL, Peak Temp.: The Moisture Sensitivity Level rating was based on JEDEC industry standard classification, and peak solder temperature.
- Device marking: The device marking of the product will follow Bravotekcorp's marking rule that may contain multiple information for tracing.

16 Tape and Reel Information



Device	Package Type	Pins	SPQ	Reel Diameters (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BV6802W	WLCSP	16	3000	180	9	1.77+/-0.05	1.77+/-0.05	0.75+/-0.05	4	8	Q1
BV6802AW	WLCSP	16	3000	180	9	1.77+/-0.05	1.77+/-0.05	0.75+/-0.05	4	8	Q1

17 Tape and Reel Box Dimension



Device	Package Type	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BV6802W	WLCSP	16	3000	183+/-3	183+/-3	85+/-3
BV6802AW	WLCSP	16	3000	183+/-3	183+/-3	85+/-3

18 VERSION HISTORY

Version #	Implemented By	Revision Date	Approved By	Approval Date	Reason
0.1	Stanley	11.25.2019			Initial Design Definition draft
0.2	Stanley	06.29.2020			Final Datasheet
0.3	Stanley	09.07.2020			Add Efficiency Curve on Page One
0.4	Stanley	12.02.2020			Add Packaging information, Tape and Reel information and box dimension
0.5	Stanley	05.24.2021			Application Circuit Modified
0.6	Stanley	11.29.2021			Add BV6802A for AVDD=3.3V

Template Version: 09/09, 2019