

130-dB, 32-Bit High-Performance DAC with Integrated Headphone Driver and Impedance Detection

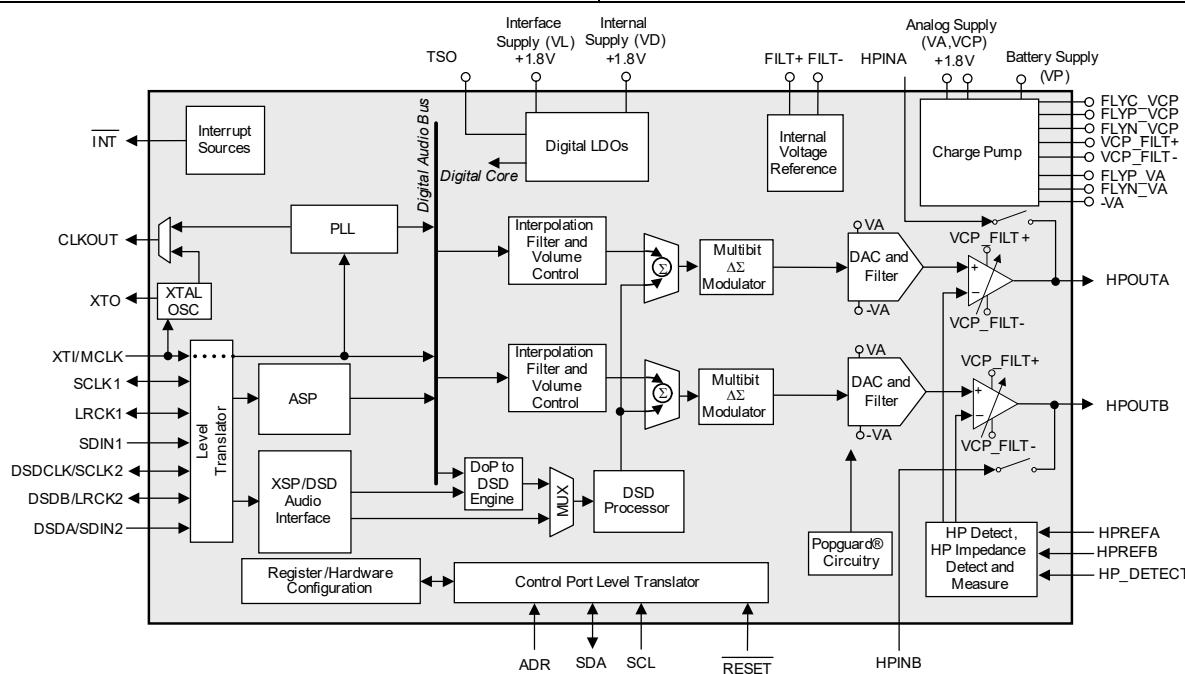
System Features

- Enhanced $\Delta\Sigma$ oversampling DAC architecture
 - 32-bit resolution
 - Up to 384-kHz sampling rate
 - Low clock jitter sensitivity
 - Auto mute detection
- Integrated high performance, ground-centered stereo headphone outputs
 - 130-dB dynamic range (A-weighted)
 - -115-dB total harmonic distortion + noise (THD+N)
 - 110-dB interchannel isolation
 - Up to 2-V_{rms} stereo output
 - Headphone power output
 - 30 mW per channel into 32 Ω
 - 5 mW per channel into 600 Ω
- Headphone detection
 - Headphone DC and AC impedance measurement
 - Headphone plug-in detection
 - Popguard® technology eliminates pop noise
- Integrated PLL
 - Support for 11.2896-/22.5792-, 12.288-/24.576-, 9.6-/19.2-, 12-/24-, and 13-/26-MHz system MCLK rates
 - Reference clock sourced from XTI/MCLK pin
 - System clock output
- Mono Mode (differential) support
- I₂C control—up to 1 MHz
- Wideband Flatness Mode Support

- Direct Stream Digital (DSD®) path
 - Up to 256×Fs DSD
 - Patented DSD processor
 - On-chip 50-kHz filter to meet Scarlet Book Super Audio Compact Disk (SACD) recommendations
 - Matched PCM and DSD analog output levels
 - Nondecimating volume control with 0.5-dB step size and soft ramp
 - DSD and Pulse-code modulation (PCM) mixing for alerts
 - Dedicated DSD and DoP pin interface
- Serial audio input path
 - Programmable Hi-Fi digital filter
 - Five selectable digital filter responses
 - Low-latency Mode minimizes pre-echo
 - 110 dB of stopband attenuation
 - Supports sample rates from 32 to 384 kHz
 - I₂S, right-justified, left-justified, TDM, and DSD-over-PCM (DoP) interface
 - Master or slave operation
 - Volume control with 0.5-dB step size and soft ramp
 - 44.1 kHz deemphasis and inverting feature
- Alternate headphone input
- 40-pin 5mm × 5mm QFN or 42-ball CSP package options

Applications

- Smart phones, tablets, portable media players, laptops, digital headphones, powered speakers, AVR, home theater systems, Blu-ray/DVD/SACD players, and pro audio



130 dB、32位高性能数模转换器，集成耳机驱动器及阻抗检测系统

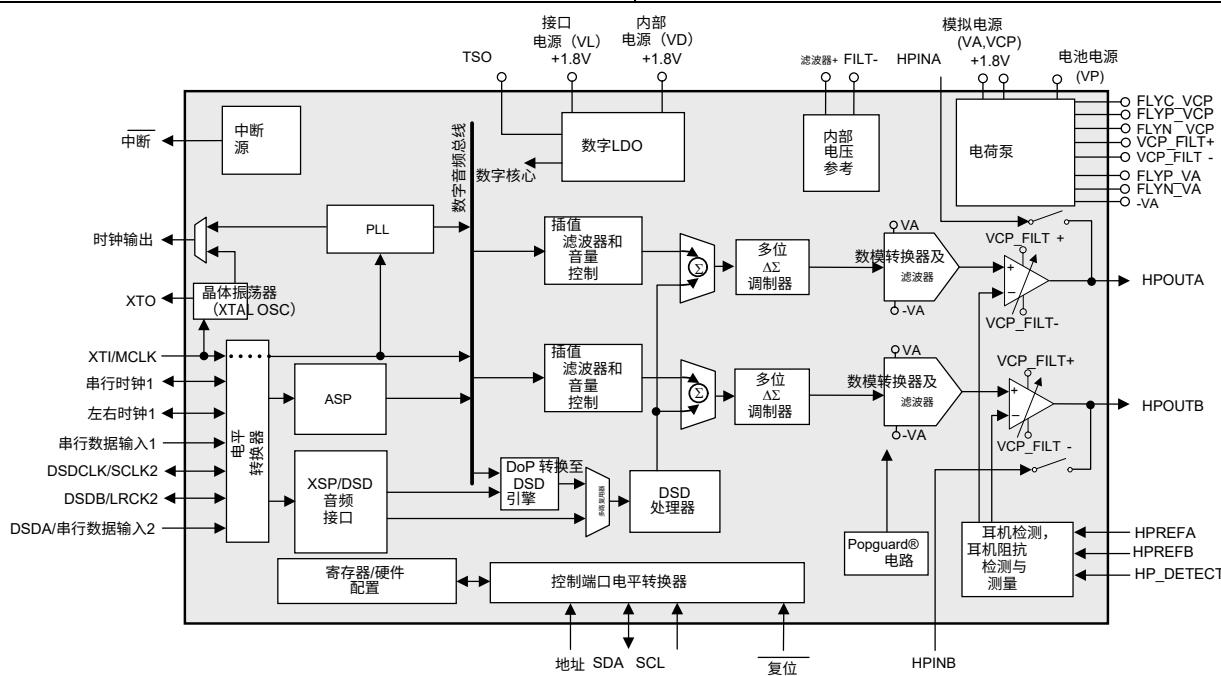
系统特性

- 增强型 $\Delta\Sigma$ 过采样数模转换器架构
 - 32 位分辨率
 - 最高 384 kHz 采样率
 - 低时钟抖动敏感度
 - 自动静音检测
- 集成高性能、接地中心立体声耳机输出
 - 130 dB 动态范围 (A 加权)
 - -115 dB 总谐波失真加噪声 (THD+N)
 - 110 dB 通道间隔离度
 - 最高 2 V_{rms} 立体声输出
 - 耳机功率输出 – 每声道 30 mW, 负载 32 Ω
 - 每通道 5 mW, 负载 600 Ω
- 耳机检测
 - 耳机直流和交流阻抗测量
 - 耳机插入检测
 - Popguard® 技术消除爆音
- 集成PLL
 - 支持 11.2896-/22.5792-、12.288-/24.576-、9.6-/19.2-、12-/24-及 13-/26 MHz 系统 MCLK 频率
 - 参考时钟源自 XTI/MCLK 引脚
 - 系统时钟输出
- 支持单声道模式 (差分)
- I²C 控制—最高 1 MHz
- 支持宽带平坦模式

- 直接流数字 (DSD®) 路径—最高 256·Fs DSD—专利 DS 处理器
 - 片内 50 kHz 滤波器, 符合 Scarlet Book 超级音频光盘 (SACD) 规范
 - 匹配的 PCM 和 DSD 模拟输出电平
 - 非抽取音量控制, 步进为 0.5 dB, 带软启动
 - DSD 与 脉冲编码调制 (PCM) 混合用于提示音
- 专用 DSD 和 DoP 引脚接口
- 串行音频输入通路
 - 可编程高保真数字滤波器
 - 五种可选数字滤波响应
 - 低延迟模式, 最大限度减少预回声
 - 110 dB 阻带衰减
 - 支持 32 至 384 kHz 采样率
 - I²S、右对齐、左对齐、TDM 及基于 PCM 的 DSD (DoP) 接口
 - 主从模式操作
 - 音量控制, 步进为 0.5 dB, 带软启动
 - 44.1 kHz 抑制及反相功能
- 备用耳机输入
 - 40 引脚 5mm × 5mm QFN 或 42 球 CSP 封装选项

应用

- 智能手机、平板电脑、便携式媒体播放器、笔记本电脑、数字耳机、有源扬声器、AVR、家庭影院系统、蓝光/DVD/SACD 播放器及专业音频设备



General Description

The CS43131 is a high-performance, 32-bit resolution, stereo audio DAC that supports up to 384-kHz sampling frequency with integrated low-noise ground-centered headphone amplifiers. The advanced 32-bit oversampled multibit modulator with mismatch shaping technology eliminates distortion due to on-chip component mismatch. Proprietary digital-interpolation filters support five selectable filter responses with pseudo-linear phase and ultralow latency to minimize pre-echos and ringing artifacts. An on-chip programmable filter is available for further response customization. Other features include volume control with 0.5-dB steps, wideband flatness mode support, and digital deemphasis for 44.1-kHz sample rate.

The integrated ground-centered stereo headphone amplifiers are capable of delivering more than 30 mW into 32- Ω load or 5 mW into 600- Ω load per channel at full performance. It is also capable of generating 2 V_{rms} on a 600- Ω load. Proprietary headphone impedance detection enables wide-band impedance detection for further digital post-processing. An internal stereo audio switch with true bypass supports an alternate analog input path for interfacing with external audio sources to minimize the overall bill-of-materials cost and PCB area.

The patented on-chip DSD processor preserves audio integrity by allowing signal processing such as volume control and 50-kHz Scarlet Book recommended filtering to be applied directly to the DSD stream without an intermediate decimation stage. Additional features like volume matching and channel mixing enable seamless transition between DSD and PCM playback paths.

The CS43131 accepts I²S, right-justified, left-justified, and TDM-format PCM data at sample rates from 32 to 384 kHz. The industry-standard high-speed I²C interface capable of up to 1-MHz operation provides easy configuration control. An integrated PLL allows for maximum clocking flexibility in any system. Popguard® technology eliminates output transients upon power-up or power-down events.

The CS43131 is available in a commercial-grade 42-ball WLCSP or 40-pin QFN package for operation from -20°C to +70°C.

概述

CS43131 是一款高性能、32 位分辨率的立体声音频数模转换器，支持最高 384 kHz 采样频率，集成低噪声接地式耳机放大器。先进的 32 位过采样多位调制器采用失配整形技术，消除片上元件失配引起的失真。专有数字插值滤波器支持五种可选滤波响应，具备伪线性相位和超低延迟，最大限度减少预回声和振铃伪影。片上可编程滤波器可用于进一步响应定制。

其他特性包括以 0.5 dB 步进的音量控制、宽带平坦模式支持以及针对 44.1 kHz 采样率的数字去强调功能。

集成的接地式立体声耳机放大器在满性能下，能够向 32- Ω 负载输出超过 30 mW，或向 600- Ω 负载每声道输出 5 mW。它还能够在 600- Ω 负载上输出 2 Vrms 电压。

专有的耳机阻抗检测技术实现宽带阻抗检测，便于进一步的数字后处理。

内部立体声音频开关具备真实旁路功能，支持备用模拟输入路径，可与外部音频源接口连接，从而最大限度降低整体物料成本和 PCB 面积。

专利片上 DSD 处理器通过允许直接对 DSD 流进行音量控制及 50 kHz Scarlet Book 推荐滤波等信号处理，避免中间抽取阶段，从而保持音频完整性。附加功能如音量匹配和声道混合实现 DSD 与 PCM 播放路径之间的无缝切换。

CS43131 支持 I²S、右对齐、左对齐及 TDM 格式的 PCM 数据，采样率范围为 32 至 384 kHz。行业标准高速 I²C 接口支持最高 1 MHz 操作，便于配置控制。集成 PLL 提供系统中最大的时钟灵活性。Popguard® 技术消除电源开启或关闭时的输出瞬变。

CS43131 提供商用级 42 球 WLCSP 封装或 40 引脚 QFN 封装，工作温度范围为 -20°C 至 +70°C。

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1 Pin Assignments and Descriptions

1.1 40-Pin QFN (Top-Down, Through-Package View)

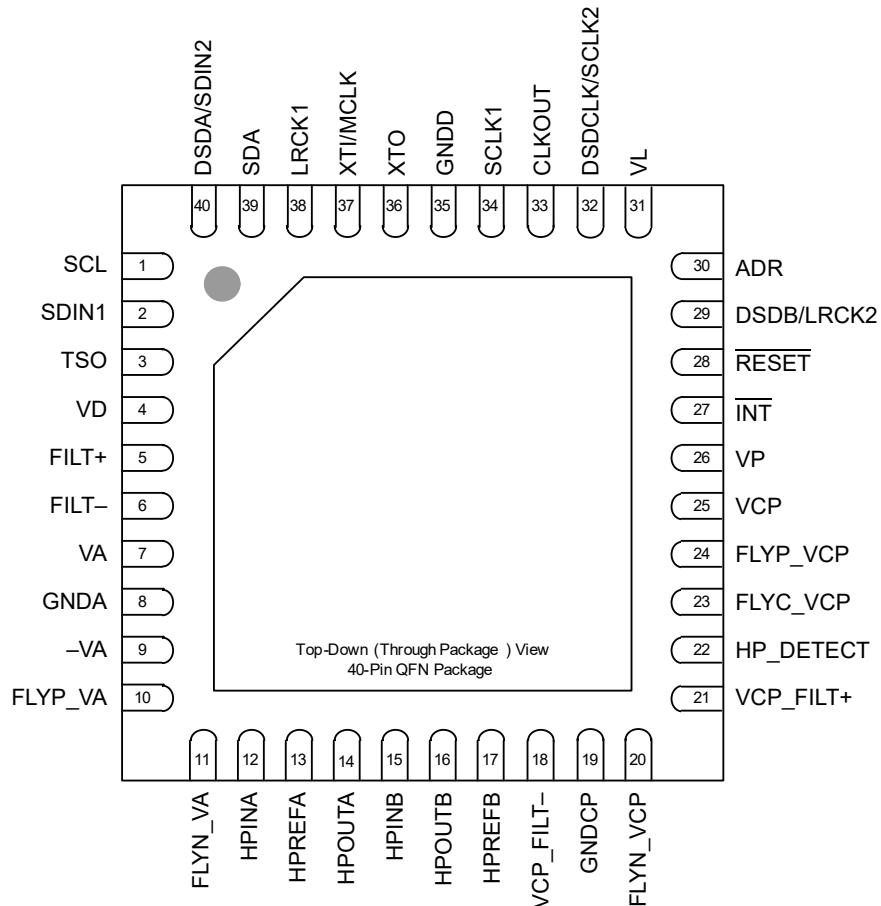


Figure 1-1. Top-Down (Through-Package) View—QFN 40-Pin Diagram

1 引脚分配及说明

1.1 40 引脚 QFN (顶视图, 穿封装视图)

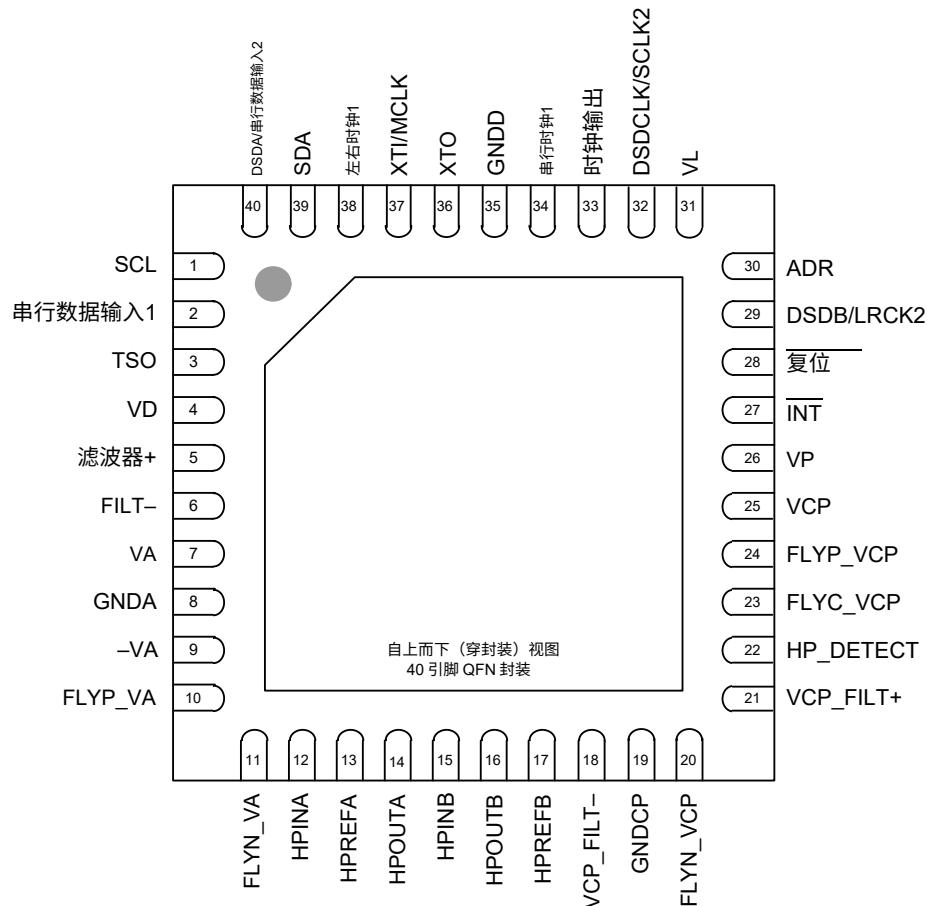


图 1-1. 自上而下 (穿封装) 视图——QFN 40 引脚图

1.2 42-Ball WLCSP (Top-down, Through-Package View)

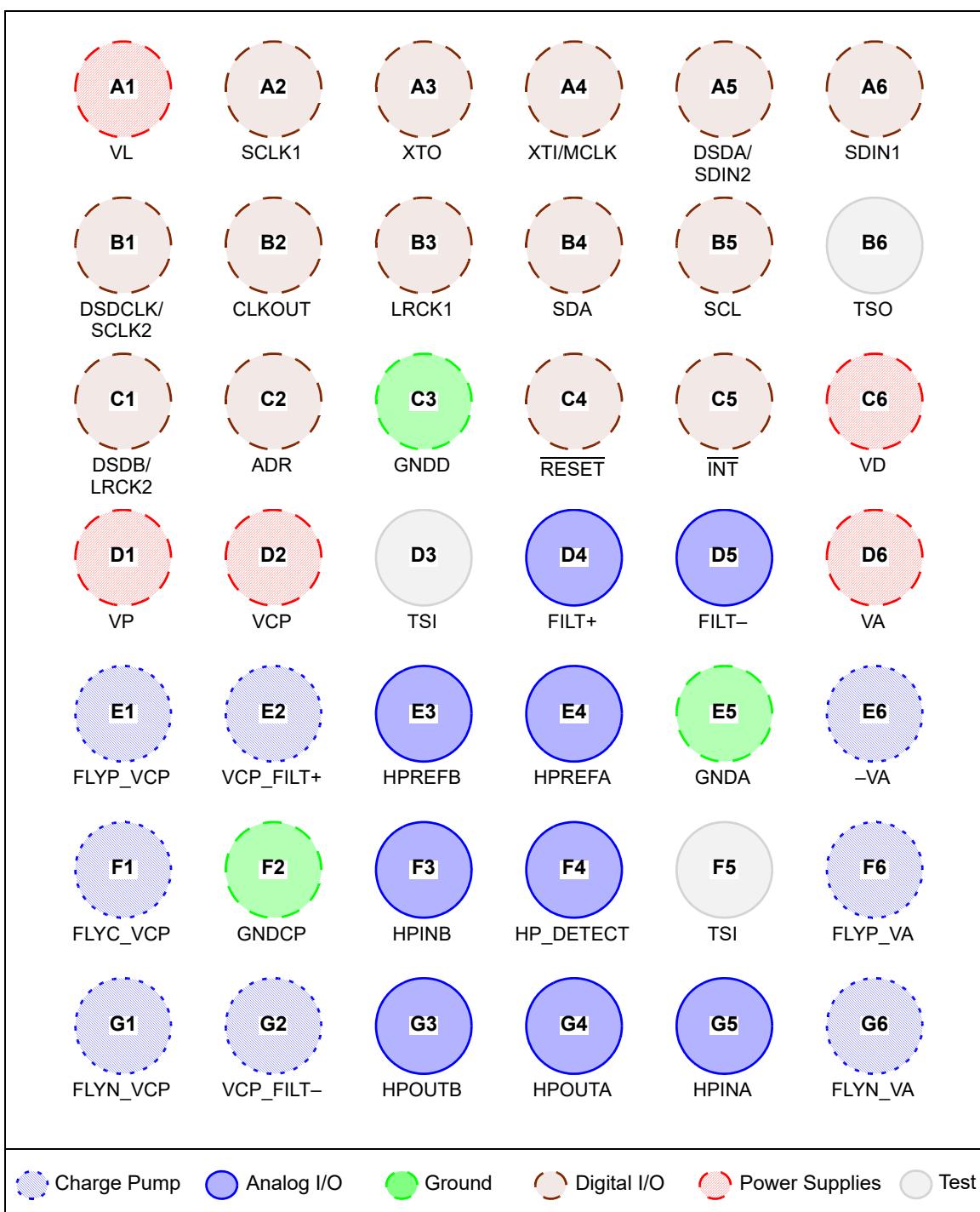


Figure 1-2. Top-Down (Through-Package) View—42-Ball WLCSP Package

1.2 42球WLCSP (自上而下, 封装透视图)

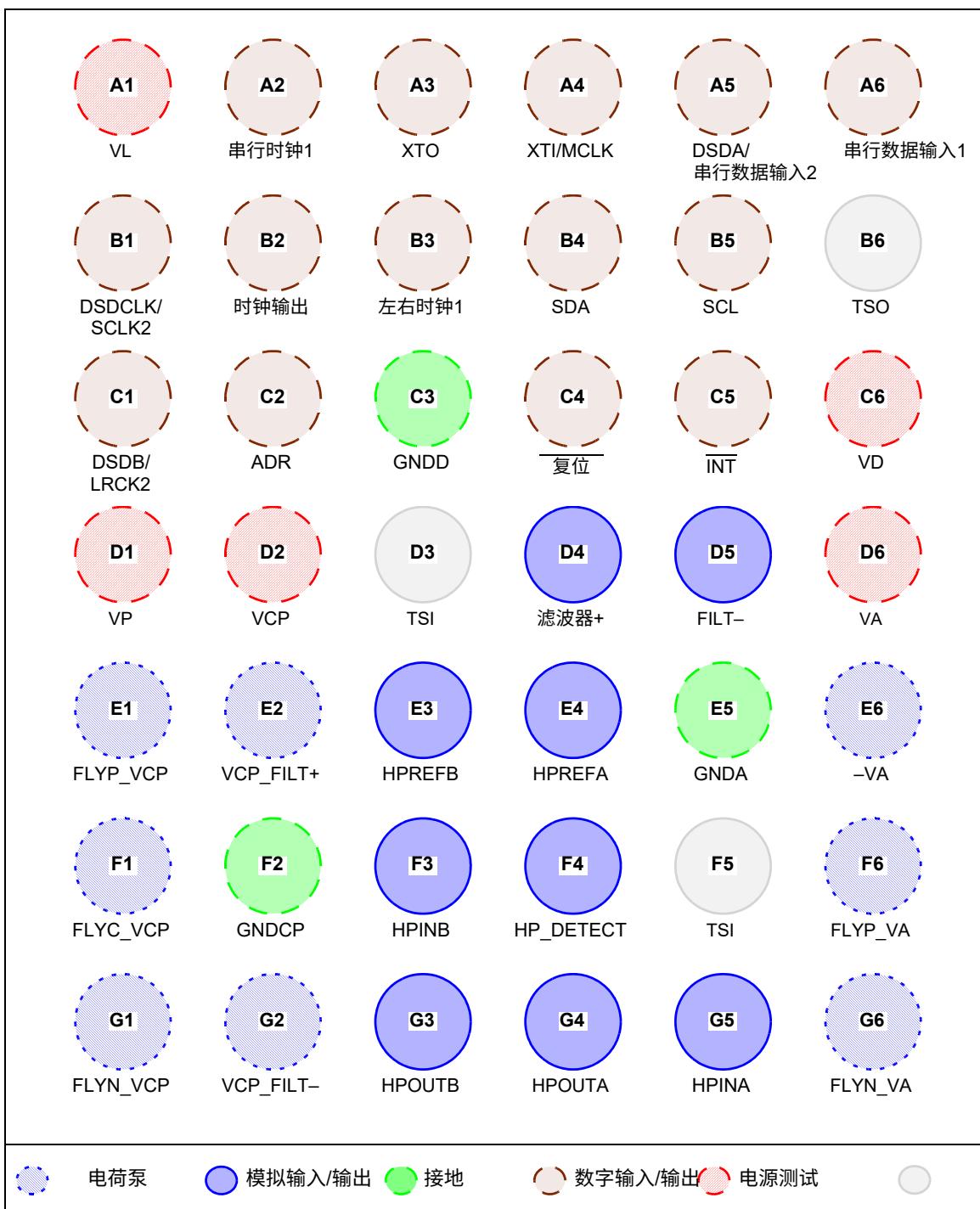


图1-2。自上而下 (封装透视) 视图——42球WLCSP封装

1.3 Pin Descriptions

Table 1-1. Pin Descriptions

Pin Name	QFN Pin #	WL CSP Ball	Power Supply	I/O	Pin Description	Internal Connection	Digital I/O Driver	Digital I/O Receiver
Digital I/O 								
ADR	30	C2	VL	I	Address Bit (I²C). In I ² C Mode, ADR is a chip address pin.	—	—	—
CLKOUT	33	B2	VL	O	CLK Output. Single-ended clock output sourced from PLL or buffered crystal.	Weak pull-down	CMOS output	—
SCLK1	34	A2	VL	I/O	Serial Audio Input Bit Clock 1. Serial bit clock for audio data on the SDIN pins.	Weak pull-down	CMOS output	Hysteresis on CMOS input
LRCK1	38	B3	VL	I/O	Serial Audio Input Left/Right Clock. Word-rate clock for the audio data on the SDIN pins.	Weak pull-down	CMOS output	Hysteresis on CMOS input
SDIN1	2	A6	VL	I	Serial Audio Input Data Port. Audio data serial input pin 1.	Weak pull-down	—	Hysteresis on CMOS input
DSDA/SDIN2	40	A5	VL	I	DSD Data Input A/Serial Data In 2. DSD audio or PCM audio data serial input pin 2.	Weak pull-down	—	Hysteresis on CMOS input
DSDB/LRCK2	29	C1	VL	I/O	DSD Data Input B/Serial Audio Input Left/Right Clock 2. DSD audio data serial input pin or word rate clock for the audio data on the SDIN2 pin.	Weak pull-down	CMOS output	Hysteresis on CMOS input
DSDCLK/SCLK2	32	B1	VL	I/O	DSD Clock Input/Serial Audio Input Bit Clock 2. DSD clock input. Serial bit clock for audio data on the SDIN2 pin.	Weak pull-down	CMOS output	Hysteresis on CMOS input
INT	27	C5	VP	O	Interrupt. When pulled up, works as system interrupt pin. Open drain, active low programmable.	—	CMOS open-drain output	—
RESET	28	C4	VP	I	System Reset. The device enters system reset when enabled.	—	—	Hysteresis on CMOS input
SDA	39	B4	VL	I/O	Serial Control Data I/O (I²C). In I ² C Mode, SDA is the control I/O data line.	—	CMOS open-drain output	Hysteresis on CMOS input
SCL	1	B5	VL	I	Software Clock (I²C). Serial control interface clock used to clock control data bits into and out of the CS43131.	—	—	Hysteresis on CMOS input
XTI/MCLK	37	A4	VL	I	Crystal/Oscillator Input/MCLK In. Crystal or digital clock input for the master clock.	Weak pull-down	—	Hysteresis on CMOS input
XTO	36	A3	VL	O	Crystal/Oscillator Output. Crystal output.	Weak pull-down	CMOS output	—
Analog I/O 								
FILT+	5	D4	VA	O	Positive/Negative Voltage Reference. Positive/negative reference voltage for DAC.	—	—	—
FILT-	6	D5						
HP DETECT	22	F4	VP	I	Headphone Detect. Can be configured to be debounced on unplugged and plugged events before it is presented as a noninterrupt status bit (HPDETECT).	—	Hi-Z	—
HPINB	15	F3	VCP_	I	Headphone Audio Input. For interfacing low power audio source, an alternate analog input path for the headphone output. Refer to analog specification table for full-scale input level.	Weak pull-down	—	—
HPINA	12	G5	FILT±					
HPOUTB	16	G3	VCP_	O	Headphone Audio Output. Refer to analog specification table for full-scale output level.	—	—	—
HPOUTA	14	G4	FILT±					
HPREFB	17	E3	VCP_	I	Headphone Output Reference. Reference for headphone amplifier and detect.	—	—	—
HPREFA	13	E4	FILT±					
Power Supplies 								
VL	31	A1	N/A	I	Logic Power. Input/Output power supply, typically +1.8 V.	—	—	—
VD	4	C6	N/A	I	Internal Digital Power. Internal digital power supply, typically +1.8 V.	—	—	—
VA	7	D6	N/A	I	Analog Power. Power supply for the internal analog section.	—	—	—

1.3 引脚说明

表 1-1. 引脚说明

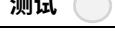
引脚名称	引脚号	WLCSP 球号	电源	电源输入 / 输出	引脚说明	内部连接	数字输入/输出 驱动	数字输入/输出 接收
数字输入/输出								
ADR	30	C2	VL	输入 地址位 (I ² C)	在 I ² C 模式下，ADR 为芯片地址引脚。	—	—	—
时钟输出	33	B2	VL	输出 时钟输出。	单端时钟输出，源自 PLL 或缓冲晶振。	弱下拉	CMOS 输出	—
串行时钟1	34	A2	VL	输入/输出 串行音频输入位时钟1。	用于SDIN引脚音频数据的串行位时钟。	弱下拉	CMOS 输出	CMOS 输入端的迟滞
左右时钟1	38	B3	VL	输入/输出 串行音频输入左右时钟。	SDIN引脚音频数据的字时钟。	弱下拉	CMOS 输出	CMOS 输入端的迟滞
串行数据输入1	2	A6	VL	输入 串行音频输入数据端口。	音频数据串行输入引脚1。	弱下拉	—	CMOS 输入端的迟滞
DSDA/ 串行数据输入2	40	A5	VL	输入 DSD数据输入A/串行数据输入2。	DSD音频或PCM音频数据串行输入引脚2。	弱下拉	—	CMOS 输入端的迟滞
DSDB/ 左右时钟2	29	C1	VL	输入/输出 DSD数据输入B/串行音频输入左右时钟2。	DSD音频数据串行输入引脚或SDIN2引脚音频数据的字时钟。 SDIN2引脚上的音频数据字时钟。	弱下拉	CMOS 输出	CMOS 输入端的迟滞
DSDCLK/ SCLK2	32	B1	VL	输入/输出 DSD时钟输入/串行音频输入位时钟2。	DSD时钟输入。用于SDIN2引脚音频数据的串行位时钟。	弱下拉	CMOS 输出	CMOS 输入端的迟滞
INT	27	C5	VP	输出 中断。	上拉时作为系统中断引脚使用。开漏，低电平有效，可编程。	—	CMOS 开漏输出	—
复位	28	C4	VP	输入 系统复位。	启用时，设备进入系统复位状态。	—	—	CMOS 输入端的迟滞
SDA	39	B4	VL	输入/输出 串行控制数据输入/输出 (I ² C)。	在 I ² C 模式下，SDA 为控制输入/输出数据线。	—	CMOS 开漏输出	CMOS 输入端的迟滞
SCL	1	B5	VL	输入 软件时钟 (I ² C)。	串行控制接口时钟，用于将控制数据位时钟输入和输出至CS43131。	—	—	CMOS 输入端的迟滞
XTI/MCLK	37	A4	VL	输入 晶体/振荡器输入/MCLK输入。	主时钟的晶体或数字时钟输入。	弱下拉	—	CMOS 输入端的迟滞
XTO	36	A3	VL	○ 晶体振荡器输出。	晶体输出。	弱下拉	CMOS 输出	—
模拟输入/输出								
FILT+	5	D4	VA	○ 正/负电压参考。	DAC的正负参考电压。	—	—	—
FILT-	6	D5						
HP_DETECT	22	F4	VP	! 耳机检测。	可配置为在拔出和插入事件去抖后，作为非中断状态位 (HPDETECT) 呈现。	—	高阻态	—
HPINB	15	F3	VCP_	! 耳机音频输入。	用于连接低功耗音频源，作为耳机输出的备用模拟输入路径。满量程输入电平请参见模拟规格表。	弱下拉	—	—
HPINA	12	G5	FILT±					
HPOUTB	16	G3	VCP_	○ 耳机音频输出。	满量程输出电平请参见模拟规格表。	—	—	—
HPOUTA	14	G4	FILT±					
HPREFB	17	E3	VCP_	! 耳机输出参考。	耳机放大器及检测的参考电压。	—	—	—
HPREFA	13	E4	FILT±					
电源								
VL	31	A1	N/A	! 逻辑电源。	输入/输出电源，典型值为 +1.8 V。	—	—	—
VD	4	C6	N/A	! 内部数字电源。	内部数字电源，典型值为 +1.8 V。	—	—	—
VA	7	D6	N/A	! 模拟电源。	内部模拟部分的电源。	—	—	—

Table 1-1. Pin Descriptions (Cont.)

Pin Name	QFN Pin #	WLCSP Ball	Power Supply	I/O	Pin Description	Internal Connection	Digital I/O Driver	Digital I/O Receiver
VCP	25	D2	N/A	I	Charge Pump Supply. Provides charge pump voltage to the headphone Class H analog output circuit.	—	—	—
VP	26	D1	N/A	I	Battery supply. Provides voltage to the headphone Class H circuit.	—	—	—
Ground 								
GNDD	35	C3	N/A	I	Digital and I/O Ground. Ground for the I/O and core logic. GNDA, GNDP, and GNDD must be connected to a common ground area under the chip.	—	—	—
GNDA	8	E5	N/A	I	Analog Ground. Ground reference for the internal analog section. GNDA, GNDP, and GNDD must be connected to a common ground area under the chip.	—	—	—
GNDP	19	F2	N/A	I	Charge Pump Ground. Ground reference for the charge pump section. GNDA, GNDP, and GNDD must be connected to a common ground area under the chip.	—	—	—
Charge Pump 								
VCP_FILT+	21	E2	VCP/ VP 1	I/O	Inverting Charge Pump Filter Connection. Power supply from the inverting charge pump that provides the positive/negative rail for the analog output. When operating in external VCP_FILT mode, these pins can directly take in supply voltage.	—	—	—
VCP_FILT-	18	G2						
-VA	9	E6	VA	O	-VA Negative Charge Pump Output. Negative charge pump output for DAC rail. It is derived from VA.	—	—	—
FLYP_VA	10	F6	VA	O	-VA Charge Pump Cap Positive/Negative Node. Positive/negative nodes for the DAC negative charge pump's flying capacitor.	—	—	—
FLYN_VA	11	G6						
FLYP_VCP	24	E1	VCP/ VP 1	O	-VCP Charge Pump Cap Positive Node. Positive node for the analog output negative charge pump's flying capacitor.	—	—	—
FLYC_VCP	23	F1	VCP/ VP 1	O	-VCP Charge Pump Cap Center Node. Center node for the analog output negative charge pump's flying capacitor.	—	—	—
FLYN_VCP	20	G1	VCP_FILT±	O	-VCP Charge Pump Cap Negative Node. Negative node for the analog output negative charge pump's flying capacitor.	—	—	—
Test 								
TSO	3	B6	N/A	I/O	Test Output.	—	—	—
TSI	—	D3, F5			Test Input.	—	—	—

1. The power supply is determined by ADPT_PWR setting (see [Section 4.3.1](#)). VP is used if ADPT_PWR = 001 (VP_LDO Mode) or when necessary for ADPTPWR = 111 (Adapt-to-Signal Mode).

表 1-1。引脚描述 (续)

引脚名称	引脚号	WLCSP 球号	电源/电源输入/输出	引脚说明	内部连接	数字输入/输出驱动	数字输入/输出接收
VCP	25	D2	N/A	电荷泵电源。为耳机 Class H 模拟输出电路提供电荷泵电压。	—	—	—
VP	26	D1	N/A	电池电源。为耳机 Class H 电路提供电压。	—	—	—
接地 							
GNDD	35	C3	N/A	数字及输入/输出接地。输入/输出及核心逻辑的接地。GNDA、GNDPC 和 GNDD 必须连接至芯片下方的公共接地区域。	—	—	—
GNDA	8	E5	N/A	模拟接地。内部模拟部分的接地参考。GNDA、GNDPC 和 GNDD 必须连接至芯片下方的公共接地区域。	—	—	—
GNDCP	19	F2	N/A	输入 电荷泵接地。电荷泵部分的接地参考。GNDA、GNDPC 和 GNDD 必须连接至芯片下方的公共接地区域。	—	—	—
电荷泵 							
VCP_FILT+	21	E2	VCP/ VP 1	输入/输出 反相电荷泵滤波器连接。来自反相电荷泵的电源，为模拟输出提供正负电源轨。在外部 VCP_FILT 模式下工作时，这些引脚可直接接收电源电压。	—	—	—
VCP_FILT-	18	G2					
-VA	9	E6	VA	输出 VA 负电荷泵输出。DAC 电源轨的负电荷泵输出，源自 VA。	—	—	—
FLYP_VA	10	F6		VA 输出 -VA 电荷泵电容正负节点。DAC 负电荷泵飞电容的正负节点	—	—	—
FLYN_VA	11	G6		。			
FLYP_VCP	24	E1	VCP/ VP 1	O -VCP 电荷泵电容正极节点。模拟输出负电荷泵飞电容的正极节点。	—	—	—
FLYC_VCP	23	F1	VCP/ VP 1	O -VCP 电荷泵电容中心节点。模拟输出负电荷泵飞电容的中心节点。	—	—	—
FLYN_VCP	20	G1	VCP_FILT±	O -VCP 电荷泵电容负极节点。模拟输出负电荷泵飞电容的负极节点。	—	—	—
测试 							
TSO	3	B6		不适用 输入/输出 测试输出。	—	—	—
TSI	—	D3, F5		测试输入。	—	—	—

1. 电源由 ADPT_PWR 设置决定（参见第 4.3.1 节）。当 ADPT_PWR = 001 (VP_LDO 模式) 或 ADPT_PWR = 111 (自适应信号模式) 且需要时，使用 VP。

1.4 Electrostatic Discharge (ESD) Protection Circuitry



ESD-sensitive device. The CS43131 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD standards.

[Fig. 1-3](#) provides a composite view of the ESD domains showing the ESD protection paths between each pad and the substrate (GND), as well as the interrelations between some domains. Note that this figure represents the structure for the internal protection devices and that additional protections can be implemented as part of the integration into the board.

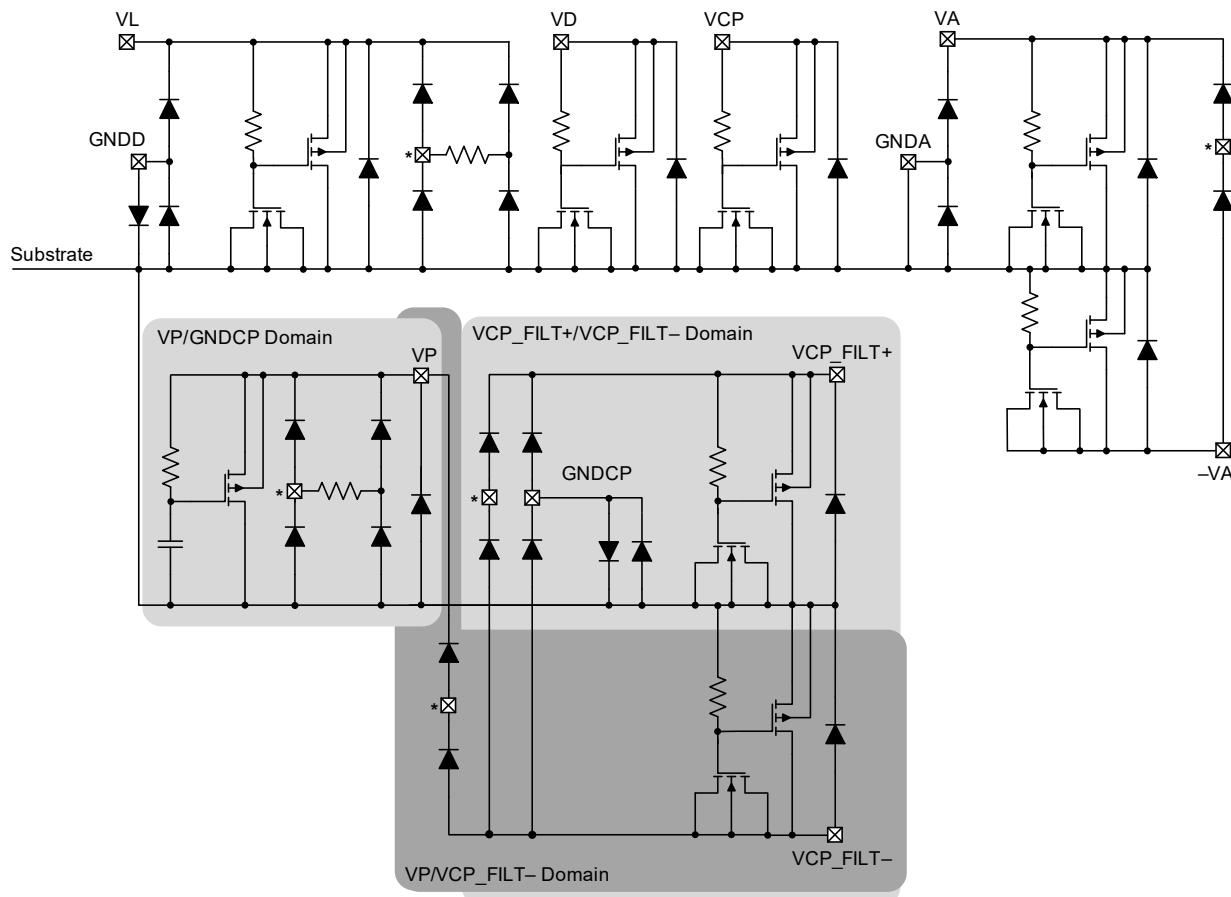
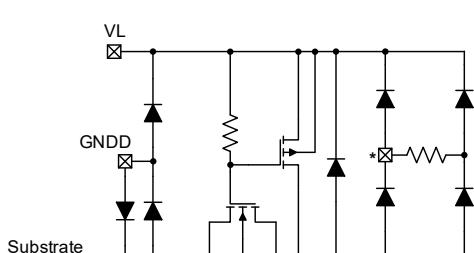


Figure 1-3. Composite ESD Topology

[Table 1-2](#) shows the individual ESD domains and lists the pins associated with each domain.

Table 1-2. ESD Domains

ESD Domain	Signal Name (See * in Topology Figures for Pad)	Topology
VL/GNDD	ADR DSDCLK/SCLK2 SCL SDA DSDB/LRCK2 DSDA/SDIN2 SDIN1 LRCK1 SCLK1 CLKOUT XTI/MCLK XTO	

1.4 静电放电 (ESD) 保护电路



ESD敏感器件。CS43131采用CMOS工艺制造。因此，其对过高的静电电压具有通用的敏感性，可能导致损坏。在操作和存储该器件时，必须采取适当的ESD防护措施。该器件符合当前JEDEC静电放电标准。

图 1-3 展示了静电放电 (ESD) 域的综合视图，显示了每个焊盘与基板 (GND) 之间的ESD保护路径，以及部分域之间的相互关系。请注意，该图表示内部保护器件的结构，额外的保护措施可作为板级集成的一部分实现。

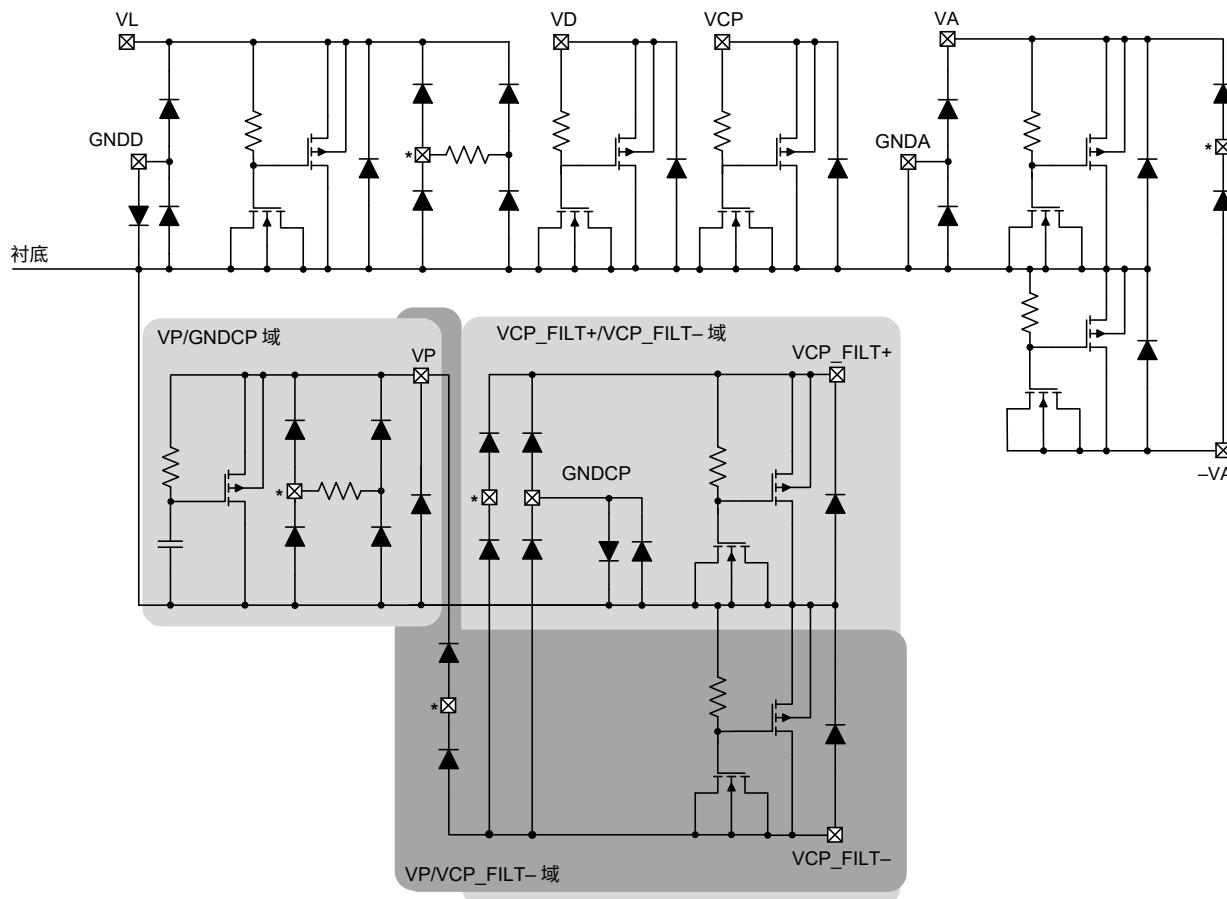


图 1-3. 综合ESD拓扑结构

表 1-2 显示了各个ESD域，并列出了与每个域相关的引脚。

表 1-2. ESD域

ESD域	信号名称 (参见拓扑图中焊盘的*标记)	拓扑结构
VL/GNDD	ADR D SDCLK/SCLK2 SC L SD A DS DB/LRCK2 DS DA/SDIN2 串行数据 输入1 L RCK1 S CLK1 CL KOUT XTI/ MCLK	<p>该图展示了VL和GNDD引脚的ESD保护拓扑。VL引脚直接连接到衬底。GNDD引脚通过一个二极管连接到衬底，然后通过一个开关元件连接到GNDD焊盘。GNDD焊盘再通过一个二极管连接到衬底，最后通过一个开关元件连接到GNDD引脚。此外，GNDD引脚还通过一个二极管连接到VCP_FILT+引脚。</p>

Table 1-2. ESD Domains (Cont.)

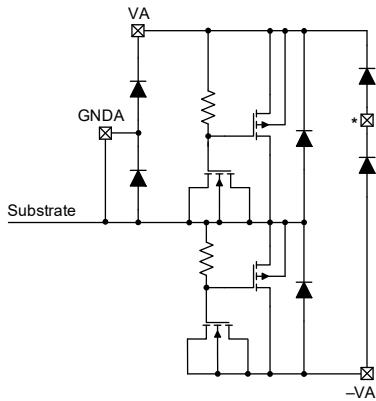
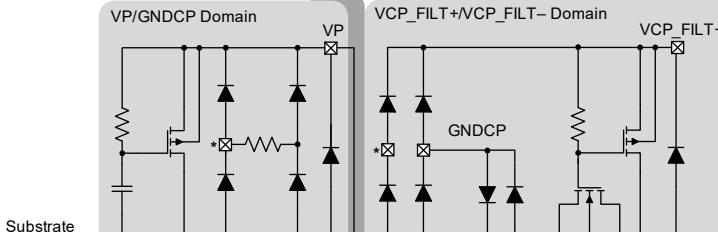
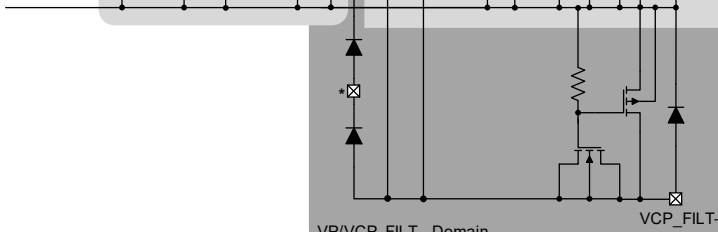
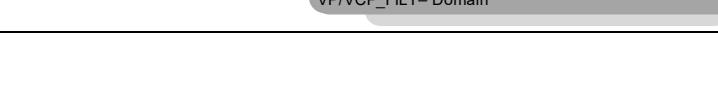
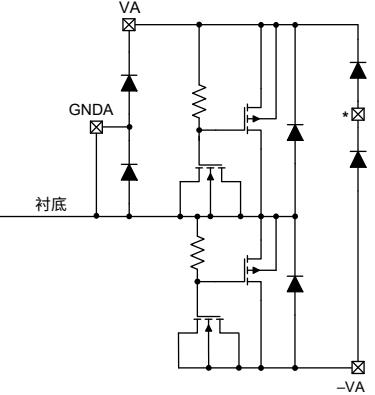
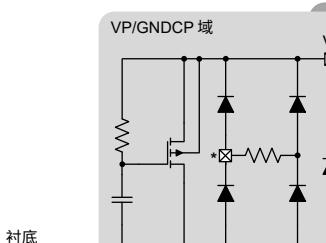
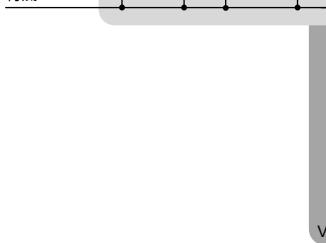
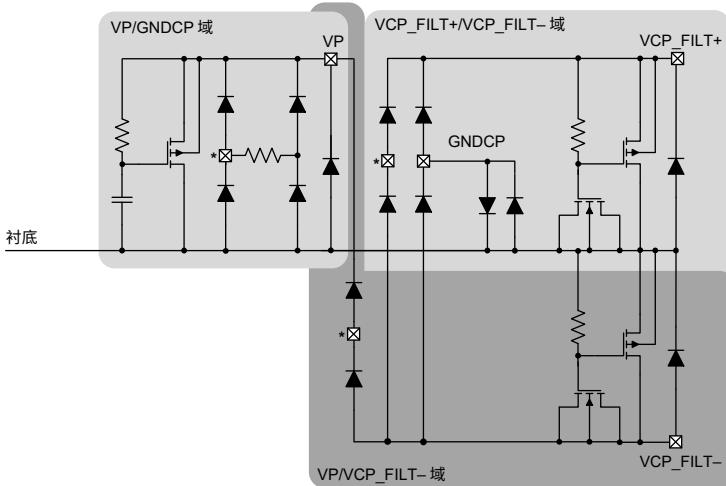
ESD Domain	Signal Name (See * in Topology Figures for Pad)	Topology
VA/-VA	FLYN_VA FLYP_VA FILT+ FILT-	 <p>This diagram shows the ESD protection circuit for the VA/-VA domain. It includes protection for four signals: FLYN_VA, FLYP_VA, FILT+, and FILT-. The circuit uses a combination of diodes, resistors, and transistors to provide protection. A substrate connection is also present.</p>
VP/GNDCP	RESET INT	 <p>This diagram shows the ESD protection circuit for the VP/GNDCP domain. It includes protection for two signals: RESET and INT. The circuit uses diodes and resistors to provide protection.</p>
VP/VCP_FILT-	FLYP_VCP FLYC_VCP HP_DETECT	 <p>This diagram shows the ESD protection circuit for the VP/VCP_FILT- domain. It includes protection for three signals: FLYP_VCP, FLYC_VCP, and HP_DETECT. The circuit uses diodes and resistors to provide protection.</p>
VCP_FILT+/ VCP_FILT-	FLYN_VCP HPINA HPINB HPOUTA HPOUTB HPREFA HPREFB	 <p>This diagram shows the ESD protection circuit for the VCP_FILT+/VCP_FILT- domain. It includes protection for multiple signals: FLYN_VCP, HPINA, HPINB, HPOUTA, HPOUTB, HPREFA, and HPREFB. The circuit is divided into three regions: VP/GNDCP Domain, VCP_FILT+/VCP_FILT- Domain, and VP/VCP_FILT- Domain. Each region contains specific protection components like diodes, resistors, and transistors.</p>

表 1-2. 静电放电域 (续)

ESD域	信号名称 (参见拓扑图中焊盘的*标记)	拓扑结构
VA/-VA	FLYN_VA FLYP_VA 滤波器+ FILT-	
VP/GNDPCP	复位 INT	
VP/VCP_FILT-	FLYP_VCP FLYC_VCP HP_DETECT	
VCP_FILT+/VCP_FILT-	FLYN_VCP HPINA HPINB HPOUTA HPOUTB HPREFA HPREFB	

2 Typical Connection Diagram

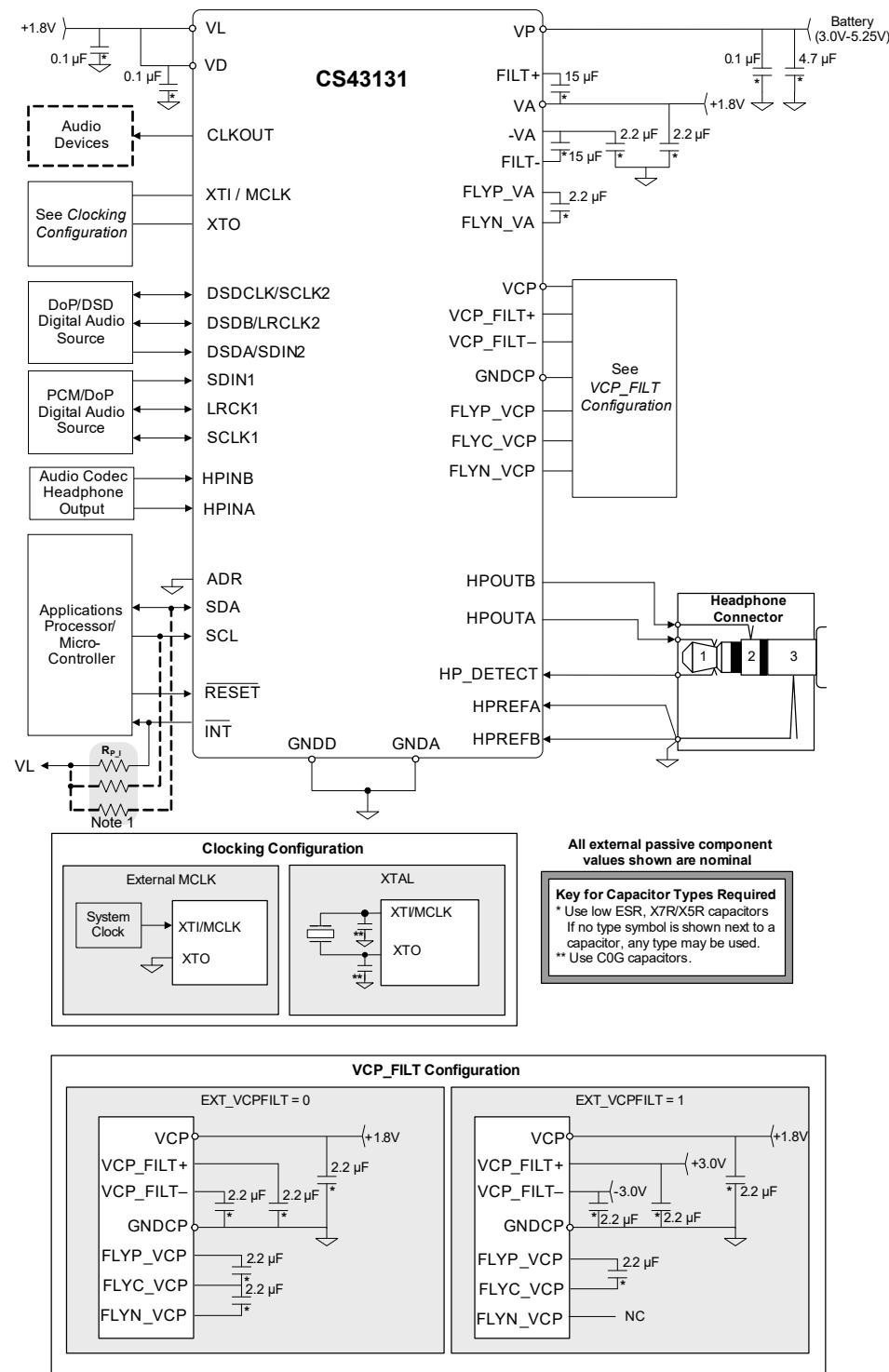


Figure 2-1. Typical Connection Diagram

2 典型连接图

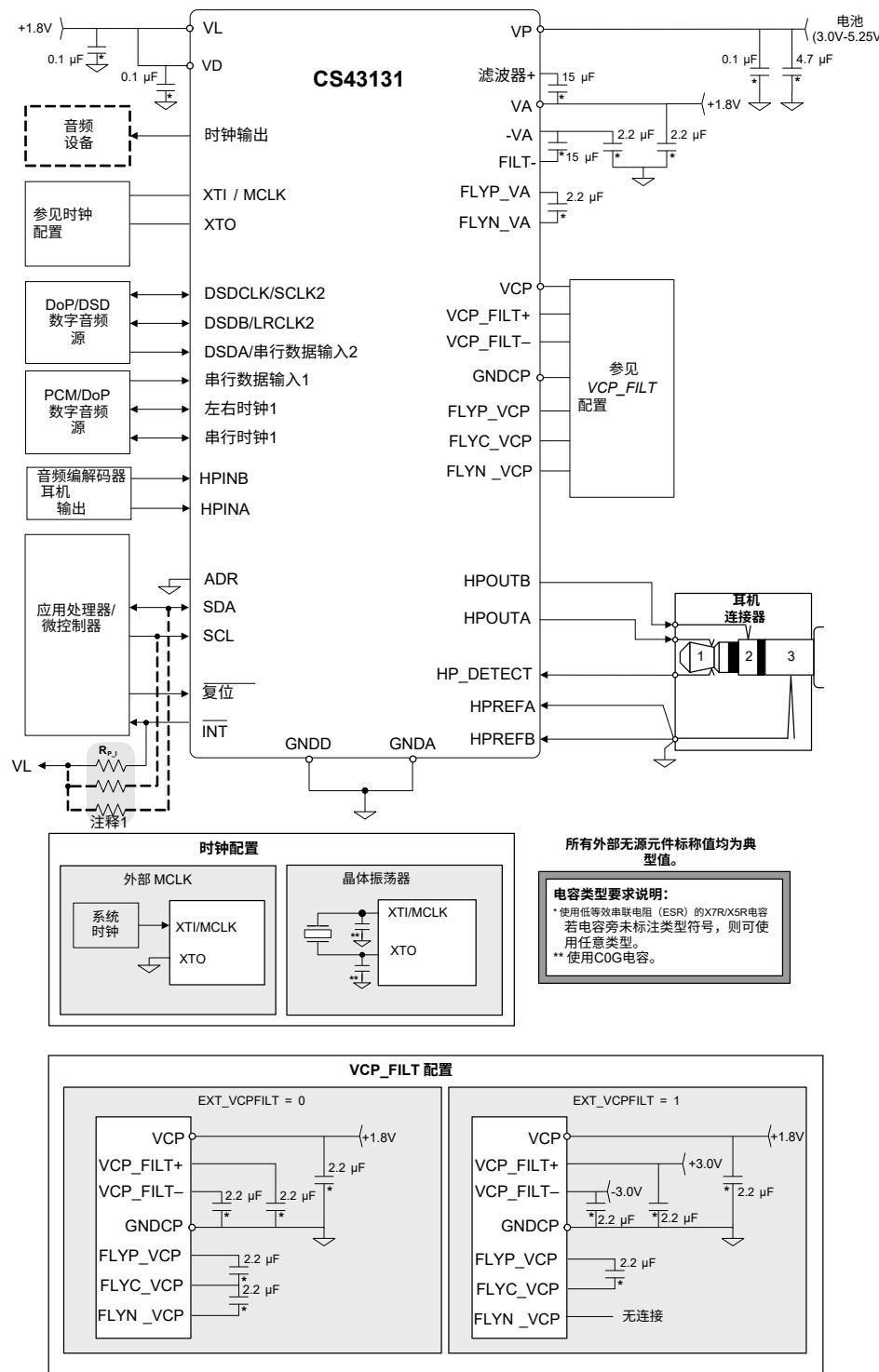


图 2-1. 典型连接图

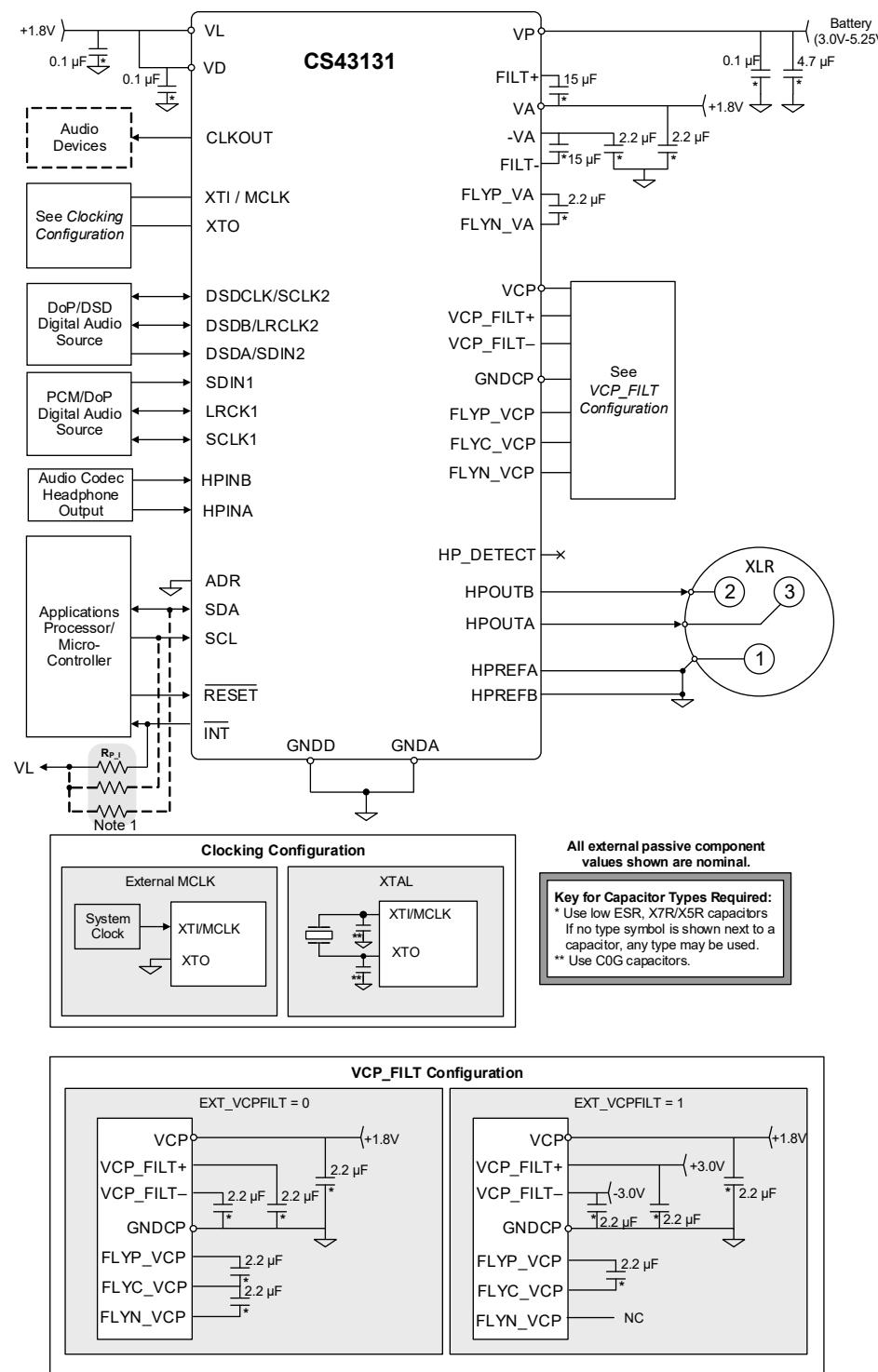
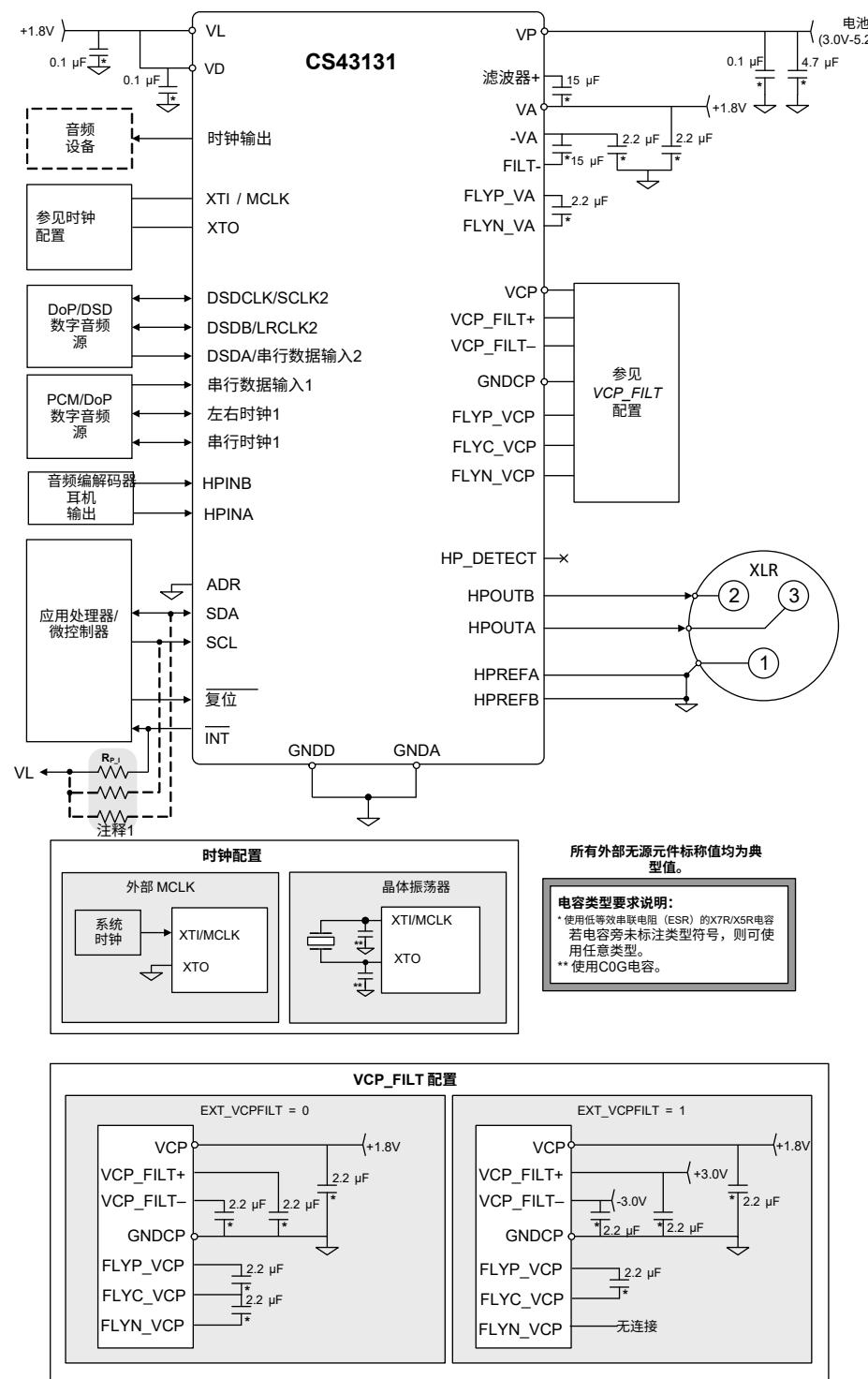


Figure 2-2. Typical Connection Diagram (Mono Mode)

Note:

1. The value for R_{P_I} can be determined by the interrupt pin specification in [Table 3-13](#).


图2-2。典型连接图（单声道模式）
注意：

 1. R_{P1} 的数值可根据表3-13中断引脚规格确定。

3 Characteristics and Specifications

Table 3-1 defines parameters as they are characterized in this section.

Table 3-1. Parameter Definitions

Parameter	Definition
Dynamic range	The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. A signal-to-noise ratio measurement over the specified bandwidth made with a -60-dB signal; 60 dB is added to resulting measurement to refer the measurement to full scale. This technique ensures that distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Dynamic range is expressed in decibel units.
Gain drift	The change in gain value with temperature, expressed in ppm/°C units.
Idle channel noise	The rms value of the signal with no input applied (properly back-terminated analog input, digital zero, or zero modulation input). Measured over the specified bandwidth.
Interchannel gain mismatch	The gain difference between left and right channel pairs. Interchannel gain mismatch is expressed in decibel units.
Interchannel phase mismatch	The phase difference between left and right channel pairs at 997-Hz sine wave input. Interchannel phase mismatch is expressed in degree units (with respect to 997-Hz sine wave input).
Interchannel isolation	A measure of cross talk between the left and right channel pairs. Interchannel isolation is measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Interchannel isolation is expressed in decibel units.
Load resistance and capacitance	The recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. The load capacitance effectively moves the band-limiting pole of the amp in the output stage. Increasing load capacitance beyond the recommended value can cause the internal op-amp to become unstable.
Output offset voltage	The DC offset voltage present at the amplifier's output when its input signal is in a mute state. The offset exists due to CMOS process limitations and is proportional to analog volume settings. When measuring the offset out of the headphone amplifier, the headphone amplifier is ON.
Total harmonic distortion + noise (THD+N)	The ratio of the rms sum of distortion and noise spectral components across the specified bandwidth (typically 20 Hz–20 kHz) relative to the rms value of the signal. THD+N is measured at -1 and -20 dBFS for the analog input and at 0 and -20 dB for the analog output, as suggested in AES17-1991 Annex A. THD+N is expressed in decibel units.
Turn-on time	Turn-on time is measured from when the PDN_HP = 0 ACK signal is received to when the signal appears on the HP output.

Table 3-2. Recommended Operating Conditions

Test conditions (unless otherwise specified): GNDD = GNDA = GNDP = 0 V, all voltages with respect to ground.

Parameters 1		Symbol	Minimum	Maximum	Units
DC power supply	Analog	VA	1.66	1.94	V
	Charge pump	VCP	1.66	1.94	V
	Filtered charge pump ² EXT_VCPFLT = 1	VCP_FILT+	2.85	3.15	V
		VCP_FILT-	-3.15	-2.85	V
	Battery supply HV_EN = 0, EXT_VCPFILT = 0 HV_EN = 1, EXT_VCPFILT = 0 EXT_VCPFILT = 1	VP	3.0	5.25	V
			3.3	5.25	V
			3.3	5.25	V
	Digital Interface	VL	1.66	1.94	V
	Digital Internal	VD	1.66	1.94	V
External voltage applied to pin 3,4	HP_DETECT pin VCP_FILT± domain pins ⁵ VL domain pins VA domain pins VP domain pins	V _{INHI} V _{VCPF} V _{VL} V _{VA} V _{VP}	-0.3 – VCP_FILT– -0.3 – VCP_FILT– -0.3 -0.3 -0.3	VP + 0.3 0.3 + VCP_FILT+ VL + 0.3 VA + 0.3 VP + 0.3	V V V V V
Ambient temperature		T _A	-20	+70	°C

1. Device functional operation is guaranteed within these limits. Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

2. If +1dB_EN = 1, the minimum VCP_FILT+ voltage becomes 3.0 V, and the maximum VCP_FILT– voltage becomes -3.0 V.

3. The maximum over/undervoltage is limited by the input current.

4. [Table 1-1](#) lists the power supply domain in which each CS43131 pin resides.

5. VCP_FILT± is specified in [Table 3-18](#).

3 特性与规格

表 3-1 定义了本节中所描述的参数。

表 3-1. 参数定义

参数	定义
动态范围	信号的均方根值与指定带宽内所有其他频谱成分均方根值之和的比值。在指定带宽内以-60 dB 信号进行的信噪比测量；测量结果加上 60 dB 以参考满量程。该技术确保失真成分低于噪声水平，不影响测量结果。该测量技术已被音频工程学会 (AES17-1991) 及日本电子工业协会 (EIAJ CP-307) 认可。动态范围以分贝单位表示。
增益漂移	增益值随温度变化的量，单位为 ppm/°C。
空闲通道噪声	无输入信号时的信号均方根值（模拟输入正确终端、数字零或零调制输入）。在指定带宽范围内测量。
通道间增益失配	左右声道对之间的增益差异。通道间增益失配以分贝为单位表示。
通道间相位失配	在997 Hz 正弦波输入下，左右声道对之间的相位差。通道间相位失配以度为单位表示（相对于997 Hz 正弦波输入）。
通道间隔离	衡量左右声道对之间串扰的指标。通道间隔离在转换器输出端测量，测试输入无信号，另一通道施加满量程信号。通道间隔离以分贝为单位表示。
负载电阻和电容	为确保内部运算放大器的稳定性和信号完整性，推荐的最小电阻和最大电容值。负载电容有效地移动输出级放大器的带限极点。负载电容超过推荐值可能导致内部运算放大器不稳定。
输出偏置电压	当放大器输入信号处于静音状态时，放大器输出端存在的直流偏移电压。该偏移电压因CMOS工艺限制而存在，且与模拟音量设置成正比。测量耳机放大器输出偏移时，耳机放大器处于开启状态。
总谐波失真加噪声 (THD+N)	在指定带宽（通常为20 Hz–20 kHz）内，失真和噪声频谱分量的均方根和与信号均方根值的比值。THD+N在模拟输入端以-1 dBFS和-20 dBFS测量，在模拟输出端以0 dB和-20 dB测量，符合AES17-1991附录A的建议。THD+N以分贝单位表示。
开启时间	开启时间是从接收到PDN_HP = 0确认信号到信号出现在耳机输出端的时间。

表 3-2. 推荐工作条件

测试条件（除非另有说明）：GNDD = GNDA = GNDGP = 0 V，所有电压均相对于接地。

参数 1		符号	最小值	最大值	单位
直流电源	模拟	VA	1.66	1.94	V
	电荷泵	VCP	1.66	1.94	V
	滤波电荷泵 ² EXT_VCPFLT = 1	VCP_FILT+	2.85	3.15	V
		VCP_FILT-	-3.15	-2.85	V
	电池电源 高压使能 = 0, EXT_VCPFILT = 0 高压使能 = 1, EXT_VCPFILT = 0 EXT_VCPFILT = 1	VP	3.0	5.25	V
			3.3	5.25	V
			3.3	5.25	V
	数字接口	VL	1.66	1.94	V
	数字内部	VD	1.66	1.94	V
外部电压 施加于引脚 3,4	HP_DETECT 引脚 VCP_FILT± 域引脚 ⁵ VL 域引脚 VA 域引脚 VP 域引脚	V _{INHI} V _{VCPF} V _{VL} V _{VA} V _{VP}	-0.3 – VCP_FILT- -0.3 – VCP_FILT- -0.3 -0.3 -0.3	VP + 0.3 0.3 + VCP_FILT+ VL + 0.3 VA + 0.3 VP + 0.3	V V V V V
环境温度		T _A	-20	+70	°C

- 设备功能性操作在此限制范围内得到保证。功能性在此限制范围之外不予保证或暗示。超出此限制范围的操作可能会对设备可靠性产生不利影响。
- 若 +1 dB_EN = 1，最小 VCP_FILT+ 电压为 3.0 V，最大 VCP_FILT- 电压为 -3.0 V。
- 最大过压/欠压由输入电流限制。
- 表 1-1 列出了每个 CS43131 引脚所在的电源域。
- VCP_FILT± 的规格见表 3-18。

Table 3-3. Absolute Maximum Ratings

Test conditions (unless otherwise specified): GNDD = GNDA = GNDP = 0 V; all voltages with respect to ground.

Parameters		Symbol	Minimum	Maximum	Units
DC power supply	Analog	VA	-0.3	2.33	V
	Battery	VP	-0.3	6.3	V
	Charge pump	VCP	-0.3	2.33	V
	Filtered charge pump (positive)	VCP_FILT+	-0.3	3.3	V
	Filtered charge pump (negative)	VCP_FILT-	-3.3	0.3	V
	Digital interface	VL	-0.3	2.33	V
	Digital internal	VD	-0.3	2.33	V
	Input current 1	I _{in}	—	±10	mA
	Ambient operating temperature (power applied)	T _A	-50	+115	°C
	Storage temperature	T _{stg}	-65	+150	°C

Caution: Stresses beyond “Absolute Maximum Ratings” levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Table 3-2, “Recommended Operating Conditions”](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Any pin except supplies and HPINx. Transient currents of up to ±100 mA on the analog input pins do not cause SCR latch-up.

Table 3-4. Analog Output Characteristics (HV_EN = 1)

Test conditions (unless otherwise specified): [Fig. 2-1](#) shows CS43131 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDP = GNDD = 0 V; voltages are with respect to ground; HV_EN = 1; ASP_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; TA = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP_SPRATE = 0001 (LRCK = 44.1-kHz mode); PDN_XTAL = 0, MCLK_INT = 1, PLUS_1DB = 0, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz); Volume = 0 dB; when testing in DSD processor mode, DSD_ZERODB = 1; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on HPRFX.

PCM and DSD Processor Mode Parameter 2,3,4			Minimum	Typical	Maximum	Units	
HPOUTx R _L = 10 kΩ C _L = 200 pF OUT_FS = 11 Volume = 0 dB +1dB_EN = 0.5 unless otherwise specified	Dynamic range (defined in Table 3-1)	24-bit, 32-bit, DSD 16-bit	A-weighted Unweighted	124 121	130 127	— —	dB dB
	THD+N (defined in Table 3-1)	24-bit, 32-bit 16-bit	0 dB -20 dB -60 dB 0 dB -20 dB -60 dB 0 dB -20 dB -60 dB	— — — — — — — — —	-115 -97 -67 -94 -74 -34 -108 -97 -67	-109 — -61 -88 — -28 -101 — -61	dB dB dB dB dB dB dB dB dB
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit, DSD	—	0.55	—	μV	
	Full-scale output voltage		4.66	4.90	5.14	Vpp	
	Interchannel isolation 6 (defined in Table 3-1)	217 Hz 1 kHz 20 kHz	— — —	120 120 100	— — —	dB dB dB	
	THD+N (defined in Table 3-1)	24-bit, 32-bit, DSD	0 dB	—	-105	dB	
	Full-scale output voltage		5.42	5.70	5.99	Vpp	

表 3-3. 绝对最大额定值

测试条件 (除非另有说明) : GNDD = GNDA = GNDGP = 0 V; 所有电压均相对于接地。

参数	符号	最小值	最大值	单位
直流电源	模拟 电池	VA VP	-0.3 -0.3	2.33 6.3
	电荷泵	VCP	-0.3	2.33
	滤波电荷泵 (正极)	VCP_FILT+	-0.3	3.3
	滤波电荷泵 (负极)	VCP_FILT-	-3.3	0.3
	数字接口	VL	-0.3	2.33
	数字内部	VD	-0.3	2.33
				V
				mA
输入电流 1	I _{in}	—	±10	
环境工作温度 (加电状态)	T _A	-50	+115	°C
存储温度	T _{stg}	-65	+150	°C

注意: 超过“绝对最大额定值”水平的应力可能会对器件造成永久性损坏。这些水平仅为应力额定值, 器件在表 3-2“推荐工作条件”中所示条件之外的任何条件下的功能性操作并不保证。长时间暴露于绝对最大额定值条件可能影响器件的可靠性。

1. 除电源和HPINx引脚外的任何引脚。模拟输入引脚上的瞬态电流高达±100 mA不会引起SCR锁定。

表 3-4. 模拟输出特性 (高压使能 = 1)

测试条件 (除非另有说明) : 图 2-1 显示了 CS43131 的连接; 输入测试信号为 32 位满量程 997 Hz 正弦波 (除非另有说明); GNDA = GNDGP = GNDD = 0 V; 电压均相对于接地; 高压使能 = 1; ASP_M/Sb = 1; 典型、最小/最大性能数据采集条件为 VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; 环境温度 TA = +25°C; 测量带宽为 20 Hz–20 kHz; ASP_SPRATE = 0001 (LRCK = 44.1 kHz 模式); PDN_XTAL = 0, MCLK_INT = 1, PL_US_1DB = 0, 且 MCLK_SRC_SEL = 00 (晶体频率 f_{XTAL} = 22.5792 MHz); 音量 = 0 dB; 在 DSD 处理器模式测试时, DSD_ZERO DB = 1; 测试噪声相关规格 (动态范围、THD+N、空闲通道噪声) 时, HPREFx 无外部阻抗。

PCM 和 DSD 处理器模式参数 2,3,4			最小值	典型	最大值	单位
HPOUTx R _L = 10 kΩ C _L = 200 pF OUT_FS = 11 音量 = 0 dB +1dB_EN = 0, 5 除非另有说明	动态范围 (定义见表 3-1)	24 位, 32 位, DSD 16 位	A 加权 非加权 A 加权 非加权	124 121 91 88	130 127 97 94	— — — —
	THD+N (定义见表 3-1)	24 位, 32 位 16 位	0 dB -20 dB -60 dB 0 dB -20 dB -60 dB 0 dB -20 dB -60 dB	— — — — — — — — —	-115 -97 -67 -94 -74 -34 -108 -97 -67	-109 — -61 -88 — -28 -101 — -61
	空闲通道噪声 (A 加权) (定义见表 3-1)	24 位, 32 位, DSD	—	0.55	—	μV
	满量程输出电压		4.66	4.90	5.14	Vpp
	通道间隔离 6 (定义见表 3-1)	217 Hz 1 kHz 20 kHz	— — —	120 120 100	— — —	dB dB dB
	THD+N (定义见表 3-1)	24 位, 32 位, DSD 0 dB	—	-105	—	dB
	满量程输出电压		5.42	5.70	5.99	Vpp

Table 3-4. Analog Output Characteristics (HV_EN = 1) 1 (Cont.)

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43131 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDP = GNDD = 0 V; voltages are with respect to ground; HV_EN = 1; ASP_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; TA = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP_SPRATE = 0001 (LRCK = 44.1-kHz mode); PDN_XTAL = 0, MCLK_INT = 1, PLUS_1DB = 0, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz); Volume = 0 dB; when testing in DSD processor mode, DSD_ZERODB = 1; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on HPREFx.

PCM and DSD Processor Mode Parameter 2,3,4			Minimum	Typical	Maximum	Units
HPOUTx RL = 600 Ω CL = 200 pF OUT_FS = 11 Volume = 0 dB +1dB_EN = 0, unless otherwise specified	Dynamic range (defined in Table 3-1)	24-bit, 32-bit, DSD 16-bit	A-weighted Unweighted A-weighted Unweighted	124 121 91 88	130 127 97 94	— — — —
	THD+N (defined in Table 3-1)	24-bit, 32-bit 16-bit DSD	0 dB -20 dB -60 dB 0 dB -20 dB -60 dB 0 dB -20 dB -60 dB	— — — — — — — — —	-115 -97 -67 -94 -74 -34 -108 -97 -67	-109 — -61 -88 — -28 -101 — -61
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit, DSD	—	0.55	—	μV
	Full-scale output voltage	—	4.66	4.90	5.14	Vpp
	Output power	—	—	5	—	mW
	Interchannel isolation (defined in Table 3-1)	217 Hz 1 kHz 20 kHz	— — —	120 120 100	— — —	dB dB dB
	THD+N (defined in Table 3-1)	24-bit, 32-bit, DSD	0 dB	—	-105	—
	Full-scale output voltage	—	5.42	5.70	5.99	Vpp
	Output power	—	—	6.8	—	mW
Other characteristics for HPOUTx	Interchannel gain mismatch (defined in Table 3-1)	—	±0.1	—	—	dB
	Interchannel phase mismatch (defined in Table 3-1)	—	—	±0.01	—	°
	Output offset voltage: Mute (defined in Table 3-1)	—	±50	±100	—	μV
	Gain drift (defined in Table 3-1)	—	±100	—	—	ppm/°C
	Load resistance (RL)	600	—	—	—	Ω
	Load capacitance (CL)	—	—	1	—	nF
	Turn-on time (defined in Table 3-1)	—	—	12	—	ms
Click/pop during PDN_HP enable or disable		A-weighted	—	±50	±100	μV

1. This table also applies to external VCP_FILT supply mode: CS43131 power up procedure is per description in Section 5.13.1; EXT_VCPFILT = 1; VCP_FILT+ and VCP_FILT- comply to Table 3-2 when EXT_VCPFILT = 1; in this mode, HV_EN must be set to 1.

2. One LSB of triangular PDF dither is added to PCM data.

3. Referred to the typical full-scale voltage. Applies to all THD+N and dynamic range values in the table.

4. DSD performance may be limited by the source recording. 0 dB-SACD = 50% modulation index.

5. The volume must be configured as indicated to achieve specified output characteristics.

表 3-4. 模拟输出特性 (HV_EN = 1) 1 (续)

测试条件 (除非另有说明) : 图 2-1 显示了 CS43131 的连接; 输入测试信号为 32 位满量程 997 Hz 正弦波 (除非另有说明); GNDA = GNDGP = GNDD = 0 V; 电压均相对于接地; 高压使能 = 1; ASP_M/Sb = 1; 典型、最小/最大性能数据采集条件为 VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; 环境温度 TA = +25°C; 测量带宽为 20 Hz–20 kHz; ASP_SPRATE = 0001 (LRCK = 44.1 kHz 模式); PDN_XTAL = 0, MCLK_INT = 1, PL_US_1DB = 0, 且 MCLK_SRC_SEL = 00 (晶体频率 f_XTAL = 22.5792 MHz); 音量 = 0 dB; 在 DSD 处理器模式测试时, DSD_ZERO DB = 1; 测试噪声相关规格 (动态范围、THD+N、空闲通道噪声) 时, HPREFx 无外部阻抗。

PCM 和 DSD 处理器模式参数 2,3,4			最小值	典型	最大值	单位
HPOUTx RL = 600 Ω CL = 200 pF OUT_FS = 11 音量 = 0 dB +1dB_EN = 0, 除非另有 说明	动态范围 (定义见表 3-1)	24 位, 32 位, DSD 16 位	A 加权 非加权 A 加权 非加权	124 121 91 88	130 127 97 94	— — — —
	THD+N (定义见表 3-1)	24 位, 32 位 16 位	0 dB -20 dB -60 dB 0 dB -20 dB -60 dB 0 dB -20 dB -60 dB	— — — — — — — — —	-115 -97 -67 -94 -74 -34 -108 -97 -67	-109 — -61 -88 — -28 -101 — -61
	空闲通道噪声 (A 加权) (定义见表 3-1)	24 位, 32 位, DSD		—	0.55	—
	满量程输出电压			4.66	4.90	5.14
	输出功率			—	5	—
	通道间隔离 (定义见表 3-1)		217 Hz 1 kHz 20 kHz	— — —	120 120 100	— — —
	THD+N (定义见表 3-1)	24 位, 32 位, DSD	0 dB	—	-105	—
	满量程输出电压			5.42	5.70	5.99
	输出功率			—	6.8	—
	的其他特性	通道间增益失配 (定义见表 3-1) 通道间相位失配 (定义见表 3-1) 输出偏置电压: 静音 (定义见表 3-1) 增益漂移 (定义见表 3-1) 负载电阻 (RL) 负载电容 (CL) 开启时间 (定义见表 3-1) PDN_HP 使能或禁用期间的点击/爆音	A 加权	— — — — 600 — — —	±0.1 — ±50 ±100 — — — ±50	— ±0.01 ±100 — — 1 12 ±100

1. 本表同样适用于外部 VCP_FILT 供电模式: CS43131 的上电流程详见第 5.13.1 节; EXT_VCPFILT = 1;

当 EXT_VCPFILT = 1 时, VCP_FILT+ 和 VCP_FILT- 符合表 3-2 的要求; 在此模式下, HV_EN 必须设置为 1。

2. 在 PCM 数据中加入了一个最低有效位的三角形概率密度函数抖动。

3. 参考典型满量程电压。适用于表中所有 THD+N 和 动态范围 数值。

4. DSD 性能可能受限于源录音。0 dB-SACD = 50% 调制指数。

5. 必须按指示配置音量以实现规定的输出特性。

6. Output test configuration. Symbolized component values are specified in the test conditions.

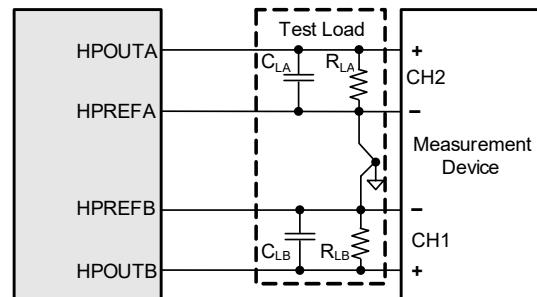


Table 3-5. Analog Output Characteristics (HV_EN = 0) 1

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43131 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDGP = GNDD = 0 V; voltages are with respect to ground; HV_EN = 0; ASP_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; TA = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP_SPRATE = 0001 (LRCK = 44.1-kHz mode); PDN_XTAL = 0, MCLK_INT = 1, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz); Volume = 0 dB; when testing in DSD processor mode, DSD_ZERODB = 1; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on HPREFx.

PCM and DSD Processor Mode Parameter 2,3,4			Minimum	Typical	Maximum	Units
HPOUTx; R _L = 10 kΩ C _L = 200 pF OUT_FS = 10 Volume = 0 dB, ⁵ unless otherwise specified	Dynamic range (defined in Table 3-1)	24-bit, 32-bit, DSD 16-bit	A-weighted Unweighted	122 119	128 125	— —
	THD+N (defined in Table 3-1)	24-bit, 32-bit 16-bit	0 dB -20 dB -60 dB 0 dB -20 dB -60 dB 0 dB -20 dB -60 dB	— — — — — — — — —	-113 -95 -65 -94 -74 -34 -109 -95 -65	-107 — -59 -88 — -28 -103 — -59
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit, DSD	—	0.55	—	μV
	Full-scale output voltage		3.76	3.96	4.16	Vpp
	Interchannel isolation ⁶ (defined in Table 3-1)	217 Hz 1 kHz 20 kHz	— — —	120 120 100	— — —	dB dB dB
	Dynamic range (defined in Table 3-1)	24-bit, 32-bit, DSD 16-bit	A-weighted Unweighted	122 119	128 125	— —
	THD+N (defined in Table 3-1)	24-bit, 32-bit 16-bit	0 dB -20 dB -60 dB 0 dB -20 dB -60 dB 0 dB -20 dB -60 dB	— — — — — — — — —	-113 -95 -65 -94 -74 -34 -109 -95 -65	-107 — -59 -88 — -28 -103 — -59
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit, DSD	—	0.55	—	μV
	Full-scale output voltage		3.76	3.96	4.16	Vpp
	Output power		—	3.3	—	mW
	Interchannel isolation ⁶ (defined in Table 3-1)	217 Hz 1 kHz 20 kHz	— — —	120 120 100	— — —	dB dB dB

6. 输出测试配置。符号化元件值在测试条件下指定。

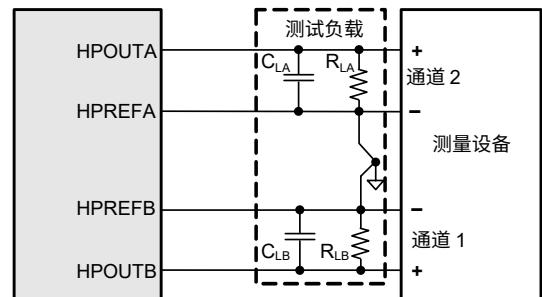


表 3-5. 模拟输出特性 (高压使能 = 0) 1

测试条件 (除非另有说明) : 图 2-1 显示了 CS43131 的连接; 输入测试信号为 32 位满量程 997 Hz 正弦波 (除非另有说明); GNDA = GNDGP = GNDD = 0 V; 电压相对于接地; 高压使能 = 0; ASP_M/Sb = 1; 典型、最小/最大性能数据采集条件为 VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; 环境温度 TA = +25°C; 测量带宽为 20 Hz~20 kHz; ASP_SPRATE = 0001 (LRCK = 44.1 kHz模式); PDN_XTAL = 0, MCLK_INT = 1, 且 MCLK_SRC_SEL = 00 (晶体频率 f_XTAL = 22.5792 MHz); 音量 = 0 dB; 在DSD处理器模式测试时, DSD_ZEROORB = 1; 测试噪声相关规格 (动态范围、THD+N、空闲通道噪声) 时, HPREFx无外部阻抗。

PCM和DSD处理器模式参数 2,3,4			最小值	典型	最大值	单位
耳机输出端口 HPOUTx; RL = 10 kΩ CL = 200 pF 输出采样率 OUT_FS = 10 音量 = 0 dB, 除非另有说明	动态范围 (定义见表 3-1) 24 位, 32 位, DSD 16 位	A 加权 非加权 A 加权 非加权	122 119 91 88	128 125 97 94	— — — —	dB dB dB dB
	THD+N (定义见表 3-1) 24 位, 32 位 16 位	0 dB -20 dB -60 dB 0 dB -20 dB -60 dB 0 dB -20 dB -60 dB	— — — — — — — — —	-113 -95 -65 -94 -74 -34 -109 -95 -65	-107 — -59 -88 — -28 -103 — -59	dB dB dB dB dB dB dB dB dB
	DSD	0 dB -20 dB -60 dB	— — —	— — —	— — —	dB dB dB
	空闲通道噪声 (A 加权) (定义见表 3-1)	24 位, 32 位, DSD	—	0.55	—	μV
	满量程输出电压		3.76	3.96	4.16	Vpp
	通道间隔离 6 (定义见表 3-1)	217 Hz 1 kHz 20 kHz	— — —	120 120 100	— — —	dB dB dB
耳机输出端口 HPOUTx; RL = 600 Ω CL = 200 pF OUT_FS = 10 音量 = 0 dB, 除非另有说明	动态范围 (定义见表 3-1) 24 位, 32 位, DSD 16 位	A 加权 非加权 A 加权 非加权	122 119 91 88	128 125 97 94	— — — —	dB dB dB dB
	THD+N (定义见表 3-1) 24 位, 32 位 16 位	0 dB -20 dB -60 dB 0 dB -20 dB -60 dB 0 dB -20 dB -60 dB	— — — — — — — — —	-113 -95 -65 -94 -74 -34 -109 -95 -65	-107 — -59 -88 — -28 -103 — -59	dB dB dB dB dB dB dB dB dB
	DSD	0 dB -20 dB -60 dB	— — —	— — —	— — —	dB dB dB
	空闲通道噪声 (A 加权) (定义见表 3-1)	24 位, 32 位, DSD	—	0.55	—	μV
	满量程输出电压		3.76	3.96	4.16	Vpp
	输出功率		—	3.3	—	mW
	通道间隔离 6 (定义见表 3-1)	217 Hz 1 kHz 20 kHz	— — —	120 120 100	— — —	dB dB dB

Table 3-5. Analog Output Characteristics (HV_EN = 0) 1 (Cont.)

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43131 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDGP = GNDD = 0 V; voltages are with respect to ground; HV_EN = 0; ASP_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; TA = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP_SPRATE = 0001 (LRCK = 44.1-kHz mode); PDN_XTAL = 0, MCLK_INT = 1, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz); Volume = 0 dB; when testing in DSD processor mode, DSD_ZERO DB = 1; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on HPREFX.

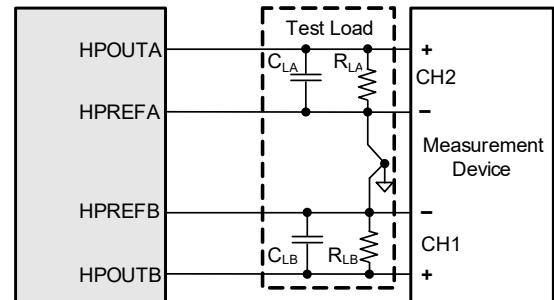
PCM and DSD Processor Mode Parameter 2,3,4			Minimum	Typical	Maximum	Units
HPOUTx; R _L = 32 Ω C _L = 200 pF OUT_FS = 01 Volume = 0 dB, unless otherwise specified	Dynamic range (defined in Table 3-1)	24-bit, 32-bit, DSD 16-bit	A-weighted Unweighted A-weighted Unweighted	119 116 91 88	125 122 97 94	— — — —
	THD+N (defined in Table 3-1)	24-bit, 32-bit 16-bit DSD	0 dB -20 dB -60 dB 0 dB -20 dB -60 dB 0 dB -20 dB -60 dB	— — — — — — — — —	-110 -92 -62 -94 -74 -34 -106 -92 -62	-104 — -56 -88 — -28 -96 — -56
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit, DSD	—	0.55	—	μV
	Full-scale output voltage		2.68	2.81	2.96	Vpp
	Output power		—	30.8	—	mW
	Interchannel isolation ⁶ (defined in Table 3-1)		217 Hz 1 kHz 20 kHz	— — —	110 105 90	— — —
	Dynamic range (defined in Table 3-1)	24-bit, 32-bit 16-bit	A-weighted Unweighted A-weighted Unweighted	113 110 89 86	119 116 95 92	— — — —
	THD+N (defined in Table 3-1)	24-bit, 32-bit 16-bit DSD	0 dB -20 dB -60 dB 0 dB -20 dB -60 dB 0 dB -20 dB -60 dB	— — — — — — — — —	-100 -86 -56 -94 -74 -34 -100 -86 -56	-94 — -50 -88 — -28 -94 — -50
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit, DSD	—	0.55	—	μV
	Full-scale output voltage		1.34	1.41	1.48	Vpp
Other characteristics for HPOUTx	Output power		—	15.6	—	mW
	Interchannel isolation ⁶ (defined in Table 3-1)		217 Hz 1 kHz 20 kHz	— — —	105 100 85	— — —
	Interchannel gain mismatch (defined in Table 3-1)		—	±0.1	—	dB
	Interchannel phase mismatch (defined in Table 3-1)		—	—	±0.01	°
	Output offset voltage: Mute (defined in Table 3-1)		—	±50	±100	μV
	Gain drift (defined in Table 3-1)		—	±100	—	ppm/°C
	Load resistance (R _L)		16	—	—	Ω
	Load capacitance (C _L)		—	—	1	nF
	Turn-on time (defined in Table 3-1)		—	—	12	ms
Audio latency after RESET released ⁷			—	—	22	ms
Click/pop during PDN_HP enable or disable			A-weighted	—	±50	±100
						μV

表 3-5. 模拟输出特性 (高压使能 = 0) 1 (续)

测试条件 (除非另有说明) : 图 2-1 显示了 CS43131 的连接; 输入测试信号为 32 位满量程 997 Hz 正弦波 (除非另有说明); GNDA = GNDGP = GNDD = 0 V; 电压相对于接地; 高压使能 = 0; ASP_M/Sb = 1; 典型、最小/最大性能数据采集条件为 VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; 环境温度 TA = +25°C; 测量带宽为 20 Hz–20 kHz; ASP_SPRATE = 0001 (LRCK = 44.1 kHz模式); PDN_XTAL = 0, MCLK_INT = 1, 且 MCLK_SRC_SEL = 00 (晶体频率 fXTAL = 22.5792 MHz); 音量 = 0 dB; 在DSD处理器模式测试时, DSD_ZERO DB = 1; 测试噪声相关规格 (动态范围、THD+N、空闲通道噪声) 时, HPREFx无外部阻抗。

PCM和DSD处理器模式参数 2,3,4			最小值	典型	最大值	单位
耳机输出端口 HPOUTx; RL = 32 Ω CL = 200 pF OUT_FS = 01 音量 = 0 dB, 除非另有说明	动态范围 (定义见表 3-1)	24 位, 32 位, DSD 16 位	A 加权 非加权 A 加权 非加权	119 116 91 88	125 122 97 94	— — — —
	THD+N (定义见表 3-1)	24 位, 32 位 16 位	0 dB -20 dB -60 dB 0 dB -20 dB -60 dB 0 dB -20 dB -60 dB	— — — — — — — — —	-110 -92 -62 -94 -74 -34 -106 -92 -62	-104 — —56 -88 — -28 —96 — -56
	空闲通道噪声 (A 加权) (定义见表 3-1)	24 位, 32 位, DSD		—	0.55	—
	满量程输出电压			2.68	2.81	2.96
	输出功率			—	30.8	—
	通道间隔离 ⁶ (定义见表 3-1)		217 Hz 1 kHz 20 kHz	— — —	110 105 90	— — —
	动态范围 (定义见表 3-1)	24 位, 32 位 16 位	A 加权 非加权 A 加权 非加权	113 110 89 86	119 116 95 92	— — — —
	THD+N (定义见表 3-1)	24 位, 32 位 16 位	0 dB -20 dB -60 dB 0 dB -20 dB -60 dB 0 dB -20 dB -60 dB	— — — — — — — — —	-100 -86 -56 -94 -74 -34 -100 -86 -56	-94 — —50 -88 — -28 —94 — -50
	空闲通道噪声 (A 加权) (定义见表 3-1)	24 位, 32 位, DSD		—	0.55	—
	满量程输出电压			1.34	1.41	1.48
HPOUTx 的其他特性	输出功率			—	15.6	—
	通道间隔离 ⁶ (定义见表 3-1)		217 Hz 1 kHz 20 kHz	— — —	105 100 85	— — —
	通道间增益失配 (定义见表 3-1)			—	±0.1	—
	通道间相位失配 (定义见表 3-1)			—	—	±0.01
	输出偏置电压: 静音 (定义见表 3-1)			—	±50	±100
	增益漂移 (定义见表 3-1)			—	±100	—
	负载电阻 (RL)			16	—	—
	负载电容 (CL)			—	—	1 nF
	开启时间 (定义见表 3-1)			—	—	12 毫秒
	复位释放后音频延迟 ⁷			—	—	22 毫秒
	PDN_HP使能或禁用期间的点击/爆音	A 加权	—	±50	±100	μV

1. This table also applies to external VCP_FILT supply mode: CS43131 power up procedure as described in Section 4.3.5; EXT_VCPFILT=1; VCP_FILT+ and VCP_FILT- comply to [Table 3-2](#) when EXT_VCPFILT = 1; in this mode, HV_EN must be set to 1.
2. One LSB of triangular PDF dither is added to PCM data.
3. Referred to the typical full-scale voltage. Applies to all THD+N and dynamic range values in the table.
4. DSD performance may be limited by the source recording. 0 dB-SACD = 50% modulation index.
5. The volume must be configured as indicated to achieve specified output characteristics.
6. HP output test configuration. Symbolized component values are specified in the test conditions.



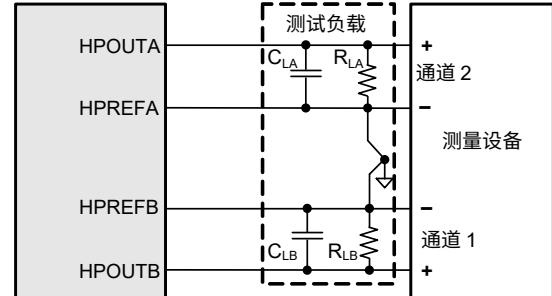
7. With I²C normal speed mode and 22.5792-MHz XTAL used as MCLK source, this specification is measured from reset released to when the audio signal appears on the output per power-up sequence listed in [Section 5.13.1](#). PCM_SZC should be set to Immediate (PCM_SZC = 00) to hear audio at 20 ms after startup.

Table 3-6. Wideband Flatness Mode Analog Output Characteristics 1

Test conditions (unless otherwise specified): [Fig. 2-1](#) shows CS43131 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; ASP_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; TA = +25°C; measurement bandwidth is 20 Hz–90 kHz; ASP_SPRATE = 0110 (LRCK = 192-kHz mode); PDN_XTAL = 0, MCLK_INT = 1, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz); Volume = 0 dB; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on HPREFx.

Wideband Flatness Mode Parameter 2,3			Minimum	Typical	Maximum	Units	
HPOUTx R _L = 600 Ω C _L = 200 pF OUT_FS = 11 Volume = 0 dB +1dB_EN = 0 HV_EN = 1, unless otherwise specified	Dynamic range (defined in Table 3-1)	24-bit, 32-bit	A-weighted	122	128	—	dB
	THD+N (20 Hz–20 kHz, defined in Table 3-1)	24-bit, 32-bit	0 dB -20 dB -60 dB	— — —	-112 -97 -67	-106 — -61	dB dB dB
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit	—	0.69	—	μV	
	Full-scale output voltage		4.66	4.90	5.14	Vpp	
	Output power		—	5	—	mW	
	Interchannel isolation (defined in Table 3-1)	217 Hz 1 kHz 20 kHz	— — —	120 120 110	— — —	dB dB dB	
	THD+N (20 Hz–20 kHz, defined in Table 3-1)	0 dB	—	-105	-99	dB	
HPOUTx R _L = 600 Ω C _L = 200 pF OUT_FS = 11 Volume = 0 dB +1dB_EN = 1 HV_EN = 1, unless otherwise specified	Full-scale output voltage		5.42	5.7	5.99	Vpp	
	Output power		—	6.8	—	mW	

1. 本表同样适用于外部 VCP_FILT 供电模式：CS43131 上电流程详见第 4.3.5 节；EXT_VCPFILT=1；VCP_FILT+ 和 VCP_FILT- 符合表 3-2 当 EXT_VCPFILT = 1 时；在此模式下，HV_EN 必须设置为 1。
2. 在 PCM 数据中加入了一个最低有效位的三角形概率密度函数抖动。
3. 参考典型满量程电压。适用于表中所有 THD+N 和 动态范围数值。
4. DSD 性能可能受限于源录音。0 dB-SACD = 50% 调制指数。
5. 必须按指示配置音量以实现规定的输出特性。
6. 耳机输出测试配置。符号化元件值在测试条件下指定。



7. 使用 I²C 正常速率模式及 22.5792 MHz 晶体振荡器作为 MCLK 源时，本规格从复位释放到音频信号根据第 5.13.1 节列出的上电序列出现在输出端进行测量。PCM_SZC 应设置为即时 (PCM_SZC = 00)，以便在启动后 20 毫秒听到音频。

表 3-6. 宽带平坦模式模拟输出特性 1

测试条件（除非另有说明）：图 2-1 显示了 CS43131 的连接；输入测试信号为 32 位满量程 997 Hz 正弦波（非特别说明除外）；GNDA = GNDGP = GNDD = 0 V；电压均相对于接地；ASP_M/Sb = 1；典型、最小/最大性能数据采集条件为 VA = VCP = 1.8 V；VL = VD = 1.8 V；VP = 3.6 V；环境温度 TA = +25°C；测量带宽为 20 Hz–90 kHz；ASP_SPRATE = 0110 (LRCK = 192 kHz 模式)；PDN_XTAL = 0, MCLK_INT = 1, 且 MCLK_SRC_SEL = 00 (晶体频率 f_{XTAL} = 22.5792 MHz)；音量 = 0 dB；测试噪声相关规格（动态范围、THD+N、空闲通道噪声）时，HPREFx 无外部阻抗。

宽带平坦模式参数 2,3			最小值	典型	最大值	单位
HPOUTx R _L = 600 Ω C _L = 200 pF OUT_FS = 11 音量 = 0 dB +1dB_EN = 0 高压使能 = 1, 除非另有说明	动态范围 24 位, 32 位 (定义见表 3-1)	A 加权	122	128	—	dB
	THD+N (20 Hz–20 kHz) 24 位, 32 位 , 定义见表 3-1)	0 dB -20 dB -60 dB	— — —	-112 -97 -67	-106 — -61	dB dB dB
	空闲通道噪声 24 位, 32 位 (A 加权) (定义见表 3-1)		—	0.69	—	μV
	满量程输出电压		4.66	4.90	5.14	Vpp
	输出功率		—	5	—	mW
	通道间隔离 (定义见表 3-1)	217 Hz 1 kHz 20 kHz	— — —	120 120 110	— — —	dB dB dB
HPOUTx R _L = 600 Ω C _L = 200 pF OUT_FS = 11 音量 = 0 dB +1dB_EN = 1 高压使能 = 1, 除非另有说明	THD+N (20 Hz–20 kHz) 24 位, 32 位 , 定义见表 3-1)	0 dB	—	-105	-99	dB
	满量程输出电压		5.42	5.7	5.99	Vpp
	输出功率		—	6.8	—	mW

Table 3-6. Wideband Flatness Mode Analog Output Characteristics 1 (Cont.)

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43131 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDGP = GNDD = 0 V; voltages are with respect to ground; ASP_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; TA = +25°C; measurement bandwidth is 20 Hz–90 kHz; ASP_SPRATE = 0110 (LRCK = 192-kHz mode); PDN_XTAL = 0, MCLK_INT = 1, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz); Volume = 0 dB; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on HPREFx.

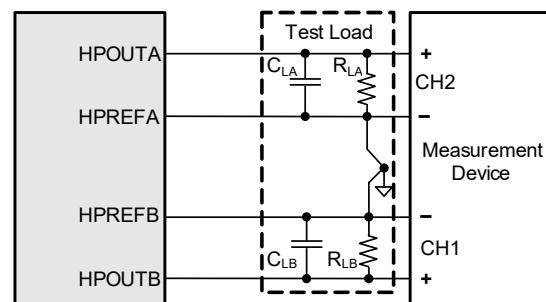
Wideband Flatness Mode Parameter 2,3			Minimum	Typical	Maximum	Units
HPOUTx; $R_L = 32 \Omega$ $C_L = 200 \text{ pF}$ OUT_FS = 01 Volume = 0 dB HV_EN = 0, unless otherwise specified	Dynamic range (defined in Table 3-1)	24-bit, 32-bit A-weighted	117	123	—	dB
	Dynamic range (MCLK = 19.2 MHz, MCLK_SRC_SEL = 01, MCLK_INT = 1)	24-bit, 32-bit (DRE_EN = 1) Unweighted	115 88	121 94	—	dB
		24-bit, 32-bit (DRE_EN = 0) A-weighted	94	100	—	dB
		24-bit, 32-bit (DRE_EN = 0) Unweighted	64	70	—	dB
	THD+N (20 Hz–20 kHz, defined in Table 3-1)	24-bit, 32-bit 0 dB -20 dB -60 dB	— — —	-110 -92 -62	-104 — -56	dB
	THD+N (20 Hz–90 kHz, defined in Table 3-1)	24-bit, 32-bit 0 dB -20 dB -60 dB	— — —	-89 -78 -38	-83 — -32	dB
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit	—	0.69	—	μV
	Full-scale output voltage		2.68	2.81	2.96	Vpp
	Output power		—	30.8	—	mW
	Interchannel isolation 4 (defined in Table 3-1)	217 Hz 1 kHz 20 kHz	— — —	110 105 90	—	dB
Other characteristics for HPOUTx	Interchannel gain mismatch (defined in Table 3-1)		—	±0.1	—	dB
	Interchannel phase mismatch (defined in Table 3-1)		—	—	±0.01	°
	Output offset voltage: Mute (defined in Table 3-1)		—	±50	±100	μV
	Gain drift (defined in Table 3-1)		—	±100	—	ppm/°C
	Load resistance (R_L)		6	—	—	Ω
	Load capacitance (C_L)		—	—	1	nF
	Turn-on time (defined in Table 3-1)		—	—	12	ms
Click/pop during PDN_HP enable or disable		A-weighted	—	±50	±100	μV

1. This table also applies to external VCP_FILT supply mode: CS43131 power up procedure is per description in Section 5.13.1; EXT_VCPFILT = 1; VCP_FILT+ and VCP_FILT- comply to Table 3-2 when EXT_VCPFILT = 1; in this mode, HV_EN must be set to 1.

2. One LSB of triangular PDF dither is added to PCM data.

3. Referred to the typical full-scale voltage. Applies to all THD+N and dynamic range values in the table.

4. HP output test configuration. Symbolized component values are specified in the test conditions.


Table 3-7. Headphone Load Measurement

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43131 connections; GNDD = GNDGP = GNDA = 0 V; voltages are with respect to ground; typical performance data taken with VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; min/max performance data taken with VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; TA = +25°C. MCLK_INT = 1, PDN_XTAL = 0, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz).

Parameters	Symbol	Minimum	Typical	Maximum	Units
Frequency range	—	20	—	20k	Hz
Frequency resolution	—	—	5.94	—	Hz

表 3-6. 宽带平坦模式模拟输出特性 1 (续)

测试条件 (除非另有说明) : 图 2-1 显示了 CS43131 的连接; 输入测试信号为 32 位满量程 997 Hz 正弦波 (非特别说明除外); GNDA = GNDGP = GNDD = 0 V; 电压均相对于接地; ASP_M/Sb = 1; 典型、最小V最大性能数据采集条件为 VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; 环境温度 TA = +25°C; 测量带宽为 20 Hz–90 kHz; ASP_SPRATE = 0110 (LRCK = 192 kHz 模式); PDN_XTAL = 0, MCLK_INT = 1, 且 MCLK_SRC_SEL = 00 (晶体频率 fXTAL = 22.5792 MHz); 音量 = 0 dB; 测试噪声相关规格 (动态范围、THD+N、空闲通道噪声) 时, HPREFx 无外部阻抗。

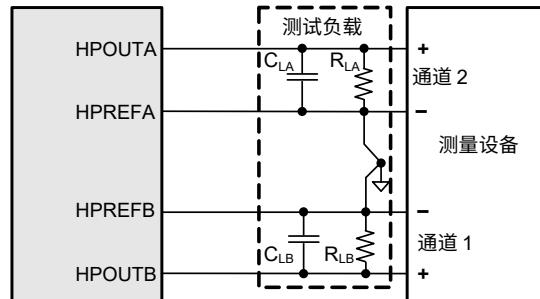
宽带平坦模式参数 2,3			最小值	典型	最大值	单位
耳机输出端口 HPOUTx; RL = 32 Ω CL = 200 pF OU T_FS = 01 音量 = 0 dB 高压使能 = 0, 除非另有说明	动态范围 (定义见表 3-1)	24 位, 32 位 A 加权	117	123	—	dB
	动态范围 (MCLK = 19.2 MHz, MCLK_SRC_SEL = 01, 24 位, 32 位 (DRE_EN = 0) MCLK_INT = 1)	24 位, 32 位 (DRE_EN = 1) A 加权 非加权 A 加权 非加权	115 88 94 64	121 94 100 70	— — — —	dB dB dB dB
	THD+N (20 Hz–20 kHz , 定义见表 3-1)	24 位, 32 位 0 dB -20 dB -60 dB	— — —	-110 -92 -62	-104 — -56	dB dB dB
	THD+N (20 Hz–90 kHz , 定义见表 3-1)	24 位, 32 位 0 dB -20 dB -60 dB	— — —	-89 -78 -38	-83 — -32	dB dB dB
	空闲通道噪声 (A 加权) (定义见表 3-1)	24 位, 32 位	—	0.69	—	μV
	满量程输出电压		2.68	2.81	2.96	Vpp
	输出功率		—	30.8	—	mW
	通道间隔离 4 (定义见表 3-1)	217 Hz 1 kHz 20 kHz	— — —	110 105 90	— — —	dB dB dB
	通道间增益失配 (定义见表 3-1)		—	±0.1	—	dB
	通道间相位失配 (定义见表 3-1)		—	—	±0.01	°
HPOUTx 的其他特性	输出偏置电压: 静音 (定义见表 3-1)		—	±50	±100	μV
	增益漂移 (定义见表 3-1)		—	±100	—	ppm/°C
	负载电阻 (RL)	6	—	—	—	Ω
	负载电容 (CL)		—	—	1	nF
	开启时间 (定义见表 3-1)		—	—	12	毫秒
	PDN_HP 使能或禁用期间的点击/爆音	A 加权	—	±50	±100	μV

- 本表同样适用于外部VCP_FILT供电模式: CS43131的上电流程详见第5.13.1节; EXT_VCPFILT = 1; 当EXT_VCPFILT = 1时, VCP_FILT+和VCP_FILT-符合表3-2的要求; 在此模式下, HV_EN必须设置为1。

2. 在PCM数据中加入了一个最低有效位的三角形概率密度函数抖动。

3. 参考典型满量程电压。适用于表中所有THD+N和动态范围数值。

4. 耳机输出测试配置。符号化元件值在测试条件下指定。


表 3-7. 耳机负载测量

测试条件 (除非另有说明) : 图 2-1 显示 CS43131 连接; GNDD = GNDGP = GNDA = 0 V; 电压均相对于接地; 典型性能数据采集条件为 VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; 最小V最大性能数据采集条件为 VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; 环境温度 TA = +25°C。MCLK_INT = 1, PDN_XTAL = 0, 且 MCLK_SRC_SEL = 00 (晶体频率 fXTAL = 22.5792 MHz)

参数	符号	最小值	典型	最大值	单位
频率范围	—	20	—	20k	Hz
频率分辨率	—	—	5.94	—	Hz

Table 3-7. Headphone Load Measurement (Cont.)

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43131 connections; GNDD = GNDP = GND = 0 V; voltages are with respect to ground; typical performance data taken with VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; min/max performance data taken with VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; TA = +25°C. MCLK_INT = 1, PDN_XTAL = 0, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz)

Parameters	Symbol	Minimum	Typical	Maximum	Units
Low frequency impedance range	—	8	—	1200	Ω
Relative impedance measurement capability ¹	—	-12 ²	—	+12	dB
Impedance measurement accuracy ³	Gain error Offset	-10 -1	—	+10 1	% Ω

1. Impedance measurement range is relative to low-frequency HP load impedance measured.

2. Or 4 Ω, whichever is greater.

3. Accuracy is referred to reported impedance.

Table 3-8. Alternate Headphone Path

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43131 connections; GNDD = GNDP = GND = 0 V; voltages are with respect to ground; typical performance data taken with VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; min/max performance data taken with VP = 3.6 V, VCP = 1.8 V, VA = 0 V, VL = VD = 1.8 V; R_L = 32 Ω; TA = +25°C; measurement bandwidth is 20 Hz–20 kHz; MCLK_SRC_SEL = 10, PDN_XTAL = 1.

Parameters	Symbol	Minimum	Typical	Maximum	Units
Switch on characteristics (PDN_HP = 1 HP_IN_EN = 1)	Signal range when switch on ¹	V _{INAI}	—	—	3.00 Vpp
	THD+N with 32 Ω @ 2.82 Vpp	—	—	-103	— dB
	Interchannel isolation	217 Hz 1 kHz 20 kHz	104 — —	110 105 90	— dB dB dB
	HPINx turn-on time ²	EXT_VCPFILT = 1 EXT_VCPFILT = 0	t _{HPIN_ON}	— —	80 μs 1.1 ms
Switch off characteristics (PDN_HP = 1, HP_IN_EN = 0)	Analog signal range when switched off ^{3,4}	V _{INOFF}	—	—	0.3 Vp
	Turn-off time ⁵	t _{HPIN_OFF}	—	—	20 μs
	Off isolation ⁶	217 Hz 1 kHz 20 kHz	— — —	120 120 100	— dB dB dB

1. When switch is on, maximally allowable voltage applied to HPINx pins.

2. HPINx turn-on time is measured when setting HP_IN_EN = 1. I²C ACK signal is received to when the signal appears on the HP out. MCLK_SRC_SEL = 00, PDN_XTAL = 0, MCLK_INT = 1. For EXT_VCPFILT = 1, VCP_FILT± has been properly charged to expected nominal values.

3. When switch is off, maximally allowable voltage applied to HPINx pins.

4. Before switch off event, it is required HPINx signal is within this range before the switch is turned off. When the switch is in off state, HPINx signal cannot exceed this specified range.

5. HPINx turn-off time is measured when HP_IN_EN = 0 ACK signal is received to when the signal disappears from the HP out. This spec also applies when register settings are: MCLK_SRC_SEL = 00, PDN_XTAL = 0, MCLK_INT = 1.

6. Off isolation specification is measured with V_{INOFF} = 0.1 Vp input.

Table 3-9. Combined DAC Digital, On-Chip Analog and HPOUTx Filter Characteristics

Test conditions (unless specified otherwise): The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs. Single-Speed Mode refers to 32-, 44.1-, and 48-kHz sample rates. Double-Speed Mode refers to 88.2- and 96-kHz sample rates. Quad-Speed Mode refers to 176.4- and 192-kHz sample rates. Octuple-Speed Mode refers to 352.8- and 384-kHz sample rates. MCLK_INT is an integer multiple of Fs; HPF disabled; no DC offset applied; group delay does not include serial port delay.

Parameter	Minimum	Typical	Maximum	Units
Fast Roll-Off (FILTER_SLOW_FASTB = 0) Single-Speed Mode ¹	Passband ² to -0.01-dB corner to -3-dB corner attenuation @ Fs/2	0 0 8.44 ³	— — —	0.4535 ⁴ 0.482 dB
	Passband ripple 10 Hz to -0.01-dB corner ⁵	-0.01	—	+0.01 dB
	Stopband	0.547	—	— Fs
	Stopband attenuation ⁶	110	—	— dB
	Group delay (linear phase) PHCOMP_LOWLATB = 1	—	39.5/Fs ⁷	— s
	Group delay (minimum phase) PHCOMB_LOWLATB = 0	—	6.3/Fs ⁸	— s
	Deemphasis error ⁹ (Relative to 1 kHz) Fs = 44.1 kHz	—	—	±0.3 dB

表 3-7. 耳机负载测量 (续)

测试条件 (除非另有说明) : 图 2-1 显示 CS43131 连接; GNDD = GNDGP = GNDA = 0 V; 电压均相对于接地; 典型性能数据采集条件为 VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; 最小/最大性能数据采集条件为 VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; 环境温度 TA = +25° C。MCLK_INT = 1, PDN_XTAL = 0, 且 MCLK_SRC_SEL = 00 (晶体频率 fXTAL = 22.5792 MHz)

参数	符号	最小值	典型	最大值	单位
低频阻抗范围	—	8	—	1200	Ω
相对阻抗测量能力 ¹	—	-12 ²	—	+12	dB
阻抗测量精度 ³	增益误差 偏置	-10 -1	—	+10 1	% Ω

1. 阻抗测量范围基于低频耳机负载阻抗的测量值。

2. 或 4 Ω, 以较大者为准。

3. 精度以报告的阻抗值为准。

表 3-8. 备用耳机路径

测试条件 (除非另有说明) : 图 2-1 显示 CS43131 连接; GNDD = GNDGP = GNDA = 0 V; 电压均相对于接地; 典型性能数据采集条件为 VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; 最小/最大性能数据在 VP = 3.6 V, VCP = 1.8 V, VA = 0 V, VL = VD = 1.8 V; RL = 32 Ω; TA = +25° C 条件下测得; 测量带宽为 20 Hz–20 kHz; MCLK_SRC_SEL = 10, PDN_XTAL = 1。

参数	符号	最小值	典型	最大值	单位
开关开启特性 (PDN_HP = 1 HP_IN_EN = 1)	V _{INAI}	—	—	3.00	V _{pp}
	—	—	-103	—	dB
	通道间隔离	217 Hz 1 kHz 20 kHz	104 — —	110 105 90	dB dB dB
	t _{HPIN_ON}	—	—	80 1.1	μs 毫秒
关闭特性 (PDN_HP = 1, HP_IN_EN = 0)	V _{关断}	—	—	0.3	峰值电压
	t _{HPIN_OFF}	—	—	20	μs
	关闭隔离度 ⁶	217 Hz 1 kHz 20 kHz	— — —	120 120 100	dB dB dB
	—	—	—	—	dB

1. 开关开启时, 允许施加于 HPINx 引脚的最大电压。

2. HPINx 开启时间在设置 HP_IN_EN = 1 时测量。当 HP 输出信号出现时, 接收到 I²C ACK 信号。MCLK_SRC_SEL = 00, PDN_XTAL = 0, MCLK_INT = 1。对于 EXT_VCPFILT = 1, VCP_FILT±已正确充电至预期标称值。

3. 开关关闭时, 允许施加于 HPINx 引脚的最大电压。

4. 在开关关闭事件之前, 要求 HPINx 信号处于此范围内。开关关闭状态时, HPINx 信号不得超过此规定范围。

5. HPINx 关闭时间指从接收到 HP_IN_EN = 0 的 ACK 信号到 HP 输出信号消失的时间。本规格同样适用于寄存器设置为: MCLK_SRC_SEL = 00, PDN_XTAL = 0, MCLK_INT = 1。

6. 关闭隔离度规格在输入 V_{关断} = 0.1 V_p 时测量。

表 3-9. 组合 DAC 数字、片上模拟及 HPOUTx 滤波器特性

测试条件 (除非另有说明) : 滤波器特性已归一化至采样频率 (Fs), 可通过将给定特性乘以 Fs 来参考所需采样率。单速模式指 32、44.1 及 48 kHz 采样率。双速模式指 88.2 及 96 kHz 采样率。四倍速模式指 176.4 kHz 和 192 kHz 采样率。八倍速模式指 352.8 kHz 和 384 kHz 采样率。MCLK_INT 为 Fs 的整数倍; 高通滤波器禁用; 无直流偏移; 群延迟不包括串行端口延迟。

参数	最小值	典型	最大值	单位
快速滚降 (FILTER_SLOW_FASTB = 0) 单速模式 ¹	至 -0.01 dB 截止频率 至 -3 dB 截止频率 Fs/2 处的衰减	0 0 8.44 ³	— — —	0.4535 ⁴ 0.482 dB
通带 ²	—	—	+0.01	dB
通带波纹 10 Hz 至 -0.01 dB 截止频率 ⁵	-0.01	—	—	—
阻带	0.547	—	—	—
阻带衰减 ⁶	110	—	—	dB
群延迟 (线性相位) PHCOMP_LOWLATB = 1	—	39.5/Fs ⁷	—	秒
群延迟 (最小相位) PHCOMB_LOWLATB = 0	—	6.3/Fs ⁸	—	秒
预加重误差 ⁹ (相对于 1 kHz)	采样频率 = 44.1 kHz	—	±0.3	dB

Table 3-9. Combined DAC Digital, On-Chip Analog and HPOUTx Filter Characteristics (Cont.)

Test conditions (unless specified otherwise): The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs. Single-Speed Mode refers to 32-, 44.1-, and 48-kHz sample rates. Double-Speed Mode refers to 88.2- and 96-kHz sample rates. Quad-Speed Mode refers to 176.4- and 192-kHz sample rates. Octuple-Speed Mode refers to 352.8- and 384-kHz sample rates. MCLK_INT is an integer multiple of Fs; HPF disabled; no DC offset applied; group delay does not include serial port delay.

Parameter		Minimum	Typical	Maximum	Units
Fast Roll-Off (FILTER_SLOW_FASTB = 0) Double-Speed Mode ¹	Passband ² to -0.01-dB corner	0	—	0.227	Fs
	to -3-dB corner	0	—	0.48	Fs
	attenuation @ Fs/2	7.77	—	—	dB
	Passband ripple 10 Hz to -0.01-dB corner	-0.01	—	0.01	dB
	Stopband	0.583	—	—	Fs
	Stopband attenuation ⁶	80	—	—	dB
Fast Roll-Off (FILTER_SLOW_FASTB = 0) Quad-Speed Mode ¹	Group delay (linear phase) PHCOMB_LOWLATB = 1	—	22.3/Fs	—	s
	Group delay (minimum phase) PHCOMB_LOWLATB = 0	—	7.5/Fs	—	s
	Passband ² to -0.01-dB corner	0	—	0.114	Fs
	to -3-dB corner	0	—	0.46	Fs
	attenuation @ Fs/2	9.44	—	—	dB
	Passband ripple 10 Hz to -0.01-dB corner	-0.01	—	0.01	dB
Slow Roll-Off (FILTER_SLOW_FASTB = 1) Single-Speed Mode ¹	Stopband	0.583	—	—	Fs
	Stopband attenuation ⁶	80	—	—	dB
	Group delay (linear phase) PHCOMB_LOWLATB = 1	—	20.7/Fs	—	s
	Group delay (minimum phase) PHCOMB_LOWLATB = 0	—	11.3/Fs	—	s
	Passband ² to -0.01-dB corner	0	—	0.417	Fs
	to -3-dB corner	0	—	0.482	Fs
Slow Roll-Off (FILTER_SLOW_FASTB = 1) Double-Speed Mode ¹	attenuation @ Fs/2	6.45 ¹⁰	—	—	dB
	Passband ripple 10 Hz to -0.01-dB corner ⁵	-0.01	—	+0.01	dB
	Stopband	0.583	—	—	Fs
	Stopband attenuation ⁶	64	—	—	dB
	Group delay (linear phase) PHCOMB_LOWLATB = 1	—	34.5/Fs ¹¹	—	s
	Group delay (minimum phase) PHCOMB_LOWLATB = 0	—	5.6/Fs ¹²	—	s
Slow Roll-Off (FILTER_SLOW_FASTB = 1) Quad-Speed Mode ¹	Deemphasis error ⁹ (Relative to 1 kHz)	Fs = 44.1 kHz	—	±0.3	dB
	Passband ² to -0.01-dB corner	0	—	0.208	Fs
	to -3-dB corner	0	—	0.458	Fs
	attenuation @ Fs/2	7	—	—	dB
	Passband ripple 10 Hz to -0.01-dB corner	-0.01	—	0.01	dB
	Stopband	0.792	—	—	Fs
Nonoversampling (NOS) (NOS = 1) Single-Speed Mode ¹	Stopband attenuation ⁶	70	—	—	dB
	Group delay (linear phase) PHCOMB_LOWLATB = 1	—	22.3/Fs	—	s
	Group delay (minimum phase) PHCOMB_LOWLATB = 0	—	6.7/Fs	—	s
	Passband ² to -0.01-dB corner	0	—	0.104	Fs
	to -3-dB corner	0	—	0.43	Fs
	attenuation @ Fs/2	7.00	—	—	dB
Nonoversampling (NOS) (NOS = 1) Double-Speed Mode ¹	Passband ripple 10 Hz to -0.01-dB corner	-0.01	—	0.01	dB
	Stopband	0.792	—	—	Fs
	Stopband attenuation ⁶	75	—	—	dB
	Group delay (linear phase) PHCOMB_LOWLATB = 1	—	20.7/Fs	—	s
	Group delay (minimum phase) PHCOMB_LOWLATB = 0	—	10.6/Fs	—	s
	Passband ² to -0.01-dB corner	0	—	0.026	Fs
Nonoversampling (NOS) (NOS = 1) Quad-Speed Mode ¹	to -3-dB corner	0	—	0.443	Fs
	Passband droop 10 Hz to 20 kHz	—	—	3.2 ¹³	dB
	Group delay	—	2.7/Fs	—	s
Nonoversampling (NOS) (NOS = 1) Double-Speed Mode ¹	Passband ² to -0.01-dB corner	0	—	0.0246	Fs
	to -3-dB corner	0	—	0.446	Fs
	Passband droop 10 Hz to 20 kHz	—	—	0.73	dB
Nonoversampling (NOS) (NOS = 1) Quad-Speed Mode ¹	Group delay	—	4.5/Fs	—	s
	Passband ² to -0.01-dB corner	0	—	0.026	Fs
	to -3-dB corner	0	—	0.405	Fs
	Passband droop 10 Hz to 20 kHz	—	—	0.17	dB
	Group delay	—	8.4/Fs	—	s

表 3-9. 组合 DAC 数字、片上模拟及 HPOUTx 滤波器特性 (续)

测试条件 (除非另有说明) : 滤波器特性已归一化至采样频率 (Fs) , 可通过将给定特性乘以 Fs 来参考所需采样率。单速模式指 32、44.1 及 48 kHz 采样率。双速模式指 88.2 及 96 kHz 采样率。四倍速模式指 176.4 kHz 和 192 kHz 采样率。八倍速模式指 352.8 kHz 和 384 kHz 采样率。MCLK_INT 为 Fs 的整数倍; 高通滤波器禁用; 无直流偏移; 群延迟不包括串行端口延迟。

参数		最小值	典型	最大单位
快速滚降 (FILTER_SLOW_FASTB = 0) 双速模式 ¹	通带 2 至 -0.01 dB 截止频率 至 -3 dB 截止频率 Fs/2 处的衰减	0 0 7.77	— — —	0.227 0.48 dB
	通带波纹 10 Hz 至 -0.01 dB 截止频率	-0.01	—	0.01 dB
	阻带	0.583	—	—
	阻带衰减 6	80	—	— dB
	群延迟 (线性相位) PHCOMB_LOWLATB = 1	—	22.3/Fs	— 秒
	群延迟 (最小相位) PHCOMB_LOWLATB = 0	—	7.5/Fs	— 秒
	通带 2 至 -0.01 dB 截止频率 至 -3 dB 截止频率 Fs/2 处的衰减	0 0 9.44	— — —	0.114 0.46 dB
快速滚降 (FILTER_SLOW_FASTB = 0) 四倍速模式 ¹	通带波纹 10 Hz 至 -0.01 dB 截止频率	-0.01	—	0.01 dB
	阻带	0.583	—	—
	阻带衰减 6	80	—	— dB
	群延迟 (线性相位) PHCOMB_LOWLATB = 1	—	20.7/采样频率	— 秒
	群延迟 (最小相位) PHCOMB_LOWLATB = 0	—	11.3/采样频率	— 秒
	通带 2 至 -0.01 dB 截止频率 至 -3 dB 截止频率 Fs/2 处的衰减	0 0 6.45 ¹⁰	— — —	0.417 0.482 dB
	通带波纹 10 Hz 至 -0.01 dB 截止频率 5	-0.01	—	+0.01 dB
慢速滚降 (FILTER_SLOW_FASTB = 1) 单速模式 ¹	阻带	0.583	—	—
	阻带衰减 6	64	—	— dB
	群延迟 (线性相位) PHCOMB_LOWLATB = 1	—	34.5/采样频率 ¹¹	— 秒
	群延迟 (最小相位) PHCOMB_LOWLATB = 0	—	5.6/采样频率 ¹²	— 秒
	预加重误差 ⁹ (相对于 1 kHz)	采样频率 = 44.1 kHz	—	±0.3 dB
	通带 2 至 -0.01 dB 截止频率 至 -3 dB 截止频率 Fs/2 处的衰减	0 0 7	— — —	0.208 0.458 dB
	通带波纹 10 Hz 至 -0.01 dB 截止频率	-0.01	—	0.01 dB
慢速滚降 (FILTER_SLOW_FASTB = 1) 双速模式 ¹	阻带	0.792	—	—
	阻带衰减 6	70	—	— dB
	群延迟 (线性相位) PHCOMB_LOWLATB = 1	—	22.3/Fs	— 秒
	群延迟 (最小相位) PHCOMB_LOWLATB = 0	—	6.7/采样频率	— 秒
	通带 2 至 -0.01 dB 截止频率 至 -3 dB 截止频率 Fs/2 处的衰减	0 0 7.00	— — —	0.104 0.43 dB
	通带波纹 10 Hz 至 -0.01 dB 截止频率	-0.01	—	0.01 dB
	阻带	0.792	—	—
慢速滚降 (FILTER_SLOW_FASTB = 1) 四倍速模式 ¹	阻带衰减 6	75	—	— dB
	群延迟 (线性相位) PHCOMB_LOWLATB = 1	—	20.7/采样频率	— 秒
	群延迟 (最小相位) PHCOMB_LOWLATB = 0	—	10.6/采样频率	— 秒
	通带 2 至 -0.01 dB 截止频率 至 -3 dB 截止频率	0 0 —	— — —	0.026 0.443 dB
	通带下陷 10 Hz 至 20 kHz	—	—	3.2 ¹³ dB
	群延迟	—	2.7/采样频率	— 秒
	通带 2 至 -0.01 dB 截止频率 至 -3 dB 截止频率	0 0 —	— — —	0.0246 0.446 dB
非过采样 (NOS) (NOS = 1) 单速模式 ¹	通带下陷 10 Hz 至 20 kHz	—	—	0.73 dB
	群延迟	—	4.5/采样频率	— 秒
	通带 2 至 -0.01 dB 截止频率 至 -3 dB 截止频率	0 0 —	— — —	0.026 0.405 dB
	通带下陷 10 Hz 至 20 kHz	—	—	0.17 dB
	群延迟	—	8.4/Fs	— 秒
	通带 2 至 -0.01 dB 截止频率 至 -3 dB 截止频率	0 0 —	— — —	0.026 0.405 dB
	通带下陷 10 Hz 至 20 kHz	—	—	0.17 dB

Table 3-9. Combined DAC Digital, On-Chip Analog and HPOUTx Filter Characteristics (Cont.)

Test conditions (unless specified otherwise): The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs. Single-Speed Mode refers to 32-, 44.1-, and 48-kHz sample rates. Double-Speed Mode refers to 88.2- and 96-kHz sample rates. Quad-Speed Mode refers to 176.4- and 192-kHz sample rates. Octuple-Speed Mode refers to 352.8- and 384-kHz sample rates. MCLK_INT is an integer multiple of Fs; HPF disabled; no DC offset applied; group delay does not include serial port delay.

Parameter		Minimum	Typical	Maximum	Units
Octuple-Speed Mode ¹	Passband ² to -0.01-dB corner to -3-dB corner	0 0	— —	0.0299 0.263	Fs Fs
	Passband droop 10 Hz to 20 kHz	—	—	0.04	dB
	Group delay	—	17/Fs	—	s

1. Filter response is by design.
2. Response is clock-dependent and scales with Fs.
3. 8.5 dB for 32-kHz sample rate.
4. 0.454 Fs for 32-kHz sample rate.
5. Filter ripple specification is invalid with deemphasis enabled.
6. For Single-Speed Mode, the measurement bandwidth is from stopband to 3 Fs.
For Double-Speed Mode, the measurement bandwidth is from stopband to 3 Fs.
For Quad-Speed Mode, the measurement bandwidth is from stopband to 1.34 Fs.
7. 39/Fs for 32-kHz sample rate.
8. 5.9/Fs for 32-kHz sample rate.
9. Deemphasis is available only in 44.1 kHz.
10. 6.5 dB for 32-kHz sample rate.
11. 34/Fs for 32-kHz sample rate.
12. 5.2/Fs for 32-kHz sample rate.
13. 3.9 dB for 32-kHz sample rate (passband droop 10 Hz to 15 kHz).

Table 3-10. Combined DAC Digital, On-Chip Analog and HPOUTx Filter Characteristics (Wideband Flatness Mode)

Test conditions (unless specified otherwise): The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs. Wideband Flatness Mode refers to Fs = 192 kHz sample rates. PCM_WBF_EN = 1. MCLK_INT is an integer multiple of Fs; HPF disabled; no DC offset applied; group delay does not include serial port delay.

Parameter		Minimum	Typical	Maximum	Units
Wideband Flatness Mode ¹	Passband ² to -0.003-dB corner to -3-dB corner attenuation @ Fs/2	0 0 3	— — —	0.417 0.46 —	Fs Fs dB
	Passband ripple 10 Hz to -0.003-dB corner	-0.003	—	0.003	dB
	Stopband	0.583	—	—	Fs
	Stopband attenuation ³	80	—	—	dB
	Group delay	—	20.7/Fs	—	s

1. Filter response is by design and may require calibration.
2. Response is clock-dependent and scales with Fs.
3. The measurement bandwidth is from stopband to 1.34 Fs.

Table 3-11. DAC High-Pass Filter (HPF) Characteristics

Test conditions (unless specified otherwise): Gains are all set to 0 dB; TA = +25°C.

Parameter 1		Minimum	Typical	Maximum	Units
Passband ²	-0.05-dB corner -3.0-dB corner	— —	0.195 x 10 ⁻³ /N 19.5 x 10 ⁻⁶ /N	— —	Fs Fs
Passband ripple (0.417x10 ⁻³ /N Fs to 0.417/N Fs; normalized to 0.417/N Fs) ²	—	—	—	0.01	dB
Phase deviation @ 0.453x10 ⁻³ /N Fs ²	—	—	2.45	—	°
Filter settling time ³	—	—	24500 x N / Fs ²	—	s

1. Response scales with Fs in PCM Mode. Specifications are normalized to Fs and are denormalized by multiplying by Fs. For DSD Mode, Fs is 44.1 kHz.
2. For PCM Single-Speed Mode, N = 1.
For PCM Double-Speed Mode, N = 2.
For PCM Quad-Speed Mode, N = 4.
For PCM Octuple-Speed Mode, N = 8.
For DSD 64 x Fs Mode, N = 1.
For DSD 128 x Fs Mode, N = 1.
3. Required time for the magnitude of the DC component present at the output of the HPF to reach 5% of the applied DC signal.

表 3-9. 组合 DAC 数字、片上模拟及 HPOUTx 滤波器特性 (续)

测试条件 (除非另有说明) : 滤波器特性已归一化至采样频率 (F_s) , 可通过将给定特性乘以 F_s 来参考所需采样率。单速模式指 32、44.1 及 48 kHz 采样率。双速模式指 88.2 及 96 kHz 采样率。四倍速模式指 176.4 kHz 和 192 kHz 采样率。八倍速模式指 352.8 kHz 和 384 kHz 采样率。MCLK_INT 为 F_s 的整数倍; 高通滤波器禁用; 无直流偏移; 群延迟不包括串行端口延迟。

参数		最小值	典型	最大单位
八倍速模式 1	通带 2 至 -0.01 dB 截止频率 至 -3 dB 截止频率	0 0	— —	0.0299 0.263 采样频率 采样频率
	通带下陷 10 Hz 至 20 kHz	—	—	0.04 dB
	群延迟	—	17/ F_s	— 秒

1. 滤波器响应由设计决定。
2. 响应依赖时钟且随采样频率 F_s 变化。
3. 32 kHz 采样率时为 8.5 dB。
4. 32 kHz 采样率时为 0.454 F_s 。
5. 启用预加重时滤波器纹波规格无效。
6. 单速模式下, 测量带宽为从阻带至 3 F_s 。
双速模式下, 测量带宽为从阻带至 3 F_s 。
7. 四倍速模式下, 测量带宽为从阻带至 1.34 F_s 。
8. 32 kHz 采样率时为 39/ F_s 。
9. 32 kHz 采样率时为 5.9/ F_s 。
10. 预加重仅适用于 44.1 kHz。
11. 32/ F_s , 适用于 32 kHz 采样率。
12. 5.2/ F_s , 适用于 32 kHz 采样率。
13. 3.9 dB, 适用于 32 kHz 采样率 (通带下陷 10 Hz 至 15 kHz)。

表 3-10. 组合 DAC 数字、片上模拟及 HPOUTx 滤波器特性 (宽带平坦模式)

测试条件 (除非另有说明) : 滤波器特性已归一化至采样频率 (F_s) , 可通过将给定特性乘以 F_s 来参考所需采样率。宽带平坦模式指 $F_s = 192$ kHz 采样率。PCM_WBF_EN = 1。MCLK_INT 为 F_s 的整数倍; 高通滤波器禁用; 无直流偏移; 群延迟不包括串行端口延迟。

参数		最小值	典型	最大单位
宽带平坦模式 1	通带 2 至 -0.003 dB 拐点 至 -3 dB 截止频率 $F_s/2$ 处的衰减	0 0 3	— — —	0.417 0.46 采样频率 采样频率 dB
	通带波纹 10 Hz 至 -0.003 dB 拐点	-0.003	—	0.003 dB
	阻带	0.583	—	— 采样频率
	阻带衰减 3	80	—	— dB
	群延迟	—	20.7/采样频率	— 秒

1. 滤波器响应为设计值, 可能需要校准。
2. 响应依赖时钟且随采样频率 F_s 变化。
3. 测量带宽范围为从阻带至 1.34 采样频率 (F_s)。

表 3-11. DAC 高通滤波器 (HPF) 特性

测试条件 (除非另有说明) : 增益均设为 0 dB; 环境温度 $A = +25^\circ\text{C}$ 。

参数 1	最小值	典型	最大值	单位
通带 2 -0.05 dB 拐点 -3.0 dB 拐点	— —	$0.195 \times 10^{-3}/N$ $19.5 \times 10^{-6}/N$	— —	采样频率 采样频率
通带波纹 ($0.417 \times 10^{-3}/N F_s$ 至 $0.417/N F_s$; 归一化至 $0.417/N F_s$) 2	—	—	0.01	dB
相位偏差 @ $0.453 \times 10^{-3}/N F_s$ 2	—	2.45	—	°
滤波器稳定时间 3	—	$24500 \times N / F_s$ 2	—	秒

1. 在 PCM 模式下响应随采样频率 (F_s) 变化。规格已归一化至 F_s , 实际值通过乘以 F_s 反归一化。对于 DSD 模式, F_s 为 44.1 kHz。
2. 对于 PCM 单速模式, $N = 1$ 。
对于 PCM 双速模式, $N = 2$ 。
对于 PCM 四倍速模式, $N = 4$ 。
对于 PCM 八倍速模式, $N = 8$ 。
对于 DSD 64 倍采样频率模式, $N = 1$ 。
对于 DSD 128 倍采样频率模式, $N = 1$ 。
3. 高通滤波器输出端直流分量幅值达到所施加直流信号 5% 所需时间。

Table 3-12. DSD Combined Digital and On-Chip Analog Filter Response 1

Test conditions (unless specified otherwise): Digital gains are all set to 0 dB; $T_A = +25^\circ\text{C}$; $\text{PDN_XTAL} = 0$, $\text{MCLK_INT} = 1$, $\text{DSD_EN} = 1$, and $\text{MCLK_SRC_SEL} = 00$ (crystal frequency $f_{\text{XTAL}} = 22.5792 \text{ MHz}$).

Parameter		Minimum	Typical	Maximum	Units
DSD Mode	Passband to -3-dB corner	—	50	—	kHz
	Frequency response 20 Hz to 20 kHz	-0.05	—	0.05	dB
	Roll-off	27	—	—	dB/Oct

1. Filter response is by design.

Table 3-13. Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43131 connections; $\text{GNDD} = \text{GND}_{\text{CP}} = \text{GND}_{\text{A}} = 0 \text{ V}$; voltages are with respect to ground; parameters can vary with VL and VP ; typical performance data taken with $\text{VP} = 3.6 \text{ V}$, $\text{VCP} = \text{VA} = 1.8 \text{ V}$, $\text{VD} = 1.8 \text{ V}$ and $\text{VL} = 1.8 \text{ V}$; min/max performance data taken with $\text{VP} = 3.6 \text{ V}$, $\text{VCP} = \text{VA} = 1.8 \text{ V}$, $\text{VD} = 1.8 \text{ V}$ and $\text{VL} = 1.8 \text{ V}$; $T_A = +25^\circ\text{C}$; $C_L = 60 \text{ pF}$.

Parameters 1	Symbol	Minimum	Maximum	Units
Input leakage current 2,3 LRCK1, DSDB/LRCK2 SDIN1, SCLK1, DSDA/SDIN2, DSDCLK/SCLK2 SDA, SCL INT, RESET	I_{in}	—	± 4	μA
		—	± 3	μA
		—	± 100	nA
		—	± 100	nA
Internal weak pull-down	—	550	2450	k Ω
Input capacitance	—	—	10	pF
INT current sink ($V_{\text{OL}} = 0.3 \text{ V}$ maximum)	—	825	—	μA
VL Logic (non-I ² C) High-level output voltage ($I_{\text{OH}} = -100 \mu\text{A}$) Low-level output voltage High-level input voltage Low-level input voltage	V_{OH}	$0.9 \cdot \text{VL}$	—	V
	V_{OL}	—	$0.1 \cdot \text{VL}$	V
	V_{IH}	$0.7 \cdot \text{VL}$	—	V
	V_{IL}	—	$0.3 \cdot \text{VL}$	V
VL Logic (I ² C only) Hysteresis voltage (Fast Mode and Fast Mode Plus) Low-level output voltage High-level input voltage Low-level input voltage	V_{HYS}	$0.05 \cdot \text{VL}$	—	V
	V_{OL}	—	$0.2 \cdot \text{VL}$	V
	V_{IH}	$0.7 \cdot \text{VL}$	—	V
	V_{IL}	—	$0.3 \cdot \text{VL}$	V
HP_DETECT ⁴ High-level input voltage Low-level input voltage	V_{IH}	$0.93 \cdot \text{VP}$	—	V
	V_{IL}	—	2.0	V
HP_DETECT current to VCP_FILT-	$I_{\text{HP_DETECT}}$	1.00	2.91	μA
RESET pulse width low	—	1000	—	μs

1. See Table 1-1 for serial and control-port power rails.

2. Specification is per pin.

3. Includes current through internal pull-up or pull-down resistors on pin.

4. The HP_DETECT input circuit allows the HP_DETECT signal to be as low of a voltage as VCP_FILT- and as high as VP. Section 4.5.1 provides configuration details.

Table 3-14. CLKOUT Characteristics

Test conditions (unless specified otherwise): $\text{GNDD} = \text{GND}_{\text{CP}} = \text{GND}_{\text{A}} = 0 \text{ V}$; voltages are with respect to ground; $\text{VP} = 3.6 \text{ V}$, $\text{VCP} = \text{VA} = 1.8 \text{ V}$, $\text{VL} = \text{VD} = 1.8 \text{ V}$; $C_L = 60 \text{ pF}$; PLL reference input must meet the phase-noise mask specified in Fig. 4-15; $T_A = +25^\circ\text{C}$; Output jitter is measured from 100 Hz to half of the output frequency.

Parameters	Symbol	Minimum	Typical	Maximum	Units
CLKOUT output frequency	f_{CLKOUT}	2.8224	3	3.072	MHz
		5.6448	6	6.144	MHz
		7.5264	8	8.192	MHz
		11.2896	12	12.288	MHz
CLKOUT output duty cycle	—	40	50	60	%
CLKOUT output TIE jitter (RMS)	t_{JIT}	—	500	—	ps

Table 3-15. PLL Characteristics

Test conditions (unless specified otherwise): $\text{GNDD} = \text{GND}_{\text{CP}} = \text{GND}_{\text{A}} = 0 \text{ V}$; voltages are with respect to ground; $\text{VP} = 3.6 \text{ V}$, $\text{VCP} = \text{VA} = 1.8 \text{ V}$, $\text{VL} = \text{VD} = 1.8 \text{ V}$; PLL reference input must meet the phase-noise mask specified in Fig. 4-15; $T_A = +25^\circ\text{C}$.

Parameters	Symbol	Minimum	Typical	Maximum	Units
PLL output frequency	f_{out}	22.5792	24	24.576	MHz
PLL lock time	t_{Lock}	—	620	1000	μs

表 3-12. DSD 组合数字与片上模拟滤波器响应 1

测试条件（除非另有说明）：数字增益均设为 0 dB； $T_A = +25^\circ\text{C}$ ； $\text{PDN_XTAL} = 0$ ， $\text{MCLK_INT} = 1$ ， $\text{DSD_EN} = 1$ ，且 $\text{MCLK_SRC_SEL} = 00$ （晶体频率 $f_{\text{XTAL}} = 22.5792 \text{ MHz}$ ）。

参数		最小	典型	最大		单位
DSD 模式	通带	—	50	—	kHz	
	频率响应 20 Hz 至 20 kHz	-0.05	—	0.05	dB	
	衰减	27	—	—	dB/Oct	

1. 濾波器响应为设计值。

表 3-13. 数字接口规格及特性

测试条件（除非另有说明）：图 2-1 显示 CS43131 连接；GNDD = GNDCP = GNDA = 0 V；电压均相对于接地；

参数可能随 VL 和 VP 变化；典型性能数据取自 VP = 3.6 V, VCP = VA = 1.8 V, VD = 1.8 V 和 VL = 1.8 V；最小/最大性能数据取自 VP = 3.6 V, VCP = VA = 1.8 V, VD = 1.8 V 和 VL = 1.8 V；环境温度 TA = +25°C；负载电容 CL = 60 pF。

参数 1		符号	最小值	最大值	单位
输入漏电流 2,3 串行数据输入1, SCLK1, DSDA/串行数据输入2, DSDCLK/SCLK2 <u>SDA, SCL</u> INT, 复位	LRCK1, DSDB/LRCK2	I_{in}	—	± 4	μA
	—		± 3	μA	
	—		± 100	nA	
	—		± 100	nA	
内部弱下拉	—	550	2450	kΩ	
输入电容	—	—	10	pF	
INT 电流汇 (V _{OL} = 最大 0.3 V)	—	825	—	μA	
VL 逻辑 (非 I ² C) 高电平输出电压 ($I_{OH} = -100 \mu A$) 低电平输出电压 高电平输入电压 低电平输入电压	V _{OH}	0.9•VL	—	V	
	V _{OL}	—	0.1•VL	V	
	V _{IH}	0.7•VL	—	V	
	V _{IL}	—	0.3•VL	V	
VL 逻辑 (仅限 I ² C) 迟滞电压 (快速模式及快速模式增强) 低电平输出电压 高电平输入电压 低电平输入电压	V _{HYS}	0.05•VL	—	V	
	V _{OL}	—	0.2•VL	V	
	V _{IH}	0.7•VL	—	V	
	V _{IL}	—	0.3•VL	V	
HP_DETECT ⁴ 高电平输入电压 低电平输入电压	V _{IH}	0.93•VP	—	V	
	V _{IL}	—	2.0	V	
HP_DETECT 至 VCP_FILT- 的电流 ⁴	I _{HP_DETECT}	1.00	2.91	μA	
复位脉冲宽度低电平	—	1000	—	μs	

1.有关串行及控制端口电源轨，请参见表 1-1。

2. 规格按单个引脚计。

3. 包括引脚内部上拉或下拉电阻的电流。

4. HP DETECT 输入电路允许 HP DETECT 信号电压最低为 VCP FILT₋, 最高为 VP。第 4.5.1 节提供配置详情。

表 3-14. CLKOUT 特性

测试条件（除非另有说明）：GNDD = GNDGP = GNDA = 0 V；电压均相对于接地；VP = 3.6 V，VCP = VA = 1.8 V，VL = VD = 1.8 V；CL = 60 pF；PLL参考输入必须满足图4-15中规定的相位噪声掩码；TA = +25°C；输出抖动测量范围为100 Hz至输出频率的一半。

参数	符号	最小值	典型	最大值	单位
CLKOUT输出频率	f_{CLKOUT}	2.8224 5.6448 7.5264 11.2896	3 6 8 12	3.072 6.144 8.192 12.288	MHz MHz MHz MHz
CLKOUT输出占空比	—	40	50	60	%
CLKOUT输出TIE抖动 (RMS)	CLKOUT_SRC_SEL = 01	t_{JIT}	—	500	—
					ps

表 3-15. PLL 特性

测试条件（除非另有说明）：GNDD = GNDP = GNDA = 0 V；电压均相对于接地；VP = 3.6 V，VCP = VA = 1.8 V，VL = VD = 1.8 V；PLL参考输入必须满足图4-15中规定的相位噪声掩码；TA = +25°C。

参数	符号	最小值	典型	最大值	单位
PLL输出频率	f_{out}	22.5792	24	24.576	MHz
PLL锁定时间	t_{Lock}	—	620	1000	μ s

Table 3-15. PLL Characteristics (Cont.)

Test conditions (unless specified otherwise): GNDD = GNDP = GNDA = 0 V; voltages are with respect to ground; VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; PLL reference input must meet the phase-noise mask specified in Fig. 4-15; TA = +25°C.

Parameters	Symbol	Minimum	Typical	Maximum	Units
PLL reference clock input	—	—	11.2896	—	MHz
		—	22.5792	—	MHz
		—	12.2880	—	MHz
		—	24.5760	—	MHz
		—	9.6000	—	MHz
		—	19.2000	—	MHz
		—	12.0000	—	MHz
		—	24.0000	—	MHz
		—	13.0000	—	MHz
		—	26.000	—	MHz
PLL reference clock input jitter	—	—	—	50	ps

Table 3-16. Crystal Characteristics

Test conditions (unless specified otherwise): GNDD = GNDP = GNDA = 0 V; voltages are with respect to ground; VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; TA = +25°C

Parameters 1	Symbol	Minimum	Typical	Maximum	Units
Crystal oscillator frequency	f _{XTAL}	22.57	22.5792/ 24.576	24.58	MHz
Crystal load capacitance	C _{L_XTAL}	5	—	8	pF
Equivalent series resistance	esr _{XTAL}	—	—	100	Ω
Startup time	t _{XTAL_pup}	—	—	6.5	ms
Shunt capacitance	C _O	—	—	0.8	pF
Maximum drive level	—	200	—	—	μW

1. Refer to Section 5.3 for supported crystal options.

Table 3-17. Power-Supply Rejection Ratio (PSRR) Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43131 connections; input test signal held low (all zero data); GNDA = GNDL = GNDP = 0 V; voltages are with respect to ground; VL = VA = VD = 1.8 V, VP = 3.6 V; When testing PSRR, PCM input test signal held low (all zero data); TA = +25°C; PCM_AMUTE = 0.

Parameter 1	Minimum	Typical	Maximum	Units
HPOUTx PSRR with 100-mVpp signal AC coupled to VA supply PDN_HP = 0, HP_IN_EN = 0	217 Hz 1 kHz 20 kHz	— 75 70	— — —	dB dB dB
HPOUTx PSRR with 100-mVpp signal AC coupled to VCP supply PDN_HP = 0, HP_IN_EN = 0	217 Hz 1 kHz 20 kHz	— 80 60	— — —	dB dB dB
HPOUTx PSRR with 100-mVpp signal AC coupled to VP supply PDN_HP = 0, HP_IN_EN = 0	217 Hz 1 kHz 20 kHz	— 100 80	— — —	dB dB dB
HPOUTx (0-dB analog gain) PSRR with 100-mVpp signal AC coupled to VCP supply PDN_HP = 1, HP_IN_EN = 1, R _L = 32 Ω	217 Hz 1 kHz 20 kHz	— 80 60	— — —	dB dB dB
HPOUTx (0-dB analog gain) PSRR with 100-mVpp signal AC coupled to VP supply PDN_HP = 1, HP_IN_EN = 1, R _L = 32 Ω	217 Hz 1 kHz 20 kHz	— 100 80	— — —	dB dB dB

1. PSRR test configuration: Typical PSRR can vary by approximately 6 dB below the indicated values.

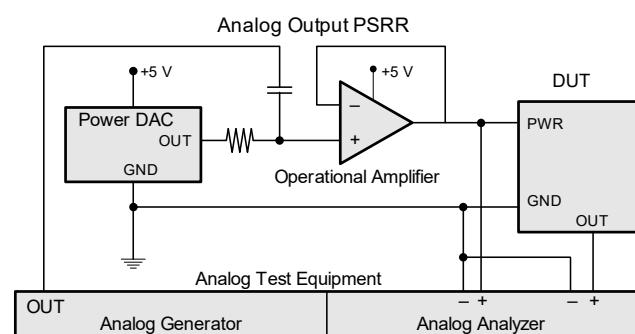


表3-15。PLL特性 (续)

测试条件 (除非另有说明) : GNDD = GNDGP = GNDA = 0 V; 电压均相对于接地; VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; PLL参考输入必须满足图4-15中规定的相位噪声掩码; TA= +25°C。

参数	符号	最小值	典型	最大值	单位
PLL参考时钟输入	—	—	11.2896	—	MHz
		—	22.5792	—	MHz
		—	12.2880	—	MHz
		—	24.5760	—	MHz
		—	9.6000	—	MHz
		—	19.2000	—	MHz
		—	12.0000	—	MHz
		—	24.0000	—	MHz
		—	13.0000	—	MHz
		—	26.000	—	MHz
PLL参考时钟输入抖动	—	—	—	50	ps

表 3-16. 晶体特性

测试条件 (除非另有说明) : GNDD = GNDGP = GNDA = 0 V; 电压均相对于接地; VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; TA= +25°C

参数 1	符号	最小值	典型	最大值	单位
晶体振荡器频率	f _{XTAL}	22.57	22.5792/ 24.576	24.58	MHz
晶体负载电容	C _{L_XTAL}	5	—	8	pF
等效串联电阻	esr _{XTAL}	—	—	100	Ω
启动时间	t _{XTAL_pup}	—	—	6.5	毫秒
并联电容	C _O	—	—	0.8	pF
最大驱动功率	—	200	—	—	μW

1. 有关支持的晶体选项, 请参见第5.3节。

表 3-17. 电源抑制比 (PSRR) 特性

测试条件 (除非另有说明) : 图 2-1显示 CS43131 连接; 输入测试信号保持低电平 (全零数据); GNDA = GNDL = GNDGP = 0 V; 电压均相对于接地; VL = VA = VD = 1.8 V, VP = 3.6 V; 测试PSRR时, PCM输入测试信号保持低电平 (全零数据); TA = +25°C; PCM_AMUTE = 0。

参数 1	最小值	典型	最大值	单位
HPOUTx 100 mVpp信号交流耦合至VA电源时的PSRR PDN_HP = 0, HP_IN_EN = 0	217 Hz 1 kHz 20 kHz	— 75 75 — 70	— — — — —	dB dB dB
HPOUTx 100 mVpp信号交流耦合至VCP电源时的PSRR PDN_HP = 0, HP_IN_EN = 0	217 Hz 1 kHz 20 kHz	— 80 80 — 60	— — — — —	dB dB dB
HPOUTx 100 mVpp信号交流耦合至VP电源时的PSRR PDN_HP = 0, HP_IN_EN = 0	217 Hz 1 kHz 20 kHz	— 100 100 — 80	— — — — —	dB dB dB
HPOUTx (0 dB模拟增益) 100 mVpp信号交流耦合至VCP电源时的PSRR PDN_HP = 1, HP_IN_EN = 1, R _L = 32 Ω	217 Hz 1 kHz 20 kHz	— 80 80 — 60	— — — — —	dB dB dB
HPOUTx (0 dB模拟增益) 100 mVpp信号交流耦合至VP电源时的PSRR PDN_HP = 1, HP_IN_EN = 1, R _L = 32 Ω	217 Hz 1 kHz 20 kHz	— 100 100 — 80	— — — — —	dB dB dB

1. PSRR测试配置: 典型PSRR值可能比标称值低约6 dB。

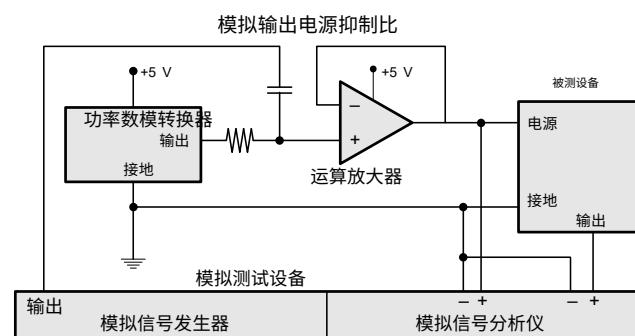


Table 3-18. DC Characteristics

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43131 connections; GNDD = GNDA = GNDP = 0 V; all voltages with respect to ground.

Parameters		Minimum	Typical	Maximum	Units
VCP_FILT (No load connected to HPOUTx) EXT_VCPFILT = 0	VP_LDO Mode	VCP_FILT+ pin (HV_EN = 1) VCP_FILT+ pin (HV_EN = 0)	— —	3.0 2.6	— —
	VCP Mode	VCP_FILT+ pin VCP_FILT- pin	— —	VCP -VCP	— —
	-VA	-VA pin	—	- VA	—
	Alternate headphone path switch-on characteristics PDN_HP = 1, HP_IN_EN = 1	On-resistance r _{ON} matching between channels	— —	0.4 0.05	— —
Other DC characteristics	FILT+ voltage	—	-0.35	—	V
	FILT- voltage	—	0.35	—	V
	HP output current limiter on threshold.	—	120	160	mA
	VD power-on reset threshold (V _{POR})	Up Down	— —	1.15 0.950	— —

Table 3-19. Power Consumption

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43131 connections; GNDA = GNDP = GNDD = 0 V; voltages are with respect to ground; performance data taken with VA = VCP = VD = VL = 1.8 V; VP = 3.6 V; T_A = +25°C; ASP_SPRATE = 0001(44.1-kHz mode); MCLK_INT = 1 (22.5792 MHz); MCLK_SRC_SEL = 00; +1dB_EN = 1; all other fields are set to defaults; no signal on any input; control port inactive; all serial ports are set to Slave or Master Mode as indicated, input clock/data are held low unless active; test load is R_L = 32 Ω and C_L = 1 nF for HPOUTx; measured values include currents consumed by the DAC and do not include current delivered to external loads unless specified otherwise (e.g., from HPOUTx outputs); see Fig. 2-1.

Use Cases		Typical Current (μA)						Total Power (μW)
		P _{OUT}	i _{VCP}	i _{VA}	i _{VD}	i _{VL}	i _{VP}	
1	Off 1	—	0	0	0	0	6	11
2	Standby 2 HPDETECT enabled	—	0	0	256	0	32	576
3	A Playback External MCLK = 22.5792 MHz, I ² S/DoP Stereo HPOUT	Quiescent 3	3808	7835	2786	0	28	26074
		0.1mW	12363	7862	2004	40	32	40199
4	Alternate HP path stereo HPIN enabled 4	Quiescent	32	0	186	0	65	625

1. Off configuration: Clock/data lines held low; RESET = LOW; VA = VD = VL = 0 V, VCP = 0 V, VP = 3.6 V.

2. Standby configuration: Clock/data lines held low; RESET = HIGH; VA = VD = VL = 1.8 V, VCP = 1.8 V, VP = 3.6 V; HP_DETECT_CTRL = 11 (enabled); HPDETECT_PLUG_INT_MASK=0 (unmasked); PDN_XTAL = 1, MCLK_SRC_SEL = 10 (RCO selected as MCLK source).

3. Quiescent configuration: data lines held low; RESET = HIGH; VA = 1.8 V, VD = VL = VCP = 1.8 V, VP = 3.6 V. Serial port, I²S/DoP Mode (ASP and SDIN, ASP_M/Sb = 0); PDN_XTAL = 1.

4. Quiescent configuration: PDN_XTAL = 1; MCLK_SRC_SEL = 10 (RCO selected as MCLK source); alternate headphone path (PDN_HP = 1, HPOUT_CLAMP = 1, HP_IN_EN = 1, HP_IN_LP = 1); data lines held low; RESET = HIGH; VA = 1.8 V, VD = VL = VCP = 1.8 V, VP = 3.6 V.

Table 3-20. Serial-Port Interface Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43131 connections; GNDA = GNDP = GNDD = 0 V; voltages are with respect to ground; parameters can vary with VL; typical performance data taken with VL = VD = VA = VCP = 1.8 V, VP = 3.6 V; min/max performance data taken with VL = 1.8 V; VD = VA = VCP = 1.8 V, VP = 3.6 V; T_A = +25°C; C_L = 60 pF; Logic 0 = ground, Logic 1 = VL; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-13).

Parameters 1,2,3,4		Symbol	Minimum	Typical	Maximum	Units
FSYNC frame rate		F _s	(See Section 4.9.5)			kHz
FSYNC high period 5		t _{H:FSYNC}	1/f _{SCLK}	—	(n-1)/f _{SCLK}	s
Master Mode	FSYNC duty cycle xSP_5050 = 1	—	45	—	55	%
	FSYNC delay time after SCLK launching edge 6	t _{D:CLK-FSYNC}	—	—	10	ns
	SCLK frequency	f _{SCLK}	—	—	f _{MCLK_INT}	MHz
	SCLK high period 7	t _{H:SCLK}	1/(2•f _{SCLK}) – 1/f _{MCLK_INT}	—	1/(2•f _{SCLK}) + 1/f _{MCLK_INT}	ns
	SDIN setup time before SCLK latching edge 6	t _{SU:SDI}	10	—	—	ns
	SDIN hold time after SCLK latching edge 6	t _{H:SDI}	5	—	—	ns

表 3-18. 直流特性

测试条件（除非另有说明）：图 2-1 显示 CS43131 连接；GNDD = GNDA = GNDPC = 0 V；所有电压均相对于接地。

参数		最小值	典型	最大值	单位
VCP_FILT (HPOUTx 无负载连接)	VP_LDO 模式 VCP_FILT+ 引脚 (高压使能 = 1) EXT_VCPFILT = 0	—	3.0	—	V
	VCP_FILT+ 引脚 (高压使能 = 0)	—	2.6	—	V
	VCP_FILT- 引脚 (高压使能 = 1)	—	-3.0	—	V
	VCP_FILT- 引脚 (高压使能 = 0)	—	-2.6	—	V
	VCP 模式	VCP_FILT+ 引脚 VCP_FILT- 引脚	— —	VCP -VCP	V V
-VA	-VA 引脚	—	-VA	—	V
备用耳机路径	导通电阻	—	0.4	—	Ω
开关特性	r _{ON} 通道间匹配	—	0.05	—	Ω
PDN_HP = 1, HP_IN_EN = 1	FILT+ 电压	—	-0.35	—	V
其他直流特性	FILT- 电压	—	0.35	—	V
	耳机输出电流限制阈值	—	120	160	mA
	VD 上电复位阈值 (V _{POR})	上升 下降	— —	1.15 0.950	V V

表 3-19. 功耗

测试条件（除非另有说明）：图 2-1 显示 CS43131 连接；GNDA = GNDPC = GNDD = 0 V；电压均相对于接地；

性能数据采集条件：VA = VCP = VD = VL = 1.8 V；VP = 3.6 V；环境温度 T_A = +25°C；ASP_SPRATE = 0001 (44.1 kHz 模式)；MCLK_IN T = 1 (22.5792 MHz)；MCLK_SRC_SEL = 00；+1 dB_EN = 1；所有其他字段均设置为默认值；所有输入无信号；控制端口处于非激活状态；所有串行端口均按指示设置为从模式或主模式，输入时钟/数据保持低电平，除非处于激活状态；测试负载为 R_L = 32 Ω 和 C_L = 1 nF，适用于 HPOUTx；测量值包括 DAC 消耗的电流，不包括送至外部负载的电流，除非另有说明（例如来自 HPOUTx 输出）；参见图 2-1。

使用案例		典型电流 (μA)						总功率 (μW)
		P _{OUT}	i _{VCP}	i _{VA}	i _{VD}	i _{VL}	i _{VP}	
1	关闭 ¹	—	0	0	0	0	6	11
2	待机 ² 启用HPDETECT	—	0	0	256	0	32	576
3	A 播放 外部MCLK = 22.5792 MHz, I ² S/DoP 立体声HPOUT	静态 ³	3808	7835	2786	0	28	26074
		0.1mW	12363	7862	2004	40	32	40199
4	备用耳机路径立体声 HPIN 启用 ⁴	静态	32	0	186	0	65	625

1. 关闭配置：时钟/数据线保持低电平；复位 = 低电平；VA = VD = VL = 0 V，VCP = 0 V，VP = 3.6 V。

2. 待机配置：时钟/数据信号线保持低电平；复位 = 高电平；VA = VD = VL = 1.8 V，VCP = 1.8 V，VP = 3.6 V；HP_DETECT_CTRL = 11 (启用)；HP_DETECT_PLUG_INT_MASK = 0 (未屏蔽)；PDN_XTAL = 1，MCLK_SRC_SEL = 10 (选择RCO作为MCLK源)。

3. 静态配置：数据信号线保持低电平；复位 = 高电平；VA = 1.8 V，VD = VL = VCP = 1.8 V，VP = 3.6 V。串口，I²S/DoP模式 (ASP和SDIN, ASP_M/Sb = 0)；PDN_XTAL = 1。

4. 静态配置：PDN_XTAL = 1；MCLK_SRC_SEL = 10 (选择RCO作为MCLK源)；备用耳机路径 (PDN_HP = 1, HPOUT_CLAMP = 1, HP_IN_EN = 1, HP_IN_LP = 1)；数据线保持低电平；复位 = 高电平；VA = 1.8 V，VD = VL = VCP = 1.8 V，VP = 3.6 V。

表 3-20. 串口接口特性

测试条件（除非另有说明）：图 2-1 显示 CS43131 连接；GNDA = GNDPC = GNDD = 0 V；电压均相对于接地；

参数可能随 VL 变化；典型性能数据采集条件为 VL = VD = VA = VCP = 1.8 V，VP = 3.6 V；最小/最大性能数据采集条件为 VL = 1.8 V；VD = VA = VCP = 1.8 V，VP = 3.6 V；T_A = +25°C；C_L = 60 pF；逻辑0 = 接地，逻辑1 = VL；输出时序在 V_{OL} 和 V_{OH} 阈值处测量（见表3-13）。

参数 1,2,3,4		符号	最小值	典型	最大值	单位
FSYNC帧率		采样频率	(见第4.9.5节)			kHz
FSYNC高电平周期 ⁵		t _{H:FSYNC}	1/f _{SCLK}	—	(n-1)/f _{SCLK}	秒
主模式	FSYNC占空比 xSP_5050 = 1	—	45	—	55	%
	SCLK启动沿后FSYNC延迟时间 ⁶	t _{D:CLK-FSYNC}	—	—	10	纳秒
SCLK频率		f _{SCLK}	—	—	f _{MCLK_INT}	MHz
	SCLK 高电平周期 ⁷	t _{H:SCLK}	1/(2*f _{SCLK}) - 1/f _{MCLK_INT}	—	1/(2*f _{SCLK}) + 1/f _{MCLK_INT}	纳秒
	SDIN 在 SCLK 锁存沿前的建立时间 ⁶	t _{SU:SDI}	10	—	—	纳秒
	SDIN 在 SCLK 锁存沿后的保持时间 ⁶	t _{H:SDI}	5	—	—	纳秒

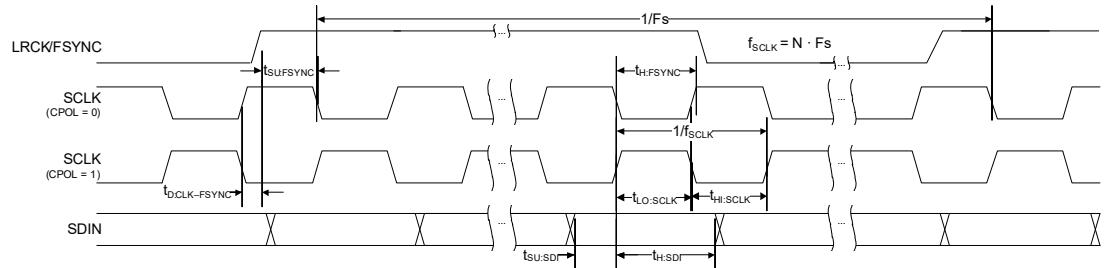
Table 3-20. Serial-Port Interface Characteristics (Cont.)

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43131 connections; GNDA = GNDP = GNDD = 0 V; voltages are with respect to ground; parameters can vary with VL; typical performance data taken with VL = VD = VA = VCP = 1.8 V, VP = 3.6 V; min/max performance data taken with VL = 1.8 V; VD = VA = VCP = 1.8 V, VP = 3.6 V; TA = +25°C; CL = 60 pF; Logic 0 = ground, Logic 1 = VL; output timings are measured at VO_{OL} and VO_{OH} thresholds (see Table 3-13).

Parameters 1,2,3,4		Symbol	Minimum	Typical	Maximum	Units
Slave Mode	FSYNC setup time before SCLK latching edge ⁶	t _{SU:FSYNC}	10	—	—	ns
	FSYNC hold time after SCLK latching edge ⁶	t _{H:FSYNC}	5	—	—	ns
	SCLK frequency	f _{SCLK}	—	—	24.58	MHz
	SCLK high period	t _{HI:SCLK}	16	—	—	ns
	SCLK low period	t _{LO:SCLK}	16	—	—	ns
	SDIN setup time before SCLK latching edge ⁸	t _{SU:SDI}	10	—	—	ns
	SDIN hold time after SCLK latching edge ⁶	t _{H:SDI}	5	—	—	ns

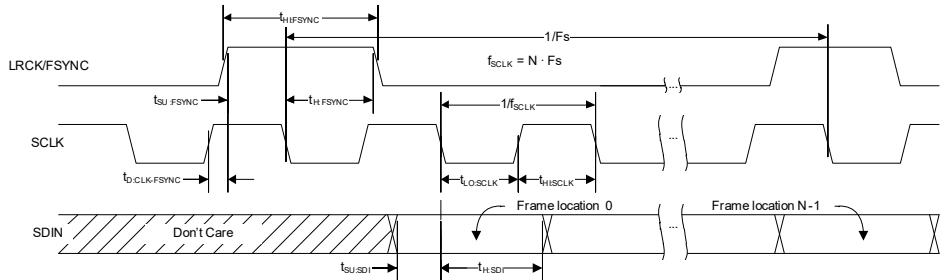
1. Output clock frequencies follow the internal master clock (MCLK_INT) frequency proportionally. Any deviation of the clock source from the nominal supported rates are directly imparted to the output clock rate by the same factor (e.g., +100-ppm offset in the frequency of MCLK_INT becomes a +100-ppm offset in LRCK/FSYNC and SCLK).

2. I₂S interface timing



3. TDM interface timing

(shown with xSP_FSD = 010, xSP_LCHI = 1)



4. Applies to Master and Slave Modes, unless specified otherwise.

5. Maximum LRCK duty cycle is equal to frame length, in SCLK periods, minus 1. Maximum duty cycle occurs when LRCK high (xSP_LCHI) is set to 768 SCLK periods and LRCK period (xSP_LCPR) is set to 769 SCLK periods.

6. Data may be latched/launched on either the rising or falling edge of SCLK.

7. SCLK duty cycle in Master Mode depends on Master Mode clock configuration, and can vary by up to 1 MCLK_INT period.

8. Data is latched/launched on the rising or falling edge of SCLK as determined by xSP_SCPOL_OUT, xSP_SCPOL_IN, and xSP_FSD bits. See the SCLK launching specs in Table 3-20.

Table 3-21. DSD Switching Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43131 connections; GNDA = GNDP = GNDD = 0 V; voltages are with respect to ground; parameters can vary with VL; typical performance data taken with VL = VD = VA = VCP = 1.8 V, VP = 3.6 V; min/max performance data taken with VL = 1.8 V; VD = VA = VCP = 1.8 V, VP = 3.6 V; TA = +25°C; CL = 60 pF; Logic 0 = ground, Logic 1 = VL; output timings are measured at VO_{OL} and VO_{OH} thresholds (see Table 3-13).

Parameter 1,2	Symbol	Minimum	Typical	Maximum	Units
DSDCLK duty cycle	—	40	—	60	%
DSDCLK pulse width low	t _{SCLKL}	40	—	—	ns
DSDCLK pulse width high	t _{SCLKH}	40	—	—	ns
DSDCLK frequency (64× oversampled) (128× oversampled) (256× oversampled)	—	1.024 2.048 4.096	2.8224 5.6448 11.2897	f _{MCLK_INT} /8 f _{MCLK_INT} /4 f _{MCLK_INT} /2	MHz MHz MHz
DSDA/DSDB valid to DSDCLK rising setup time	t _{SDLRS}	10	—	—	ns
DSDCLK rising to DSDA or DSDB hold time	t _{SDH}	10	—	—	ns
DSD clock to data transition (Phase Modulation Mode) (64× oversampled) (128× oversampled)	t _{DPM}	-20 -10	—	20 10	ns ns

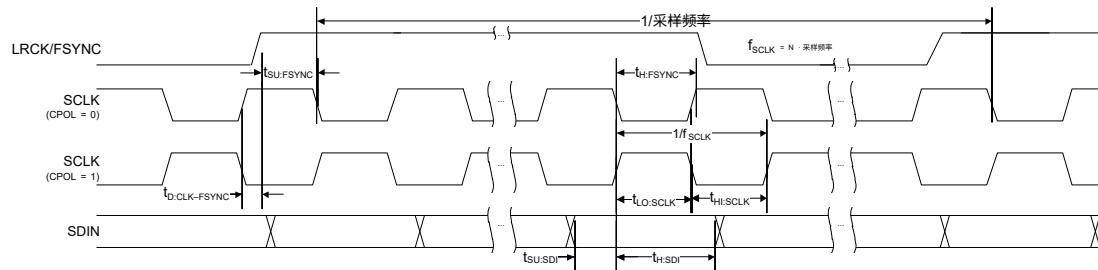
表 3-20. 串行接口特性 (续)

测试条件 (除非另有说明) : 图 2-1 显示 CS43131 连接; GNDA = GNDP = GNDD = 0 V; 电压均相对于接地;
 参数可能随 VL 变化; 典型性能数据采集条件为 VL = VD = VA = VCP = 1.8 V, VP = 3.6 V; 最小/最大性能数据采集条件为 VL = 1.8 V; VD = VA = VCP = 1.8 V, VP = 3.6 V; TA = +25°C; CL = 60 pF; 逻辑0 = 接地, 逻辑1 = VL; 输出时序在VOL和VOH阈值处测量 (见表3-13)。

参数 1,2,3,4		符号	最小值	典型	最大值	单位
从属模式	FSYNC 在 SCLK 锁存沿前的建立时间 6	tSU:FSYNC	10	—	—	纳秒
	FSYNC 在 SCLK 锁存沿后的保持时间 6	tH:FSYNC	5	—	—	纳秒
	SCLK 频率	fSCLK	—	—	24.58	MHz
	SCLK 高电平周期	tHI:SCLK	16	—	—	纳秒
	SCLK 低电平周期	tLO:SCLK	16	—	—	纳秒
	SDIN 在 SCLK 锁存边沿前的建立时间 8	tSU:SDI	10	—	—	纳秒
	SDIN 在 SCLK 锁存沿后的保持时间 6	tH:SDI	5	—	—	纳秒

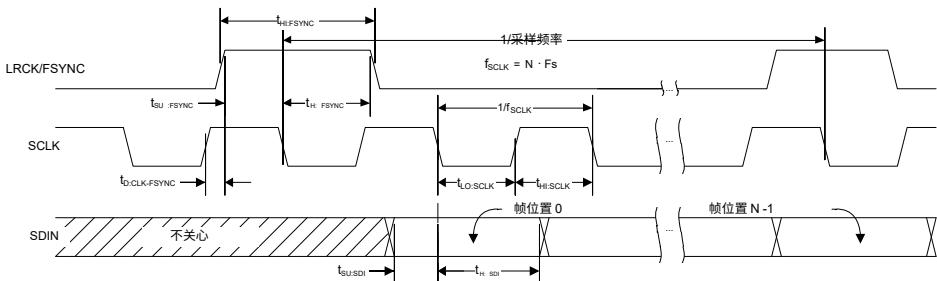
1. 输出时钟频率与内部主时钟 (MCLK_INT) 频率成比例。时钟源相对于标称支持频率的任何偏差, 都会以相同的比例直接影响输出时钟频率 (例如, MCLK_INT 频率的 +100 ppm 偏移将导致 LRCK/FSYNC 和 SCLK 频率出现 +100 ppm 偏移)。

2.I2S 接口时序



3. TDM 接口时序

(显示为 xSP_FSD = 010, xSP_LCHI = 1)



4. 适用于主模式和从模式, 除非另有说明。

5. 最大 LRCK 占空比等于帧长度 (以 SCLK 周期计) 减 1。最大占空比发生在 LRCK 高电平 (xSP_LCHI) 设置为 768 个 SCLK 周期且 LRCK 周期 (xSP_LCPR) 设置为 769 个 SCLK 周期。

6. 数据可在 SCLK 的上升沿或下降沿锁存/发送。

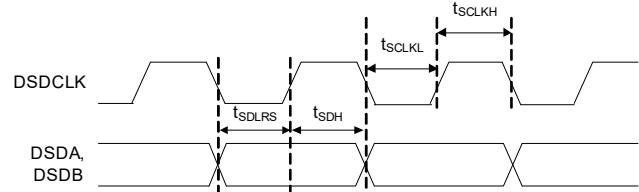
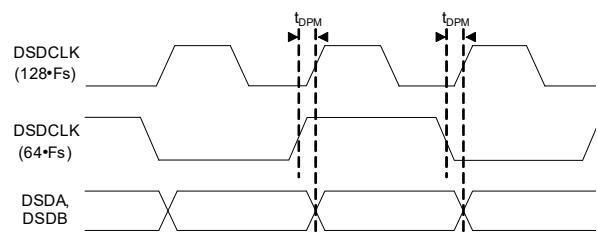
7. 主模式下 SCLK 的占空比取决于主模式时钟配置, 且可变化最多 1 个 MCLK_INT 周期。

8. 数据在 SCLK 的上升沿或下降沿锁存/发送, 具体由 xSP_SCPOL_OUT、xSP_SCPOL_IN 和 xSP_FSD 位决定。详见表3-20中的SCLK发送规范。

表 3-21. DSD 切换特性

测试条件 (除非另有说明) : 图 2-1 显示 CS43131 连接; GNDA = GNDP = GNDD = 0 V; 电压均相对于接地;
 参数可能随 VL 变化; 典型性能数据采集条件为 VL = VD = VA = VCP = 1.8 V, VP = 3.6 V; 最小/最大性能数据采集条件为 VL = 1.8 V; VD = VA = VCP = 1.8 V, VP = 3.6 V; TA = +25°C; CL = 60 pF; 逻辑0 = 接地, 逻辑1 = VL; 输出时序在VOL和VOH阈值处测量 (见表3-13)。

参数 1,2	符号	最小值	典型	最大值	单位
DSDCLK 占空比	—	40	—	60	%
DSDCLK 脉冲宽度低电平	tSCLKL	40	—	—	纳秒
DSDCLK 脉冲宽度高电平	tSCLKH	40	—	—	纳秒
DSDCLK 频率 (64×过采样) (128×过采样) (256×过采样)	—	1.024 2.048 4.096	2.8224 5.6448 11.2897	$f_{MCLK_INT}/8$ $f_{MCLK_INT}/4$ $f_{MCLK_INT}/2$	MHz MHz MHz
DSDA/DSDB 对 DSDCLK 上升沿的建立时间有效	tSDLRS	10	—	—	纳秒
DSDCLK 上升沿至 DSDA 或 DSDB 的保持时间	tSDH	10	—	—	纳秒
DSD 时钟到数据转换 (相位调制模式) (64×过采样) (128×过采样)	tDPM	-20 -10	—	20 10	ns ns

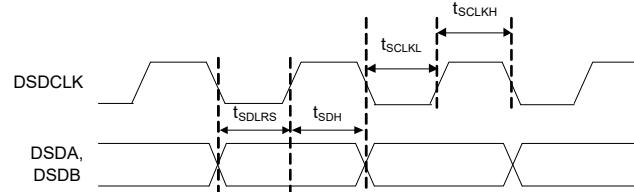
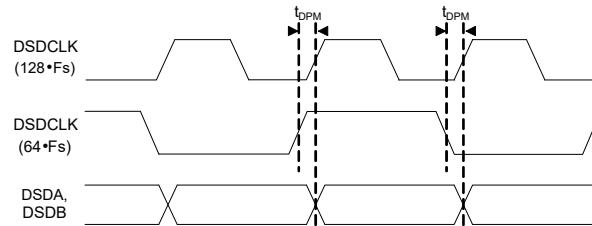
1. Serial audio input interface timing

2. Phase modulation mode serial audio input interface timing

Table 3-22. I²C Slave Port Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections; Inputs: GNDA = GNDL = GNDCP = 0 V; all voltages with respect to ground; VL = 1.8 V; inputs: Logic 0 = GNDA = 0 V, Logic 1 = VL; TA = +25°C; SDA load capacitance equal to maximum value of CB = 400 pF; minimum SDA pull-up resistance, RP(min);¹ Table 3-1 describes some parameters in detail. All specifications are valid for the signals at the pins of the CS43131 with the specified load capacitance.

Parameter ²	Symbol ³	Minimum	Maximum	Units
SCL clock frequency	f _{SCL}	—	1000	kHz
Clock low time	t _{LOW}	500	—	ns
Clock high time	t _{HIGH}	260	—	ns
Start condition hold time (before first clock pulse)	t _{HDST}	260	—	ns
Setup time for repeated start	t _{SUST}	260	—	ns
Rise time of SCL and SDA	t _{RC}	—	1000	ns
		—	300	ns
		—	120	ns
Fall time of SCL and SDA	t _{FC}	—	300	ns
		—	300	ns
		—	120	ns
Setup time for stop condition	t _{SUSP}	260	—	ns
SDA setup time to SCL rising	t _{SUD}	50	—	ns
SDA input hold time from SCL falling ⁴	t _{HDDI}	0	—	ns
Output data valid (Data/Ack) ⁵	t _{VDDO}	—	3450	ns
		—	900	ns
		—	450	ns
Bus free time between transmissions	t _{BUF}	500	—	ns
SDA bus capacitance	C _B	—	340	pF
		—	400	pF
SCL/SDA pull-up resistance ¹	V _L = 1.8 V	R _P	350	Ω
Pulse width of spikes to be suppressed	t _{PS}	—	50	ns
Switching time between RCO and MCLK_INT ⁶	—	150	—	μs
Power-up delay (delay before I ² C can communicate after RESET released)	t _{PUD}	1500	—	μs

1. The minimum R_P value (resistor shown in Fig. 2-1) is determined by using the maximum level of VL, the minimum sink current strength of its respective output, and the maximum low-level output voltage V_{OL}. The maximum R_P value may be determined by how fast its associated signal must transition (e.g., the lower the value of R_P, the faster the I²C bus is able to operate for a given bus load capacitance). See I²C bus specification referenced in Section 13.

2. All timing is relative to thresholds specified in Table 3-13, V_{IL} and V_{IH} for input signals, and V_{OL} and V_{OH} for output signals.

1. 串行音频输入接口时序

2. 相位调制模式串行音频输入接口时序

表 3-22. I²C 从属端口特性

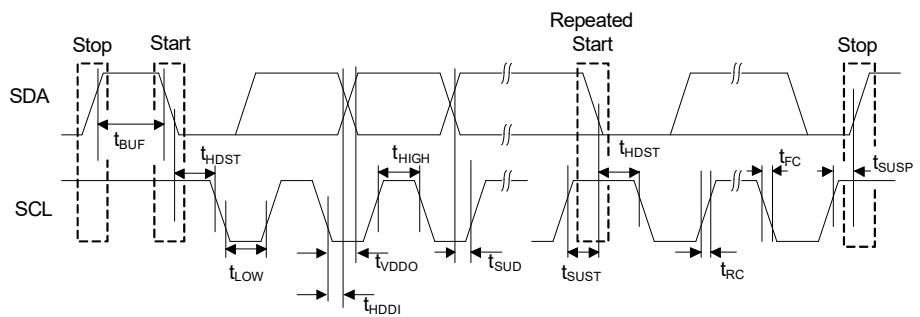
测试条件（除非另有说明）：图 2-1 显示典型连接；输入：GND_A = GND_L = GND_{CP} = 0 V；所有电压均相对于接地；V_L = 1.8 V；输入：逻辑 0 = GND_A = 0 V，逻辑 1 = V_L；T_A = +25°C；SDA 负载电容等于最大值 C_B = 400 pF；最小 SDA 上拉电阻 R_{P(min)}。表 3-1 详细描述部分参数。所有规格均适用于 CS43131 引脚上的信号及指定的负载电容。

参数 ²	符号 ³	最小值	最大值	单位
SCL 时钟频率	f _{SCL}	—	1000	kHz
时钟低电平时间	t _{LOW}	500	—	纳秒
时钟高电平时间	t _{HIGH}	260	—	纳秒
起始条件保持时间（首次时钟脉冲前）	t _{HDST}	260	—	纳秒
重复起始建立时间	t _{SUST}	260	—	纳秒
SCL 和 SDA 的上升时间	标准模式 快速模式 快速模式 Plus	t _{RC}	— — —	纳秒 纳秒 纳秒
SCL 和 SDA 的下降时间	标准模式 快速模式 快速模式 Plus	t _{FC}	— — —	纳秒 纳秒 纳秒
停止条件建立时间	t _{SUSP}	260	—	纳秒
SDA 对 SCL 上升沿的建立时间	t _{SUD}	50	—	纳秒
SDA 输入保持时间（自 SCL 下降沿起） ⁴	t _{HDDI}	0	—	纳秒
输出数据有效时间（数据/应答） ⁵	标准模式 快速模式 快速模式 Plus	t _{VDDO}	— — —	纳秒 纳秒 纳秒
传输间总线空闲时间	t _{BUF}	500	—	纳秒
SDA 总线电容	SCL 频率 = 1 MHz, V _L = 1.8 V SCL 频率 ≤ 400 kHz	C _B	— —	340 pF 400 pF
SCL/SDA 上拉电阻 ¹	V _L = 1.8 V	R _P	350	— Ω
需抑制脉冲宽度	t _{PS}	—	50	纳秒
RCO 与 MCLK_INT 之间的切换时间 ⁶	—	t _{PUD}	150	— μs
上电延迟（复位释放后 I ² C 可通信的延迟）	—	t _{PUD}	1500	— μs

1. 最小的 R_P 值（如图 2-1 所示的电阻）是根据最大电平 V_L、对应输出的最小吸收电流强度及最大低电平输出电压 V_{O(L)} 确定的。最大 R_P 值取决于其相关信号的转换速度（例如，R_P 值越低，在给定总线负载电容下，I²C 总线的运行速度越快）。详见第 13 节引用的 I²C 总线规范。

2. 所有时序均相对于表 3-13 中规定的阈值，输入信号的 V_{I(L)} 和 V_{I(H)}，以及输出信号的 V_{O(L)} 和 V_{O(H)}。

3. I²C control-port timing

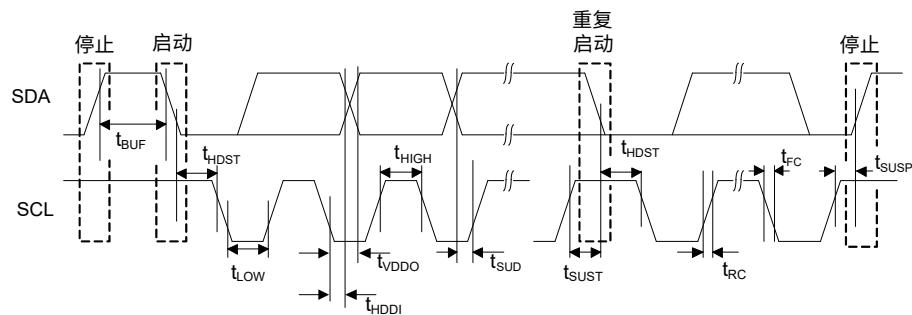


4. Data must be held long enough to bridge the transition time, t_F , of SCL.

5. Time from falling edge of SCL until data output is valid.

6. Upon setting MCLK_SRC_SEL and sending the I²C stop condition, the switching of RCO and other MCLK_INT sources occurs. A least wait time as specified is required after changing MCLK_SRC_SEL and sending the I²C stop condition before the next I²C transaction is initiated.

3.I²C 控制端口时序



4. 数据必须保持足够长的时间，以覆盖SCL的转换时间 t_F 。

5. 从SCL下降沿到数据输出有效的时间。

6. 设置MCLK_SRC_SEL并发送I²C停止条件后，RCO及其他MCLK_INT源将切换。更改MCLK_SRC_SEL并发送I²C停止条件后，启动下一次I²C事务前，需满足规定的最短等待时间。

4 Functional Description

This section describes the general theory of operation of the CS43131, tracing the signal and control flow through the various blocks within the device. It comprises the following sections:

- [Section 4.1, “Overview”](#)
- [Section 4.2, “Analog Outputs”](#)
- [Section 4.3, “Class H Amplifier Output”](#)
- [Section 4.4, “Alternate Headphone Inputs”](#)
- [Section 4.5, “Headphone Presence Detect and Output Load Detection”](#)
- [Section 4.6, “Clocking Architecture”](#)
- [Section 4.7, “Clock Output and Fractional-N PLL”](#)
- [Section 4.8, “Filtering Options”](#)
- [Section 4.9, “Audio Serial Port \(ASP\)”](#)
- [Section 4.10, “DSD Interface”](#)
- [Section 4.11, “DSD and PCM Mixing”](#)
- [Section 4.12, “Standard Interrupts”](#)
- [Section 4.13, “Control Port Operation”](#)
- [Section 4.14, “Programmable Filter”](#)

4.1 Overview

4.1.1 Analog Outputs

The analog output block includes separate pseudodifferential headphone Class H amplifiers output. An on-chip inverting charge pump creates a positive and negative voltage equal to the input, allowing an adaptable, full-scale output swing centered around ground. The resulting internal amplifier supply can be $\pm V_{CP}$, or $\pm V_{P_LDO}$ (either ± 3.0 V with $HV_EN = 1$ or ± 2.6 V with $HV_EN = 0$).

The inverting architecture eliminates the need for large DC-blocking capacitors and allows the amplifier to deliver more power to HP loads at lower supply voltages. This adaptive power supply scheme converts traditional Class AB amplifiers into more power-efficient Class H amplifiers.

4.1.2 Alternate Headphone Inputs

The alternate headphone inputs provide an integrated selectable path to interface between the system codec output and the headphone connector, which allows for lower-power operation in applications such as voice or compressed music playback. These inputs eliminate the need for an external audio switch and prevent the high-fidelity headphone outputs of CS43131 from degradation by the external audio switch.

4.1.3 Headphone Detection

The CS43131 detects the presence of a headphone and notifies the application processor to wake up through an interrupt event.

4.1.4 Headphone Impedance Measurement

The CS43131 detects headphone impedance information at low frequencies, which can be used to adjust the system properly to accommodate different load conditions. One example is to adjust signal chain gain to avoid distortion.

The CS43131 also provides impedance measurement functions to evaluate the headphone load within 20 Hz to 20 kHz. A specific frequency is selected and the impedance measurement process is initiated by setting the register. Through a series of interrupt events, the CS43131 notifies application processor to retrieve the impedance information after completion.

4 功能描述

本节介绍CS43131的一般工作原理，追踪信号和控制流经器件各模块的过程。内容包括以下章节：

- 第4.1节，“概述”
- 第4.2节，“模拟输出”
- 第4.3节，“Class H放大器输出”
- 第4.4节，“备用耳机输入”
- 第4.5节，“耳机存在检测及输出负载检测”
- 第4.6节，“时钟架构”
- 第4.7节，“时钟输出及分数-N PLL”
- 第4.8节，“滤波选项”
- 第4.9节，“音频串行端口（ASP）”
- 第4.10节，“DSD接口”
- 第4.11节，“DSD与PCM混合”
- 第4.12节，“标准中断”
- 第4.13节，“控制端口操作”
- 第4.14节，“可编程滤波器”

4.1 概述

4.1.1 模拟输出

模拟输出模块包括独立的伪差分耳机Class H放大器输出。片内反相电荷泵产生与输入电压相等的正负电压，实现以接地为中心的可调满量程输出摆幅。由此产生的内部放大器电源可为 $\pm V_{CP}$ ，或 $\pm V_{P_LDO}$ （高压使能 = 1时为 $\pm 3.0\text{ V}$ ，高压使能 = 0时为 $\pm 2.6\text{ V}$ ）。

反相架构消除了对大型直流隔离电容的需求，使放大器能够在较低电源电压下向耳机负载提供更大功率。该自适应电源方案将传统的AB类放大器转换为更高效的H类放大器。

4.1.2 备用耳机输入

备用耳机输入提供了一个集成的可选路径，用于连接系统编解码器输出与耳机接口，支持在语音或压缩音乐播放等应用中实现低功耗运行。这些输入消除了外部音频开关的需求，避免外部音频开关对CS43131高保真耳机输出性能的影响。

4.1.3 耳机检测

CS43131能够检测耳机的插入状态，并通过中断事件通知应用处理器唤醒。

4.1.4 耳机阻抗测量

CS43131在低频下检测耳机阻抗信息，可用于系统的适当调整以适应不同负载条件。一个示例是调整信号链增益以避免失真。

CS43131还提供阻抗测量功能，可在20 Hz至20 kHz范围内评估耳机负载。

通过选择特定频率并设置寄存器启动阻抗测量过程。通过一系列中断事件，CS43131在完成后通知应用处理器获取阻抗信息。

4.1.5 Audio Interfaces and Supported Formats

There are two serial input ports on the CS43131, the audio serial port (ASP) and the auxiliary serial port (XSP). The ASP on the CS43131 supports I²S, TDM, and DoP (DSD over PCM) formats up to a 384-kHz sample rate. The XSP on the CS43131 supports the DoP format up to a 352.8-kHz sample rate.

The CS43131 also has a dedicated DSD interface to support up to a 256•Fs DSD stream. The DSD interface shares pins with the XSP.

4.1.6 System Clocking

The CS43131 internal MCLK can be sourced from three options:

- Direct MCLK/crystal mode. The internal MCLK is provided through XTI/MCLK pin directly or generated by crystal oscillator.
- PLL mode. A PLL reference CLK is provided by externally through XTI/MCLK. The PLL is configured, and output is used as the internal MCLK.
- RCO mode. An internal RCO is used as the internal MCLK. Note that HPIN input path is the only supported audio playback feature in this mode for optimized power consumption. This mode can also support HP detection and I²C communication. DAC playback and headphone impedance measurement functions are not supported.

The clock output is provided for audio applications that require high quality audio rate system clock. This clock output can be sourced from the following two options:

- The clock generated by the CS43131 crystal oscillator.
- Output of the internal Fractional-N PLL that refers to MCLK input. See [Section 4.7.1](#) for supported frequencies.

The internal MCLK is used to generate serial port clocks. See [Table 4-6](#) for supported LRCK combinations.

4.1.7 System Interrupts

The CS43131 includes an open-drain interrupt output (INT pin). Interrupt mask registers control whether an event associated with an interrupt status/mask bit pair triggers the assertion of INT. All types of interrupt are described in [Section 4.11](#).

4.1.8 System Reset

The CS43131 offers two types of reset options:

- Asserting RESET. If RESET is asserted, all registers and state machines are immediately set to their default values/states. No operation can begin until RESET is deasserted. Before normal operation can begin, RESET must be asserted at least once after the VP supply is first brought up.
- Power-on reset (POR). If the VD supply is lower than the POR threshold specified in [Table 3-18](#), all registers and state machines are set to their default values/states. The POR releases the reset when the VD supply goes above the POR threshold. When the VD supply is turned on, the VL and VA supplies must also be turned on at the same time.

4.1.9 Power Down

The CS43131 has a register to power down individual components on the chip. Before any change can be applied to an individual component (except PLL), the block must be powered down first. For the PLL, changes can be applied after PLL_START is cleared.

The PDN_HP bit is responsible for enabling or disabling the signal chain playback operation. Setting PDN_HP disables signal chain playback operation. All the necessary components for playback operation need to be powered up and configured properly before PDN_HP is cleared. PDN_HP needs to be set before making any changes to the playback signal chain setup, except the following functions:

- Volume and mute related functions
- PCM filter settings (see [Section 7.5.2](#))

4.1.5 音频接口及支持格式

CS43131设有两个串行输入端口，分别为音频串行端口（ASP）和辅助串行端口（XSP）。CS43131的ASP支持I²S、TDM及DoP（DSD over PCM）格式，最高采样率达384 kHz。CS43131的XSP支持DoP格式，最高采样率达352.8 kHz。

CS43131还配备专用DSD接口，支持最高256•Fs的DSD流。DSD接口与XSP共用引脚。

4.1.6 系统时钟

CS43131 内部 MCLK 可由三种方式提供：

- 直接 MCLK/晶体模式。内部 MCLK 通过 XTI/MCLK 引脚直接提供，或由晶体振荡器生成。
- PLL 模式。PLL 参考时钟由外部通过 XTI/MCLK 提供。PLL 配置完成后，其输出作为内部 MCLK。
- RCO 模式。内部 RCO 用作内部 MCLK。注意，该模式下仅支持 HPIN 输入路径的音频播放功能，以优化功耗。该模式还支持耳机检测和 I²C 通信。不支持 DAC 播放和耳机阻抗测量功能。

时钟输出用于需要高质量音频采样率系统时钟的音频应用。该时钟输出可由以下两种方式提供：

- 由 CS43131 晶体振荡器生成的时钟。
- 参考 MCLK 输入的内部 Fractional-N PLL 输出。有关支持的频率，请参见第4.7.1节。

内部MCLK用于生成串行端口时钟。有关支持的LRCK组合，请参见表4-6。

4.1.7 系统中断

CS43131包含一个开漏中断输出（INT引脚）。中断屏蔽寄存器控制与中断状态/屏蔽位对相关的事件是否触发INT信号。所有类型的中断均在第4.11节中描述。

4.1.8 系统复位

CS43131提供两种复位选项：

- 断言复位（RESET）。如果复位被断言，所有寄存器和状态机将立即恢复到默认值/状态。在复位解除之前，任何操作均无法开始。在正常操作开始之前，复位必须在VP电源首次上电后至少断言一次。
- 上电复位（POR）。如果VD电源低于表3-18中规定的POR阈值，所有寄存器和状态机将恢复到默认值/状态。当VD电源电压超过POR阈值时，POR释放复位。当VD电源开启时，VL和VA电源必须同时开启。

4.1.9 断电

CS43131具有用于单独关闭芯片内各组件电源的寄存器。在对单个组件（PLL除外）进行任何更改之前，必须先关闭该模块电源。对于PLL，更改可在PLL_START清除后应用。

PDN_HP位负责启用或禁用信号链播放操作。设置PDN_HP将禁用信号链播放操作。在清除PDN_HP之前，所有播放操作所需的组件必须上电并正确配置。在对播放信号链设置进行任何更改之前，必须先设置PDN_HP，以下功能除外：

- 音量和静音相关功能
- PCM滤波器设置（参见第7.5.2节）

Before ASP, XSP, or DSDIF can be safely powered down, PDN_HP must be asserted, and PDN_DONE_INT must be present. For XTAL or PLL used as the source of internal MCLK, PDN_HP needs to be set first and MCLK source needs to be properly switched away before PDN_XTAL or PDN_PLL is set. If PLL output is only used as the source of CLKOUT, PDN_PLL can be set without PDN_HP being asserted. If the steps described above are not followed, the CS43131 enters an unresponsive state.

PDN_CLKOUT does not require PDN_HP to be set before it is enabled.

PDN_HP should be set before using headphone input path and load detection function. Refer to the functional description of these two components for further details.

Recommended power-up and power-down sequences can be found in the [Section 5.2](#).

在安全关闭ASP、XSP或DSDIF电源之前，必须断言PDN_HP，并且必须存在PDN_DONE_INT。对于用作内部MCLK源的晶体振荡器或PLL，需先设置PDN_HP，并在设置PDN_XTAL或PDN_PLL之前正确切换MCLK源。如果PLL输出仅用作CLKOUT的源，则可在未断言PDN_HP的情况下设置PDN_PLL。如果未遵循上述步骤，CS43131将进入无响应状态。

启用PDN_CLKOUT前无需先设置PDN_HP。

使用耳机输入路径和负载检测功能前，应先设置PDN_HP。有关这两个组件的详细信息，请参阅其功能描述。

推荐的上电和断电顺序详见第5.2节。

4.2 Analog Outputs

The CS43131 provides an analog output that is derived from the digital audio input ports. This section describes the general flow of the analog outputs.

4.2.1 Analog Output Signal Flow

The CS43131 signal flow is shown in Fig. 4-1.

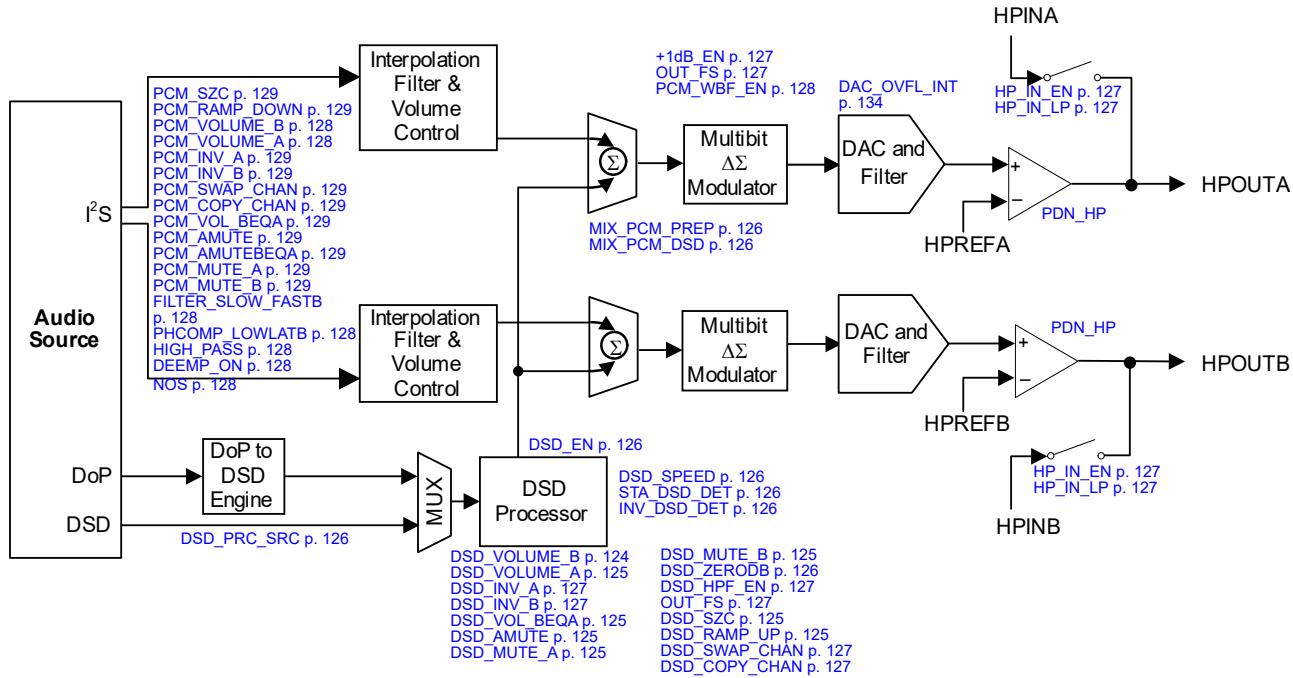


Figure 4-1. Analog Output Signal Flow

The CS43131 has 4 settings of full scale voltage, which are determined by OUT_FS[1:0]. When OUT_FS[1:0] = 11 and HV_EN = 1, the +1dB_EN bit can boost the output voltage to 2 V_{rms}. In any other setting combination of OUT_FS[1:0] and HV_EN, the +1dB_EN bit is ignored. The proper full scale voltage must be set first, and the digital volume settings is used to control signal levels.

The CS43131 digital volume control allows independent control of the signal level in 1/2 dB increments from 0 dB (0b0000 0000) to -127 dB (0b1111 1110) by using x_VOLUME_y (where "x" is either PCM or DSD; "y" is either A or B) register. When the x_VOL_BEQA bit is set, both volumes can be changed simultaneously using x_VOLUME_A. The volume changes are implemented as dictated by PCM_SZC[1:0] and DSD_SZC in the signal control register (see [Section 7.4.3](#) and [Section 7.5.5](#)). If soft ramping is enabled, gain and attenuation changes are carried out by incrementally changing the volume level in 1/8-dB steps, from the previous level to the new level. For PCM, when PCM_SZC[1:0] = 2, the volume level changes at an approximate rate of 1 dB/ms. The volume level also changes at a rate of 1 dB/ms for DSD. Both channels can be inverted independently by setting the INV_A and INV_B bits. Both channels can be swapped by setting the x_SWAP_CHAN bit. Channel A content can be copied to channel B by setting the x_COPY_CHAN bit. Mono mode can be enabled with proper setting of these bits.

The CS43131 provides individual ramp-up and ramp-down control options (from the global soft ramp settings) for two specific scenarios. The PCM_RAMP_DOWN bit is for the scenario when the interpolation filter configuration switches (as configured by the PCM Filter Option register) during PCM playback. DSD_RAMP_UP bit is for the scenario when DSD playback recovers from detected DSD stream errors. Refer to each individual register description for setting details.

The CS43131 can mute both channels simultaneously or independently. Also, it can auto-mute on both PCM stream and DSD stream when mute pattern is identified (defined in PCM_AMUTE and DSD_AMUTE). Additional signal and mute control options can be found in [Section 7.4.3](#) and [Section 7.5.5](#).

4.2 模拟输出

CS43131提供基于数字音频输入端口的模拟输出。本节描述模拟输出的一般流程。

4.2.1 模拟输出信号流程

CS43131信号流程如图4-1所示。

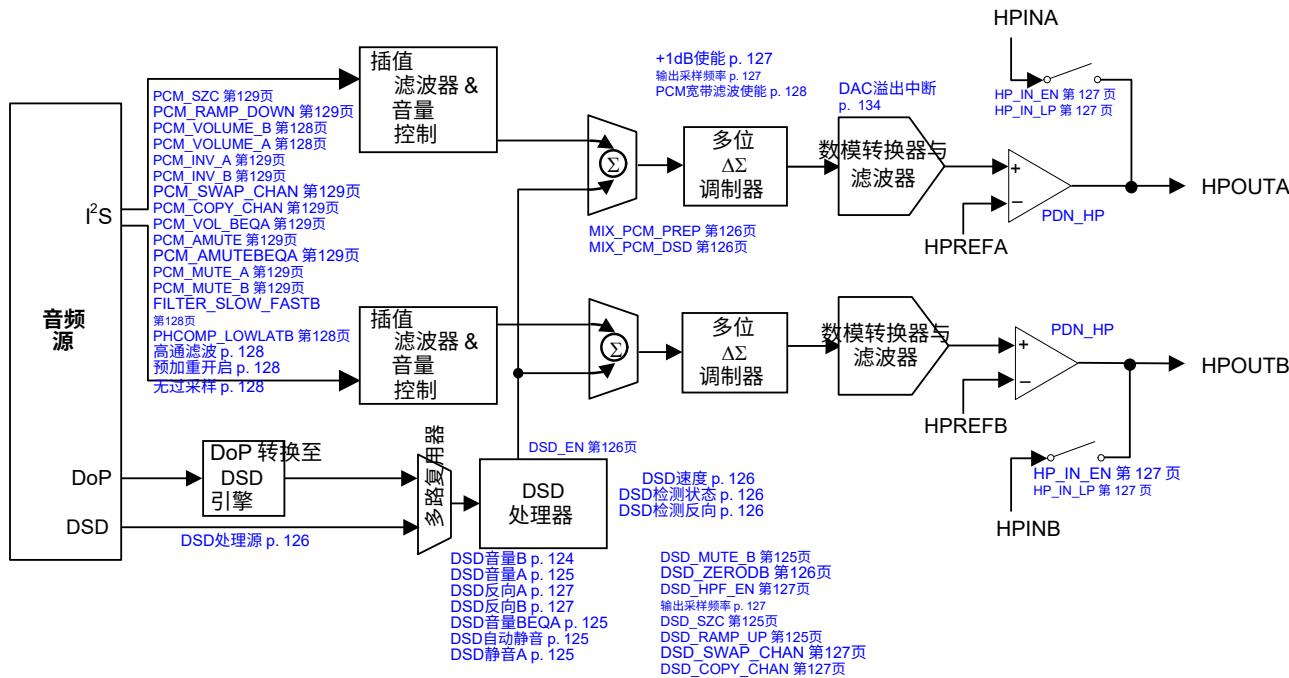


图 4-1. 模拟输出信号流程

CS43131 具有 4 种满量程电压设置，由 OUT_FS[1:0] 决定。当 OUT_FS[1:0] = 11 且高压使能 = 1 时，+1dB_EN 位可将输出电压提升至 2 V_{rms}。在 OUT_FS[1:0] 和高压使能 的其他任何设置组合中，+1dB_EN 位将被忽略。必须先设置正确的满量程电压，数字音量设置用于控制信号电平。

CS43131 数字音量控制允许通过 x_VOLUME_y 寄存器（其中 “x” 为 PCM 或 DSD，“y” 为 A 或 B）以 1/2 dB 递增独立控制信号电平，范围从 0 dB (0b0000 0000) 到 -127 dB (0b1111 1110)。当设置 x_VOL_BEQA 位时，可通过 x_VOLUME_A 同时调整两个音量。音量变化依据信号控制寄存器中的 PCM_SZC[1:0] 和 DSD_SZC 规定执行（详见第 7.4.3 节和第 7.5.5 节）。若启用软斜坡，增益和衰减变化将以 1/8 dB 步进逐渐调整音量级别，从先前级别过渡至新级别。对于 PCM，当 PCM_SZC[1:0] = 2 时，音量级别变化速率约为 1 dB/ms；对于 DSD，变化速率亦为 1 dB/ms。通过设置 INV_A 和 INV_B 位，可独立反转两个通道；设置 x_SWAP_CHAN 位可交换两个通道；设置 x_COPY_CHAN 位可将通道 A 内容复制至通道 B。适当设置上述位后，可启用单声道模式。

CS43131 提供针对两种特定场景的独立上升斜坡和下降斜坡控制选项（基于全局软斜坡设置）。PCM_RAMP_DOWN 位用于 PCM 播放过程中插值滤波器配置切换的场景（由 PCM Filter Option 寄存器配置）。DSD_RAMP_UP 位用于 DSD 播放从检测到的 DSD 流错误中恢复的场景。有关设置详情，请参阅各寄存器描述。

CS43131 可同时或独立静音两个声道。此外，当检测到静音模式（在 PCM_AMUTE 和 DSD_AMUTE 中定义）时，可自动对 PCM 流和 DSD 流进行静音。更多信号和静音控制选项详见第 7.4.3 节和第 7.5.5 节。

The CS43131 has an independent set of controls for the DSD processor path as shown in [Fig. 4-1](#). The DSD processor also offers the control bit SIGCTL_DSDEQPCM, which maps the PCM_x setting to DSD_x setting, once enabled. As a result, some of the DSD_x register settings are ignored. The registers affected are DSD_RAMP_UP, DSD_VOL_BEQA, DSD_SZC, DSD_AMUTE, DSD_AMUTE_BEQA, DSD_MUTE_A, DSD_MUTE_B, DSD_INV_A, DSD_INV_B, DSD_SWAP_CHAN, and DSD_COPY_CHAN. Refer to [Section 7.4.1–Section 7.4.7](#) for control register details.

4.2.2 Wideband Flatness Mode

The CS43131 specifically optimizes for wideband flatness playback, which is enabled by PCM_WBF_EN bit. This mode should only be enabled when PCM plays back at 192 kHz. When operating in other speeds or modes, this bit should be properly disabled. If wideband flatness mode enabled, the filter spec complies to [Table 3-10](#). There is no option for filter roll-off or phase response in this mode. NOS filter mode should be disabled for proper operation. Note that wideband flatness mode can only be enabled or disabled when PDN_HP is set.

4.2.3 Mono Mode

The CS43131 supports mono (differential) mode playback. Mono mode allows driving a differential interconnect such as a XLR connector or implementing a stereo differential headphone utilizing two CS43131 devices. [Fig. 2-2](#) shows a typical connection of the CS43131 to a XLR connector in mono mode.

4.3 Class H Amplifier Output

[Fig. 4-2](#) shows the Class H operation.

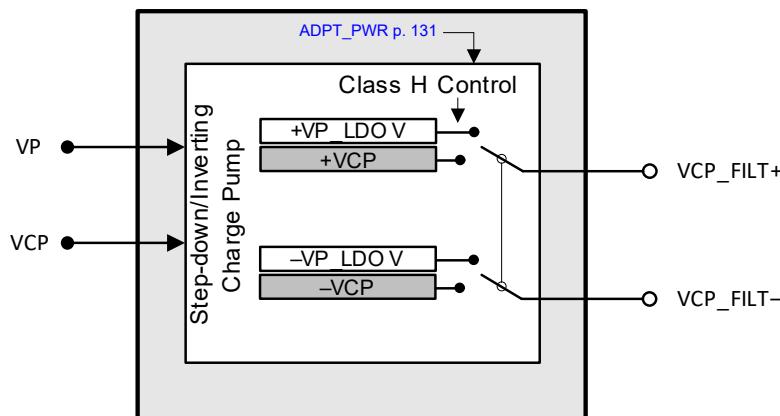


Figure 4-2. Class H Operation

The CS43131 headphone output amplifiers use Cirrus Logic two-mode Class H technology. This technology maximizes operating efficiency of the typical Class AB amplifier while maintaining high performance. In a Class H amplifier design, the rail voltages supplied to the amplifier vary with the needs of the music passage that is being amplified. This prevents unnecessarily wasting energy during low power passages of program material or when the program material is played back at a low volume level.

The internal charge pump, which creates the rail voltages for the headphone amplifiers, is the central component of the two-mode Class H technology implemented in the CS43131. The charge pump receives its input voltage from the voltage present on the VCP or VP pin. From this input voltage, the charge pump creates the differential rail voltages supplied to the amplifier output stages. The charge pump can supply two sets of differential rail voltages: $\pm VCP_{LDO}$ and $\pm VP_{LDO}$.

CS43131 对 DSD 处理路径具有独立的控制集，如图4-1所示。DSD 处理器还提供控制位 SIGCTL_DSDEQPCM，启用后将 PCM_x 设置映射至 DSD_x 设置。因此，部分 DSD_x 寄存器设置将被忽略。受影响的寄存器包括 DSD_RAMP_UP、DSD_VOL_BEQA、DSD_SZC、DSD_AMUTE、DSD_AMUTE_BEQA、DSD_MUTE_A、DSD_MUTE_B、DSD_INV_A、DSD_INV_B、DSD_SWAP_CHAN 和 DSD_COPY_CHAN。有关控制寄存器的详细信息，请参见第7.4.1节至第7.4.7节。

4.2.2 宽带平坦模式

CS43131 专门针对宽带平坦播放进行了优化，该功能由 PCM_WBF_EN 位启用。此模式仅应在 PCM 以 192 kHz 播放时启用。在其他速率或模式下，应适当禁用该位。启用宽带平坦模式时，滤波器规格符合表 3-10。该模式下无滤波器滚降或相位响应选项。为确保正常运行，应禁用 NOS 滤波器模式。请注意，宽带平坦模式仅能在 PDN_HP 设定时启用或禁用。

4.2.3 单声道模式

CS43131 支持单声道（差分）模式播放。单声道模式允许驱动差分互连，如 XLR 连接器，或利用两个 CS43131 设备实现立体声差分耳机。图 2-2 显示了 CS43131 在单声道模式下连接至 XLR 连接器的典型示意图。

4.3 Class H 放大器输出

图 4-2 显示了 Class H 工作模式。

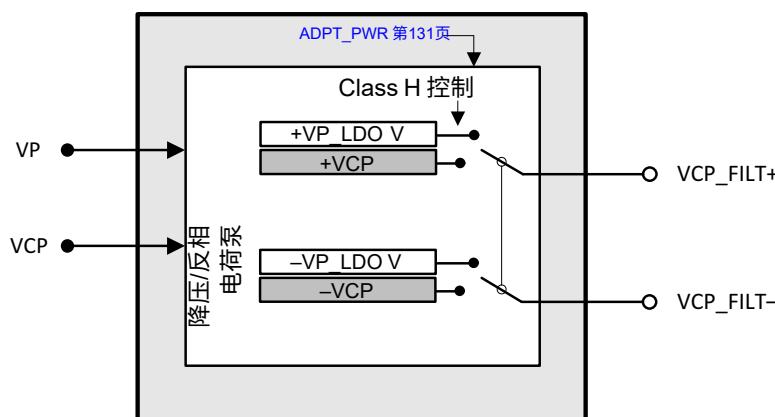


图 4-2. Class H 工作模式

CS43131 耳机输出放大器采用 Cirrus Logic 双模式 Class H 技术。该技术在保持高性能的同时，最大化典型 Class AB 放大器的工作效率。在 Class H 放大器设计中，供给放大器的轨电压会根据被放大的音乐片段需求而变化。这避免了在低功率音乐片段或以低音量播放节目材料时不必要的能量浪费。

内部电荷泵为耳机放大器产生轨电压，是 CS43131 中实现的双模式 Class H 技术的核心组件。电荷泵从 VCP 或 VP 引脚的电压输入获取电压，并由此产生供给放大器输出级的差分轨电压。电荷泵可提供两组差分轨电压： $\pm VCP$ 和 $\pm VP_LD$ O。

HV_EN setting, as shown in [Fig. 4-3](#), determines the VP_LDO voltage as shown in [Table 4-1](#). HV_EN = 1 setting is required to support the 1.7-V full-scale voltage for a 600- Ω load and above. In this setting, minimum VP is required to be higher than 3.3 V, and any load below 600 Ω is not supported. When HV_EN = 0, the max output voltage is 1.4-V RMS full-scale voltage. In this setting, minimum VP is required to be higher than 3 V, and the full headphone load range is supported.

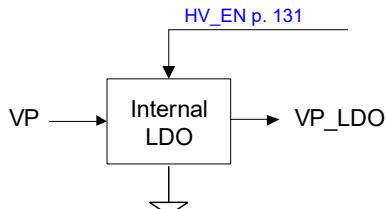


Figure 4-3. Internal LDO Configuration

Table 4-1. VP_LDO Voltage Per HV_EN Setting

HV_EN	VP_LDO Voltage
0	2.6 V
1	3.0 V

[Table 4-2](#) shows the nominal signal and volume level ranges when the output is set to the adapt modes explained in [Section 4.3.1](#). If the signal level is greater than the maximum value of this range, then clipping can occur.

Table 4-2. Class H Supply Modes

Mode	Class H Supply Level	Signal 1 or Volume Level Range 2,3,4
0	\pm VP_LDO V, internally regulated from VP	≥ -11 dB
1	\pm VCP	< -11 dB

1. In adapt-to-signal, the volume level ranges are approximations but are within -0.5 dB from the values shown.
2. Relative to digital full scale with output gain set to 0 dB.
3. In fixed modes, clipping can occur if the signal level exceeds the maximum of this range due to setting the amplifier's supply too low.
4. Thresholds shown are nominal for a 16- Ω stereo load.

4.3.1 Power Supply Control Options

This section describes the two types of operation: standard Class AB and adapt-to-output signal. The set of rail voltages supplied to the amplifier output stages depends on the [ADPT_PWR](#) (see [p. 131](#)) setting.

4.3.1.1 Standard Class AB Operation (ADPT_PWR = 001 or 010)

If ADPT_PWR is set to 001 or 010, the rail voltages supplied to the amplifiers are held to \pm VP_LDO or \pm VCP, respectively. The rail voltages supplied to the output stages are held constant, regardless of the output signal level. The CS43131 amplifiers simply operate in a traditional Class AB configuration.

4.3.1.2 Adapt-to-Output Signal (ADPT_PWR = 111)

If ADPT_PWR is set to 111, the rail voltage sent to the amplifiers is based solely on whether the signal sent to the amplifiers would cause the amplifiers to clip when operating on the lower set of rail voltages at certain threshold values.

- If it would cause clipping, the control logic instructs the charge pump to provide the next higher set of rail voltages to the amplifiers.
- If it would not cause clipping, the control logic instructs the charge pump to provide the lower set of rail voltages to the amplifiers, eliminating the need to advise the CS43131 of volume settings external to the device.

高压使能设置，如图4-3所示，决定了表4-1中显示的VP_LDO电压。高压使能 = 1 设置用于支持 600Ω 及以上负载的1.7 V满量程电压。在此设置下，最低VP需高于3.3 V，且不支持低于 600Ω 的任何负载。当高压使能 = 0时，最大输出电压为1.4 V RMS满量程电压。在此设置下，最低VP需高于3 V，且支持全耳机负载范围。

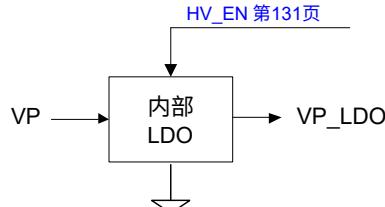


图4-3. 内部LDO配置

表 4-1。VP_LDO 电压对应 HV_EN 设置 HV_EN

VP_LDO 电压	
0	2.6 V
1	3.0 V

表4-2显示了当输出设置为第4.3.1节中说明的自适应模式时的标称信号和音量级别范围。如果信号电平超过该范围的最大值，则可能发生削波。

表 4-2。Class H 电源模式

模式	Class H 电源级别	信号 1或音量级别范围 2,3,4
0	$\pm VP_LDO$ V, 内部由VP稳压。	≥ -11 dB
1	$\pm VCP$	< -11 dB

1. 在自适应信号模式中，音量级别范围为近似值，但与所示数值的偏差不超过 -0.5 dB。
2. 相对于数字满量程，输出增益设置为 0 dB。
3. 在固定模式下，如果信号电平超过该范围的最大值，可能会发生削波，原因是放大器电源设置过低。
4. 阈值为 16Ω 立体声负载的标称值。

4.3.1 电源控制选项

本节描述两种操作模式：标准Class AB和适应输出信号。供给放大器输出级的轨电压组取决于ADPT_PWR（见第131页）设置。

4.3.1.1 标准Class AB操作 (ADPT_PWR = 001或010)

当ADPT_PWR设置为001或010时，供给放大器的轨电压分别保持为 $\pm VP_LDO$ 或 $\pm VCP$ 。供给输出级的轨电压保持恒定，不受输出信号电平影响。CS43131放大器仅以传统Class AB配置工作。

4.3.1.2 适应输出信号 (ADPT_PWR = 111)

当ADPT_PWR设置为111时，供给放大器的轨电压仅基于信号是否会在较低轨电压下使放大器在某些阈值处发生削波。

- 如果会导致削波，控制逻辑会指示电荷泵向放大器提供下一组更高的轨电压。
- 如果不会导致削波，控制逻辑会指示电荷泵向放大器提供较低的轨电压，从而无需向CS43131通报设备外部的音量设置。

4.3.2 Power-Supply Transitions

Charge-pump transitions from the lower to the higher set of rail voltages occur on the next FLYN/FLYP clock cycle. Despite the system's fast response time, the VCP_FILT pin's capacitive elements prevent rail voltages from changing instantly. Instead, the rail voltages ramp up from the lower to the higher supply, based on the time constant created by the output impedance of the charge pump and the capacitor on the VCP_FILT pin (the transition time is approximately 20 μ s).

Fig. 4-4 shows Class H supply switching. During this charging transition, a high dv/dt transient on the inputs may briefly clip the outputs before the rail voltages charge to the full higher supply level. This transitory clipping has been found to be inaudible in listening tests.

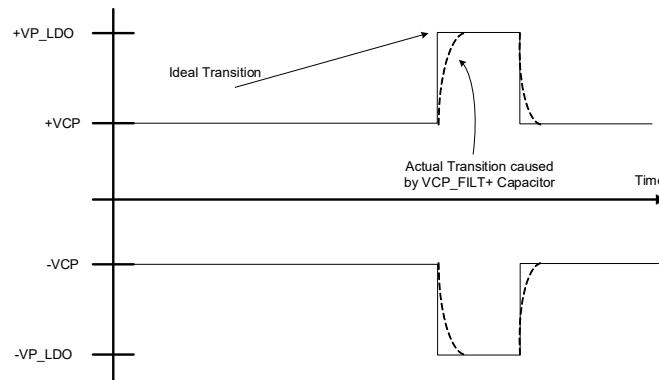


Figure 4-4. VCP_FILT Transitions

When the charge pump transitions from the lower to higher set of rail voltage, there is no delay associated with the transition.

4.3.2 电源转换

电荷泵从较低轨电压切换到较高轨电压发生在下一个FLYN/FLYP时钟周期。尽管系统响应时间很快，VCP_FILT引脚的电容元件阻止轨电压瞬间变化。

轨电压根据电荷泵输出阻抗与VCP_FILT引脚电容形成的时间常数，从较低电压逐渐上升到较高电压（转换时间约为20 μs）。

图4-4显示了Class H电源切换。在充电转换期间，输入端的高dv/dt瞬态可能会在轨电压充至完全较高电平之前短暂夹断输出。听觉测试表明该瞬态削波不可闻。

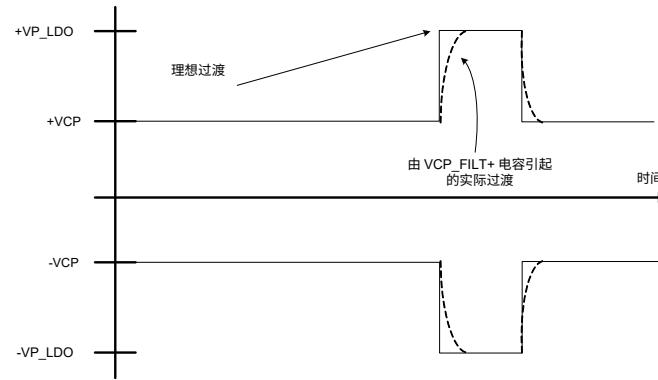


图 4-4. VCP_FILT 过渡

当电荷泵从较低电压档切换至较高电压档或轨电压时，过渡无延迟。

When the charge pump transitions from the higher to the lower set of rail voltages, there is an approximate 5.5-s delay before the charge pump supplies the lower rail voltages to the amplifiers. This hysteresis ensures that the charge pump does not toggle between the two rail voltages as signals approach the clip threshold. It also prevents clipping in the instance of repetitive high-level transients in the input signal. [Fig. 4-5](#) shows examples of this transitional behavior.

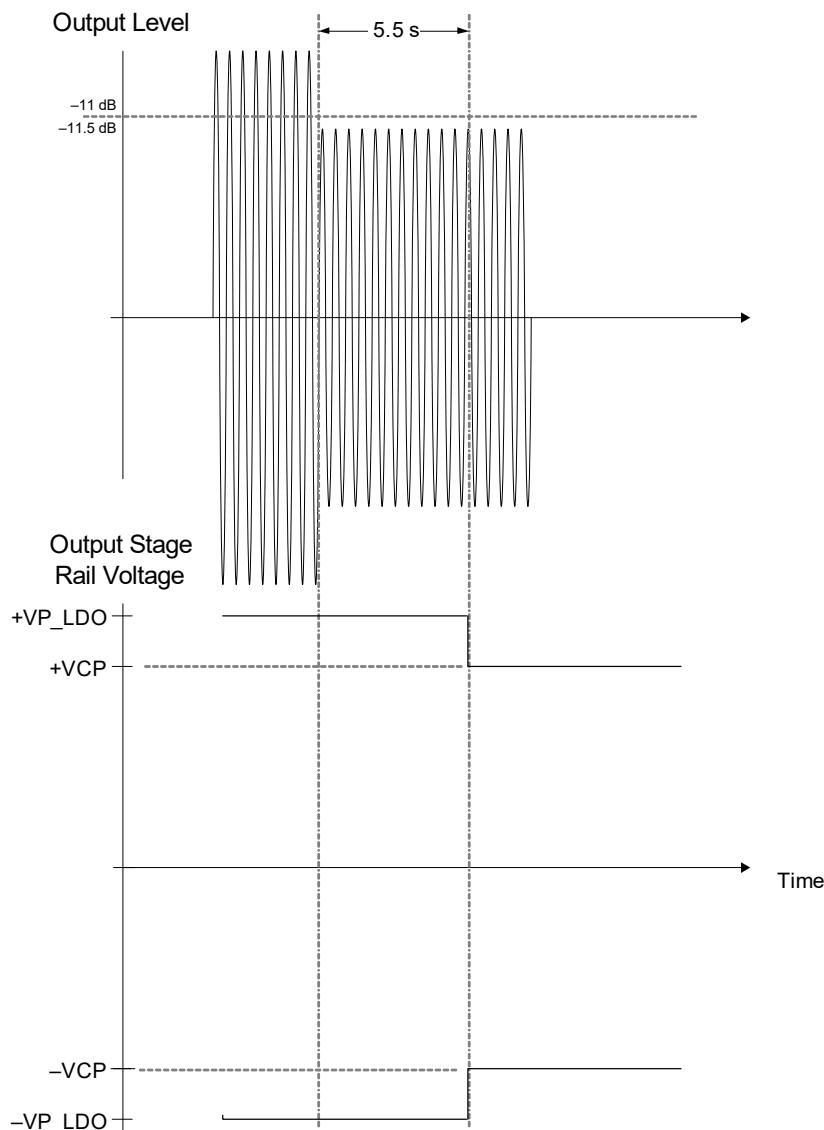


Figure 4-5. VCP_FILT Hysteresis

当电荷泵从较高电压档切换至较低电压档时，电荷泵在向放大器提供较低轨电压前约有 5.5 微秒延迟。该迟滞确保电荷泵在信号接近削波阈值时不会在两个轨电压间切换。它还防止了输入信号中重复高电平瞬态情况下的削波。图 4-5 展示了此过渡行为示例。

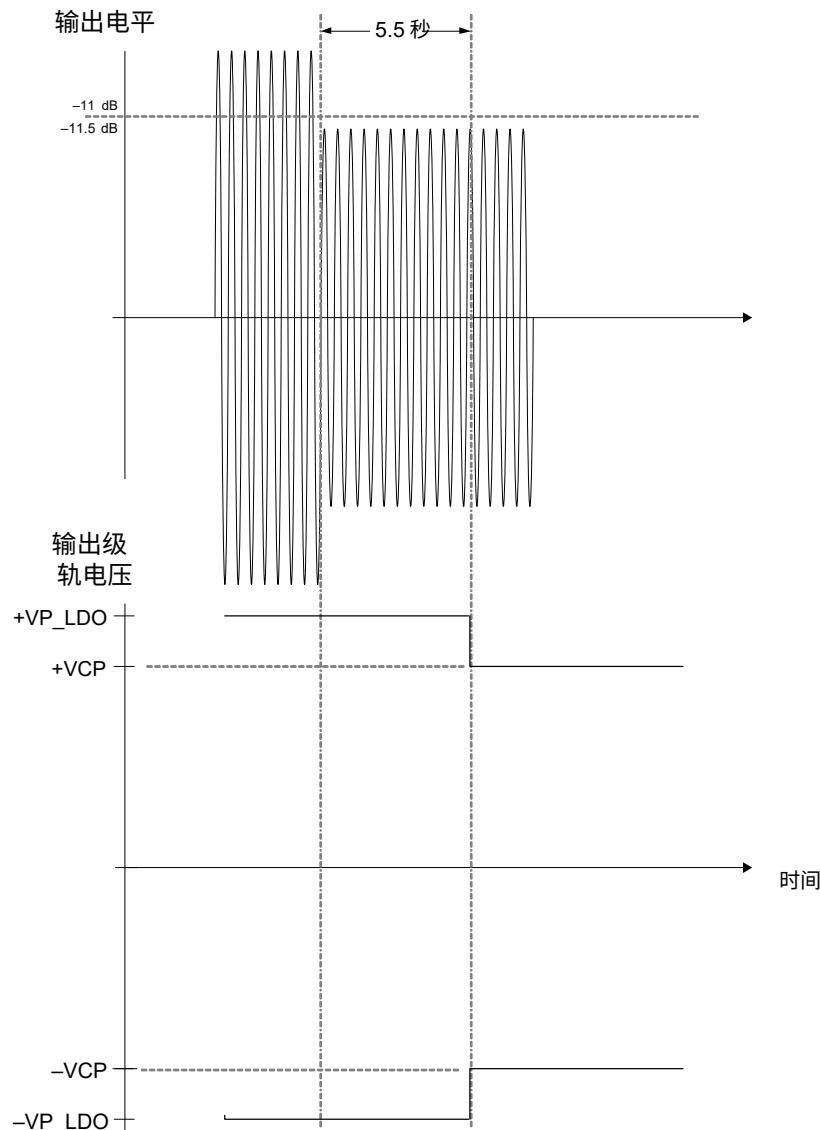


图 4-5. VCP_FILT 迟滞

4.3.3 HP Current Limiter

The CS43131 features built-in current-limit protection for the headphone output. [Table 3-18](#) lists the threshold for the current limit during the short-circuit conditions shown in [Fig. 4-6](#). For the HP amplifiers, current is from the internal charge pump output, and, as such, applies the current from VCP or VP.

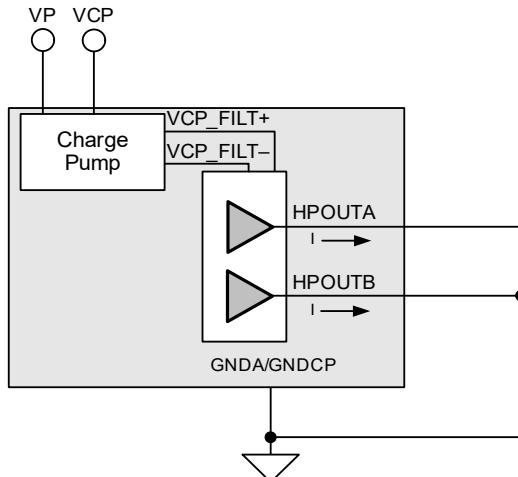


Figure 4-6. HP Short Circuit Setup

4.3.4 External VCP_FILT Supply Mode

To bypass the CS43131 Class-H charge-pump circuit, provide external VCP_FILT \pm supply with the following conditions:

- When CS43131 is operating, apply +3.0 V with $\pm 5\%$ accuracy to VCP_FILT+ and apply -3.0 V with $\pm 5\%$ accuracy to VCP_FILT-.
- When CS43131 is powered down, external circuits present Hi-Z state to the VCP_FILT+ pin ($>1k$ impedance) and VCP_FILT- pin ($>10k$ impedance).
- To avoid possible damage, VCP_FILT \pm pins must remain within the absolute maximum rating specified.

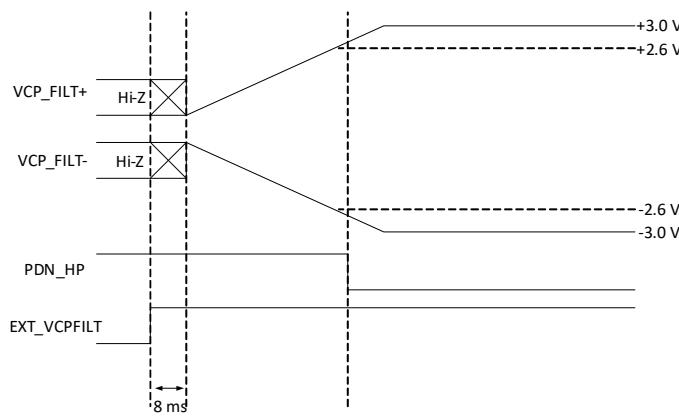


Figure 4-7. External VCP_FILT Power-Up Sequence

For powering up CS43131 in this mode, the recommended sequence must be followed. This assumes that the CS43131 starts from the status where VCP_FILT \pm pins are presented with Hi-Z.

1. Set EXT_VCPFILTER and HV_EN bits.
2. Wait 8 ms after I²C ACK.
3. Release and start to ramp external voltage on VCP_FILT \pm pins.
4. Wait until VCP_FILT+ pin voltage to be greater than +2.6V and VCP_FILT- to be less than -2.6 V.

4.3.3 耳机电流限制器

CS43131 具备内置耳机输出电流限制保护功能。表 3-18 列出了图 4-6 所示短路条件下的电流限制阈值。对于耳机放大器，电流来自内部电荷泵输出，因此电流来源于 VCP 或 VP。

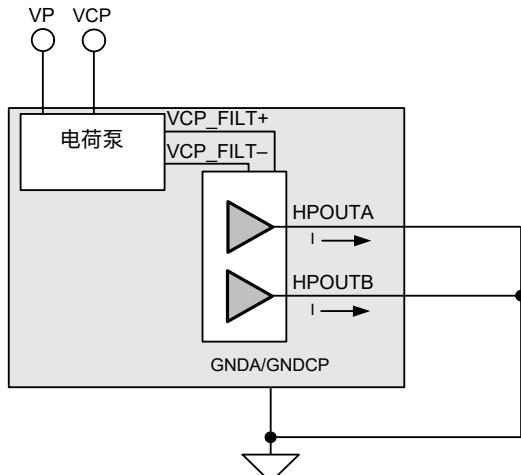


图 4-6. 耳机短路设置

4.3.4 外部 VCP_FILT 电源模式

要绕过 CS43131 的 Class-H 电荷泵电路，请提供满足以下条件的外部 VCP_FILT \pm 电源：

- 当 CS43131 工作时，VCP_FILT+ 施加 +3.0 V，精度为 $\pm 5\%$ ；VCP_FILT- 施加 -3.0 V，精度为 $\pm 5\%$ 。
- 当 CS43131 断电时，外部电路对 VCP_FILT+ 引脚呈现高阻抗状态（阻抗 $>1\text{k}\Omega$ ），对 VCP_FILT- 引脚呈现高阻抗状态（阻抗 $>10\text{k}\Omega$ ）。
- 为避免可能损坏，VCP_FILT \pm 引脚电压必须保持在规定的绝对最大额定值范围内。

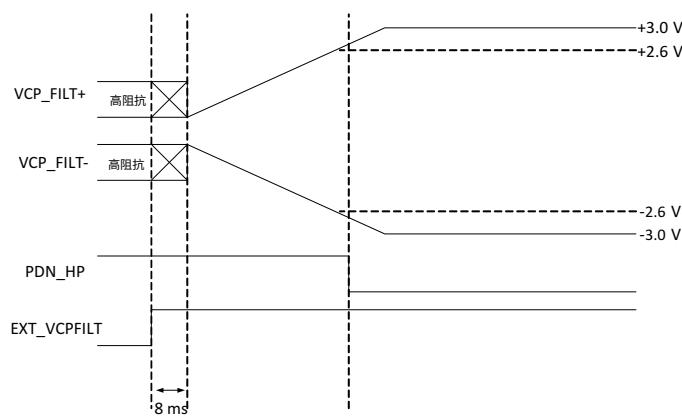


图 4-7. 外部 VCP_FILT 上电顺序

在此模式下为 CS43131 上电时，必须遵循推荐的顺序。假设 CS43131 启动时，VCP_FILT \pm 引脚处于高阻抗状态。

1. 设置 EXT_VCPFILT 和 HV_EN 位。
2. 等待 I²C 应答后 8 毫秒。
3. 释放并开始对 VCP_FILT \pm 引脚施加外部电压斜升。
4. 等待 VCP_FILT+ 引脚电压高于 +2.6V，且 VCP_FILT- 引脚电压低于 -2.6V。

5. Clear the PDN_HP bit.

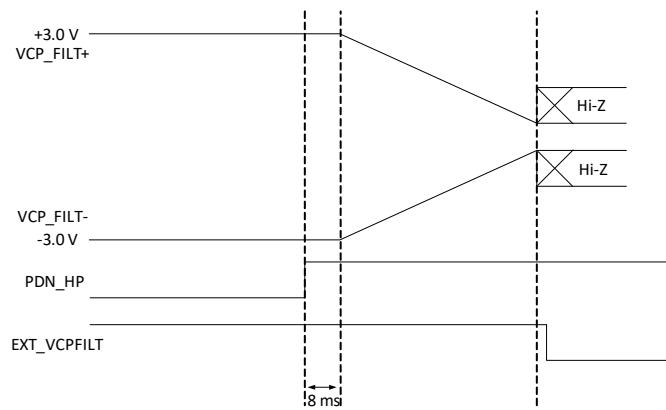


Figure 4-8. External VCP_FILT Power-Down Sequence

For powering down in this mode, use the following recommended sequence. This assumes that the CS43131 starts from the status where $VCP_FILT\pm$ pins are presented with ± 3.0 V, respectively.

1. Set PDN_HP.
2. Wait 8 ms after I²C ACK.
3. Start to shut-off external supply to $VCP_FILT\pm$ pins.
4. Wait until Hi-Z mode is presented on $VCP_FILT\pm$ pins.
5. Clear EXT_VCPFILT and HV_EN bits.

4.4 Alternate Headphone Inputs

The top-level schematic of the alternate headphone inputs is shown in Fig. 4-9. Bits PDN_HP and HP_IN_EN configure the audio source for the HPOUT pins. The switches connected to HPINx are controlled by HP_IN_EN. The switches connected to the internal headphone driver are controlled by PDN_HP. When the alternate headphone inputs are selected ($HP_IN_EN = 1$), the CS43131 internal headphone driver output needs to be disconnected ($PDN_HP = 1$). Likewise, when the CS43131 internal headphone drivers are enabled, the HPINx switch needs to be open and not in the signal path.

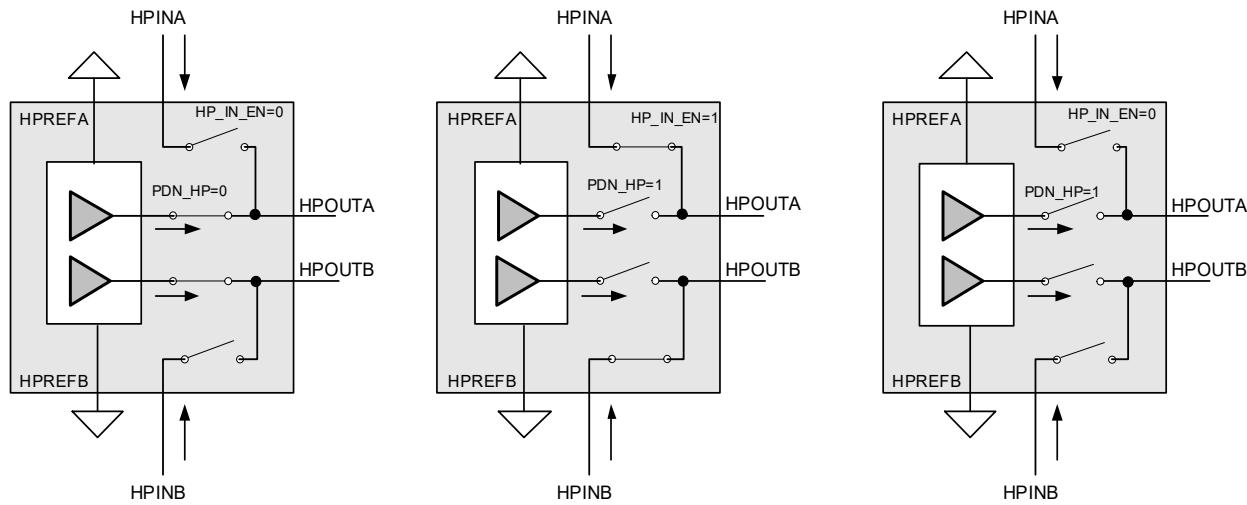


Figure 4-9. Alternative Headphone Input Setup

5. 清除 PDN_HP 位。

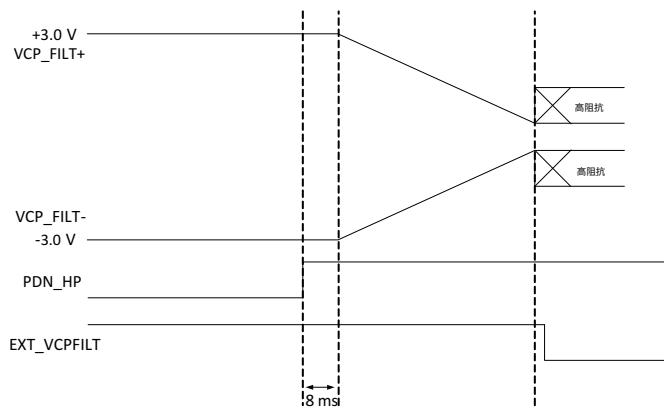


图 4-8。外部 VCP_FILT 断电顺序

在此模式下断电，请使用以下推荐顺序。假设 CS43131 起始状态为 VCP_FILT \pm 引脚分别呈现 $\pm 3.0\text{ V}$ 。

1. 设置 PDN_HP。
2. 等待 I²C 应答后 8 毫秒。
3. 开始关闭外部对 VCP_FILT \pm 引脚的供电。
4. 等待 VCP_FILT \pm 引脚进入高阻抗模式。
5. 清除 EXT_VCPFILT 和 HV_EN 位。

4.4 备用耳机输入

备用耳机输入的顶层原理图如图 4-9 所示。PDN_HP 和 HP_IN_EN 位配置 HPOUT 引脚的音频源。连接到 HPINx 的开关由 HP_IN_EN 控制，连接到内部耳机驱动器的开关由 PDN_HP 控制。当选择备用耳机输入 (HP_IN_EN = 1) 时，需断开 CS43131 内部耳机驱动器输出 (PDN_HP = 1)。同样，当 CS43131 内部耳机驱动器启用时，HPINx 开关需断开且不在信号路径中。

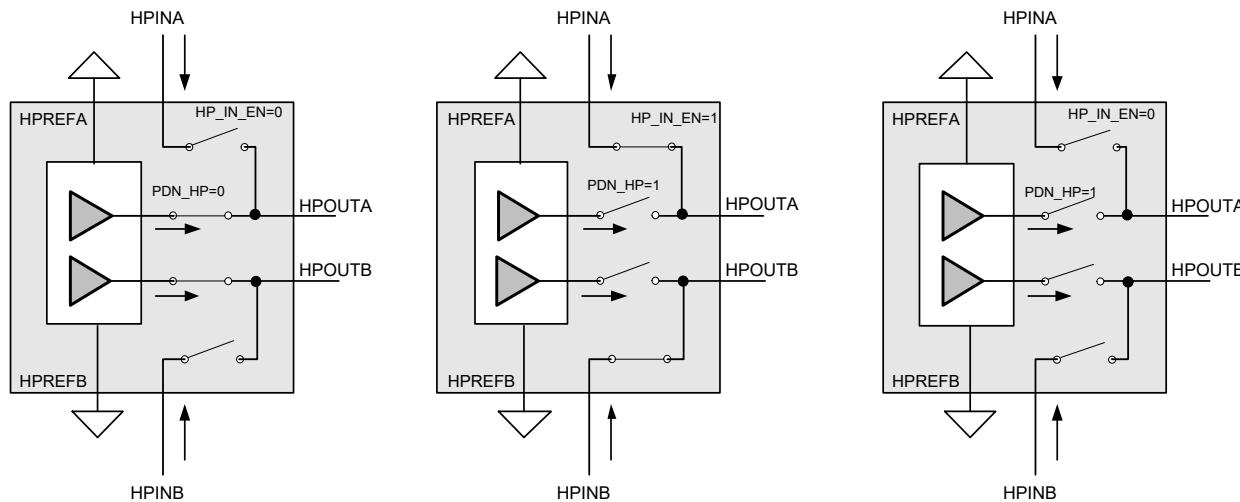


图 4-9。备用耳机输入设置

Before opening the HPINx switches, ramp down any active signal on HPINx pins to a voltage less than the V_{INOFF} value specified in [Table 3-8](#). Similarly, the voltage cannot exceed the same voltage requirement before the switches are closed. To prevent any pop on the headphone, the input should be muted during these transition. The CS43131 has ultralow offset when muted. For pop-free transition on the headphone, it is expected that the source on HPINx pins have low offset to ground when muted.

The recommended sequence to switch from CS43131 to HPINx is as follows:

1. Soft ramp content on CS43131 down to mute.
2. Set PDN_HP and wait for PDN_DONE_INT event.
3. If saving power is desired, switch MCLK_INT source to RCO.
4. Set HP_IN_EN.

The recommended sequence to switch from HPINx to CS43131 is as follows:

1. Setup CS43131 intended MCLK source for DAC operation (if needed)
2. Soft ramp content on HPINx down to mute.
3. Clear HP_IN_EN.
4. Switch MCLK_INT to the intended MCLK source when ready.
5. Clear PDN_HP.

The CS43131 has a HP_IN_LP setting to further reduce power when HPINx is enabled. This low power mode is only supported if EXT_VCPFILT = 0. When selected, the HPINx path is placed into low power mode. This setting is only in effect when HP_IN_EN = 1. It should only be set after HP_IN_EN = 1, and the user must wait for t_{HPIN_ON} (EXT_VCPFILT = 1) before enabling HP_IN_LP bit. HP_IN_LP should be cleared before HP_IN_EN is cleared. When HP_IN_LP = 1, the maximum supported clock speed for I²C is 400 kHz.

4.5 Headphone Presence Detect and Output Load Detection

The CS43131 provides headphone presence-detect and load-detection functionalities.

4.5.1 Headphone Presence Detect

The CS43131 supports headphone presence-detect capability via the HP_DETECT sense pin. HP_DETECT is debounced to filter out brief events before being reported to the corresponding presence-detect status bit and generating an interrupt if appropriate.

4.5.1.1 Headphone Plug Types

The presence detect scheme is designed to support the following plug types:

- Tip-Ring-Sleeve (TRS). Consists of a segmented metal barrel with the tip connector used for HPOUTA, a ring connector used for HPOUTB, and a sleeve connector used for HPGND.
- Tip-Ring-Ring-Sleeve (TRRS). Similar to TRS, with an additional ring connector for the HSIN connection. There are two common pinouts for TRRS plugs:
 - The tip is used for HPOUTA, the first ring for HPOUTB, the second ring for HSGND, and the sleeve for HSIN.
 - An alternate pinout, OMTP (open mobile terminal platform), also called “China headset,” swaps the third and fourth connections so that the second ring carries HSIN and the sleeve carries HSGND.

Note that if both TRRS plug types need to be supported at the same time, the CS43131 requires an additional IC to perform the OMTP detect functions and to present the identified HSGND to the CS43131 HPREFx. However, the switch inside the detect IC may degrade the CS43131 performance.

在打开 HPINx 开关之前，应将 HPINx 引脚上的任何活动信号逐渐降低至低于表 3-8 中指定的 V_{INOFF} 值。同样，在关闭开关之前，电压不得超过相同的电压限制。

为防止耳机产生爆音，切换过程中应对输入信号进行静音处理。CS43131 在静音状态下具有超低偏移。为实现耳机无爆音切换，期望 HPINx 引脚上的信号源在静音时对接地具有低偏移。

从 CS43131 切换到 HPINx 的推荐顺序如下：

1. CS43131 上的软启动内容逐渐降低至静音状态。
2. 设置 PDN_HP 并等待 PDN_DONE_INT 事件。
3. 如需节能，请将 MCLK_INT 源切换至 RCO。
4. 设置 HP_IN_EN。

从 HPINx 切换至 CS43131 的推荐顺序如下：

1. 设置 CS43131 用于 DAC 操作的预期 MCLK 源（如有必要）
2. HPINx 上的软启动内容逐渐降低至静音状态。
3. 清除 HP_IN_EN。
4. 准备就绪后，将 MCLK_INT 切换至预期的 MCLK 源。
5. 清除 PDN_HP。

CS43131 具有 HP_IN_LP 设置，可在启用 HPINx 时进一步降低功耗。此低功耗模式仅在 $EXT_VCPFILT = 0$ 时支持。选中后，HPINx 路径将进入低功耗模式。此设置仅在 $HP_IN_EN = 1$ 时生效。应在 $HP_IN_EN = 1$ 之后设置，且用户必须等待 t_{HPIN_ON} ($EXT_VCPFILT = 1$) 后才能启用 HP_IN_LP 位。清除 HP_IN_EN 前应先清除 HP_IN_LP 。当 $HP_IN_LP = 1$ 时，I²C 支持的最大时钟频率为 400 kHz。

4.5 耳机存在检测及输出负载检测

CS43131 提供耳机存在检测及负载检测功能。

4.5.1 耳机存在检测

CS43131 通过 HP_DETECT 感测引脚支持耳机存在检测功能。HP_DETECT 经过消抖处理，以滤除短暂事件，随后将状态报告至相应存在检测状态位，并在适当情况下触发中断。

4.5.1.1 耳机插头类型

该存在检测方案设计支持以下插头类型：

- Tip-Ring-Sleeve (TRS) 由分段金属外壳组成，尖端连接器用于 HPOUTA，环形连接器用于 HPOUTB，套筒连接器用于 HPGND。
- Tip-Ring-Ring-Sleeve (TRRS) 与 TRS 类似，增加了一个环形连接器用于 HSIN 连接。TRRS 插头有两种常见的引脚排列：
 - 插头尖端用于 HPOUTA，第一个环用于 HPOUTB，第二个环用于 HSGND，插套用于 HSIN。
 - 另一种引脚排列方式 OMTP（开放移动终端平台），也称为“中式耳机”，将第三和第四个连接交换，使第二个环承载 HSIN，插套承载 HSGND。

注意，如果需要同时支持两种 TRRS 插头类型，CS43131 需要额外的集成电路来执行 OMTP 检测功能，并将识别出的 HSGND 提供给 CS43131 的 HPREFx 引脚。然而，检测集成电路内部的开关可能会降低 CS43131 的性能。

4.5.1.2 Headphone Detect Methods

CS43131 can detect the presence or absence of a plug. For a headphone-presence detect, a sense pin is connected to a terminal on the receptacle such that, if no plug is inserted, the pin is floating. If a plug is inserted, the pin is shorted to the tip (T) terminal. The presence detect function is accomplished by having a small current source inside the CS43131 to pull up the pin if it is left floating (no plug). If a plug is inserted and the sense pin is shorted to HPOUTA, when HP amp is powered down, it is assumed that the sense pin is pulled low via clamps at the HP amp output. If the HP amp is running, the sense pin is shorted to the output signal and, therefore, is pulled below a certain threshold via the output stage of the HP amp. Thus, a low level at the sense pin indicates plug inserted, and a high level at the sense pin indicates plug removed.

4.5.1.3 Headphone Detect Registers

This section describes the behavior and interaction of the headphone-detect debounce register fields. See [Fig. 4-10](#) for reference.

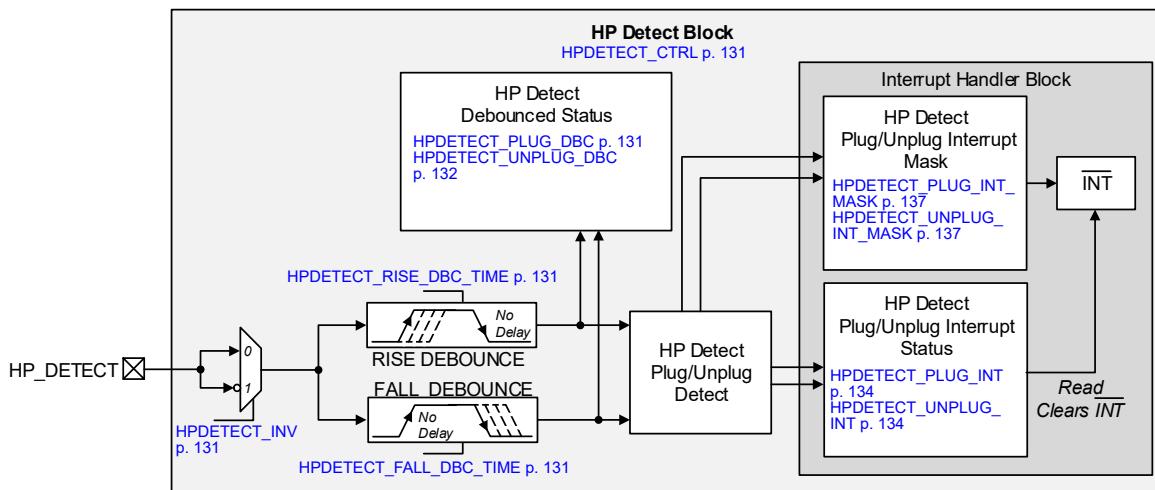


Figure 4-10. Headphone Detect Block Diagram

- HPDETECT_CTRL configures the operation of the HP detect circuit.
- HPDETECT_INV inverts the signal from the HP detect circuit.
- HPDETECT_FALL_DBC_TIME configures the HP_DETECT falling debounce time.
- HPDETECT_RISE_DBC_TIME configures the HP_DETECT rising debounce time.
- HPDETECT_PLUG_DBC shows the falling-edge-debounced version of HP_DETECT signal.
- HPDETECT_UNPLUG_DBC shows the rising-edge-debounced version of HP_DETECT signal.
- HPDETECT_PLUG_INT shows the headphone plug-in event status.
- HPDETECT_UNPLUG_INT shows the headphone unplug event status.
- HPDETECT_PLUG_INT_MASK is the interrupt mask of headphone plug-in event status.
- HPDETECT_UNPLUG_INT_MASK is the interrupt mask of headphone unplug event status.

4.5.1.4 Headphone Detect and Interrupts Setup Instructions

The following steps are required for activation of headphone-detect debounce interrupt status:

1. Ensure the I²C is ready to respond to control port command.
2. Clear the interrupt masks.
3. Write to HPDETECT_RISE_DBC_TIME and HPDETECT_FALL_DBC_TIME (see [p. 131](#)) to enable debounce for presence detect plug/unplug.
4. Set HPDETECT_CTRL to 11 to enable the HPDETECT functions.

4.5.1.2 耳机检测方法

CS43131 可以检测插头的存在与否。对于耳机存在检测，感应引脚连接到插座的一个端子，若未插入插头，该引脚处于悬空状态。如果插入插头，引脚将与尖端 (T) 端短接。CS43131 内部设有一个小电流源，当引脚悬空（无插头）时将其拉高，从而实现存在检测功能。如果插入插头且检测引脚与 HPOUTA 短接，当耳机放大器关闭时，假定检测引脚通过耳机放大器输出端的钳位被拉低。如果耳机放大器工作，检测引脚与输出信号短接，因此通过耳机放大器的输出级被拉低至某一阈值以下。检测引脚的低电平表示插头已插入，高电平表示插头已拔出。

4.5.1.3 耳机检测寄存器

本节描述耳机检测消抖寄存器字段的行为及其相互作用。详见图4-10。

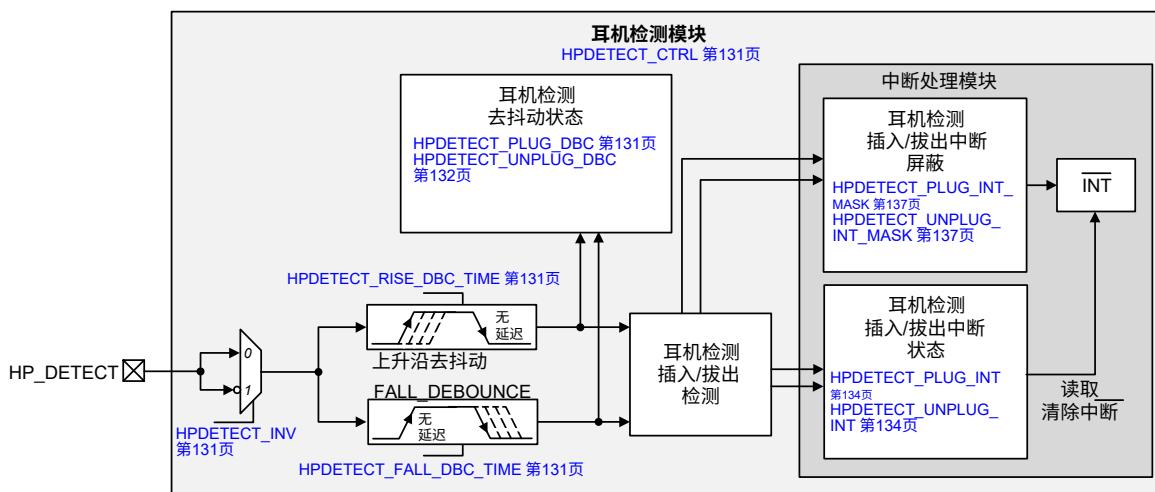


图4-10。耳机检测框图

- HPDETECT_CTRL 配置耳机检测电路的工作方式。
- HPDETECT_INV 对耳机检测电路的信号进行反相处理。
- HPDETECT_FALL_DBC_TIME 配置 HP_DETECT 信号下降沿的消抖时间。
- HPDETECT_RISE_DBC_TIME 配置 HP_DETECT 信号上升沿的消抖时间。
- HPDETECT_PLUG_DBC 显示 HP_DETECT 信号经过下降沿消抖后的状态。
- HPDETECT_UNPLUG_DBC 显示 HP_DETECT 信号经过上升沿消抖后的状态。
- HPDETECT_PLUG_INT 显示耳机插入事件状态。
- HPDETECT_UNPLUG_INT 显示耳机拔出事件状态。
- HPDETECT_PLUG_INT_MASK 是耳机插入事件状态的中断屏蔽位。
- HPDETECT_UNPLUG_INT_MASK 是耳机拔出事件状态的中断屏蔽位。

4.5.1.4 耳机检测及中断设置说明

激活耳机检测消抖中断状态需执行以下步骤：

1. 确保 I²C 已准备好响应控制端口命令。
2. 清除中断屏蔽。
3. 写入 HPDETECT_RISE_DBC_TIME 和 HPDETECT_FALL_DBC_TIME（见第131页）以启用插入/拔出检测的去抖动功能。
4. 将 HPDETECT_CTRL 设置为 11 以启用耳机检测功能。

The interrupt status bits can be found in [Section 7.6.1](#).

4.5.2 HP Load Detection

The CS43131 can measure the impedance of headphone DC load. Before taking measurements, the following criteria must be met:

- The CS43131 is out of reset.
- XTAL is powered on, an external MCLK is provided or PLL mode is used to generate internal MCLK. MCLK_INT is properly configured.
- The headphone output is powered down (PDN_HP = 1).
- The alternate headphone input is powered down (HP_IN_EN = 0).
- HPDETECT is high to indicate a headphone is plugged in.
- The HPOLOAD_EN bit is set to turn on the impedance measurement subsystem. HPOLOAD_ON_INT is unmasked and there has been a long enough wait to confirm the subsystem is properly started.
- The HPOLOAD_DC_DONE interrupt is unmasked.

Either Channel A or Channel B to be measured by setting HPOLOAD_CHN_SEL. The measurement process by clearing and setting the HPOLOAD_DC_START bit. Once started, HPOLOAD_DC_BUSY bit is set and a slowly ramping voltage is asserted on the headphone load for a maximum of 200 ms, then holds constant for 100 ms. [Fig. 4-11](#) shows the waveform of the impedance detection voltage.

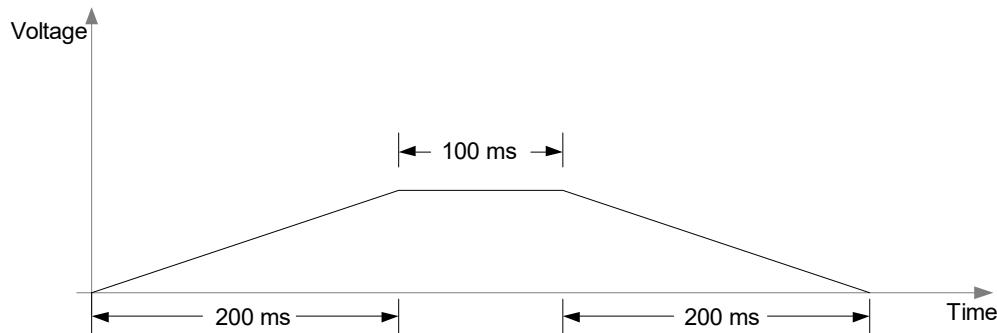


Figure 4-11. Impedance Detection Voltage

Upon measurement completion, the following occurs:

1. The voltage asserted ramps down for 200 ms and is then removed.
2. The result of the measured resistance is reported in RL_DC_STAT.
3. HPOLOAD_DC_DONE bit is set and the interrupt is triggered.
4. If HPOLOAD_DC_ONCE bit has not been set, it is set. This bit is sticky until an HP unplug event has happened.

Once interrupted, the application processor services the interrupt by reading HPOLOAD_DC_DONE_INT. At this point, another measurement process can be initiated by clearing and setting the HPOLOAD_DC_START bit. The impedance measurement subsystem can also be turned off by clearing the HPOLOAD_EN bit. HPOLOAD_EN must be cleared (and confirmed by unmasked HPOLOAD_OFF_INT) before enabling the headphone output or the alternate headphone input.

During the impedance measurement process, the following conditions trigger the error interrupt bits:

- The headphone load is not present or is unplugged before the impedance measurement is complete (HPOLOAD_UNPLUG_INT).
- The headphone load is out of range, as specified in [Table 3-7](#) (HPOLOAD_OOR_INT).
- The headphone load measurement process is started without HP being properly turned off (HPOLOAD_HPON_INT).
- The AC headphone load measurement process is initiated before the HPOLOAD_DC_ONCE bit is set (HPOLOAD_NO_DC_INT).

中断状态位详见第7.6.1节。

4.5.2 耳机负载检测

CS43131能够测量耳机直流负载的阻抗。在进行测量之前，必须满足以下条件：

- CS43131已退出复位状态。
- 晶体振荡器已上电，提供外部MCLK，或使用PLL模式生成内部MCLK。MCLK_INT已正确配置。
- 耳机输出已关闭电源（PDN_HP = 1）。
- 备用耳机输入已关闭电源（HP_IN_EN = 0）。
- HPDETECT为高电平，表示耳机已插入。
- HPOLOAD_EN位被置位以开启阻抗测量子系统。HPOLOAD_ON_INT未屏蔽，且已等待足够时间以确认子系统已正确启动。
- HPOLOAD_DC_DONE 中断未屏蔽。

通过设置 HPOLOAD_CHN_SEL 选择测量通道 A 或通道 B。测量过程通过清除并设置 HPOLOAD_DC_START 位启动。启动后，HPOLOAD_DC_BUSY 位被置位，耳机负载上施加一个缓慢上升的电压，最长持续 200 毫秒，然后保持恒定 100 毫秒。图 4-11 显示了阻抗检测电压的波形。

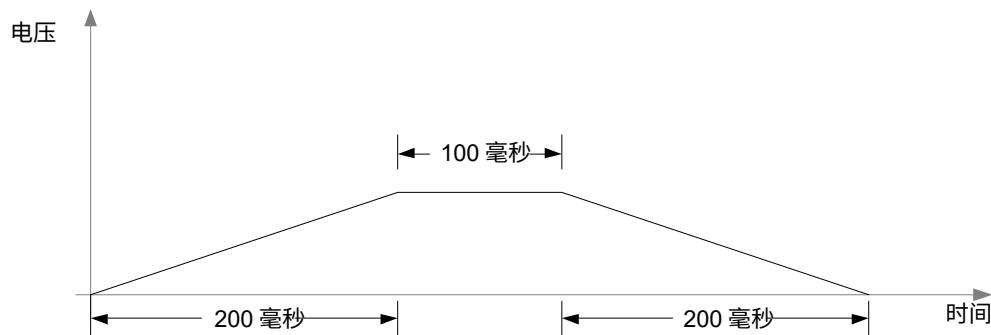


图 4-11。阻抗检测电压

测量完成后，发生以下情况：

1. 施加的电压在 200 毫秒内逐渐降低，然后被移除。
2. 测得的电阻结果报告在 RL_DC_STAT 中。
3. HPOLOAD_DC_DONE 位被置位，中断被触发。
4. 如果 HPOLOAD_DC_ONCE 位尚未置位，则将其置位。该位保持有效，直到发生耳机拔出事件。

一旦发生中断，应用处理器通过读取 HPOLOAD_DC_DONE_INT 来处理中断。此时，可以通过清除并设置 HPOLOAD_DC_START 位来启动新的测量过程。通过清除 HPOLOAD_EN 位，还可以关闭阻抗测量子系统。在启用耳机输出或备用耳机输入之前，必须先清除 HPOLOAD_EN（并通过未屏蔽的 HPOLOAD_OFF_INT 确认）。

在阻抗测量过程中，以下情况会触发错误中断位：

- 耳机负载不存在或在阻抗测量完成前被拔出（HPOLOAD_UNPLUG_INT）。
- 耳机负载超出表 3-7 所示范围（HPOLOAD_OOR_INT）。
- 在未正确关闭耳机的情况下启动耳机负载测量过程（HPOLOAD_HPON_INT）。
- 在设置 HPOLOAD_DC_ONCE 位之前启动交流耳机负载测量过程（HPOLOAD_NO_DC_INT）。

The HPOLOAD error interrupt bits are sticky. If any HPOLOAD error interrupt bits are flagged, the RL_DC_STAT value should be treated as invalid.

4.5.2.1 AC Load Detection

The CS43131 can also measure the headphone load impedance in the frequency range of 20 Hz to 20 kHz. The required conditions before the measurement is similar to the low frequency load measurement, with one exception—HPOLOAD_MEAS_FREQ is set at the frequency of interest. Refer to [Section 7.5.14](#) and [Section 7.5.15](#) for details.

After HPOLOAD_AC_START bit is cleared and set:

1. HPOLOAD_AC_BUSY bit is set
2. The result of the measured resistance is reported in RL_AC_STAT.
3. HPOLOAD_AC_DONE_INT is set and the interrupt is triggered.

For each headphone, the low-frequency load measurement must be performed (as indicated by the HPOLOAD_DC_ONCE bit) before any impedance is measured at other frequencies. If the low-frequency load measurement is not performed and the process is initiated by pulsing the HPOLOAD_AC_START bit low and high, the CS43131 can not generate a test signal and sets the HPOLOAD_NO_DC_INT error interrupt bit. Any RL_AC_STAT value should be treated as invalid.

Once the measurement begins, a tone at the specified frequency is applied on the headphone load. Because the test tone is in the audio frequency range, it can be audible by the headphone user. It is recommended that the user system notify the headphone user of the expected events before initiating this measurement.

For each frequency, the measurement completion time is affected by the frequency of interest. The lower the frequency, the longer the measurement time. For the relationship between the frequency under test and the measurement time, the following applies:

- For frequencies under test less than 6 kHz or when the CS43131 comes out of reset, 10 periods of the test tone is the measurement time.
- For frequencies under test between 6 and 13 kHz, 20 periods of the test tone is the measurement time.
- For frequencies under test between 13 and 20 kHz, 30 periods of the test tone is the measurement time.

See [Section 5.14.2](#) for example code of AC impedance measurement.

4.6 Clocking Architecture

4.6.1 Master Clock (MCLK) Sources

The MCLK is required by the CS43131 to operate any functionality associated with control, serial-port operation, or data conversion. Depending on the setting of [MCLK_SRC_SEL](#) (see p. 114), the MCLK can be provided by one of following methods:

- Sourced from a crystal oscillator between XTI/MCLK and XTO pins (see [Fig. 4-12](#)), then used directly as MCLK_INT
- Externally sourced through the XTI/MCLK input pin (see [Fig. 4-13](#))
- PLL reference clock is provided through the XTI/MCLK input pin (see [Fig. 4-13](#)), then use internal PLL to convert into MCLK_INT

HPOLOAD 错误中断位为粘滞位。如果任何 HPOLOAD 错误中断位被置位，则 RL_DC_STAT 值应视为无效。

4.5.2.1 交流负载检测

CS43131 还可以测量频率范围为 20 Hz 至 20 kHz 的耳机负载阻抗。测量前的必要条件与低频负载测量类似，唯一例外是 HPOLOAD_MEAS_FREQ 设置为所关注的频率。详情请参见第 7.5.14 节和第 7.5.15 节。

在清除并设置 HPOLOAD_AC_START 位后：

1. HPOLOAD_AC_BUSY 位被置位。
2. 测量得到的电阻结果报告在 RL_AC_STAT 中。
3. HPOLOAD_AC_DONE_INT 被置位并触发中断。

对于每个耳机，必须先执行低频负载测量（由 HPOLOAD_DC_ONCE 位指示），然后才能测量其他频率的阻抗。如果未执行低频负载测量，且通过将 HPOLOAD_AC_START 位由低脉冲至高启动该过程，CS43131 将无法生成测试信号，并置位 HPOLOAD_NO_DC_INT 错误中断位。任何 RL_AC_STAT 值均应视为无效。

一旦测量开始，将在耳机负载上施加指定频率的音调。由于测试音调处于音频频率范围内，耳机用户能够听到该音调。建议用户系统在启动此测量之前通知耳机用户预期的事件。

对于每个频率，测量完成时间受所测频率的影响。频率越低，测量时间越长。关于被测频率与测量时间的关系，适用以下规则：

- 对于低于 6 kHz 的被测频率或 CS43131 刚刚复位时，测量时间为测试音调的 10 个周期。
- 对于 6 至 13 kHz 之间的被测频率，测量时间为测试音调的 20 个周期。
- 对于 13 至 20 kHz 之间的被测频率，测量时间为测试音调的 30 个周期。

有关交流阻抗测量的示例代码，请参见第 5.14.2 节。

4.6 时钟架构

4.6.1 主时钟 (MCLK) 源

CS43131 需要 MCLK 以实现与控制、串行端口操作或数据转换相关的任何功能。根据 MCLK_SRC_SEL 的设置（见第 14 页），MCLK 可通过以下方式之一提供：

- 由连接 XTI/MCLK 和 XTO 引脚之间的晶体振荡器提供（见图 4-12），然后直接用作 MCLK_INT。
- 通过 XTI/MCLK 输入引脚外部提供（见图 4-13）。
- 通过 XTI/MCLK 输入引脚提供 PLL 参考时钟（见图 4-13），然后使用内部 PLL 转换为 MCLK_INT。

- Use internal RCO as MCLK. Note that for optimized power consumption, the HPIN input path is the only supported audio playback feature in this mode. This mode can also support HP detection and I²C communication. DAC playback and headphone impedance measurement functions are not supported.

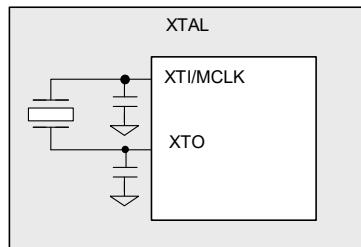


Figure 4-12. System Clocking—Crystal Mode

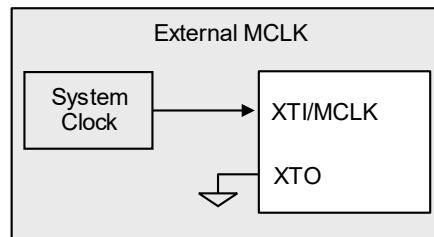


Figure 4-13. System Clocking—External MCLK Mode

If XTAL is used, the supported crystal characteristics and frequencies are listed in [Table 3-16](#). Based on the crystal selection, XTAL_IBIAS must be set properly before powering up. The XTAL_IBIAS information can be found in [Section 5.3](#). PDN_XTAL is cleared to start the crystal oscillator. PDN_XTAL is set to power down the crystal oscillator. The XTAL_READY_INT and XTAL_ERROR_INT status bits indicate the status of crystal operation after power-up. At t_{XTAL_pup} after the crystal oscillator is powered up, if the crystal is started successfully and ready to be used, XTAL_READY_INT is set; if the crystal is started unsuccessfully, XTAL_ERROR_INT is set. The two bits are mutually exclusive when set. Both status bits have corresponding interrupt status bits and interrupt mask bits. To be informed on the crystal status at t_{XTAL_pup} after power-up, unmask both interrupts before powering up the crystal.

When the MCLK is supplied to the device through the XTI/MCLK pin, it must comply with the phase-noise mask shown in [Fig. 4-14](#). Its frequency must be one of the nominal MCLK_INT frequencies (22.5792 or 24.576 MHz), and its duty cycle must be between 45% to 55%.

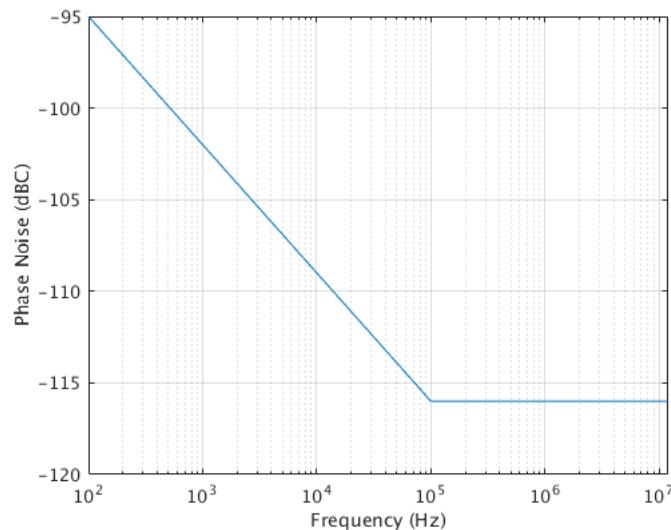


Figure 4-14. MCLK Phase Noise Mask Without PLL

- 使用内部 RCO 作为 MCLK。请注意，为优化功耗，此模式下仅支持 HPIN 输入路径的音频播放功能。该模式还支持耳机检测和 I2C 通信。不支持 DAC 播放和耳机阻抗测量功能。

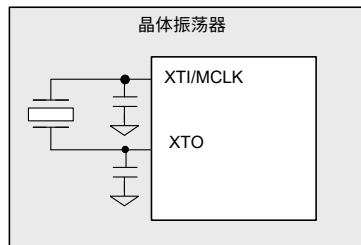


图 4-12。系统时钟——晶体模式

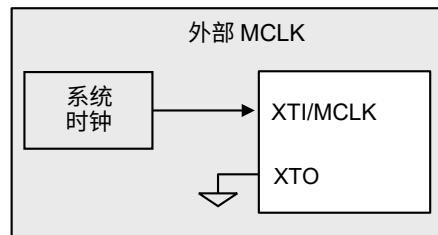


图 4-13。系统时钟——外部 MCLK 模式

如果使用晶体振荡器，支持的晶体特性和频率列于表 3-16。根据晶体的选择，必须在上电前正确设置 XTAL_IBIAS。XTAL_IBIAS 的相关信息见第 5.3 节。清除 PDN_XTAL 以启动晶体振荡器。设置 PDN_XTAL 以关闭晶体振荡器。XTAL_READY_INT 和 XTAL_ERROR_INT 状态位指示晶体上电后的运行状态。在晶体振荡器上电后的 tXTAL_pup 时，如果晶体启动成功且准备就绪，XTAL_READY_INT 被置位；如果晶体启动失败，XTAL_ERROR_INT 被置位。两者互斥。两个状态位均对应中断状态位和中断屏蔽位。要在晶体上电后的 tXTAL_pup 时获知晶体状态，请在上电前取消屏蔽这两个中断。

当通过XTI/MCLK引脚向器件提供MCLK时，必须符合图4-14所示的相位噪声掩码。其频率必须为标称MCLK_INT频率之一（22.5792 MHz或24.576 MHz），且占空比必须在45%至55%之间。

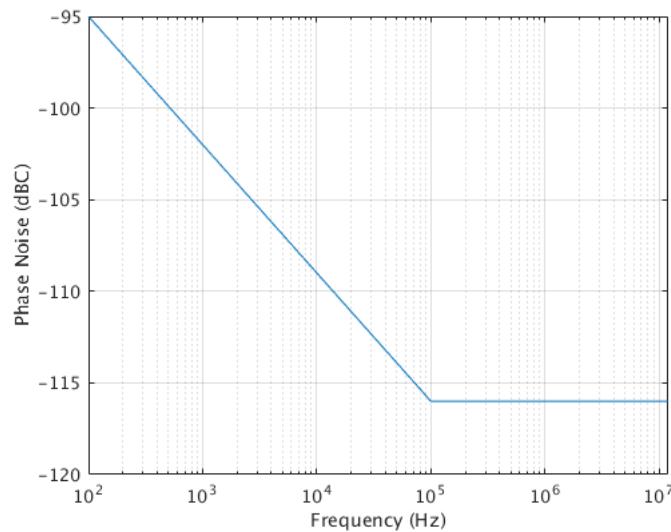


图 4-14。无 PLL 时的 MCLK 相位噪声掩码

When the PLL reference clock is supplied to the device through the XTI/MCLK pin, it must comply with the phase-noise mask shown in Fig. 4-15.

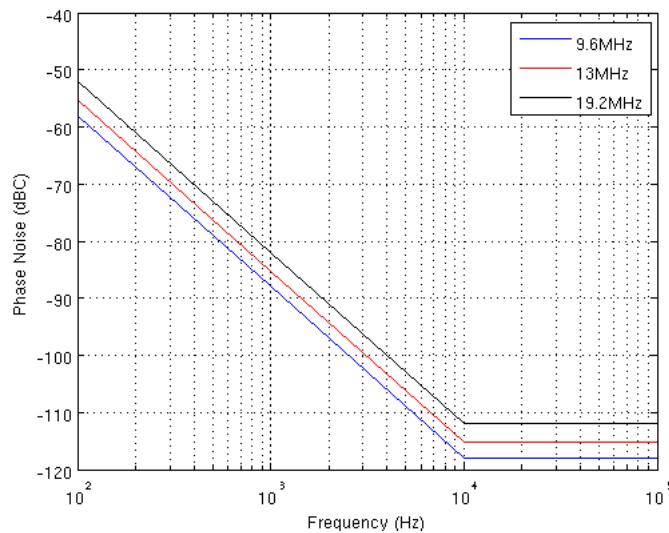


Figure 4-15. MCLK Phase Noise Mask With PLL

Further restrictions are listed in Table 4-3.

Table 4-3. MCLK Source Restrictions

Internal MCLK Source	MCLK_SRC_SEL	MCLK_INT	Restrictions
Direct MCLK or XTAL	00	0	<ul style="list-style-type: none"> Nominal MCLK_INT frequency = 24.576 MHz All specified CLKOUT frequencies (generated by PLL or XTAL) are supported CLKOUT outputs (/2, /3, /4, /8 divide) optionally
		1	<ul style="list-style-type: none"> Nominal MCLK_INT frequency = 22.5792 MHz All specified CLKOUT frequencies (generated by PLL or XTAL) are supported CLKOUT outputs (/2, /3, /4, /8 divide) optionally
PLL	01	0	<ul style="list-style-type: none"> Nominal MCLK_INT frequency = 24.576 MHz PDN_PLL = 0 and PLL properly configured to generate 24.576 MHz given reference input frequency on XTI/MCLK pin Only MCLK_INT on CLKOUT is supported on CLKOUT pin CLKOUT outputs (/2, /3, /4, /8 divide) optionally
		1	<ul style="list-style-type: none"> Nominal MCLK_INT frequency = 22.5792MHz PDN_PLL = 0 and PLL properly configured to generate 22.5792 MHz given reference input frequency on XTI/MCLK pin Only MCLK_INT on CLKOUT is supported on CLKOUT pin CLKOUT outputs (/2, /3, /4, /8 divide) optionally
RCO	10	X	<ul style="list-style-type: none"> No MCLK_INT selection necessary. DAC playback is not supported. I2C port and HPIN_x pins are supported.

当通过XTI/MCLK引脚向器件提供PLL参考时钟时，必须符合图4-15所示的相位噪声掩码。

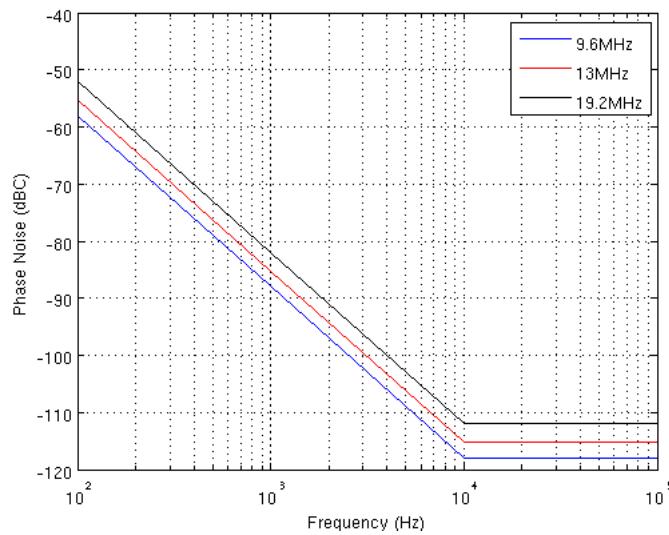


图4-15。有PLL时的MCLK相位噪声掩码

更多限制详见表4-3。

表4-3. MCLK源限制

内部 MCLK 源	MCLK_SRC_SEL	MCLK_INT	限制
直接MCLK 或晶体振荡器	00	0	<ul style="list-style-type: none"> • 标称MCLK_INT频率 = 24.576 MHz • 支持所有指定的CLKOUT频率（由PLL或晶体振荡器生成） • CLKOUT输出（可选/2、/3、/4、/8分频）
		1	<ul style="list-style-type: none"> • 标称MCLK_INT频率 = 22.5792 MHz • 支持所有指定的CLKOUT频率（由PLL或晶体振荡器生成） • CLKOUT输出（可选/2、/3、/4、/8分频）
PLL	01	0	<ul style="list-style-type: none"> • 标称MCLK_INT频率 = 24.576 MHz • PDN_PLL = 0，且PLL已正确配置以在XTI/MCLK引脚输入参考频率下生成24.576 MHz • CLKOUT引脚仅支持MCLK_INT作为CLKOUT • CLKOUT输出（可选/2、/3、/4、/8分频）
		1	<ul style="list-style-type: none"> • 标称MCLK_INT频率 = 22.5792 MHz • PDN_PLL = 0，且PLL已正确配置以在XTI/MCLK引脚输入参考频率下生成22.5792 MHz • CLKOUT引脚仅支持MCLK_INT作为CLKOUT • CLKOUT输出（可选/2、/3、/4、/8分频）
RCO	10	X	<ul style="list-style-type: none"> • 无需选择MCLK_INT。不支持DAC回放。支持I2C端口和HPIN_x引脚。

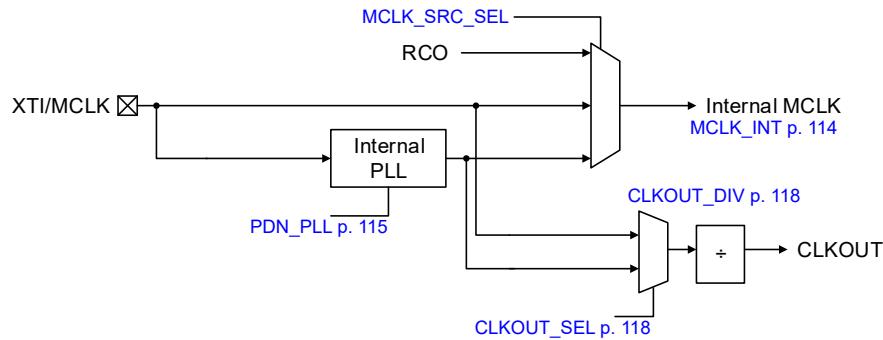


Figure 4-16. MCLK Source Switching

A source to MCLK_INT, either the XTAL (or external MCLK), PLL, or the RCO, must be provided as long as CS43131 is operating; otherwise, the CS43131 will enter a non-responsive state. The only way to recover from this non-responsive state is either through a reset or POR event. Switching MCLK sources during DAC operation causes audible artifacts, but does not put the device in an unrecoverable state. In an MCLK source-switching event, the destined clock source must be present and ready before switching occurs.

After POR or reset event, RCO is selected as default source of MCLK_INT.

4.6.1.1 Internal RC Oscillator

As described in [Section 4.6.1](#), the CS43131 includes an internal RC oscillator that can be used as a clock source for peripheral circuit such as control port or charge pump.

4.7 Clock Output and Fractional-N PLL

The CS43131 clock output can be used as a master clock for other data-conversion or signal-processing components, which requires synchronous timing to the CS43131.

The CLKOUT output is enabled by clearing PDN_CLKOUT.

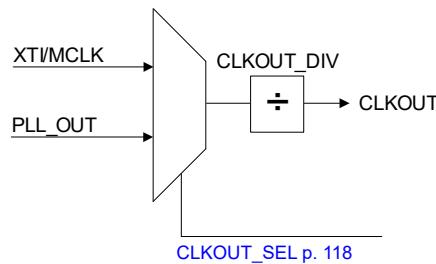


Figure 4-17. CLKOUT Source Selection

Once enabled, CLKOUT is generated either from the internal crystal oscillator output (when used) or from the integrated fractional-N PLL; it can be selected by CLKOUT_SEL. CLKOUT_DIV can be used to set /2, /3, /4, or /8 to divide the selected clock source to targeted frequency.

4.7.1 Fractional-N PLL

The CS43131 has an integrated fractional-N PLL to support the clocking requirements of various applications. This PLL can be enabled or disabled by clearing or setting PDN_PLL bit. The input reference clock for the PLL is signal on XTI/MCLK pin (crystal-generated or external-feed).

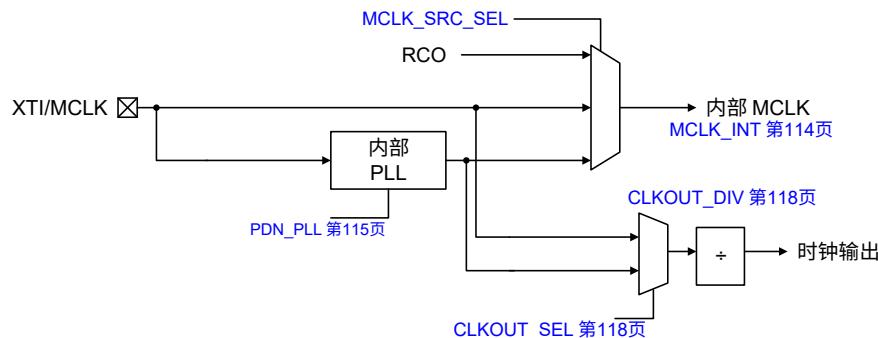


图4-16. MCLK源切换

只要CS43131工作，必须为MCLK_INT提供一个源，可能是晶体振荡器（或外部MCLK）、PLL或RCO；否则，CS43131将进入无响应状态。从该无响应状态恢复的唯一方法是通过复位或上电复位（POR）事件。在DAC运行期间切换MCLK源会导致可听见的杂音，但不会使设备进入不可恢复状态。在MCLK源切换事件中，目标时钟源必须存在且准备就绪后方可切换。

在POR或复位事件后，RCO被选为MCLK_INT的默认时钟源。

4.6.1.1 内部 RC 振荡器

如第4.6.1节所述，CS43131包含一个内部RC振荡器，可用作控制端口或电荷泵等外围电路的时钟源。

4.7 时钟输出与分数-N PLL

CS43131的时钟输出可用作其他数据转换或信号处理组件的主时钟，这些组件需要与CS43131同步定时。

通过清除PDN_CLKOUT可使CLKOUT输出使能。

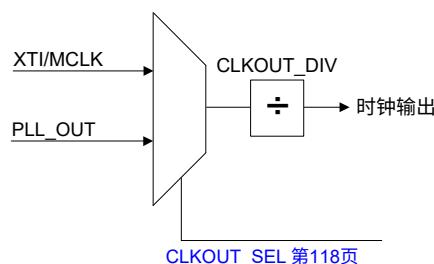


图4-17. CLKOUT时钟源选择

一旦启用，CLKOUT将由内部晶体振荡器输出（如使用）或集成的分数-N PLL生成；可通过CLKOUT_SEL选择。CLKOUT_DIV可用于设置/2、/3、/4或/8，以将所选时钟源分频至目标频率。

4.7.1 分数-N PLL

CS43131集成了分数-N PLL，以满足各种应用的时钟需求。通过清除或设置PDN_PLL位可启用或禁用该PLL。PLL的输入参考时钟为XTI/MCLK引脚上的信号（晶体振荡器输出或外部输入）。

4.7.2 Fractional-N PLL Internal Interface

Fig. 4-18 shows how PLL operation can be configured.

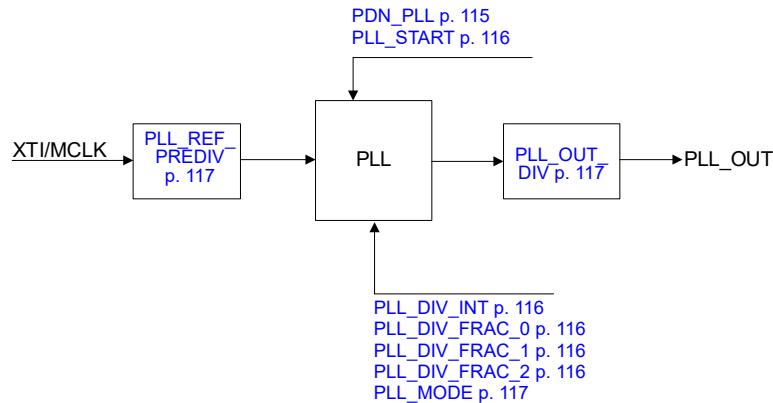


Figure 4-18. Fractional-N PLL

Use Eq. 4-1 to calculate the PLL output frequency.

$$\text{PLL_OUT} = \frac{\text{PLL_REF}}{\text{PLL_REF_PREDIV}} \times \frac{\text{PLL_DIV_INT} + \text{PLL_DIV_FRAC}}{\frac{500}{512} \text{ or } 1, \text{ selected by PLL_Mode}} \times \frac{1}{\text{PLL_OUT_DIV}}$$

Equation 4-1. PLL Output Frequency Equation

PLL_REF source must be in range below:

PLL_REF Source	PLL_REF_PREDIV Input	
	Minimum	Maximum
MCLK/XIN pin	9.6 MHz	26 MHz

Table 4-4 lists common settings with XTAL input as PLL reference.

Table 4-4. PLL Configuration for Typical Use Case (XTAL as the PLL Reference)

XTAL (MHz)	PLL_REF_PREDIV (Divide-by Value)	PLL_REF_PREDIV (Setting)	PLL_DIV_INT	PLL_DIV_FRAC	PLL_OUT_DIV	PLL_MODE	PLL_OUT (MHz)	PLL_CAL_RATIO
22.5792	8	0x3	0x44	0x06 F700	0x08	0	24.576	139
24.576	8	0x3	0x49	0x80 0000	0x0A	1	22.5792	118

Table 4-5 lists common settings with MCLK input as PLL reference.

Table 4-5. PLL Configuration for Typical Use Case (XIN/MCLK as the PLL Reference)

XIN/MCLK (MHz)	PLL_REF_PREDIV (Divide-by Value)	PLL_REF_PREDIV (Setting)	PLL_DIV_INT	PLL_DIV_FRAC	PLL_OUT_DIV	PLL_MODE	PLL_OUT (MHz)	PLL_CAL_RATIO
11.2896	4	0x2	0x40	0x00 0000	0x08	1	22.5792	128
	4	0x2	0x44	0x06 F700	0x08	0	24.576	139
22.5792	8	0x3	0x44	0x06 F700	0x08	0	24.576	139
12.000	4	0x2	0x49	0x80 0000	0x0A	0	22.5792	120
	4	0x2	0x40	0x00 0000	0x08	0	24.576	131
24.000	8	0x3	0x49	0x80 0000	0x0A	0	22.5792	120
	8	0x3	0x40	0x00 0000	0x08	0	24.576	131
12.288	4	0x2	0x49	0x80 0000	0x0A	1	22.5792	118
	4	0x2	0x40	0x00 0000	0x08	1	24.576	128
24.576	8	0x3	0x49	0x80 0000	0x0A	1	22.5792	118
9.600	4	0x2	0x49	0x80 0000	0x08	0	22.5792	151
	4	0x2	0x50	0x00 0000	0x08	0	24.576	164

4.7.2

分数-N PLL 内部接口

图 4-18 展示了 PLL 操作的配置方法。

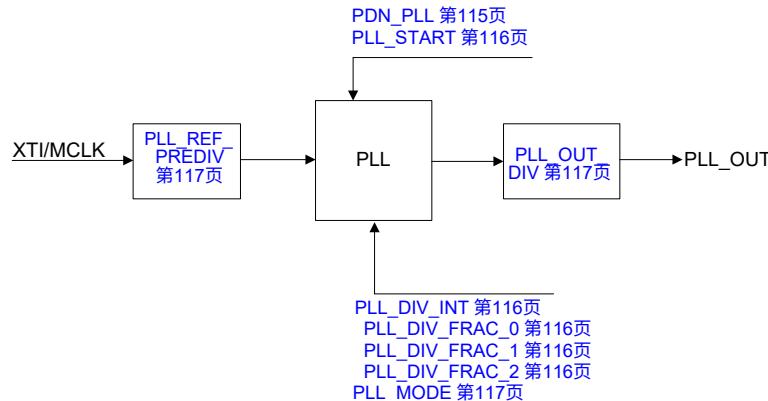


图 4-18. 分数-N PLL

使用公式 4-1 计算 PLL 输出频率。

$$PLL_OUT = \frac{PLL_REF}{PLL_REF_PREDIV} \times \frac{500}{\text{或 } 512 \text{, 由 } PLL_Mode \text{ 选择}} \times \frac{1}{PLL_OUT_DIV}$$

公式 4-1。PLL 输出频率公式

PLL_REF 源必须处于以下范围：

PLL_REF 源	PLL_REF_PREDIV 输入	
	最小值	最大值
MCLK/XIN 引脚	9.6 MHz	26 MHz

表 4-4 列出了以晶体振荡器 (XTAL) 输入作为 PLL 参考的常用设置。

表 4-4。典型应用的 PLL 配置（以晶体振荡器作为 PLL 参考）

晶体振荡器 (MHz)	PLL_REF_PREDIV (分频值)	PLL_REF_PREDIV (设置)	PLL_DIV_INT	PLL_DIV_FRAC	PLL_OUT_DIV	PLL 模式	PLL 输出 (MHz)	PLL_CAL_比率
22.5792	8	0x3	0x44	0x06 F700	0x08	0	24.576	139
24.576	8	0x3	0x49	0x80 0000	0x0A	1	22.5792	118

表 4-5 列出了以主时钟 (MCLK) 输入作为 PLL 参考的常用设置。

表 4-5。典型应用场景的 PLL 配置 (XIN/MCLK 作为 PLL 参考)

XIN/MCLK (MHz)	PLL_REF_PREDIV (分频值)	PLL_REF_PREDIV (设置)	PLL_DIV_INT	PLL_DIV_FRAC	PLL_OUT_DIV	PLL 模式	PLL 输出 (MHz)	PLL_CAL_比率
11.2896	4	0x2	0x40	0x00 0000	0x08	1	22.5792	128
	4	0x2	0x44	0x06 F700	0x08	0	24.576	139
22.5792	8	0x3	0x44	0x06 F700	0x08	0	24.576	139
12.000	4	0x2	0x49	0x80 0000	0x0A	0	22.5792	120
	4	0x2	0x40	0x00 0000	0x08	0	24.576	131
24.000	8	0x3	0x49	0x80 0000	0x0A	0	22.5792	120
	8	0x3	0x40	0x00 0000	0x08	0	24.576	131
12.288	4	0x2	0x49	0x80 0000	0x0A	1	22.5792	118
	4	0x2	0x40	0x00 0000	0x08	1	24.576	128
24.576	8	0x3	0x49	0x80 0000	0x0A	1	22.5792	118
9.600	4	0x2	0x49	0x80 0000	0x08	0	22.5792	151
	4	0x2	0x50	0x00 0000	0x08	0	24.576	164

Table 4-5. PLL Configuration for Typical Use Case (XIN/MCLK as the PLL Reference) (Cont.)

XIN/MCLK (MHz)	PLL_REF_PREDIV (Divide-by Value)	PLL_REF_PREDIV (Setting)	PLL_DIV_INT	PLL_DIV_FRAC	PLL_OUT_DIV	PLL_MODE	PLL_OUT (MHz)	PLL_CAL_RATIO
19.200	8	0x3	0x49	0x80 0000	0x08	0	22.5792	151
	8	0x3	0x50	0x00 0000	0x08	0	24.576	164
13.000	4	0x2	0x45	0x79 7680	0x0A	1	22.5792	111
	4	0x2	0x3C	0x7E A940	0x08	1	24.576	121
26.000	8	0x3	0x45	0x79 7680	0x0A	1	22.5792	111
	8	0x3	0x3C	0x7E A940	0x08	1	24.576	121

Note that in [Table 4-4](#) and [Table 4-5](#):

- The PLL_OUT_DIV value must be even.
- PLL_OUT frequencies are at 22.5792 or 24.576 MHz. CLKOUT frequencies can be obtained by configuring the CLK_OUT_DIV value:

PLL_OUT	CLK_OUT_DIV (2)	CLK_OUT_DIV (3)	CLK_OUT_DIV (4)	CLK_OUT_DIV (8)
22.5792 MHz	11.2896 MHz	7.5264 MHz	5.6448 MHz	2.8224 MHz
24.576 MHz	12.288 MHz	8.192 MHz	6.144 MHz	4.096 MHz

- PLL_ERROR_INT constantly monitors the PLL error status after PLL_START is set, assuming the PLL reference input is stable and accurate.

4.7.2.1 Powering Up the PLLs

To power up the PLL, use the following default sequence:

1. Enable the PLL by clearing PDN_PLL.
2. Configure PLL_REF_PREDIV.
3. Configure PLL_OUT_DIV.
4. Configure the three fractional factor registers, PLL_DIV_FRAC.
5. Set the integer factor, PLL_DIV_INT, to the desired value.
6. Configure PLL_MODE and PLL_CAL_RATIO.
7. After properly unmasked (clearing PLL_READY_INT_MASK and PLL_ERROR_INT_MASK), PLL_READY_INT, and PLL_ERROR_INT are used to monitor if PLL has been successfully started.
8. Turn on the PLL by setting PLL_START.

4.7.2.2 Powering Down the PLL

1. Clear PLL_START to stop the PLL operation.
2. For further power saving, set PDN_PLL to disable the PLL block.

4.8 Filtering Options

To accommodate the increasingly complex requirements of digital audio systems, the CS43131 incorporates selectable filters in different playback modes.

For PCM/TDM mode, the following interpolation filtering options can be selected:

- Fast roll-off and slow roll-off interpolation filter options.
- In each option above, both low-latency and normal phase-compensation filtering options can be used.
- Nonoversampling (NOS) mode is provided, which minimizes the internal digital processing. Once NOS mode is set, the settings on the above two options are ignored.

表 4-5。典型使用场景的PLL配置 (XIN/MCLK作为PLL参考) (续)

XIN/MCLK (MHz)	PLL_REF_PREDIV (分频值)	PLL_REF_PREDIV (设置)	PLL_DIV_INT	PLL_DIV_FRAC	PLL_OUT_DIV	PLL_ 模式	PLL 输出 (MHz)	PLL_CAL_ 比率
19.200	8	0x3	0x49	0x80 0000	0x08	0	22.5792	151
	8	0x3	0x50	0x00 0000	0x08	0	24.576	164
13.000	4	0x2	0x45	0x79 7680	0x0A	1	22.5792	111
	4	0x2	0x3C	0x7E A940	0x08	1	24.576	121
26.000	8	0x3	0x45	0x79 7680	0x0A	1	22.5792	111
	8	0x3	0x3C	0x7E A940	0x08	1	24.576	121

注意表4-4和表4-5：

- PLL_OUT_DIV 值必须为偶数。
- PLL_OUT 频率为22.5792 MHz或24.576 MHz。通过配置 CLK_OUT_DIV 值可获得 CLKOUT 频率：

PLL_OUT	CLK_OUT_DIV (2)	CLK_OUT_DIV (3)	CLK_OUT_DIV (4)	CLK_OUT_DIV (8)
22.5792 MHz	11.2896 MHz	7.5264 MHz	5.6448 MHz	2.8224 MHz
24.576 MHz	12.288 MHz	8.192 MHz	6.144 MHz	4.096 MHz

- PLL_ERROR_INT 在设置 PLL_START 后持续监测 PLL 错误状态，前提是 PLL 参考输入稳定且准确。

4.7.2.1 PLL 上电

要启动PLL，请使用以下默认序列：

1. 通过清除PDN_PLL使能PLL。
2. 配置PLL_REF_PREDIV。
3. 配置PLL_OUT_DIV。
4. 配置三个分数因子寄存器PLL_DIV_FRAC。
5. 将整数因子PLL_DIV_INT设置为所需值。
6. 配置PLL_MODE和PLL_CAL_RATIO。
7. 在正确取消屏蔽（清除PLL_READY_INT_MASK和PLL_ERROR_INT_MASK）后，使用PLL_READY_INT和PL_L_ERROR_INT监控PLL是否成功启动。
8. 通过设置PLL_START开启PLL。

4.7.2.2 关闭PLL电源

1. 清除PLL_START以停止PLL操作。
2. 为进一步节能，设置PDN_PLL以禁用PLL模块。

4.8 滤波选项

为满足数字音频系统日益复杂的需求，CS43131在不同播放模式中集成了可选滤波器。

对于PCM/TDM模式，可选择以下插值滤波选项：

- 快速衰减和慢速衰减插值滤波选项。
- 上述每种选项中均可使用低延迟和正常相位补偿滤波选项。
- 提供非过采样 (NOS) 模式，以最小化内部数字处理。一旦设置为NOS模式，上述两个选项的设置将被忽略。

The combination of the options results in five different filter combinations. The specifications for each filter can be found in [Table 3-9](#), and response plots can be found in [Section 9](#). These filters have been designed to accommodate a variety of musical tastes and styles. The PCM filter option register (see [Section 7.5.2](#)) is used to select filter options.

When in octuple-speed mode, the filter options above are not available and the internal digital processing is minimized. See the specification in [Table 3-9](#) for filter characteristics.

The DSD processor mode uses a decimation-free DSD processing technique that allows for features such as matched PCM level output, DSD volume control, and 50-kHz on-chip filter.

4.9 Audio Serial Port (ASP)

The independent, highly configurable ASPs and auxiliary serial ports (XSPs) communicate audio data from other system devices, such as applications processors. Both ports can be configured to support common audio interfaces, TDM/I²S and left-justified (LJ).

ASP supports both PCM and DoP stream playback. XSP can only support DoP stream playback. For DAC playback, only one port needs to be enabled. Both ports are enabled only in specific application, such as PCM notification mixing with DSD/DoP content. Details regarding this application setup can be found in [Section 4.12](#).

In this section, the reference to both ports is generalized as “xSP” to explain the common settings between the two ports.

4.9.1 Master and Slave Timing

Each serial port can operate as either the master of timing or as a slave to another device's timing. If xSP_M/S is set, the serial port acts as a clock master. If xSP_M/S is cleared, the serial port acts as a clock slave.

- In Master Mode, xSP_SCLK and xSP_LRCK are outputs derived from the internal MCLK.
- In Slave Mode, xSP_SCLK and xSP_LRCK are inputs. Although the CS43131 does not generate the interface timings in Slave Mode, the expected LRCK and SCLK format must be programmed in the same way as in Master Mode (see [Table 3-20](#)).
- In both modes, the serial port sample rate register (xSP_SPRATE) must be set per audio content before enabling the serial port.
- When using ASP for PCM playback, the audio serial port sample bit size register (ASP_SPSIZE) must be set per audio content before enabling the ASP.
- When using XSP or ASP for DoP playback, the serial port sample bit size register (XSP_SPSIZE or ASP_SPSIZE) must be set per audio content before enabling the XSP or ASP. Note that the XSP_SPSIZE or ASP_SPSIZE must reflect the length of both DSD marker bits together with audio bits.

4.9.2 Power-Up, Power-Down, and Tristate

The xSP has separate power-down and tristate controls (PDN_xSP and xSP_3ST) for input data paths, which minimizes power consumption if the input port is not used. xSP master/slave operation is controlled only by the xSP_M/S setting, irrespective of the PDN_xSP and xSP_3ST settings.

- PDN_xSP. If a serial port's SDIN functionality is not required, xSP can be powered down by setting PDN_xSP, which powers down the input data path and clocks of the serial port.
- xSP_3ST. In Master Mode, setting xSP_3ST tri-states the SCLK and LRCK clocks. Before setting an xSP_3ST bit, the associated serial port must be powered down and must not be powered up until the xSP_3ST bit is cleared. In Slave Mode, xSP_3ST does not affect the functionality of SCLK and LRCK clocks, given both pins are input pins.

4.9.3 I/O

The ASP port is associated with SDIN1, SCLK1, and LRCK1. The XSP port is associated with SDIN2, SCLK2, and LRCK2, which are shared with DSD interface:

- SCLKx—Serial data shift clock

这些选项的组合形成五种不同的滤波器组合。各滤波器的规格详见表3-9，响应曲线详见第9节。这些滤波器设计旨在满足多样的音乐品味和风格。PCM滤波器选项寄存器（见第7.5.2节）用于选择滤波器选项。

在八倍速模式下，上述滤波器选项不可用，且内部数字处理被最小化。
滤波器特性详见表3-9的规格。

DSD处理器模式采用无抽取DSD处理技术，支持匹配PCM电平输出、DSD音量控制及50 kHz片上滤波器等功能。

4.9 音频串行端口 (ASP)

独立且高度可配置的ASP和辅助串行端口 (XSP) 用于与其他系统设备（如应用处理器）通信音频数据。两个端口均可配置为支持常见音频接口，TDM/I²S 及左对齐 (LJ) 格式。

ASP 支持 PCM 和 DoP 流播放。XSP 仅支持 DoP 流播放。对于 DAC 播放，仅需启用一个端口。仅在特定应用中启用两个端口，例如 PCM 通知与 DSD/DoP 内容混合。有关此应用设置的详细信息，请参见第 4.12 节。

本节中，两个端口统称为“xSP”，以说明两个端口的通用设置。

4.9.1 主从时序

每个串行端口可作为时钟主设备或从设备运行。若设置 xSP_M/S，串行端口作为时钟主设备。若清除 xSP_M/S，串行端口作为时钟从设备。

- 在主模式下，xSP_SCLK 和 xSP_LRCK 是由内部 MCLK 派生的输出信号。
- 在从模式下，xSP_SCLK 和 xSP_LRCK 为输入信号。尽管 CS43131 在从模式下不生成接口时序，但预期的 LRCK 和 SCLK 格式必须与主模式中相同方式编程（参见表 3-20）。
- 在两种模式下，串行端口采样率寄存器 (xSP_SPRATE) 必须根据音频内容设置后，方可启用串行端口。
- 使用 ASP 进行 PCM 播放时，音频串行端口采样位宽寄存器 (ASP_SPSIZE) 必须根据音频内容设置后，方可启用 ASP。
- 使用 XSP 或 ASP 进行 DoP 播放时，串行端口采样位宽寄存器 (XSP_SPSIZE 或 ASP_SPSIZE) 必须根据音频内容设置后，方可启用 XSP 或 ASP。请注意，XSP_SPSIZE 或 ASP_SPSIZE 必须反映 DSD 标记位与音频位的总长度。

4.9.2 上电、断电及三态

xSP 具有独立的掉电和三态控制 (PDN_xSP 和 xSP_3ST) 用于输入数据路径，当输入端口未使用时，可最大限度降低功耗。xSP 主/从操作仅由 xSP_M/S 设置控制，与 PDN_xSP 和 xSP_3ST 设置无关。

- PDN_xSP。如果不需要串行端口的 SDIN 功能，可通过设置 PDN_xSP 对 xSP 进行掉电，从而关闭串行端口的输入数据路径和时钟。
- xSP_3ST。在主模式下，设置 xSP_3ST 会使 SCLK 和 LRCK 时钟进入三态状态。在设置 xSP_3ST 位之前，必须先对相关串行端口进行掉电，且在清除 xSP_3ST 位之前不得重新上电。在从模式下，xSP_3ST 不影响 SCLK 和 LRCK 时钟的功能，因为这两个引脚均为输入引脚。

4.9.3 输入/输出

ASP端口关联串行数据输入1 (SDIN1)、串行时钟1 (SCLK1) 和左右时钟1 (LRCK1)。XSP端口关联串行数据输入2 (SDIN2)、串行时钟2 (SCLK2) 和左右时钟2 (LRCK2)，这些信号与DSD接口共享：

- SCLKx—串行数据移位时钟

- LRCKx—Toggles at external sample rate ($F_{s_{ext}}$). LRCK (left/right, I²S) identifies each channel's (left or right) location in the data word when I²S format is used. LRCK identifies the start of each serialized data word. FSYNC (frame sync clock, TDM) identifies the start of each TDM frame.
- SDINx—Serial data input

4.9.4 High-Impedance Mode

Serial ports can be placed on a clock bus that allows multiple masters without the need for external buffers. xSP_3ST bits place the internal buffers for the respective serial-port interface signals in a high-impedance state, allowing another device to transmit clocks without bus contention. When the CS43131 serial port is a timing slave, its SCLK and LRCK I/Os are always inputs and are thus unaffected by the xSP_3ST control. Fig. 4-19 shows the busing for CS43131 master timing serial-port use case.

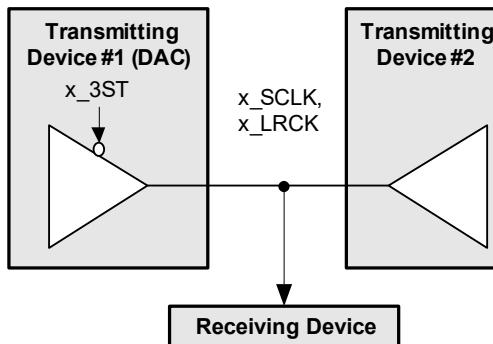


Figure 4-19. Serial Port Busing when Master Timed

4.9.5 Clock Generation and Control

The CS43131 has a flexible serial port clock generation subsystem that allows independent clocking of the two serial ports. When operating as a master port, the serial port provides a bit clock (xSP_SCLK) and a left-right/frame sync signal (xSP_LRCK/FSYNC).

Fig. 4-20 and Fig. 4-21 show the serial port clocking architecture.

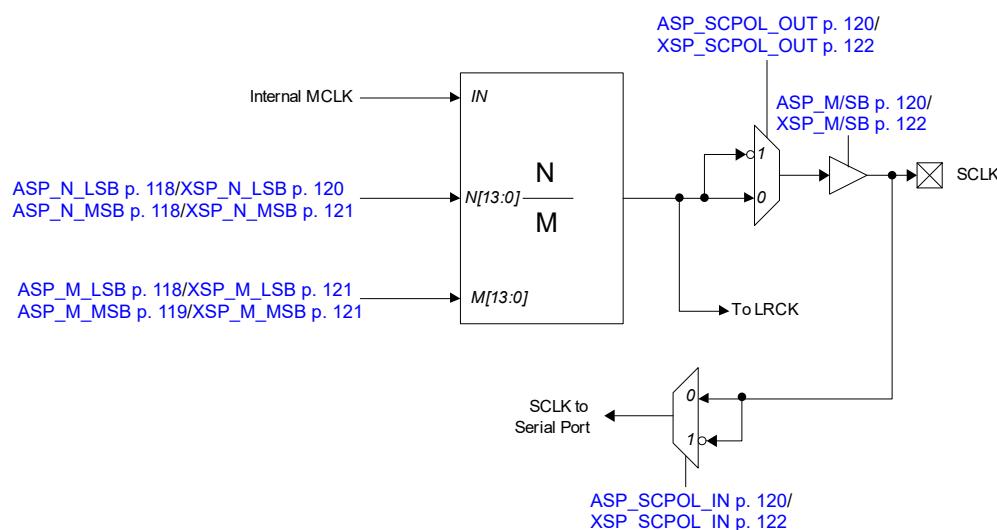
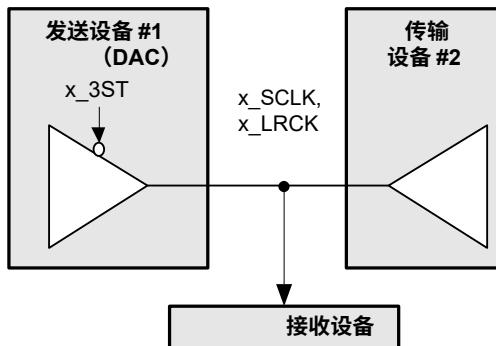


Figure 4-20. xSP SCLK and MCLK Architecture

- LRCKx—以外部采样频率 (Fs) 切换。LRCK (左右, I²S) 用于标识在使用I²S格式时数据字中每个通道 (左或右) 的位置。LRCK标识每个串行数据字的起始。FSYNC (帧同步时钟, TDM) 标识每个TDM帧的起始。
- SDINx—串行数据输入

4.9.4 高阻抗模式

串行端口可置于允许多主设备的时钟总线上，无需外部缓冲器。xSP_3ST位将相应串行端口接口信号的内部缓冲器置于高阻抗状态，允许其他设备传输时钟而不会产生总线冲突。当 CS43131 串行端口作为时序从属时，其 SCLK 和 LRCK 输入/输出端口始终为输入端口，因此不受 xSP_3ST 控制的影响。图 4-19 显示了 CS43131 主时序串行端口的总线连接示意图。



注：x 表示 XSP 或 ASP

图 4-19。主时序下的串行端口总线连接

4.9.5 时钟生成与控制

CS43131 具有灵活的串行端口时钟生成子系统，允许两个串行端口独立时钟驱动。

作为主端口工作时，串行端口提供位时钟 (xSP_SCLK) 和左右声道/帧同步信号 (xSP_LRCK/FSYNC)。

图 4-20 和图 4-21 展示了串行端口的时钟架构。

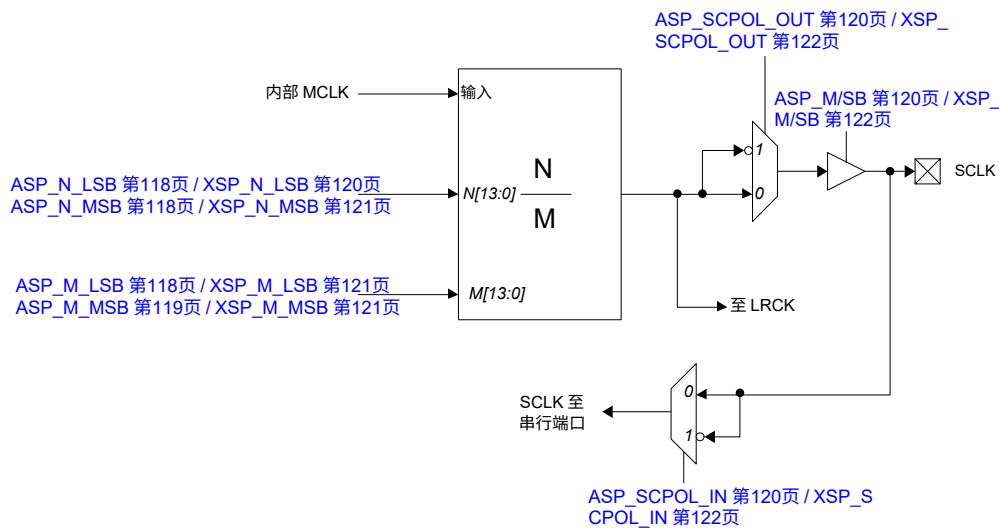


图 4-20。xSP SCLK 与 MCLK 架构

As shown in Fig. 4-20, the master-mode SCLK output for each serial port is derived from the internal MCLK. The SCLK output can be configured to various frequencies to accommodate many sample rates, sample sizes, and channel counts. The SCLK is output of a fractional divide from the internal MCLK input, where N is the numerator and M is the denominator.

Note: Depending on the chosen fractional divide configuration, the SCLK duty cycle can vary by one MCLK period.

Input and output SCLK polarity controls (xSP_SCPOL_IN and xSP_SCPOL_OUT) are also available. As shown in Fig. 4-20, if Master Mode is used, both polarity controls affect the SCLK used by the serial port module. For example, both polarity controls must be set (xSP_SCPOL_IN = xSP_SCPOL_OUT = 1) to invert the SCLK output and output data on the falling edge. In typical use cases, the values of xSP_SCPOL_IN equals xSP_SCPOL_OUT in each serial port. See Fig. 4-23 for example waveforms showing the various settings of the SCLK polarity controls.

Likewise, input and output LRCK polarity controls (xSP_LCPOL_IN and xSP_LCPOL_OUT) are available. In Master Mode, both LRCK polarity controls affect the LRCK used by the serial-port module as shown in Fig. 4-21. In typical-use cases, the value of xSP_LCPOL_IN equals xSP_LCPOL_OUT in each serial port.

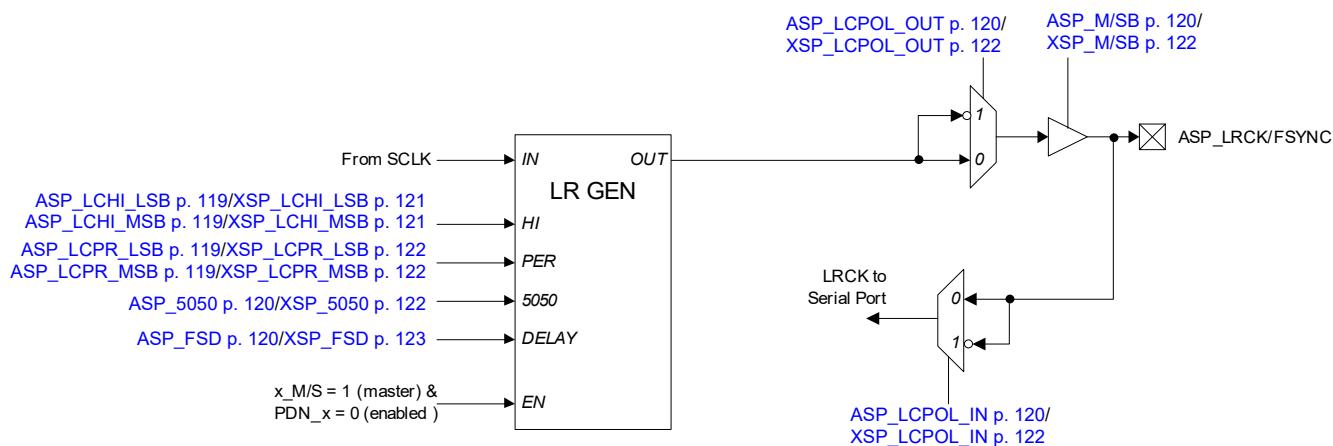


Figure 4-21. xSP LRCK Architecture

As shown in Fig. 4-22, xSP_LCPR determines the LRCK/FSYNC period, in units of SCLK periods. The LRCK period effectively sets the length of the frame and the number of SCLK periods per Fs. Frame length may be programmed in single SCLK period multiples from a minimum of 16 SCLK:Fs up to 1536 SCLK:Fs.

The LRCK-high width (xSP_LCHI) controls the number of SCLK periods for which the LRCK signal is held high during each frame. Like the LRCK period, the LRCK-high width is programmable in single SCLK periods, from a minimum of one period to a maximum of the LRCK period minus one (and an absolute maximum of 768 SCLK periods). That is, LRCK-high width must be less than the LRCK period.

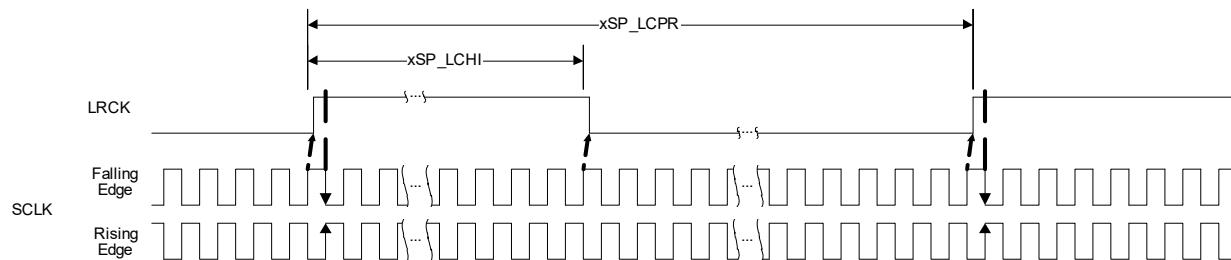


Figure 4-22. xSP LRCK Period, High Width

如图4-20所示，每个串行端口的主模式SCLK输出源自内部MCLK。SCLK输出可配置为多种频率，以适应多种采样率、采样位数和通道数。

SCLK是内部MCLK输入的分数分频输出，其中N为分子，M为分母。

注意：根据所选的分数分频配置，SCLK的占空比可能会变化一个MCLK周期。

输入和输出 SCLK 极性控制 (xSP_SCPOL_IN 和 xSP_SCPOL_OUT) 也可用。如图 4-20 所示，若使用主模式，则两个极性控制均会影响串行端口模块所用的 SCLK。例如，必须同时设置两个极性控制 (xSP_SCPOL_IN = xSP_SCPO L_OUT = 1)，以反转 SCLK 输出并在下降沿输出数据。在典型用例中，每个串行端口的 xSP_SCPOL_IN 值均等于 xSP_SCPO L_OUT。有关 SCLK 极性控制各种设置的示例波形，请参见图 4-23。

同样，输入和输出 LRCK 极性控制 (xSP_LCPOL_IN 和 xSP_LCPOL_OUT) 也可用。在主模式下，如图4-21所示，两个LRCK极性控制均影响串行端口模块所使用的LRCK信号。在典型使用情况下，每个串行端口中xSP_LCPOL_IN的值等于xSP_LCPOL_OUT。

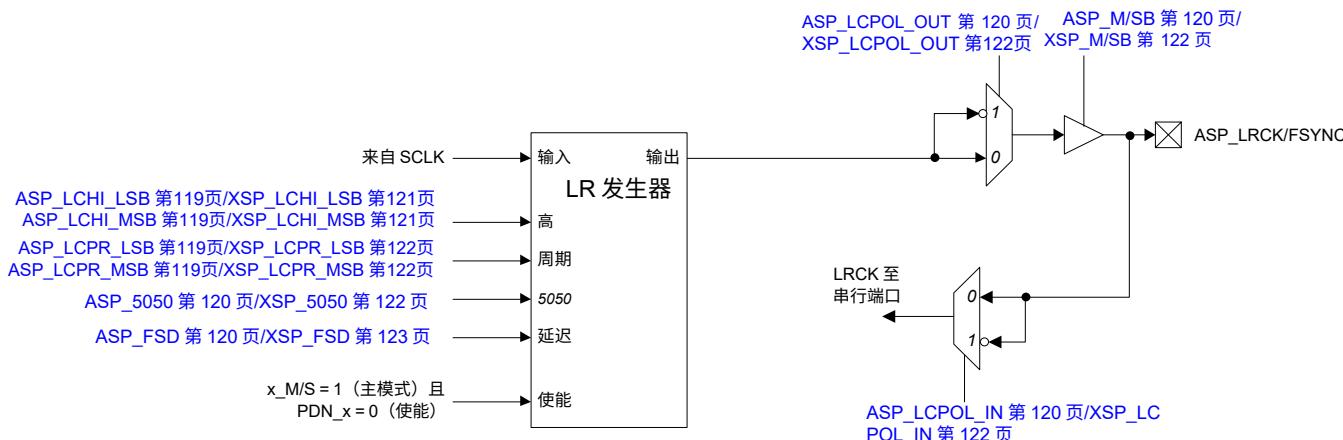


图4-21 xSP LRCK架构

如图4-22所示，xSP_LCPR决定LRCK/FSYNC周期，单位为SCLK周期。LRCK周期有效设定了帧长度及每个采样频率 (Fs) 对应的SCLK周期数。帧长度可编程为单个SCLK周期的整数倍，范围从最小16个SCLK:Fs至最大1536个SCLK:Fs。

LRCK高电平宽度 (xSP_LCHI) 控制每帧中LRCK信号保持高电平的SCLK周期数。与LRCK周期类似，LRCK高电平宽度可编程为单个SCLK周期，范围从最小1个周期至最大LRCK周期减1（绝对最大值为768个SCLK周期）。即 LRCK 高电平宽度必须小于 LRCK 周期。

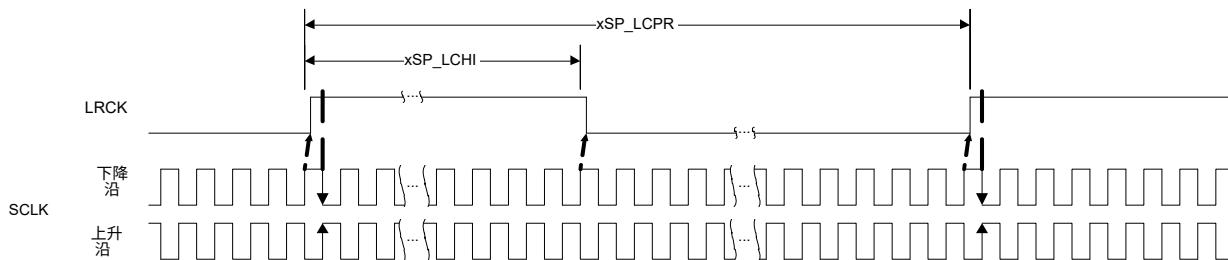


图 4-22。xSP LRCK 周期，高电平宽度

As shown in Fig. 4-23, if Serial Port 50/50 Mode is enabled ($xSP_5050 = 1$), the LRCK high duration must be programmed to the LRCK period divided by two (rounded down to the nearest integer when the LRCK period is odd). When the serial port is in 50/50 Mode, setting the LRCK high duration to a value other than half of the period results in erroneous operation.

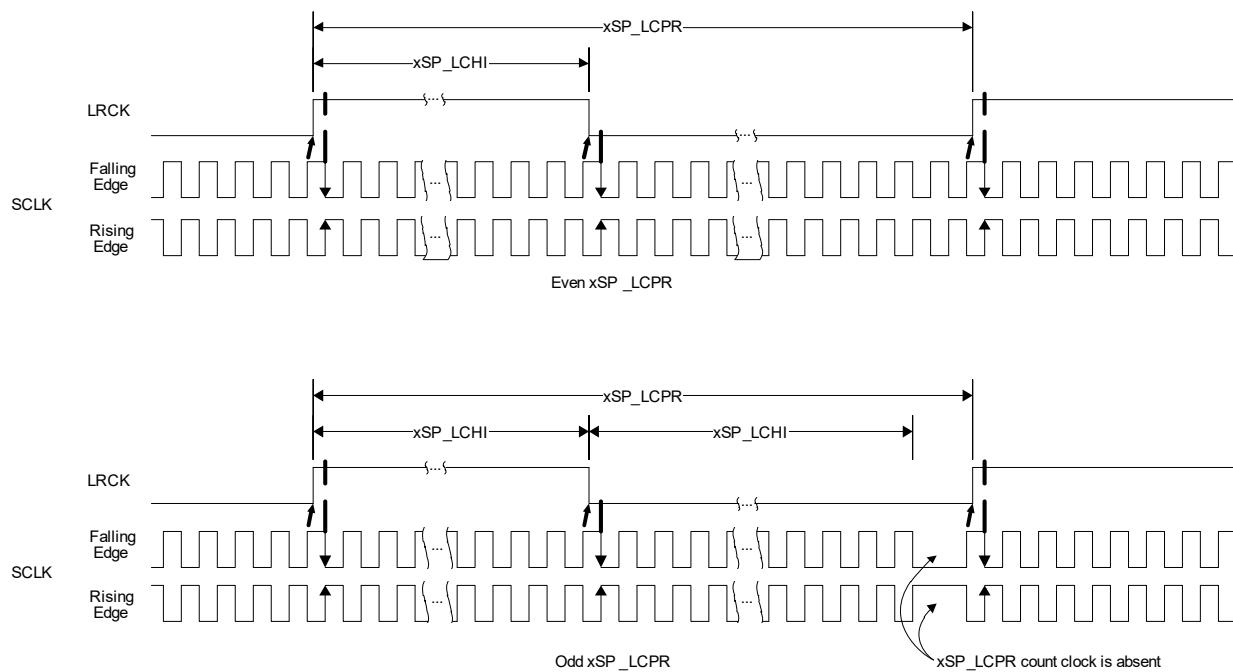


Figure 4-23. xSP_LRCK Period, High Width, 50/50 Mode

如图4-23所示，若启用串行端口50/50模式 ($xSP_5050 = 1$)，则LRCK高电平持续时间为LRCK周期的一半（当LRCK周期为奇数时，向下取整至最接近的整数）。当串行端口处于50/50模式时，将LRCK高电平持续时间设置为非周期一半的值将导致错误操作。

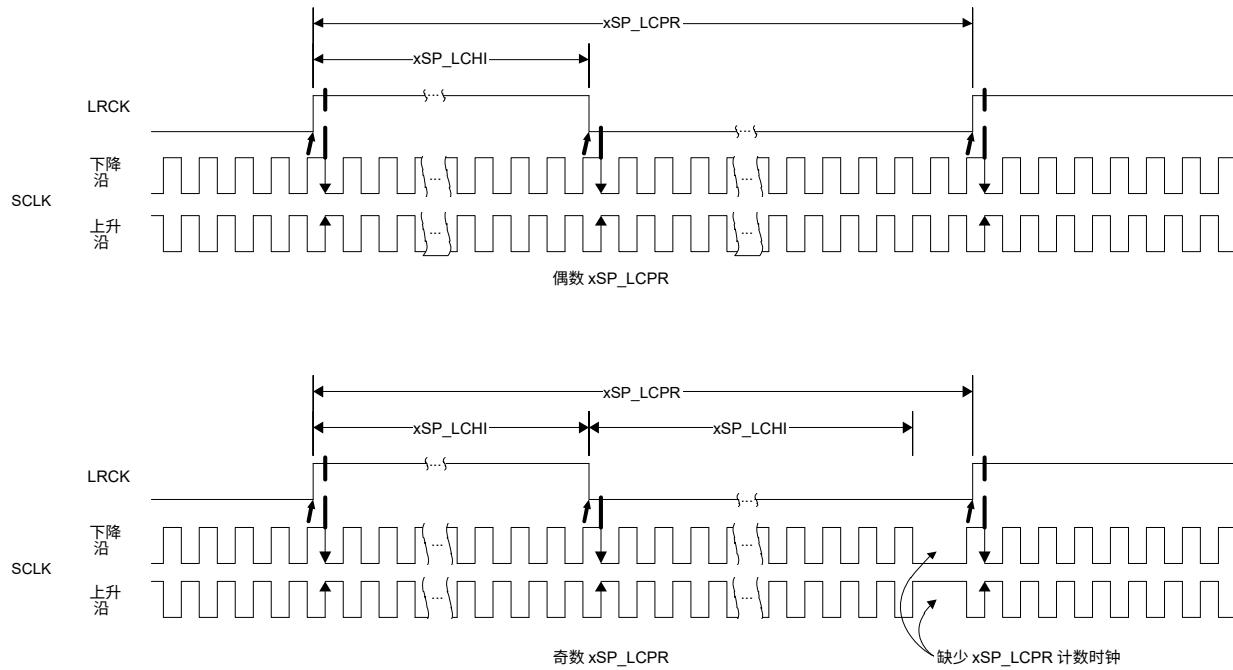


图4-23。xSP_LRCK 周期，高电平宽度，50/50 模式

Fig. 4-24 shows how LRCK frame start delay (xSP_FSD) controls the number of SCLK periods delay from the LRCK synchronization edge to the start of frame data.

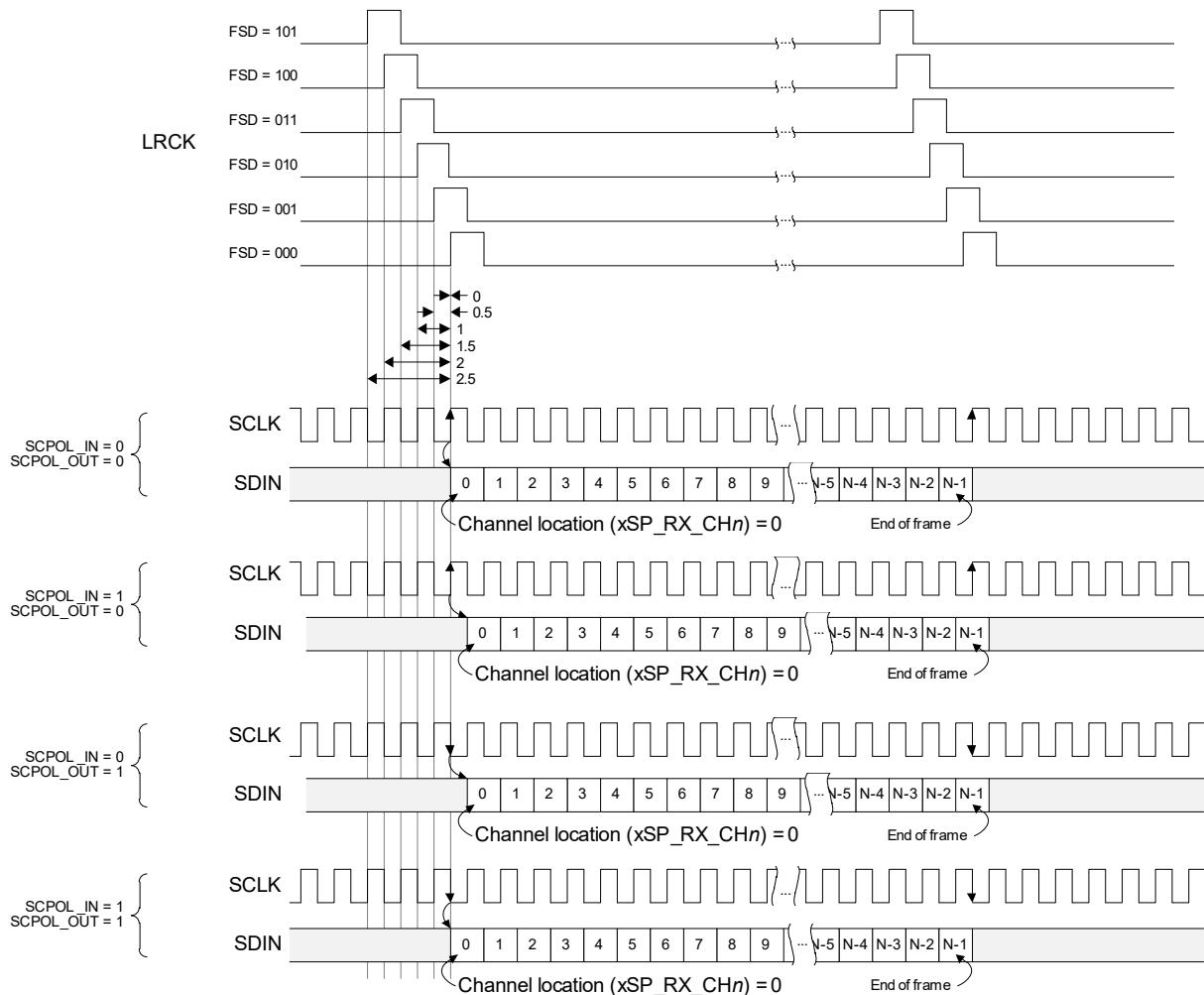


Figure 4-24. LRCK FSD and SCLK Polarity Example Diagram

Table 4-6. Serial Port Clock Generation—Supported Configurations for 32 bits and 2 Channels

Frequency (MHz)	LRCK/FSYNC Rate (kHz)	SCLKs per LRCK Frame		xSP_N[15:0]	xSP_M[15:0]
		xSP_LCPRI + 1	xSP_LCPRI[10:0]		
22.5792	32.000	64	63	40	441
	44.100	64	63	1	8
	48.000	64	63	20	147
	88.200	64	63	1	4
	96.000	64	63	40	147
	176.400	64	63	1	2
	192.000	64	63	80	147
	352.800	64	63	1	1
24.576	32.000	64	63	1	12
	44.100	64	63	147	1280
	48.000	64	63	1	8
	88.200	64	63	147	640
	96.000	64	63	1	4
	176.400	64	63	147	320
	192.000	64	63	1	2
	352.800	64	63	147	160
	384.000	64	63	1	1

图 4-24 显示了 LRCK 帧起始延迟 (xSP_FSD) 如何控制从 LRCK 同步边沿到帧数据起始的 SCLK 周期数延迟。

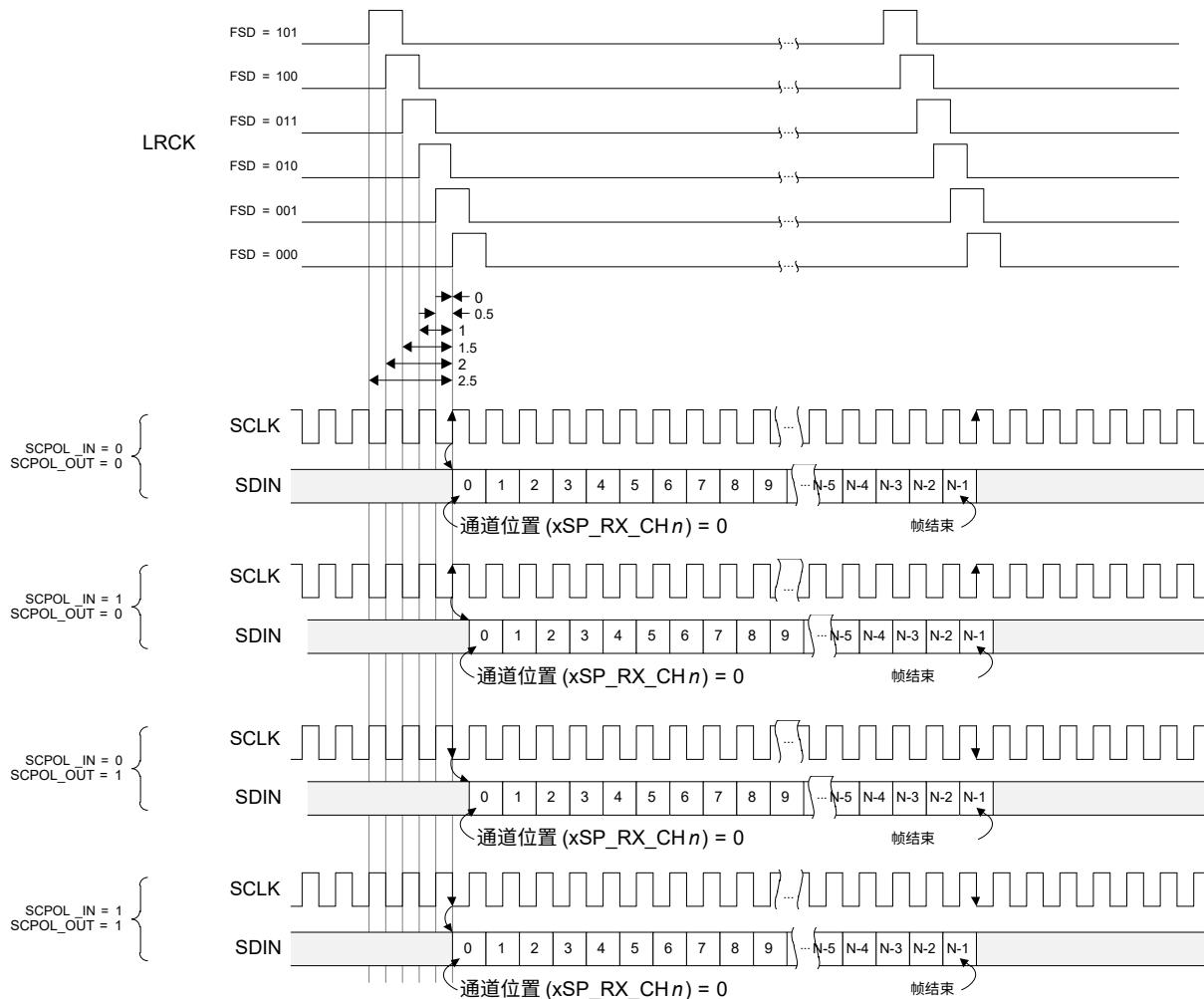


图 4-24。LRCK FSD 与 SCLK 极性示意图

表 4-6。串行端口时钟生成——支持的 32 位 2 通道配置

频率 (MHz)	LRCK/FSYNC 速率 (kHz)	每个 LRCK 帧的 SCLK 数		xSP_N[15:0]	xSP_M[15:0]
		xSP_LCPR + 1	xSP_LCPR[10:0]		
22.5792	32.000	64	63	40	441
	44.100	64	63	1	8
	48.000	64	63	20	147
	88.200	64	63	1	4
	96.000	64	63	40	147
	176.400	64	63	1	2
	192.000	64	63	80	147
	352.800	64	63	1	1
24.576	32.000	64	63	1	12
	44.100	64	63	147	1280
	48.000	64	63	1	8
	88.200	64	63	147	640
	96.000	64	63	1	4
	176.400	64	63	147	320
	192.000	64	63	1	2
	352.800	64	63	147	160
	384.000	64	63	1	1

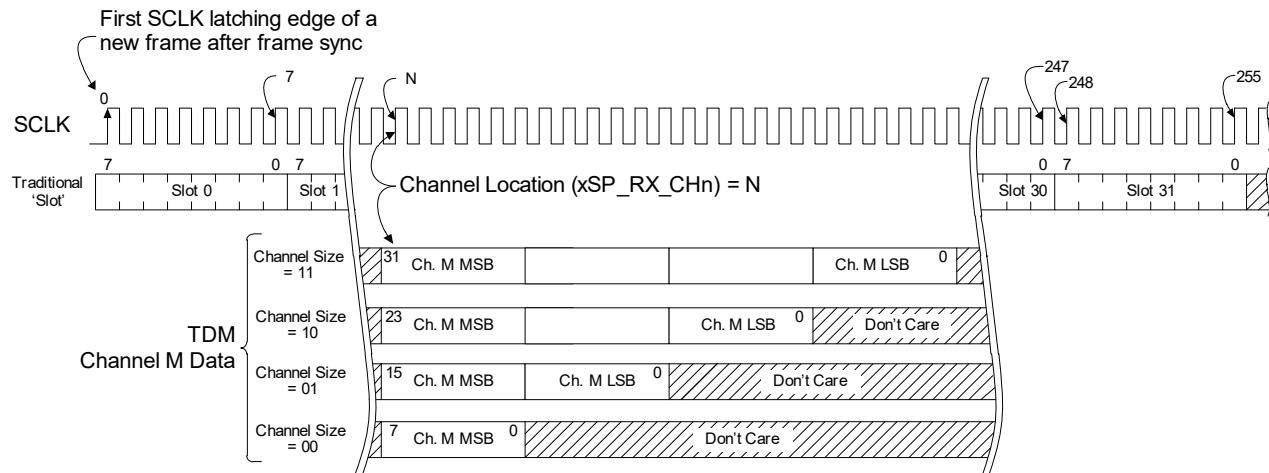
Table 4-7. Serial Port Clock Generation—Supported Configurations for 32-bits and 4-Channels

Frequency (MHz)	LRCK/FSYNC Rate (kHz)	SCLKs per LRCK Frame		xSP_N[15:0]	xSP_M[15:0]
		xSP_LCPR + 1	xSP_LCPR[10:0]		
22.5792	32.000	128	127	80	441
	44.100	128	127	1	4
	48.000	128	127	40	147
	88.200	128	127	1	2
	96.000	128	127	80	147
	176.400	128	127	1	1
24.576	32.000	128	127	1	6
	44.100	128	127	147	640
	48.000	128	127	1	4
	88.200	128	127	147	320
	96.000	128	127	1	2
	176.400	128	127	147	160
	192.000	128	127	1	1

4.9.6 Channel Location and Size

Each serial-port channel has a programmable location offset (xSP_RX_CHn). Channel location is programmable in single SCLK period resolution. When set to the minimum location offset, the channel transmits or receives on the first SCLK period of a new frame.

Channel size is programmable in byte resolution from 8 to 32 bits using xSP_RX_CHn_RES. Channel size and location must not be programmed such that channel data extends beyond the frame boundary. Size and location must not be programmed such that data from a given SCLK period is assigned to more than one channel. The example in [Fig. 4-25](#) shows channel location and size.


Figure 4-25. Example Channel Location and Size

4.9.7 Frame Start Phase

The serial port can start a frame when xSP_LRCK/FSYNC is high or low, depending on xSP_STP. In typical TDM use cases, a frame starts when FSYNC is high (xSP_STP = 1).

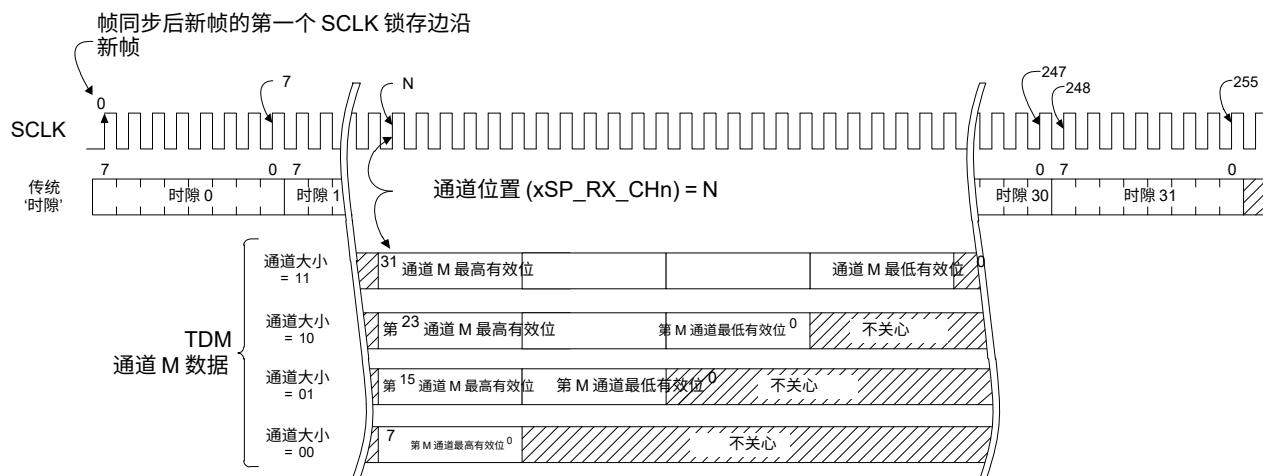
表 4-7。串口时钟生成——支持的 32 位和 4 通道配置

频率 (MHz)	LRCK/FSYNC 速率 (kHz)	每个 LRCK 帧的 SCLK 数		xSP_N[15:0]	xSP_M[15:0]
		xSP_LCPR + 1	xSP_LCPR[10:0]		
22.5792	32.000	128	127	80	441
	44.100	128	127	1	4
	48.000	128	127	40	147
	88.200	128	127	1	2
	96.000	128	127	80	147
	176.400	128	127	1	1
24.576	32.000	128	127	1	6
	44.100	128	127	147	640
	48.000	128	127	1	4
	88.200	128	127	147	320
	96.000	128	127	1	2
	176.400	128	127	147	160
	192.000	128	127	1	1

4.9.6 通道位置与大小

每个串行端口通道具有可编程的位置偏移 (xSP_RX_CHn)。通道位置可编程，分辨率为单个 SCLK 周期。当设置为最小位置偏移时，通道在新帧的第一个 SCLK 周期传输或接收数据。

通道大小可通过 xSP_RX_CHn_RES 以字节为单位编程，范围为 8 至 32 位。通道大小和位置不得编程为使通道数据超出帧边界。大小和位置不得编程为使同一 SCLK 周期的数据分配给多个通道。图 4-25 中的示例显示了通道位置和大小。


图 4-25。示例通道位置与大小

4.9.7 帧起始相位

串口可根据 xSP_STP 在 xSP_LRCK/FSYNC 为高或低时启动帧。在典型的 TDM 应用中，帧在 FSYNC 为高时开始 (xSP_STP = 1)。

- If $xSP_STP = 0$, the frame begins when LRCK/FSYNC transitions from high to low. See Fig. 4-26 for an example in 50/50 mode. The TDM Mode behaves similarly.

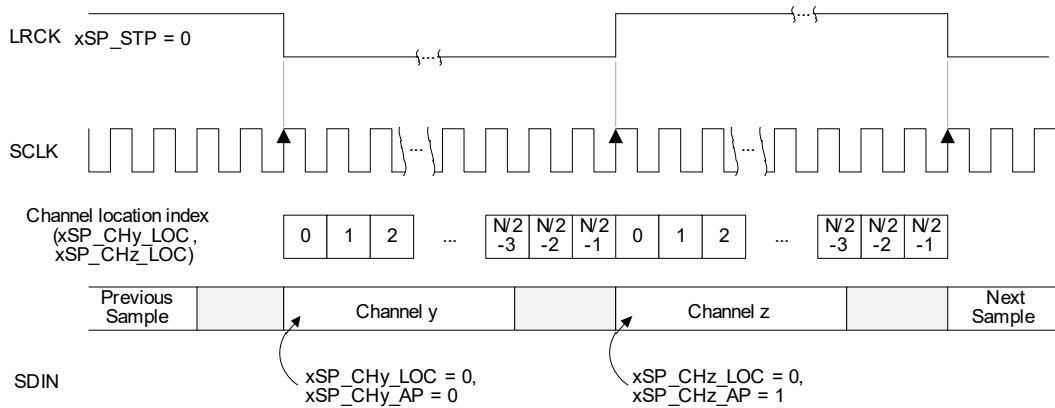


Figure 4-26. Example 50/50 Mode (ASP_STP = 0)

- If $xSP_STP = 1$, the frame begins when LRCK/FSYNC transitions from low to high. See Fig. 4-27 for an example in 50/50 mode. TDM mode is similar.

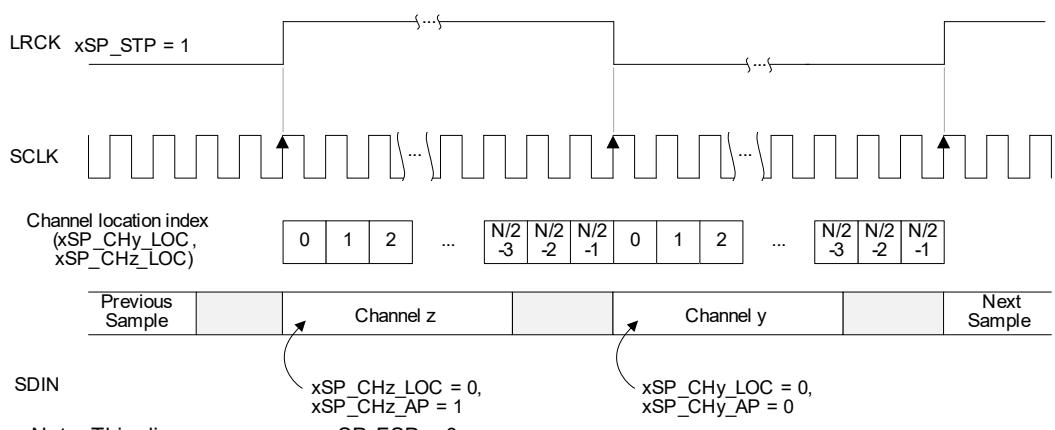


Figure 4-27. Example 50/50 Mode (ASP_STP = 1)

4.9.8 50/50 Mode

In typical two-channel I²S operation (50/50 Mode, $xSP_5050 = 1$), the LRCK duty cycle is 50%, and each channel is transferred during one of the two LRCK phases. In this mode, each serial port channel can be independently programmed to output when LRCK/FSYNC is high or low; this is called the *channel-active phase*.

If the active-phase control bit ($xSP_RX_Chn_AP$) is set, the respective channel is output when LRCK/FSYNC is high. If $xSP_RX_Chn_AP$ is cleared, the respective channel is output if LRCK/FSYNC is low. Examples of each setting of $xSP_RX_Chn_AP$ are shown in Fig. 4-26 and Fig. 4-27.

In 50/50 Mode, the channel location (see Section 4.9.6) is calculated within the channel-active phase. If there are N bits in a frame, the location of the last bit of each active phase is equal to $(N/2) - 1$.

Note: If xSP_5050 is set, xSP_LCHI must be programmed to half of xSP_LCPR for a 50% duty cycle. Also, only two channels can be enabled for the corresponding serial port.

- 当 $xSP_STP = 0$ 时，帧在 LRCK/FSYNC 从高电平跳变至低电平时开始。50/50 模式示例见图 4-26。TDM 模式的行为类似。

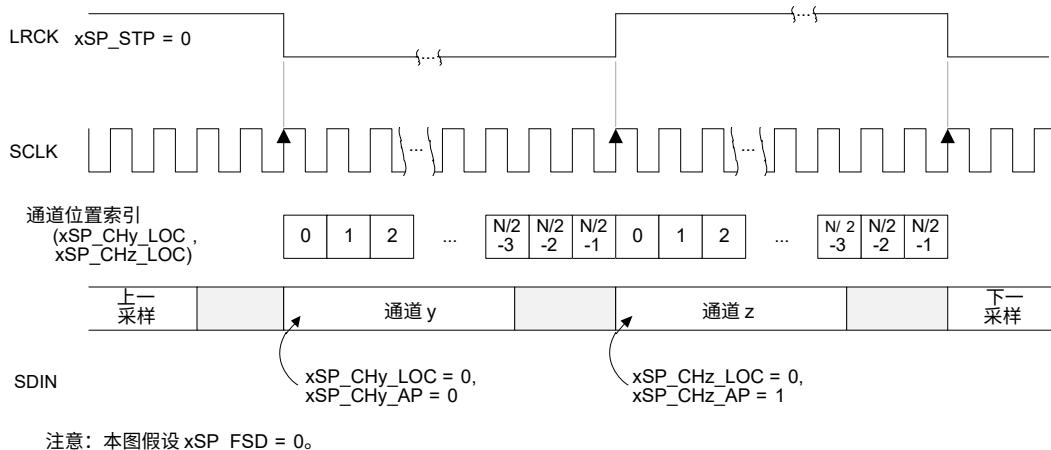


图 4-26。50/50 模式示例 (ASP_STP = 0)

- 当 $xSP_STP = 1$ 时，帧在 LRCK/FSYNC 从低电平跳变至高电平时开始。50/50 模式示例见图 4-27。TDM 模式类似。

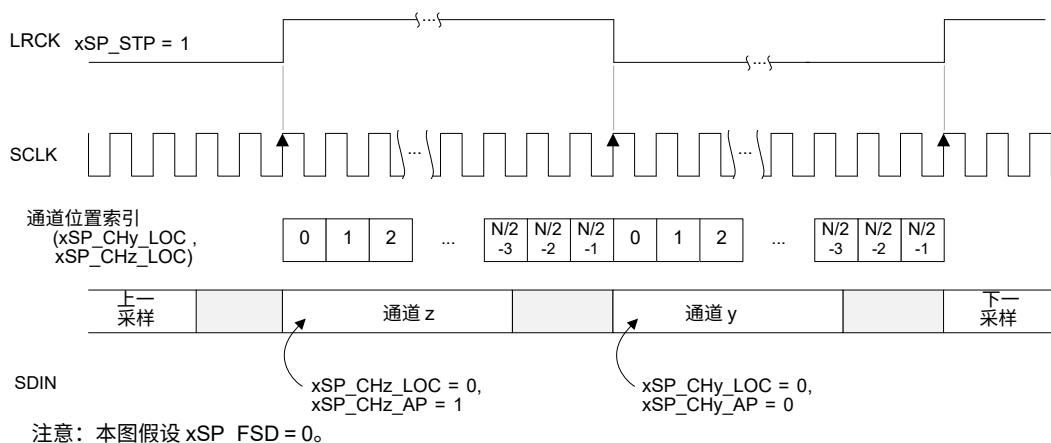


图 4-27。50/50 模式示例 (ASP_STP = 1)

4.9.8 50/50 模式

在典型的双通道 I²S 操作（50/50 模式， $xSP_5050 = 1$ ）中，LRCK 占空比为 50%，每个通道在两个 LRCK 相位中的一个期间传输。在此模式下，每个串行端口通道可独立编程为在 LRCK/FSYNC 为高电平时或低电平时输出；这称为通道激活相。

如果激活相控制位 ($xSP_RX_CHn_AP$) 被设置，则相应通道在 LRCK/FSYNC 为高电平时输出。如果 $xSP_RX_CHn_AP$ 被清除，则相应通道在 LRCK/FSYNC 为低电平时输出。 $xSP_RX_CHn_AP$ 各设置的示例见图 4-26 和图 4-27。

在 50/50 模式下，通道位置（见第 4.9.6 节）在通道激活相内计算。如果一帧中有 N 位，则每个激活相最后一位的位置等于 ($N/2$) - 1。

注意：如果设置了 xSP_5050 ，则 xSP_LCHI 必须编程为 xSP_LCPR 的一半，以实现 50% 的占空比。此外，仅可为对应的串行端口启用两个通道。

4.9.9 Serial Port Status

Each serial port has five status bits. Each bit is sticky and must be read to be cleared. The status bits have associated mask bits to mask setting the INT pin when the status bit sets. A brief description of each status bit is shown in [Table 4-8](#).

Table 4-8. Serial Port Status

Name	Description	Register Reference
Request Overload	Set when too many input buffers request processing at the same time. If all channel size and location registers are properly configured to non-overlapping values, this error status must never set.	ASP_OVFL_INT p. 134 XSP_OVFL_INT p. 135
LRCK Error	Logical OR of LRCK early and LRCK late (see below).	ASP_ERROR_INT p. 135 XSP_ERROR_INT p. 135
LRCK Early	Set when the number of SCLK periods per LRCK phase (high or low) is less than the expected count as determined by xSP_LCPR and xSP_LCHI. Note: The Rx LRCK early interrupt status is set during the first receive LRCK early event. Subsequent receive LRCK early events are not indicated until after valid LRCK transitions are detected.	ASP_EARLY_INT p. 135 XSP_EARLY_INT p. 135
LRCK Late	Set when the number of SCLK periods per LRCK phase (high or low) is greater than the expected count as determined by xSP_LCPR and xSP_LCHI.	ASP_LATE_INT p. 135 XSP_LATE_INT p. 135
No LRCK	Set when the number of SCLK periods counted exceeds twice the value of LRCK period (xSP_LCPR) without an LRCK edge. The Tx No LRCK interrupt status is set during the first instance of a no transmit LRCK condition. Subsequent no transmit LRCK conditions are not indicated until after valid LRCK transitions are detected.	ASP_NOLRCK_INT p. 135 XSP_NOLRCK_INT p. 135

4.9.10 Serial Port Clock Pin Status

There are various control bits available that affect the output state of the serial port clock and data pins. [Table 4-9](#) summarizes the possible states depending on these bit settings.

Table 4-9. xSP_SCLK and xSP_LRCK/FSYNC Pin States

xSP_3ST	xSP_M/S	PDN_xSP	xSP_SCLK Pin State	xSP_LRCK/FSYNC Pin State
1	x	x	Hi-Z with weak pull-down	Hi-Z with weak pull-down
0	0	x	Hi-Z with weak pull-down	Hi-Z with weak pull-down
0	1	0	Active	Active
0	1	1	Inactive	Inactive ¹

1. If xSP_LCPOL_OUT is set, xSP_LRCK/FSYNC inactive output is high. If xSP_LCPOL_OUT is cleared, xSP_LRCK/FSYNC inactive output is low.

4.9.11 DoP (DSD over PCM) Mode

DoP is a protocol for packetizing DSD data into a PCM frame for transmission over an existing I2S interface. The ASP or XSP can accept DSD data in DoP format.

To use the DoP interface in Slave Mode, if MCLK_INT = 22.5792 MHz, the DoP interface clocks are required to be synchronous to MCLK_INT.

4.9.9 串行端口状态

每个串行端口包含五个状态位。每个位均为粘滞位，必须读取后才能清除。状态位配有关于在状态位置位时屏蔽INT引脚的触发。各状态位的简要说明见表4-8。

表4-8 串行端口状态

名称	描述	寄存器参考
请求溢出	当过多输入缓冲区同时请求处理时设置。如果所有通道大小和位置寄存器均正确配置为不重叠的值，则此错误状态绝不应被设置。	ASP_OVFL_INT 第134页 XSP_OVFL_INT 第135页
LRCK 错误	LRCK 过早和 LRCK 过迟的逻辑或（见下文）。	ASP_ERROR_INT 第135页 XSP_ERROR_INT 第135页
LRCK 过早	当每个 LRCK 相位（高或低）的 SCLK 周期数少于由 xSP_LCPRI 和 xSP_LCHI 确定的预期计数时设置。 注意：接收端 LRCK 过早中断状态在首次接收 LRCK 过早事件时设置。在检测到有效的 LRCK 变换之前，不会指示后续的接收 LRCK 过早事件。	ASP_EARLY_INT 第135页 XSP_EARLY_INT 第135页
LRCK 延迟	当每个 LRCK 相位（高电平或低电平）内的 SCLK 周期数超过由 xSP_LCPRI 和 xSP_LCHI 设定的预期计数时设置。	ASP_LATE_INT 第135页 XSP_LATE_INT 第135页
无 LRCK	当计数的 SCLK 周期数超过 LRCK 周期 (xSP_LCPRI) 两倍且无 LRCK 边沿时设置。 首次出现无传输 LRCK 状态时，设置 Tx 无 LRCK 中断状态。在检测到有效 LRCK 跳变之前，不会指示后续的无传输 LRCK 状态。	ASP_NOLRCK_INT 第135页 XSP_NOLRCK_INT 第135页

4.9.10 串行端口时钟引脚状态

多种控制位可影响串行端口时钟和数据信号引脚的输出状态。表4-9总结了基于这些位设置的可能状态。

表 4-9。 xSP_SCLK 和 xSP_LRCK/FSYNC 引脚状态

xSP_3ST	xSP_M/S	PDN_xSP	xSP_SCLK 引脚状态	xSP_LRCK/FSYNC 引脚状态
1	x	x	高阻态，带弱下拉	高阻态，带弱下拉
0	0	x	高阻态，带弱下拉	高阻态，带弱下拉
0	1	0	激活	激活
0	1	1	未激活	未激活 ¹

1. 如果设置了 xSP_LCPOL_OUT，xSP_LRCK/FSYNC 非活动输出为高电平。如果清除了 xSP_LCPOL_OUT，xSP_LRCK/FSYNC 非活动输出为低电平。

4.9.11 DoP (DSD over PCM) 模式

DoP是一种将DSD数据封装进PCM帧以通过现有I2S接口传输的协议。ASP或XSP支持接收DoP格式的DSD数据。

在从模式下使用DoP接口时，若MCLK_INT为22.5792 MHz，则DoP接口时钟必须与MCLK_INT同步。

Each sample is 24 bits, as shown in [Fig. 4-28](#), where the 8 most significant bits are used for the DSD marker and alternate with each sample between 0x05/0xFA. Each channel within a sample contains the same marker. The remaining 16 lower bits are then used for the DSD data, with the first or oldest bit in Slot t₀.

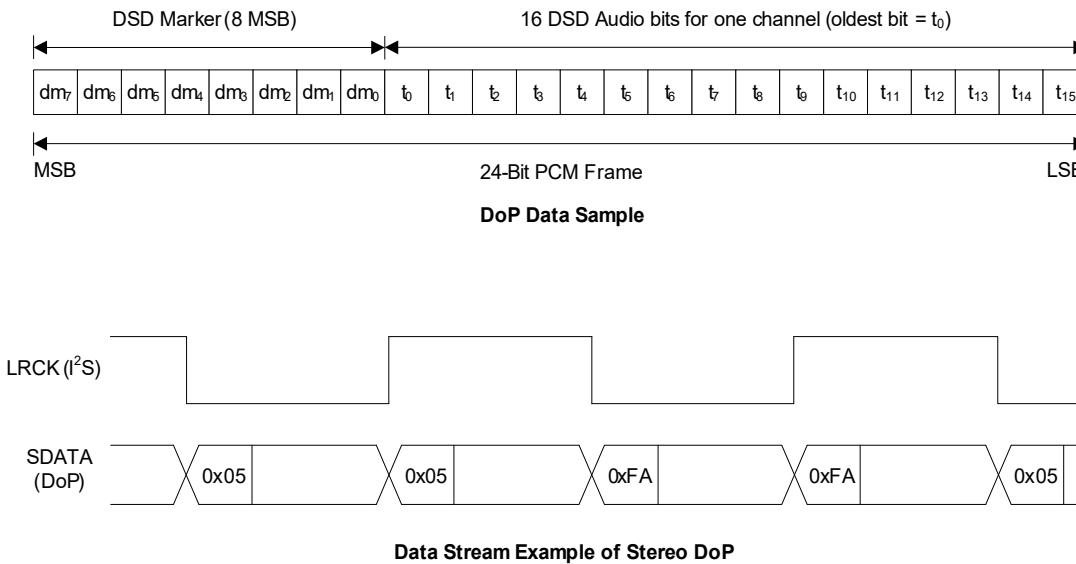


Figure 4-28. DoP Data Sample and Stereo Stream Example

Each PCM frame is assigned to a specific channel (left or right), and when used for DSD streaming, each PCM frame contains only DSD data corresponding to its assigned channel. The CS43131 unpacks the received DoP data and reforms it into a DSD stream to feed the internal DSD data paths.

It includes the following features:

- 24 bits per PCM data sample
- I²S format is supported
- DoP data is unpacketed internally for DSD playback
- Clock Master and Slave Mode
- Up to 128•Fs DSD stream
 - Accepts a 64•Fs DSD stream with LRCK@176.4 kHz
 - Accepts a 128•Fs DSD stream with LRCK@352.8 kHz

To enable DoP interface on the ASP to take in DSD source:

1. Configure the ASP per clocking/format required by DoP content.
2. Configure DSD_SPEED per DoP content.
3. Set DSD_PRC_SRC = 10 and DSD_EN = 1.

4.10 DSD Interface

The DSD interface is enabled or disabled by PDN_DSDIF bit. When cleared, the DSD data interface is enabled. When using this interface, the DSD interface clock can be mastered by the CS43131 (DSD_M/SB=1). If set to Master Mode, DSDCLK toggles if both PDN_DSDIF and XSP_3ST bits are cleared, and DSD_EN is set.

If the DSD interface clock is slaved (DSD_M/SB=0), when MCLK_INT is set as 22.5792 MHz, DSDCLK is required to be synchronous to MCLK_INT. The DSDCLK can be derived by either:

- Exporting 1/2, 1/4, or 1/8 the frequency of the CS43131 crystal to CLKOUT, or
- Sourcing MCLK_INT and DSDCLK from the same external clock source

每个采样为 24 位，如图 4-28 所示，其中最高的 8 位用于 DSD 标记，并在每个采样间交替为 0x05/0xFA。每个采样内的各通道包含相同的标记。剩余的 16 个低位用于 DSD 数据，第一位或最旧的位位于时隙 t0。

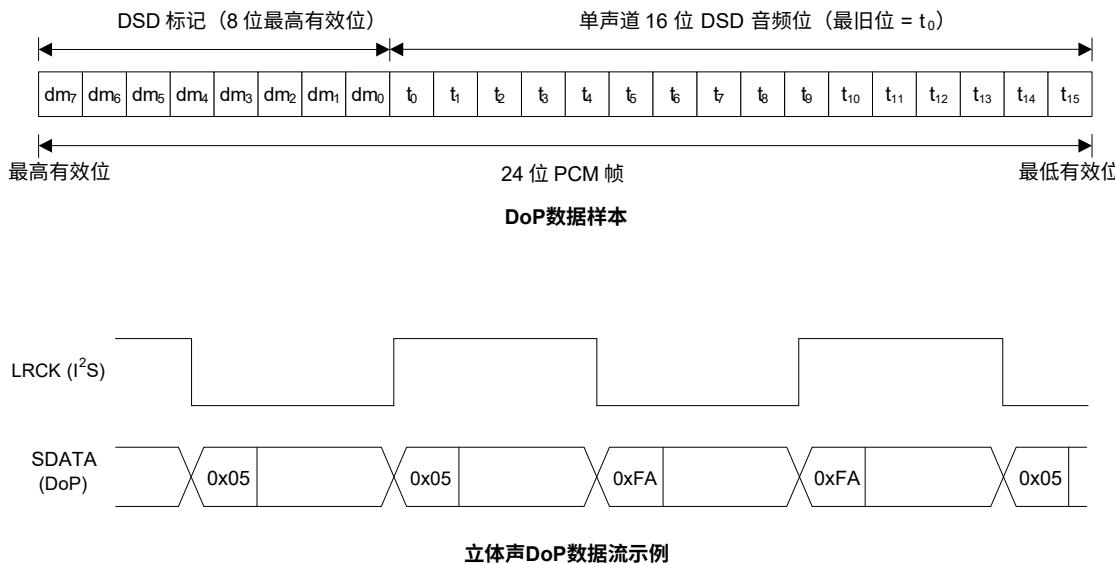


图 4-28。DoP 数据采样及立体声流示例

每个 PCM 帧分配给特定通道（左或右），用于 DSD 流时，每个 PCM 帧仅包含其分配通道对应的 DSD 数据。CS43131 解包接收的 DoP 数据，并将其重组为 DSD 流以供内部 DSD 数据路径使用。

其包含以下特性：

- 每个PCM数据采样24位
- 支持I²S格式
- 内部对DoP数据进行解包以实现DSD播放
- 时钟主从模式
- 支持最高128•Fs的DSD流
 - 支持LRCK@176.4 kHz时的64•Fs DSD流
 - 支持LRCK@352.8 kHz时的128•Fs DSD流

要启用ASP上的DoP接口以接收DSD源：

1. 根据DoP内容配置ASP的时钟和格式。
2. 根据DoP内容配置DSD_SPEED。
3. 设置DSD_PRC_SRC = 10且DSD_EN = 1。

4.10 DSD接口

通过PDN_DSDIF位启用或禁用DSD接口。清零时，DSD数据接口启用。使用该接口时，DSD接口时钟可由CS43131主控 (DSD_M/SB=1)。若设置为主模式，当PDN_DSDIF和XSP_3ST位均清零且DSD_EN置位时，DSDCLK将切换。

如果 DSD 接口时钟为从属模式 (DSD_M/SB=0)，当 MCLK_INT 设置为 22.5792 MHz 时，DSDCLK 需与 MCLK_INT 同步。DSDCLK 可通过以下方式获得：

- 将 CS43131 晶体频率的 1/2、1/4 或 1/8 输出至 CLKOUT，或
- 从同一外部时钟源提供 MCLK_INT 和 DSDCLK

The DSD_EN bit, when set, is used to configure the device for processing DSD sources. DSD_PRC_SRC configures the DSD interface used for feeding into the DSD processor. DSD_SPEED specifies if a 64•Fs, 128•Fs, or 256•Fs DSD stream is provided. If PDN_DSDIF = 0 and DSD_M/SB = 1, DSD_SPEED determines the DSDCLK clock frequency generated. When configuring the DSD interface, follow these steps:

1. Configure the DSD_M/SB, DSD_SPEED, DSD_PRC_SRC, and XSP_3ST.
2. Release PDN_DSDIF.
3. Enable DSD_EN.

The DSD_PM_EN bit selects phase modulation (data plus data inverted) as the style of data input. In this mode, the DSD_PM_SEL bit selects whether a 2x or 1x data rate clock is used for phase-modulated data (see Fig. 4-29). Use of phase modulation mode may not directly affect the performance of the CS43131, but may lower the sensitivity of other board-level components to the DSD data signals. Note that phase modulation mode is supported only for DSD 64•Fs and DSD 128•Fs data rates. If the 2x data rate mode is used, DSD_INV_B and DSD_INV_A need to be set before the mode is enabled. After the 2x data rate mode is disabled, DSD_INV_B and DSD_INV_A need to be cleared appropriately.

The CS43131 can detect overmodulation errors in the DSD data that do not comply to the SACD specification. Setting INV_DSD_DET enables detection of overmodulation errors. This condition is reported through the DSD_INVAL_A_INT and DSD_INVAL_B_INT status bits. Overmodulated DSD data is converted as received without intervention, but performance at these levels cannot be guaranteed. Setting STA_DSD_DET allows the CS43131 to mute a DSD stream that is stuck at 1 or 0. This condition is reported through the DSD_STUCK_INT status bit. See [Section 7.6.5](#) for descriptions of the DSD error reporting bits.

More information for these register bits can be found in [Section 7](#).

The DSD input structure and analog outputs are designed to handle a nominal 0 dB-SACD (50% modulation index) at full-rated performance. When 0 dB-SACD and 0 dBFS PCM need to be level matched, DSD_ZERODB must be set. In this mode, signals of +3-dB SACD may be applied for brief periods of time; however, performance at these levels is not guaranteed. If sustained levels approaching +3-dB SACD levels are required, DSD_ZERODB must be cleared, which matches a +3-dB SACD output level.

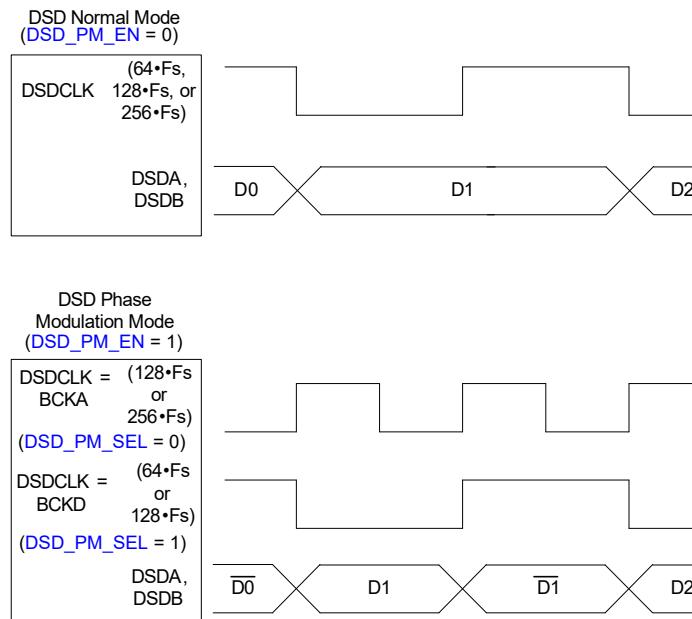


Figure 4-29. DSD Phase Modulation Mode Diagram

设置DSD_EN位时，用于配置设备以处理DSD信号源。DSD_PRC_SRC配置用于输入至DSD处理器的DSD接口。DSD_SPEED指定提供64•Fs、128•Fs或256•Fs的DSD流。当PDN_DSDIF = 0且DSD_M/SB = 1时，DSD_SPEED决定生成的DSDCLK时钟频率。

配置DSD接口时，请按照以下步骤操作：

1. 配置DSD_M/SB、DSD_SPEED、DSD_PRC_SRC和XSP_3ST。
2. 释放PDN_DSDIF。
3. 使能DSD_EN。

DSD_PM_EN位选择相位调制（数据加数据反相）作为数据输入方式。在此模式下，DSD_PM_SEL位选择用于相位调制数据的时钟为2x或1x数据速率（参见图4-29）。使用相位调制模式可能不会直接影响CS43131的性能，但可能降低其他板级组件对DSD数据信号的敏感度。请注意，相位调制模式仅支持DSD 64•采样频率和DSD 128•采样频率数据速率。如果使用2x数据速率模式，则需在启用该模式之前设置DSD_INV_B和DSD_INV_A。在禁用2x数据速率模式后，需适当清除DSD_INV_B和DSD_INV_A。

CS43131能检测不符合SACD规范的DSD数据中的过调制错误。设置INV_DSD_DET可启用过调制错误检测。该状态通过DSD_INVAL_A_INT和DSD_INVAL_B_INT状态位报告。过调制的DSD数据将按接收状态直接转换，但在此类水平下的性能无法保证。设置STA_DSD_DET允许CS43131对卡在1或0的DSD流进行静音处理。该状态通过DSD_STUCK_INT状态位报告。有关DSD错误报告位的描述，请参见第7.6.5节。

有关这些寄存器位的更多信息，请参见第7节。

DSD输入结构和模拟输出设计用于处理标称0 dB-SACD（50%调制指数）下的全额定性能。当需要将0 dB-SACD与0 dBFS PCM进行电平匹配时，必须设置DSD_ZERODB。在此模式下，+3 dB SACD信号可在短时间内施加；但在此类水平下的性能无法保证。如果需要持续接近+3 dB SACD水平的信号，必须清除DSD_ZERODB，以匹配+3 dB SACD输出电平。

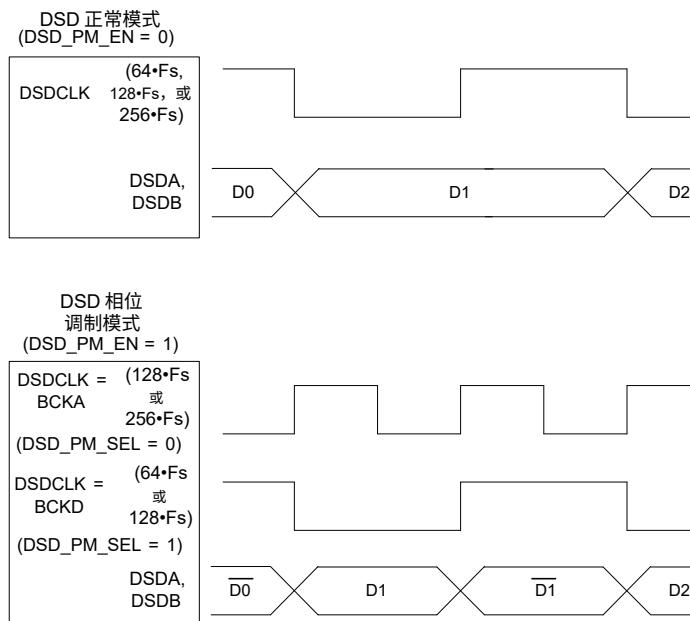


图4-29。DSD相位调制模式图

4.11 DSD and PCM Mixing

For mobile application, the CS43131 provides a feature for mixing in PCM notification during DSD playback, with the setup in [Table 4-10](#).

Table 4-10. Mixing Configurations Supported by the CS43131

PCM Input Configuration			DSD Input Configuration		
I ² S or TDM on ASP	44.1 kHz	Master	DSD on DSD IF	2.8224, 5.6448, or 11.2896 MHz on DSDCLK	Master
		Slave 1			Slave 1
	DoP on XSP	Master	176.4 or 352.8 kHz	Master	
		Slave 1			Slave 1

1.The ASP/XSP subclocks and DSDCLK are required to be synchronous.

It is assumed that the DSD path has been properly configured for DSD playback.

During normal DSD playback, the ASP can be shut down. At the PCM notification event, the ASP must be properly configured to receive PCM samples at 44.1 kHz. After the ASP subclocks are running, set MIX_PCM_PREP to indicate to the CS43131 that the PCM mixing event is imminent. After 1.6 ms, MIX_PCM_DSD can be safely set to initiate the mixing process. After the PCM notification mixing is complete, clear both MIX_PCM_DSD and MIX_PCM_PREP at the same time. If desired, the ASP can be shut down to save power.

When mixing, use both PCM and DSD volume controls to attenuate the signal content on both paths (e.g., at least -6-dB attenuation on each) to avoid clipping on the mixing product. Use PCM_VOLUMEx to adjust the PCM path and DSD_VOLUMEx to adjust the DSD path. All the signal path settings apply to both path's individual settings.

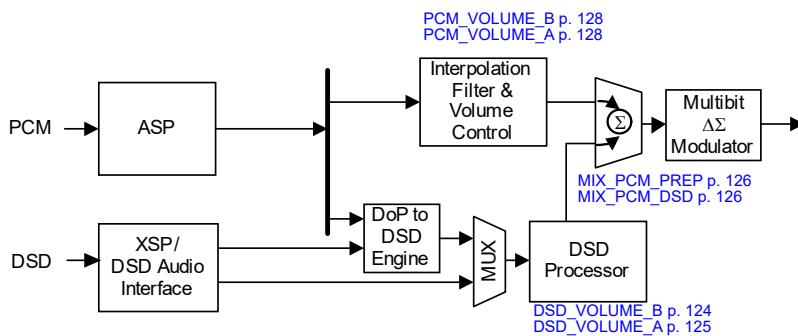


Figure 4-30. PCM and DSD Mixing Signal Flow

4.12 Standard Interrupts

The interrupt output pin, INT, is used to signal the occurrence of events within the device's interrupt status registers. Events can be masked individually by setting corresponding bits in the interrupt mask registers. [Table 4-11](#) lists interrupt status and mask registers. The configuration of mask bits determines which events cause the immediate assertion of INT:

- When an unmasked interrupt status event is detected, the status bit is set, and INT is asserted.
- When a masked interrupt status event is detected, the interrupt status bit is set, but INT is not affected.

Once INT is asserted, it remains asserted until all status bits that are unmasked and set have been read. Interrupt status bits are sticky and read-to-clear. Once set, they remain set until the register is read and the associated interrupt condition is not present. If a condition is still present and the status bit is read, although INT is deasserted, the status bit remains set.

To clear status bits set due to the initiation of a block, all interrupt status bits must be read after the corresponding module is enabled and before normal operation begins. Otherwise, unmasking these previously set status bits causes assertion of INT.

Interrupt source bits are set when edge-detect interrupts are detected, and they remain set until the register is read and the condition that caused the bit to assert is no longer present.

4.11 DSD与PCM混合

针对移动应用，CS43131 提供了在 DSD 播放期间混合 PCM 通知的功能，设置见表 4-10。

表 4-10。CS43131 支持的混合配置

PCM 输入配置			DSD 输入配置		
I ² S 或 TDM 在 ASP 上	44.1 kHz	主设备	DSD 在 DSD IF 上	2.8224、5.6448 或 11.2896 MHz 在 DSDCLK 上	主设备
		从设备 1			从设备 1
		主设备	DoP 在 XSP 上	176.4 或 352.8 kHz	主设备
		从设备 1			从设备 1

1. ASP/XSP 子时钟和 DSDCLK 需同步。

假设 DSD 路径已正确配置以支持 DSD 播放。

在正常 DSD 播放期间，ASP 可关闭。在 PCM 通知事件时，ASP 必须正确配置以接收 44.1 kHz 的 PCM 采样。ASP 子时钟启动后，设置 MIX_PCM_PREP 以通知 CS43131 即将发生 PCM 混音事件。在 1.6 毫秒后，可以安全设置 MIX_PCM_DSD 以启动混音过程。PCM 通知混音完成后，应同时清除 MIX_PCM_DSD 和 MIX_PCM_PREP。如有需要，可关闭 ASP 以节省功耗。

混音时，应使用 PCM 和 DSD 音量控制对两个路径的信号进行衰减（例如，每个路径至少衰减 -6 dB），以避免混音产物出现削波。使用 PCM_VOLUME_x 调节 PCM 路径，使用 DSD_VOLUME_x 调节 DSD 路径。所有信号路径设置均适用于两个路径的各自设置。

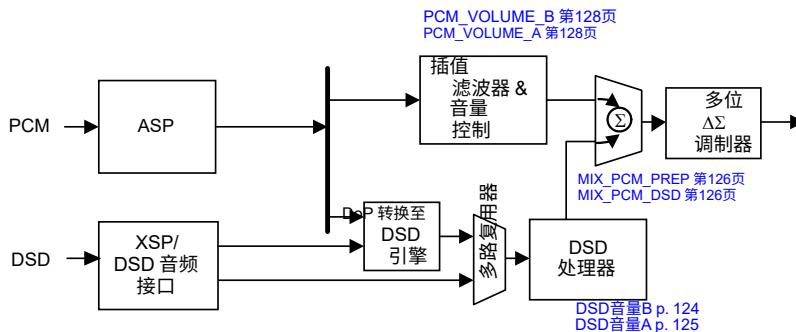


图 4-30。PCM 与 DSD 混音信号流程

4.12 标准中断

中断输出引脚 INT 用于指示设备中断状态寄存器中事件的发生。通过设置中断屏蔽寄存器中的相应位，可以单独屏蔽各事件。表 4-11 列出了中断状态和屏蔽寄存器。掩码位的配置决定了哪些事件会导致 INT 的立即断言：

- 当检测到未屏蔽的中断状态事件时，状态位被置位，且 INT 被断言。
- 当检测到屏蔽的中断状态事件时，中断状态位被置位，但 INT 不受影响。

一旦 INT 被断言，直到所有未屏蔽且已置位的状态位被读取后，INT 才会取消断言。中断状态位为粘滞位，读取后清除。一旦置位，状态位将保持置位，直到寄存器被读取且相关中断条件不再存在。如果条件仍然存在且状态位被读取，尽管 INT 被取消断言，状态位仍保持置位。

为清除因块启动而置位的状态位，必须在相应模块启用后且正常操作开始前读取所有中断状态位。否则，取消屏蔽这些先前置位的状态位将导致 INT 断言。

当检测到边缘触发中断时，中断源位被置位，且保持置位，直到寄存器被读取且导致该位断言的条件不再存在。

Fig. 4-31 shows sticky-bit behavior.

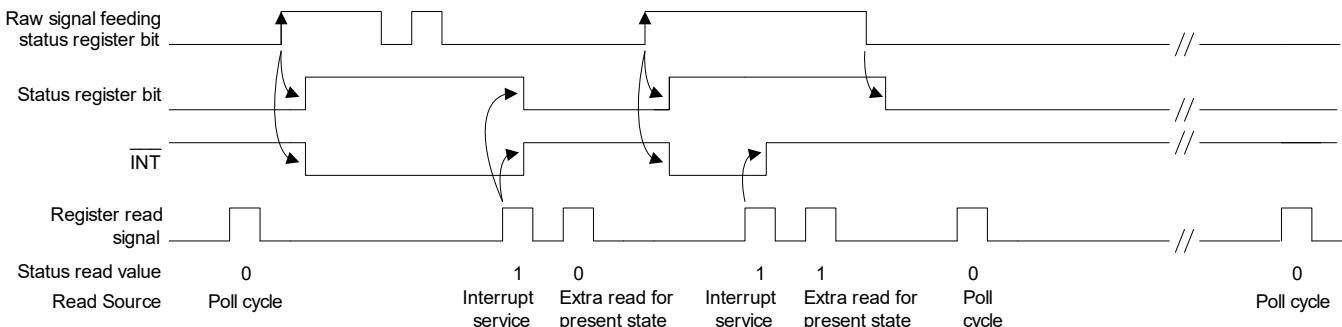


Figure 4-31. Example of Rising-Edge-Sensitive, Sticky, Interrupt-Status-Bit Behavior

Table 4-11. Interrupt Events and Register Bit Fields

Interrupt	Register Bit Field	Interrupt Mask Field
DAC overflow	DAC_OVFL_INT	DAC_OVFL_INT_MASK
HP unplug detect	HPDETECT_UNPLUG_INT	HPDETECT_UNPLUG_INT_MASK
HP plug detect	HPDETECT_PLUG_INT	HPDETECT_PLUG_INT_MASK
XTAL is ready	XTAL_READY_INT	XTAL_READY_INT_MASK
XTAL error detected	XTAL_ERROR_INT	XTAL_ERROR_INT_MASK
ASP overload	ASP_OVLD_INT	ASP_OVLD_INT_MASK
ASP error	ASP_ERR_INT	ASP_ERR_INT_MASK
ASP late	ASP_LATE_INT	ASP_LATE_INT_MASK
ASP early	ASP_EARLY_INT	ASP_EARLY_INT_MASK
ASP no LRCK	ASP_NOLRCK_INT	ASP_NOLRCK_INT_MASK
XSP overload	XSP_OVLD_INT	XSP_OVLD_INT_MASK
XSP error	XSP_ERR_INT	XSP_ERR_INT_MASK
XSP late	XSP_LATE_INT	XSP_LATE_INT_MASK
XSP early	XSP_EARLY_INT	XSP_EARLY_INT_MASK
XSP no LRCK	XSP_NOLRCK_INT	XSP_NOLRCK_INT_MASK
PLL is ready	PLL_READY_INT	PLL_READY_INT_MASK
PLL error detected	PLL_ERROR_INT	PLL_ERROR_INT_MASK
Power down done	PDN_DONE_INT	PDN_DONE_INT_MASK
HP load error: DC measurement is not performed before AC measurement is initiated	HLOAD_NO_DC_INT	HLOAD_NO_DC_INT_MASK
HP load error: HP is unplugged during the measurement process	HLOAD_UNPLUG_INT	HLOAD_UNPLUG_INT_MASK
HP load error: PDN_HP is not properly set before HP load measurement is started	HLOAD_HPON_INT	HLOAD_HPON_INT_MASK
HP load error: out of range result is measured	HLOAD_OOR_INT	HLOAD_OOR_INT_MASK
HP load AC detection done	HLOAD_AC_DONE_INT	HLOAD_AC_DONE_INT_MASK
HP load DC detection done	HLOAD_DC_DONE_INT	HLOAD_DC_DONE_INT_MASK
HP load state machine turned off properly	HLOAD_OFF_INT	HLOAD_OFF_INT_MASK
HP load state machine turned on properly	HLOAD_ON_INT	HLOAD_ON_INT_MASK
DSD stuck Error	DSD_STUCK_INT	DSD_STUCK_INT_MASK
DSD channel A invalid error	DSD_INVAL_A_INT	DSD_INVAL_A_INT_MASK
DSD channel B invalid error	DSD_INVAL_B_INT	DSD_INVAL_B_INT_MASK
DSD channel A silence pattern detected	DSD_SILENCE_A_INT	DSD_SILENCE_A_INT_MASK
DSD channel B silence pattern detected	DSD_SILENCE_B_INT	DSD_SILENCE_B_INT_MASK
DSD rate error detected	DSD_RATE_INT	DSD_RATE_INT_MASK
DoP marker detected	DOP_MRK_DET_INT	DOP_MRK_DET_INT_MASK
DoP engine on	DOP_ON_INT	DOP_ON_INT_MASK

图 4-31 显示了粘滞位行为。

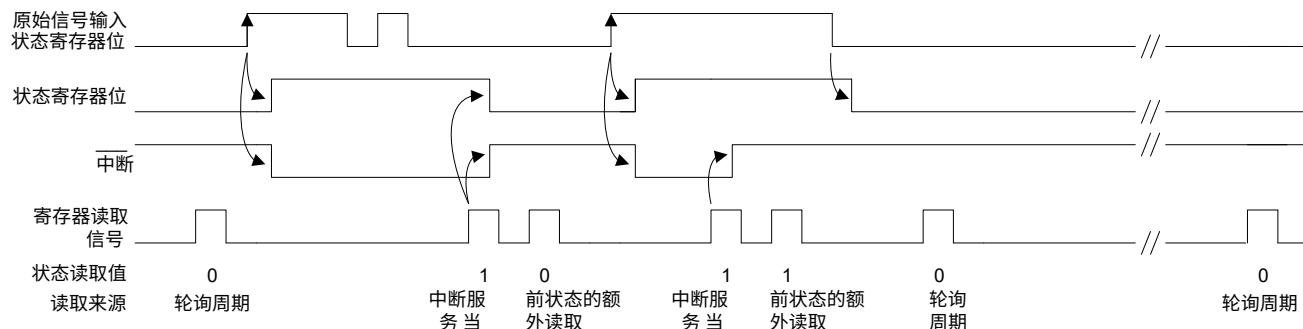


图 4-31。上升沿敏感、粘滞型中断状态位行为示例

表 4-11 中断事件与寄存器位字段

中断	寄存器位字段	中断屏蔽字段
DAC 溢出	DAC_OVFL_INT	DAC_OVFL_INT_MASK
耳机拔出检测	HPDETECT_UNPLUG_INT	HPDETECT_UNPLUG_INT_MASK
耳机插入检测	HPDETECT_PLUG_INT	HPDETECT_PLUG_INT_MASK
晶体振荡器准备就绪	XTAL_READY_INT	XTAL_READY_INT_MASK
检测到晶体振荡器错误	XTAL_ERROR_INT	XTAL_ERROR_INT_MASK
ASP 过载	ASP_OVLD_INT	ASP_OVLD_INT_MASK
ASP 错误	ASP_ERR_INT	ASP_ERR_INT_MASK
ASP 延迟	ASP_LATE_INT	ASP_LATE_INT_MASK
ASP 提前	ASP_EARLY_INT	ASP_EARLY_INT_MASK
ASP 无 LRCK	ASP_NOLRCK_INT	ASP_NOLRCK_INT_MASK
XSP 过载	XSP_OVLD_INT	XSP_OVLD_INT_MASK
XSP 错误	XSP_ERR_INT	XSP_ERR_INT_MASK
XSP 延迟	XSP_LATE_INT	XSP_LATE_INT_MASK
XSP 提前	XSP_EARLY_INT	XSP_EARLY_INT_MASK
XSP 无 LRCK	XSP_NOLRCK_INT	XSP_NOLRCK_INT_MASK
PLL 已就绪	PLL_READY_INT	PLL_READY_INT_MASK
检测到 PLL 错误	PLL_ERROR_INT	PLL_ERROR_INT_MASK
电源关闭完成	PDN_DONE_INT	PDN_DONE_INT_MASK
耳机负载错误：在启动交流测量前未进行直流测量	HLOAD_NO_DC_INT	HLOAD_NO_DC_INT_MASK
耳机负载错误：测量过程中耳机被拔出	HLOAD_UNPLUG_INT	HLOAD_UNPLUG_INT_MASK
耳机负载错误：启动耳机负载测量前 PDN_HP 未正确设置	HLOAD_HPON_INT	HLOAD_HPON_INT_MASK
耳机负载错误：测量结果超出范围	HLOAD_OOR_INT	HLOAD_OOR_INT_MASK
耳机负载交流检测完成	HLOAD_AC_DONE_INT	HLOAD_AC_DONE_INT_MASK
耳机负载直流检测完成	HLOAD_DC_DONE_INT	HLOAD_DC_DONE_INT_MASK
耳机负载状态机已正确关闭	HLOAD_OFF_INT	HLOAD_OFF_INT_MASK
耳机负载状态机已正确开启	HLOAD_ON_INT	HLOAD_ON_INT_MASK
DSD 卡死错误	DSD_STUCK_INT	DSD_STUCK_INT_MASK
DSD 通道 A 无效错误	DSD_INVAL_A_INT	DSD_INVAL_A_INT_MASK
DSD 通道 B 无效错误	DSD_INVAL_B_INT	DSD_INVAL_B_INT_MASK
检测到 DSD 通道 A 静音模式	DSD_SILENCE_A_INT	DSD_SILENCE_A_INT_MASK
检测到 DSD 通道 B 静音模式	DSD_SILENCE_B_INT	DSD_SILENCE_B_INT_MASK
检测到 DSD 速率错误	DSD_RATE_INT	DSD_RATE_INT_MASK
检测到 DoP 标记	DOP_MRK_DET_INT	DOP_MRK_DET_INT_MASK
DoP 引擎已开启	DOP_ON_INT	DOP_ON_INT_MASK

4.13 Control Port Operation

The control port is used to access control registers and on-chip memory locations, allowing the device to be configured for desired operational modes and formats. Control port operation may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, control port pins must remain static if no operation is required.

The control port operates using a I²C interface with the CS43131 acting as a slave device. Device communication must not begin until t_{PUD} (refer to [Table 3-22](#)) after power conditions are ready and RESET is released.

4.13.1 I²C Control Port Operation

The I²C control port operates completely asynchronously with the audio sample rates. However, to avoid interference problems, the I²C control-port pins must remain static if no operation is required.

The control-port uses the I²C interface, with the chip acting as a slave device. The I²C control port can operate in the following modes:

- Standard Mode (SM), with a bit rate of up to 100 kbit/s
- Fast Mode (FM), with a bit rate of up to 400 kbit/s
- Fast Mode Plus (FM+), with a bit rate of up to 1 Mbit/s

SDA is a bidirectional data line. Data is clocked into and out of the CS43131 by the SCL clock. [Fig. 4-32](#), [Fig. 4-33](#), and [Fig. 4-34](#) show signal timings for read and write cycles. A Start condition is defined as a falling transition of SDA while SCL is high. A stop condition is defined as a rising transition of SDA while SCL is high. All other transitions of SDA must occur while SCL is low. Note that when HP_IN_LP is set, only SM and FM modes are supported.

To configure the last two bits of I²C address, CS43131 detects the ADR resistor connection type and measures the resistance upon a device power up (POR event) or after a hardware reset event (RESET deasserted). Based on the detected resistance, the I²C address is latched and cannot be changed until the next hardware reset event. The I²C address configuration is not ready until t_{PUD} after the hardware reset event. During this period, the CS43131 does not respond to any user-issued I²C command. After configuration, the IC tristates the ADR pin and becomes high impedance internally to avoid a constant bias current.

To directly connect the ADR pin and ground, the last two bits of the I²C address are configured as the default 00. For the other options, use a resistor (with 5% accuracy) as suggested in the [Table 4-12](#).

Table 4-12. I²C Address Configurations

Connection Type	Resistor Value (Ω)	Last Two Bits of I ² C Address
Pull-up to VL	0	11
Pull-up to VL	4990	10
Pull-down to GND	4990	01
Pull-down to GND	0	00 (Default)

If the operation is a write, the 3 bytes after the chip address are the memory address pointer (MAP) that select the address of the register to be read or written to next. The byte following the MAP is the control byte. Bit[0] of the control byte, INCR, selects whether autoincrementing is to be used (INCR = 1), allowing successive reads or writes of consecutive registers. Bits[2:1] of the control byte indicate the size of the data for the autoincrement to be acted on. [Table 4-13](#) explains the format for the I²C control byte.

Table 4-13. I²C Control-Byte Format

Bit	Name	Description
7:3	—	Reserved Default: 0
2:1	SIZE	Register access width. Specifies the width of the register access. 00 8-bit (1 byte) 01–11 Reserved

4.13 控制端口操作

控制端口用于访问控制寄存器和片上存储器位置，允许设备配置为所需的操作模式和格式。控制端口操作可以完全异步于音频采样率。然而，为避免潜在干扰问题，若无操作需求，控制端口引脚必须保持静止。

控制端口通过I²C接口工作，CS43131作为从设备。设备通信必须在电源条件准备就绪且复位释放后，等待t_{PUD}（参见表3-22）时间后方可开始。

4.13.1 I²C控制端口操作

I²C控制端口操作完全异步于音频采样率。然而，为避免干扰问题，若无操作需求，I²C控制端口引脚必须保持静止状态。

控制端口采用I²C接口，芯片作为从设备。I²C控制端口可在以下模式下工作：

- 标准模式（SM），比特率最高可达100 kbit/s。
- 快速模式（FM），比特率最高可达400 kbit/s。
- 快速模式增强版（FM+），比特率最高可达1 Mbit/s。

SDA为双向数据线。数据通过SCL时钟输入和输出至CS43131。图4-32、图4-33及图4-34展示了读写周期的信号时序。起始条件定义为SCL为高电平时，SDA发生下降沿。停止条件定义为SCL为高电平时，SDA发生上升沿。SDA的所有其他跳变必须在SCL处于低电平时发生。请注意，当HP_IN_LP设置时，仅支持SM和FM模式。

为配置I²C地址的最后两位，CS43131会检测ADR电阻的连接类型，并在设备上电复位（POR事件）或硬件复位事件（复位信号释放）后测量电阻值。基于检测到的电阻值，I²C地址被锁存，直到下一次硬件复位事件之前不可更改。I²C地址配置在硬件复位事件后经过t_{PUD}时间才准备就绪。在此期间，CS43131不响应任何用户发出的I²C命令。配置完成后，IC会将ADR引脚置为三态，内部变为高阻抗，以避免持续偏置电流。

若直接将ADR引脚接地，则I²C地址的最后两位配置为默认的00。对于其他选项，使用表4-12中建议的电阻器（精度为5%）。

表4-12。I²C地址配置

连接类型	电阻值 (Ω)	I ² C地址的最后两位
上拉至VL	0	11
上拉至VL	4990	10
下拉至GND	4990	01
下拉至GND	0	00（默认）

如果操作为写入，则芯片地址后的3个字节为内存地址指针（MAP），用于选择下一步要读写的寄存器地址。紧随MAP之后的字节为控制字节。控制字节的Bit[0]，INCR，选择是否使用自动递增（INCR = 1），允许连续读取或写入连续寄存器。

控制字节的Bits[2:1]指示自动递增操作的数据大小。表4-13说明了I²C控制字节的格式。

表4-13。I²C控制字节格式

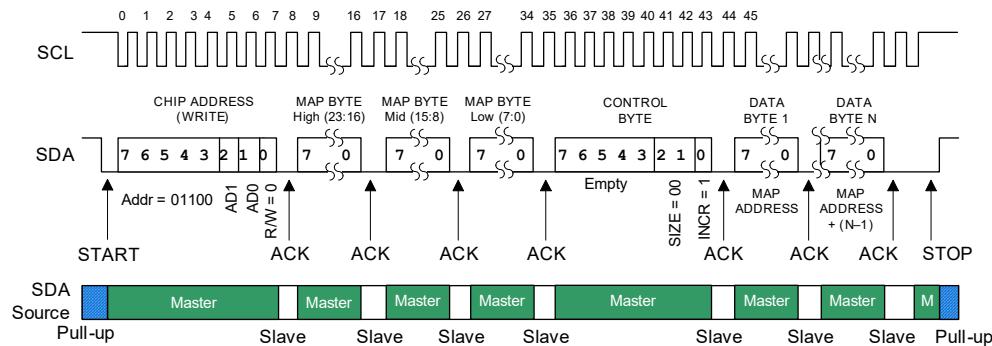
位	名称	描述
7:3	—	保留 默认值：0
2:1	大小	寄存器访问宽度。指定寄存器访问的宽度。 00 8位 (1字节) 01-11 保留

Table 4-13. I²C Control-Byte Format (Cont.)

Bit	Name	Description
0	INCR	Setting this bit allows the MAP address to autoincrement. The MAP address automatically increments every SIZE + 1 bytes accessed consecutively. 0 Disabled 1 Enabled

Each byte transferred on the I²C bus is separated by an acknowledge (ACK) bit. The CS43131 acknowledges each input byte read from the host, and the host must acknowledge each byte transmitted from the CS43131.

For write operations, the data bytes following the MAP byte are written to the CS43131 register addresses pointed to by the last received MAP address, plus however many autoincrements have occurred. Fig. 4-32 shows a write pattern with autoincrementing.


Figure 4-32. Control Port Timing, I²C Writes with Autoincrement (8-bit Data Access)

For read operations, the contents of the register pointed to by the last received MAP address (plus however many autoincrements have occurred if INCR was previously set) are output in the next byte. Fig. 4-33 shows a read pattern following the write pattern in Fig. 4-32. Notice how read addresses are based on the MAP bytes from Fig. 4-32.

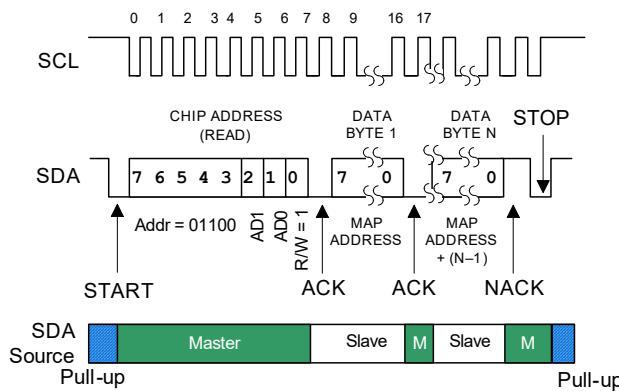
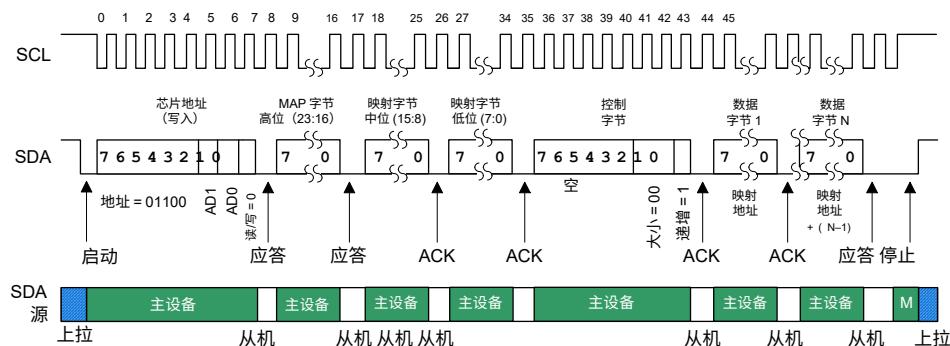

Figure 4-33. Control Port Timing, I²C Reads with Autoincrement (8-Bit Data Access)

表 4-13。I²C 控制字节格式 (续)

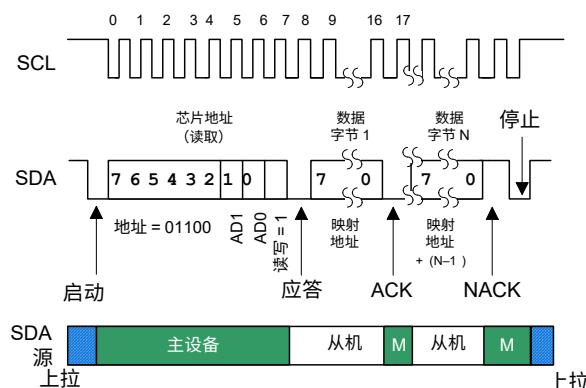
位	名称	描述
0	INCR	设置此位允许 MAP 地址自动递增。MAP 地址在连续访问 SIZE + 1 字节时自动递增。 0 禁用 1 启用

I²C 总线上传输的每个字节之间由应答 (ACK) 位分隔。CS43131 对从主机读取的每个输入字节进行应答，主机必须对从 CS43131 传输的每个字节进行应答。

对于写操作，紧随 MAP 字节之后的数据字节写入由最后接收的 MAP 地址指向的 CS43131 寄存器地址，加上发生的自动递增次数。图 4-32 显示了带自动递增的写入模式。


图 4-32。控制端口时序，带自动递增的 I²C 写操作 (8 位数据访问)

对于读操作，下一字节输出由最后接收的 MAP 地址指向的寄存器内容（如果之前设置了 INCR，则加上发生的自动递增次数）。图 4-33 显示了紧随图 4-32 写入模式之后的读取模式。请注意读取地址基于图 4-32 中的 MAP 字节。


图 4-33。控制端口时序，I²C 读取带自动递增 (8 位数据访问)

To generate a read address not based on the last received MAP address, an aborted write operation can be used as a preamble (see Fig. 4-34). Here, a write operation is aborted (after the ACK for the control byte) by sending a Stop condition.

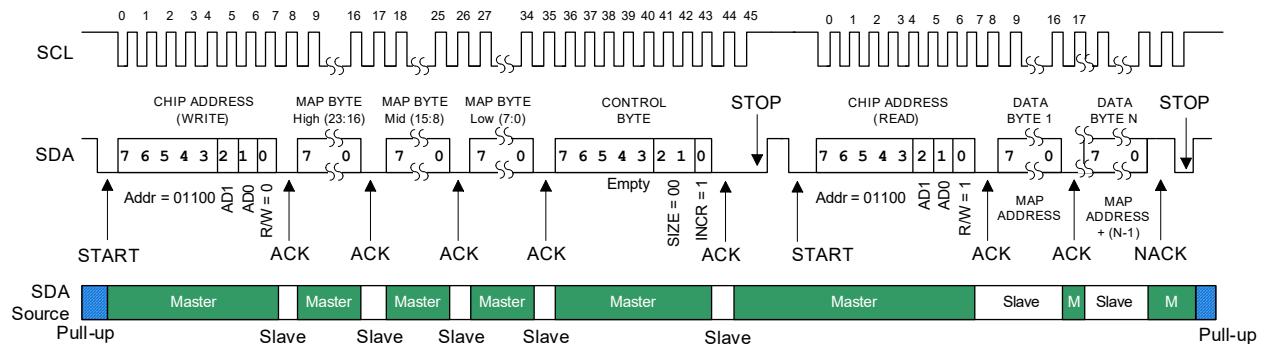


Figure 4-34. Control Port Timing, I²C Reads with Preamble and Autoincrement (8-Bit Data Access)

为了生成非基于最后接收映射地址的读取地址，可以使用中止写操作作为前导（参见图4-34）。此处通过发送停止条件，在控制字节ACK之后中止写操作。

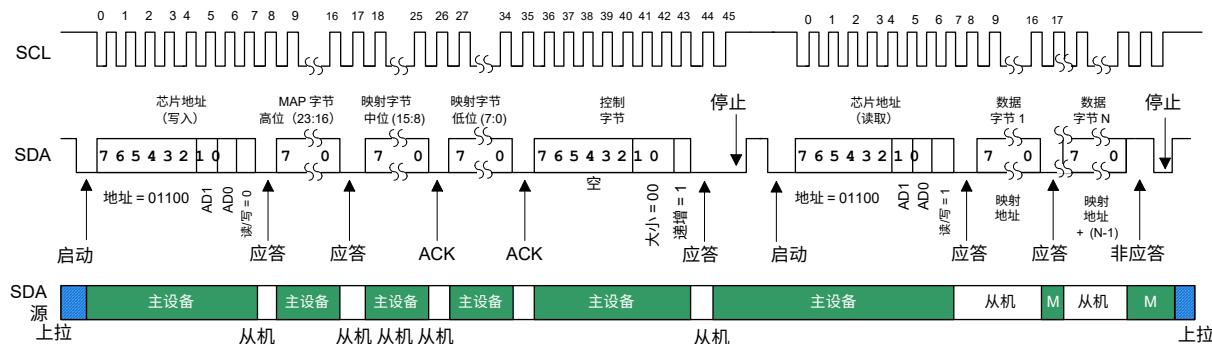


图4-34。控制端口时序，带前导和自动递增的I2C读取（8位数据访问）

4.14 Programmable Filter

In the CS43131, there are a series of programmable filters which is open for user's customization. The filter coefficients can be programmed for altering frequency response or other characteristics to fit the design intention. The filter runs at the input sample rate as set by xSP. This feature is intended to be used for normal PCM playback under single-, double-, and quad-speed settings. (If operating at 192 kHz, MCLK_INT is required to be at 24.576 MHz.) For WBF mode and impedance measurement mode, the filter should be properly turned off.

The filter series are composed of 1 first-order IIR system (FOS) and 3 second-order IIR system (SOS), which effectively is a seventh-order system. FOS and SOS structures are illustrated as in Fig. 4-35 and Fig. 4-36, respectively. Any filter stage can be chosen to be either utilized or bypassed through coefficient settings. Each stage is represented by filter coefficients, which is accessed through I²C writes. The filter coefficients are located in register address 0x09 000C to 0x09 0041. Each coefficient is comprised of a most-significant byte, a least-significant byte, and a sign byte.

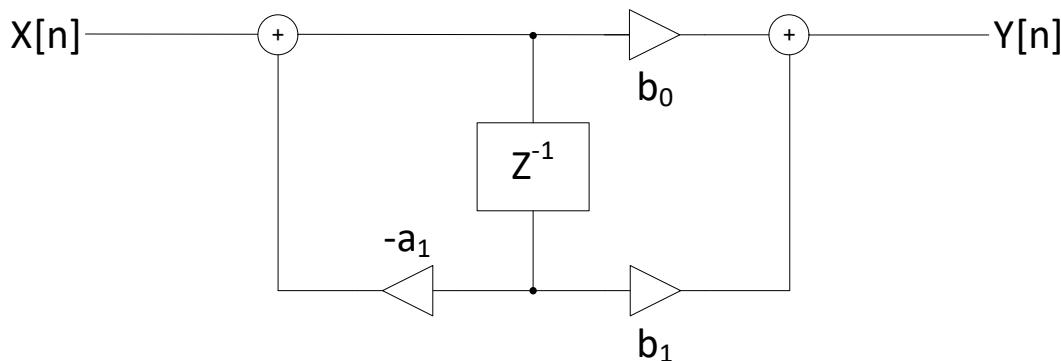


Figure 4-35. First-Order IIR System

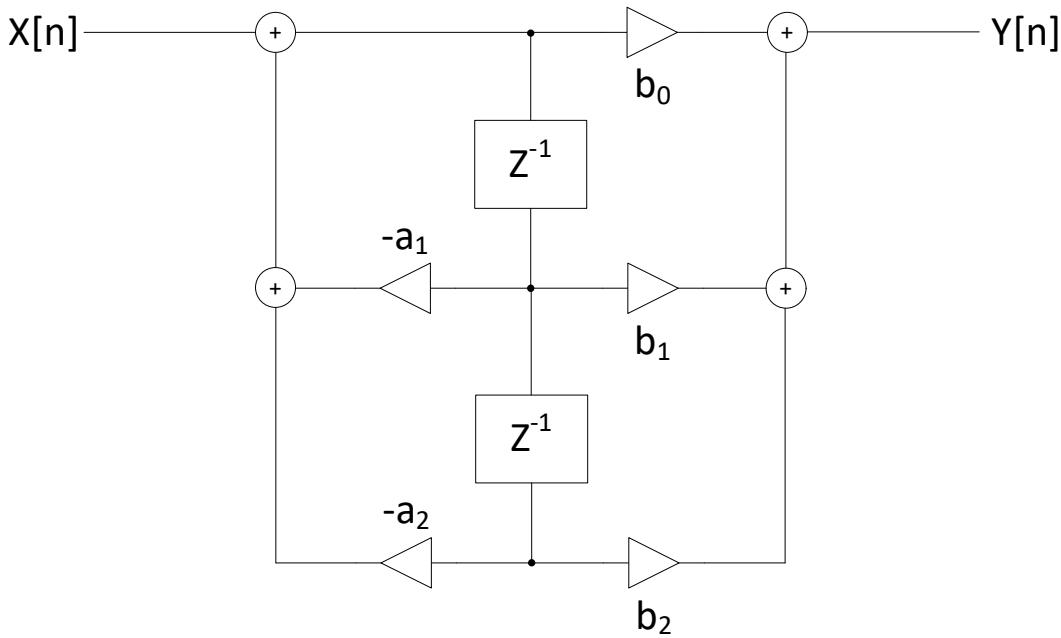


Figure 4-36. Second-Order IIR System

The filter can only be programmed when PDN_HP is set. Program the filter coefficients when PDN_HP is cleared will result in non-expected behavior.

To properly enable each filter's coefficients, after the coefficients is programmed in control port, user enable the control port filter coefficients through registers [Programmable Filter Control 1](#) and [Programmable Filter Control 2](#). When user not using the programmable filters, the filter should be disabled properly.

4.14 可编程滤波器

CS43131内置一系列可编程滤波器，供用户自定义。滤波器系数可编程，用于调整频率响应或其他特性，以满足设计需求。滤波器以由xSP设置的输入采样率运行。该功能适用于单速、双速及四速设置下的常规PCM播放。（若工作于192 kHz，MCLK_INT需为24.576 MHz。）对于WBF模式和阻抗测量模式，滤波器应适当关闭。

滤波器系列由1个一阶IIR系统（FOS）和3个二阶IIR系统（SOS）组成，实际为七阶系统。FOS和SOS结构分别如图4-35和图4-36所示。任何滤波器级均可通过系数设置选择启用或旁路。每个级别由滤波器系数表示，通过I2C写入访问。滤波器系数位于寄存器地址0x09000C至0x090041。每个系数由最高有效字节、最低有效字节及符号字节组成。

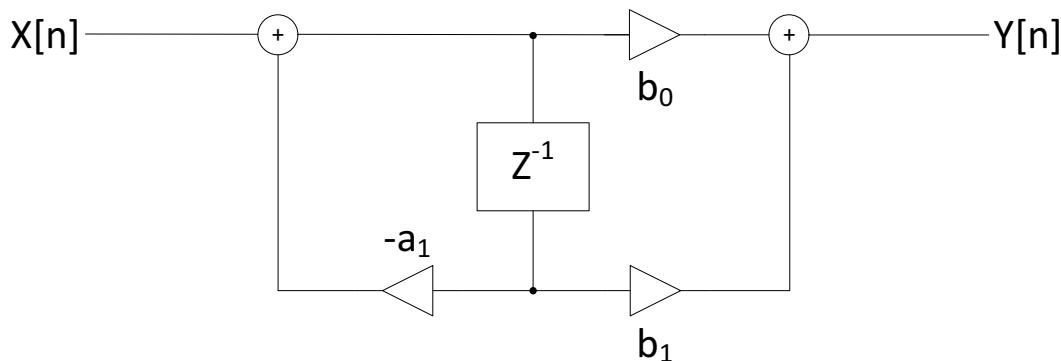


图4-35 一阶IIR系统

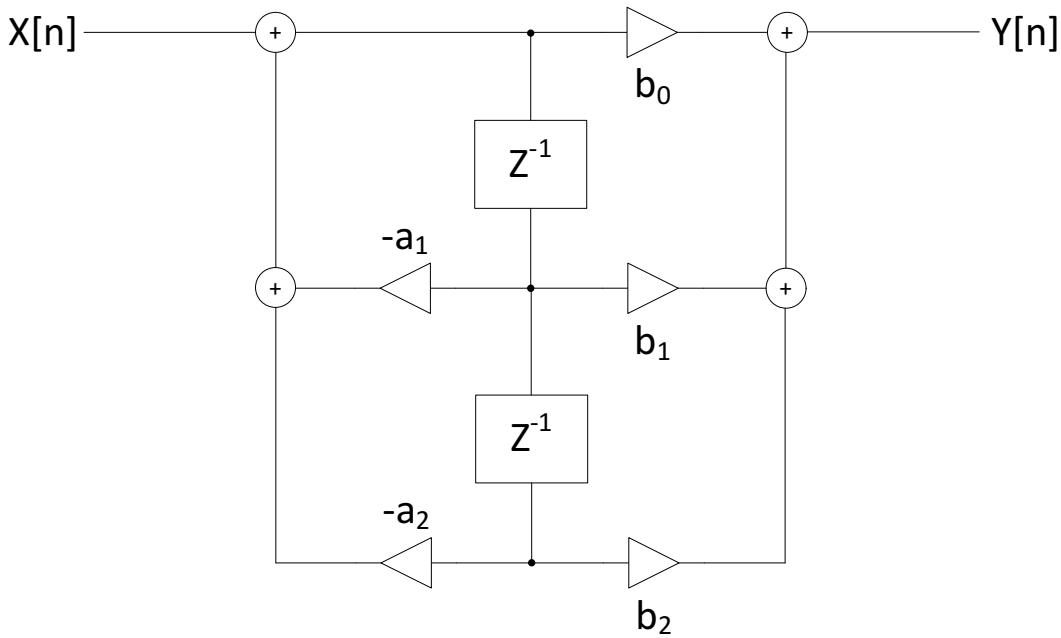


图4-36 二阶IIR系统

仅当 PDN_HP 置位时，滤波器才能被编程。在 PDN_HP 清除时编程滤波器系数将导致非预期行为。

为了正确启用每个滤波器的系数，在控制端口编程系数后，用户需通过寄存器可编程滤波器控制1和可编程滤波器控制2启用控制端口滤波器系数。当用户不使用可编程滤波器时，应正确禁用滤波器。

5 Applications

This section provides recommended application procedures and instruction sequences for standard CS43131 operations.

5.1 PLL Clocking

Data-path logic is in the MCLK_INT domain, where MCLK_INT is expected to be 22.5792 or 24.576 MHz. For clocking scenarios in which the external system MCLK provided to CS43131 is neither 22.5792 nor 24.576 MHz, the PLL must be turned on to provide the desired internal MCLK. At start up, the system uses RCO as the internal MCLK for PLL programming over I²C and switches to the PLL output after it settles. PLL start-up time is a maximum of 1 ms.

5.2 Power Sequencing

Note the following for power-up sequencing on the CS43131:

- VP must be powered up first.
- All other supplies can come up in any order before RESET is released.

Note the following for power-down sequencing on the CS43131:

- After RESET is asserted, VA/VCP/VL/VD can be removed in any order.
- VP must be powered down last.

5.3 Crystal Tuning

The CS43131 uses an external crystal as the source for internal MCLK. Refer to [Table 3-16](#) for the load capacitance that is supported by CS43131. [Table 5-1](#) lists supported crystals that meet the requirements for CS43131 and also shows also shows the XTAL_IBIAS settings for different crystals.

Table 5-1. Example List of Supported Crystals

Manufacturer ¹	Part Number ¹	Frequency (MHz)	Bias Current Strength (μ A)	Crystal Setting Register (0x20052)
River Electronics	FCX-06-22.5792J51933	22.5792	12.5	0x04
	FCX-06-24.5760J51930	24.576	7.5	0x06
NDK	NX2016SA 22.5792M EXS00A-CS09116	22.5792	15	0x02
	NX2016SA 24.576M EXS00A-CS09117	24.576		
TXC	8Y22570001	22.5792	12.5	0x04
	8Y24570001	24.576		

1. Contact your local Cirrus Logic representative for a list of supported manufacturers and part numbers.

The crystal setting register (0x20052) must be set appropriately based on the crystal used.

The frequency at which the crystal eventually oscillates can be calculated using the formula below:

$$F_{osc} = 1/(2\pi\sqrt{L_m(C_m + C_0 + C_L)}) ,$$

where

L_m = motional inductance of crystal

C_m = motional capacitance of crystal

C_0 = shunt capacitance

C_L = load capacitance

Trace capacitance and pad capacitance (approximately 0.5 pF) must also be taken into account while calculating the value of the load capacitors. Below are the steps to tune the crystal to the correct frequency:

1. Select load capacitor values that match the load capacitance spec in crystal manufacturer's data sheet.

5 应用

本节提供标准 CS43131 操作的推荐应用流程及指令序列。

5.1 PLL时钟

数据路径逻辑位于 MCLK_INT 域内，其中 MCLK_INT 预期为 22.5792 或 24.576 MHz。对于外部系统提供给 CS43131 的 MCLK 既非 22.5792 也非 24.576 MHz 的时钟场景，必须开启 PLL 以提供所需的内部 MCLK。启动时，系统使用 RCO 作为 PLL 编程的内部 MCLK（通过 I²C），并在 PLL 稳定后切换至 PLL 输出。PLL 启动时间最长为 1 ms。

5.2 电源顺序

关于 CS43131 的上电顺序，请注意以下事项：

- VP 必须首先上电。
- 在释放复位之前，所有其他电源可按任意顺序上电。

关于 CS43131 的断电顺序，请注意以下事项：

- 复位被断言后，VA/VCP/VL/VD 可按任意顺序断电。
- VP 必须最后断电。

5.3 晶体调谐

CS43131 使用外部晶体作为内部 MCLK 的时钟源。有关 CS43131 支持的负载电容，请参见表 3-16。表 5-1 列出了符合 CS43131 要求的支持晶体，并显示了不同晶体的 XTAL_IBIAS 设置。

表 5-1 支持的晶体示例列表

制造商 1	零件编号 1	频率 (MHz)	偏置电流强度 (μA)	晶体设置寄存器 (0x20052)
River Electronics	FCX-06-22.5792J51933	22.5792	12.5	0x04
	FCX-06-24.5760J51930	24.576	7.5	0x06
NDK	NX2016SA 22.5792M EXS00A-CS09116	22.5792	15	0x02
	NX2016SA 24.576M EXS00A-CS09117	24.576		
TJC	8Y22570001	22.5792	12.5	0x04
	8Y24570001	24.576		

1. 请联系您当地的 Cirrus Logic 代表，获取支持的制造商及零件编号列表。

晶体设置寄存器 (0x20052) 必须根据所用晶体进行适当设置。

晶体最终振荡频率可通过以下公式计算：

$$F_{osc} = 1/(2\pi\sqrt{L_m(C_m + C_L)/(C_m + C_0 + C_L)})$$

，其中

L_m = 晶体的动感电感

C_m = 晶体的动感电容

C_0 = 并联电容

C_L = 负载电容

计算负载电容值时，还必须考虑走线电容和焊盘电容（约 0.5 pF）。以下是将晶体调谐至正确频率的步骤：

1. 选择与晶体制造商数据表中负载电容规格相匹配的负载电容值。

2. Power up and verify communication with CS43131. If there is no communication, it is possible that the crystal did not start. Check power rails and load capacitance and try again.
3. Clear PDN_CLKOUT in the Power Down Control (0x20000) register. This sets the clock output at MCLK_INT/2 frequency from CLKOUT pin.
4. Measure the frequency and verify that it is within acceptable range of the desired frequency. If yes, continue normal operation. If not, power down the chip, change the load capacitor values and go back to step 2.

Note: These steps need to be performed only once per PCB.

5.4 Alert Mixing Shutdown

To prevent a DSD mute pattern from turning off the DAC while mixing DSD data with PCM data, turn off the auto mute by clearing the [DSD_AMUTE](#) bit.

5.5 Enable/Disable Alternate Headphone Path (HPINx)

If the user decides to use the HPINx path, the following sequences must be followed to enable/disable the alternate headphone path (HPINx).

5.5.1 HPINx Alternate Headphone Path Enable Sequence

To enable the HPINx path, follow the sequence in [Ex. 5-1](#).

Example 5-1. HPINx Enable Sequence

TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
Enable headphone input	HP Output Control 1. 0x80000	0x38	
	HP_CLAMPA	0	Function disabled
	HP_CLAMPB	0	Function disabled
	OUT_FS	11	Headphone output voltage setting is irrelevant
	HP_IN_EN	1	Enable HPIN switch
	HP_IN_LP	0	Function disabled
	Reserved	0	
	+1dB_EN	0	
Wait for 1.1 ms.			
Enable low power mode	HP Output Control 1. 0x80000	0x3C	
	HP_CLAMPA	0	Function disabled
	HP_CLAMPB	0	Function disabled
	OUT_FS	11	Headphone output voltage setting is irrelevant
	HP_IN_EN	1	Enable HPIN switch
	HP_IN_LP	1	Function enabled
	Reserved	0	
	+1dB_EN	0	

5.5.2 HPINx Disable Sequence

To disable the HPINx path, follow the sequence in [Ex. 5-2](#). For pop-free operation, the audio input must be completely ramped down before executing this sequence.

Example 5-2. HPINx Disable

TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
Disable HPINx low power mode	HP Output Control 1. 0x80000	0x38	
	HP_CLAMPA	0	Function disabled
	HP_CLAMPB	0	Function disabled
	OUT_FS	11	Headphone output voltage setting is irrelevant
	HP_IN_EN	1	Enable HPIN switch
	HP_IN_LP	0	Function disabled
	Reserved	0	
	+1dB_EN	0	

2. 上电并验证与CS43131的通信。如无通信，可能是晶振未启动。检查电源轨和负载电容后重试。
3. 清除电源关闭控制寄存器（0x20000）中的PDN_CLKOUT位。此操作将CLKOUT引脚的时钟输出设置为MCLK_INT/2频率。
4. 测量频率并确认其在期望频率的可接受范围内。如符合，继续正常操作。如不符合，关闭芯片电源，更改负载电容值，然后返回步骤2。

注意：这些步骤每块PCB仅需执行一次。

5.4 警报混合关断

为防止在混合DSD数据与PCM数据时DSD静音模式关闭DAC，通过清除DSD_AMUTE位关闭自动静音。

5.5 启用/禁用备用耳机路径 (HPINx)

如果用户决定使用 HPINx 路径，必须遵循以下步骤以启用或禁用备用耳机路径 (HPINx)。

5.5.1 HPINx 备用耳机路径启用序列

要启用 HPINx 路径，请按照示例 5-1 中的顺序操作。

示例 5-1. HPINx 启用序列

TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
启用耳机输入 HP 输出控制 1。0x80000		0x38	
	HP_CLAMPA	0	功能禁用
	HP_CLAMPB	0	功能禁用
	OUT_FS	11	耳机输出电压设置无关紧要
	HP_IN_EN	1	使能 HPIN 开关
	HP_IN_LP	0	功能已禁用
	保留	0	
	+1dB_EN	0	
等待 1.1 毫秒。			
使能低功耗模式 耳机输出控制 1, 0x80000		0x3C	
	HP_CLAMPA	0	功能禁用
	HP_CLAMPB	0	功能禁用
	OUT_FS	11	耳机输出电压设置无关紧要
	HP_IN_EN	1	使能 HPIN 开关
	HP_IN_LP	1	功能已启用
	保留	0	
	+1dB_EN	0	

5.5.2 HPINx 禁用序列

要禁用 HPINx 路径，请按照示例 5-2 中的顺序操作。为实现无噪声操作，执行此序列前必须完全降低音频输入电平。

示例 5-2. HPINx 禁用

TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
禁用 HPINx 备用耳机模式	耳机输出控制 1, 0x80000	0x38	
	HP_CLAMPA	0	功能禁用
	HP_CLAMPB	0	功能禁用
	OUT_FS	11	耳机输出电压设置无关紧要
	HP_IN_EN	1	使能 HPIN 开关
	HP_IN_LP	0	功能已禁用
	保留	0	
	+1dB_EN	0	

Example 5-2. HPINx Disable (Cont.)

TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
Disable headphone input	HP Output Control 1. 0x80000	0x30	
	HP_CLAMPA	0	
	HP_CLAMPB	0	
	OUT_FS	11	
	HP_IN_EN	0	
	HP_IN_LP	0	
	Reserved	0	
	+1dB_EN	0	Disable HPIN

5.6 Headphone Power Down Sequences

Examples of power down sequences for PCM and DSD are shown in [Ex. 5-3](#) and [Ex. 5-4](#), respectively. Follow the stated sequence every time to shut down the headphone output. The sequence assumes that the PDN_DONE_INT interrupt bit is unmasked.

5.6.1 PCM Power Down Sequence

Example 5-3. PCM Power Down Sequence

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Enable PDN_DONE interrupt	Interrupt Mask 1. 0xF0010	data(0xF0010) AND (0xFE)	
		DAC_OVFL_INT_MASK	x	
		HPDETECT_PLUG_INT_MASK	x	
		HPDETECT_UNPLUG_INT_MASK	x	
		XTAL_READY_INT_MASK	x	
		XTAL_ERROR_INT_MASK	x	
		PLL_READY_INT_MASK	x	
		PLL_ERROR_INT_MASK	x	
		PDN_DONE_INT_MASK	0	Enable PDN_DONE interrupt
2	Power down amplifier	Power Down Control. 0x20000	data(0x20000) OR (0x10)	
		PDN_XSP	x	
		PDN_ASP	x	
		PDN_DSDIF	x	
		PDN_HP	1	Turn off HP
		PDN_XTAL	x	
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	x	
3	Wait for interrupt. Check for PDN_DONE_INT = 1 in Interrupt Status 1 register (0xF0000).			
4	Power down ASP	Power Down Control. 0x20000	data(0x20000) OR (0x40)	
		PDN_XSP	x	
		PDN_ASP	1	Turn off ASP
		PDN_DSDIF	x	
		PDN_HP	x	
		PDN_XTAL	x	
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	x	

5.6.2 DSD Power Down Sequence

Example 5-4. DSD Power Down Sequence

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Enable PDN_DONE interrupt	Interrupt Mask 1. 0xF0010	data(0xF0010) AND (0xFE)	
		DAC_OVFL_INT_MASK	x	
		HPDETECT_PLUG_INT_MASK	x	
		HPDETECT_UNPLUG_INT_MASK	x	
		XTAL_READY_INT_MASK	x	
		XTAL_ERROR_INT_MASK	x	
		PLL_READY_INT_MASK	x	
		PLL_ERROR_INT_MASK	x	
		PDN_DONE_INT_MASK	0	Enable PDN_DONE interrupt

示例 5-2. HPINx 禁用 (续)

TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
禁用耳机输入 耳机输出控制 1, 0x80000		0x30	
	HP_CLAMPA	0	
	HP_CLAMPB	0	
	OUT_FS	11	
	HP_IN_EN	0	禁用 HPIN
	HP_IN_LP	0	
	保留	0	
	+1dB_EN	0	

5.6 耳机电源关闭顺序

PCM 和 DSD 的关机顺序示例分别见示例 5-3 和示例 5-4。每次关闭耳机输出时，请遵循所述顺序。该顺序假设 PDN_DONE_INT 中断位未屏蔽。

5.6.1 PCM 关机顺序

示例 5-3. PCM 关机顺序

步骤	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1 使能 PDN_DONE 中断	中断屏蔽 1, 0xF0010		数据(0xF0010) 与 (0xFE)	
	DAC_OVFL_INT_MASK	x		
	HPDETECT_PLUG_INT_MASK	x		
	HPDETECT_UNPLUG_INT_MASK	x		
	XTAL_READY_INT_MASK	x		
	XTAL_ERROR_INT_MASK	x		
	PLL_READY_INT_MASK	x		
	PLL_ERROR_INT_MASK	x		
	PDN_DONE_INT_MASK	0	使能 PDN_DONE 中断	
2 功放关断控制, 0x20000			数据(0x20000) 或 (0x10)	
	PDN_XSP	x		
	PDN_ASP	x		
	PDN_DSDIF	x		
	PDN_HP	1	关闭耳机	
	PDN_XTAL	x		
	PDN_PLL	x		
	PDN_CLKOUT	x		
	保留	x		
3 等待中断。检查中断状态寄存器 1 (0xF0000) 中 PDN_DONE_INT 是否为 1。				
4 关闭 ASP	关断控制, 0x20000		数据(0x20000) 或 (0x40)	
	PDN_XSP	x		
	PDN_AS	1	关闭 ASP	
	P_PDN_DSD	x		
	IF_PDN	x		
	HP_PDN_X	x		
	TAL_PDN	x		
	PLL_PDN_CL	x		
	KOUT 保留	x		

5.6.2 DSD 关机顺序

示例 5-4. DSD 关机顺序

步骤	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1 使能 PDN_DONE 中断	中断屏蔽 1, 0xF0010		数据(0xF0010) 与 (0xFE)	
	DAC_OVFL_INT_MASK	x		
	HPDETECT_PLUG_INT_MASK	x		
	HPDETECT_UNPLUG_INT_MASK	x		
	XTAL_READY_INT_MASK	x		
	XTAL_ERROR_INT_MASK	x		
	PLL_READY_INT_MASK	x		
	PLL_ERROR_INT_MASK	x		
	PDN_DONE_INT_MASK	0	使能 PDN_DONE 中断	

Example 5-4. DSD Power Down Sequence (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
2	Power down amplifier	Power Down Control. 0x20000	data(0x20000) OR (0x10)	
		PDN_XSP	x	
		PDN_ASP	x	
		PDN_DSDIF	x	
		PDN_HP	1	Turn off HP
		PDN_XTAL	x	
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	x	
3	Wait for interrupt. Check for PDN_DONE_INT = 1 in Interrupt Status 1 register (0xF0000).			
4	Power down XSP/ASP/ DSDIF interfaces	Power Down Control. 0x20000	data(0x20000) OR (0xE0)	
		PDN_XSP	1	
		PDN_ASP	1	
		PDN_DSDIF	1	
		PDN_HP	x	
		PDN_XTAL	x	
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	x	

5.7 Headphone Power-Up Sequence

An example of the power-up sequence for PCM and DSD are shown in [Ex. 5-5](#) and [Ex. 5-6](#), respectively. Follow the stated sequence every time to power up the headphone output.

5.7.1 PCM Power-Up Sequence

Example 5-5. PCM Power-Up Sequence

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Pop-free power-up settings	0x10010 0x80032	0x99 0x20	
2	Power on appropriate interface. Power Down Control. 0x20000		data (0x20000) AND (0xBF)	
		PDN_XSP	x	
		PDN_ASP	0	Power up ASP
		PDN_DSDIF	x	
		PDN_HP	x	
		PDN_XTAL	x	
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	0	
3	Power on amplifier	Power Down Control. 0x20000	data (0x20000) AND (0xEF)	
		PDN_XSP	x	
		PDN_ASP	x	
		PDN_DSDIF	x	
		PDN_HP	0	Power up HP
		PDN_XTAL	x	
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	0	
4	Wait for 12 ms			
5	Restore default settings	0x80032 0x10010	0x00 0x00	

示例 5-4。DSD 断电序列 (续)

步骤	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
2	功放关断控制, 0x20000		数据(0x20000) 或 (0x10)	
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT 保留	x x x 1 x x x x	关闭耳机
3	等待中断。检查中断状态寄存器 1 (0xF0000) 中 PDN_DONE_INT 是否为 1。			
4	关闭 XSP/ASP/ DSDIF 接口	关断控制, 0x20000	数据(0x20000) 或 (0xE0)	
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT 保留	1 1 1 x x x x x	

5.7 耳机上电顺序

PCM 和 DSD 的上电顺序示例如示例 5-5 和示例 5-6 所示。每次上电耳机输出时，请遵循所述顺序。

5.7.1 PCM 上电顺序

示例 5-5. PCM 上电顺序

步骤	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	无爆音上电设置 0x10010		0x99	
		0x80032	0x20	
2	开启相应接口。关机控制。0x20000		数据 (0x20000) 与 (0xBF)	
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT 保留	x 0 x x x x x 0	上电 ASP
3	开启放大器	关断控制, 0x20000	数据 (0x20000) 与 (0xEF)	
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT 保留	x x x 0 x x x 0	耳机供电开启
4	等待 12 毫秒			
5	恢复默认设置	0x80032	0x00	
		0x10010	0x00	

5.7.2 DSD Power-Up Sequence

Example 5-6. DSD Power-Up Sequence

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Pop-free power-up settings	0x10010	0x99	
		0x80032	0x20	
2	Power on appropriate interface. Power Down Control. 0x20000		data (0x20000) AND (0xHH)	For DoP on XSP, HH = 7F. For DoP on ASP, HH = BF. For DSD interface, HH = DF.
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT Reserved	B B B x x x x x	Enable XSP, ASP, or DSDIF interface
3	Power on amplifier	Power Down Control. 0x20000	data (0x20000) AND (0xEF)	
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT Reserved	x x x 0 x x x 0	Power up HP
4	Wait for 12 ms			
5	Restore default settings	0x80032 0x10010	0x00 0x00	

5.8 Power-Down Sequence in External VCPFILT Mode

These sequences allow the CS43131 to be powered down in external VCPFILT mode without any audible pops.

5.8.1 PCM Pop-Free Power-Down Sequence in External VCPFILT Mode

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Pop-free power-down settings	0x10010	0x99	
		0x80046	0x21	
2	Mute both channels	PCM Path Signal Control 1. 0x90003	data(0x90003) OR (0x03)	
		PCM_RAMP_DOWN PCM_VOL_BEQA PCM_SZC PCM_AMUTE PCM_AMUTEBEQA PCM_MUTE_A PCM_MUTE_B	x x xx x x 1 1	Channel A is muted Channel B is muted
3	Wait 150 ms for mute to occur			
4	Enable PDN_DONE interrupt	Interrupt Mask 1. 0xF0010	data(0xF0010) AND (0xFE)	
		DAC_OVFL_INT_MASK HPDETECT_PLUG_INT_MASK HPDETECT_UNPLUG_INT_MASK XTAL_READY_INT_MASK XTAL_ERROR_INT_MASK PLL_READY_INT_MASK PLL_ERROR_INT_MASK PDN_DONE_INT_MASK	x x x x x x x 0	Enable PDN_DONE interrupt
5	Power down amplifier	Power Down Control. 0x20000	data(0x20000) OR (0x10)	
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT Reserved	x x x 1 x x x x	Turn off HP
6	Wait for interrupt. Check for PDN_DONE_INT = 1 in Interrupt Status 1 register (0xF0000).			

5.7.2 DSD 上电序列

示例 5-6。DSD 上电序列

步骤	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1 无爆音上电设置	0x10010		0x99	
		0x80032	0x20	
2 开启相应接口。关机控制。0x20000			数据 (0x20000) 与 (0xEF)	XSP 上的 DoP, HH = 7F。 ASP 上的 DoP, HH = BF。 DSD 接口, HH = DF。
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT 保留	B B B x x x x x	启用 XSP、ASP 或 DSDIF 接口
3 开启放大器	关断控制, 0x20000		数据 (0x20000) 与 (0xEF)	
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT 保留	x x x 0 x x x 0	耳机供电开启
4 等待 12 毫秒				
5 恢复默认设置	0x80032		0x00	
		0x10010	0x00	

5.8 外部 VCPFILT 模式下的断电序列

这些序列允许 CS43131 在外部 VCPFILT 模式下断电时无任何可听噼啪声。

5.8.1 外部 VCPFILT 模式下的 PCM 无噼啪断电序列

步骤	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1 无爆音关机设置	0x10010 0x80046		0x99 0x21	
2 静音两个通道	PCM路径信号控制1, 0x90003		数据(0x90003) 或 (0x03)	
	PCM_RAMP_DOWN PCM_VOL_BEQA PCM_SZC PCM_AMUTE PCM_AMUTEBEQA PCM_MUTE_A PCM_MUTE_B		x x xx x x 1 1	通道A已静音 通道B已静音
3 等待150毫秒以实现静音				
4 使能 PDN_DONE 中断	中断屏蔽 1, 0xF0010		数据(0xF0010) 与 (0xFE)	
	DAC_OVFL_INT_MASK HPDETECT_PLUG_INT_MASK HPDETECT_UNPLUG_INT_MASK XTAL_READY_INT_MASK XTAL_ERROR_INT_MASK PLL_READY_INT_MASK PLL_ERROR_INT_MASK PDN_DONE_INT_MASK		x x x x x x x 0	使能 PDN_DONE 中断
5 关闭放大器电源	关断控制, 0x20000		数据(0x20000) 或 (0x10)	
	PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT 保留		x x x 1 x x x x	关闭耳机
6 等待中断。检查中断状态寄存器 1 (0xF0000) 中 PDN_DONE_INT 是否为 1。				

7	Power down ASP	Power Down Control. 0x20000	data(0x20000) OR (0x40)
		PDN_XSP	x
		PDN_ASP	1
		PDN_DSDIF	x
		PDN_HP	x
		PDN_XTAL	x
		PDN_PLL	x
		PDN_CLKOUT	x
		Reserved	x
8	Unmute both channels	PCM Path Signal Control 1. 0x90003	data(0x90003) AND (0xFC)
		PCM_RAMP_DOWN	x
		PCM_VOL_BEQA	x
		PCM_SZC	xx
		PCM_AMUTE	x
		PCM_AMUTEBEQA	x
		PCM_MUTE_A	0
		PCM_MUTE_B	0
9	Restore default settings	0x80046 0x10010	0x20 0x00

5.8.2 DSD Pop-Free Power-Down Sequence in External VCPFILT Mode

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Pop-free power-down settings	0x10010 0x80046	0x99 0x21	
2	Mute both channels	DSD Processor Path Signal Control 1. 0x70002	data(0x70002) OR (0x03)	
		DSD_RAMP_UP	x	
		DSD_VOL_BEQA	x	
		DSD_SZC	x	
		Reserved	x	
		DSD_AMUTE	x	
		DSD_AMUTE_BEQA	x	
		DSD_MUTE_A	1	Channel A is muted
		DSD_MUTE_B	1	Channel B is muted
3	Wait 150 ms for mute to occur			
4	Enable PDN_DONE interrupt	Interrupt Mask 1. 0xF0010	data(0xF0010) AND (0xFE)	
		DAC_OVFL_INT_MASK	x	
		HPDETECT_PLUG_INT_MASK	x	
		HPDETECT_UNPLUG_INT_MASK	x	
		XTAL_READY_INT_MASK	x	
		XTAL_ERROR_INT_MASK	x	
		PLL_READY_INT_MASK	x	
		PLL_ERROR_INT_MASK	x	
		PDN_DONE_INT_MASK	0	Enable PDN_DONE interrupt
5	Power down amplifier	Power Down Control. 0x20000	data(0x20000) OR (0x10)	
		PDN_XSP	x	
		PDN_ASP	x	
		PDN_DSDIF	x	
		PDN_HP	1	Turn off HP
		PDN_XTAL	x	
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	x	
6	Wait for interrupt. Check for PDN_DONE_INT = 1 in Interrupt Status 1 register (0xF0000).			
7	Power down XSP/ASP/DSDIF interfaces	Power Down Control. 0x20000	data(0x20000) OR (0xE0)	
		PDN_XSP	1	
		PDN_ASP	1	
		PDN_DSDIF	1	
		PDN_HP	x	
		PDN_XTAL	x	
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	x	

7 关闭 ASP	关断控制, 0x20000	数据(0x20000) 或 (0x40)
	PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT 保留	x 1 x x x x x x
8 取消两个通道静音	PCM路径信号控制1, 0x90003	数据(0x90003) 与 (0xFC)
	PCM_RAMP_DOWN PCM_VOL_BEQA PCM_SZC PCM_AMUTE PCM_AMUTEBEQA PCM_MUTE_A PCM_MUTE_B	x x xx x x 0 通道A已取消静音 0 通道B已取消静音
9 恢复默认设置	0x80046 0x10010	0x20 0x00

5.8.2 外部VCPFILT模式下的DSD无爆音关机序列

步骤	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1 无爆音关机设置		0x10010 0x80046	0x99 0x21	
2 静音两个通道		DSD处理器路径信号控制1 0x70002	数据(0x70002) 或 (0x03)	
	DSD_RAMP_UP DSD_VOL_BEQA DSD_SZC 保留 DSD_AMUTE DSD_AMUTE_BEQA DSD_MUTE_A DSD_MUTE_B	x x x x x x 1 通道A已静音 1 通道B已静音		
3 等待150毫秒以实现静音				
4 使能 PDN_DONE 中断		中断屏蔽 1, 0xF0010	数据(0xF0010) 与 (0xFE)	
	DAC_OVFL_INT_MASK HPDETECT_PLUG_INT_MASK HPDETECT_UNPLUG_INT_MASK XTAL_READY_INT_MASK XTAL_ERROR_INT_MASK PLL_READY_INT_MASK PLL_ERROR_INT_MASK PDN_DONE_INT_MASK	x x x x x x x 0		使能 PDN_DONE 中断
5 关闭放大器电源		关断控制, 0x20000	数据(0x20000) 或 (0x10)	
	PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT 保留	x x x 1 关闭耳机 x x x x		
6 等待中断。检查中断状态寄存器 1 (0xF0000) 中 PDN_DONE_INT 是否为 1。				
7 关闭 XSP/ASP/DSDIF 接口的电源关闭控制。0x20000			数据(0x20000) 或 (0xE0)	
	PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT 保留	1 1 1 x x x x		

8	Unmute both channels	DSD Processor Path Signal Control 1. 0x70002	data(0x70002) AND (0xFC)
		DSD_RAMP_UP	x
		DSD_VOL_BEQA	x
		DSD_SZC	x
		Reserved	x
		DSD_AMUTE	x
		DSD_AMUTE_BEQA	x
		DSD_MUTE_A	0
		DSD_MUTE_B	0
			Channel A is unmuted Channel B is unmuted
9	Restore default settings	0x80046 0x10010	0x20 0x00

5.9 Enabling and Disabling NOS Filter

Section 5.9.1 and Section 5.9.2 describe pop-free sequences for enabling and disabling the NOS filter, respectively.

5.9.1 Sequence for Enabling NOS Filter

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Set mute to occur with soft ramp only	PCM Path Signal Control 1. 0x90003	data (0x90003) AND (0xEF) OR (0x20)	
		PCM_RAMP_DOWN	x	
		PCM_VOL_BEQA	x	
		PCM_SZC	10	Enable soft ramp
		PCM_AMUTE	x	
		PCM_AMUTEBEQA	x	
		PCM_MUTE_A	x	
		PCM_MUTE_B	x	
2	Mute both channels	PCM Path Signal Control 1. 0x90003	data (0x90003) OR (0x03)	
		PCM_RAMP_DOWN	x	
		PCM_VOL_BEQA	x	
		PCM_SZC	xx	
		PCM_AMUTE	x	
		PCM_AMUTEBEQA	x	
		PCM_MUTE_A	1	Channel A output is muted
		PCM_MUTE_B	1	Channel B output is muted
3	Wait for 150 ms for mute to occur			
4	Enable NOS filter	PCM Filter Option. 0x90000	data (0x90000) OR (0x20)	
		FILTER_SLOW_FASTB	x	
		PHCOMP_LOWLATB	x	
		NOS	1	NOS emulation mode is on
		Reserved	0 0	
		PCM_WBF_EN	x	
		HIGH_PASS	x	
		DEEMP_ON	x	
5	Restore PCM_SZC mode if desired	PCM Path Signal Control 1. 0x90003	0xHH	
		PCM_RAMP_DOWN	x	
		PCM_VOL_BEQA	x	
		PCM_SZC	BB	Restore PCM_SZC to desired value
		PCM_AMUTE	x	
		PCM_AMUTEBEQA	x	
		PCM_MUTE_A	x	
		PCM_MUTE_B	x	
6	Unmute both channels	PCM Path Signal Control 1. 0x90003	data (0x90003) AND (0xFC)	
		PCM_RAMP_DOWN	x	
		PCM_VOL_BEQA	x	
		PCM_SZC	xx	
		PCM_AMUTE	x	
		PCM_AMUTEBEQA	x	
		PCM_MUTE_A	0	Function is disabled
		PCM_MUTE_B	0	Function is disabled

8 取消两个通道静音	DSD处理器路径信号控制1 0x70002	数据(0x70002) 与(0xFC)
	DSD_RAMP_UP	x
	DSD_VOL_BEQA	x
	DSD_SZC	x
	保留	x
	DSD_AMUTE	x
	DSD_AMUTE_BEQA	x
	DSD_MUTE_A	0 通道A已取消静音
	DSD_MUTE_B	0 通道B已取消静音
9 恢复默认设置	0x80046 0x10010	0x20 0x00

5.9 NOS 滤波器的启用与禁用

第 5.9.1 节和第 5.9.2 节分别描述了启用和禁用 NOS 滤波器的无爆音序列。

5.9.1 启用 NOS 滤波器的序列

步骤	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	PCM路径信号控制1, 0x90003	数据(0x90003) 与(0xEF)或 (0x20)		
	PCM_RAMP_DOWN	x		
	PCM_VOL_BEQA	x		
	PCM_SZC	10	启用软斜坡	
	PCM_AMUTE	x		
	PCM_AMUTEBEQA	x		
	PCM_MUTE_A	x		
	PCM_MUTE_B	x		
2 静音两个通道	PCM路径信号控制1, 0x90003	数据(0x90003) 或(0x03)		
	PCM_RAMP_DOWN	x		
	PCM_VOL_BEQA	x		
	PCM_SZC	xx		
	PCM_AMUTE	x		
	PCM_AMUTEBEQA	x		
	PCM_MUTE_A	1 通道 A 输出静音		
	PCM_MUTE_B	1 通道 B 输出静音		
3 等待 150 毫秒以完成静音				
4 启用 NOS 滤波器	PCM 滤波器选项。0x90000	数据(0x90000) 或(0x20)		
	FILTER_SLOW_FASTB	x		
	PHCOMP_LOWLATB	x		
	NOS	1	NOS 仿真模式已开启	
	保留	0 0		
	PCM_WBF_EN	x		
	HIGH_PASS	x		
	DEEMP_ON	x		
5 如需, 恢复 PCM_SZC 模式	PCM路径信号控制1, 0x90003	0xHH		
	PCM_RAMP_DOWN	x		
	PCM_VOL_BEQA	x		
	PCM_SZC	BB	将 PCM_SZC 恢复至所需值	
	PCM_AMUTE	x		
	PCM_AMUTEBEQA	x		
	PCM_MUTE_A	x		
	PCM_MUTE_B	x		
6 取消两个通道静音	PCM路径信号控制1, 0x90003	数据(0x90003) 与(0xFC)		
	PCM_RAMP_DOWN	x		
	PCM_VOL_BEQA	x		
	PCM_SZC	xx		
	PCM_AMUTE	x		
	PCM_AMUTEBEQA	x		
	PCM_MUTE_A	0 功能已禁用		
	PCM_MUTE_B	0 功能已禁用		

5.9.2 Sequence for Disabling NOS Filter

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Set mute to occur with soft ramp only	PCM Path Signal Control 1. 0x90003	data (0x90003) AND (0xEF) OR (0x20)	
		PCM_RAMP_DOWN PCM_VOL_BEQA PCM_SZC PCM_AMUTE PCM_AMUTEBEQA PCM_MUTE_A PCM_MUTE_B	x x 10 x x x x	Enable soft ramp
2	Mute both channels	PCM Path Signal Control 1. 0x90003	data (0x90003) OR (0x03)	
		PCM_RAMP_DOWN PCM_VOL_BEQA PCM_SZC PCM_AMUTE PCM_AMUTEBEQA PCM_MUTE_A PCM_MUTE_B	x x xx x x 1 1	Channel A output is muted Channel B output is muted
3	Wait for 150 ms for mute to occur			
4	Disable NOS filter	PCM Filter Option. 0x90000	data (0x90000) AND (0xDF)	
		FILTER_SLOW_FASTB PHCOMP_LOWLATB NOS Reserved PCM_WBF_EN HIGH_PASS DEEMP_ON	x x 0 0 0 x x x	NOS emulation mode is off
5	Restore PCM_SZC mode if desired	PCM Path Signal Control 1. 0x90003	0xHH	
		PCM_RAMP_DOWN PCM_VOL_BEQA PCM_SZC PCM_AMUTE PCM_AMUTEBEQA PCM_MUTE_A PCM_MUTE_B	x x BB x x x x	Restore PCM_SZC to desired value
6	Unmute both channels	PCM Path Signal Control 1. 0x90003	data (0x90003) AND (0xFC)	
		PCM_RAMP_DOWN PCM_VOL_BEQA PCM_SZC PCM_AMUTE PCM_AMUTEBEQA PCM_MUTE_A PCM_MUTE_B	x x xx x x 0 0	Function is disabled Function is disabled

5.10 Sequence for Using PCM Invert Bits

[Section 5.10.1](#) and [Section 5.10.2](#) describe sequences for enabling the PCM_INV_A and PCM_INV_B bits, respectively.

5.10.1 Sequence for Enabling Channel A Invert

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Invert channel A calibration	0x180005 0x180006 0x180015 0x180016 0x180025 0x180026 0x180035 0x180036	0xDC 0xFA 0xFB 0xFB 0xF5 0xFE 0x8F 0xFC	
2	Enable channel A invert	PCM Path Signal Control 2. 0x90004	data (0x90004) OR (0x08)	
		Reserved PCM_INV_A PCM_INV_B PCM_SWAP_CHAN PCM_COPY_CHAN	0000 1 x x x	Enable Channel A invert

5.9.2 禁用 NOS 滤波器的序列

步骤	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1 设置静音仅在软斜坡期间发生	PCM路径信号控制1, 0x90003		数据 (0x90003) 与 (0xEF) 或 (0x20)	
	PCM_RAMP_DOWN		x	
	PCM_VOL_BEQA		x	
	PCM_SZC		10	启用软斜坡
	PCM_AMUTE		x	
	PCM_AMUTEBEQA		x	
	PCM_MUTE_A		x	
	PCM_MUTE_B		x	
2 静音两个通道	PCM路径信号控制1, 0x90003		数据 (0x90003) 或 (0x03)	
	PCM_RAMP_DOWN		x	
	PCM_VOL_BEQA		x	
	PCM_SZC		xx	
	PCM_AMUTE		x	
	PCM_AMUTEBEQA		x	
	PCM_MUTE_A		1	通道 A 输出静音
	PCM_MUTE_B		1	通道 B 输出静音
3 等待 150 毫秒以完成静音				
4 禁用 NOS 滤波器	PCM 滤波器选项。0x90000		数据 (0x90000) 与 (0xDF) 进行 AND 运算	
	FILTER_SLOW_FASTB		x	
	PHCOMP_LOWLATB		x	
	NOS		0	NOS 仿真模式已关闭
	保留		0 0	
	PCM_WBF_EN		x	
	HIGH_PASS		x	
	DEEMP_ON		x	
5 如需, 恢复 PCM_SZC 模式	PCM路径信号控制1, 0x90003		0xHH	
	PCM_RAMP_DOWN		x	
	PCM_VOL_BEQA		x	
	PCM_SZC		BB	将 PCM_SZC 恢复至所需值
	PCM_AMUTE		x	
	PCM_AMUTEBEQA		x	
	PCM_MUTE_A		x	
	PCM_MUTE_B		x	
6 取消两个通道静音	PCM路径信号控制1, 0x90003		数据 (0x90003) 与 (0xFC)	
	PCM_RAMP_DOWN		x	
	PCM_VOL_BEQA		x	
	PCM_SZC		xx	
	PCM_AMUTE		x	
	PCM_AMUTEBEQA		x	
	PCM_MUTE_A		0	功能已禁用
	PCM_MUTE_B		0	功能已禁用

5.10 使用 PCM 反转位的顺序

第 5.10.1 节和第 5.10.2 节分别描述了启用 PCM_INV_A 和 PCM_INV_B 位的序列。

5.10.1 启用通道 A 反转的序列

步骤	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1 反转通道 A 校准		0x180005	0xDC	
		0x180006	0xFA	
		0x180015	0xFB	
		0x180016	0xFB	
		0x180025	0xF5	
		0x180026	0xFE	
		0x180035	0x8F	
		0x180036	0xFC	
2 使能通道A反相	PCM路径信号控制2, 地址0x90004		数据 (0x90004) 或 (0x08)	
	保留		0000	
	PCM_INV_A		1	使能通道A反相
	PCM_INV_B		x	
	PCM_SWAP_CHAN		x	
	PCM_COPY_CHAN		x	

5.10.2 Sequence for Disabling Channel A Invert

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Restore channel A calibration	0x180005	0x24	
		0x180006	0x05	
		0x180015	0x05	
		0x180016	0x04	
		0x180025	0xB	
		0x180026	0x01	
		0x180035	0x71	
		0x180036	0x03	
2	Disable channel A invert	PCM Path Signal Control 2. 0x90004	data (0x90004) AND (0xF7)	
		Reserved	0000	
		PCM_INV_A	0	Disable Channel A invert
		PCM_INV_B	x	
		PCM_SWAP_CHAN	x	
		PCM_COPY_CHAN	x	

5.10.3 Sequence for Enabling Channel B Invert

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Invert channel B calibration	0x18000D	0x74	
		0x18000E	0xFA	
		0x18001D	0xCF	
		0x18001E	0xFB	
		0x18002D	0xD0	
		0x18002E	0xFE	
		0x18003D	0x64	
		0x18003E	0xFC	
2	Enable channel B invert	PCM Path Signal Control 2. 0x90004	data (0x90004) OR (0x04)	
		Reserved	0000	
		PCM_INV_A	x	
		PCM_INV_B	1	Enable Channel B invert
		PCM_SWAP_CHAN	x	
		PCM_COPY_CHAN	x	

5.10.4 Sequence for Disabling Channel B Invert

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Restore channel B calibration	0x18000D	0x8C	
		0x18000E	0x05	
		0x18001D	0x31	
		0x18001E	0x04	
		0x18002D	0x30	
		0x18002E	0x01	
		0x18003D	0x9C	
		0x18003E	0x03	
2	Disable channel B invert	PCM Path Signal Control 2. 0x90004	data (0x90004) AND (0xFB)	
		Reserved	0000	
		PCM_INV_A	x	
		PCM_INV_B	0	Disable Channel B invert
		PCM_SWAP_CHAN	x	
		PCM_COPY_CHAN	x	

5.10.2 禁用通道A反相的操作顺序

步骤	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	恢复通道A校准 0x180005		0x24	
		0x180006	0x05	
		0x180015	0x05	
		0x180016	0x04	
		0x180025	0x0B	
		0x180026	0x01	
		0x180035	0x71	
		0x180036	0x03	
2	禁用通道A反相	PCM路径信号控制2, 地址0x90004	数据 (0x90004) 与运算 (0xF7)	
		保留	0000	
		PCM_INV_A	0	禁用通道A反相
		PCM_INV_B	x	
		PCM_SWAP_CHAN	x	
		PCM_COPY_CHAN	x	

5.10.3 启用通道B反相的操作顺序

步骤	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	反相通道B校准	0x18000D	0x74	
		0x18000E	0xFA	
		0x18001D	0xCF	
		0x18001E	0xFB	
		0x18002D	0xD0	
		0x18002E	0xFE	
		0x18003D	0x64	
		0x18003E	0xFC	
2	使能通道B反相	PCM路径信号控制2, 地址0x90004	数据 (0x90004) 或 (0x04)	
		保留	0000	
		PCM_INV_A	x	
		PCM_INV_B	1	使能通道B反相
		PCM_SWAP_CHAN	x	
		PCM_COPY_CHAN	x	

5.10.4 禁用通道B反相的操作序列

步骤	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	恢复通道B校准 0x18000D		0x8C	
		0x18000E	0x05	
		0x18001D	0x31	
		0x18001E	0x04	
		0x18002D	0x30	
		0x18002E	0x01	
		0x18003D	0x9C	
		0x18003E	0x03	
2	禁用通道B反相	PCM路径信号控制2, 地址0x90004	数据 (0x90004) 与 (0xFB)	
		保留	0000	
		PCM_INV_A	x	
		PCM_INV_B	0	禁用通道B反相
		PCM_SWAP_CHAN	x	
		PCM_COPY_CHAN	x	

5.11 Sequences for Using the PCM Channel Swap Bit

The following subsections describe sequences for enabling and disabling the PCM_SWAP_CHAN bit.

5.11.1 Sequence for Enabling the PCM_SWAP_CHAN Bit

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Swap channel A/B calibration	0x180005	0x8C	
		0x180007	0xAB	
		0x180015	0x31	
		0x180017	0xB2	
		0x180025	0x30	
		0x180027	0x84	
		0x180035	0x9C	
		0x180037	0xAE	
		0x18000D	0x24	
		0x18000F	0xA3	
		0x18001D	0x05	
		0x18001F	0xD4	
		0x18002D	0x0B	
		0x18002F	0xC7	
		0x18003D	0x71	
		0x18003F	0xE7	
2	Enable PCM channel swap	PCM Path Signal Control 2. 0x90004	data (0x90004) OR (0x02)	
		Reserved	0000	
		PCM_INV_A	x	
		PCM_INV_B	x	
		PCM_SWAP_CHAN	1	Enable PCM channel swap
		PCM_COPY_CHAN	x	

5.11.2 Sequence for Disabling the PCM_SWAP_CHAN Bit

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Restore channel A/B calibration	0x180005	0x24	
		0x180007	0xA3	
		0x180015	0x05	
		0x180017	0xD4	
		0x180025	0x0B	
		0x180027	0xC7	
		0x180035	0x71	
		0x180037	0xE7	
		0x18000D	0x8C	
		0x18000F	0xAB	
		0x18001D	0x31	
		0x18001F	0xB2	
		0x18002D	0x30	
		0x18002F	0x84	
		0x18003D	0x9C	
		0x18003F	0xAE	
2	Disable PCM channel swap	PCM Path Signal Control 2. 0x90004	data (0x90004) AND (0xFD)	
		Reserved	0000	
		PCM_INV_A	x	
		PCM_INV_B	x	
		PCM_SWAP_CHAN	0	Disable PCM channel swap
		PCM_COPY_CHAN	x	

5.11 使用 PCM 通道交换位的顺序

以下小节描述启用和禁用 PCM_SWAP_CHAN 位的序列。

5.11.1 启用 PCM_SWAP_CHAN 位的序列

步骤	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1 交换通道 A/B 校准	0x180005		0x8C	
		0x180007	0xAB	
		0x180015	0x31	
		0x180017	0xB2	
		0x180025	0x30	
		0x180027	0x84	
		0x180035	0x9C	
		0x180037	0xAE	
		0x18000D	0x24	
		0x18000F	0xA3	
		0x18001D	0x05	
		0x18001F	0xD4	
		0x18002D	0x0B	
		0x18002F	0xC7	
		0x18003D	0x71	
		0x18003F	0xE7	
2 启用 PCM 通道交换		PCM路径信号控制2, 地址0x90004	数据 (0x90004) 或 (0x02)	
		保留	0000	
		PCM_INV_A	x	
		PCM_INV_B	x	
		PCM_SWAP_CHAN	1	启用 PCM 通道交换
		PCM_COPY_CHAN	x	

5.11.2 禁用 PCM_SWAP_CHAN 位的操作顺序

步骤	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1 恢复通道 A/B 校准	0x180005		0x24	
		0x180007	0xA3	
		0x180015	0x05	
		0x180017	0xD4	
		0x180025	0x0B	
		0x180027	0xC7	
		0x180035	0x71	
		0x180037	0xE7	
		0x18000D	0x8C	
		0x18000F	0xAB	
		0x18001D	0x31	
		0x18001F	0xB2	
		0x18002D	0x30	
		0x18002F	0x84	
		0x18003D	0x9C	
		0x18003F	0xAE	
2 禁用 PCM 通道交换		PCM路径信号控制2, 地址0x90004	数据 (0x90004) 与 (0xFD)	
		保留	0000	
		PCM_INV_A	x	
		PCM_INV_B	x	
		PCM_SWAP_CHAN	0	禁用 PCM 通道交换
		PCM_COPY_CHAN	x	

5.12 Sequences for Enabling and Disabling Mono Mode for PCM Playback

The following subsections describe sequences for enabling and disabling mono mode for PCM playback.

5.12.1 Sequence for Enabling Mono Mode for PCM Playback

STEP	TASK	REGISTER/BIT FIELDS	VALUE
1	Enable mono mode	0x180009	0x2F
		0x18000A	0xB4
		0x18000B	0x25
		0x18000C	0x80
		0x18000F	0x55
		0x180010	0xFA
		0x180019	0x2F
		0x18001A	0xB4
		0x18001B	0x25
		0x18001C	0x80
		0x18001F	0x4E
		0x180020	0xFD
		0x180029	0x2F
		0x18002A	0xB4
		0x18002B	0x25
		0x18002C	0x80
		0x18002F	0x7C
		0x180030	0xFD
		0x180039	0x2F
		0x18003A	0xB4
		0x18003B	0x25
		0x18003C	0x80
		0x18003F	0x52
		0x180040	0xFE

5.12.2 Sequence for Disabling Mono Mode for PCM Playback

STEP	TASK	REGISTER/BIT FIELDS	VALUE
1	Disable mono mode	0x180009	0xD1
		0x18000A	0x4B
		0x18000B	0xDA
		0x18000C	0x7F
		0x18000F	0xAB
		0x180010	0x05
		0x180019	0xD1
		0x18001A	0x4B
		0x18001B	0xDA
		0x18001C	0x7F
		0x18001F	0xB2
		0x180020	0x02
		0x180029	0xD1
		0x18002A	0x4B
		0x18002B	0xDA
		0x18002C	0x7F
		0x18002F	0x84
		0x180030	0x02
		0x180039	0xD1
		0x18003A	0x4B
		0x18003B	0xDA
		0x18003C	0x7F
		0x18003F	0xAE
		0x180040	0x01

5.12 启用和禁用 PCM 播放单声道模式的序列

以下小节描述了启用和禁用 PCM 播放单声道模式的操作序列。

5.12.1 启用 PCM 播放单声道模式的序列

步骤	TASK	REGISTER/BIT FIELDS	VALUE
1	启用单声道模式	0x180009	0x2F
		0x18000A	0xB4
		0x18000B	0x25
		0x18000C	0x80
		0x18000F	0x55
		0x180010	0xFA
		0x180019	0x2F
		0x18001A	0xB4
		0x18001B	0x25
		0x18001C	0x80
		0x18001F	0x4E
		0x180020	0xFD
		0x180029	0x2F
		0x18002A	0xB4
		0x18002B	0x25
		0x18002C	0x80
		0x18002F	0x7C
		0x180030	0xFD
		0x180039	0x2F
		0x18003A	0xB4
		0x18003B	0x25
		0x18003C	0x80
		0x18003F	0x52
		0x180040	0xFE

5.12.2 禁用 PCM 播放单声道模式的序列

步骤	TASK	REGISTER/BIT FIELDS	VALUE
1	禁用单声道模式	0x180009	0xD1
		0x18000A	0x4B
		0x18000B	0xDA
		0x18000C	0x7F
		0x18000F	0xAB
		0x180010	0x05
		0x180019	0xD1
		0x18001A	0x4B
		0x18001B	0xDA
		0x18001C	0x7F
		0x18001F	0xB2
		0x180020	0x02
		0x180029	0xD1
		0x18002A	0x4B
		0x18002B	0xDA
		0x18002C	0x7F
		0x18002F	0x84
		0x180030	0x02
		0x180039	0xD1
		0x18003A	0x4B
		0x18003B	0xDA
		0x18003C	0x7F
		0x18003F	0xAE
		0x180040	0x01

5.13 Example Sequences

This section provides recommended instruction sequences for standard CS43131 operations.

5.13.1 Power-up Sequence to I²S Playback

In Ex. 5-7, a 22.5792-MHz crystal is used, ASP is set to I²S master at 44.1 kHz, and full-scale output is 1.732 Vrms.

Example 5-7. Startup to I²S Playback

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Apply all relevant power supplies, then assert RESET.			
2	Wait for 1.5 ms.			
3	Configure XTAL driver			
4	Configure XTAL bias current strength (assuming River Crystal at 22.5792 MHz)	Crystal Setting. 0x20052 Reserved XTAL_IBIAS	0x04 0000 0 100	Bias current set to 12.5 μ A
5	Read Interrupt Status 1 register (0xF0000) to clear any pending interrupts.			
6	Enable XTAL interrupts	Interrupt Mask 1. 0xF0010 DAC_OVFL_INT_MASK HPDETECT_PLUG_INT_MASK HPDETECT_UNPLUG_INT_MASK XTAL_READY_INT_MASK XTAL_ERROR_INT_MASK PLL_READY_INT_MASK PLL_ERROR_INT_MASK PDN_DONE_INT_MASK	0xE7 1 1 1 0 0 1 1 1	Enable XTAL_READY interrupt Enable XTAL_ERROR interrupt
7	Start XTAL	Power Down Control. 0x20000 PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT Reserved	0xF6 1 1 1 1 0 1 1 0	Power up XTAL driver
8	Configure ASP interface. Sample rate set to 44.1 kHz. ASP is clock master.			
9	Set ASP sample rate	Serial Port Sample Rate. 0x1000B Reserved ASP_SPRATE	0x01 0000 0001	Set sample rate to 44.1 kHz
10	Set ASP sample bit size. XSP is don't care	Serial Port Sample Bit Size. 0x1000C Reserved XSP_SPSIZE ASP_SPSIZE	0x04 0000 01 00	XSP sample bit size set to 24 bits ASP sample bit size set to 32 bits
11	Set ASP numerator	ASP Numerator 1. 0x40010 ASP_N_LSB ASP Numerator 2. 0x40011 ASP_N_MSB	0x01 0x01 0x00 0x00	LSB of ASP sample rate fractional divide numerator MSB of ASP sample rate fractional divide numerator
12	Set ASP denominator	ASP Denominator 1. 0x40012 ASP_M_LSB ASP Denominator 2. 0x40013 ASP_M_MSB	0x08 0x08 0x00 0x00	LSB of ASP sample rate fractional divide denominator MSB of ASP sample rate fractional divide denominator
13	Set ASP LRCK high time	ASP_LRCK_High_Time 1. 0x40014 ASP_LCHI_LSB ASP_LRCK_High_Time 2. 0x40015 ASP_LCHI_MSB	0x1F 0x1F 0x00 0x00	LSB of ASP LRCK high time duration MSB of ASP LRCK high time duration
14	Set ASP LRCK period	ASP_LRCK_Period 1. 0x40016 ASP_LCPRLSB ASP_LRCK_Period 2. 0x40017 ASP_LCPR_MSB	0x3F 0x3F 0x00 0x00	LSB of ASP LRCK period MSB of ASP LRCK period
15	Configure ASP clock	ASP_Clock_Configuration. 0x40018 Reserved ASP_M/SB ASP_SCPOL_OUT ASP_SCPOL_IN ASP_LCPOL_OUT ASP_LCPOL_IN	0x1C 000 1 1 1 0 0	Set ASP port to be master Configure clock polarity for I ² S input

5.13 示例顺序

本节提供标准CS43131操作的推荐指令序列。

5.13.1 上电序列至I2S播放

在示例5-7中，使用22.5792 MHz晶体，ASP设置为44.1 kHz的I2S主模式，满量程输出为1.732 Vrms。

示例5-7。启动至I2S播放

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	施加所有相关电源，然后断言复位。			
2	等待1.5毫秒。			
3	配置晶体振荡器驱动			
4	配置晶体振荡器偏置 电流强度（假设River Crystal频率为22.5792 MHz）	晶体设置。0x20052 保留 晶体振荡器偏置电流	0x04 0000 0 100 偏置电流设置为12.5 μA	
5	读取中断状态1寄存器（0xF0000）以清除所有待处理中断。			
6	启用晶体振荡器中断屏蔽1。0xF0010	DAC_OVFL_INT_MASK HPDETECT_PLUG_INT_MASK HPDETECT_UNPLUG_INT_MASK XTAL_READY_INT_MASK XTAL_ERROR_INT_MASK PLL_READY_INT_MASK PLL_ERROR_INT_MASK PDN_DONE_INT_MASK	0xE7 1 1 1 0 0 1 1 1	启用晶体振荡器就绪中断 启用晶体振荡器错误中断
7	启动晶体振荡器	关断控制，0x20000 PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT 保留	0xF6 1 1 1 1 0 1 1 0	
8	配置ASP接口。采样率设置为44.1 kHz，ASP为时钟主控。			
9	设置ASP采样率串行端口采样率。0x1000B	保留 ASP采样率	0x01 0000 0001	设置采样率为44.1 kHz
10	设置ASP采样位宽。 XSP为无关项	串行端口采样位宽。0x1000C 保留 XSP_SPSIZE ASP_SPSIZE	0x04 0000 01 00	XSP 采样位宽设置为 24 位 ASP 采样位宽设置为 32 位
11	设置 ASP 分子	ASP 分子 1, 地址 0x40010 ASP_N_LSB ASP 分子 2, 地址 0x40011 ASP_N_MSB	0x01 0x01 0x00 0x00	ASP 采样率分数除法分子最低有效位 ASP 采样率分数除法分子最高有效位
12	设置 ASP 分母ASP 分母 1, 地址 0x40012	ASP_M_LSB ASP 分母 2, 地址 0x40013 ASP_M_MSB	0x08 0x08 0x00 0x00	ASP 采样率分数除法分母最低有效位 ASP 采样率分数除法分母最高有效位
13	设置 ASP LRCK 高电平时间	ASP_LRCK 高电平时间 1, 地址 0x40014 ASP_LCHI_LSB ASP_LRCK 高电平时间 2, 地址 0x40015 ASP_LCHI_MSB	0x1F 0x1F 0x00 0x00	ASP_LRCK 高电平时间持续时长最低有效位 ASP_LRCK 高电平时间持续时长最高有效位
14	设置 ASP LRCK 周期	ASP_LRCK 周期 1.0x40016 ASP_LCPRI_LSB ASP_LRCK 周期 2.0x40017 ASP_LCPRI_MSB	0x3F 0x3F 0x00 0x00	ASP_LRCK 周期的最低有效位 ASP_LRCK 周期的最高有效位
15	配置 ASP 时钟 ASP 时钟配置。	0x40018 保留 M/SB_AS P_SCPOL_OUT_A SP_SCPOL_IN AS_P_LCPOL_OUT AS_P_LCPOL_IN	0x1C 000 1 1 1 0 0	设置 ASP 端口为主设备 配置 I2S 输入的时钟极性

Example 5-7. Startup to I2S Playback (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
16	Configure ASP frame	ASP Frame Configuration. 0x40019	0x0A	
		Reserved	000	Configure ASP port to accept I2S input
		ASP_STP	0	
		ASP_5050	1	
		ASP_FSD	010	
17	Set ASP channel location	ASP Channel 1 Location. 0x50000	0x00	
		ASP_RX_CH1	0x00	ASP Channel 1 starts on SCLK0
		ASP Channel 2 Location. 0x50001	0x00	
		ASP_RX_CH2	0x00	ASP Channel 2 starts on SCLK0
18	Set ASP channel size and enable	ASP Channel 1 Size and Enable. 0x5000A	0x07	
		Reserved	0000	
		ASP_RX_CH1_AP	0	ASP Channel 1 Active Phase
		ASP_RX_CH1_EN	1	ASP Channel 1 Enable
		ASP_RX_CH1_RES	11	ASP Channel 1 Size is 32 bits
		ASP Channel 2 Size and Enable. 0x5000B	0xF	
		Reserved	0000	
		ASP_RX_CH2_AP	1	ASP Channel 2 Active Phase
		ASP_RX_CH2_EN	1	ASP Channel 2 Enable
		ASP_RX_CH2_RES	11	ASP Channel 2 Size is 32 bits
19	Configure PCM interface. HPF filter is used. Deemphasis off.			
20	Configure PCM filter	PCM Filter Option. 0x90000	0x02	
		FILTER_SLOW_FASTB	0	
		PHCOMP_LOWLATB	0	
		NOS	0	
		Reserved	00	
		PCM_WBF_EN	0	
		HIGH_PASS	1	High pass filter is selected
		DEEMP_ON	0	
21	Set volume for channel B	PCM Volume B. 0x90001	0x00	
		PCM_VOLUME_B	0x00	Set volume to 0 dB
22	Set volume for channel A	PCM Volume A. 0x90002	0x00	
		PCM_VOLUME_A	0x00	Set volume to 0 dB
23	Configure PCM path signal control	PCM Path Signal Control 1. 0x90003	0xEC	
		PCM_RAMP_DOWN	1	Soft ramp down of volume on filter change
		PCM_VOL_BEQA	1	Volume setting on both channels controlled by PCM_VOLUME_A
		PCM_SZC	10	Enable soft ramp
		PCM_AMUTE	1	Mute after reception of 8192 samples of 0 or -1.
		PCM_AMUTEBEQA	1	Mute only when AMUTE condition is detected on both channels
		PCM_MUTE_A	0	Function is disabled
		PCM_MUTE_B	0	Function is disabled
		PCM Path Signal Control 2. 0x90004	0x00	
		Reserved	0000	
		PCM_INV_A	0	Disable all functions in this register
		PCM_INV_B	0	
		PCM_SWAP_CHAN	0	
		PCM_COPY_CHAN	0	
24	Configure HP			
25	Configure Class H amplifier	Class H Control. 0xB0000	0x1E	
		Reserved	000	
		ADPT_PWR	1 11	Output signal determines voltage level
		HV_EN	1	High voltage mode enabled
		EXT_VCPFILT	0	Using internal VCPFILT source.
26	Set HP output to full scale	HP Output Control 1. 0x80000	0x30	
		HP_CLAMPA	0	
		HP_CLAMPB	0	
		OUT_FS	11	Set headphone output to full scale (1.732 V rms)
		HP_IN_EN	0	
		HP_IN_LP	0	
		Reserved	0	
		+1dB_EN	0	
27	Configure Headphone detect	HP Detect. 0xD0000	0x04	
		HPDETECT_CTRL	00	HP detect disabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	0 0	Tip sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	

示例5-7。启动至 I²S 播放（连续）

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
16	配置 ASP 帧 ASP 帧配置。0x40019		0x0A	
	保留		000	配置 ASP 端口以接收 I ² S 输入
	ASP_STP		0	
	ASP_5050		1	
	ASP_FSD		010	
17	设置 ASP 通道位置 ASP 通道 1 位置。0x50000		0x00	
	ASP_RX_CH1		0x00	ASP 通道 1 从 SCLK0 开始
	ASP 通道 2 位置。0x50001		0x00	
	ASP_RX_CH2		0x00	ASP 通道 2 从 SCLK0 开始
18	设置 ASP 通道大小及启用，地址 0x5000A		0x07	
	保留		0000	
	ASP_RX_CH1_AP		0	ASP 通道 1 有效相位
	ASP_RX_CH1_EN		1	启用 ASP 通道 1
	ASP_RX_CH1_RES		11	ASP 通道 1 大小为 32 位
	ASP 通道 2 大小及启用，地址 0x5000B		0xF	
	保留		0000	
	ASP_RX_CH2_AP		1	ASP 通道 2 有效相位
	ASP_RX_CH2_EN		1	启用 ASP 通道 2
	ASP_RX_CH2_RES		11	ASP 通道 2 大小为 32 位
19	配置 PCM 接口，使用高通滤波器，取消预加重			
20	配置 PCM 滤波器	PCM 滤波器选项。0x90000	0x02	
	FILTER_SLOW_FASTB		0	
	PHCOMP_LOWLATB		0	
	NOS		0	
	保留		00	
	PCM_WBF_EN		0	
	HIGH_PASS		1	选择高通滤波器
	DEEMP_ON		0	
21	设置通道 B 音量，PCM 音量 B，地址 0x90001		0x00	
	PCM_VOLUME_B		0x00	设置音量为 0 dB
22	设置通道 A 的音量 PCM Volume A。0x90002		0x00	
	PCM_VOLUME_A		0x00	设置音量为 0 dB
23	控制配置 PCM 路径信号	PCM 路径信号控制1，0x90003	0xEC	
	PCM_RAMP_DOWN		1	滤波器切换时音量软降
	PCM_VOL_BEQA		1	两个通道的音量设置由 PCM_VOLUME_A 控制
	PCM_SZC		10	启用软斜坡
	PCM_AMUTE		1	接收 8192 个值为 0 或 -1 的样本后静音
	PCM_AMUTEBEQA		1	仅当两个通道均检测到 AMUTE 条件时静音
	PCM_MUTE_A		0	功能已禁用
	PCM_MUTE_B		0	功能已禁用
	PCM 路径信号控制2，地址0x90004		0x00	
	保留		0000	
	PCM_INV_A		0	禁用此寄存器中的所有功能
	PCM_INV_B		0	
	PCM_SWAP_CHAN		0	
	PCM_COPY_CHAN		0	
24	配置耳机			
25	配置 Class H 放大器 Class H 控制。0xB0000		0x1E	
	保留		000	
	ADPT_PWR		1 1 1	输出信号决定电压等级
	HV_EN		1	高电压模式已启用
	EXT_VCPFILT		0	使用内部 VCPFILT 源。
26	将耳机输出设置为满量程耳机输出控制 1，0x80000		0x30	
	HP_CLAMPA		0	
	HP_CLAMPB		0	
	OUT_FS		11	将耳机输出设置为满量程 (1.732 V rms)
	HP_IN_EN		0	
	HP_IN_LP		0	
	保留		0	
	+1dB_EN		0	
27	配置耳机检测	耳机检测，0xD0000	0x04	
	HPDETECT_CTRL		00	耳机检测已禁用
	HPDETECT_IN		0	耳机检测输入未反相
	V_HPDetect_RISE_DBC_TI		0 0	Tip 感应上升消抖时间设置为 0 毫秒
	ME_HPDetect_FALL_DBC_T		10	Tip 感应下降消抖时间设置为 500 毫秒
	IME 保留		0	

Example 5-7. Startup to I²S Playback (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
28	Headphone detect	HP Detect. 0xD0000	0xC4	
		HPDETECT_CTRL	11	HP detect enabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	0 0	Tip sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
29	Enable interrupts			
30	Read Interrupt Status 1 register (0xF0000) and Interrupt Status 2 register (0xF0001) to clear sticky bits.			
31	Enable headphone detect interrupts	Interrupt Mask 1. 0xF0010	0x87	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	0	Enable HPDETECT_PLUG interrupt
		HPDETECT_UNPLUG_INT_MASK	0	Enable HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	0	
		XTAL_ERROR_INT_MASK	0	
		PLL_READY_INT_MASK	1	
		PLL_ERROR_INT_MASK	1	
		PDN_DONE_INT_MASK	1	
32	Enable ASP interrupts	Interrupt Mask 2. 0xF0011	0x07	
		ASP_OVFL_INT_MASK	0	Enable ASP_OVFL interrupt
		ASP_ERROR_INT_MASK	0	Enable ASP_ERROR interrupt
		ASP_LATE_INT_MASK	0	Enable ASP_LATE interrupt
		ASP_EARLY_INT_MASK	0	Enable ASP_EARLY interrupt
		ASP_NOLRCK_INT_MASK	0	Enable ASP_NOLRCK interrupt
		Reserved	111	
33	Wait for interrupt. Check if XTAL_READY_INT = 1 in Interrupt Status 1 register (0xF0000).			
34	Switch MCLK source to XTAL	System Clocking Control 1. 0x10006	0x04	
		Reserved	0000 0	MCLK Source set to XTAL. MCLK_INT frequency set to
		MCLK_INT	1	22.5792 MHz
		MCLK_SRC_SEL	00	
35	Wait at least 150 µs.			
36	Enable ASP clocks	Pad Interface Configuration. 0x1000D	0x02	
		Reserved	0000 00	
		XSP_3ST	1	XSP Interface status is don't care (set to default)
		ASP_3ST	0	Enable serial clocks in Master Mode
37	Power up HP	Refer to Ex. 5-5 for PCM power-up sequence		

5.13.2 Power-Up Sequence to DSD Playback

In [Ex. 5-8](#), a 22.5792-MHz crystal is used, the PLL is used to create a 24.576-MHz MCLK, XSP is set as DSD slave at 2.8224 MHz, and full-scale output is 1.732 Vrms.

Example 5-8. Startup to DSD Playback

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Apply all relevant power supplies, then assert RESET.			
2	Wait for 1.5 ms.			
3	Configure XTAL driver			
4	Configure XTAL bias current strength (assuming River Crystal at 22.5792 MHz)	Crystal Setting. 0x20052	0x04	
		Reserved	0000 0	
		XTAL_IBIAS	100	Bias current set to 12.5 µA
5	Read Interrupt Status 1 register (0xF0000) to clear any pending interrupts.			
6	Enable XTAL interrupts	Interrupt Mask 1. 0xF0010	0xE7	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	1	
		HPDETECT_UNPLUG_INT_MASK	1	
		XTAL_READY_INT_MASK	0	Enable XTAL_READY interrupt
		XTAL_ERROR_INT_MASK	0	Enable XTAL_ERROR interrupt
		PLL_READY_INT_MASK	1	
		PLL_ERROR_INT_MASK	1	
		PDN_DONE_INT_MASK	1	
7	Start XTAL	Power Down Control. 0x20000	0xF6	
		PDN_XSP	1	
		PDN_ASP	1	
		PDN_DSDIF	1	
		PDN_HP	1	
		PDN_XTAL	0	Power up XTAL driver
		PDN_PLL	1	
		PDN_CLKOUT	1	
		Reserved	0	

示例5-7。启动至I2S播放（连续）

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
28	耳机检测	耳机检测, 0xD0000	0xC4	
		HPDETECT_CTRL	11	启用耳机检测
		HPDETECT_IN	0	耳机检测输入未反相
		V HPDETECT_RISE_DBC_TI	0 0	Tip 感应上升消抖时间设置为 0 毫秒
		ME HPDETECT_FALL_DBC_T	10	Tip 感应下降消抖时间设置为 500 毫秒
		IME 保留	0	
29	启用中断			
30	读取中断状态寄存器1 (0xF0000) 和中断状态寄存器2 (0xF0001) 以清除粘滞位。			
31	中断启用耳机检测	中断屏蔽 1, 0xF0010	0x87	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	0	启用HPDETECT_PLUG中断
		HPDETECT_UNPLUG_INT_MASK	0	启用HPDETECT_UNPLUG中断
		XTAL_READY_INT_MASK	0	
		XTAL_ERROR_INT_MASK	0	
		PLL_READY_INT_MASK	1	
		PLL_ERROR_INT_MASK	1	
		PDN_DONE_INT_MASK	1	
32	启用ASP中断中断掩码2, 地址0xF0011		0x07	
		ASP_OVFL_INT_MASK	0	启用ASP_OVFL中断
		ASP_ERROR_INT_MASK	0	启用ASP_ERROR中断
		K ASP_LATE_INT_MASK	0	启用ASP_LATE中断
		SK ASP_EARLY_INT_MASK	0	启用ASP_EARLY中断
		ASK ASP_NOLRCK_INT_MASK	0	启用ASP_NOLRCK中断
		保留	111	
33	等待中断。检查中断状态寄存器1 (0xF0000) 中XTAL_READY_INT位是否为1。			
34	切换MCLK时钟源至XTAL	系统时钟控制寄存器1, 地址0x10006	0x04	
		保留	0000 0	MCLK源设置为晶体振荡器。MCLK_INT频率设置为22
		MCLK_INT	1	.5792 MHz。
		MCLK_SRC_SEL	00	
35	等待至少150 μs。			
36	启用ASP时钟。	引脚接口配置。0x1000D	0x02	
		保留	0000 00	
		XSP_3ST	1	XSP接口状态为无关 (设置为默认值)
		ASP_3ST	0	主模式下启用串行时钟。
37	耳机供电开启	参见示例5-5的PCM上电顺序。		

5.13.2 上电序列至 DSD 播放

在示例 5-8 中, 使用 22.5792 MHz 晶体, PLL 用于生成 24.576 MHz MCLK, XSP 设置为 2.8224 MHz 的 DSD 从机, 满量程输出为 1.732 Vrms。

示例5-8。启动至DSD播放。

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	施加所有相关电源, 然后断言复位。			
2	等待1.5 ms。			
3	配置晶体振荡器驱动。			
4	配置晶体振荡器偏置电流强度 (假设River Crystal为22.5792 MHz)。	晶体设置。0x20052	0x04	
		保留	0000 0	
		晶体振荡器偏置电流	100	偏置电流设置为 12.5 μA。
5	读取中断状态1寄存器 (0xF0000) 以清除所有待处理中断。			
6	启用晶体振荡器中断。	中断屏蔽 1, 0xF0010	0xE7	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	1	
		HPDETECT_UNPLUG_INT_MASK	1	
		XTAL_READY_INT_MASK	0	启用晶体振荡器就绪中断
		XTAL_ERROR_INT_MASK	0	启用晶体振荡器错误中断
		PLL_READY_INT_MASK	1	
		PLL_ERROR_INT_MASK	1	
		PDN_DONE_INT_MASK	1	
7	启动晶体振荡器	关断控制, 0x20000	0xF6	
		PDN_XSP	1	
		PDN_ASP	1	
		PDN_DSDIF	1	
		PDN_HP	1	
		PDN_XTAL	0	晶体振荡器驱动器上电
		PDN_PLL	1	
		PDN_CLKOUT	1	
		保留	0	

Example 5-8. Startup to DSD Playback (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
8	Configure PLL. Input is 22.5792 MHz. Output is 24.576 MHz.			
9	Power up PLL	Power Down Control. 0x20000	0xF2	
		PDN_XSP	1	
		PDN_ASP	1	
		PDN_DSDIF	1	
		PDN_HP	1	
		PDN_XTAL	0	
		PDN_PLL	0	Power up PLL
		PDN_CLKOUT	1	
		Reserved	0	
10	Set PLL predivide	PLL Setting 9. 0x40002	0x03	
		Reserved	0000 00	
		PLL_REF_PREDIV	11	Divide PLL Reference by 8
11	Set PLL Output Divide	PLL Setting 6. 0x30008	0x08	
		PLL_OUT_DIV	0x08	Divide PLL output by 8
12	Set Fractional portion of PLL divide ratio	PLL Setting 2. 0x30002	0x00	
		PLL_DIV_FRAC_0	0x00	
		PLL Setting 3. 0x30003	0xF7	
		PLL_DIV_FRAC_1	0xF7	
		PLL Setting 4. 0x30004	0x06	
		PLL_DIV_FRAC_2	0x06	
13	Set integer portion of PLL divide ratio	PLL Setting 5. 0x30005	0x44	
		PLL_DIV_INT	0x44	
14	Set PLL Mode	PLL Setting 8. 0x3001B	0x01	
		Reserved	0000 00	
		PLL_MODE	0	Use 500/512 factor
		Reserved	1	
15	Set PLL Calibration Ratio	PLL Setting 7. 0x3000A	0x8B	
		PLL_CAL_RATIO	0x8B	Set PLL Cal Ratio to 139
16	Read Interrupt Status 1 register (0xF0000) to clear any pending interrupts.			
17	Enable PLL Interrupts	Interrupt Mask 1. 0xF0010	0xE1	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	1	
		HPDETECT_UNPLUG_INT_MASK	1	Enable PLL Ready and Error Interrupts
		XTAL_READY_INT_MASK	0	
		XTAL_ERROR_INT_MASK	0	
		PLL_READY_INT_MASK	0	
		PLL_ERROR_INT_MASK	0	
		PDN_DONE_INT_MASK	1	
18	Start PLL	PLL Setting 1. 0x30001	0x01	
		Reserved	0000 000	
		PLL_START	1	Start PLL
19	Configure DSDIF to playback 64•Fs DSD stream. DSDIF is configured as Slave			
20	Configure DSD Volume	DSD Volume A. 0x70001	0x00	
		DSD_VOLUME_A	0x00	Channel A volume set to 0dB
21	Configure DSD path Signal Control1	DSD Processor Path Signal Control 1. 0x70002	0xCC	
		DSD_RAMP_UP	1	
		DSD_VOL_BEQA	1	DSD Volume B equals DSD volume A
		DSD_SZC	0	Immediate change
		Reserved	0	
		DSD_AMUTE	1	Mute occurs after 256 repeated 8-bit DSD mute patterns
		DSD_AMUTE_BEQA	1	Mute happens only when mute pattern is detected in both channels
		DSD_MUTE_A	0	Function is disabled
		DSD_MUTE_B	0	Function is disabled
22	Configure DSD Interface	DSD Interface Configuration. 0x70003	0x00	
		Reserved	0000 0	
		DSD_M/SB	0	DSD is clock slave
		DSD_PM_EN	0	Function is disabled
		DSD_PM_SEL	0	Function is disabled

示例5-8。启动至DSD播放 (续)

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
8	配置PLL。输入为22.5792 MHz, 输出为24.576 MHz。			
9	PLL上电。	关断控制, 0x20000	0xF2	
		PDN_XSP	1	
		PDN_ASP	1	
		PDN_DSDIF	1	
		PDN_HP	1	
		PDN_XTAL	0	
		PDN_PLL	0	PLL上电。
		PDN_CLKOUT	1	
		保留	0	
10	设置 PLL 预分频	PLL 设置 9, 0x40002	0x03	
		保留	0000 00	
		PLL_REF_PREDIV	11	PLL 参考信号分频除以 8
11	设置 PLL 输出分频	PLL 设置 6, 0x30008	0x08	
		PLL_OUT_DIV	0x08	PLL 输出分频除以 8
12	设置 PLL 分频比的小数部分	PLL 设置 2, 0x30002	0x00	
		PLL_DIV_FRAC_0	0x00	
		PLL 设置 3, 0x30003	0xF7	
		PLL_DIV_FRAC_1	0xF7	
		PLL 设置 4, 0x30004	0x06	
		PLL_DIV_FRAC_2	0x06	
13	设置PLL分频比的整数部分	PLL 设置 5, 0x30005	0x44	
		PLL_DIV_INT	0x44	
14	设置 PLL 模式	PLL 设置 8, 0x3001B	0x01	
		保留	0000 00	
		PLL_MODE	0	使用 500/512 因子
		保留	1	
15	设置 PLL 校准比率	PLL 设置 7, 0x3000A	0x8B	
		PLL_CAL_RATIO	0x8B	设置 PLL 校准比率为 139
16	读取中断状态1寄存器 (0xF0000) 以清除所有待处理中断。			
17	启用 PLL 中断	中断屏蔽 1, 0xF0010	0xE1	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	1	
		HPDETECT_UNPLUG_INT_MASK	1	启用 PLL 就绪和错误中断
		XTAL_READY_INT_MASK	0	
		XTAL_ERROR_INT_MASK	0	
		PLL_READY_INT_MASK	0	
		PLL_ERROR_INT_MASK	0	
		PDN_DONE_INT_MASK	1	
18	启动 PLL	PLL 设置 1, 0x30001	0x01	
		保留	0000 000	
		PLL_START	1	启动 PLL
19	配置 DSDIF 以播放 64·Fs DSD 流	DSDIF 配置为从属模式		
20	配置 DSD 音量	DSD 音量 A, 0x70001	0x00	
		DSD_VOLUME_A	0x00	通道 A 音量设置为 0dB
21	配置 DSD 路径信号控制1	DSD处理器路径信号控制1 0x70002	0xCC	
		DSD_RAMP_UP	1	
		DSD_VOL_BEQA	1	DSD音量B等于DSD音量A
		DSD_SZC	0	立即更改
		保留	0	
		DSD_AMUTE	1	静音在256次重复的8位DSD静音模式后发生
		DSD_AMUTE_BEQA	1	仅当两个通道均检测到静音模式时才触发静音
		DSD静音A	0	功能已禁用
		DSD静音B	0	功能已禁用
22	配置DSD接口	DSD接口配置。0x70003 0x00 保留 DSD_M/S		
		B_DSD_P	0000 0	
		M_EN_DSD	0	DSD为时钟从属
		_PM_SEL	0	功能已禁用
		保留	0	功能已禁用

Example 5-8. Startup to DSD Playback (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
23	Configure DSD path Signal Control 2	DSD Processor Path Signal Control 2. 0x70004	0x13	
		Reserved	0	
		DSD_PRC_SRC	00	Set source of DSD processor to DSDIF
		DSD_EN	1	Enable DSD playback
		Reserved	0	
		DSD_SPEED	0	Set DSD clock speed to 64•FS
		STA_DSD_DET	1	Static DSD detection enabled
		INV_DSD_DET	1	Invalid DSD detection enabled
24	Configure HP			
25	Configure Class H Amplifier	Class H Control. 0xB0000	0x1E	
		Reserved	000	
		ADPT_PWR	111	Output signal determines voltage level
		HV_EN	1	High Voltage Mode Enabled
		EXT_VCPFILT	0	Using Internal VCPFILT source.
26	Set HP output to full scale	HP Output Control 1. 0x80000	0x30	
		HP_CLAMPA	0	
		HP_CLAMPB	0	
		OUT_FS	11	Set headphone output to Full Scale (1.732 V rms)
		HP_IN_EN	0	
		HP_IN_LP	0	
		Reserved	0	
		+1dB_EN	0	
27	Configure Headphone Detect	HP Detect. 0xD0000	0x04	
		HPDETECT_CTRL	00	HP detect disabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	0 0	Tip Sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
28	Headphone Detect	HP Detect. 0xD0004	0xC4	
		HPDETECT_CTRL	11	HP detect enabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	0 0	Tip sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
29	Enable Interrupts			
30	Read Interrupt Status 1 register (0xF0000) and Interrupt Status 5 register (0xF0004) to clear sticky bits			
31	Enable Headphone Detect Interrupts	Interrupt Mask 1. 0xF0010	0x81	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	0	Unmask HPDETECT_PLUG interrupt and
		HPDETECT_UNPLUG_INT_MASK	0	HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	0	
		XTAL_ERROR_INT_MASK	0	
		PLL_READY_INT_MASK	0	
		PLL_ERROR_INT_MASK	0	
		PDN_DONE_INT_MASK	1	
32	Enable DSD Interrupts	Interrupt Mask 5. 0xF0014	0x03	
		DSD_STUCK_INT_MASK	0	Enable DSD_STUCK interrupt
		DSD_INVAL_A_INT_MASK	0	Enable DSD_INVAL_A interrupt
		DSD_INVAL_B_INT_MASK	0	Enable DSD_INVAL_B interrupt
		DSD_SILENCE_A_INT_MASK	0	Enable DSD_SILENCE_A interrupt
		DSD_SILENCE_B_INT_MASK	0	Enable DSD_SILENCE_B interrupt
		DSD_RATE_ERROR_INT_MASK	0	Enable DSD_RATE_ERROR interrupt
		DOP_MRK_DET_INT_MASK	1	Disable DOP_MRK_DET interrupt
		DOP_ON_INT_MASK	1	Disable DOP_ON interrupt
33	Wait for interrupt. Check if PLL_READY_INT = 1 in Interrupt Status 1 register(0xF0000)			
34	Switch MCLK source to PLL	System Clocking Control 1. 0x10006	0x01	
		Reserved	0000 0	
		MCLK_INT	0	MCLK Source set to PLL. MCLK_INT frequency set to
		MCLK_SRC_SEL	01	24.576 MHz
35	Wait at least 150 µs.			
36	Power up HP	Refer to Ex. 5-6 for DSD power-up sequence. Note that in Step 1 of Ex. 5-6 , use HH = DF for the DSD interface.		

示例5-8。启动至DSD播放 (续)

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
23	配置DSD路径信号控制。 2	0x7004 DSD处理路径信号控制2。	0x13	
		保留	0	
		DSD_PRC_SRC	00	将DSD处理器源设置为DSDIF
		DSD_EN	1	启用DSD播放
		保留	0	
		DSD_SPEED	0	将DSD时钟速度设置为64•FS
		STA_DSD_DET	1	启用静态DSD检测
		INV_DSD_DET	1	启用无效DSD检测
24	配置耳机			
25	配置Class H放大器Class H控制。	0xB0000	0x1E	
		保留	000	
		ADPT_PWR	111	输出信号决定电压等级
		HV_EN	1	启用高压模式
		EXT_VCPFILT	0	使用内部VCPFILT源
26	将耳机输出设置为满量程	耳机输出控制 1, 0x80000	0x30	
		HP_CLAMPA	0	
		HP_CLAMPB	0	
		OUT_FS	11	将耳机输出设置为满量程 (1.732 V rms)
		HP_IN_EN	0	
		HP_IN_LP	0	
		保留	0	
		+1dB_EN	0	
27	配置耳机检测耳机检测。	0xD0000	0x04	
		HPDETECT_CTRL	00	耳机检测已禁用
		HPDETECT_IN	0	耳机检测输入未反相
		V_HPDetect_RISE_DBC_TI	0.0	Tip Sense上升消抖时间设置为0毫秒
		ME_HPDetect_Fall_DBC_T	10	Tip 感应下降消抖时间设置为 500 毫秒
		IME 保留	0	
28	耳机检测	耳机检测, 0xD0000	0xC4	
		HPDETECT_CTRL	11	启用耳机检测
		HPDETECT_IN	0	耳机检测输入未反相
		V_HPDetect_RISE_DBC_TI	0.0	Tip 感应上升消抖时间设置为 0 毫秒
		ME_HPDetect_Fall_DBC_T	10	Tip 感应下降消抖时间设置为 500 毫秒
		IME 保留	0	
29	启用中断			
30	读取中断状态1寄存器 (0xF0000) 和中断状态5寄存器 (0xF0004) 以清除粘滞位			
31	启用耳机检测 中断	中断屏蔽 1, 0xF0010	0x81	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	0	取消屏蔽HPDETECT_PLUG中断和HPDETECT_UNPLUG中断
		HPDETECT_UNPLUG_INT_MASK	0	
		XTAL_READY_INT_MASK	0	
		XTAL_ERROR_INT_MASK	0	
		PLL_READY_INT_MASK	0	
		PLL_ERROR_INT_MASK	0	
		PDN_DONE_INT_MASK	1	
32	启用DSD中断	中断屏蔽5, 0xF0014	0x03	
		DSD_STUCK_INT_MASK	0	启用DSD_STUCK中断
		DSD_INVAL_A_INT_MASK	0	使能 DSD_INVAL_A 中断
		DSD_INVAL_B_INT_MASK	0	使能 DSD_INVAL_B 中断
		DSD_SILENCE_A_INT_MASK	0	使能 DSD_SILENCE_A 中断
		DSD_SILENCE_B_INT_MASK	0	使能 DSD_SILENCE_B 中断
		DSD_RATE_ERROR_INT_MASK	0	使能 DSD_RATE_ERROR 中断
		DOP_MRK_DET_INT_MASK	1	禁用 DOP_MRK_DET 中断
		DOP_ON_INT_MASK	1	禁用 DOP_ON 中断
33	等待中断。检查中断状态寄存器 1 (0xF0000) 中 PLL_READY_INT 是否为 1			
34	切换 MCLK 源至 PLL 系统时钟控制 1, 地址 0x10006, 值 0x01		0000 0	
		MCLK_INT	010	MCLK 源设置为 PLL, MCLK_INT 频率设置为 24.576 MHz
		MCLK_SRC_SEL		
35	等待至少150 μs。			
36	耳机供电开启	有关 DSD 上电顺序, 请参见示例 5-6。注意, 在示例 5-6 的步骤 1 中, DSD 接口使用 HH = DF。		

5.13.3 Power-Up Sequence to DoP Playback with PLL

In Ex. 5-9, an external 19.2-MHz MCLK is used with a PLL to generate an internal MCLK or 22.5792 MHz, and the ASP is in clock master receiving DoP data with LRCLK at 176.4 kHz and SCLK at 8.4672 MHz.

Example 5-9. DoP Playback with PLL

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Apply all relevant power supplies, then assert RESET.			
2	Wait for 1.5 ms.			
3	Configure PLL. XTI/MCLK input coming from an external 19.2 MHz source with PLL output set to 22.5792 MHz. Refer to Section 4.7.2 for register settings for other frequency combinations			
4	Power up PLL	Power Down Control. 0x20000	0xFA	
		PDN_XSP	x	
		PDN_ASP	x	
		PDN_DSDIF	x	
		PDN_HP	x	
		PDN_XTAL	x	
		PDN_PLL	0	Power up PLL block
		PDN_CLKOUT	x	
		Reserved	0	
5	Set PLL Predivide value	PLL Setting 9. 0x40002	0x03	
		Reserved	0000 00	
		PLL_REF_PREDIV	11	Set PLL predivide value to 8
6	Set PLL output divide	PLL Setting 6. 0x30008	0x08	
		PLL_OUT_DIV	0x08	Set PLL output divide value to 8
7	Set Fractional portion of PLL Divide Ratio	PLL Setting 2. 0x30002	0x00	
		PLL_DIV_FRAC_0	0x00	Set LSB of PLL fractional divider value to 0
		PLL Setting 3. 0x30003	0x00	
		PLL_DIV_FRAC_1	0x00	Set Middle Byte of PLL fractional divider value to 0
		PLL Setting 4. 0x30004	0x80	
		PLL_DIV_FRAC_2	0x80	Set MSB of PLL fractional divider value to 0x80
8	Set Integer portion of PLL Divide Ratio	PLL Setting 5. 0x30005	0x49	
		PLL_DIV_INT	0x49	Set PLL integer Divide value to 0x49
9	Set PLL mode	PLL Setting 8. 0x3001B	0x01	
		Reserved	0000 00	
		PLL_MODE	0	500/512 factor is used in PLL frequency calculation
		Reserved	1	
10	Read Interrupt Status 1 register (0xF0000) to clear sticky bits.			
11	Set PLL calibration ratio	PLL Setting 7. 0x3000A	0x97	
		PLL_CAL_RATIO	0x97	PLL Calibration Ratio is set to 0x97 (151)
12	Enable PLL interrupts	Interrupt Mask 1. 0xF0010	0xF9	
		DAC_OVFL_INT_MASK	1	DAC_OVFL_INT is don't care
		HPDETECT_PLUG_INT_MASK	1	Unmask HPDETECT_PLUG interrupt
		HPDETECT_UNPLUG_INT_MASK	1	Unmask HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	1	XTAL_READY_INT is Don't Care
		XTAL_ERROR_INT_MASK	1	XTAL_ERROR_INT is Don't Care
		PLL_READY_INT_MASK	0	PLL_READY_INTERRUPT is already unmasked
		PLL_ERROR_INT_MASK	0	PLL_ERROR_INTERRUPT is already unmasked
		PDN_DONE_INT_MASK	1	PDN_DONE_INT is Don't Care
13	Start PLL	PLL Setting 1. 0x30001	0x01	
		Reserved	0000 000	
		PLL_START	1	Enable PLL Output
14	Playback DoP audio. Assuming 64*Fs DSD stream			
15	Configure ASP interface for DoP input			
16	Set ASP sample rate	Serial Port Sample Rate. 0x1000B	0x05	
		Reserved	0000	
		ASP_SPRATE	0101	Set sample rate to 176.4 kHz
17	Set ASP sample bit size. XSP is don't care	Serial Port Sample Bit Size. 0x1000C	0x05	
		Reserved	0000	
		XSP_SPSIZE	01	XSP sample bit size set to 24 bits
		ASP_SPSIZE	01	ASP sample bit size set to 24 bits
18	Set ASP numerator	ASP Numerator 1. 0x40010	0x03	
		ASP_N_LSB	0x03	LSB of ASP sample rate fractional divide numerator
		ASP Numerator 2. 0x40011	0x00	
		ASP_N_MSB	0x00	MSB of ASP sample rate fractional divide numerator

5.13.3 使用 PLL 进行 DoP 播放的上电顺序

在示例 5-9 中，外部 19.2 MHz MCLK 与 PLL 配合使用，生成内部 MCLK 或 22.5792 MHz，ASP 作为时钟主设备接收 DoP 数据，LRCLK 为 176.4 kHz，SCLK 为 8.4672 MHz。

示例 5-9。带 PLL 的 DoP 播放

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	施加所有相关电源，然后断言复位。			
2	等待1.5毫秒。			
3	配置 PLL。XTI/MCLK 输入来自外部 19.2 MHz 信号，PLL 输出设置为 22.5792 MHz。其他频率组合的寄存器设置详见第 4.7.2 节			
4	PLL上电。	关断控制, 0x20000	0xFA	
		PDN_XSP	x	
		PDN_ASP	x	
		PDN_DSDIF	x	
		PDN_HP	x	
		PDN_XTAL	x	
		PDN_PLL	0 启动 PLL 模块	
		PDN_CLKOUT	x	
		保留	0	
5	设置 PLL 预分频值	PLL 设置 9, 0x40002	0x03	
		保留	0000 00	
		PLL_REF_PREDIV	11 将 PLL 预分频值设置为 8	
6	设置 PLL 输出分频值	PLL 设置 6, 0x30008	0x08	
		PLL_OUT_DIV	0x08 将 PLL 输出分频值设置为 8	
7	设置 PLL 分频比的小数部分 PLL 设置 2, 0x30002		0x00	
		PLL_DIV_FRAC_0	0x00 将 PLL 小数分频器最低有效位设置为 0	
		PLL 设置 3, 0x30003	0x00	
		PLL_DIV_FRAC_1	0x00 将 PLL 小数分频器中间字节设置为 0	
		PLL 设置 4, 0x30004	0x80	
		PLL_DIV_FRAC_2	0x80 将 PLL 小数分频器最高有效位设置为 0x80	
8	设置 PLL 分频比的整数部分	PLL 设置 5, 0x30005	0x49	
		PLL_DIV_INT	0x49 将 PLL 整数分频值设置为 0x49	
9	设置 PLL 模式	PLL 设置 8, 0x3001B	0x01	
		保留	0000 00	
		PLL_MODE	0 PLL 频率计算中采用 500/512 因子	
		保留	1	
10	读取中断状态寄存器1 (0xF0000) 以清除粘滞位。			
11	设置PLL校准比率	PLL 设置 7, 0x3000A	0x97	
		PLL_CAL_RATIO	PLL校准比率设置为0x97 (151)	
12	使能PLL中断	中断屏蔽 1, 0xF0010	0xF9	
		DAC_OVFL_INT_MASK	1 DAC_OVFL_INT 为无关状态	
		HPDETECT_PLUG_INT_MASK	1 取消屏蔽HPDETECT_PLUG中断	
		HPDETECT_UNPLUG_INT_MASK	1 取消屏蔽HPDETECT_UNPLUG中断	
		XTAL_READY_INT_MASK	1 XTAL_READY_INT 为无关状态	
		XTAL_ERROR_INT_MASK	1 XTAL_ERROR_INT 为无关状态	
		PLL_READY_INT_MASK	0 PLL_READY中断已取消屏蔽	
		PLL_ERROR_INT_MASK	0 PLL_ERROR中断已取消屏蔽	
		PDN_DONE_INT_MASK	1 PDN_DONE_INT 为无关状态	
13	启动 PLL	PLL 设置 1, 0x30001	0x01	
		保留	0000 0000	
		PLL_START	1 使能PLL输出	
14	播放DoP音频。假设64•Fs的DSD流			
15	配置ASP接口以支持DoP输入			
16	设置 ASP 采样率	串口采样率。0x1000B	0x05	
		保留	0000	
		ASP_SPRATE	0101 设置采样率为 176.4 kHz	
17	设置 ASP 采样位宽XSP 不关心 串口采样位宽。0x1000C 0x05 保留			
		XSP_SPSIZE	01 XSP 采样位宽设置为 24 位	
		ASP_SPSIZE	01 ASP 采样位宽设置为 24 位	
18	设置 ASP 分子	ASP 分子 1, 地址 0x40010	0x03	
		ASP_N_LSB	0x03 ASP 采样率分数分子最低有效位	
		ASP 分子 2, 地址 0x40011	0x00	
		ASP_N_MSB	0x00 ASP 采样率分数分子最高有效位	

Example 5-9. DoP Playback with PLL (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
19	Set ASP denominator	ASP Denominator 1. 0x40012	0x08	
		ASP_M_LSB	0x08	LSB of ASP sample rate fractional divide denominator
		ASP Denominator 2. 0x40013	0x00	
		ASP_M_MSB	0x00	MSB of ASP sample rate fractional divide denominator
20	Set ASP LRCK high time	ASP LRCK High Time 1. 0x40014	0x17	
		ASP_LCHI LSB	0x17	LSB of ASP LRCK high time duration
		ASP LRCK High Time 2. 0x40015	0x00	
		ASP_LCHI MSB	0x00	MSB of ASP LRCK high time duration
21	Set ASP LRCK period	ASP LRCK Period 1. 0x40016	0x2F	
		ASP_LCPR LSB	0x2F	LSB of ASP LRCK period
		ASP LRCK Period 2. 0x40017	0x00	
		ASP_LCPR MSB	0x00	MSB of ASP LRCK period
22	Configure ASP clock	ASP Clock Configuration. 0x40018	0x1C	
		Reserved	000	
		ASP_M/SB	1	Set ASP port to be Master
		ASP_SCPOL_OUT	1	Set output SCLK polarity
		ASP_SCPOL_IN	1	Input SCLK polarity is don't care
		ASP_LCPOL_OUT	0	Set Output LRCK polarity
		ASP_LCPOL_IN	0	Input LRCK polarity is don't care
23	Configure ASP frame	ASP Frame Configuration. 0x40019	0x0A	
		Reserved	000	
		ASP_STP	0	
		ASP_5050	1	Configure ASP port to accept I2S input
		ASP_FSD	010	
24	Set ASP channel location	ASP Channel 1 Location. 0x50000	0x00	
		ASP_RX_CH1	0x00	ASP Channel 1 starts on SCLK0
		ASP Channel 2 Location. 0x50001	0x00	
		ASP_RX_CH2	0x00	ASP Channel 2 starts on SCLK0
25	Set ASP channel size and enable	ASP Channel 1 Size and Enable. 0x5000A	0x06	
		Reserved	0000	
		ASP_RX_CH1_AP	0	ASP Channel 1 active phase
		ASP_RX_CH1_EN	1	ASP Channel 1 enable
		ASP_RX_CH1_RES	10	ASP Channel 1 size is 24 bits
		ASP Channel 2 Size and Enable. 0x5000B	0x0E	
		Reserved	0000	
		ASP_RX_CH2_AP	1	ASP Channel 2 active phase
		ASP_RX_CH2_EN	1	ASP Channel 2 enable
		ASP_RX_CH2_RES	10	ASP Channel 2 size is 24 bits
26	Wait for interrupt. Check if PLL_READY_INT = 1 in Interrupt Status 1 register(0xF0000).			
27	Configure DSD processor			
28	Configure DSD volume	DSD Volume A. 0x70001	0x00	
		DSD_VOLUME_A	0x00	Channel A volume set to 0 dB
29	Configure DSD Path Signal Control 1	DSD Processor Path Signal Control 1. 0x70002	0xCC	
		DSD_RAMP_UP	1	
		DSD_VOL_BEQA	1	DSD Volume B equals DSD volume A
		DSD_SZC	0	Immediate change
		Reserved	0	
		DSD_AMUTE	1	Mute occurs after 256 repeated 8-bit DSD mute patterns
		DSD_AMUTE_BEQA	1	Mute happens only when mute pattern is detected in both channels
		DSD_MUTE_A	0	Function is disabled
		DSD_MUTE_B	0	Function is disabled
30	Configure DSD interface	DSD Interface Configuration. 0x70003	0x04	
		Reserved	0000 0	
		DSD_M/SB	1	DSD is clock master
		DSD_PM_EN	0	Function is disabled
		DSD_PM_SEL	0	Function is disabled

示例5-9。带PLL的DoP播放 (续)

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
19 设置 ASP 分母	ASP 分母 1。0x40012	0x08		
	ASP_M_LSB	0x08	ASP 采样率分母最低有效位	
	ASP 分母 2, 地址 0x40013	0x00		
	ASP_M_MSB	0x00	ASP 采样率分母最高有效位	
20 设置 ASP LRCK 高电平时间	ASP LRCK 高电平时间 1。0x40014	0x17		
	ASP_LCHI_LSB	0x17	ASP LRCK 高电平时间持续最低有效位	
	ASP LRCK 高电平时间 2. 0x40015	0x00		
	ASP_LCHI_MSB	0x00	ASP LRCK 高电平时间持续时长最高有效位	
21 设置 ASP LRCK 周期	ASP LRCK 周期 1. 0x40016	0x2F		
	ASP_LCPR_LSB	0x2F	ASP LRCK 周期的最低有效位	
	ASP LRCK 周期 2. 0x40017	0x00		
	ASP_LCPR_MSB	0x00	ASP LRCK 周期的最高有效位	
22 配置 ASP 时钟	ASP 时钟配置. 0x40018	0x1C		
	保留	000		
	ASP_M/SB	1	设置 ASP 端口为主设备	
	ASP_SCPOL_OUT	1	设置输出 SCLK 极性	
	ASP_SCPOL_IN	1	输入 SCLK 极性不关心	
	ASP_LCPOL_OUT	0	设置输出 LRCK 极性	
	ASP_LCPOL_IN	0	输入 LRCK 极性不关心	
23 配置 ASP 帧格式	ASP 帧格式配置. 0x40019	0x0A 保留 ASP_		
	STP ASP	000		
	_5050 AS	0		
	P_FSD	1	配置 ASP 端口以接收 I2S 输入	
		010		
24 设置 ASP 通道位置	ASP 通道 1 位置. 0x50000	0x00		
	ASP_RX_CH1	0x00	ASP 通道 1 从 SCLK0 开始	
	ASP 通道 2 位置. 0x50001	0x00		
	ASP_RX_CH2	0x00	ASP 通道 2 从 SCLK0 开始	
25 设置 ASP 通道大小及使能	ASP 通道 1 大小及使能。0x5000A	0x06		
	保留	0000		
	ASP_RX_CH1_AP	0	ASP 通道 1 有效相位	
	ASP_RX_CH1_EN	1	ASP 通道 1 使能	
	ASP_RX_CH1_RES	10	ASP 通道 1 大小为 24 位	
	ASP 通道 2 大小及使能。0x5000B	0x0E		
	保留	0000		
	ASP_RX_CH2_AP	1	ASP 通道 2 有效相位	
	ASP_RX_CH2_EN	1	ASP 通道 2 使能	
	ASP_RX_CH2_RES	10	ASP 通道 2 大小为 24 位	
26 等待中断。检查中断状态寄存器 1 (0xF0000) 中 PLL_READY_INT 是否为 1。				
27 配置 DSD 处理器				
28 配置 DSD 音量	DSD 音量 A, 0x70001	0x00		
	DSD_VOLUME_A	0x00	通道 A 音量设置为 0 dB	
29 配置 DSD 路径信号控制 1		0xCC		
	DSD_RAMP_UP	1		
	DSD_VOL_BEQA	1	DSD 音量 B 等于 DSD 音量 A	
	DSD_SZC	0	立即更改	
	保留	0		
	DSD_AMUTE	1	静音发生在重复 256 次 8 位 DSD 静音模式后	
	DSD_AMUTE_BEQA	1	仅当两个通道均检测到静音模式时才发生静音	
	DSD 静音 A	0	功能已禁用	
	DSD 静音 B	0	功能已禁用	
30 配置DSD接口	DSD接口配置。0x70003	0x04		
	保留	0000 0		
	DSD_M/SB	1	DSD 为时钟主控	
	DSD_PM_EN	0	功能已禁用	
	DSD_PM_SEL	0	功能已禁用	

Example 5-9. DoP Playback with PLL (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
31	Configure DSD Path Signal Control 2	DSD Processor Path Signal Control 2. 0x70004	0x50	
		Reserved	0	
		DSD_PRC_SRC	10	Set source of DSD processor to ASP
		DSD_EN	1	Enable DSD playback
		Reserved	0	
		DSD_SPEED	0	Set DSD clock speed to 64·Fs
		STA_DSD_DET	0	Static DSD detection disabled
		INV_DSD_DET	0	Invalid DSD detection disabled
32	Configure DSD path Signal Control 3	DSD Processor Path Signal Control 3. 0x70006	0xC0	
		DSD_ZERO_DB	1	The SACD 0-dB reference level (50% modulation index) matches PCM 0-dB full scale.
		DSD_HPF_EN	1	Enable HPF in DSD processor
		Reserved	0	
		SIGCTL_DSDEQPCM	0	Function is disabled
		DSD_INV_A	0	Function is disabled
		DSD_INV_B	0	Function is disabled
		DSD_SWAP_CHAN	0	Function is disabled
		DSD_COPY_CHAN	0	Function is disabled
33	Configure headphone output for 1.732 V rms			
34	Configure Class H amplifier	Class H Control. 0xB0000	0x1E	
		Reserved	000	
		ADPT_PWR	1 11	Output signal determines voltage level
		HV_EN	1	High voltage mode enabled
		EXT_VCPFILT	0	Using internal VCPFILT source.
35	Set HP output to full scale	HP Output Control 1. 0x80000	0x30	
		HP_CLAMPA	0	
		HP_CLAMPB	0	
		OUT_FS	11	Set headphone output to full scale (1.732 V rms)
		HP_IN_EN	0	
		HP_IN_LP	0	
		Reserved	0	
		+1dB_EN	0	
36	Headphone detect	HP Detect. 0xD0000	0xC4	
		HPDETECT_CTRL	11	HP detect enabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	0 0	Tip Sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
37	Enable interrupts			
38	Read Interrupt Status 1 register (0xF0000), Interrupt Status 2 register (0xF0001) and Interrupt Status 5 register (0xF0004) to clear sticky bits.			
39	Enable headphone detect interrupts	Interrupt Mask 1. 0xF0010	0x99	
		DAC_OVFL_INT_MASK	1	DAC_OVFL_INT is don't care
		HPDETECT_PLUG_INT_MASK	0	Enable HPDETECT_PLUG interrupt
		HPDETECT_UNPLUG_INT_MASK	0	Enable HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	1	XTAL_READY_INT is don't care
		XTAL_ERROR_INT_MASK	1	XTAL_ERROR_INT is don't care
		PLL_READY_INT_MASK	0	PLL_READY interrupt already enabled
		PLL_ERROR_INT_MASK	0	PLL_ERROR interrupt already enabled
		PDN_DONE_INT_MASK	1	PDN_DONE_INT is don't care
40	Enable ASP interrupts	Interrupt Mask 2. 0xF0011	0x07	
		ASP_OVFL_INT_MASK	0	Enable ASP_OVFL interrupt
		ASP_ERROR_INT_MASK	0	Enable ASP_ERROR interrupt
		ASP_LATE_INT_MASK	0	Enable ASP_LATE interrupt
		ASP_EARLY_INT_MASK	0	Enable ASP_EARLY interrupt
		ASP_NOLRCK_INT_MASK	0	Enable ASP_NOLRCK interrupt
		Reserved	111	
41	Enable DSD and DoP interrupts	Interrupt Mask 5. 0xF0014	0x01	
		DSD_STUCK_INT_MASK	0	Enable DSD_STUCK interrupt
		DSD_INVAL_A_INT_MASK	0	Enable DSD_INVAL_A interrupt
		DSD_INVAL_B_INT_MASK	0	Enable DSD_INVAL_B interrupt
		DSD_SILENCE_A_INT_MASK	0	Enable DSD_SILENCE_A interrupt
		DSD_SILENCE_B_INT_MASK	0	Enable DSD_SILENCE_B interrupt
		DSD_RATE_ERROR_INT_MASK	0	Enable DSD_RATE_ERROR interrupt
		DOP_MRK_DET_INT_MASK	0	Enable DOP_MRK_DET interrupt
		DOP_ON_INT_MASK	1	Disable DOP_ON interrupt
42	Wait for interrupt. Check if PLL_READY_INT = 1 in Interrupt Status 1 register(0xF0000).			
43	Set MCLK source and frequency	System Clocking Control. 0x10006	0x05	
		Reserved	0000 0	
		MCLK_INT	1	MCLK Frequency is set to 22.5792 MHz
		MCLK_SRC_SEL	01	MCLK Source is set to PLL
44	Wait for at least 150 µs.			

示例5-9。带PLL的DoP播放 (续)

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
31 配置DSD路径信号控制2			0x50	
		保留	0	
		DSD_PRC_SRC	10	将DSD处理器源设置为ASP
		DSD_EN	1	启用DSD播放
		保留	0	
		DSD_SPEED	0	将DSD时钟速度设置为64·Fs
		STA_DSD_DET	0	禁用静态DSD检测
		INV_DSD_DET	0	禁用无效DSD检测
32 配置DSD路径信号控制3			0xC0	
		DSD_ZERO_DB	1	SACD 0 dB参考电平 (50% 调制指数) 与PCM 0 dB满量程相匹配。
		DSD_HPF_EN	1	启用DSD处理器中的高通滤波器
		保留	0	
		SIGCTL_DSDEQPCM	0	功能已禁用
		DSD_INV_A	0	功能已禁用
		DSD_INV_B	0	功能已禁用
		DSD_SWAP_CHAN	0	功能已禁用
		DSD_COPY_CHAN	0	功能已禁用
33 配置耳机输出为1.732 V rms				
34 配置 Class H 放大器	Class H 控制。0xB0000		0x1E	
	保留	000		
	ADPT_PWR	1 11		输出信号决定电压等级
	HV_EN	1		高电压模式已启用
	EXT_VCPFILT	0		使用内部 VCPFILT 源。
35 将耳机输出设置为满量程	耳机输出控制 1, 0x80000		0x30	
	HP_CLAMPA	0		
	HP_CLAMPB	0		
	OUT_FS	11		将耳机输出设置为满量程 (1.732 V rms)
	HP_IN_EN	0		
	HP_IN_LP	0		
	保留	0		
	+1dB_EN	0		
36 耳机检测	耳机检测, 0xD0000		0xC4	
	HPDETECT_CTRL	11		启用耳机检测
	HPDETECT_IN	0		耳机检测输入未反相
	V_HPDetect_RISE_DBC_TI	0 0		Tip Sense 上升沿消抖时间设置为 0 毫秒
	ME_HPDetect_Fall_DBC_T	10		Tip 感应下降消抖时间设置为 500 毫秒
	IME 保留	0		
37 启用中断				
38 读取中断状态寄存器 1 (0xF0000)、中断状态寄存器 2 (0xF0001) 和中断状态寄存器 5 (0xF0004) 以清除粘滞位。				
39 启用耳机检测中断	中断屏蔽 1, 0xF0010		0x99	
	DAC_OVFL_INT_MASK	1		DAC_OVFL_INT 为无关状态
	HPDETECT_PLUG_INT_MASK	0		启用 HPDETECT_PLUG 中断
	HPDETECT_UNPLUG_INT_MASK	0		启用 HPDETECT_UNPLUG 中断
	XTAL_READY_INT_MASK	1		XTAL_READY_INT 不关心
	XTAL_ERROR_INT_MASK	1		XTAL_ERROR_INT 不关心
	PLL_READY_INT_MASK	0		PLL_READY 中断已启用
	PLL_ERROR_INT_MASK	0		PLL_ERROR 中断已启用
	PDN_DONE_INT_MASK	1		PDN_DONE_INT 不关心
40 启用 ASP 中断	中断屏蔽 2, 0xF0011		0x07	
	ASP_OVFL_INT_MASK	0		启用 ASP_OVFL 中断
	ASP_ERROR_INT_MASK	0		启用 ASP_ERROR 中断
	K ASP_LATE_INT_M	0		启用 ASP_LATE 中断
	SK ASP_EARLY_INT_M	0		启用 ASP_EARLY 中断
	ASK ASP_NOLRCK_INT_MASK 保留	111		启用 ASP_NOLRCK 中断
41 启用 DSD 和 DoP 中断	中断屏蔽 5, 0xF0014		0x01	
	DSD_STUCK_INT_MASK	0		启用 DSD_STUCK 中断
	DSD_INVAL_A_INT_MASK	0		使能 DSD_INVAL_A 中断
	DSD_INVAL_B_INT_MASK	0		使能 DSD_INVAL_B 中断
	DSD_SILENCE_A_INT_MASK	0		使能 DSD_SILENCE_A 中断
	DSD_SILENCE_B_INT_MASK	0		使能 DSD_SILENCE_B 中断
	DSD_RATE_ERROR_INT_MASK	0		使能 DSD_RATE_ERROR 中断
	DOP_MRK_DET_INT_MASK	0		启用 DOP_MRK_DET 中断
	DOP_ON_INT_MASK	1		禁用 DOP_ON 中断
42 等待中断。检查中断状态寄存器 1 (0xF0000) 中 PLL_READY_INT 是否为 1。				
43 设置 MCLK 源和频率	系统时钟控制。0x10006		0x05	
	保留	0000 0		
	MCLK_INT	1		MCLK 频率设置为 22.5792 MHz
	MCLK_SRC_SEL	01		MCLK 源设置为 PLL
44 等待至少 150 μs。				

Example 5-9. DoP Playback with PLL (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
45	Enable ASP clocks	Pad Interface Configuration. 0x1000D	0x02	
		Reserved	0000 00	
		XSP_3ST	1	XSP Interface status is don't care (set to default)
		ASP_3ST	0	Enable serial clocks in Master Mode
46	Power up HP	Refer to Ex. 5-6 for DSD power-up sequence. Note that in Step 1 of Ex. 5-6 , use HH = BF for DoP over ASP interface.		

5.13.4 Power-up Sequence to I2S Playback in Mono Mode

In [Ex. 5-7](#), a 22.5792-MHz crystal is used, ASP is set to I2S master at 44.1 kHz, and full-scale output is 1.732 Vrms.

Example 5-10. Startup to I2S Playback in Mono Mode

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Apply all relevant power supplies, then assert <u>RESET</u> .			
2	Wait for 1.5 ms.			
3	Configure XTAL driver			
4	Configure XTAL bias current strength (assuming River Crystal at 22.5792 MHz)	Crystal Setting. 0x20052	0x04	
		Reserved	0000 0	
		XTAL_IBIAS	100	Bias current set to 12.5 μ A
5	Read Interrupt Status 1 register (0xF0000) to clear any pending interrupts.			
6	Enable XTAL interrupts	Interrupt Mask 1. 0xF0010	0xE7	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	1	Enable XTAL_READY interrupt
		HPDETECT_UNPLUG_INT_MASK	1	Enable XTAL_ERROR interrupt
		XTAL_READY_INT_MASK	0	
		XTAL_ERROR_INT_MASK	0	
		PLL_READY_INT_MASK	1	
		PLL_ERROR_INT_MASK	1	
		PDN_DONE_INT_MASK	1	
7	Start XTAL	Power Down Control. 0x20000	0xF6	
		PDN_XSP	1	
		PDN_ASP	1	
		PDN_DSDIF	1	
		PDN_HP	1	
		PDN_XTAL	0	Power up XTAL driver
		PDN_PLL	1	
		PDN_CLKOUT	1	
		Reserved	0	
8	Configure ASP interface. Sample rate set to 44.1 kHz. ASP is clock master.			
9	Set ASP sample rate	Serial Port Sample Rate. 0x1000B	0x01	
		Reserved	0000	
		ASP_SPRATE	0001	Set sample rate to 44.1 kHz
10	Set ASP sample bit size. XSP is don't care	Serial Port Sample Bit Size. 0x1000C	0x04	
		Reserved	0000	
		XSP_SPSIZE	01	XSP sample bit size set to 24 bits
		ASP_SPSIZE	00	ASP sample bit size set to 32 bits
11	Set ASP numerator	ASP Numerator 1. 0x40010	0x01	
		ASP_N_LSB	0x01	LSB of ASP sample rate fractional divide numerator
		ASP Numerator 2. 0x40011	0x00	
		ASP_N_MSB	0x00	MSB of ASP sample rate fractional divide numerator
12	Set ASP denominator	ASP Denominator 1. 0x40012	0x08	
		ASP_M_LSB	0x08	LSB of ASP sample rate fractional divide denominator
		ASP Denominator 2. 0x40013	0x00	
		ASP_M_MSB	0x00	MSB of ASP sample rate fractional divide denominator
13	Set ASP LRCK high time	ASP LRCK High Time 1. 0x40014	0x1F	
		ASP_LCHI_LSB	0x1F	LSB of ASP LRCK high time duration
		ASP LRCK High Time 2. 0x40015	0x00	
		ASP_LCHI_MSB	0x00	MSB of ASP LRCK high time duration
14	Set ASP LRCK period	ASP LRCK Period 1. 0x40016	0x3F	
		ASP_LCPY_LSB	0x3F	LSB of ASP LRCK period
		ASP LRCK Period 2. 0x40017	0x00	
		ASP_LCPY_MSB	0x00	MSB of ASP LRCK period

示例5-9。带PLL的DoP播放 (续)

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
45 使能 ASP 时钟		引脚接口配置。0x1000D 0x02		
		保留	0000 00	
		XSP_3ST	1	XSP 接口状态无关 (设置为默认)
		ASP_3ST	0	主模式下启用串行时钟。
46 上电耳机驱动器		有关 DSD 上电顺序, 请参见示例 5-6。注意, 在示例 5-6 的步骤 1 中, ASP 接口上的 DoP 使用 H = BF。		

5.13.4 单声道模式下 I2S 播放的上电序列

在示例5-7中, 使用22.5792 MHz晶体, ASP设置为44.1 kHz的I2S主模式, 满量程输出为1.732 Vrms。

示例 5-10。单声道模式下启动 I2S 播放

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	施加所有相关电源, 然后断言复位。			
2	等待1.5毫秒。			
3	配置晶体振荡器驱动			
4	配置晶体振荡器偏置 电流强度 (假设River Crystal频率为22.5792 MHz)	晶体设置。0x20052 保留	0x04 0000 0	
		晶体振荡器偏置电流	100	偏置电流设置为12.5 μA
5	读取中断状态1寄存器 (0xF0000) 以清除所有待处理中断。			
6	启用晶体振荡器中断中断屏蔽1。0xF0010		0xE7	
		DAC_OVFL_INT_MASK HPDETECT_PLUG_INT_MASK HPDETECT_UNPLUG_INT_MASK XTAL_READY_INT_MASK XTAL_ERROR_INT_MASK PLL_READY_INT_MASK PLL_ERROR_INT_MASK PDN_DONE_INT_MASK	1 1 1 0 0 1 1 1	启用晶体振荡器就绪中断 启用晶体振荡器错误中断
7	启动晶体振荡器	关断控制, 0x20000	0xF6	
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT 保留	1 1 1 1 0 1 1 0	晶体振荡器驱动器上电
8	配置ASP接口。采样率设置为44.1 kHz, ASP为时钟主控。			
9	设置ASP采样率串行端口采样率。0x1000B		0x01	
		保留 ASP采样率	0000 0001	设置采样率为44.1 kHz
10	XSP 状态无关设置 ASP 采样位宽。	串行端口采样位宽。0x1000C	0x04	
		保留 XSP_SPSIZE ASP_SPSIZE	0000 01 00	XSP 采样位宽设置为 24 位 ASP 采样位宽设置为 32 位
11	设置 ASP 分子	ASP 分子 1, 地址 0x40010 ASP_N_LSB ASP 分子 2, 地址 0x40011 ASP_N_MSB	0x01 0x01 0x00 0x00	
12	设置 ASP 分母ASP 分母 1, 地址 0x40012 ASP_M_LSB ASP 分母 2, 地址 0x40013 ASP_M_MSB		0x08 0x08 0x00 0x00	ASP 采样率分数除法分母最低有效位 ASP 采样率分数除法分母最高有效位
13	设置 ASP LRCK 高电平时间 ASP LRCK 高电平时间 1, 地址 0x40014 ASP_LCHI_LSB ASP LRCK 高电平时间 2, 地址 0x40015 ASP_LCHI_MSB		0x1F 0x1F 0x00 0x00	ASP 采样率分数除法分母最低有效位 ASP 采样率分数除法分母最高有效位
14	设置 ASP LRCK 周期 ASP_LRCK 周期 1.0x40016 ASP_LCPY_LSB ASP_LRCK 周期 2.0x40017 ASP_LCPY_MSB		0x3F 0x3F 0x00 0x00	ASP 采样率周期的最低有效位 ASP 采样率周期的最高有效位

Example 5-10. Startup to I2S Playback in Mono Mode (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
15	Configure ASP clock	ASP Clock Configuration. 0x40018	0x1C	
		Reserved	000	
		ASP_M/SB	1	Set ASP port to be master
		ASP_SCPOL_OUT	1	Configure clock polarity for I2S input
		ASP_SCPOL_IN	1	
		ASP_LCPOL_OUT	0	
		ASP_LCPOL_IN	0	
16	Configure ASP frame	ASP Frame Configuration. 0x40019	0xA	
		Reserved	000	Configure ASP port to accept I2S input
		ASP_STP	0	
		ASP_5050	1	
		ASP_FSD	010	
17	Set ASP channel location	ASP Channel 1 Location. 0x50000	0x00	
		ASP_RX_CH1	0x00	ASP Channel 1 starts on SCLK0
		ASP Channel 2 Location. 0x50001	0x00	
		ASP_RX_CH2	0x00	ASP Channel 2 starts on SCLK0
18	Set ASP channel size and enable. Set both Channel 1 and Channel 2 to the same active phase to get the same data for mono mode.	ASP Channel 1 Size and Enable. 0x5000A	0x07/0xF for Left/Right channel	
		Reserved	0000	
		ASP_RX_CH1_AP	0/1	ASP Channel 1 Active Phase
		ASP_RX_CH1_EN	1	ASP Channel 1 Enable
		ASP_RX_CH1_RES	11	ASP Channel 1 Size is 32 bits
		ASP Channel 2 Size and Enable. 0x5000B	0x07/0xF for Left/Right channel	
		Reserved	0000	
		ASP_RX_CH2_AP	0/1	ASP Channel 2 Active Phase
		ASP_RX_CH2_EN	1	ASP Channel 2 Enable
		ASP_RX_CH2_RES	11	ASP Channel 2 Size is 32 bits
19	Configure PCM interface. HPF filter is used. Deemphasis off.			
20	Configure PCM filter	PCM Filter Option. 0x90000	0x02	
		FILTER_SLOW_FASTB	0	
		PHCOMP_LOWLATB	0	
		NOS	0	
		Reserved	0 0	
		PCM_WBF_EN	0	
		HIGH_PASS	1	High pass filter is selected
		DEEMP_ON	0	
21	Set volume for channel B	PCM Volume B. 0x90001	0x00	
		PCM_VOLUME_B	0x00	Set volume to 0 dB
22	Set volume for channel A	PCM Volume A. 0x90002	0x00	
		PCM_VOLUME_A	0x00	Set volume to 0 dB
23	Configure PCM path signal control	PCM Path Signal Control 1. 0x90003	0xEC	
		PCM_RAMP_DOWN	1	Soft ramp down of volume on filter change
		PCM_VOL_BEQA	1	Volume setting on both channels controlled by PCM_VOLUME_A
		PCM_SZC	10	Enable soft ramp
		PCM_AMUTE	1	Mute after reception of 8192 samples of 0 or -1.
		PCM_AMUTEBEQA	1	Mute only when AMUTE condition is detected on both channels
		PCM_MUTE_A	0	Function is disabled
		PCM_MUTE_B	0	Function is disabled
		PCM Path Signal Control 2. 0x90004	0x00	
		Reserved	0000	
		PCM_INV_A	0	Disable all functions in this register
		PCM_INV_B	0	
		PCM_SWAP_CHAN	0	
		PCM_COPY_CHAN	0	
24	Configure HP			
25	Configure Class H amplifier	Class H Control. 0xB0000	0x1E	
		Reserved	000	
		ADPT_PWR	1 11	Output signal determines voltage level
		HV_EN	1	High voltage mode enabled
		EXT_VCPFILT	0	Using internal VCPFILT source.
26	Set HP output to full scale	HP Output Control 1. 0x80000	0x30	
		HP_CLAMPA	0	
		HP_CLAMPB	0	
		OUT_FS	11	Set headphone output to full scale (1.732 V rms)
		HP_IN_EN	0	
		HP_IN_LP	0	
		Reserved	0	
		+1dB_EN	0	

示例 5-10。单声道模式下启动 I²S 播放 (续)

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
15	配置 ASP 时钟 ASP 时钟配置。0x40018		0x1C	
	保留		000	
	M/SB_AS		1	设置 ASP 端口为主设备
	P_SCPOL_OUT_A		1	配置 I ² S 输入的时钟极性
	SP_SCPOL_IN		1	
	ASP_LCPOL_OUT		0	
	ASP_LCPOL_IN		0	
16	配置 ASP 帧 ASP 帧配置。0x40019		0x0A	
	保留		000	配置 ASP 端口以接收 I ² S 输入
	ASP_STP		0	
	ASP_5050		1	
	ASP_FSD		010	
17	设置 ASP 通道位置 ASP 通道 1 位置。0x50000		0x00	
	ASP_RX_CH1		0x00	ASP 通道 1 从 SCLK0 开始
	ASP 通道 2 位置。0x50001		0x00	
	ASP_RX_CH2		0x00	ASP 通道 2 从 SCLK0 开始
18	设置 ASP 通道大小并使能 。将通道 1 和通道 2 设置 为相同的激活相位，以获 得单声道模式下相同的数据。	ASP 通道 1 大小及启用，地址 0x5000A	左/右通道分别为 0x07/0x0F	
	保留		0000	
	ASP_RX_CH1_AP		0/1	ASP 通道 1 有效相位
	ASP_RX_CH1_EN		1	启用 ASP 通道 1
	ASP_RX_CH1_RES		11	ASP 通道 1 大小为 32 位
	ASP 通道 2 大小及启用，地址 0x5000B		左/右通道分别为 0x07/0x0F	
	保留		0000	
	ASP_RX_CH2_AP		0/1	ASP 通道 2 有效相位
	ASP_RX_CH2_EN		1	启用 ASP 通道 2
	ASP_RX_CH2_RES		11	ASP 通道 2 大小为 32 位
19	配置 PCM 接口，使用高通滤波器，取消预加重			
20	配置 PCM 滤波器	PCM 滤波器选项。0x90000	0x02	
	FILTER_SLOW_FASTB		0	
	PHCOMP_LOWLATB		0	
	NOS		0	
	保留		0 0	
	PCM_WBF_EN		0	
	HIGH_PASS		1	选择高通滤波器
	DEEMP_ON		0	
21	设置通道 B 音量，PCM 音量 B，地址 0x90001		0x00	
	PCM_VOLUME_B		0x00	设置音量为 0 dB
22	设置通道 A 的音量 PCM Volume A。0x90002		0x00	
	PCM_VOLUME_A		0x00	设置音量为 0 dB
23	配置 PCM 路径信号 控制	PCM 路径信号控制1，0x90003	0xEC	
	PCM_RAMP_DOWN		1	滤波器切换时音量软降
	PCM_VOL_BEQA		1	两个通道的音量设置由 PCM_VOLUME_A 控制
	PCM_SZC		10	启用软斜坡
	PCM_AMUTE		1	接收 8192 个值为 0 或 -1 的样本后静音
	PCM_AMUTEBEQA		1	仅当两个通道均检测到 AMUTE 条件时静音
	PCM_MUTE_A		0	功能已禁用
	PCM_MUTE_B		0	功能已禁用
	PCM 路径信号控制2，地址0x90004		0x00	
	保留		0000	
	PCM_INV_A		0	禁用此寄存器中的所有功能
	PCM_INV_B		0	
	PCM_SWAP_CHAN		0	
	PCM_COPY_CHAN		0	
24	配置耳机			
25	配置 Class H 放大器 Class H 控制。0xB0000		0x1E	
	保留		000	
	ADPT_PWR		1 11	输出信号决定电压等级
	HV_EN		1	高电压模式已启用
	EXT_VCPFILT		0	使用内部 VCPFILT 源。
26	将耳机输出设置为满量程耳机输出控制 1，0x80000		0x30	
	HP_CLAMPA		0	
	HP_CLAMPB		0	
	OUT_FS		11	将耳机输出设置为满量程 (1.732 V rms)
	HP_IN_EN		0	
	HP_IN_LP		0	
	保留		0	
	+1dB_EN		0	

Example 5-10. Startup to I2S Playback in Mono Mode (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
27	Configure Headphone detect	HP Detect. 0xD0000	0x04	
		HPDETECT_CTRL	00	HP detect disabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	0 0	Tip sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
28	Headphone detect	HP Detect. 0xD0000	0xC4	
		HPDETECT_CTRL	11	HP detect enabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	0 0	Tip sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
29	Enable interrupts			
30	Read Interrupt Status 1 register (0xF0000) and Interrupt Status 2 register (0xF0001) to clear sticky bits.			
31	Enable headphone detect interrupts	Interrupt Mask 1. 0xF0010	0x87	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	0	Enable HPDETECT_PLUG interrupt
		HPDETECT_UNPLUG_INT_MASK	0	Enable HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	0	
		XTAL_ERROR_INT_MASK	0	
		PLL_READY_INT_MASK	1	
		PLL_ERROR_INT_MASK	1	
		PDN_DONE_INT_MASK	1	
32	Enable ASP interrupts	Interrupt Mask 2. 0xF0011	0x07	
		ASP_OVFL_INT_MASK	0	Enable ASP_OVFL interrupt
		ASP_ERROR_INT_MASK	0	Enable ASP_ERROR interrupt
		ASP_LATE_INT_MASK	0	Enable ASP_LATE interrupt
		ASP_EARLY_INT_MASK	0	Enable ASP_EARLY interrupt
		ASP_NOLRCK_INT_MASK	0	Enable ASP_NOLRCK interrupt
		Reserved	111	
33	Wait for interrupt. Check if XTAL_READY_INT = 1 in Interrupt Status 1 register (0xF0000).			
34	Switch MCLK source to XTAL	System Clocking Control 1. 0x10006	0x04	
		Reserved	0000 0	MCLK Source set to XTAL. MCLK_INT frequency set to
		MCLK_INT	1	22.5792 MHz
		MCLK_SRC_SEL	00	
35	Wait at least 150 µs.			
36	Enable ASP clocks	Pad Interface Configuration. 0x1000D	0x02	
		Reserved	0000 00	
		XSP_3ST	1	XSP Interface status is don't care (set to default)
		ASP_3ST	0	Enable serial clocks in Master Mode
37	Enable mono mode	Refer to Section 5.12.1 for the Sequence for Enabling Mono Mode		
38	Power up HP	Refer to Ex. 5-5 for PCM power-up sequence		

5.13.5 Power-Up Sequence to DSD Playback in Mono Mode

In [Ex. 5-8](#), a 22.5792-MHz crystal is used, the PLL is used to create a 24.576-MHz MCLK, XSP is set as DSD slave at 2.8224 MHz, and full-scale output is 1.732 Vrms.

Example 5-11. Startup to DSD Playback in Mono Mode

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Apply all relevant power supplies, then assert RESET.			
2	Wait for 1.5 ms.			
3	Configure XTAL driver			
4	Configure XTAL bias current strength (assuming River Crystal at 22.5792 MHz)	Crystal Setting. 0x20052	0x04	
		Reserved	0000 0	
		XTAL_IBIAS	100	Bias current set to 12.5 µA
5	Read Interrupt Status 1 register (0xF0000) to clear any pending interrupts.			
6	Enable XTAL interrupts	Interrupt Mask 1. 0xF0010	0xE7	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	1	
		HPDETECT_UNPLUG_INT_MASK	1	
		XTAL_READY_INT_MASK	0	Enable XTAL_READY interrupt
		XTAL_ERROR_INT_MASK	0	Enable XTAL_ERROR interrupt
		PLL_READY_INT_MASK	1	
		PLL_ERROR_INT_MASK	1	
		PDN_DONE_INT_MASK	1	

示例 5-10。单声道模式下启动 I2S 播放 (续)

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
27	配置耳机检测	耳机检测, 0xD0000	0x04	
		HPDETECT_CTRL	00	耳机检测已禁用
		HPDETECT_IN	0	耳机检测输入未反相
		V HPDETECT_RISE_DBC_TI	0 0	Tip 感应上升消抖时间设置为 0 毫秒
		ME HPDETECT_FALL_DBC_T	10	Tip 感应下降消抖时间设置为 500 毫秒
		IME 保留	0	
28	耳机检测	耳机检测, 0xD0000	0xC4	
		HPDETECT_CTRL	11	启用耳机检测
		HPDETECT_IN	0	耳机检测输入未反相
		V HPDETECT_RISE_DBC_TI	0 0	Tip 感应上升消抖时间设置为 0 毫秒
		ME HPDETECT_FALL_DBC_T	10	Tip 感应下降消抖时间设置为 500 毫秒
		IME 保留	0	
29	启用中断			
30	读取中断状态寄存器1 (0xF0000) 和中断状态寄存器2 (0xF0001) 以清除粘滞位。			
31	中断启用耳机检测	中断屏蔽 1, 0xF0010	0x87	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	0	启用HPDETECT_PLUG中断
		HPDETECT_UNPLUG_INT_MASK	0	启用HPDETECT_UNPLUG中断
		XTAL_READY_INT_MASK	0	
		XTAL_ERROR_INT_MASK	0	
		PLL_READY_INT_MASK	1	
		PLL_ERROR_INT_MASK	1	
		PDN_DONE_INT_MASK	1	
32	启用ASP中断中断掩码2, 地址0xF0011		0x07	
		ASP_OVFL_INT_MASK	0	启用ASP_OVFL中断
		ASP_ERROR_INT_MASK	0	启用ASP_ERROR中断
		K ASP_LATE_INT_MASK	0	启用ASP_LATE中断
		SK ASP_EARLY_INT_MASK	0	启用ASP_EARLY中断
		ASK ASP_NOLRCK_INT_MASK	0	启用ASP_NOLRCK中断
		MASK 保留	111	
33	等待中断。检查中断状态寄存器1 (0xF0000) 中XTAL_READY_INT位是否为1。			
34	切换MCLK时钟源至 XTAL	系统时钟控制寄存器1, 地址0x10006	0x04	
		保留	0000 0	MCLK源设置为晶体振荡器。MCLK_INT频率设置为22
		MCLK_INT	1	.5792 MHz。
		MCLK_SRC_SEL	00	
35	等待至少150 μs。			
36	启用ASP时钟。	引脚接口配置。0x1000D	0x02	
		保留	0000 00	
		XSP_3ST	1	XSP接口状态为无关 (设置为默认值)
		ASP_3ST	0	主模式下启用串行时钟。
37	启用单声道模式	有关启用单声道模式的序列, 请参见第 5.12.1 节		
38	耳机供电开启	参见示例5-5的PCM上电顺序。		

5.13.5 单声道模式下 DSD 播放的上电序列

在示例 5-8 中, 使用 22.5792 MHz 晶体, PLL 用于生成 24.576 MHz MCLK, XSP 设置为 2.8224 MHz 的 DSD 从机, 满量程输出为 1.732 Vrms。

示例 5-11。启动至单声道模式下的 DSD 播放

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	施加所有相关电源, 然后断言复位。			
2	等待1.5 ms。			
3	配置晶体振荡器驱动。			
4	配置晶体振荡器偏置电流强度 (假设River Crystal为22.5792 MHz)。	晶体设置。0x20052	0x04	
		保留	0000 0	
		晶体振荡器偏置电流	100	偏置电流设置为 12.5 μA。
5	读取中断状态1寄存器 (0xF0000) 以清除所有待处理中断。			
6	启用晶体振荡器中断。	中断屏蔽 1, 0xF0010	0xE7	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	1	
		HPDETECT_UNPLUG_INT_MASK	1	
		XTAL_READY_INT_MASK	0	启用晶体振荡器就绪中断
		XTAL_ERROR_INT_MASK	0	启用晶体振荡器错误中断
		PLL_READY_INT_MASK	1	
		PLL_ERROR_INT_MASK	1	
		PDN_DONE_INT_MASK	1	

Example 5-11. Startup to DSD Playback in Mono Mode (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
7	Start XTAL	Power Down Control. 0x20000	0xF6	
		PDN_XSP	1	
		PDN_ASP	1	
		PDN_DSDIF	1	
		PDN_HP	1	
		PDN_XTAL	0	Power up XTAL driver
		PDN_PLL	1	
		PDN_CLKOUT	1	
		Reserved	0	
8	Configure PLL. Input is 22.5792 MHz. Output is 24.576 MHz.			
9	Power up PLL	Power Down Control. 0x20000	0xF2	
		PDN_XSP	1	
		PDN_ASP	1	
		PDN_DSDIF	1	
		PDN_HP	1	
		PDN_XTAL	0	Power up PLL
		PDN_PLL	0	
		PDN_CLKOUT	1	
		Reserved	0	
10	Set PLL predive	PLL Setting 9. 0x40002	0x03	
		Reserved	0000 00	
		PLL_REF_PREDIV	11	Divide PLL Reference by 8
11	Set PLL Output Divide	PLL Setting 6. 0x30008	0x08	
		PLL_OUT_DIV	0x08	Divide PLL output by 8
12	Set Fractional portion of PLL divide ratio	PLL Setting 2. 0x30002	0x00	
		PLL_DIV_FRAC_0	0x00	
		PLL Setting 3. 0x30003	0xF7	
		PLL_DIV_FRAC_1	0xF7	
		PLL Setting 4. 0x30004	0x06	
		PLL_DIV_FRAC_2	0x06	
13	Set integer portion of PLL divide ratio	PLL Setting 5. 0x30005	0x44	
		PLL_DIV_INT	0x44	
14	Set PLL Mode	PLL Setting 8. 0x3001B	0x01	
		Reserved	0000 00	
		PLL_MODE	0	Use 500/512 factor
		Reserved	1	
15	Set PLL Calibration Ratio	PLL Setting 7. 0x3000A	0x8B	
		PLL_CAL_RATIO	0x8B	Set PLL Cal Ratio to 139
16	Read Interrupt Status 1 register (0xF0000) to clear any pending interrupts.			
17	Enable PLL Interrupts	Interrupt Mask 1. 0xF0010	0xE1	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	1	
		HPDETECT_UNPLUG_INT_MASK	1	Enable PLL Ready and Error Interrupts
		XTAL_READY_INT_MASK	0	
		XTAL_ERROR_INT_MASK	0	
		PLL_READY_INT_MASK	0	
		PLL_ERROR_INT_MASK	0	
		PDN_DONE_INT_MASK	1	
18	Start PLL	PLL Setting 1. 0x30001	0x01	
		Reserved	0000 000	
		PLL_START	1	Start PLL
19	Configure DSDIF to playback 64•Fs DSD stream. DSDIF is configured as Slave			
20	Configure DSD Volume	DSD Volume A. 0x70001	0x00	
		DSD_VOLUME_A	0x00	Channel A volume set to 0dB
21	Configure DSD path Signal Control1	DSD Processor Path Signal Control 1. 0x70002	0xCC	
		DSD_RAMP_UP	1	
		DSD_VOL_BEQA	1	DSD Volume B equals DSD volume A
		DSD_SZC	0	Immediate change
		Reserved	0	
		DSD_AMUTE	1	Mute occurs after 256 repeated 8-bit DSD mute patterns
		DSD_AMUTE_BEQA	1	Mute happens only when mute pattern is detected in both channels
		DSD_MUTE_A	0	Function is disabled
		DSD_MUTE_B	0	Function is disabled

示例 5-11。启动至单声道模式下的 DSD 播放 (续)

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
7	启动晶体振荡器	关断控制, 0x20000	0xF6	
		PDN_XSP	1	
		PDN_ASP	1	
		PDN_DSDIF	1	
		PDN_HP	1	
		PDN_XTAL	0	晶体振荡器驱动器上电
		PDN_PLL	1	
		PDN_CLKOUT	1	
		保留	0	
8	配置PLL。输入为22.5792 MHz, 输出为24.576 MHz。			
9	PLL上电。	关断控制, 0x20000	0xF2	
		PDN_XSP	1	
		PDN_ASP	1	
		PDN_DSDIF	1	
		PDN_HP	1	
		PDN_XTAL	0	
		PDN_PLL	0	PLL上电。
		PDN_CLKOUT	1	
		保留	0	
10	设置 PLL 预分频	PLL 设置 9, 0x40002	0x03	
		保留	0000 00	
		PLL_REF_PREDIV	11	PLL 参考信号分频除以 8
11	设置 PLL 输出分频	PLL 设置 6, 0x30008	0x08	
		PLL_OUT_DIV	0x08	PLL 输出分频除以 8
12	设置 PLL 分频比的小数部分	PLL 设置 2, 0x30002	0x00	
		PLL_DIV_FRAC_0	0x00	
		PLL 设置 3, 0x30003	0xF7	
		PLL_DIV_FRAC_1	0xF7	
		PLL 设置 4, 0x30004	0x06	
		PLL_DIV_FRAC_2	0x06	
13	设置PLL分频比的整数部分	PLL 设置 5, 0x30005	0x44	
		PLL_DIV_INT	0x44	
14	设置 PLL 模式	PLL 设置 8, 0x3001B	0x01	
		保留	0000 00	
		PLL_MODE	0	使用 500/512 因子
		保留	1	
15	设置 PLL 校准比率	PLL 设置 7, 0x3000A	0x8B	
		PLL_CAL_RATIO	0x8B	设置 PLL 校准比率为 139
16	读取中断状态1寄存器 (0xF0000) 以清除所有待处理中断。			
17	启用 PLL 中断	中断屏蔽 1, 0xF0010	0xE1	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	1	
		HPDETECT_UNPLUG_INT_MASK	1	启用 PLL 就绪和错误中断
		XTAL_READY_INT_MASK	0	
		XTAL_ERROR_INT_MASK	0	
		PLL_READY_INT_MASK	0	
		PLL_ERROR_INT_MASK	0	
		PDN_DONE_INT_MASK	1	
18	启动 PLL	PLL 设置 1, 0x30001	0x01	
		保留	0000 000	
		PLL_START	1	启动 PLL
19	配置 DSDIF 以播放 64·Fs DSD 流	DSDIF 配置为从属模式		
20	配置 DSD 音量	DSD 音量 A, 0x70001	0x00	
		DSD_VOLUME_A	0x00	通道 A 音量设置为 0dB
21	配置 DSD 路径信号 控制1	DSD处理器路径信号控制1 0x70002	0xCC	
		DSD_RAMP_UP	1	
		DSD_VOL_BEQA	1	DSD音量B等于DSD音量A
		DSD_SZC	0	立即更改
		保留	0	
		DSD_AMUTE	1	静音在256次重复的8位DSD静音模式后发生
		DSD_AMUTE_BEQA	1	仅当两个通道均检测到静音模式时才触发静音
		DSD静音A	0	功能已禁用
		DSD静音B	0	功能已禁用

Example 5-11. Startup to DSD Playback in Mono Mode (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
22	Configure DSD Interface	DSD Interface Configuration. 0x70003	0x00	
		Reserved	0000 0	
		DSD_M/SB	0	DSD is clock slave
		DSD_PM_EN	0	Function is disabled
		DSD_PM_SEL	0	Function is disabled
23	Configure DSD path Signal Control 2	DSD Processor Path Signal Control 2. 0x70004	0x13	
		Reserved	0	
		DSD_PRC_SRC	00	Set source of DSD processor to DSDIF
		DSD_EN	1	Enable DSD playback
		Reserved	0	
		DSD_SPEED	0	Set DSD clock speed to 64•FS
		STA_DSD_DET	1	Static DSD detection enabled
		INV_DSD_DET	1	Invalid DSD detection enabled
24	Configure DSD path Signal Control 3.	DSD Processor Path Signal Control 3. 0xC5/0xC7 for Left/Right channel 0x70006		
	Enable mono mode:	DSD_ZERO_DB	1	The SACD 0-dB reference level (50% modulation index) matches PCM 0-dB full scale.
a.	Select Channel A/B (DSD_SWAP_CHAN)	DSD_HPF_EN	1	Enable HPF in DSD processor
b.	Copy Channel A to B (DSD_COPY_CHAN)	Reserved	0	
c.	Invert Channel B (DSD_INV_B)	SIGCTL_DSDEQPCM	0	Function is disabled
		DSD_INV_A	0	Function is disabled
		DSD_INV_B	1	Function is enabled
		DSD_SWAP_CHAN	0/1	Function is enabled/disabled
		DSD_COPY_CHAN	1	Function is enabled
25	Configure HP			
26	Configure Class H Amplifier	Class H Control. 0xB0000	0x1E	
		Reserved	000	
		ADPT_PWR	111	Output signal determines voltage level
		HV_EN	1	High Voltage Mode Enabled
		EXT_VCPFILT	0	Using Internal VCPFILT source.
27	Set HP output to full scale	HP Output Control 1. 0x80000	0x30	
		HP_CLAMPA	0	
		HP_CLAMPB	0	
		OUT_FS	11	Set headphone output to Full Scale (1.732 V rms)
		HP_IN_EN	0	
		HP_IN_LP	0	
		Reserved	0	
		+1dB_EN	0	
28	Configure Headphone Detect	HP Detect. 0xD0000	0x04	
		HPDETECT_CTRL	00	HP detect disabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	0 0	Tip Sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
29	Headphone Detect	HP Detect. 0xD0000	0xC4	
		HPDETECT_CTRL	11	HP detect enabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	0 0	Tip sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
30	Enable Interrupts			
31	Read Interrupt Status 1 register (0xF0000) and Interrupt Status 5 register (0xF0004) to clear sticky bits			
32	Enable Headphone Detect Interrupts	Interrupt Mask 1. 0xF0010	0x81	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	0	Unmask HPDETECT_PLUG interrupt and
		HPDETECT_UNPLUG_INT_MASK	0	HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	0	
		XTAL_ERROR_INT_MASK	0	
		PLL_READY_INT_MASK	0	
		PLL_ERROR_INT_MASK	0	
		PDN_DONE_INT_MASK	1	
33	Enable DSD Interrupts	Interrupt Mask 5. 0xF0014	0x03	
		DSD_STUCK_INT_MASK	0	Enable DSD_STUCK interrupt
		DSD_INVAL_A_INT_MASK	0	Enable DSD_INVAL_A interrupt
		DSD_INVAL_B_INT_MASK	0	Enable DSD_INVAL_B interrupt
		DSD_SILENCE_A_INT_MASK	0	Enable DSD_SILENCE_A interrupt
		DSD_SILENCE_B_INT_MASK	0	Enable DSD_SILENCE_B interrupt
		DSD_RATE_ERROR_INT_MASK	0	Enable DSD_RATE_ERROR interrupt
		DOP_MRK_DET_INT_MASK	1	Disable DOP_MRK_DET interrupt
		DOP_ON_INT_MASK	1	Disable DOP_ON interrupt
34	Wait for interrupt. Check if PLL_READY_INT = 1 in Interrupt Status 1 register(0xF0000)			

示例 5-11。启动至单声道模式下的 DSD 播放 (续)

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
22	配置DSD接口	DSD接口配置。0x70003 0x00 保留 DSD_M/S		
		B_DSD_P	0000 0	
		M_EN_DSD	0	DSD为时钟从属
		_PM_SEL	0	功能已禁用
			0	功能已禁用
23	配置DSD路径信号控制 ₂	0x7004 DSD处理器路径信号控制2。	0x13	
		保留	0	
		DSD_PRC_SRC	00	将DSD处理器源设置为DSDIF
		DSD_EN	1	启用DSD播放
		保留	0	
		DSD_SPEED	0	将DSD时钟速度设置为64·FS
		STA_DSD_DET	1	启用静态DSD检测
		INV_DSD_DET	1	启用无效DSD检测
24	配置 DSD 路径信号控制 3。 启用单声道模式： a. 选择通道 A/B (DSD_SWAP_CHAN) b. 复制通道 A 至 B (DSD_COPY_CHAN) c. 反转通道 B (DSD_INV_B)	0x7006 DSD处理器路径信号控制3。	左/右通道对应 0xC5/0xC7	
		DSD_ZERO_DB	1	SACD 0 dB参考电平 (50% 调制指数) 与 PCM 0 dB满量程相匹配。
		DSD_HPF_EN	1	启用DSD处理器中的高通滤波器
		保留	0	
		SIGCTL_DSDEQPCM	0	功能已禁用
		DSD_INV_A	0	功能已禁用
		DSD_INV_B	1	功能已启用
		DSD_SWAP_CHAN	0/1	功能已启用/禁用
		DSD_COPY_CHAN	1	功能已启用
25	配置耳机			
26	配置 Class H 放大器 Class H 控制。0xB0000		0x1E	
		保留	000	
		ADPT_PWR	111	输出信号决定电压等级
		HV_EN	1	启用高压模式
		EXT_VCPFILT	0	使用内部VCPFILT源
27	将耳机输出设置为满量程	耳机输出控制 1, 0x80000	0x30	
		HP_CLAMPA	0	
		HP_CLAMPB	0	
		OUT_FS	11	将耳机输出设置为满量程 (1.732 V rms)
		HP_IN_EN	0	
		HP_IN_LP	0	
		保留	0	
		+1dB_EN	0	
28	配置耳机检测耳机检测。0xD0000		0x04	
		HPDETECT_CTRL	00	耳机检测已禁用
		HPDETECT_IN	0	耳机检测输入未反相
		V_HPDETECT_RISE_DBC_T1	0 0	Tip Sense 上升沿消抖时间设置为 0 毫秒
		ME HPDETECT_FALL_DBC_T	10	Tip 感应下降消抖时间设置为 500 毫秒
		IME 保留	0	
29	耳机检测	耳机检测, 0xD0000	0xC4	
		HPDETECT_CTRL	11	启用耳机检测
		HPDETECT_IN	0	耳机检测输入未反相
		V_HPDETECT_RISE_DBC_T1	0 0	Tip 感应上升消抖时间设置为 0 毫秒
		ME HPDETECT_FALL_DBC_T	10	Tip 感应下降消抖时间设置为 500 毫秒
		IME 保留	0	
30	启用中断			
31	读取中断状态1寄存器 (0xF0000) 和中断状态5寄存器 (0xF0004) 以清除粘滞位			
32	启用耳机检测中断	中断屏蔽 1, 0xF0010	0x81	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	0	取消屏蔽HPDETECT_PLUG中断和HPDETECT_UNPLUG中断
		HPDETECT_UNPLUG_INT_MASK	0	
		XTAL_READY_INT_MASK	0	
		XTAL_ERROR_INT_MASK	0	
		PLL_READY_INT_MASK	0	
		PLL_ERROR_INT_MASK	0	
		PDN_DONE_INT_MASK	1	
33	启用DSD中断	中断屏蔽5, 0xF0014	0x03	
		DSD_STUCK_INT_MASK	0	启用DSD_STUCK中断
		DSD_INVAL_A_INT_MASK	0	使能 DSD_INVAL_A 中断
		DSD_INVAL_B_INT_MASK	0	使能 DSD_INVAL_B 中断
		DSD_SILENCE_A_INT_MASK	0	使能 DSD_SILENCE_A 中断
		DSD_SILENCE_B_INT_MASK	0	使能 DSD_SILENCE_B 中断
		DSD_RATE_ERROR_INT_MASK	0	使能 DSD_RATE_ERROR 中断
		DOP_MRK_DET_INT_MASK	1	禁用 DOP_MRK_DET 中断
		DOP_ON_INT_MASK	1	禁用 DOP_ON 中断
34	等待中断。检查中断状态寄存器 1 (0xF0000) 中 PLL_READY_INT 是否为 1			

Example 5-11. Startup to DSD Playback in Mono Mode (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
35	Switch MCLK source to PLL	System Clocking Control 1. 0x10006	0x01	
		Reserved	0000 0	
		MCLK_INT	0	MCLK Source set to PLL. MCLK_INT frequency set to
		MCLK_SRC_SEL	01	24.576 MHz
36	Wait at least 150 µs.			
37	Power up HP	Refer to Ex. 5-6 for DSD power-up sequence. Note that in Step 1 of Ex. 5-6 , use HH = DF for the DSD interface.		

5.13.6 Power-Up Sequence to DoP Playback with PLL in Mono Mode

In [Ex. 5-9](#), an external 19.2-MHz MCLK is used with a PLL to generate an internal MCLK or 22.5792 MHz, and the ASP is in clock master receiving DoP data with LRCLK at 176.4 kHz and SCLK at 8.4672 MHz.

Example 5-12. DoP Playback with PLL in Mono Mode

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Apply all relevant power supplies, then assert RESET.			
2	Wait for 1.5 ms.			
3	Configure PLL. XT/I/MCLK input coming from an external 19.2 MHz source with PLL output set to 22.5792 MHz. Refer to Section 4.7.2 for register settings for other frequency combinations			
4	Power up PLL	Power Down Control. 0x20000	0xFA	
		PDN_XSP	x	
		PDN_ASP	x	
		PDN_DSDIF	x	
		PDN_HP	x	
		PDN_XTAL	x	
		PDN_PLL	0	Power up PLL block
		PDN_CLKOUT	x	
		Reserved	0	
5	Set PLL Predivide value	PLL Setting 9. 0x40002	0x03	
		Reserved	0000 00	
		PLL_REF_PREDIV	11	Set PLL predivide value to 8
6	Set PLL output divide	PLL Setting 6. 0x30008	0x08	
		PLL_OUT_DIV	0x08	Set PLL output divide value to 8
7	Set Fractional portion of PLL Divide Ratio	PLL Setting 2. 0x30002	0x00	
		PLL_DIV_FRAC_0	0x00	Set LSB of PLL fractional divider value to 0
		PLL Setting 3. 0x30003	0x00	
		PLL_DIV_FRAC_1	0x00	Set Middle Byte of PLL fractional divider value to 0
		PLL Setting 4. 0x30004	0x80	
		PLL_DIV_FRAC_2	0x80	Set MSB of PLL fractional divider value to 0x80
8	Set Integer portion of PLL Divide Ratio	PLL Setting 5. 0x30005	0x49	
		PLL_DIV_INT	0x49	Set PLL integer Divide value to 0x49
9	Set PLL mode	PLL Setting 8. 0x3001B	0x01	
		Reserved	0000 00	
		PLL_MODE	0	500/512 factor is used in PLL frequency calculation
		Reserved	1	
10	Read Interrupt Status 1 register (0xF0000) to clear sticky bits.			
11	Set PLL calibration ratio	PLL Setting 7. 0x3000A	0x97	
		PLL_CAL_RATIO	0x97	PLL Calibration Ratio is set to 0x97 (151)
12	Enable PLL interrupts	Interrupt Mask 1. 0xF0010	0xF9	
		DAC_OVFL_INT_MASK	1	DAC_OVFL_INT is don't care
		HPDETECT_PLUG_INT_MASK	1	Unmask HPDETECT_PLUG interrupt
		HPDETECT_UNPLUG_INT_MASK	1	Unmask HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	1	XTAL_READY_INT is Don't Care
		XTAL_ERROR_INT_MASK	1	XTAL_ERROR_INT is Don't Care
		PLL_READY_INT_MASK	0	PLL_READY Interrupt is already unmasked
		PLL_ERROR_INT_MASK	0	PLL_ERROR Interrupt is already unmasked
		PDN_DONE_INT_MASK	1	PDN_DONE_INT is Don't Care
13	Start PLL	PLL Setting 1. 0x30001	0x01	
		Reserved	0000 000	
		PLL_START	1	Enable PLL Output
14	Playback DoP audio. Assuming 64•Fs DSD stream			
15	Configure ASP interface for DoP input			
16	Set ASP sample rate	Serial Port Sample Rate. 0x1000B	0x05	
		Reserved	0000	
		ASP_SPRATE	0101	Set sample rate to 176.4 kHz

示例 5-11。启动至单声道模式下的 DSD 播放 (续)

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
35	切换 MCLK 源至 PLL 系统时钟控制 1。0x10006 0x01 保留	MCLK_INT MCLK_SRC_SEL	0000 0 010	MCLK 源设置为 PLL, MCLK_INT 频率设置为 24.576 MHz
36	等待至少 150 μs。			
37	上电耳机驱动器			有关 DSD 上电顺序, 请参见示例 5-6。注意, 在示例 5-6 的步骤 1 中, DSD 接口使用 HH = DF。

5.13.6 单声道模式下带 PLL 的 DoP 播放上电序列

在示例 5-9 中, 外部 19.2 MHz MCLK 与 PLL 配合使用, 生成内部 MCLK 或 22.5792 MHz, ASP 作为时钟主设备接收 DoP 数据, LRCLK 为 176.4 kHz, SCLK 为 8.4672 MHz。

示例 5-12。单声道模式下带 PLL 的 DoP 播放

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	施加所有相关电源, 然后断言复位。			
2	等待1.5毫秒。			
3	配置 PLL。XTI/MCLK 输入来自外部 19.2 MHz 信号, PLL 输出设置为 22.5792 MHz。其他频率组合的寄存器设置详见第 4.7.2 节			
4	PLL上电。	关断控制, 0x20000	0xFA	
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT 保留	x x x x x 0 x 0	启动 PLL 模块
5	设置 PLL 预分频值	PLL 设置 9, 0x40002	0x03	
		保留 PLL_REF_PREDIV	0000 00 11	将 PLL 预分频值设置为 8
6	设置 PLL 输出分频值	PLL 设置 6, 0x30008	0x08	
		PLL_OUT_DIV	0x08	将 PLL 输出分频值设置为 8
7	设置 PLL 分频比的小数部分	PLL 设置 2, 0x30002	0x00	
		PLL_DIV_FRAC_0 PLL 设置 3, 0x30003 PLL_DIV_FRAC_1 PLL 设置 4, 0x30004 PLL_DIV_FRAC_2	0x00 0x00 0x00 0x80 0x80	将 PLL 小数分频器最低有效位设置为 0 将 PLL 小数分频器中间字节设置为 0 将 PLL 小数分频器最高有效位设置为 0x80
8	设置 PLL 分频比的整数部分	PLL 设置 5, 0x30005	0x49	
		PLL_DIV_INT	0x49	将 PLL 整数分频值设置为 0x49
9	设置 PLL 模式	PLL 设置 8, 0x3001B	0x01	
		保留 PLL_MODE 保留	0000 00 0 1	PLL 频率计算中采用 500/512 因子
10	读取中断状态寄存器1 (0xF0000) 以清除粘滞位。			
11	设置PLL校准比率	PLL 设置 7, 0x3000A	0x97	
		PLL_CAL_RATIO		PLL校准比率设置为0x97 (151)
12	使能PLL中断	中断屏蔽 1, 0xF0010	0xF9	
		DAC_OVFL_INT_MASK HPDETECT_PLUG_INT_MASK HPDETECT_UNPLUG_INT_MASK XTAL_READY_INT_MASK XTAL_ERROR_INT_MASK PLL_READY_INT_MASK PLL_ERROR_INT_MASK PDN_DONE_INT_MASK	1 1 1 1 1 0 0 1	DAC_OVFL_INT 为无关状态 取消屏蔽HPDETECT_PLUG中断 取消屏蔽HPDETECT_UNPLUG中断 XTAL_READY_INT 为无关状态 XTAL_ERROR_INT 为无关状态 PLL_READY_INT 中断已取消屏蔽 PLL_ERROR_INT 中断已取消屏蔽 PDN_DONE_INT 为无关状态
13	启动 PLL	PLL 设置 1, 0x30001	0x01	
		保留 PLL_START	0000 0000 1	使能PLL输出
14	播放DoP音频。假设64•Fs的DSD流			
15	配置ASP接口以支持DoP输入			
16	设置 ASP 采样率	串口采样率。0x1000B 0x05		
		保留 ASP_SPRATE	0000 0101	设置采样率为 176.4 kHz

Example 5-12. DoP Playback with PLL in Mono Mode (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
17	Set ASP sample bit size. XSP is don't care	Serial Port Sample Bit Size. 0x1000C	0x05	
		Reserved	0000	
		XSP_SPSIZE	01	XSP sample bit size set to 24 bits
		ASP_SPSIZE	01	ASP sample bit size set to 24 bits
18	Set ASP numerator	ASP Numerator 1. 0x40010	0x03	
		ASP_N_LSB	0x03	LSB of ASP sample rate fractional divide numerator
		ASP Numerator 2. 0x40011	0x00	
		ASP_N_MSB	0x00	MSB of ASP sample rate fractional divide numerator
19	Set ASP denominator	ASP Denominator 1. 0x40012	0x08	
		ASP_M_LSB	0x08	LSB of ASP sample rate fractional divide denominator
		ASP Denominator 2. 0x40013	0x00	
		ASP_M_MSB	0x00	MSB of ASP sample rate fractional divide denominator
20	Set ASP LRCK high time	ASP LRCK High Time 1. 0x40014	0x17	
		ASP_LCHI_LSB	0x17	LSB of ASP LRCK high time duration
		ASP LRCK High Time 2. 0x40015	0x00	
		ASP_LCHI_MSB	0x00	MSB of ASP LRCK high time duration
21	Set ASP LRCK period	ASP LRCK Period 1. 0x40016	0x2F	
		ASP_LCPRI_LSB	0x2F	LSB of ASP LRCK period
		ASP LRCK Period 2. 0x40017	0x00	
		ASP_LCPRI_MSB	0x00	MSB of ASP LRCK period
22	Configure ASP clock	ASP Clock Configuration. 0x40018	0x1C	
		Reserved	000	
		ASP_M/SB	1	Set ASP port to be Master
		ASP_SCPOL_OUT	1	Set output SCLK polarity
		ASP_SCPOL_IN	1	Input SCLK polarity is don't care
		ASP_LCPOL_OUT	0	Set Output LRCK polarity
		ASP_LCPOL_IN	0	Input LRCK polarity is don't care
23	Configure ASP frame	ASP Frame Configuration. 0x40019	0x0A	
		Reserved	000	
		ASP_STP	0	
		ASP_5050	1	Configure ASP port to accept I2S input
		ASP_FSD	010	
24	Set ASP channel location	ASP Channel 1 Location. 0x50000	0x00	
		ASP_RX_CH1	0x00	ASP Channel 1 starts on SCLK0
		ASP Channel 2 Location. 0x50001	0x00	
		ASP_RX_CH2	0x00	ASP Channel 2 starts on SCLK0
25	Set ASP channel size and enable	ASP Channel 1 Size and Enable. 0x5000A	0x06	
		Reserved	0000	
		ASP_RX_CH1_AP	0	ASP Channel 1 active phase
		ASP_RX_CH1_EN	1	ASP Channel 1 enable
		ASP_RX_CH1_RES	10	ASP Channel 1 size is 24 bits
		ASP Channel 2 Size and Enable. 0x5000B	0x0E	
		Reserved	0000	
		ASP_RX_CH2_AP	1	ASP Channel 2 active phase
		ASP_RX_CH2_EN	1	ASP Channel 2 enable
		ASP_RX_CH2_RES	10	ASP Channel 2 size is 24 bits
26	Wait for interrupt. Check if PLL_READY_INT = 1 in Interrupt Status 1 register(0xF0000).			
27	Configure DSD processor			
28	Configure DSD volume	DSD Volume A. 0x70001	0x00	
		DSD_VOLUME_A	0x00	Channel A volume set to 0 dB
29	Configure DSD Path Signal Control 1	DSD Processor Path Signal Control 1. 0x70002	0xCC	
		DSD_RAMP_UP	1	
		DSD_VOL_BEQA	1	DSD Volume B equals DSD volume A
		DSD_SZC	0	Immediate change
		Reserved	0	
		DSD_AMUTE	1	Mute occurs after 256 repeated 8-bit DSD mute patterns
		DSD_AMUTE_BEQA	1	Mute happens only when mute pattern is detected in both channels
		DSD_MUTE_A	0	Function is disabled
		DSD_MUTE_B	0	Function is disabled

示例 5-12。单声道模式下带 PLL 的 DoP 播放 (续)

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
17	设置 ASP 采样位宽XSP 不关心串口采样位宽。0x1000C 0x05 保留	XSP_SPSIZE ASP_SPSIZE	0000 01 01	XSP 采样位宽设置为 24 位 ASP 采样位宽设置为 24 位
18	设置 ASP 分子	ASP 分子 1, 地址 0x40010 ASP_N_LSB	0x03 0x03	ASP 采样率分数分子最低有效位
		ASP 分子 2, 地址 0x40011 ASP_N_MSB	0x00 0x00	ASP 采样率分数分子最高有效位
19	设置 ASP 分母	ASP 分母 1。0x40012 ASP_M_LSB	0x08 0x08	ASP 采样率分数分母最低有效位
		ASP 分母 2, 地址 0x40013 ASP_M_MSB	0x00 0x00	ASP 采样率分数分母最高有效位
20	设置 ASP LRCK 高电平时间	ASP_LRCK 高电平时间 1。0x40014 ASP_LCHI_LSB	0x17 0x17	ASP_LRCK 高电平时间持续最低有效位
		ASP_LRCK 高电平时间 2. 0x40015 ASP_LCHI_MSB	0x00 0x00	ASP_LRCK 高电平时间持续时长最高有效位
21	设置 ASP LRCK 周期	ASP_LRCK 周期 1. 0x40016 ASP_LCPY_LSB	0x2F 0x2F	ASP_LRCK 周期的最低有效位
		ASP_LRCK 周期 2. 0x40017 ASP_LCPY_MSB	0x00 0x00	ASP_LRCK 周期的最高有效位
22	配置 ASP 时钟	ASP 时钟配置. 0x40018 保留 ASP_M/SB ASP_SCPOL_OUT ASP_SCPOL_IN ASP_LCPOL_OUT ASP_LCPOL_IN	0x1C 000 1 1 1 0 0	0x1C 设置 ASP 端口为主设备 设置输出 SCLK 极性 输入 SCLK 极性不关心 设置输出 LRCK 极性 输入 LRCK 极性不关心
23	配置 ASP 帧格式	ASP 帧格式配置. 0x40019 保留 STP ASP 5050 AS P_FSD	0x0A 000 0 1 010	保留 设置 ASP 端口以接收 I2S 输入
24	设置 ASP 通道位置	ASP 通道 1 位置. 0x50000 ASP_RX_CH1 ASP 通道 2 位置. 0x50001 ASP_RX_CH2	0x00 0x00 0x00 0x00	0x00 0x00 ASP 通道 1 从 SCLK0 开始 0x00 ASP 通道 2 从 SCLK0 开始
25	设置 ASP 通道大小及使能	ASP 通道 1 大小及使能。 0x5000A 保留 ASP_RX_CH1_AP ASP_RX_CH1_EN ASP_RX_CH1_RES	0x06 0000 0 1 10	0x06 设置 ASP 通道 1 有效相位 ASP 通道 1 使能 ASP 通道 1 大小为 24 位
		ASP 通道 2 大小及使能。 0x5000B 保留 ASP_RX_CH2_AP ASP_RX_CH2_EN ASP_RX_CH2_RES	0x0E 0000 1 1 10	0x0E 设置 ASP 通道 2 有效相位 ASP 通道 2 使能 ASP 通道 2 大小为 24 位
26	等待中断。检查中断状态寄存器 1 (0xF0000) 中 PLL_READY_INT 是否为 1。			
27	配置 DSD 处理器			
28	配置 DSD 音量	DSD 音量 A, 0x70001 DSD_VOLUME_A	0x00 0x00	0x00 通道 A 音量设置为 0 dB
29	配置 DSD 路径信号控制 1	DSD 信号路径控制字控制 1。 0x70002 DSD_RAMP_UP DSD_VOL_BEQA DSD_SZC 保留 DSD_AMUTE	0xCC 1 1 0 0 1	0xCC 立即更改 DSD 音量 B 等于 DSD 音量 A 静音发生在重复 256 次 8 位 DSD 静音模式后 仅当两个通道均检测到静音模式时才发生静音
		DSD_AMUTE_BEQA DSD 静音 A DSD 静音 B	1 0 0	功能已禁用 功能已禁用

Example 5-12. DoP Playback with PLL in Mono Mode (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
30	Configure DSD interface	DSD Interface Configuration. 0x70003	0x04	
		Reserved	0000 0	
		DSD_M/SB	1	DSD is clock master
		DSD_PM_EN	0	Function is disabled
		DSD_PM_SEL	0	Function is disabled
31	Configure DSD Path Signal Control 2	DSD Processor Path Signal Control 2. 0x70004	0x50	
		Reserved	0	
		DSD_PRC_SRC	10	Set source of DSD processor to ASP
		DSD_EN	1	Enable DSD playback
		Reserved	0	
		DSD_SPEED	0	Set DSD clock speed to 64·Fs
		STA_DSD_DET	0	Static DSD detection disabled
		INV_DSD_DET	0	Invalid DSD detection disabled
32	Configure DSD path Signal Control 3.	DSD Processor Path Signal Control 3. 0xC5/0xC7 for Left/Right channel 0x70006		
	Enable mono mode:			
a.	Select Channel A/B (DSD_SWAP_CHAN)	DSD_ZERObdb	1	The SACD 0-dB reference level (50% modulation index) matches PCM 0-dB full scale.
b.	Copy Channel A to B (DSD_COPY_CHAN)	DSD_HPF_EN	1	Enable HPF in DSD processor
c.	Invert Channel B (DSD_INV_B)	Reserved	0	
		SIGCTL_DSDEQPCM	0	Function is disabled
		DSD_INV_A	0	Function is disabled
		DSD_INV_B	1	Function is enabled
		DSD_SWAP_CHAN	0/1	Function is enabled/disabled
		DSD_COPY_CHAN	1	Function is enabled
33	Configure headphone output for 1.732 V rms			
34	Configure Class H amplifier	Class H Control. 0xB0000	0x1E	
		Reserved	000	
		ADPT_PWR	1 11	Output signal determines voltage level
		HV_EN	1	High voltage mode enabled
		EXT_VCPFILT	0	Using internal VCPFILT source.
35	Set HP output to full scale	HP Output Control 1. 0x80000	0x30	
		HP_CLAMPA	0	
		HP_CLAMPB	0	
		OUT_FS	11	Set headphone output to full scale (1.732 V rms)
		HP_IN_EN	0	
		HP_IN_LP	0	
		Reserved	0	
		+1dB_EN	0	
36	Headphone detect	HP Detect. 0xD0000	0xC4	
		HPDETECT_CTRL	11	HP detect enabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	0 0	Tip Sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
37	Enable interrupts			
38	Read Interrupt Status 1 register (0xF0000), Interrupt Status 2 register (0xF0001) and Interrupt Status 5 register (0xF0004) to clear sticky bits.			
39	Enable headphone detect interrupts	Interrupt Mask 1. 0xF0010	0x99	
		DAC_OVFL_INT_MASK	1	DAC_OVFL_INT is don't care
		HPDETECT_PLUG_INT_MASK	0	Enable HPDETECT_PLUG interrupt
		HPDETECT_UNPLUG_INT_MASK	0	Enable HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	1	XTAL_READY_INT is don't care
		XTAL_ERROR_INT_MASK	1	XTAL_ERROR_INT is don't care
		PLL_READY_INT_MASK	0	PLL_READY_INTERRUPT already enabled
		PLL_ERROR_INT_MASK	0	PLL_ERROR_INTERRUPT already enabled
		PDN_DONE_INT_MASK	1	PDN_DONE_INT is don't care
40	Enable ASP interrupts	Interrupt Mask 2. 0xF0011	0x07	
		ASP_OVFL_INT_MASK	0	Enable ASP_OVFL_INTERRUPT
		ASP_ERROR_INT_MASK	0	Enable ASP_ERROR_INTERRUPT
		ASP_LATE_INT_MASK	0	Enable ASP_LATE_INTERRUPT
		ASP_EARLY_INT_MASK	0	Enable ASP_EARLY_INTERRUPT
		ASP_NOLRCK_INT_MASK	0	Enable ASP_NOLRCK_INTERRUPT
		Reserved	111	
41	Enable DSD and DoP interrupts	Interrupt Mask 5. 0xF0014	0x01	
		DSD_STUCK_INT_MASK	0	Enable DSD_STUCK_INTERRUPT
		DSD_INVAL_A_INT_MASK	0	Enable DSD_INVAL_A_INTERRUPT
		DSD_INVAL_B_INT_MASK	0	Enable DSD_INVAL_B_INTERRUPT
		DSD_SILENCE_A_INT_MASK	0	Enable DSD_SILENCE_A_INTERRUPT
		DSD_SILENCE_B_INT_MASK	0	Enable DSD_SILENCE_B_INTERRUPT
		DSD_RATE_ERROR_INT_MASK	0	Enable DSD_RATE_ERROR_INTERRUPT
		DOP_MRK_DET_INT_MASK	0	Enable DOP_MRK_DET_INTERRUPT
		DOP_ON_INT_MASK	1	Disable DOP_ON_INTERRUPT

示例 5-12。单声道模式下带 PLL 的 DoP 播放 (续)

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
30 配置DSD接口	DSD接口配置。 0x70003		0x04	
	保留	0000 0		
	DSD_M/SB	1	DSD为时钟主控	
	DSD_PM_EN	0	功能已禁用	
	DSD_PM_SEL	0	功能已禁用	
31 配置DSD路径信号控制2	DSD处理器路径信号控制。 0x70004		0x50	
	保留	0		
	DSD_PRC_SRC	10	将DSD处理器源设置为ASP	
	DSD_EN	1	启用DSD播放	
	保留	0		
	DSD_SPEED	0	将DSD时钟速度设置为64·Fs	
	STA_DSD_DET	0	禁用静态DSD检测	
	INV_DSD_DET	0	禁用无效DSD检测	
32 配置 DSD 路径信号控制 3。	DSD 处理器路径信号控制 3。 0x70006		左/右通道对应 0xC5/0xC7	
启用单声道模式：				
a. 选择通道 A/B (DSD_SWAP_CHAN)	DSD_ZERO_DB	1	SACD 0 dB参考电平 (50% 调制指数) 与 PCM 0 dB满量程相匹配。	
b. 复制通道 A 至 B (DSD_COPY_CHAN)	DSD_HPF_EN	1	启用DSD处理器中的高通滤波器	
c. 反转通道 B (DSD_INV_B)	保留	0		
	SIGCTL_DSDEQPCM	0	功能已禁用	
	DSD_INV_A	0	功能已禁用	
	DSD_INV_B	1	功能已启用	
	DSD_SWAP_CHAN	0/1	功能已启用/禁用	
	DSD_COPY_CHAN	1	功能已启用	
33 配置耳机输出为1.732 V rms	Class H 控制。0xB0000		0x1E	
34 配置 Class H 放大器				
	保留	000		
	ADPT_PWR	1 11	输出信号决定电压等级	
	HV_EN	1	高电压模式已启用	
	EXT_VCPFILT	0	使用内部 VCPFILT 源。	
35 将耳机输出设置为满量程	耳机输出控制 1, 0x80000		0x30	
	HP_CLAMP_A	0		
	HP_CLAMP_B	0		
	OUT_FS	11	将耳机输出设置为满量程 (1.732 V rms)	
	HP_IN_EN	0		
	HP_IN_LP	0		
	保留	0		
	+1dB_EN	0		
36 耳机检测	耳机检测, 0xD0000		0xC4	
	HPDETECT_CTRL	11	启用耳机检测	
	HPDETECT_IN	0	耳机检测输入未反相	
	V HPDETECT_RISE_DBC_TI	0 0	Tip Sense上升沿消抖时间设置为0毫秒	
	ME HPDETECT_FALL_DBC_T	10	Tip 感应下降消抖时间设置为 500 毫秒	
	IME 保留	0		
37 启用中断				
38 读取中断状态寄存器 1 (0xF0000)、中断状态寄存器 2 (0xF0001) 和中断状态寄存器 5 (0xF0004) 以清除粘滞位。				
39 启用耳机检测中断	中断屏蔽 1, 0xF0010		0x99	
	DAC_OVFL_INT_MASK	1	DAC_OVFL_INT 为无关状态	
	HPDETECT_PLUG_INT_MASK	0	启用HPDETECT_PLUG中断	
	HPDETECT_UNPLUG_INT_MASK	0	启用HPDETECT_UNPLUG中断	
	XTAL_READY_INT_MASK	1	XTAL_READY_INT 不关心	
	XTAL_ERROR_INT_MASK	1	XTAL_ERROR_INT 不关心	
	PLL_READY_INT_MASK	0	PLL_READY 中断已启用	
	PLL_ERROR_INT_MASK	0	PLL_ERROR 中断已启用	
	PDN_DONE_INT_MASK	1	PDN_DONE_INT 不关心	
40 启用 ASP 中断	中断屏蔽 2, 0xF0011		0x07	
	ASP_OVFL_INT_MASK	0	启用ASP_OVFL中断	
	ASP_ERROR_INT_MASK	0	启用ASP_ERROR中断	
	K ASP_LATE_INT_MASK	0	启用ASP_LATE中断	
	SK ASP_EARLY_INT_MASK	0	启用ASP_EARLY中断	
	ASK ASP_NOLRCK_INT_MASK	0	启用ASP_NOLRCK中断	
	保留	111		
41 启用 DSD 和 DoP 中断	中断屏蔽5, 0xF0014		0x01	
	DSD_STUCK_INT_MASK	0	启用DSD_STUCK中断	
	DSD_INVAL_A_INT_MASK	0	使能 DSD_INVAL_A 中断	
	DSD_INVAL_B_INT_MASK	0	使能 DSD_INVAL_B 中断	
	DSD_SILENCE_A_INT_MASK	0	使能 DSD_SILENCE_A 中断	
	DSD_SILENCE_B_INT_MASK	0	使能 DSD_SILENCE_B 中断	
	DSD_RATE_ERROR_INT_MASK	0	使能 DSD_RATE_ERROR 中断	
	DOP_MRK_DET_INT_MASK	0	启用 DOP_MRK_DET 中断	
	DOP_ON_INT_MASK	1	禁用 DOP_ON 中断	

Example 5-12. DoP Playback with PLL in Mono Mode (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
42	Wait for interrupt. Check if PLL_READY_INT = 1 in Interrupt Status 1 register(0xF0000).			
43	Set MCLK source and frequency	System Clocking Control. 0x10006	0x05	
		Reserved	0000 0	
		MCLK_INT	1	MCLK Frequency is set to 22.5792 MHz
		MCLK_SRC_SEL	01	MCLK Source is set to PLL
44	Wait for at least 150 µs.			
45	Enable ASP clocks	Pad Interface Configuration. 0x1000D	0x02	
		Reserved	0000 00	
		XSP_3ST	1	XSP Interface status is don't care (set to default)
		ASP_3ST	0	Enable serial clocks in Master Mode
46	Power up HP	Refer to Ex. 5-6 for DSD power-up sequence. Note that in Step 1 of Ex. 5-6 , use HH = BF for DoP over ASP interface.		

5.13.7 Analog-In Startup

[Ex. 5-13](#) shows an example sequence of starting up the CS43131 in analog passthrough mode.

Example 5-13. Start Up to Analog-In

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Apply all relevant power supplies, then assert RESET.			
2	Wait for 1.5 ms. MCLK Source is set to RCO by default.			
3	Enable Headphone detect. Refer to Section 5.13.11 "Headphone Detection"			
4	Enable HPINx path. Refer to Section 5.5.1 "HPINx Alternate Headphone Path Enable Sequence"			

5.13.8 Switching from Analog-In to PCM Playback

[Ex. 5-14](#) assumes that:

- The CS43131 is powered up, out of reset, and is currently operating in analog passthrough mode as in [Ex. 5-13](#).
- The ASP and PCM interfaces are not yet configured.
- CS43131 XTI/XTO is connected to a 22.5792-MHz crystal.
- ASP interface is slave.

Example 5-14. Switching from Analog-In to PCM Playback

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Configure XTAL driver.			
2	Configure XTAL bias current strength (assuming River Crystal at 22.5792 MHz)	Crystal Setting. 0x20052 Reserved XTAL_IBIAS	0x04 0000 0 100	Bias current set to 12.5 µA
3	Read Interrupt Status 1 register (0xF0000) to clear sticky bits.			
4	Enable XTAL interrupts	Interrupt Mask 1. 0xF0010 DAC_OVFL_INT_MASK HPDETECT_PLUG_INT_MASK HPDETECT_UNPLUG_INT_MASK XTAL_READY_INT_MASK XTAL_ERROR_INT_MASK PLL_READY_INT_MASK PLL_ERROR_INT_MASK PDN_DONE_INT_MASK	data(0xF0010) AND 0xE7 x x x 0 0 x x x x	Enable XTAL_READY interrupt Enable XTAL_ERROR interrupt
5	Start XTAL	Power Down Control. 0x20000 PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT Reserved	data(0x20000) AND 0xF6 x x x x 0 x x 0	Power up XTAL driver
6	Configure ASP interface. Sample rate set to 44.1 kHz. ASP is slave to incoming clock.			
7	Set ASP sample rate	Serial Port Sample Rate. 0x1000B Reserved ASP_SPRATE	0x01 0000 0001	Set sample rate to 44.1 kHz

示例 5-12。单声道模式下带 PLL 的 DoP 播放 (续)

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
42	等待中断。检查中断状态寄存器 1 (0xF0000) 中 PLL_READY_INT 是否为 1。			
43	设置 MCLK 源和频率	系统时钟控制。0x10006 0x05		
		保留	0000 0	
		MCLK_INT	1	MCLK 频率设置为 22.5792 MHz
		MCLK_SRC_SEL	01	MCLK 源设置为 PLL
44	等待至少 150 μs。			
45	启用ASP时钟。	引脚接口配置。0x1000D 0x02		
		保留	0000 00	
		XSP_3ST	1	XSP 接口状态无关 (设置为默认)
		ASP_3ST	0	主模式下启用串行时钟。
46	耳机供电开启	有关 DSD 上电顺序, 请参见示例 5-6。注意, 在示例 5-6 的步骤 1 中, ASP 接口上的 DoP 使用 H = BF。		

5.13.7 模拟输入启动

示例 5-13 展示了 CS43131 在模拟直通模式下的启动示例序列。

示例 5-13 启动至模拟输入

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	施加所有相关电源, 然后断言复位。			
2	等待 1.5 毫秒。MCLK 源默认设置为 RCO。			
3	启用耳机检测。参见第 5.13.11 节“耳机检测”			
4	启用 HPINx 路径。参见第 5.5.1 节“HPINx 备用耳机路径启用顺序”			

5.13.8 从模拟输入切换至 PCM 播放

示例 5-14 假设:

- CS43131 已上电, 已完成复位, 当前如示例 5-13 所示运行于模拟直通模式。
- ASP 和 PCM 接口尚未配置。
- CS43131 XTI/XTO 连接至 22.5792 MHz 晶体。
- ASP 接口为从属模式。

示例 5-14 从模拟输入切换至 PCM 播放

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	配置晶体振荡器驱动。			
2	配置晶体振荡器偏置电流强度 (假设River Crystal为22.5792 MHz)。	晶体设置。0x20052 保留 晶体振荡器偏置电流	0x04 0000 0 100	偏置电流设置为 12.5 μA。
3	读取中断状态寄存器1 (0xF0000) 以清除粘滞位。			
4	启用晶体振荡器中断。	中断屏蔽 1, 0xF0010	数据(0xF0010) 与 0xE7 进行 AND 运算	
		DAC_OVFL_INT_MASK HPDETECT_PLUG_INT_MASK HPDETECT_UNPLUG_INT_MASK XTAL_READY_INT_MASK XTAL_ERROR_INT_MASK PLL_READY_INT_MASK PLL_ERROR_INT_MASK PDN_DONE_INT_MASK	x x x 0 0 x x x	启用晶体振荡器就绪中断 启用晶体振荡器错误中断 晶体振荡器驱动器上电
5	启动晶体振荡器	关断控制, 0x20000	数据 (0x20000) 与 0xF6 进行 AND 运算	
		PDN_XSP PDN_ASP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT 保留	x x x x 0 x x 0	
6	配置ASP接口。采样率设置为 44.1 kHz。ASP 为输入时钟的从属。			
7	设置 ASP 采样率	串行端口采样率。0x1000B 保留 ASP采样率	0x01 0000 0001	设置采样率为 44.1 kHz

Example 5-14. Switching from Analog-In to PCM Playback (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
8	Set ASP sample bit size. XSP is don't care	Serial Port Sample Bit Size. 0x1000C	0x04	
		Reserved	0000	
		XSP_SPSIZE	01	XSP sample bit size is don't care
		ASP_SPSIZE	00	ASP sample bit size set to 32 bits
9	Set ASP numerator	ASP Numerator 1. 0x40010	0x01	
		ASP_N_LSB	0x01	LSB of ASP sample rate fractional divide numerator
		ASP Numerator 2. 0x40011	0x00	
		ASP_N_MSB	0x00	MSB of ASP sample rate fractional divide numerator
10	Set ASP denominator	ASP Denominator 1. 0x40012	0x08	
		ASP_M_LSB	0x08	LSB of ASP sample rate fractional divide denominator
		ASP Denominator 2. 0x40013	0x00	
		ASP_M_MSB	0x00	MSB of ASP sample rate fractional divide denominator
11	Set ASP LRCK high time	ASP LRCK High Time 1. 0x40014	0x1F	
		ASP_LCHI_LSB	0x1F	LSB of ASP LRCK high time duration
		ASP LRCK High Time 2. 0x40015	0x00	
		ASP_LCHI_MSB	0x00	MSB of ASP LRCK high time duration
12	Set ASP LRCK period	ASP LRCK Period 1. 0x40016	0x3F	
		ASP_LCPRI_LSB	0x3F	LSB of ASP LRCK period
		ASP LRCK Period 2. 0x40017	0x00	
		ASP_LCPRI_MSB	0x00	MSB of ASP LRCK period
13	Configure ASP clock	ASP Clock Configuration. 0x40018	0x0C	
		Reserved	000	
		ASP_M/SB	0	Set ASP port to be Slave
		ASP_SCPOL_OUT	1	Configure clock polarity for I ² S input
		ASP_SCPOL_IN	1	
		ASP_LCPOL_OUT	0	
		ASP_LCPOL_IN	0	
14	Configure ASP frame	ASP Frame Configuration. 0x40019	0x0A	
		Reserved	000	Configure ASP port to accept I ² S input
		ASP_STP	0	
		ASP_5050	1	
		ASP_FSD	010	
15	Set ASP channel location	ASP Channel 1 Location. 0x50000	0x00	
		ASP_RX_CH1	0x00	ASP Channel 1 starts on SCLK0
		ASP Channel 2 Location. 0x50001	0x00	
		ASP_RX_CH2	0x00	ASP Channel 2 starts on SCLK0
16	Set ASP channel size and enable	ASP Channel 1 Size and Enable. 0x5000A	0x07	
		Reserved	0000	
		ASP_RX_CH1_AP	0	ASP Channel 1 active phase
		ASP_RX_CH1_EN	1	ASP Channel 1 enable
		ASP_RX_CH1_RES	11	ASP Channel 1 size is 32 bits
		ASP Channel 2 Size and Enable. 0x5000B	0x0F	
		Reserved	0000	
		ASP_RX_CH2_AP	1	ASP Channel 2 active phase
		ASP_RX_CH2_EN	1	ASP Channel 2 enable
		ASP_RX_CH2_RES	11	ASP Channel 2 size is 32 bits
17	Configure PCM interface. HPF filter is used. Deemphasis off.			
18	Configure PCM Filter	PCM Filter Option. 0x90000	0x02	
		FILTER_SLOW_FASTB	0	
		PHCOMP_LOWLATB	0	
		NOS	0	
		Reserved	00	
		PCM_WBF_EN	0	
		HIGH_PASS	1	High Pass Filter is selected
		DEEMP_ON	0	
19	Set Volume for Channel B	PCM Volume B. 0x90001	0x00	
		PCM_VOLUME_B	0x00	Set volume to 0 dB
20	Set Volume for Channel A	PCM Volume A. 0x90002	0x00	
		PCM_VOLUME_A	0x00	Set volume to 0 dB

示例 5-14 从模拟输入切换至 PCM 播放 (续)

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
8	设置 ASP 采样位宽。ASP 为无关状态	串行端口采样位宽。0x1000C	0x04	
		保留	0000	
		XSP_SPSIZE	01	XSP采样位宽无关
		ASP_SPSIZE	00	ASP采样位宽设置为32位
9	设置 ASP 分子	ASP分子1, 地址0x40010	0x01	
		ASP_N_LSB	0x01	ASP采样率分数分子最低有效位
		ASP分子2, 地址0x40011	0x00	
		ASP_N_MSB	0x00	ASP采样率分数分子最高有效位
10	设置 ASP 分母	ASP分母1。0x40012	0x08	
		ASP_M_LSB	0x08	ASP采样率分数分母最低有效位
		ASP分母2, 地址0x40013	0x00	
		ASP_M_MSB	0x00	ASP采样率分数分母最高有效位
11	设置 ASP LRCK 高电平时间	ASP LRCK高电平时间1, 地址0x40014	0x1F	
		ASP_LCHI_LSB	0x1F	ASP LRCK高电平时间持续最低有效位
		ASP LRCK 高电平时间2, 地址0x40015	0x00	
		ASP_LCHI_MSB	0x00	ASP LRCK高电平时间持续最高有效位
12	设置 ASP LRCK 周期	ASP LRCK 周期1. 0x40016	0x3F	
		ASP_LCPRLSB	0x3F	ASP LRCK周期最低有效位
		ASP LRCK 周期2. 0x40017	0x00	
		ASP_LCPR_MSB	0x00	ASP LRCK周期最高有效位
13	配置 ASP 时钟	ASP时钟配置, 地址0x40018	0x0C	
		保留 ASP	000	
		M/SB AS	0	设置ASP端口为从属模式
		P_SCPOL_OUT A	1	配置I ² S输入的时钟极性
		SP_SCPOL_IN	1	
		ASP_LCPOL_OUT	0	
		ASP_LCPOL_IN	0	
14	配置 ASP 帧格式	ASP帧配置, 地址0x40019	0x0A	
		保留	000	配置ASP端口以接收I ² S输入
		ASP_STP	0	
		ASP_5050	1	
		ASP_FSD	010	
15	设置 ASP 通道位置	ASP通道1位置, 地址0x50000	0x00	
		ASP_RX_CH1	0x00	ASP通道1从SCLK0开始
		ASP通道2位置。0x50001	0x00	
		ASP_RX_CH2	0x00	ASP通道2从SCLK0开始
16	设置 ASP 通道大小并启用 ASP 通道1 大小及启用	0x5000A	0x07	
		保留	0000	
		ASP_RX_CH1_AP	0	ASP通道1有效相位
		ASP_RX_CH1_EN	1	ASP通道1使能
		ASP_RX_CH1_RES	11	ASP通道1大小为32位
		ASP通道2大小及使能。0x5000B	0x0F	
		保留	0000	
		ASP_RX_CH2_AP	1	ASP通道2有效相位
		ASP_RX_CH2_EN	1	ASP通道2使能
		ASP_RX_CH2_RES	11	ASP通道2大小为32位
17	配置 PCM 接口, 使用高通滤波器, 取消预加重			
18	配置 PCM 滤波器	PCM滤波器选项。0x90000	0x02	
		FILTER_SLOW_FASTB	0	
		PHCOMP_LOWLATB	0	
		NOS	0	
		保留	00	
		PCM_WBF_EN	0	
		HIGH_PASS	1	选择高通滤波器
		DEEMP_ON	0	
19	设置通道 B 音量	PCM音量B, 0x90001	0x00	
		PCM_VOLUME_B	0x00	将音量设置为0dB
20	设置通道 A 音量	PCM音量A, 0x90002	0x00	
		PCM_VOLUME_A	0x00	将音量设置为0dB

Example 5-14. Switching from Analog-In to PCM Playback (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
21	Configure PCM Path Signal Control	PCM Path Signal Control 1. 0x90003	0xEC	
		PCM_RAMP_DOWN	1	Soft ramp down of volume on filter change
		PCM_VOL_BEQA	1	Volume setting on both channels controlled by PCM_VOLUME_A
		PCM_SZC	10	Enable soft ramp
		PCM_AMUTE	1	Mute after reception of 8192 samples of 0 or -1.
		PCM_AMUTEBEQA	1	Mute only when AMUTE condition is detected on both channels
		PCM_MUTE_A	0	Function is disabled
		PCM_MUTE_B	0	Function is disabled
		PCM Path Signal Control 2. 0x90004	0x00	
		Reserved	0000	Disable all functions in this register
		PCM_INV_A	0	
		PCM_INV_B	0	
		PCM_SWAP_CHAN	0	
		PCM_COPY_CHAN	0	
22	Configure HP interface			
23	Configure Class H Amplifier	Class H Control. 0xB0000	0x1E	
		Reserved	000	
		ADPT_PWR	111	Output signal determines voltage level
		HV_EN	1	High voltage mode enabled
		EXT_VCPFILT	0	Using Internal VCPFILT source.
24	Headphone Detect	HP Detect. 0xD0000	0xC4	
		HPDETECT_CTRL	11	HP Detect enabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	00	Tip Sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
25	Enable interrupts			
26	Read Interrupt Status 1 register (0xF0000) and Interrupt Status 2 register (0xF0001) to clear sticky bits.			
27	Enable headphone detect interrupts	Interrupt Mask 1. 0xF0010	data(0xF0010) AND 0x9F	
		DAC_OVFL_INT_MASK	x	
		HPDETECT_PLUG_INT_MASK	0	Enable HPDETECT_PLUG interrupt
		HPDETECT_UNPLUG_INT_MASK	0	Enable HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	x	
		XTAL_ERROR_INT_MASK	x	
		PLL_READY_INT_MASK	x	
		PLL_ERROR_INT_MASK	x	
		PDN_DONE_INT_MASK	x	
28	Enable ASP interrupts	Interrupt Mask 2. 0xF0011	0x07	
		ASP_OVFL_INT_MASK	0	Enable ASP_OVFL interrupt
		ASP_ERROR_INT_MASK	0	Enable ASP_ERROR interrupt
		ASP_LATE_INT_MASK	0	Enable ASP_LATE interrupt
		ASP_EARLY_INT_MASK	0	Enable ASP_EARLY interrupt
		ASP_NOLRCK_INT_MASK	0	Enable ASP_NOLRCK interrupt
		Reserved	111	
29	Initiate a soft ramp down of HPINx input to mute.			
30	Disable HPINx	Refer to Section 5.5.2		
31	Wait for interrupt. Check if XTAL_READY_INT = 1 in Interrupt Status 1 register(0xF0000).			
32	Switch MCLK source to XTAL	System Clocking Control 1. 0x10006	0x04	
		Reserved	0000 0	
		MCLK_INT	1	MCLK Source set to XTAL. MCLK_INT frequency set
		MCLK_SRC_SEL	00	to 22.5792MHz
33	Wait at least 150 µs.			
34	Power up ASP	Power Down Control. 0x20000	0xB6	
		PDN_XSP	1	
		PDN_ASP	0	Enable ASP data pins
		PDN_DSDIF	1	XTAL is already enabled
		PDN_HP	1	
		PDN_XTAL	0	
		PDN_PLL	1	
		PDN_CLKOUT	1	
		Reserved	0	
35	Power up HP	Refer to Ex. 5-5 for PCM power-up sequence		

示例 5-14 从模拟输入切换至 PCM 播放 (续)

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
21	控制配置 PCM 路径信号	PCM路径信号控制1, 地址0x90003	0xEC	
		PCM_RAMP_DOWN	1	滤波器切换时音量软降
		PCM_VOL_BEQA	1	两个通道的音量设置由 PCM_VOLUME_A 控制
		PCM_SZC	10	启用软斜坡
		PCM_AMUTE	1	接收 8192 个值为 0 或 -1 的样本后静音
		PCM_AMUTEBEQA	1	仅当两个通道均检测到 AMUTE 条件时静音
		PCM_MUTE_A	0	功能已禁用
		PCM_MUTE_B	0	功能已禁用
		PCM路径信号控制2, 地址0x90004	0x00	
		保留	0000	禁用此寄存器中的所有功能
		PCM_INV_A	0	
		PCM_INV_B	0	
		PCM_SWAP_CHAN	0	
		PCM_COPY_CHAN	0	
22	配置耳机接口			
23	配置Class H放大器Class H控制。	0xB0000	0x1E	
		保留	000	
		ADPT_PWR	111	输出信号决定电压等级
		HV_EN	1	高压模式已启用
		EXT_VCPFILT	0	使用内部VCPFILT源
24	耳机检测	耳机检测, 0xD0000	0xC4	
		HPDETECT_CTRL	11	启用耳机检测
		HPDETECT_IN	0	耳机检测输入未反相
		V HPDETECT_RISE_DBC TI	0 0	Tip Sense上升沿消抖时间设置为0毫秒
		ME HPDETECT_FALL_DBC_T	10	Tip 感应下降消抖时间设置为 500 毫秒
		IME 保留	0	
25	启用中断			
26	读取中断状态寄存器1 (0xF0000) 和中断状态寄存器2 (0xF0001) 以清除粘滞位。			
27	使能耳机检测中断	中断屏蔽 1, 0xF0010	数据(0xF0010) 与 0x9F 进行 AND 运算	
		DAC_OVFL_INT_MASK	x	
		HPDETECT_PLUG_INT_MASK	0	启用HPDETECT_PLUG中断
		HPDETECT_UNPLUG_INT_MASK	0	启用HPDETECT_UNPLUG中断
		XTAL_READY_INT_MASK	x	
		XTAL_ERROR_INT_MASK	x	
		PLL_READY_INT_MASK	x	
		PLL_ERROR_INT_MASK	x	
		PDN_DONE_INT_MASK	x	
28	启用 ASP 中断	中断屏蔽 2。0xF0011	0x07	
		ASP_OVFL_INT_MASK	0	启用ASP_OVFL中断
		ASP_ERROR_INT_MASK	0	启用ASP_ERROR中断
		K ASP_LATE_INT_MASK	0	启用ASP_LATE中断
		SK ASP_EARLY_INT_MASK	0	启用ASP_EARLY中断
		ASK ASP_NOLRCK_INT_MASK 保留	111	启用ASP_NOLRCK中断
29	启动 HPINx 输入的软降音以实现静音			
30	禁用 HPINx	参见第 5.5.2 节		
31	等待中断。检查中断状态寄存器 1 (0xF0000) 中的 XTAL_READY_INT 是否为 1。			
32	切换 MCLK 源至 XTAL 系统时钟控制 1, 地址 0x10006		0x04	
		保留	0000 0	
		MCLK_INT	1	MCLK 源设置为 XTAL, MCLK_INT 频率设置为 22.5792MH
		MCLK_SRC_SEL	00 z	
33	等待至少 150 μs。			
34	上电 ASP	关断控制, 0x20000	0xB6	
		PDN_XSP	1	
		PDN_ASP	0	启用 ASP 数据引脚
		PDN_DSDIF	1	XTAL 已启用
		PDN_HP	1	
		PDN_XTAL	0	
		PDN_PLL	1	
		PDN_CLKOUT	1	
		保留	0	
35	耳机供电开启	参见示例5-5的PCM上电顺序。		

5.13.9 Switching from PCM to Analog-In Playback

Ex. 5-15 makes the following assumptions:

- The CS43131 is powered up, out of reset, and currently operating in PCM playback mode.
- A headphone is connected to the headphone jack.
- Headphone detect is enabled and HPDETECT_PLUG_INT = 1.
- XTAL is used as MCLK source.

Example 5-15. Switching from PCM to Analog-In Playback

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Enable soft ramp	PCM Path Signal Control 1. 0x90003	data(0x90003) OR (0xA0)	
		PCM_RAMP_DOWN	1	Enable soft ramp
		PCM_VOL_BEQA	x	
		PCM_SZC	10	
		PCM_AMUTE	x	
		PCM_AMUTEBEQA	x	
		PCM_MUTE_A	0	
		PCM_MUTE_B	0	
2	PCM Power Down Sequence	Refer to Section 5.6.1		
3	Set MCLK Source to RCO	System Clocking Control 1. 0x10006	0x06	
		Reserved	0000 0	
		MCLK_INT	1	Frequency of MCLK_INT is don't care
		MCLK_SRC_SEL	10	MCLK source set to RCO
4	Wait for 150 µs.			
5	Power down crystal	Power Down Control. 0x20000	data (0x20000) OR (0x08)	
		PDN_XSP	x	
		PDN_ASP	1	ASP already powered down
		PDN_DSDIF	x	
		PDN_HP	1	HP already powered down
		PDN_XTAL	1	Power down XTAL.
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	0	
6	Enable HPINx	Refer to Section 5.5.1		

5.13.9 从 PCM 切换至模拟输入播放

示例 5-15 假设如下：

- CS43131 已上电，复位完成，当前处于 PCM 播放模式。
- 耳机已连接至耳机插孔。
- 耳机检测已启用，且 HPDETECT_PLUG_INT = 1。
- XTAL 用作 MCLK 源。

示例 5-15。从 PCM 切换至模拟输入播放

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	启用软斜坡	PCM 路径信号控制 1, 地址 0x90003, 数据 (0x90003) 或 (0xA0)		
		PCM_RAMP_DOWN	1	启用软斜坡
		PCM_VOL_BEQA	x	
		PCM_SZC	10	
		PCM_AMUTE	x	
		PCM_AMUTEBEQA	x	
		PCM_MUTE_A	0	
		PCM_MUTE_B	0	
2	PCM 断电顺序 参见第 5.6.1 节			
3	将 MCLK 源设置为 RCO 系统时钟控制 1, 0x10006		0x06	
		保留	0000 0	
		MCLK_INT	1	MCLK_INT 频率不关心
		MCLK_SRC_SEL	10	MCLK 源设置为 RCO
4	等待 150 μs。			
5	关闭晶体振荡器电源	关断控制, 0x20000	数据 (0x20000) 或 (0x08)	
		PDN_XSP	x	
		PDN_ASP	1	ASP 已断电
		PDN_DSDIF	x	
		PDN_HP	1	耳机已断电
		PDN_XTAL	1	关闭晶体振荡器电源。
		PDN_PLL	x	
		PDN_CLKOUT	x	
		保留	0	
6	使能 HPINx	参见第 5.5.1 节		

5.13.10 Switching MCLK Frequency

Ex. 5-16 shows steps necessary to switch the MCLK frequency in order to play audio at a different sample rate that is no longer an integer divide of current MCLK. It makes the following assumptions:

- The CS43131 is already powered up and out of reset.
- MCLK_INT is 22.5792 MHz, and the sample rate is an integer divide of MCLK.
- ASP is used for audio delivery and PDN_HP = 0.

Example 5-16. Sequence for Switching MCLK Frequency

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Power down PCM	Refer to Ex. 5-3 for PCM power-down sequence		
2	Switch MCLK Source to RCO			
3	Set MCLK Source to RCO	System Clocking Control 1. 0x10006	0x06	
		Reserved	0000 0	
		MCLK_INT	1	Frequency of MCLK_INT is don't care
		MCLK_SRC_SEL	10	MCLK source set to RCO
4	Wait for 150 µs.			
5	Switch to a different MCLK Frequency. Assuming new MCLK frequency is 24.576MHz.			
6	Change MCLK_INT frequency to 24.576 MHz	System Clocking Control 1. 0x10006	0x02	
		Reserved	0000 0	
		MCLK_INT	0	MCLK_INT frequency set to 24.576 MHz
		MCLK_SRC_SEL	10	
7	Configure ASP for appropriate sample rate, bit size and clock mode. Unmute PCM CHA and CHB outputs. Enable appropriate interrupts			
8	Switch MCLK source to direct MCLK mode	System Clocking Control 1. 0x10006	0x0	
		Reserved	0000 0	
		MCLK_INT	0	MCLK_INT frequency set to 24.576 MHz
		MCLK_SRC_SEL	00	MCLK source set to direct MCLK mode
9	Wait at least 150 µs.			
10	Power up ASP	Power Down Control. 0x20000	data(0x20000) AND (0xBF)	
		PDN_XSP	x	
		PDN_ASP	0	Enable ASP data pins
		PDN_DSDIF	x	
		PDN_HP	1	
		PDN_XTAL	0	XTAL is already enabled
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	0	
11	Power up HP	Refer to Ex. 5-5 for PCM power-up sequence		

5.13.11 Headphone Detection

Ex. 5-17 shows steps necessary to detect the presence of a headphone. It makes the following assumptions:

- The CS43131 is already powered up and out of reset.
- The HP Detect register is not configured.

Example 5-17. Sequence for Headphone Detection

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Read Interrupt Status 1 register (0xF0000) to clear any sticky bits.			
2	Read HP Status register (0xD0001) to clear any sticky bits.			
3	Enable HPDETECT interrupts	Interrupt Mask 1. 0xF0010	data (0xF0010) AND 0x9F	
		DAC_OVFL_INT_MASK	x	
		HPDETECT_PLUG_INT_MASK	0	Enable HPDETECT interrupts
		HPDETECT_UNPLUG_INT_MASK	0	
		XTAL_READY_INT_MASK	x	
		XTAL_ERROR_INT_MASK	x	
		PLL_READY_INT_MASK	x	
		PLL_ERROR_INT_MASK	x	
		PDN_DONE_INT_MASK	x	
4	Configure HP Detect parameters	HP Detect. 0xD0000	0x04	
		HPDETECT_CTRL	00	
		HPDETECT_INV	0	
		HPDETECT_RISE_DBC_TIME	0 0	Rising edge debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Falling edge debounce time set to 500 ms
		Reserved	0	

5.13.10 切换 MCLK 频率

示例 5-16 显示了切换 MCLK 频率以播放不同采样率音频所需的步骤，该采样率不再是当前 MCLK 的整数分频。假设如下：

- CS43131 已上电且已退出复位状态。
- MCLK_INT 为 22.5792 MHz，采样率为 MCLK 的整数分频。
- ASP 用于音频传输且 PDN_HP = 0。

示例 5-16。切换 MCLK 频率的流程

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	关闭 PCM 电源	有关 PCM 关闭电源的流程，请参见示例 5-3		
2	将 MCLK 源切换至 RCO			
3	设置 MCLK 源为 RCO	系统时钟控制 1, 地址 0x10006, 值 0x06		
		保留	0000 0	
		MCLK_INT	1	MCLK_INT 频率为无关参数
		MCLK_SRC_SEL	10	MCLK 源设置为 RCO
4	等待 150 μs。			
5	切换至不同的 MCLK 频率，假设新频率为 24.576 MHz。			
6	将 MCLK_INT 频率更改为 24.576 MHz	系统时钟控制 1, 地址 0x10006, 值 0x02		
		保留	0000 0	
		MCLK_INT	0	MCLK_INT 频率设置为 24.576 MHz
		MCLK_SRC_SEL	10	
7	配置 ASP 以匹配适当的采样率、位宽和时钟模式。取消静音 PCM CHA 和 CHB 输出。启用相应中断			
8	切换 MCLK 源至直接 MCLK 模式，系统时钟控制 1, 地址 0x10006		0x0	
		保留	0000 0	
		MCLK_INT	0	MCLK_INT 频率设置为 24.576 MHz
		MCLK_SRC_SEL	00	MCLK 源设置为直接 MCLK 模式
9	等待至少 150 μs。			
10	上电 ASP	关断控制, 0x20000	数据(0x20000) 与 (0xBF)	
		PDN_XSP	x	
		PDN_ASP	0	启用 ASP 数据引脚
		PDN_DSDIF	x	
		PDN_HP	1	
		PDN_XTAL	0	晶体振荡器已启用
		PDN_PLL	x	
		PDN_CLKOUT	x	
		保留	0	
11	耳机供电开启	参见示例 5-5 的 PCM 上电顺序。		

5.13.11 耳机检测

示例 5-17 展示了检测耳机存在所需的步骤。假设如下：

- CS43131 已上电且已退出复位状态。
- HP Detect 寄存器未配置。

示例 5-17。耳机检测序列

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	读取中断状态 1 寄存器 (0xF0000) 以清除所有粘滞位。			
2	读取耳机状态寄存器 (0xD0001) 以清除所有粘滞位。			
3	启用耳机检测中断	中断屏蔽 1, 0xF0010	数据 (0xF0010) 与 0x9F 进行 AND 运算	
		DAC_OVFL_INT_MASK	x	
		HPDETECT_PLUG_INT_MASK	0	启用耳机检测中断
		HPDETECT_UNPLUG_INT_MASK	0	
		XTAL_READY_INT_MASK	x	
		XTAL_ERROR_INT_MASK	x	
		PLL_READY_INT_MASK	x	
		PLL_ERROR_INT_MASK	x	
		PDN_DONE_INT_MASK	x	
4	配置耳机检测参数	耳机检测, 0xD0000	0x04	
		HPDETECT_CTRL	00	
		HPDETECT_IN	0	
		V_HPDETECT_RISE_DBC_T1	0 0	上升沿消抖时间设置为 0 毫秒
		ME_HPDETECT_FALL_DBC_T1	10	下降沿消抖时间设置为 500 毫秒
		IME 保留	0	

Example 5-17. Sequence for Headphone Detection (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
5	Enable HP Detect	HP Detect. 0xD0000	data (0xD0000) OR (0xC0)	
		HPDETECT_CTRL	11	Enable headphone detection
		HPDETECT_INV	x	
		HPDETECT_RISE_DBC_TIME	xx	
		HPDETECT_FALL_DBC_TIME	xx	
		Reserved	0	
6	Wait for interrupt. Check if HPDETECT_PLUG_INT or HPDETECT_UNPLUG_INT is set in the Interrupt Status 1 register (0xF0000).			

5.13.12 DoP and PCM Mixing

[Ex. 5-18](#) shows steps necessary to mix DoP and PCM. The XSP is in clock master receiving DoP data with LRCLK at 176.4 kHz and SCLK at 8.4672 MHz. The ASP is clock master receiving PCM data with LRCLK at 44.1 kHz and SCLK at 2.8224 MHz.

Example 5-18. DoP and PCM Mixing

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Apply all relevant power supplies, then assert RESET.			
2	Wait for 1.5 ms			
3	Configure XTAL Driver			
4	Configure XTAL_bias current strength (assuming River Crystal at 22.5792 MHz)	Crystal Setting. 0x20052 Reserved XTAL_IBIAS	0x04 0000 0 100	Bias current set to 12.5 µA
5	Enable XTAL interrupts	Interrupt Mask 1. 0xF0010 DAC_OVFL_INT_MASK HPDETECT_PLUG_INT_MASK HPDETECT_UNPLUG_INT_MASK XTAL_READY_INT_MASK XTAL_ERROR_INT_MASK PLL_READY_INT_MASK PLL_ERROR_INT_MASK PDN_DONE_INT_MASK	0xE7 1 1 1 0 0 1 1 1	Enable XTAL_READY interrupt Enable XTAL_ERROR interrupt
6	Start XTAL	Power Down Control. 0x20000 PDN_XSP PDN_XSP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT Reserved	0xF6 1 1 1 1 0 1 1 0	Power up XTAL driver
7	Playback DoP audio. Assuming 64•Fs DSD stream			
8	Configure XSP interface for DoP input.			
9	Set sample bit size.	Serial Port Sample Bit Size. 0x1000C Reserved XSP_SPSIZE ASP_SPSIZE	0x05 0000 01 01	XSP sample bit size is set to 24 bits ASP sample bit size is set to 24 bits
10	Set XSP Numerator	XSP Numerator 1. 0x40020 XSP_N_LSB XSP Numerator 2. 0x40021 XSP_N_MSB	0x03 0x03 0x00 0x00	LSB of XSP sample rate fractional divide numerator MSB of XSP sample rate fractional divide numerator
11	Set XSP Denominator	XSP Denominator 1. 0x40022 XSP_M_LSB XSP Denominator 2. 0x40023 XSP_M_MSB	0x08 0x08 0x00 0x00	LSB of XSP sample rate fractional divide denominator MSB of XSP sample rate fractional divide denominator
12	Set XSP LRCK high Time	XSP_LRCK_High_Time 1. 0x40024 XSP_LCHI_LSB XSP_LRCK_High_Time 2. 0x40025 XSP_LCHI_MSB	0x17 0x17 0x00 0x00	LSB of XSP LRCK high time duration MSB of XSP LRCK high time duration
13	Set XSP LRCK period	XSP_LRCK_Period 1. 0x40026 XSP_LCPR_LSB XSP_LRCK_Period 2. 0x40027 XSP_LCPR_MSB	0x2F 0x2F 0x00 0x00	LSB of XSP LRCK period MSB of XSP LRCK period

示例5-17。耳机检测序列（续）

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
5	启用耳机检测	耳机检测, 0xD0000	数据(0xD0000) 或(0xC0)	
		HPDETECT_CTRL HPDETECT_IN V HPDETECT_RISE_DBC_TI ME HPDETECT_FALL_DBC_T IME 保留	11 x xx xx 0	启用耳机检测功能
6	等待中断。检查中断状态寄存器 1 (0xF0000) 中是否设置了 HPDETECT_PLUG_INT 或 HPDETECT_UNPLUG_INT。			

5.13.12 DoP与PCM混合

示例5-18展示了混合DoP和PCM所需的步骤。XSP作为时钟主控，接收DoP数据，LRCLK为176.4 kHz，SCLK为8.4672 MHz。ASP作为时钟主控，接收PCM数据，LRCLK为44.1 kHz，SCLK为2.8224 MHz。

示例 5-18. DoP 与 PCM 混合

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	施加所有相关电源，然后断言复位。			
2	等待 1.5 毫秒			
3	配置晶体振荡器驱动器			
4	配置晶体振荡器偏置电流强度（假设 River Crystal 频率为 22.5792 MHz）	晶体设置。0x20052 保留 晶体振荡器偏置电流	0x04 0000 0 100	偏置电流设置为 12.5 μA。
5	启用晶体振荡器中断屏蔽1。0xF0010		0xE7	
		DAC_OVFL_INT_MASK HPDETECT_PLUG_INT_MASK HPDETECT_UNPLUG_INT_MASK XTAL_READY_INT_MASK XTAL_ERROR_INT_MASK PLL_READY_INT_MASK PLL_ERROR_INT_MASK PDN_DONE_INT_MASK	1 1 1 0 0 1 1 1	启用晶体振荡器就绪中断 启用晶体振荡器错误中断
6	启动晶体振荡器	关断控制，0x20000	0xF6	
		PDN_XSP PDN_XSP PDN_DSDIF PDN_HP PDN_XTAL PDN_PLL PDN_CLKOUT 保留	1 1 1 1 0 1 1 0	晶体振荡器驱动器上电
7	播放DoP音频。假设64•Fs的DSD流			
8	配置 XSP 接口以支持 DoP 输入。			
9	设置采样位数。	串行端口采样位数。0x1000C 0x05 保留		
		XSP_SPSIZE ASP_SPSIZE	0000 01 01	XSP 采样位数设置为 24 位 ASP 采样位数设置为 24 位
10	设置 XSP 分子	XSP 分子 1。0x40020 XSP_N_LSB	0x03 0x03	XSP 采样率分数除法分子最低有效位
		XSP 分子 2, 0x40021 XSP_N_MSB	0x00 0x00	XSP 采样率分数除法分子最高有效位
11	设置 XSP 分母	XSP 分母 1, 0x40022 XSP_M_LSB	0x08 0x08	XSP 采样率分数除法分母最低有效位
		XSP 分母 2, 0x40023 XSP_M_MSB	0x00 0x00	XSP 采样率分数除法分母最高有效位
12	设置 XSP LRCK 高电平时间	XSP_LRCK 高电平时间 1, 0x40024 0x17 XSP_LCHI LSB	0x17	XSP_LRCK 高电平时间持续的最低有效位
		XSP_LRCK 高电平时间 2, 0x40025 0x00 XSP_LCHI_MSB	0x00	XSP_LRCK 高电平时间持续的最高有效位
13	设置 XSP LRCK 周期	XSP_LRCK 周期 1, 0x40026 XSP_LCPR_LSB	0x2F 0x2F	XSP_LRCK 周期最低有效位
		XSP_LRCK 周期 2, 0x40027 XSP_LCPR_MSB	0x00 0x00	XSP_LRCK 周期的最高有效位

Example 5-18. DoP and PCM Mixing (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
14	Configure XSP Clock	XSP Clock Configuration. 0x40028	0x1C	
		Reserved	000	
		XSP_M/SB	1	Set XSP port to be Master
		XSP_SCPOL_OUT	1	Set output SCLK polarity
		XSP_SCPOL_IN	1	Input SCLK polarity is don't care
		XSP_LCPOL_OUT	0	Set Output LRCLK polarity
		XSP_LCPOL_IN	0	Input LRCLK polarity is don't care
15	Configure XSP Frame	XSP Frame Configuration. 0x40029	0x0A	
		Reserved	000	
		XSP_STP	0	Configure XSP port to accept I2S input
		XSP_5050	1	
		XSP_FSD	010	
16	Set XSP Channel Location	XSP Channel 1 Location. 0x60000	0x00	
		XSP_RX_CH1	0x00	XSP Channel 1 starts on SCLK0
		XSP Channel 2 Location. 0x60001	0x00	
		XSP_RX_CH2	0x00	XSP Channel 2 starts on SCLK0
17	Set XSP Channel Size and Enable	XSP Channel 1 Size and Enable. 0x6000A	0x06	
		Reserved	0000	
		XSP_RX_CH1_AP	0	XSP Channel 1 Active Phase
		XSP_RX_CH1_EN	1	XSP Channel 1 Enable
		XSP_RX_CH1_RES	10	XSP Channel 1 Size is 24 bits
		XSP Channel 2 Size and Enable. 0x6000B	0x0E	
		Reserved	0000	
		XSP_RX_CH2_AP	1	XSP Channel 2 Active Phase
		XSP_RX_CH2_EN	1	XSP Channel 2 Enable
		XSP_RX_CH2_RES	10	XSP Channel 2 Size is 24 bits
18	Configure DSD Processor			
19	Configure DSD Volume	DSD Volume A. 0x70001	0x00	
		DSD_VOLUME_A	0x00	Channel A volume set to 0 dB
20	Configure DSD path Signal Control 1	DSD Processor Path Signal Control 1. 0x70002	0xCC	
		DSD_RAMP_UP	1	
		DSD_VOL_BEQA	1	DSD Volume B equals DSD volume A
		DSD_SZC	0	Immediate change
		Reserved	0	
		DSD_AMUTE	1	Mute occurs after 256 repeated 8-bit DSD mute patterns
		DSD_AMUTE_BEQA	1	Mute happens only when mute pattern is detected in both channels
		DSD_MUTE_A	0	Function is disabled
		DSD_MUTE_B	0	Function is disabled
21	Configure DSD Interface	DSD Interface Configuration. 0x70003	0x00	
		Reserved	0000 0	
		DSD_M/SB	0	DSD_M/SB is don't care
		DSD_PM_EN	0	Function is disabled
		DSD_PM_SEL	0	Function is disabled
22	Configure DSD path Signal Control 2	DSD Processor Path Signal Control 2. 0x70004	0x70	
		Reserved	0	
		DSD_PRC_SRC	11	Set source of DSD processor to XSP
		DSD_EN	1	Enable DSD playback
		Reserved	0	
		DSD_SPEED	0	Set DSD clock speed to 64*FS
		STA_DSD_DET	0	Static DSD detection disabled
		INV_DSD_DET	0	Invalid DSD detection disabled
23	Configure DSD path Signal Control 3	DSD Processor Path Signal Control 3. 0x70006	0xC0	
		DSD_ZEROdB	1	DSD stream volume setting
		DSD_HPF_EN	1	Enable DSD HPF
		Reserved	0	
		SIGCTL_DSDEQPCM	0	Function is disabled
		DSD_INV_A	0	Function is disabled
		DSD_INV_B	0	Function is disabled
		DSD_SWAP_CHAN	0	Function is disabled
		DSD_COPY_CHAN	0	Function is disabled
24	Configure HP Output for 1.732 Vrms			

示例 5-18。DoP 与 PCM 混合（续）

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
14	配置 XSP 时钟	XSP 时钟配置。0x40028 0x1C		
		保留	000	
		XSP_M/SB	1	设置 XSP 端口为主设备
		XSP_SCPOL_OUT	1	设置输出 SCLK 极性
		XSP_LCPOL_IN	1	输入 SCLK 极性不关心
		XSP_LCPOL_OUT	0	设置输出 LRCLK 极性
		XSP_LCPOL_IN	0	输入 LRCLK 极性不关心
15	配置 XSP 帧格式	XSP 帧配置。0x40029 0x0A		
		保留	000	
		XSP_STP	0	配置 XSP 端口以接收 I2S 输入
		XSP_5050	1	
		XSP_FSD	010	
16	设置 XSP 通道位置，XSP 通道 1 位置。0x60000 0x00 XSP_RX_CH1			
			0x00	XSP 通道 1 从 SCLK0 开始
		XSP 通道 2 位置。0x60001 0x00		
			0x00	XSP 通道 2 从 SCLK0 开始
17	启用设置 XSP 通道大小及	XSP 通道 1 大小及启用	0x06	
		0x6000A		
		保留	0000	
		XSP_RX_CH1_AP	0	XSP 通道 1 有效相位
		XSP_RX_CH1_EN	1	XSP 通道 1 使能
		XSP_RX_CH1_RES	10	XSP 通道 1 位宽为 24 位
		XSP 通道 2 位宽及使能	0x0E	
		0x6000B		
		保留	0000	
		XSP_RX_CH2_AP	1	XSP 通道 2 有效相位
		XSP_RX_CH2_EN	1	XSP 通道 2 使能
		XSP_RX_CH2_RES	10	XSP 通道 2 位宽为 24 位
18	配置 DSD 处理器			
19	配置 DSD 音量	DSD 音量 A。0x70001	0x00	
		DSD_VOLUME_A	0x00	通道 A 音量设置为 0 dB
20	控制 1 配置 DSD 路径信号		0xCC	
		DSD_RAMP_UP	1	
		DSD_VOL_BEQA	1	DSD 音量 B 等于 DSD 音量 A
		DSD_SZC	0	立即更改
		保留	0	
		DSD_AMUTE	1	静音在 256 次重复的 8 位 DSD 静音模式后发生
		DSD_AMUTE_BEQA	1	仅当两个通道均检测到静音模式时才触发静音
		DSD 静音 A	0	功能已禁用
		DSD 静音 B	0	功能已禁用
21	配置 DSD 接口	DSD 接口配置。0x70003	0x00	
		保留	0000 0	
		DSD_M/SB	0	DSD M/SB 不关心
		DSD_PM_EN	0	功能已禁用
		DSD_PM_SEL	0	功能已禁用
22	配置 DSD 路径信号控制 2。	0x70004	0x70	
		保留	0	
		DSD_PRC_SRC	11	设置 DSD 处理器源为 XSP
		DSD_EN	1	启用 DSD 播放
		保留	0	
		DSD_SPEED	0	设置 DSD 时钟速度为 64•采样频率
		STA_DSD_DET	0	禁用静态 DSD 检测
		INV_DSD_DET	0	禁用无效 DSD 检测
23	配置 DSD 路径信号控制 3。	0x70006	0xC0	
		DSD_ZERO_DB	1	DSD 流音量设置
		DSD_HPF_E	1	启用 DSD 高通滤波器
		N 保留 SI	0	
		GCTL_DSDEQPCM_D	0	功能已禁用
		SD_INV_A	0	功能已禁用
		DSD_INV	0	功能已禁用
		B_DSD_SWAP_CH	0	功能已禁用
		AN_DSD_COPY_CH	0	功能已禁用
24	配置耳机输出为 1.732 Vrms			

Example 5-18. DoP and PCM Mixing (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
25	Configure Class H Amplifier	Class H Control. 0xB0000	0x1E	
		Reserved	000	
		ADPT_PWR	111	Output Signal determines voltage level
		HV_EN	1	High Voltage Mode enabled
		EXT_VCPFILT	0	Using Internal VCPFILT source.
26	Set HP output to full scale	HP Output Control 1. 0x80000	0x30	
		HP_CLAMPA	0	
		HP_CLAMPB	0	
		OUT_FS	11	Set HP output to Full Scale (1.732 Vrms)
		HP_IN_EN	0	
		HP_IN_LP	0	
		Reserved	0	
		+1dB_EN	0	
27	Headphone Detect	HP Detect. 0xD0000	0xC4	
		HPDETECT_CTRL	11	HP detect enabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	00	Tip Sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
28	Enable Interrupts			
29	Read Interrupt Status 1 register (0xF0000), Interrupt Status 2 register (0xF0001) and Interrupt Status 5 register (0xF0004) to clear sticky bits			
30	Enable Headphone Detect Interrupts	Interrupt Mask 1. 0xF0010	0x99	
		DAC_OVFL_INT_MASK	1	DAC_OVFL_INT is don't care
		HPDETECT_PLUG_INT_MASK	0	Unmask HPDETECT_PLUG interrupt
		HPDETECT_UNPLUG_INT_MASK	0	Unmask HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	1	XTAL_READY_INT is don't care
		XTAL_ERROR_INT_MASK	1	XTAL_ERROR_INT is don't care
		PLL_READY_INT_MASK	0	PLL_READY_INTERRUPT is already unmasked
		PLL_ERROR_INT_MASK	0	PLL_ERROR_INTERRUPT is already unmasked
		PDN_DONE_INT_MASK	1	PDN_DONE_INT is don't care
31	Enable XSP Interrupts	Interrupt Mask 2. 0xF0011	0x07	
		XSP_OVFL_INT_MASK	0	Enable XSP_OVFL interrupt
		XSP_ERROR_INT_MASK	0	Enable XSP_ERROR interrupt
		XSP_LATE_INT_MASK	0	Enable XSP_LATE interrupt
		XSP_EARLY_INT_MASK	0	Enable XSP_EARLY interrupt
		XSP_NOLRCK_INT_MASK	0	Enable XSP_NOLRCK interrupt
		Reserved	111	
32	Enable DSD and DoP Interrupts	Interrupt Mask 5. 0xF0014	0x01	
		DSD_STUCK_INT_MASK	0	Enable DSD_STUCK interrupt
		DSD_INVAL_A_INT_MASK	0	Enable DSD_INVAL_A interrupt
		DSD_INVAL_B_INT_MASK	0	Enable DSD_INVAL_B interrupt
		DSD_SILENCE_A_INT_MASK	0	Enable DSD_SILENCE_A interrupt
		DSD_SILENCE_B_INT_MASK	0	Enable DSD_SILENCE_B interrupt
		DSD_RATE_ERROR_INT_MASK	0	Enable DSD_RATE_ERROR interrupt
		DOP_MRK_DET_INT_MASK	0	Enable DOP_MRK_DET interrupt
		DOP_ON_INT_MASK	1	Disable DOP_ON interrupt
33	Set MCLK Source and Frequency	System Clocking Control. 0x10006	0x04	
		Reserved	0000 0	
		MCLK_INT	1	MCLK Frequency is set to 22.5792 MHz
		MCLK_SRC_SEL	00	MCLK Source is set to XTAL
34	Wait for at least 150 µs			
35	Enable XSP Clocks	Pad Interface Configuration. 0x1000D	0x01	
		Reserved	0000 00	
		XSP_3ST	0	ASP Interface status is don't care (set to default)
		ASP_3ST	1	Enable XSP serial clocks in master mode
36	Enable XSP and CLKOUT	Power Down Control. 0x20000	0x74	
		PDN_XSP	0	Enable XSP Data pins and CLKOUT
		PDN ASP	1	
		PDN_DSDIF	1	
		PDN_HP	1	
		PDN_XTAL	0	XTAL is already enabled
		PDN_PLL	1	
		PDN_CLKOUT	0	
		Reserved	0	
37	Apply the DSD Power-up Sequence in Ex. 5-6. Note that in Step 1 of Ex. 5-6, use HH = 7F for DoP over XSP interface.			
38	Enable ASP			
39	Set ASP sample rate	Serial Port Sample Rate. 0x1000B	0x01	
		Reserved	0000	
		ASP_SPRATE	0001	Set sample rate to 44.1 kHz

示例 5-18。DoP 与 PCM 混合（续）

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
25	配置 Class H 放大器 Class H 控制。0xB0000		0x1E	
	保留	000		
	ADPT_PWR	111		输出信号决定电压等级
	HV_EN	1		启用高电压模式
	EXT_VCPFILT	0		使用内部VCPFILT源
26	设置耳机输出为满量程耳机输出控制 1。0x80000		0x30	
	HP_CLAMPA	0		
	HP_CLAMPB	0		
	OUT_FS	11		设置耳机输出为满量程 (1.732 Vrms)
	HP_IN_EN	0		
	HP_IN_LP	0		
	保留	0		
	+1dB_EN	0		
27	耳机检测	耳机检测, 0xD0000	0xC4	
	HPDETECT_CTRL	11		启用耳机检测
	HPDETECT_IN	0		耳机检测输入未反相
	V HPDETECT_RISE_DBC_TI	00		Tip Sense上升沿消抖时间设置为0毫秒
	ME HPDETECT_FALL_DBC_T	10		Tip 感应下降消抖时间设置为 500 毫秒
	IME 保留	0		
28	启用中断			
29	读取中断状态 1 寄存器 (0xF0000)、中断状态 2 寄存器 (0xF0001) 和中断状态 5 寄存器 (0xF0004) 以清除粘滞位			
30	启用耳机检测 中断	中断屏蔽 1, 0xF0010	0x99	
	DAC_OVFL_INT_MASK	1		DAC_OVFL_INT 不关心
	HPDTECT_PLUG_INT_MASK	0		取消屏蔽HPDTECT_PLUG中断
	HPDTECT_UNPLUG_INT_MASK	0		取消屏蔽HPDTECT_UNPLUG中断
	XTAL_READY_INT_MASK	1		XTAL_READY_INT 不关心
	XTAL_ERROR_INT_MASK	1		XTAL_ERROR_INT 不关心
	PLL_READY_INT_MASK	0		PLL_READY中断已取消屏蔽
	PLL_ERROR_INT_MASK	0		PLL_ERROR中断已取消屏蔽
	PDN_DONE_INT_MASK	1		PDN_DONE_INT 不关心
31	使能 XSP 中断	中断屏蔽 2, 0xF0011	0x07	
	XSP_OVFL_INT_MASK	0		使能 XSP_OVFL 中断
	XSP_ERROR_INT_MASK	0		使能 XSP_ERROR 中断
	XSP_LATE_INT_MASK	0		使能 XSP_LATE 中断
	XSP_EARLY_INT_MASK	0		使能 XSP_EARLY 中断
	XSP_NOLRCK_INT_MASK	0		使能 XSP_NOLRCK 中断
	保留	111		
32	使能 DSD 和 DoP 中断	中断屏蔽5, 0xF0014	0x01	
	DSD_STUCK_INT_MASK	0		启用DSD_STUCK中断
	DSD_INVAL_A_INT_MASK	0		使能DSD_INVAL_A中断
	DSD_INVAL_B_INT_MASK	0		使能DSD_INVAL_B中断
	DSD_SILENCE_A_INT_MASK	0		使能DSD_SILENCE_A中断
	DSD_SILENCE_B_INT_MASK	0		使能DSD_SILENCE_B中断
	DSD_RATE_ERROR_INT_MASK	0		使能DSD_RATE_ERROR中断
	DOP_MRK_DET_INT_MASK	0		启用DOP_MRK_DET中断
	DOP_ON_INT_MASK	1		禁用DOP_ON中断
33	设置 MCLK 源和 频率	系统时钟控制。0x10006 0x04		
	保留	0000 0		
	MCLK_INT	1		MCLK 频率设置为 22.5792 MHz
	MCLK_SRC_SEL	00		MCLK 源设置为晶体振荡器
34	等待至少 150 μs			
35	使能 XSP 时钟	引脚接口配置。0x1000D 0x01		
	保留	0000 00		
	XSP_3ST	0		ASP接口状态为无关 (设置为默认)
	ASP_3ST	1		在主模式下启用XSP串行时钟
36	启用XSP和CLKOUT电源关闭控制。0x20000		0x74	
	PDN_XSP	0		启用XSP数据引脚和CLKOUT
	PDN_ASPI	1		
	PDN_DSDIF	1		
	PDN_HP	1		
	PDN_XTAL	0		晶体振荡器已启用
	PDN_PLL	1		
	PDN_CLKOUT	0		
	保留	0		
37	在示例5-6中应用DSD上电序列。注意，在示例5-6的步骤1中，XSP接口的DoP使用HH = 7F。			
38	启用ASP			
39	设置 ASP 采样率	串口采样率。0x1000B 0x01		
	保留	0000		
	ASP_SPRATE	0001		设置采样率为44.1 kHz

Example 5-18. DoP and PCM Mixing (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
40	Set ASP sample bit size	Serial Port Sample Bit Size. 0x1000C	0x04	
		Reserved	0000	
		XSP_SPSIZE	01	
		ASP_SPSIZE	00	ASP sample bit size set to 32 bits
41	Set ASP Numerator	ASP Numerator 1. 0x40010	0x01	
		ASP_N_LSB	0x01	LSB of ASP sample rate fractional divide numerator
		ASP Numerator 2. 0x40011	0x00	
		ASP_N_MSB	0x00	MSB of ASP sample rate fractional divide numerator
42	Set ASP Denominator	ASP Denominator 1. 0x40012	0x08	
		ASP_M_LSB	0x08	LSB of ASP sample rate fractional divide denominator
		ASP Denominator 2. 0x40013	0x00	
		ASP_M_MSB	0x00	MSB of ASP sample rate fractional divide denominator
43	Set ASP LRCK high Time	ASP LRCK High Time 1. 0x40014	0x1F	
		ASP_LCHI_LSB	0x1F	LSB of ASP LRCK high time duration
		ASP LRCK High Time 2. 0x40015	0x00	
		ASP_LCHI_MSB	0x00	MSB of ASP LRCK high time duration
44	Set ASP LRCK period	ASP LRCK Period 1. 0x40016	0x3F	
		ASP_LCPRI_LSB	0x3F	LSB of ASP LRCK period
		ASP LRCK Period 2. 0x40017	0x00	
		ASP_LCPRI_MSB	0x00	MSB of ASP LRCK period
45	Configure ASP Clock	ASP Clock Configuration. 0x40018	0x1C	
		Reserved	000	
		ASP_M/SB	1	Set ASP port to be Master
		ASP_SCPOL_OUT	1	Set output SCLK polarity
		ASP_SCPOL_IN	1	Input SCLK polarity is don't care
		ASP_LCPOL_OUT	0	Set Output LRCLK polarity
		ASP_LCPOL_IN	0	Input LRCLK polarity is don't care
46	Configure ASP Frame	ASP Frame Configuration. 0x40019	0x0A	
		Reserved	000	Configure ASP port to accept I2S input
		ASP_STP	0	
		ASP_5050	1	
		ASP_FSD	010	
47	Set ASP Channel Location	ASP Channel 1 Location. 0x50000	0x00	
		ASP_RX_CH1	0x00	ASP Channel 1 starts on SCLK0
		ASP Channel 2 Location. 0x50001	0x00	
		ASP_RX_CH2	0x00	ASP Channel 2 starts on SCLK0
48	Set ASP Channel Size and Enable	ASP Channel 1 Size and Enable. 0x5000A	0x07	
		Reserved	0000	
		ASP_RX_CH1_AP	0	ASP Channel 1 Active Phase
		ASP_RX_CH1_EN	1	ASP Channel 1 Enable
		ASP_RX_CH1_RES	11	ASP Channel 1 Size is 32 bits
		ASP Channel 2 Size and Enable. 0x5000B	0x0F	
		Reserved	0000	
		ASP_RX_CH2_AP	1	ASP Channel 2 Active Phase
		ASP_RX_CH2_EN	1	ASP Channel 2 Enable
		ASP_RX_CH2_RES	11	ASP Channel 2 Size is 32 bits
49	Setup PCM			
50	Configure PCM Filter	PCM Filter Option. 0x90000	0x02	
		FILTER_SLOW_FASTB	0	
		PHCOMP_LOWLATB	0	
		NOS	0	
		Reserved	0.0	
		PCM_WBF_EN	0	
		HIGH_PASS	1	High Pass Filter is selected
		DEEMP_ON	0	
51	Set Volume for Channel B	PCM Volume B. 0x90001	0x0C	
		PCM_VOLUME_B	0x0C	Set volume to -6 dB
52	Set Volume for Channel A	PCM Volume A. 0x90002	0x0C	
		PCM_VOLUME_A	0x0C	Set volume to -6 dB

示例 5-18。DoP 与 PCM 混合（续）

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
40	设置ASP采样位数串口采样位数。0x1000C 0x04			
	保留		0000	
	XSP_SPSIZE		01	
	ASP_SPSIZE		00	ASP采样位数设置为32位
41	设置ASP分子	ASP 分子 1, 地址 0x40010	0x01	
	ASP_N_LSB		0x01	ASP 采样率分数除法分子最低有效位
	ASP 分子 2, 地址 0x40011		0x00	
	ASP_N_MSB		0x00	ASP 采样率分数除法分子最高有效位
42	设置ASP分母	ASP 分母 1。0x40012	0x08	
	ASP_M_LSB		0x08	ASP 采样率分数除法分母最低有效位
	ASP 分母 2, 地址 0x40013		0x00	
	ASP_M_MSB		0x00	ASP 采样率分数除法分母最高有效位
43	设置ASP LRCK高电平时间ASP LRCK高电平时间1。0x40014 0x1F ASP_L	CHI_LSB	0x1F	ASP LRCK 高电平时间持续时长最低有效位
	ASP LRCK 高电平时间 2. 0x40015	0x00		
	ASP_LCHI_MSB		0x00	ASP LRCK 高电平时间持续时长最高有效位
44	设置 ASP LRCK 周期	ASP LRCK 周期 1. 0x40016	0x3F	
	ASP_LCPRLSB		0x3F	ASP LRCK 周期的最低有效位
	ASP LRCK 周期 2. 0x40017		0x00	
	ASP_LCPR_MSB		0x00	ASP LRCK 周期的最高有效位
45	配置 ASP 时钟	ASP 时钟配置. 0x40018 0x1C		
	保留		000	
	ASP_M/SB		1	设置 ASP 端口为主设备
	ASP_SCPOL_OUT		1	设置输出 SCLK 极性
	ASP_SCPOL_IN		1	输入 SCLK 极性不关心
	ASP_LCPOL_OUT		0	设置输出 LRCLK 极性
	ASP_LCPOL_IN		0	输入 LRCLK 极性不关心
46	配置 ASP 帧	ASP 帧格式配置. 0x40019 0x0A 保留 ASP_		
	STP ASP		000	配置 ASP 端口以接收 I2S 输入
	5050 AS		0	
	P_FSD		1	
			010	
47	设置 ASP 通道位置, ASP 通道 1 位置。0x50000 0x00	ASP_RX_CH1	0x00	ASP 通道 1 从 SCLK0 开始
	ASP 通道 2 位置. 0x50001 0x00			
	ASP_RX_CH2		0x00	ASP 通道 2 从 SCLK0 开始
48	设置ASP通道大小并使能	ASP 通道 1 大小及使能。0x5000A	0x07	
	保留		0000	
	ASP_RX_CH1_AP		0	ASP 通道 1 有效相位
	ASP_RX_CH1_EN		1	启用 ASP 通道 1
	ASP_RX_CH1_RES		11	ASP 通道 1 大小为 32 位
	ASP 通道 2 大小及使能。0x5000B		0x0F	
	保留		0000	
	ASP_RX_CH2_AP		1	ASP 通道 2 有效相位
	ASP_RX_CH2_EN		1	启用 ASP 通道 2
	ASP_RX_CH2_RES		11	ASP 通道 2 大小为 32 位
49	设置 PCM			
50	配置 PCM 滤波器	PCM 滤波器选项。0x90000	0x02	
	FILTER_SLOW_FASTB		0	
	PHCOMP_LOWLATB		0	
	NOS		0	
	保留		00	
	PCM_WBF_EN		0	
	HIGH_PASS		1	选择高通滤波器
	DEEMP_ON		0	
51	设置通道 B 音量, PCM 音量 B。0x90001	PCM_VOLUME_B	0x0C	
			0x0C	设置音量至 -6 dB
52	设置通道 A 音量, PCM 音量 A。0x90002	PCM_VOLUME_A	0x0C	
			0x0C	设置音量至 -6 dB

Example 5-18. DoP and PCM Mixing (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
53	Configure PCM Path Signal Control	PCM Path Signal Control 1. 0x90003	0xEC	
		PCM_RAMP_DOWN	1	Soft ramp down of volume on filter change
		PCM_VOL_BEQA	1	Volume setting on both channels controlled by PCM_VOLUME_A
		PCM_SZC	10	Enable soft ramp
		PCM_AMUTE	1	Mute after reception of 8192 samples of 0 or -1.
		PCM_AMUTEBEQA	1	Mute only when AMUTE condition is detected on both channels
		PCM_MUTE_A	0	Function is disabled
		PCM_MUTE_B	0	Function is disabled
		PCM Path Signal Control 2. 0x90004	0x00	
		Reserved	0000	Disable all functions in this register
		PCM_INV_A	0	
		PCM_INV_B	0	
		PCM_SWAP_CHAN	0	
		PCM_COPY_CHAN	0	
54	Read interrupt status 2 register	Interrupt Status 2. 0xF0001		Clear sticky bits
55	Enable ASP Interrupts	Interrupt Mask 2. 0xF0011	0x07	
		ASP_OVFL_INT_MASK	0	Enable ASP_OVFL interrupt
		ASP_ERROR_INT_MASK	0	Enable ASP_ERROR interrupt
		ASP_LATE_INT_MASK	0	Enable ASP_LATE interrupt
		ASP_EARLY_INT_MASK	0	Enable ASP_EARLY interrupt
		ASP_NOLRCK_INT_MASK	0	Enable ASP_NOLRCK interrupt
		Reserved	111	
56	Enable ASP Clocks	Pad Interface Configuration. 0x1000D	0x00	
		Reserved	0000 00	
		XSP_3ST	0	Enable ASP serial clocks
		ASP_3ST	0	
57	Enable ASP	Power Down Control. 0x20000	0x24	
		PDN_XSP	0	
		PDN_ASP	0	Enable ASP
		PDN_DSDIF	1	
		PDN_HP	0	
		PDN_XTAL	0	
		PDN_PLL	1	
		PDN_CLKOUT	0	
		Reserved	0	
58	Enable PCM/DoP mix			
59	Configure DSD Volume	DSD Volume A. 0x70001	0x0C	
		DSD_VOLUME_A	0x0C	Channel A volume set to 0 dB
60	Prepare for PCM/DoP Mix operation	DSD and PCM Mixing Control. 0x70005	0x02	
		Reserved	0000 00	Enable PCM playback path for DoP Mixing
		MIX_PCM_PREP	1	
		MIX_PCM_DSD	0	
61	Wait for 6 ms			
62	Enable PCM/DoP mix	DSD and PCM Mixing Control. 0x70005	0x03	
		Reserved	0000 00	Enable PCM/DoP Mixing
		MIX_PCM_PREP	1	
		MIX_PCM_DSD	1	

5.14 Headphone Load Measurement

The CS43131 can be configured to measure the impedance of headphone load. Please refer to [Section 4.5.2](#) for a description of headphone load detection. The following subsections describe the steps needed to measure DC impedance or both AC/DC impedance of the headphone.

示例 5-18。DoP 与 PCM 混合（续）

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
53	配置 PCM 路径信号控制	PCM 路径信号控制 1, 0x90003 0xEC		
		PCM_RAMP_DOWN	1	滤波器切换时音量软降
		PCM_VOL_BEQA	1	两个通道的音量设置由 PCM_VOLUME_A 控制
		PCM_SZC	10	启用软斜坡
		PCM_AMUTE	1	接收 8192 个值为 0 或 -1 的样本后静音
		PCM_AMUTEBEQA	1	仅当两个通道均检测到 AMUTE 条件时静音
		PCM_MUTE_A	0	功能已禁用
		PCM_MUTE_B	0	功能已禁用
		PCM 路径信号控制 2, 0x90004 0x00		
		保留	0000	禁用此寄存器中的所有功能
		PCM_INV_A	0	
		PCM_INV_B	0	
		PCM_SWAP_CHAN	0	
		PCM_COPY_CHAN	0	
54	读取中断状态 2 寄存器	中断状态 2, 0xF0001		清除粘滞位
55	启用ASP中断	中断屏蔽 2, 0xF0011	0x07	
		ASP_OVFL_INT_MASK	0	启用ASP_OVFL中断
		ASP_ERROR_INT_MAS	0	启用ASP_ERROR中断
		KASP_LATE_INT_MA	0	启用ASP_LATE中断
		SKASP_EARLY_INT_M	0	启用ASP_EARLY中断
		ASKASP_NOLRCK_INT_	0	启用ASP_NOLRCK中断
		MASK 保留	111	
56	启用ASP时钟	引脚接口配置, 0x1000D 0x00 保留 XSP_3S		
		T ASP_3	0000 00	
		ST	0	启用ASP串行时钟
			0	
57	启用ASP	关断控制, 0x20000	0x24	
		PDN_XSP	0	
		PDN_ASP	0	启用ASP
		PDN_DSDIF	1	
		PDN_HP	0	
		PDN_XTAL	0	
		PDN_PLL	1	
		PDN_CLKOUT	0	
		保留	0	
58	启用PCM/DoP混合			
59	配置 DSD 音量	DSD 音量 A, 0x70001	0x0C	
		DSD_VOLUME_A	0x0C	通道A音量设置为0 dB
60	准备PCM/DoP混合操作	DSD与PCM混合控制, 0x70005	0x02	
		保留	0000 00	启用PCM播放路径以进行DoP混合
		MIX_PCM_PREP	1	
		MIX_PCM_DSD	0	
61	等待6毫秒			
62	启用PCM/DoP混合	DSD与PCM混合控制, 0x70005	0x03	
		保留	0000 00	启用PCM/DoP混合
		MIX_PCM_PREP	1	
		MIX_PCM_DSD	1	

5.14 耳机负载测量

CS43131 可配置为测量耳机负载阻抗。有关耳机负载检测的说明，请参见第 4.5.2 节。以下小节描述测量耳机直流阻抗或交流/直流阻抗的步骤。

5.14.1 Measuring Only DC Impedance

Fig. 5-1 shows and Ex. 5-19 describes the steps necessary for measuring DC impedance with the following assumptions:

- The CS43131 is already powered up and out of reset.
- MCLK_INT is 22.5792 or 24.576 MHz sourced from MCLK/XTAL or PLL (MCLK_SRC_SEL = 00 or 01).
- HP_IN_EN = 0 and HPOLOAD_EN = 0.
- A headphone is already plugged in and HPDETECT_PLUG_INT = 1.

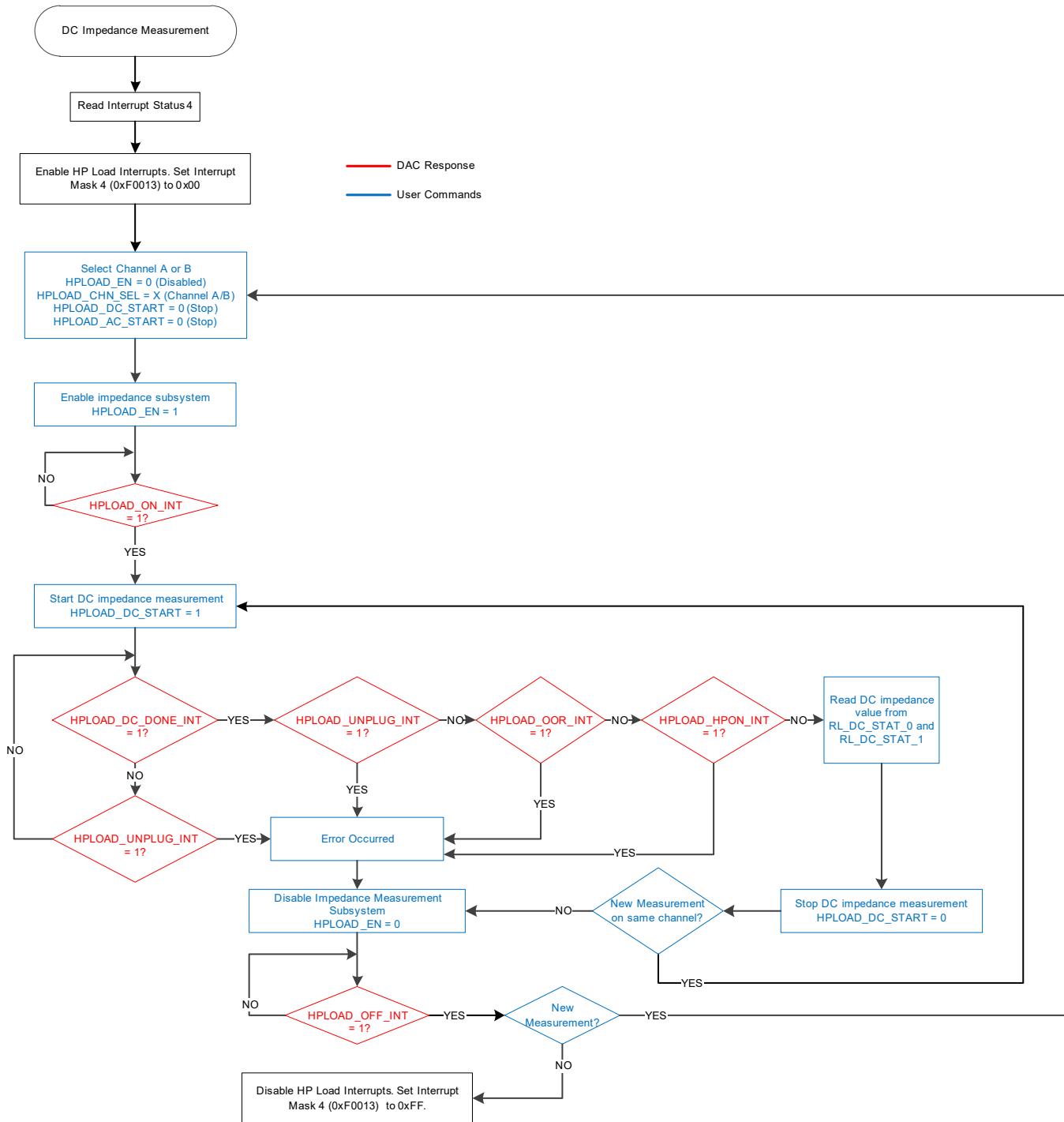


Figure 5-1. DC Impedance Measurement Flowchart

5.14.1 仅测量直流阻抗

图 5-1 显示，示例 5-19 描述了在以下假设条件下测量直流阻抗所需的步骤：

- CS43131 已上电且已退出复位状态。
- MCLK_INT 为 22.5792 MHz 或 24.576 MHz，来源于 MCLK/晶体振荡器或 PLL (MCLK_SRC_SEL = 00 或 01)。
- HP_IN_EN = 0 且 HPOLOAD_EN = 0。
- 耳机已插入，且 HPDETECT_PLUG_INT = 1。

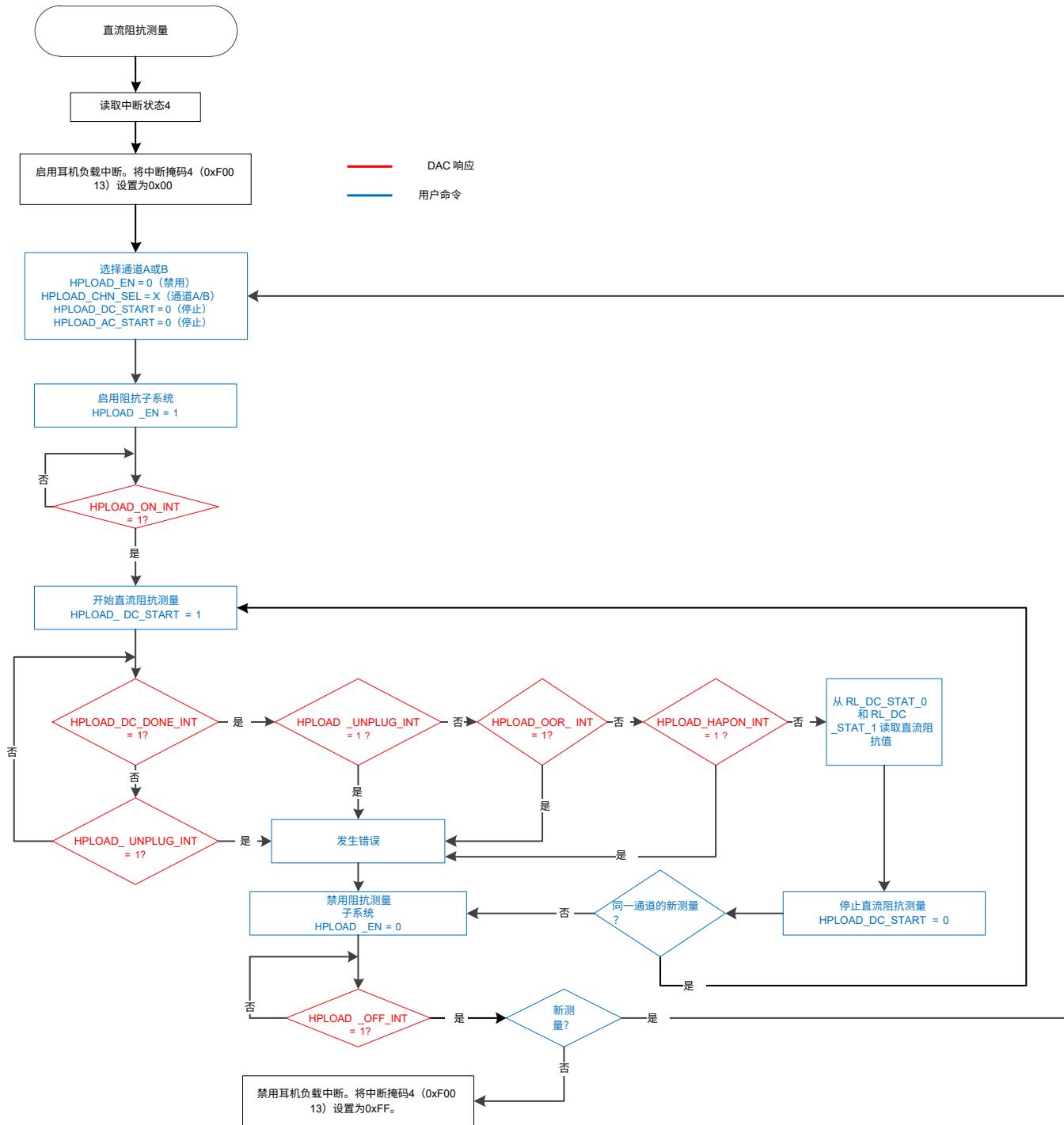


图 5-1。直流阻抗测量流程图

Ex. 5-19 demonstrates measuring DC impedance for both channels of the CS43131.

Example 5-19. Sequence for DC Impedance Measurement

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Read Interrupt Status 4 register (0xF0003) to clear sticky bits.			
2	Enable HP Load Interrupts	Interrupt Mask 4. 0xF0013	0x00	
		HPLOAD_NO_DC_INT_MASK	0	Enable HPLOAD_NO_DC interrupt
		HPLOAD_UNPLUG_INT_MASK	0	Enable HPLOAD_UNPLUG interrupt
		HPLOAD_HPON_INT_MASK	0	Enable HPLOAD_HPON interrupt
		HPLOAD_OOR_INT_MASK	0	Enable HPLOAD_OOR interrupt
		HPLOAD_AC_DONE_INT_MASK	0	Enable HPLOAD_AC_DONE interrupt
		HPLOAD_DC_DONE_INT_MASK	0	Enable HPLOAD_DC_DONE interrupt
		HPLOAD_OFF_INT_MASK	0	Enable HPLOAD_OFF interrupt
		HPLOAD_ON_INT_MASK	0	Enable HPLOAD_ON interrupt
3	Select Channel A	HP Load 1. 0xE0000	0x00	
		HPLOAD_EN	0	
		Reserved	00	
		HPLOAD_CHN_SEL	0	HPOUTA selected
		Reserved	00	
		HPLOAD_AC_START	0	
		HPLOAD_DC_START	0	
4	Enable impedance subsystem	HP Load 1. 0xE0000	0x80	
		HPLOAD_EN	1	Enable impedance subsystem
		Reserved	00	
		HPLOAD_CHN_SEL	0	
		Reserved	00	
		HPLOAD_AC_START	0	
		HPLOAD_DC_START	0	
5	Wait for interrupt. Check if HPLOAD_ON_INT = 1 in Interrupt Status 4 register (0xF0003)			
6	Start DC impedance measurement	HP Load 1. 0xE0000	0x81	
		HPLOAD_EN	1	
		Reserved	00	
		HPLOAD_CHN_SEL	0	
		Reserved	00	
		HPLOAD_AC_START	0	
		HPLOAD_DC_START	1	Start DC impedance measurement
7	Wait for interrupt. Read Interrupt Status 4 register (0xF0003). If HPLOAD_UNPLUG_INT = 1, go to the last step as an error has occurred. If HPLOAD_OOR_INT = 1, go to the last step as an error has occurred. Otherwise, if HPLOAD_DC_DONE_INT = 1, go to the next step.			
8	DC impedance values are available in HP DC Load Status 0 (0xE000D) and HP DC Load Status 1 (0xE000E) registers.			
9	Turn off impedance measurement subsystem	HP Load 1. 0xE0000	0x00	
		HPLOAD_EN	0	Disable impedance measurement
		Reserved	00	
		HPLOAD_CHN_SEL	0	
		Reserved	00	
		HPLOAD_AC_START	0	
		HPLOAD_DC_START	0	Stop DC impedance measurement
10	Wait for interrupt. Read Interrupt Status 4 register (0xF0003). Check for HPLOAD_OFF_INT = 1.			
11	Select Channel B	HP Load 1. 0xE0000	0x10	
		HPLOAD_EN	0	
		Reserved	00	
		HPLOAD_CHN_SEL	1	HPOUTB selected
		Reserved	00	
		HPLOAD_AC_START	0	
		HPLOAD_DC_START	0	
12	Enable impedance subsystem	HP Load 1. 0xE0000	0x90	
		HPLOAD_EN	1	Enable impedance subsystem
		Reserved	00	
		HPLOAD_CHN_SEL	1	HPOUTB selected
		Reserved	00	
		HPLOAD_AC_START	0	
		HPLOAD_DC_START	0	
13	Wait for interrupt. Check if HPLOAD_ON_INT = 1 in Interrupt Status 4 register (0xF0003)			
14	Start DC impedance measurement	HP Load 1. 0xE0000	0x91	
		HPLOAD_EN	1	
		Reserved	00	
		HPLOAD_CHN_SEL	1	HPOUTB selected
		Reserved	00	
		HPLOAD_AC_START	0	
		HPLOAD_DC_START	1	Start DC impedance measurement
15	Wait for interrupt. Read Interrupt Status 4 register (0xF0003). If HPLOAD_UNPLUG_INT = 1, go to the last step as an error has occurred. If HPLOAD_OOR_INT = 1, go to the last step as an error has occurred. Otherwise, if HPLOAD_DC_DONE_INT = 1, go to the next step.			
16	DC impedance values are available in HP DC Load Status 0 (0xE000D) and HP DC Load Status 1 (0xE000E) registers.			

示例 5-19 演示了对 CS43131 两个通道的直流阻抗测量。

示例 5-19。 直流阻抗测量序列

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	读取中断状态寄存器 4 (0xF0003) 以清除粘滞位。			
2	启用耳机负载中断	中断屏蔽 4, 地址 0xF0013	0x00	
		HPLOAD_NO_DC_INT_MASK HPLOAD_UNPLUG_INT_MASK HPLOAD_HPON_INT_MASK HPLOAD_OOR_INT_MASK HPLOAD_AC_DONE_INT_MASK HPLOAD_DC_DONE_INT_MASK HPLOAD_OFF_INT_MASK HPLOAD_ON_INT_MASK	0 0 0 0 0 0 0 0	启用 HPLOAD_NO_DC 中断 启用 HPLOAD_UNPLUG 中断 启用 HPLOAD_HPON 中断 启用 HPLOAD_OOR 中断 启用 HPLOAD_AC_DONE 中断 启用 HPLOAD_DC_DONE 中断 启用 HPLOAD_OFF 中断 启用 HPLOAD_ON 中断
3	选择通道 A	耳机负载 1, 地址 0xE0000	0x00	
		HPLOAD_EN 保留 HPLOAD_CHN_SEL 保留 HPLOAD_AC_START HPLOAD_DC_START	0 00 0 00 0 0	选择 HPOUTA
4	启用阻抗子系统	耳机负载 1, 地址 0xE0000	0x80	
		HPLOAD_EN 保留 HPLOAD_CHN_SEL 保留 HPLOAD_AC_START HPLOAD_DC_START	1 00 0 00 0 0	启用阻抗子系统
5	等待中断。检查中断状态4寄存器 (0xF0003) 中HPLOAD_ON_INT是否为1			
6	启动直流阻抗测量HP负载1, 地址0xE0000		0x81	
		HPLOAD_EN 保留 HPLOAD_CHN_SEL 保留 HPLOAD_AC_START HPLOAD_DC_START	1 00 0 00 0 1	开始直流阻抗测量
7	等待中断。读取中断状态4寄存器 (0xF0003) 若HPLOAD_UNPLUG_INT为1, 因发生错误, 跳至最后一步若HPLOAD_OOR_INT为1, 因发生错误, 跳至最后一步否则, 若HPLOAD_DC_DONE_INT为1, 进入下一步			
8	直流阻抗值可在HP DC Load Status 0 (0xE000D) 和HP DC Load Status 1 (0xE000E) 寄存器中读取			
9	关闭阻抗测量子系统	耳机负载 1, 地址 0xE0000	0x00	
		HPLOAD_EN 保留 HPLOAD_CHN_SEL 保留 HPLOAD_AC_START HPLOAD_DC_START	0 00 0 00 0 0	禁用阻抗测量
				停止直流阻抗测量
10	等待中断。读取中断状态4寄存器 (0xF0003) 检查HPLOAD_OFF_INT是否为1			
11	选择通道B	耳机负载 1, 地址 0xE0000	0x10	
		HPLOAD_EN 保留 HPLOAD_CHN_SEL 保留 HPLOAD_AC_START HPLOAD_DC_START	0 00 1 00 0 0	选择 HPOUTB
12	启用阻抗子系统	耳机负载 1, 地址 0xE0000	0x90	
		HPLOAD_EN 保留 HPLOAD_CHN_SEL 保留 HPLOAD_AC_START HPLOAD_DC_START	1 00 1 00 0 0	启用阻抗子系统 选择 HPOUTB
13	等待中断。检查中断状态4寄存器 (0xF0003) 中HPLOAD_ON_INT是否为1			
14	启动直流阻抗测量HP负载1, 地址0xE0000		0x91	
		HPLOAD_EN 保留 HPLOAD_CHN_SEL 保留 HPLOAD_AC_START HPLOAD_DC_START	1 00 1 00 0 1	选择 HPOUTB 开始直流阻抗测量
15	等待中断。读取中断状态4寄存器 (0xF0003) 若HPLOAD_UNPLUG_INT为1, 因发生错误, 跳至最后一步若HPLOAD_OOR_INT为1, 因发生错误, 跳至最后一步否则, 若HPLOAD_DC_DONE_INT为1, 进入下一步			
16	直流阻抗值可在HP DC Load Status 0 (0xE000D) 和HP DC Load Status 1 (0xE000E) 寄存器中读取			

Example 5-19. Sequence for DC Impedance Measurement (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
17	Turn off impedance measurement subsystem	HP Load 1. 0xE0000	0x00	
		HPLOAD_EN	0	Disable impedance measurement subsystem
		Reserved	00	
		HPLOAD_CHN_SEL	0	
		Reserved	00	
		HPLOAD_AC_START	0	
		HPLOAD_DC_START	0	
18	Wait for interrupt. Check if HPLOAD_OFF_INT = 1 in Interrupt Status 4 register (0xF0003).			
19	Disable HP Load Interrupts	Interrupt Mask 4. 0xF0013	0xFF	

示例 5-19。 直流阻抗测量序列（续）

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
17 关闭阻抗测量子系统		耳机负载 1, 地址 0xE0000	0x00	
		HLOAD_EN	0	禁用阻抗测量子系统
		保留	00	
		HLOAD_CHN_SEL	0	
		保留	00	
		HLOAD_AC_START	0	
		HLOAD_DC_START	0	
18 等待中断。检查中断状态4寄存器（0xF0003）中HLOAD_OFF_INT是否为1。				
19 禁用耳机负载中断		中断屏蔽 4, 地址 0xF0013	0xFF	

5.14.2 Measuring AC and DC Impedance

Fig. 5-2 shows and Ex. 5-20 describes the steps necessary to measure AC/DC impedance with the following assumptions:

- The CS43131 is already powered up and out of reset.
- MCLK_INT is 22.5792 or 24.576 MHz sourced from MCLK/XTAL or PLL (MCLK_SRC_SEL = 00 or 01).
- HP_IN_EN = 0 and HPOLOAD_EN = 0.
- A headphone is already plugged in and HPDETECT_PLUG_INT = 1.

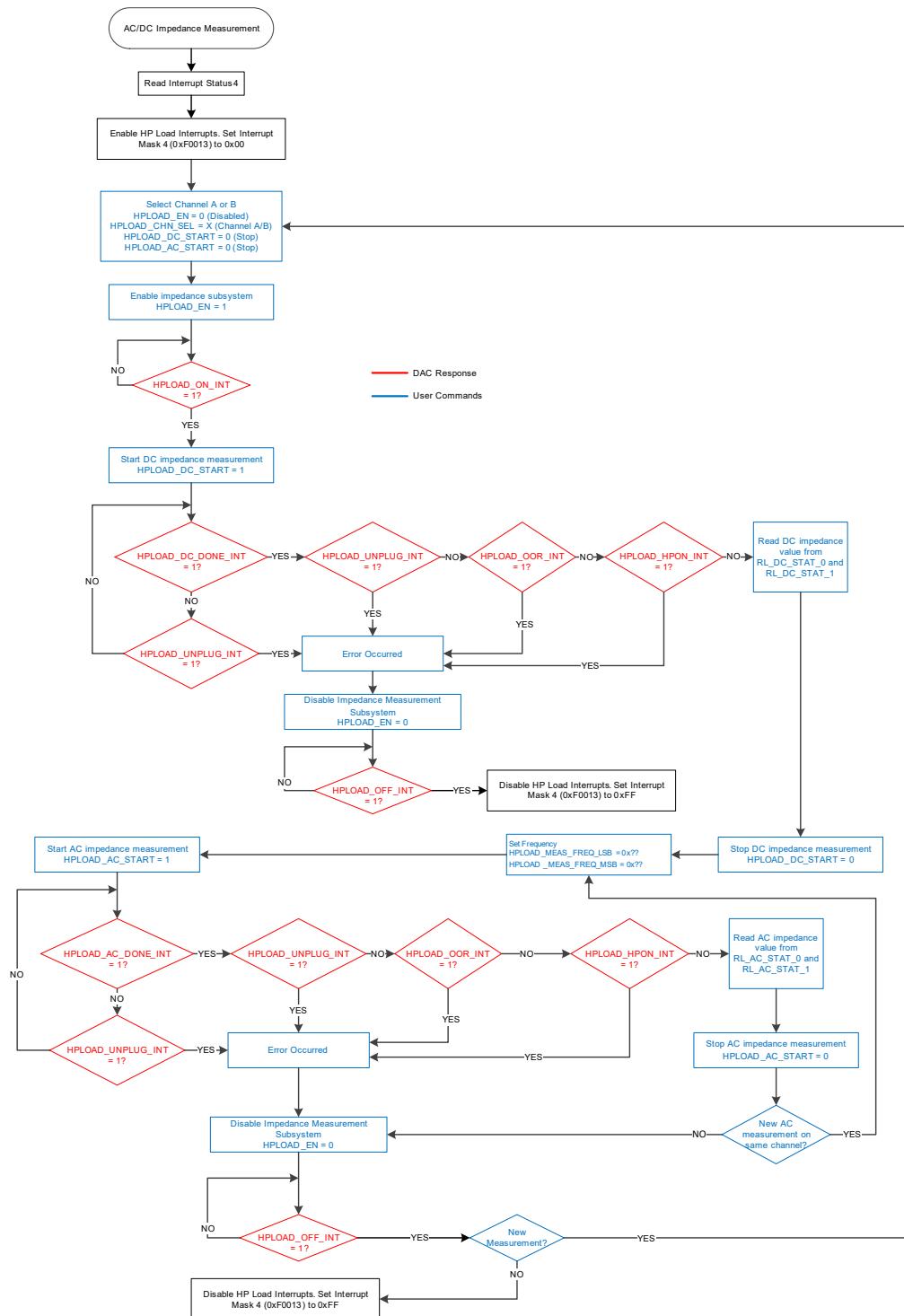


Figure 5-2. AC and DC Impedance Measurement Flowchart

5.14.2 交流和直流阻抗测量

图5-2展示了，示例5-20描述了在以下假设条件下测量交流/直流阻抗所需的步骤：

- CS43131 已上电且已退出复位状态。
 - MCLK_INT 为 22.5792 MHz 或 24.576 MHz，来源于 MCLK/晶体振荡器或 PLL（MCLK_SRC_SEL = 00 或 01）。
 - HP_IN_EN = 0 且 HPOLOAD_EN = 0。
 - 耳机已插入，且 HPDETECT_PLUG_INT = 1。

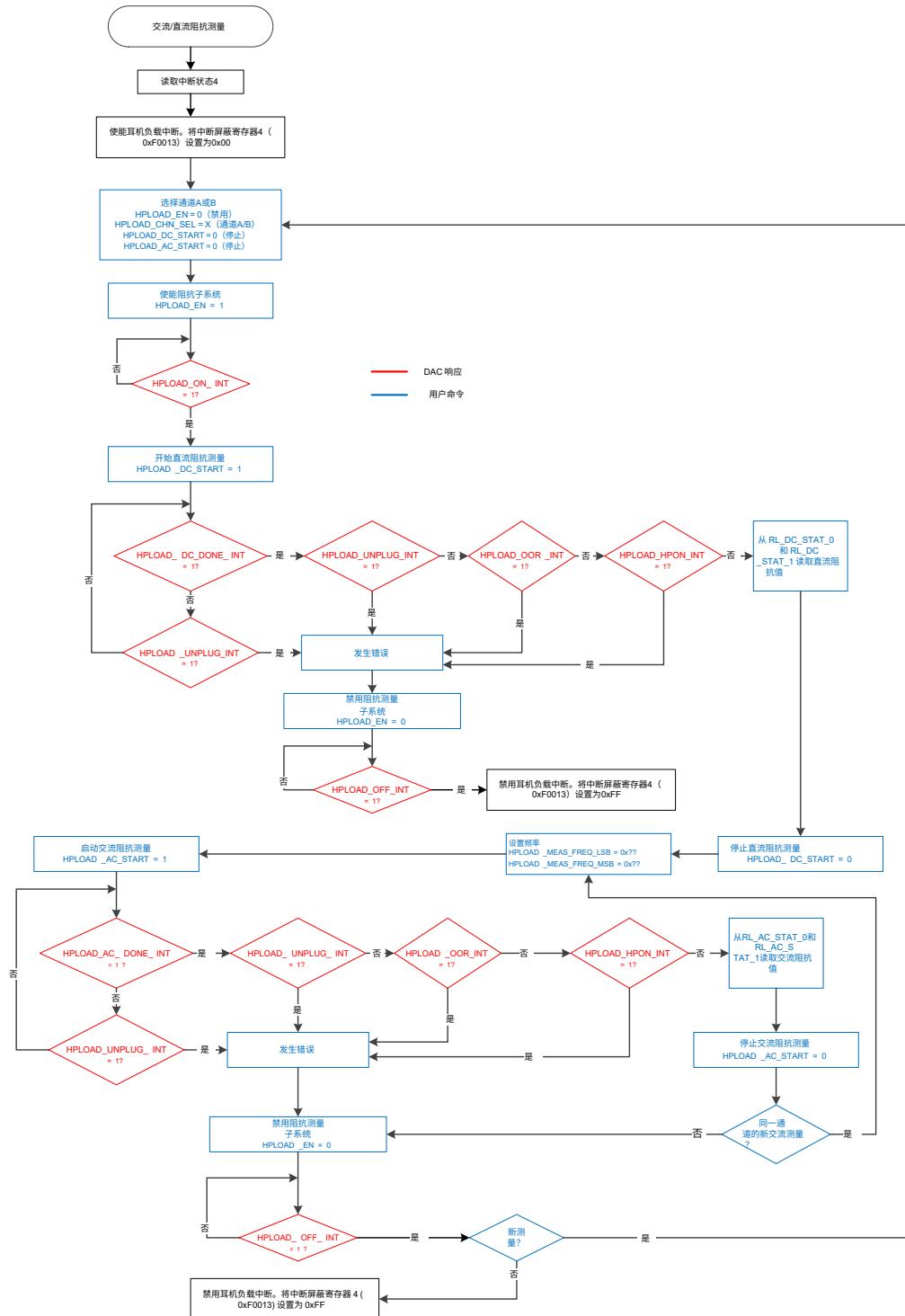


图5-2。交流和直流阻抗测量流程图

Ex. 5-20 demonstrates measuring both AC and DC impedance for both channels of the CS43131.

Example 5-20. AC and DC Impedance Measurement

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Read Interrupt Status 4 register (0xF0003) to clear sticky bits.			
2	Enable HP Load Interrupts	Interrupt Mask 4. 0xF0013	0x00	
		HPLOAD_NO_DC_INT_MASK	0	Enable HPLOAD_NO_DC interrupt
		HPLOAD_UNPLUG_INT_MASK	0	Enable HPLOAD_UNPLUG interrupt
		HPLOAD_HPON_INT_MASK	0	Enable HPLOAD_HPON interrupt
		HPLOAD_OOR_INT_MASK	0	Enable HPLOAD_OOR interrupt
		HPLOAD_AC_DONE_INT_MASK	0	Enable HPLOAD_AC_DONE interrupt
		HPLOAD_DC_DONE_INT_MASK	0	Enable HPLOAD_DC_DONE interrupt
		HPLOAD_OFF_INT_MASK	0	Enable HPLOAD_OFF interrupt
		HPLOAD_ON_INT_MASK	0	Enable HPLOAD_ON interrupt
3	Select Channel A	HP Load 1. 0xE0000	0x00	
		HPLOAD_EN	0	
		Reserved	00	
		HPLOAD_CHN_SEL	0	HPOUTA selected
		Reserved	00	
		HPLOAD_AC_START	0	
		HPLOAD_DC_START	0	
4	Enable impedance subsystem	HP Load 1. 0xE0000	0x80	
		HPLOAD_EN	1	Enable impedance subsystem
		Reserved	00	
		HPLOAD_CHN_SEL	0	
		Reserved	00	
		HPLOAD_AC_START	0	
		HPLOAD_DC_START	0	
5	Wait for interrupt. Check if HPLOAD_ON_INT = 1 in Interrupt Status 4 register (0xF0003)			
6	Start DC impedance measurement	HP Load 1. 0xE0000	0x81	
		HPLOAD_EN	1	
		Reserved	00	
		HPLOAD_CHN_SEL	0	
		Reserved	00	
		HPLOAD_AC_START	0	
		HPLOAD_DC_START	1	Start DC impedance measurement
7	Wait for interrupt. Read Interrupt Status 4 register (0xF0003). If HPLOAD_UNPLUG_INT = 1, go to the last step as an error has occurred. If HPLOAD_OOR_INT = 1, go to the last step as an error has occurred. Otherwise, if HPLOAD_DC_DONE_INT = 1, go to the next step.			
8	DC impedance values are available in HP DC Load Status 0 (0xE000D) and HP DC Load Status 1 (0xE000E) registers.			
9	Set HP load measurement frequency to desired frequency. Assuming 1 kHz.	HP Load Measurement 1. 0xE0003	0xA8	
		HPLOAD_MEAS_FREQ_LSB	0xA8	Set measurement frequency = 1 kHz
		HP Load Measurement 2. 0xE0004	0x00	
		HPLOAD_MEAS_FREQ_MSB	0x00	MSB of load measurement frequency
10	Start AC impedance measurement	HP Load 1. 0xE0000	0x82	
		HPLOAD_EN	1	
		Reserved	00	
		HPLOAD_CHN_SEL	0	
		Reserved	00	
		HPLOAD_AC_START	1	Start AC impedance measurement
		HPLOAD_DC_START	0	
11	Wait for interrupt. Read Interrupt Status 4 register (0xF0003). If HPLOAD_UNPLUG_INT = 1, go to the last step as an error has occurred. If HPLOAD_OOR_INT = 1, go to the last step as an error has occurred. Otherwise, if HPLOAD_AC_DONE_INT = 1, go to the next step.			
12	AC impedance values are available in HP AC Load Status 0 (0xE0010) and HP AC Load Status 1 (0xE0011) registers.			
13	Stop AC impedance measurement.	HP Load 1. 0xE0000	0x80	
14	If another frequency point is desired, go back to step 9. Otherwise continue.			
15	Disable impedance measurement subsystem and select channel B	HP Load 1. 0xE0000	0x10	
16	Wait for interrupt. Read Interrupt Status 4 register (0xF0003). Check for HPLOAD_OFF_INT = 1. If Channel B measurement is desired, continue to the next step; otherwise go to step 30 to end the impedance measurement.			
17	Enable impedance subsystem	HP Load 1. 0xE0000	0x90	
		HPLOAD_EN	1	Enable impedance subsystem
		Reserved	00	
		HPLOAD_CHN_SEL	1	HPOUTB selected
		Reserved	00	
		HPLOAD_AC_START	0	
		HPLOAD_DC_START	0	
18	Wait for interrupt. Check if HPLOAD_ON_INT = 1 in Interrupt Status 4 register (0xF0003)			

示例 5-20 演示了如何测量 CS43131 两个通道的交流和直流阻抗。

示例 5-20。 交流和直流阻抗测量

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	读取中断状态寄存器 4 (0xF0003) 以清除粘滞位。			
2	启用耳机负载中断	中断屏蔽 4, 地址 0xF0013	0x00	
		HPLOAD_NO_DC_INT_MASK HPLOAD_UNPLUG_INT_MASK HPLOAD_HPON_INT_MASK HPLOAD_OOR_INT_MASK HPLOAD_AC_DONE_INT_MASK HPLOAD_DC_DONE_INT_MASK HPLOAD_OFF_INT_MASK HPLOAD_ON_INT_MASK	0 0 0 0 0 0 0 0	启用 HPLOAD_NO_DC 中断 启用 HPLOAD_UNPLUG 中断 启用 HPLOAD_HPON 中断 启用 HPLOAD_OOR 中断 启用 HPLOAD_AC_DONE 中断 启用 HPLOAD_DC_DONE 中断 启用 HPLOAD_OFF 中断 启用 HPLOAD_ON 中断
3	选择通道 A	耳机负载 1, 地址 0xE0000	0x00	
		HPLOAD_EN 保留 HPLOAD_CHN_SEL 保留 HPLOAD_AC_START HPLOAD_DC_START	0 00 0 00 0 0	选择 HPOUTA
4	启用阻抗子系统	耳机负载 1, 地址 0xE0000	0x80	
		HPLOAD_EN 保留 HPLOAD_CHN_SEL 保留 HPLOAD_AC_START HPLOAD_DC_START	1 00 0 00 0 0	启用阻抗子系统
5	等待中断。检查中断状态4寄存器 (0xF0003) 中HPLOAD_ON_INT是否为1			
6	启动直流阻抗测量HP负载1, 地址0xE0000		0x81	
		HPLOAD_EN 保留 HPLOAD_CHN_SEL 保留 HPLOAD_AC_START HPLOAD_DC_START	1 00 0 00 0 1	开始直流阻抗测量
7	等待中断。读取中断状态4寄存器 (0xF0003) 若HPLOAD_UNPLUG_INT为1, 因发生错误, 跳至最后一步若HPLOAD_OOR_INT为1, 因发生错误, 跳至最后一步否则, 若HPLOAD_DC_DONE_INT为1, 进入下一步			
8	直流阻抗值可在HP DC Load Status 0 (0xE000D) 和HP DC Load Status 1 (0xE000E) 寄存器中读取			
9	将耳机负载测量频率设置为所需频率。假设为 1 kHz。耳机负载测量 1, 寄存器地址 0xE0003		0xA8	设置测量频率 = 1 kHz
		HPLOAD_MEAS_FREQ_LSB	0xA8	
		耳机负载测量 2, 寄存器地址 0xE0004	0x00	
		HPLOAD_MEAS_FREQ_MSB	0x00	负载测量频率的最高有效位
10	启动交流阻抗测量	耳机负载 1, 地址 0xE0000	0x82	
		HPLOAD_EN 保留 HPLOAD_CHN_SEL 保留 HPLOAD_AC_START HPLOAD_DC_START	1 00 0 00 1 0	启动交流阻抗测量
11	等待中断。读取中断状态4寄存器 (0xF0003) 若HPLOAD_UNPLUG_INT为1, 因发生错误, 跳至最后一步若HPLOAD_OOR_INT为1, 因发生错误, 跳至最后一步否则, 如果HPLOAD_AC_DONE_INT = 1, 则进入下一步。			
12	交流阻抗值可在 HP AC Load Status 0 (0xE0010) 和 HP AC Load Status 1 (0xE0011) 寄存器中读取。			
13	停止交流阻抗测量。	耳机负载 1, 地址 0xE0000	0x80	
14	如需测量其他频点, 请返回步骤 9, 否则继续。			
15	禁用阻抗测量子系统并选择通道 B	耳机负载 1, 地址 0xE0000	0x10	
		HPLOAD_EN 保留 HPLOAD_CHN_SEL 保留 HPLOAD_AC_START HPLOAD_DC_START	0 00 0 00 0 0	
16	等待中断。读取中断状态4寄存器 (0xF0003) 检查 HPLOAD_OFF_INT 是否为 1。如需测量通道 B, 继续下一步; 否则转至步骤 30 结束阻抗测量。			
17	启用阻抗子系统	耳机负载 1, 地址 0xE0000	0x90	
		HPLOAD_EN 保留 HPLOAD_CHN_SEL 保留 HPLOAD_AC_START HPLOAD_DC_START	1 00 1 00 0 0	启用阻抗子系统 选择 HPOUTB
18	等待中断。检查中断状态4寄存器 (0xF0003) 中HPLOAD_ON_INT是否为1			

Example 5-20. AC and DC Impedance Measurement (Cont.)

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
19	Start DC impedance measurement	HP Load 1. 0xE0000	0x91	
		HLOAD_EN	1	
		Reserved	00	
		HLOAD_CHN_SEL	1	HPOUTB selected
		Reserved	00	
		HLOAD_AC_START	0	
		HLOAD_DC_START	1	Start DC impedance measurement
20	Wait for interrupt. Read Interrupt Status 4 register (0xF0003). If HLOAD_UNPLUG_INT = 1, go to the last step as an error has occurred. If HLOAD_OOR_INT = 1, go to the last step as an error has occurred. Otherwise, if HLOAD_DC_DONE_INT = 1, go to the next step.			
21	DC impedance values are available in HP DC Load Status 0 (0xE000D) and HP DC Load Status 1 (0xE000E) registers.			
22	Set HP load measurement frequency to desired frequency. Assuming 1 kHz.	HP Load Measurement 1. 0xE0003	0xA8	
		HLOAD_MEAS_FREQ_LSB	0xA8	Set measurement frequency = 1 kHz
		HP Load Measurement 2. 0xE0004	0x00	
		HLOAD_MEAS_FREQ_MSB	0x00	MSB of load measurement frequency
23	Start AC impedance measurement	HP Load 1. 0xE0000	0x92	
		HLOAD_EN	1	
		Reserved	00	
		HLOAD_CHN_SEL	1	HPOUTB selected
		Reserved	00	
		HLOAD_AC_START	1	
		HLOAD_DC_START	0	Start AC impedance measurement
24	Wait for interrupt. Read Interrupt Status 4 register (0xF0003). If HLOAD_UNPLUG_INT = 1, go to the last step as an error has occurred. If HLOAD_OOR_INT = 1, go to the last step as an error has occurred. Otherwise, if HLOAD_AC_DONE_INT = 1, go to the next step.			
25	AC impedance values are available in HP AC Load Status 0 (0xE0010) and HP AC Load Status 1 (0xE0011) registers.			
26	Stop AC impedance measurement.	HP Load 1. 0xE0000	0x90	
27	If another frequency point is desired go back to step 22. Otherwise continue.			
28	Disable impedance measurement subsystem and select channel B	HP Load 1. 0xE0000	0x00	
29	Wait for interrupt. Check if HLOAD_OFF_INT = 1 in Interrupt Status 4 register (0xF0003).			
30	Disable HP Load Interrupts	Interrupt Mask 4. 0xF0013	0xFF	

示例 5-20。交流和直流阻抗测量（续）

步骤	任务	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
19	启动直流阻抗测量HP负载1，地址0xE0000		0x91	
	HLOAD_EN		1	
	保留		00	
	HLOAD_CHN_SEL		1	选择HPOUTB
	保留		00	
	HLOAD_AC_START		0	
	HLOAD_DC_START		1	开始直流阻抗测量
20	等待中断。读取中断状态4寄存器（0xF0003）若HLOAD_UNPLUG_INT为1，因发生错误，跳至最后一步若HLOAD_OOR_INT为1，因发生错误，跳至最后一步否则，若HLOAD_DC_DONE_INT为1，进入下一步			
21	直流阻抗值可在HP DC Load Status 0 (0xE000D) 和HP DC Load Status 1 (0xE000E) 寄存器中读取			
22	将耳机负载测量频率设置为所需频率，假设为1 kHz。	耳机负载测量 1，地址 0xE0003	0xA8	
	HLOAD_MEAS_FREQ_LSB		0xA8	设置测量频率 = 1 kHz
	耳机负载测量 2，寄存器地址 0xE0004		0x00	
	HLOAD_MEAS_FREQ_MSB		0x00	负载测量频率的最高有效位
23	启动交流阻抗测量	耳机负载 1，地址 0xE0000	0x92	
	HLOAD_EN		1	
	保留		00	
	HLOAD_CHN_SEL		1	选择HPOUTB
	保留		00	
	HLOAD_AC_START		1	启动交流阻抗测量
	HLOAD_DC_START		0	
24	等待中断。读取中断状态4寄存器（0xF0003）若HLOAD_UNPLUG_INT为1，因发生错误，跳至最后一步若HLOAD_OOR_INT为1，因发生错误，跳至最后一步否则，如果 HLOAD_AC_DONE_INT = 1，则进入下一步。			
25	交流阻抗值可在 HP AC Load Status 0 (0xE0010) 和 HP AC Load Status 1 (0xE0011) 寄存器中读取。			
26	停止交流阻抗测量。耳机负载 1，地址 0xE0000		0x90	
27	如需测量其他频点，请返回步骤 22，否则继续。			
28	禁用阻抗测量子系统并选择通道 B	耳机负载 1，地址 0xE0000	0x00	
	。			
29	等待中断。检查中断状态4寄存器（0xF0003）中HLOAD_OFF_INT是否为1。			
30	禁用耳机负载中断。	中断屏蔽 4，地址 0xF0013	0xFF	

6 Register Quick Reference

The registers for each CS43131 module are located at specific base addresses within the 24-bit register address space. The organization of this register space is summarized in [Table 6-1](#).

Table 6-1. Register Base Addresses

Base Address	Module	Reference
0x01 0000	Global Registers	Section 6.1
0x03 0000	PLL Registers	Section 6.2
0x04 0000	ASP and XSP Registers	Section 6.3
0x06 0000	DSD Registers	Section 6.4
0x08 0000	Headphone and PCM Registers	Section 6.5
0x0F 0000	Interrupt Status and Mask Registers	Section 6.6

Notes: Default values are shown below the bit field names. The default values in all reserved bits must be preserved.

6.1 Global Registers

Address	Function	7	6	5	4	3	2	1	0
0x01 0000	Device ID A and B p. 113 (Read Only)	0	1	0	0	0	0	1	1
0x01 0001	Device ID C and D p. 113 (Read Only)	0	0	0	1	0	0	1	1
0x01 0002	Device ID E (Read Only) p. 113	0	0	0	1	0	0	—	0
0x01 0004	Revision ID (Read Only) p. 113	x	x	x	x	x	x	x	x
0x01 0005	Subrevision ID (Read Only) p. 113	0	x	x	x	x	x	x	x
0x01 0006	System Clocking Control p. 114	0	0	—	0	0	MCLK_INT 1	MCLK_SRC_SEL 1	0
0x01 0007– 0x01 000A	Reserved	0	0	0	0	0	0	0	0
0x01 000B	Serial Port Sample Rate p. 114	0	0	—	0	0	0	0	1
0x01 000C	Serial Port Sample Bit Size p. 114	0	0	0	0	0	XSP_SPSIZE 1	ASP_SPSIZE 0	1
0x01 000D	Pad Interface Configuration p. 114	0	0	0	—	0	0	XSP_3ST 1	ASP_3ST 1
0x01 000E– 0x01 FFFF	Reserved	0	0	0	0	0	0	0	0
0x02 0000	Power Down Control p. 115	PDN_XSP 1	PDN_ASP 1	PDN_DSDIF 1	PDN_HP 1	PDN_XTAL 1	PDN_PLL 1	PDN_CLKOUT 1	— 0
0x02 0001– 0x02 0051	Reserved	0	0	0	0	0	0	0	0
0x02 0052	Crystal Setting p. 115	0	0	—	0	0	1	0	0
0x02 0053– 0x03 0000	Reserved	0	0	0	0	—	0	0	0

6.2 PLL Registers

Address	Function	7	6	5	4	3	2	1	0
0x03 0001	PLL Setting 1 p. 116	0	0	0	—	0	0	0	PLL_START 0
0x03 0002	PLL Setting 2 p. 116	0	0	0	PLL_DIV_FRAC_0	0	0	0	0
0x03 0003	PLL Setting 3 p. 116	0	0	0	PLL_DIV_FRAC_1	0	0	0	0
0x03 0004	PLL Setting 4 p. 116	0	0	0	PLL_DIV_FRAC_2	0	0	0	0

6 寄存器快速参考

每个 CS43131 模块的寄存器位于 24 位寄存器地址空间内的特定基址处。
该寄存器空间的组织结构总结见表6-1。

表6-1 寄存器地址

基地址	模块	参考
0x01 0000	全局寄存器	第6.1节
0x03 0000	PLL寄存器	第6.2节
0x04 0000	ASP和XSP寄存器	第6.3节
0x06 0000	DSD寄存器	第6.4节
0x08 0000	耳机及PCM寄存器	第6.5节
0x0F 0000	中断状态与屏蔽寄存器	第6.6节

注：默认值显示在位域名称下方。所有保留位的默认值必须保持不变。

6.1 全局寄存器

地址	功能	7	6	5	4	3	2	1	0
0x01 0000 第113页	设备ID A和B (只读)	0	1	0	0	0	0	1	1
0x01 0001 第113页	设备ID C和D (只读)	0	0	0	1	0	0	1	1
0x01 0002 第113页	设备ID E (只读)	0	0	0	1	0	0	0	0
0x01 0004 第113页	版本ID (只读)	x	x	x	x	x	x	x	x
0x01 0005 第113页	子版本ID (只读)	0	x	x	x	x	x	x	x
0x01 0006 第114页	系统时钟控制	0	0	0	0	0	1	1	0
0x01 0007- 0x01 000A	保留	0	0	0	0	0	0	0	0
0x01 000B 第114页	串口采样率	0	0	0	0	0	0	0	1
0x01 000C 第114页	串口采样位宽	0	0	0	0	0	1	0	1
0x01 000D 第114页	引脚接口 配置	0	0	0	0	0	0	1	1
0x01 000E- 0x01 FFFF	保留	0	0	0	0	0	0	0	0
0x02 0000 第115页	掉电控制	PDN_XSP 1	PDN_ASP 1	PDN_DSIF 1	PDN_HP 1	PDN_XTAL 1	PDN_PLL 1	PDN_CLKOUT 1	— 0
0x02 0001- 0x02 0051	保留	0	0	0	0	0	0	0	0
0x02 0052 第115页	晶体振荡器设置	0	0	0	0	0	1	0	0
0x02 0053- 0x03 0000	保留	0	0	0	0	0	0	0	0

6.2 PLL 寄存器

地址	功能	7	6	5	4	3	2	1	0
0x03 0001 第116页	PLL 设置 1	0	0	0	—	0	0	0	PLL_START 0
0x03 0002 第116页	PLL 设置 2	0	0	0	PLL_DIV_FRAC_0	0	0	0	0
0x03 0003 第116页	PLL 设置 3	0	0	0	PLL_DIV_FRAC_1	0	0	0	0
0x03 0004 第116页	PLL 设置 4	0	0	0	PLL_DIV_FRAC_2	0	0	0	0

Address	Function	7	6	5	4	3	2	1	0
0x03 0005 p. 116	PLL Setting 5	0	1	0	0	0	0	0	0
0x03 0006– 0x03 0007	Reserved	0	0	0	0	—	0	0	0
0x03 0008 p. 117	PLL Setting 6	0	0	0	1	0	0	0	0
0x03 0009	Reserved	0	0	0	0	0	0	0	0
0x03 000A p. 117	PLL Setting 7	1	0	0	0	0	0	0	0
0x03 000B– 0x03 001A	Reserved	0	0	0	0	0	0	0	0
0x03 001B p. 117	PLL Setting 8	0	0	—	0	—	0	PLL_MODE 1	—
0x03 001C– 0x04 0001	Reserved	0	0	0	0	—	0	0	0

6.3 ASP and XSP Registers

Address	Function	7	6	5	4	3	2	1	0
0x04 0002 p. 117	PLL Setting 9	0	0	0	0	0	0	PLL_REF_PREDIV 1	0
0x04 0003	Reserved	0	0	0	0	0	0	0	0
0x04 0004 p. 118	CLKOUT Control	—	0	0	0	0	0	CLKOUT_SEL 0	0
0x04 0005– 0x04 000F	Reserved	0	0	0	0	0	0	0	0
0x04 0010 p. 118	ASP Numerator 1	0	0	0	0	0	0	0	1
0x04 0011 p. 118	ASP Numerator 2	0	0	0	0	0	0	0	0
0x04 0012 p. 118	ASP Denominator 1	0	0	0	0	1	0	0	0
0x04 0013 p. 119	ASP Denominator 2	0	0	0	0	0	0	0	0
0x04 0014 p. 119	ASP LRCK High Time 1	0	0	0	1	1	1	1	1
0x04 0015 p. 119	ASP LRCK High Time 2	0	0	0	0	0	0	0	0
0x04 0016 p. 119	ASP LRCK Period 1	0	0	1	1	1	1	1	1
0x04 0017 p. 119	ASP LRCK Period 2	0	0	0	0	0	0	0	0
0x04 0018 p. 120	ASP Clock Configuration	—	0	ASP_M/SB	ASP_SCPOL_OUT 1	ASP_SCPOL_IN 1	ASP_LCPOL_OUT 0	ASP_LCPOL_IN 0	
0x04 0019 p. 120	ASP Frame Configuration	—	0	ASP_STP 0	ASP_5050 1	0	ASP_FSD 1	0	
0x04 001A– 0x04 001F	Reserved	0	0	0	0	0	0	0	0
0x04 0020 p. 120	XSP Numerator 1	0	0	0	0	0	0	0	1
0x04 0021 p. 121	XSP Numerator 2	0	0	0	0	0	0	0	0
0x04 0022 p. 121	XSP Denominator 1	0	0	0	0	0	0	1	0
0x04 0023 p. 121	XSP Denominator 2	0	0	0	0	0	0	0	0
0x04 0024 p. 121	XSP LRCK High Time 1	0	0	0	1	1	1	1	1
0x04 0025 p. 121	XSP LRCK High Time 2	0	0	0	0	0	0	0	0

地址	功能	7	6	5	4	3	2	1	0
0x03 0005 第116页	PLL 设置 5	0	1	0	0	0	0	0	0
0x03 0006- 0x03 0007	保留	0	0	0	0	—	0	0	0
0x03 0008 第117页	PLL 设置 6	0	0	0	1	0	0	0	0
0x03 0009	保留	0	0	0	0	0	0	0	0
0x03 000A 第117页	PLL 设置 7	1	0	0	0	0	0	0	0
0x03 000B- 0x03 001A	保留	0	0	0	0	0	0	0	0
0x03 001B 第117页	PLL 设置 8	0	0	0	0	—	0	PLL_MODE 1	— 1
0x03 001C- 0x04 0001	保留	0	0	0	0	—	0	0	0

6.3 ASP 和 XSP 寄存器

地址	功能	7	6	5	4	3	2	1	0
0x04 0002 第117页	PLL 设置 9	0	0	0	0	0	0	PLL_REF_PREDIV 1	0
0x04 0003	保留	0	0	0	0	0	0	0	0
0x04 0004 第118页	CLKOUT 控制	—	0	0	0	0	0	CLKOUT_SEL 0	0
0x04 0005- 0x04 000F	保留	0	0	0	0	0	0	0	0
0x04 0010 第118页	ASP 分子 1	0	0	0	0	0	0	0	1
0x04 0011 第118页	ASP 分子 2	0	0	0	0	0	0	0	0
0x04 0012 第118页	ASP 分母 1	0	0	0	0	1	0	0	0
0x04 0013 第119页	ASP 分母 2	0	0	0	0	0	0	0	0
0x04 0014 第119页	ASP LRCK 高电平时间 1	0	0	0	1	1	1	1	1
0x04 0015 第119页	ASP LRCK 高电平时间 2	0	0	0	0	0	0	0	0
0x04 0016 第119页	ASP LRCK 周期 1	0	0	1	1	1	1	1	1
0x04 0017 第119页	ASP LRCK 周期 2	0	0	0	0	0	0	0	0
0x04 0018 第120页	ASP 时钟配置	—	0	ASP_M/SB 0	ASP_SCPOL_输出 1	ASP_SCPOL_输入 1	ASP_LCPOL_输出 0	ASP_LCPOL_输入 0	
0x04 0019 第120页	ASP 帧配置	—	0	ASP_STP 0	ASP_5050 1	0	ASP_FSD 1	0	
0x04 001A- 0x04 001F	保留	0	0	0	0	0	0	0	0
0x04 0020 第120页	XSP 分子 1	0	0	0	0	0	0	0	1
0x04 0021 第121页	XSP 分子 2	0	0	0	0	0	0	0	0
0x04 0022 第121页	XSP 分母 1	0	0	0	0	0	0	1	0
0x04 0023 第121页	XSP 分母 2	0	0	0	0	0	0	0	0
0x04 0024 第121页	XSP LRCK 高电平时间 1	0	0	0	1	1	1	1	1
0x04 0025 第121页	XSP LRCK 高电平时间 2	0	0	0	0	0	0	0	0

Address	Function	7	6	5	4	3	2	1	0
0x04 0026 p. 122	XSP LRCK Period 1	0	0	1	1	1	1	1	1
0x04 0027 p. 122	XSP LRCK Period 2	0	0	0	0	0	0	0	0
0x04 0028 p. 122	XSP Clock Configuration	—	—	—	XSP_M/SB	XSP_SCPOL_OUT	XSP_SCPOL_IN	XSP_LCPOL_OUT	XSP_LCPOL_IN
0x04 0029 p. 122	XSP Frame Configuration	0	0	0	XSP_STP	XSP_5050	0	XSP_FSD	0
0x04 002A– 0x04 FFFF	Reserved	0	0	0	0	0	0	0	0
0x05 0000 p. 123	ASP Channel 1 Location	0	0	0	0	0	0	0	0
0x05 0001 p. 123	ASP Channel 2 Location	0	0	0	0	0	0	0	0
0x05 0002– 0x05 0009	Reserved	0	0	0	0	0	0	0	0
0x05 000A p. 123	ASP Channel 1 Size and Enable	—	—	—	ASP_RX_CH1_AP	ASP_RX_CH1_EN	ASP_RX_CH1_RES	1	0
0x05 000B p. 123	ASP Channel 2 Size and Enable	—	—	—	ASP_RX_CH2_AP	ASP_RX_CH2_EN	ASP_RX_CH2_RES	1	0
0x05 000C– 0x05 FFFF	Reserved	0	0	0	0	0	0	0	0

6.4 DSD Registers

Address	Function	7	6	5	4	3	2	1	0
0x06 0000 p. 124	XSP Channel 1 Location	0	0	0	0	0	0	0	0
0x06 0001 p. 124	XSP Channel 2 Location	0	0	0	0	0	0	0	0
0x06 0002– 0x06 0009	Reserved	0	0	0	0	0	0	0	0
0x06 000A p. 124	XSP Channel 1 Size and Enable	—	—	—	XSP_RX_CH1_AP	XSP_RX_CH1_EN	XSP_RX_CH1_RES	1	0
0x06 000B p. 124	XSP Channel 2 Size and Enable	—	—	—	XSP_RX_CH2_AP	XSP_RX_CH2_EN	XSP_RX_CH2_RES	1	0
0x06 000C– 0x06 FFFF	Reserved	0	0	0	0	0	0	0	0
0x07 0000 p. 124	DSD Volume B	0	1	1	1	1	0	0	0
0x07 0001 p. 125	DSD Volume A	0	1	1	1	1	0	0	0
0x07 0002 p. 125	DSD Processor Path Signal Control 1	DSD_RAMP_UP 1	DSD_VOL_BEQA 0	DSD_SZC 1	—	DSD_AMUTE 0	DSD_AMUTE_BEQA 0	DSD_MUTE_A 0	DSD_MUTE_B 0
0x07 0003 p. 125	DSD Interface Configuration	—	—	—	—	—	DSD_M_SB 0	DSD_PM_EN 0	DSD_PM_SEL 0
0x07 0004 p. 126	DSD Processor Path Signal Control 2	—	DSD_PRC_SRC	DSD_EN	DSD_SPEED	—	STA_DSD_DET 1	INV_DSD_DET 0	—
0x07 0005 p. 126	DSD and PCM Mixing Control	0	0	0	—	—	MIX_PCM_PREP 0	MIX_PCM_DSD 0	—
0x07 0006 p. 126	DSD Processor Path Signal Control 3	DSD_ZERODB 0	DSD_HPF_EN 1	—	SIGCTL_DSDEQPCM 0	DSD_INV_A 0	DSD_INV_B 0	DSD_SWAP_CHAN 0	DSD_COPY_CHAN 0
0x07 0007– 0x07 FFFF	Reserved	0	0	0	0	0	0	0	0

地址	功能	7	6	5	4	3	2	1	0
0x04 0026 第122页	XSP LRCK 周期 1	0	0	1	1	1	1	1	1
0x04 0027 第122页	XSP LRCK 周期 2	0	0	0	0	0	0	0	0
0x04 0028 第122页	XSP 时钟配置	—	—	XSP_M/SB 0	XSP_SCPOL_输出 1	XSP_SCPOL_输入 1	XSP_LCPOL_输出 0	XSP_LCPOL_输入 0	
0x04 0029 第122页	XSP 帧配置	0	—	0	XSP_STP 0	XSP_5050 1	0	XSP_FSD 1	0
0x04 002A~ 0x04 FFFF	保留	0	0	0	0	0	0	0	0
0x05 0000 第123页	ASP 通道 1 位置	0	0	0	0	0	0	0	0
0x05 0001 第123页	ASP 通道 2 位置	0	0	0	0	0	0	0	0
0x05 0002~ 0x05 0009	保留	—	—	—	—	—	—	—	—
0x05 000A 第123页	ASP 通道 1 大小及使能	—	—	XSP_RX_CH1_AP 0	XSP_RX_CH1_EN 1	XSP_RX_CH1_RES 1	—	—	—
0x05 000B 第123页	ASP 通道 2 大小及使能	—	—	XSP_RX_CH2_AP 1	XSP_RX_CH2_EN 1	XSP_RX_CH2_RES 1	—	—	—
0x05 000C~ 0x05 FFFF	保留	—	—	—	—	—	—	—	—

6.4 DSD 寄存器

地址	功能	7	6	5	4	3	2	1	0
0x06 0000 第124页	XSP 通道 1 位置	0	0	0	0	0	0	0	0
0x06 0001 第124页	XSP 通道 2 位置	0	0	0	0	0	0	0	0
0x06 0002~ 0x06 0009	保留	—	—	—	—	—	—	—	—
0x06 000A 第124页	XSP 通道 1 大小及使能	—	—	XSP_RX_CH1_AP 0	XSP_RX_CH1_EN 1	XSP_RX_CH1_RES 1	—	—	—
0x06 000B 第124页	XSP 通道 2 大小及使能	—	—	XSP_RX_CH2_AP 1	XSP_RX_CH2_EN 1	XSP_RX_CH2_RES 1	—	—	—
0x06 000C~ 0x06 FFFF	保留	—	—	—	—	—	—	—	—
0x07 0000 第124页	DSD 音量 B	0	1	1	1	1	0	0	0
0x07 0001 第125页	DSD 音量 A	0	1	1	1	1	0	0	0
0x07 0002 第125页	DSD 处理路径信号控制 1	DSD_RAMP_UP 1	DSD_VOL_BEQA 0	DSD_SZC 1	—	DSD_AMUTE 0	DSD_AMUTE_BEQA 0	DSD_MUTE_A 0	DSD_MUTE_B 0
0x07 0003 第125页	DSD 接口配置	—	0	0	—	0	DSD_M_SB 0	DSD_PM_EN 0	DSD_PM_SEL 0
0x07 0004 第126页	DSD 处理路径信号控制 2	—	0	0	DSD_EN	—	DSD_SPEED 0	STA_DSD_DET 1	INV_DSD_DET 0
0x07 0005 第126页	DSD 与 PCM 混合控制	0	0	0	—	0	0	MIX_PCM_PREP 0	MIX_PCM_DSD 0
0x07 0006 第126页	DSD 处理路径信号控制 3	DSD_ZERODB 0	DSD_HPF_EN 1	—	SIGCTL_DSDEQPPCM 0	DSD_INV_A 0	DSD_INV_B 0	DSD_SWAP_CHAN 0	DSD_COPY_CHAN 0
0x07 0007~ 0x07 FFFF	保留	—	—	—	—	—	—	—	—

6.5 Headphone and PCM Registers

Address	Function	7	6	5	4	3	2	1	0
0x08 0000 p. 127	HP Output Control 1	HP_CLAMPA 0	HP_CLAMPB 0	OUT_FS 1	1	HP_IN_EN 0	HP_IN_LP 0	— 0	+1dB_EN 0
0x09 0000 p. 128	PCM Filter Option	FILTER_SLOW_FASTB 0	PHCOMP_LOWLATB 0	NOS 0	— 0	PCM_WBF_EN 0	HIGH_PASS 1	DEEMP_ON 0	
0x09 0001 p. 128	PCM Volume B	0	1	1	1	PCM_VOLUME_B 1	0	0	0
0x09 0002 p. 128	PCM Volume A	0	1	1	1	PCM_VOLUME_A 1	0	0	0
0x09 0003 p. 129	PCM Path Signal Control 1	PCM_RAMP_DOWN 1	PCM_VOL_BEQA 0	PCM_SZC 1	0	PCM_AMUTE 1	PCM_AMUTEBEQA 0	PCM_MUTE_A 0	PCM_MUTE_B 0
0x09 0004 p. 129	PCM Path Signal Control 2	— 0	0	0	0	PCM_INV_A 0	PCM_INV_B 0	PCM_SWAP_CHAN 0	PCM_COPY_CHAN 0
0x09 000A p. 130	Programmable Filter Control 1	SOS1_CTRL 0	— 0	SOS2_CTRL 0	0	FOS_CTRL 0	SOS3_ON 0	— 0	
0x09 000B p. 130	Programmable Filter Control 2	— 0	0	0	0	SOS1_COEFF_CP 0	SOS2_COEFF_CP 0	FOS_COEFF_CP 0	— 0
0x09 000C p. 130	Programmable Filter Coefficients	0	0	0	0	SOS1_COEFF_B0_LSBYTE 0	0	0	0
0x09 000D p. 130	Programmable Filter Coefficients	1	0	0	0	SOS1_COEFF_B0_MSBYTE 0	0	0	0
0x09 000E p. 130	Programmable Filter Coefficients	— 0	0	0	0	0	0	0	SOS1_COEFF_B0_SIGN 0
0x09 000F p. 130	Programmable Filter Coefficients	0	0	0	0	SOS1_COEFF_B1_LSBYTE 0	0	0	0
0x09 0010 p. 130	Programmable Filter Coefficients	0	0	0	0	SOS1_COEFF_B1_MSBYTE 0	0	0	0
0x09 0011 p. 130	Programmable Filter Coefficients	— 0	0	0	0	0	0	0	SOS1_COEFF_B1_SIGN 0
0x09 0012 p. 130	Programmable Filter Coefficients	0	0	0	0	SOS1_COEFF_B2_LSBYTE 0	0	0	0
0x09 0013 p. 130	Programmable Filter Coefficients	0	0	0	0	SOS1_COEFF_B2_MSBYTE 0	0	0	0
0x09 0014 p. 130	Programmable Filter Coefficients	— 0	0	0	0	0	0	0	SOS1_COEFF_B2_SIGN 0
0x09 0015 p. 130	Programmable Filter Coefficients	0	0	0	0	SOS1_COEFF_A1_LSBYTE 0	0	0	0
0x09 0016 p. 130	Programmable Filter Coefficients	0	0	0	0	SOS1_COEFF_A1_MSBYTE 0	0	0	0
0x09 0017 p. 130	Programmable Filter Coefficients	— 0	0	0	0	0	0	0	SOS1_COEFF_A1_SIGN 0
0x09 0018 p. 130	Programmable Filter Coefficients	0	0	0	0	SOS1_COEFF_A2_LSBYTE 0	0	0	0
0x09 0019 p. 130	Programmable Filter Coefficients	0	0	0	0	SOS1_COEFF_A2_MSBYTE 0	0	0	0
0x09 001A p. 130	Programmable Filter Coefficients	— 0	0	0	0	0	0	0	SOS1_COEFF_A2_SIGN 0
0x09 001B p. 130	Programmable Filter Coefficients	0	0	0	0	SOS2_COEFF_B0_LSBYTE 0	0	0	0
0x09 001C p. 130	Programmable Filter Coefficients	1	0	0	0	SOS2_COEFF_B0_MSBYTE 0	0	0	0

6.5 耳机和 PCM 寄存器

地址	功能	7	6	5	4	3	2	1	0
0x08 0000 第127页	耳机输出控制 1	HP_CLAMPA 0	HP_CLAMPB 0	OUT_FS 1	1	HP_IN_EN 0	HP_IN_LP 0	— 0	+1dB_EN 0
0x09 0000 第128页	PCM 滤波器选项	FILTER_SLOW_FASTB 0	PHCOMP_LOWLATB 0	NOS 0	— 0	PCM_WBF_EN 0	HIGH_PASS 1	DEEMP_ON 0	
0x09 0001 第128页	PCM 音量 B	0	1	1	1	PCM_VOLUME_B 1	0	0	0
0x09 0002 第128页	PCM 音量 A	0	1	1	1	PCM_VOLUME_A 1	0	0	0
0x09 0003 第129页	PCM 路径信号控制 1	PCM_RAMP_DOWN 1	PCM_VOL_BEQA 0	PCM_SZC 1	0	PCM_AMUTE 1	PCM_AMUTEBEQA 0	PCM_MUTE_A 0	PCM_MUTE_B 0
0x09 0004 第129页	PCM 路径信号控制 2	— 0	0	0	0	PCM_INV_A 0	PCM_INV_B 0	PCM_SWAP_CHAN 0	PCM_COPY_CHAN 0
0x09 000A 第130页	可编程滤波器控制 1	SOS1_CTRL 0	— 0	SOS2_CTRL 0	0	FOS_CTRL 0	SOS3_ON 0	— 0	
0x09 000B 第130页	可编程滤波器控制 2	— 0	0	0	0	SOS1系数_CP 0	SOS2系数_CP 0	FOS系数_CP 0	— 0
0x09 000C 第130页	可编程滤波器系数	0	0	0	0	SOS1_COEFF_B0_LSBYTE 0	0	0	0
0x09 000D 第130页	可编程滤波器系数	1	0	0	0	SOS1_COEFF_B0_MSBYTE 0	0	0	0
0x09 000E 第130页	可编程滤波器系数	— 0	0	0	0	0	0	0	SOS1系数_B0_符号 0
0x09 000F 第130页	可编程滤波器系数	0	0	0	0	SOS1_COEFF_B1_LSBYTE 0	0	0	0
0x09 0010 第130页	可编程滤波器系数	0	0	0	0	SOS1_COEFF_B1_MSBYTE 0	0	0	0
0x09 0011 第130页	可编程滤波器系数	— 0	0	0	0	0	0	0	SOS1_COEFF_B1_SIGN 0
0x09 0012 第130页	可编程滤波器系数	0	0	0	0	SOS1_COEFF_B2_LSBYTE 0	0	0	0
0x09 0013 第130页	可编程滤波器系数	0	0	0	0	SOS1_COEFF_B2_MSBYTE 0	0	0	0
0x09 0014 第130页	可编程滤波器系数	— 0	0	0	0	0	0	0	SOS1_COEFF_B2_SIGN 0
0x09 0015 第130页	可编程滤波器系数	0	0	0	0	SOS1_COEFF_A1_LSBYTE 0	0	0	0
0x09 0016 第130页	可编程滤波器系数	0	0	0	0	SOS1_COEFF_A1_MSBYTE 0	0	0	0
0x09 0017 第130页	可编程滤波器系数	— 0	0	0	0	0	0	0	SOS1_COEFF_A1_SIGN 0
0x09 0018 第130页	可编程滤波器系数	0	0	0	0	SOS1_COEFF_A2_LSBYTE 0	0	0	0
0x09 0019 第130页	可编程滤波器系数	0	0	0	0	SOS1_COEFF_A2_MSBYTE 0	0	0	0
0x09 001A 第130页	可编程滤波器系数	— 0	0	0	0	0	0	0	SOS1_COEFF_A2_SIGN 0
0x09 001B 第130页	可编程滤波器系数	0	0	0	0	SOS2_COEFF_B0_LSBYTE 0	0	0	0
0x09 001C 第130页	可编程滤波器系数	1	0	0	0	SOS2_COEFF_B0_MSBYTE 0	0	0	0

Address	Function	7	6	5	4	3	2	1	0
0x09 001D p. 130	Programmable Filter Coefficients				—				SOS2_COEFF_B0_SIGN 0
0x09 001E p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 001F p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 0020 p. 130	Programmable Filter Coefficients				—				SOS2_COEFF_B1_SIGN 0
0x09 0021 p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 0022 p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 0023 p. 130	Programmable Filter Coefficients				—				SOS2_COEFF_B2_SIGN 0
0x09 0024 p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 0025 p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 0026 p. 130	Programmable Filter Coefficients				—				SOS2_COEFF_A1_SIGN 0
0x09 0027 p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 0028 p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 0029 p. 130	Programmable Filter Coefficients				—				SOS2_COEFF_A2_SIGN 0
0x09 002A p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 002B p. 130	Programmable Filter Coefficients	1	0	0	0	0	0	0	0
0x09 002C p. 130	Programmable Filter Coefficients				—				SOS3_COEFF_B0_SIGN 0
0x09 002D p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 002E p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 002F p. 130	Programmable Filter Coefficients				—				SOS3_COEFF_B1_SIGN 0
0x09 0030 p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 0031 p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 0032 p. 130	Programmable Filter Coefficients				—				SOS3_COEFF_B2_SIGN 0
0x09 0033 p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 0034 p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 0035 p. 130	Programmable Filter Coefficients				—				SOS3_COEFF_A1_SIGN 0

地址	功能	7	6	5	4	3	2	1	0
0x09 001D 第130页	可编程滤波器系数				—				SOS2_COEFF_B0_SIGN_0
0x09 001E 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 001F 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 0020 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 0021 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 0022 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 0023 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 0024 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 0025 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 0026 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 0027 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 0028 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 0029 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 002A 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 002B 第130页	可编程滤波器系数	1	0	0	0	0	0	0	0
0x09 002C 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 002D 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 002E 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 002F 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 0030 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 0031 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 0032 第130页	可编程滤波器系数				—				SOS3_COEFF_B2_SIGN_0
0x09 0033 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 0034 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 0035 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0

Address	Function	7	6	5	4	3	2	1	0
0x09 0036 p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 0037 p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 0038 p. 130	Programmable Filter Coefficients	—	—	—	—	—	—	SOS3_COEFF_A2_SIGN	0
0x09 0039 p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 003A p. 130	Programmable Filter Coefficients	1	0	0	0	0	0	0	0
0x09 003B p. 130	Programmable Filter Coefficients	—	—	—	—	—	—	FOS_COEFF_B0_SIGN	0
0x09 003C p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 003D p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 003E p. 130	Programmable Filter Coefficients	—	—	—	—	—	—	FOS_COEFF_B1_SIGN	0
0x09 003F p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 0040 p. 130	Programmable Filter Coefficients	0	0	0	0	0	0	0	0
0x09 0041 p. 130	Programmable Filter Coefficients	—	—	—	—	—	—	FOS_COEFF_A1_SIGN	0
0x0B 0000 p. 131	Class H Control	0	—	0	1	1	1	HV_EN	EXT_VCPFILT
0xD 0000 p. 131	HP Detect	HPDETECT_CTRL	HPDETECT_INV	HPDETECT_RISE_DBC_TIME	HPDETECT_FALL_DBC_TIME	—	—	—	—
0xD 0001 p. 131	HP Status (Read Only)	—	HPDETECT_PLUG_DBC	HPDETECT_UNPLUG_DBC	0	0	0	0	0
0xD 0002– 0xD FFFF	Reserved	0	0	0	0	—	0	0	0
0xE 0000 p. 132	HP Load 1	HPLOAD_EN	—	HPLOAD_CHN_SEL	—	HPLOAD_AC_START	HPLOAD_DC_START	0	0
0xE 0001– 0xE 0002	Reserved	0	0	0	0	0	0	0	0
0xE 0003 p. 132	HP Load Measurement 1	0	0	0	0	0	0	0	0
0xE 0004 p. 132	HP Load Measurement 2	0	0	0	0	0	0	0	0
0xE 0005– 0xE 000C	Reserved	0	0	0	0	0	0	0	0
0xE 000D p. 133	HP DC Load Status 0 (Read Only)	0	0	0	0	0	0	0	0
0xE 000E p. 133	HP DC Load Status 1 (Read Only)	0	0	0	0	0	0	0	0
0xE 000F	Reserved	0	0	0	0	0	0	0	0
0xE 0010 p. 133	HP AC Load Status 0 (Read Only)	0	0	0	0	0	0	0	0
0xE 0011 p. 133	HP AC Load Status 1 (Read Only)	0	0	0	0	0	0	0	0
0xE 0012– 0xE 0019	Reserved	0	0	0	0	—	0	0	0

地址	功能	7	6	5	4	3	2	1	0
0x09 0036 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 0037 第130页	可编程滤波器系数	0	0	0	0	0	0	0	0
0x09 0038 第130页	可编程滤波器系数	—						SOS3_COEFF_A2_SIGN	0
0x09 0039 第130页	可编程滤波器系数	0	0	0	FOS_COEFF_B0_LSBYTE				
0x09 003A 第130页	可编程滤波器系数	1	0	0	FOS_COEFF_B0_MSBYTE				
0x09 003B 第130页	可编程滤波器系数	—						FOS_COEFF_B0_SIGN	0
0x09 003C 第130页	可编程滤波器系数	0	0	0	FOS_COEFF_B1_LSBYTE				
0x09 003D 第130页	可编程滤波器系数	0	0	0	FOS_COEFF_B1_MSBYTE				
0x09 003E 第130页	可编程滤波器系数	—						FOS_COEFF_B1_SIGN	0
0x09 003F 第130页	可编程滤波器系数	0	0	0	FOS_COEFF_A1_LSBYTE				
0x09 0040 第130页	可编程滤波器系数	0	0	0	FOS_COEFF_A1_MSBYTE				
0x09 0041 第130页	可编程滤波器系数	—						FOS_COEFF_A1_SIGN	0
0x0B 0000 第131页	Class H 控制	—	0	0	ADPT_PWR	1	1	HV_EN	EXT_VCPFILT
0xD 0000 第131页	耳机检测	HPDETECT_CTRL	HPDETECT_反向	0	HPDETECT_RISE_DBC_TIME	0	1	HPDETECT_FALL_DBC_TIME	—
0xD 0001 第131页	耳机状态 (只读)	—	HPDETECT_PLUG_DBC	HPDETECT_UNPLUG_DBC	0	0	0	0	0
0xD 0002–0xD FFFF	保留	0	0	0	0	—	0	0	0
0xE 0000 第132页	耳机负载 1	HPLOAD_EN	—	0	HPLOAD_CHN_SEL	—	0	HPLOAD_AC_START	HPLOAD_DC_START
0xE 0001–0xE 0002	保留	0	0	0	0	0	0	0	0
0xE 0003 第132页	耳机负载测量 1	0	0	0	HPLOAD_MEAS_FREQ LSB	0	0	0	0
0xE 0004 第132页	耳机负载测量 2	0	0	0	HPLOAD_MEAS_FREQ MSB	0	0	0	0
0xE 0005–0xE 000C	保留	0	0	0	—	0	0	0	0
0xE 000D 第133页	耳机直流负载状态 0 (只读)	0	0	0	RL_DC_STAT_0	0	0	0	0
0xE 000E 第133页	耳机直流负载状态 1 (只读)	0	0	0	RL_DC_STAT_1	0	0	0	0
0xE 000F	保留	0	0	0	—	0	0	0	0
0xE 0010 第133页	耳机交流负载状态 0 (只读)	0	0	0	RL_AC_STAT_0	0	0	0	0
0xE 0011 第133页	耳机交流负载状态 1 (只读)	0	0	0	RL_AC_STAT_1	0	0	0	0
0xE 0012–0xE 0019	保留	0	0	0	—	0	0	0	0

Address	Function	7	6	5	4	3	2	1	0
0x0E 001A p. 133	HP Load Status (Read Only)	HLOAD_DC_ONCE 0	HLOAD_BUSY 0	— 0	— 0	HLOAD_AC_DONE 0	HLOAD_AC_BUSY 0	HLOAD_DC_DONE 0	HLOAD_DC_BUSY 0
0x0E 001B– 0x0E FFFF	Reserved	0	0	0	0	0	0	0	0

6.6 Interrupt Status and Mask Registers

Address	Function	7	6	5	4	3	2	1	0
0x0F 0000 p. 134	Interrupt Status 1 (Read Only)	DAC_OVFL_INT 0	HP_DETECT_PLUG_INT 0	HP_DETECT_UNPLUG_INT 0	XTAL_READY_INT 0	XTAL_ERROR_INT 0	PLL_READY_INT 0	PLL_ERROR_INT 0	PDN_DONE_INT 0
0x0F 0001 p. 134	Interrupt Status 2 (Read Only)	ASP_OVFL_INT 0	ASP_ERROR_INT 0	ASP_LATE_INT 0	ASP_EARLY_INT 0	ASP_NOLRCK_INT 0	0	0	—
0x0F 0002 p. 135	Interrupt Status 3 (Read Only)	XSP_OVFL_INT 0	XSP_ERROR_INT 0	XSP_LATE_INT 0	XSP_EARLY_INT 0	XSP_NOLRCK_INT 0	—	—	—
0x0F 0003 p. 135	Interrupt Status 4 (Read Only)	HLOAD_NO_DC_INT 0	HLOAD_UNPLUG_INT 0	HLOAD_HPON_INT 0	HLOAD_OOR_INT 0	HLOAD_AC_DONE_INT 0	HLOAD_DC_DONE_INT 0	HLOAD_OFF_INT 0	HLOAD_ON_INT 0
0x0F 0004 p. 136	Interrupt Status 5 (Read Only)	DSD_STUCK_INT 0	DSD_INVAL_A_INT 0	DSD_INVAL_B_INT 0	DSD_SILENCE_A_INT 0	DSD_SILENCE_B_INT 0	DSD_RATE_ERROR_INT 0	DOP_MRK_DET_INT 0	DOP_ON_INT 0
0x0F 0005– 0x0F 000F	Reserved	0	0	0	0	0	0	0	0
0x0F 0010 p. 136	Interrupt Mask 1	DAC_OVFL_INT_MASK 1	HP_DETECT_PLUG_INT_MASK 1	HP_DETECT_UNPLUG_INT_MASK 1	XTAL_READY_INT_MASK 1	XTAL_ERROR_INT_MASK 1	PLL_READY_INT_MASK 1	PLL_ERROR_INT_MASK 1	PDN_DONE_INT_MASK 1
0x0F 0011 p. 137	Interrupt Mask 2	ASP_OVFL_INT_MASK 1	ASP_ERROR_INT_MASK 1	ASP_LATE_INT_MASK 1	ASP_EARLY_INT_MASK 1	ASP_NOLRCK_INT_MASK 1	0	0	—
0x0F 0012 p. 137	Interrupt Mask 3	XSP_OVFL_INT_MASK 1	XSP_ERROR_INT_MASK 1	XSP_LATE_INT_MASK 1	XSP_EARLY_INT_MASK 1	XSP_NOLRCK_INT_MASK 1	1	1	1
0x0F 0013 p. 138	Interrupt Mask 4	HLOAD_NO_DC_INT_MASK 1	HLOAD_UNPLUG_INT_MASK 1	HLOAD_HPON_INT_MASK 1	HLOAD_OOR_INT_MASK 1	HLOAD_AC_DONE_INT_MASK 1	HLOAD_DC_DONE_INT_MASK 1	HLOAD_OFF_INT_MASK 1	HLOAD_ON_INT_MASK 1
0x0F 0014 p. 138	Interrupt Mask 5	DSD_STUCK_INT_MASK 1	DSD_INVAL_A_INT_MASK 1	DSD_INVAL_B_INT_MASK 1	DSD_SILENCE_A_INT_MASK 1	DSD_SILENCE_B_INT_MASK 1	DSD_RATE_ERROR_INT_MASK 1	DOP_MRK_DET_INT_MASK 1	DOP_ON_INT_MASK 1
0x0F 0015– 0x0F FFFF	Reserved	0	0	0	0	0	0	0	0
0x10 0000 p. 139	ASP Master Mode Slew Rate Control	— 0	— 0	— 1	— 0	SCLK1_SLEW_RATE 1 0	— 1	— 0	— 0
0x10 0001 p. 139	XSP Master Mode Slew Rate Control	— 0	— 0	— 1	— 0	DSDCLK_SCLK2_SLEW_RATE 1 0	— 1	— 0	— 0

地址	功能	7	6	5	4	3	2	1	0
0x0E 001A 第133页	耳机负载状态（只读）	HLOAD_DC_— 0	HLOAD忙 0	— 0	— 0	HLOAD_AC_完成 0	HLOAD_AC忙 0	HLOAD_DC完成 0	HLOAD_DC忙 0
0x0E 001B— 0x0E FFFF	保留	0	0	0	0	0	0	0	0

6.6 中断状态与屏蔽寄存器

地址	功能	7	6	5	4	3	2	1	0
0x0F 0000 第134页	中断状态 1 （只读）	DAC_OVFL_INT 0	HP_DETECT_PLUG_INT 0	HP_DETECT_UNPLUG_INT 0	晶体振荡器 READY_INT 0	晶体振荡器 ERROR_INT 0	PLL_READY_INT 0	PLL_ERROR_INT 0	PDN_DONE_INT 0
0x0F 0001 第134页	中断状态 2 （只读）	ASP_OVFL_INT 0	ASP_ERROR_INT 0	ASP_LATE_INT 0	ASP_EARLY_INT 0	ASP_NOLRCK_INT 0	— 0	0	0
0x0F 0002 第135页	中断状态 3 （只读）	XSP_OVFL_INT 0	XSP_ERROR_INT 0	XSP_LATE_INT 0	XSP_EARLY_INT 0	XSP_NOLRCK_INT 0	— 0	0	0
0x0F 0003 第135页	中断状态 4 （只读）	HLOAD_NO_DC_INT 0	HLOAD_UNPLUG_INT 0	HLOAD_HPON_INT 0	HLOAD_OOR_INT 0	HLOAD_AC_DONE_INT 0	HLOAD_DC_DONE_INT 0	HLOAD_OFF_INT 0	HLOAD_ON_中断 0
0x0F 0004 第136页	中断状态 5 （只读）	DSD_STUCK_中断 0	DSD_INVAL_A_中断 0	DSD_INVAL_B_中断 0	DSD_静音_A_中断 0	DSD_静音_B_中断 0	DSD_速率错误_中断 0	DOP_MRK检测_中断 0	DOP_ON_INT 0
0x0F 0005— 0x0F 000F	保留	0	0	0	0	0	0	0	0
0x0F 0010 第136页	中断屏蔽 1	DAC_OVFL_中断屏蔽 1	HP检测插入中断掩码 1	HP检测拔出中断掩码 1	晶体振荡器 READY_INT_MASK 1	晶体振荡器 ERROR_INT_MASK 1	PLL_READY_INT_MASK 1	PLL_ERROR_INT_MASK 1	PDN_DONE_INT_MASK 1
0x0F 0011 第137页	中断屏蔽 2	ASP_OVFL_INT_MASK 1	ASP_ERROR_INT_MASK 1	ASP_LATE_INT_MASK 1	ASP_EARLY_INT_MASK 1	ASP_NOLRCK_INT_MASK 1	— 0	0	0
0x0F 0012 第137页	中断屏蔽 3	XSP_OVFL_INT_MASK 1	XSP_ERROR_INT_MASK 1	XSP_LATE_INT_MASK 1	XSP_EARLY_INT_MASK 1	XSP_NOLRCK_INT_MASK 1	— 1	1	1
0x0F 0013 第138页	中断屏蔽 4	HLOAD_NO_DC_INT_MASK 1	HLOAD_UNPLUG_INT_MASK 1	HLOAD_HPON_INT_MASK 1	HLOAD_OOR_INT_MASK 1	HLOAD_AC_DONE_INT_MASK 1	HLOAD_DC_DONE_INT_MASK 1	HLOAD_OFF_INT_MASK 1	HLOAD_ON_INT_MASK 1
0x0F 0014 第138页	中断屏蔽 5	DSD_STUCK_INT_MASK 1	DSD_INVAL_A_INT_MASK 1	DSD_INVAL_B_INT_MASK 1	DSD_SILENCE_A_INT_MASK 1	DSD_SILENCE_B_INT_MASK 1	DSD_RATE_ERROR_INT_MASK 1	DOP_MRK_DET_INT_MASK 1	DOP_ON_INT_MASK 1
0x0F 0015— 0x0F FFFF	保留	0	0	0	0	0	0	0	0
0x10 0000 第139页	ASP 主模式 转换速率控制	— 0	— 0	— 1	— 0	SCLK1_SLEW_RATE 1 0	— 1	— 0	— 0
0x10 0001 第139页	XSP 主模式 转换速率控制	— 0	— 0	— 1	— 0	DSDCLK_SCLK2_SLEW_RATE 1 0	— 1	— 0	— 0

7 Register Descriptions

All registers are read/write, except for the device's ID, revision, and status registers, which are read only. The following tables describe bit assignments. The default state of each bit after a power-up sequence or reset is listed in each bit description. All reserved bits must maintain their default state.

7.1 Global Registers

7.1.1 Device ID A and B

Address 0x10000

R/O	7	6	5	4	3	2	1	0
DEVIDA								
Default	0	1	0	0	0	0	1	1

Bits	Name	Description
7:4	DEVIDA	Part number first digit: 4
3:0	DEVIDB	Part number second digit: 3

7.1.2 Device ID C and D

Address 0x10001

R/O	7	6	5	4	3	2	1	0
DEVIDC								
Default	0	0	0	1	0	0	1	1

Bits	Name	Description
7:4	DEVIDC	Part number third digit: 1
3:0	DEVIDD	Part number fourth digit: 3

7.1.3 Device ID E

Address 0x10002

R/O	7	6	5	4	3	2	1	0
DEVIDE								
Default	0	0	0	1	0	0	0	0

Bits	Name	Description
7:4	DEVIDE	Part number fifth digit: 1
3:0	—	Reserved

7.1.4 Revision ID

Address 0x10004

R/O	7	6	5	4	3	2	1	0
AREVID								
Default	x	x	x	x	x	x	x	x

Bits	Name	Description
7:4	AREVID	Alpha revision. CS43131 alpha revision level. AREVID and MTLREVID from the complete device revision ID (e.g., A0, B2).
3:0	MTLREVID	Metal revision. CS43131 metal revision level. AREVID and MTLREVID from the complete device revision ID (e.g., A0, B2).

7.1.5 Subrevision ID

Address 0x10005

R/O	7	6	5	4	3	2	1	0
SUBREVID								
Default	0	x	x	x	x	x	x	x

Bits	Name	Description
7:0	SUBREVID	CS43131 subrevision level.

7 寄存器描述

所有寄存器均支持读写，设备ID、版本号及状态寄存器仅支持读取。下表描述了各位的分配情况。每个位在上电序列或复位后的默认状态均在各位描述中列出。所有保留位必须保持其默认状态。

7.1 全局寄存器

7.1.1 设备ID A 和 B 地址 0x10000

只读	7	6	5	4	3	2	1	0
DEVIDA								
默认	0	1	0	0	0	0	1	1

位数	名称	描述
7:4	DEVIDA	零件编号第一位：4
3:0	DEVIDB	零件编号第二位：3

7.1.2 设备ID C和D 地址 0x10001

只读	7	6	5	4	3	2	1	0
DEVIDC								
默认	0	0	0	1	0	0	1	1

位数	名称	描述
7:4	DEVIDC	零件编号第三位：1
3:0	DEVIDD	零件编号第四位：3

7.1.3 设备ID E 地址 0x10002

只读	7	6	5	4	3	2	1	0
设备 ID								
默认	0	0	0	1	0	0	0	0

位数	名称	描述
7:4	设备 ID	零件编号第五位：1
3:0	—	保留

7.1.4 修订版ID 地址 0x10004

只读	7	6	5	4	3	2	1	0
AREVID								
默认	X	X	X	X	X	X	X	X

位数	名称	描述
7:4	AREVID	Alpha版本CS43131 Alpha版本级别完整设备修订版ID中的AREVID和MTLREVID（例如 A0、B2）
3:0	MTLREVID	金属版本CS43131金属版本级别完整设备修订版ID中的AREVID和MTLREVID（例如 A0、B2）

7.1.5 子版本 ID 地址 0x10005

只读	7	6	5	4	3	2	1	0
SUBREVID								
默认	0	X	X	X	X	X	X	X

位数	名称	描述
7:0	SUBREVID	CS43131 子版本级别

7.1.6 System Clocking Control

Address 0x10006

R/W	7	6	5	4	3	2	1	0
	—			—		MCLK_INT		MCLK_SRC_SEL
Default	0	0	0	0	0	1	1	0

Bits	Name	Description
7:3	—	Reserved
2	MCLK_INT	The frequency of internal MCLK. 0 Internal MCLK is expected to be 24.576 MHz 1 (Default) Internal MCLK is expected to be 22.5792 MHz
1:0	MCLK_SRC_SEL	Select the source of internal MCLK. 00 Direct MCLK/XTAL Mode 01 PLL Mode 10 (Default) RCO Mode 11 Reserved

7.1.7 Serial Port Sample Rate

Address 0x1000B

R/W	7	6	5	4	3	2	1	0
	—			—			ASP_SPRATE	
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:4	—	Reserved
3:0	ASP_SPRATE	ASP sample rate. This register must be programmed for both Master Mode and Slave Mode operation. If ASP_SPRATE = 384 kHz and the CS43131 operates in Master Mode, MCLK_INT is required to be 24.576 MHz. For all other rates, MCLK_INT can be either 22.5792 MHz or 24.576 MHz. 0000 32 kHz 0001 (Default) 44.1 kHz 0010 48 kHz 0011 88.2 kHz 0100 96 kHz 0101 176.4 kHz 0110 192 kHz 0111 352.8 kHz 1000 384 kHz 1001–1111 Reserved

7.1.8 Serial Port Sample Bit Size

Address 0x1000C

R/W	7	6	5	4	3	2	1	0
	—			—	XSP_SPSIZE		ASP_SPSIZE	
Default	0	0	0	0	0	1	0	1

Bits	Name	Description
7:4	—	Reserved
3:2	XSP_SPSIZE	XSP sample bit size. 00 32 bits 01 (Default) 24 bits 10–11 Reserved
1:0	ASP_SPSIZE	ASP sample bit size. 00 32 bits 01 (Default) 24 bits 10 16 bits 11 8 bits

7.1.9 Pad Interface Configuration

Address 0x1000D

R/W	7	6	5	4	3	2	1	0
	—			—			XSP_3ST	ASP_3ST
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7:2	—	Reserved

7.1.6 系统时钟控制

地址 0x10006

读/写	7	6	5	4	3	2	1	0
	—			—	MCLK_INT		MCLK_SRC_SEL	
默认	0	0	0	0	0	1	1	0

位数	名称	描述
7:3	—	保留
2	MCLK_INT	内部 MCLK 频率 0 内部 MCLK 预期为 24.576 MHz 1 (默认) 内部 MCLK 预期为 22.5792 MHz
1:0	MCLK_SRC_SEL	选择内部 MCLK 的来源 00 直接 MCLK/晶体振荡器模式 01 PLL 模式 10 (默认) RCO 模式 11 保留

7.1.7 串行端口采样率

地址 0x1000B

读/写	7	6	5	4	3	2	1	0
	—			—	ASP_SPRATE			
默认	0	0	0	0	0	0	0	1

位数	名称	描述
7:4	—	保留
3:0		ASP_SPRATE ASP 采样率该寄存器必须针对主模式和从模式操作进行编程。如果 ASP_SPRATE = 384 kHz 且 CS43131 在主模式下工作，则 MCLK_INT 需为 24.576 MHz。对于所有其他采样率，MCLK_INT 可为 2.5792 MHz 或 24.576 MHz。 0000 32 kHz 0001 (默认) 44.1 kHz 0010 48 kHz 0011 88.2 kHz 0100 96 kHz 0101 176.4 kHz 0110 192 kHz 0111 352.8 kHz 1000 384 kHz 1001–1111 保留

7.1.8 串行端口采样位宽

地址 0x1000C

读/写	7	6	5	4	3	2	1	0
	—			—	XSP_SPSIZE		ASP_SPSIZE	
默认	0	0	0	0	0	1	0	1

位数	名称	描述
7:4	—	保留
3:2	XSP_SPSIZE	XSP 采样位宽。 00 32 位 01 (默认) 24 位 10–11 保留
1:0	ASP_SPSIZE	ASP 采样位数。 00 32 位 01 (默认) 24 位 10 16 位 11 8 位

7.1.9 引脚接口配置

地址 0x1000D

读/写	7	6	5	4	3	2	1	0
	—			—	XSP_3ST		ASP_3ST	
默认	0	0	0	0	0	0	1	1

位数	名称	描述
7:2	—	保留

Bits	Name	Description
1	XSP_3ST	Determines the state of the XSP clock drivers when in Master Mode. When in Slave Mode, the serial port clocks are inputs, whose function is not affected by this bit. Before setting an xSP_3ST bit, the associated serial port must be powered down and not powered up until the xSP_3ST bit is cleared. 0 When in Master Mode, serial port clocks are active. 1 (Default) When in Master Mode, serial port clocks are Hi-Z.
0	ASP_3ST	Determines the state of the ASP clock drivers when in Master Mode. When in Slave Mode, the serial port clock pins are inputs, whose function is not affected by this bit. Before setting an xSP_3ST bit, the associated serial port must be powered down and not powered up until the xSP_3ST bit is cleared. 0 When in Master Mode, serial port clocks are active. 1 (Default) When in Master Mode, serial port clocks are Hi-Z.

7.1.10 Power Down Control

Address 0x20000

R/W	7	6	5	4	3	2	1	0
	PDN_XSP	PDN_ASP	PDN_DSDIF	PDN_HP	PDN_XTAL	PDN_PLL	PDN_CLKOUT	—
Default	1	1	1	1	1	1	1	0

Bits	Name	Description
7	PDN_XSP	XSP input path power control. Configures XSP SDIN path power state. 0 Powered up. 1 (Default) Powered down.
6	PDN_ASP	ASP input path power control. Configures ASP SDIN path power state. 0 Powered up. 1 (Default) Powered down.
5	PDN_DSDIF	DSD interface power control. Sets the power state of the DSD interface block. 0 Powered up. 1 (Default) Powered down.
4	PDN_HP	Power down HPOUTx. 0 Powered up. The HP driver and DACx are powered up. 1 (Default) Powered down. The HP driver and DACx are powered down. When this bit is set, the audio outputs are soft ramped to mute.
3	PDN_XTAL	Power down crystal oscillator. 0 Powered up. The XTAL driver is powered up to start generating MCLK. 1 (Default) Powered down. The XTAL driver is powered down.
2	PDN_PLL	PLL output power control. Sets the power state of the PLL block. 0 Powered up. 1 (Default) Powered down. PLL block is powered down.
1	PDN_CLKOUT	CLKOUT output power control. Sets the power state of the CLOCKOUT output. 0 Powered up 1 (Default) Powered down. CLKOUT are driven low.
0	—	Reserved

7.1.11 Crystal Setting

Address 0x20052

R/W	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	XTAL_IBIAS	—
Default	0	0	0	0	0	1	0	0

Bits	Name	Description
7:3	—	Reserved
2:0	XTAL_IBIAS	Crystal bias current strength. 010 15.0 μ A 100 (Default) 12.5 μ A 110 7.5 μ A Others Reserved

位数	名称	描述
1	XSP_3ST	确定XSP时钟驱动器在主模式下的状态。在从模式下，串行端口时钟为输入，其功能不受此位影响。在设置xSP_3ST位之前，必须关闭相关串行端口电源，且在xSP_3ST位清除之前不得重新上电。 0 在主模式下，串行端口时钟为有效状态。 1 (默认) 在主模式下，串行端口时钟为高阻态。
0	ASP_3ST	确定ASP时钟驱动器在主模式下的状态。在从模式下，串行端口时钟引脚为输入，其功能不受此位影响。在设置xSP_3ST位之前，必须关闭相关串行端口电源，且在xSP_3ST位清除之前不得重新上电。 0 在主模式下，串行端口时钟为有效状态。 1 (默认) 在主模式下，串行端口时钟为高阻态。

7.1.10 断电控制

地址 0x20000

读/写	7	6	5	4	3	2	1	0
	PDN_XSP	PDN_ASP	PDN_DSDIF	PDN_HP	PDN_XTAL	PDN_PLL	PDN_CLKOUT	—
默认	1	1	1	1	1	1	1	0

位数	名称	描述
7	PDN_XSP	XSP 输入路径电源控制。配置 XSP SDIN 路径的电源状态。 0 上电。 1 (默认) 断电。
6	PDN_ASP	ASP 输入路径电源控制。配置 ASP SDIN 路径的电源状态。 0 上电。 1 (默认) 断电。
5	PDN_DSDIF	DSD 接口电源控制。设置 DSD 接口模块的电源状态。 0 上电。 1 (默认) 断电。
4	PDN_HP	断电 HPOUTx。 0 上电。耳机驱动器和 DACx 上电。 1 (默认) 断电。耳机驱动器和 DACx 断电。当该位被设置时，音频输出将软启动至静音。
3	PDN_XTAL	断电晶体振荡器。 0 上电。晶体振荡器驱动器上电，开始生成 MCLK。 1 (默认) 断电。晶体振荡器驱动器断电。
2	PDN_PLL	PLL 输出功率控制。设置 PLL 模块的电源状态。 0 上电。 1 (默认) 断电。PLL 模块已断电。
1	PDN_CLKOUT	CLKOUT 输出功率控制。设置 CLKOUT 输出的电源状态。 0 上电。 1 (默认) 断电，CLKOUT 输出低电平。
0	—	保留

7.1.11 晶体设置

地址 0x20052

读/写	7	6	5	4	3	2	1	0
	—	—	—	—	—	XTAL_IBIAS	—	—
默认	0	0	0	0	0	1	0	0

位数	名称	描述
7:3	—	保留
2:0	XTAL_IBIAS	晶体偏置电流强度。 010 15.0 μ A 100 (默认) 12.5 μ A 110 7.5 μ A 其他 保留

7.2 PLL Registers

7.2.1 PLL Setting 1

Address 0x30001

R/W	7	6	5	4	—	3	2	1	0
Default	0	0	0	0		0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	PLL_START	PLL start bit. Enable PLL output after it has been properly configured. 0 (Default) PLL is not started 1 PLL is started

7.2.2 PLL Setting 2

Address 0x30002

R/W	7	6	5	4	—	3	2	1	0
Default	0	0	0	0		0	0	0	0

Bits	Name	Description
7:0	PLL_DIV_FRAC_0	PLL fractional portion of divide ratio LSB. There are 3 bytes of PLL feedback divider fraction portion and this is LSB byte; e.g., 0xFF means $(2^{-17} + 2^{-18} + \dots + 2^{-24})$. 0000 0000 (Default)

7.2.3 PLL Setting 3

Address 0x30003

R/W	7	6	5	4	—	3	2	1	0
Default	0	0	0	0		0	0	0	0

Bits	Name	Description
7:0	PLL_DIV_FRAC_1	PLL fractional portion of divide ratio middle byte; e.g., 0xFF means $(2^{-9} + 2^{-10} + \dots + 2^{-16})$. 0000 0000 (Default)

7.2.4 PLL Setting 4

Address 0x30004

R/W	7	6	5	4	—	3	2	1	0
Default	0	0	0	0		0	0	0	0

Bits	Name	Description
7:0	PLL_DIV_FRAC_2	PLL fractional portion of divide ratio MSB; e.g., 0xFF means $(2^{-1} + 2^{-2} + \dots + 2^{-8})$. 0000 0000 (Default)

7.2.5 PLL Setting 5

Address 0x30005

R/W	7	6	5	4	—	3	2	1	0
Default	0	1	0	0		0	0	0	0

Bits	Name	Description
7:0	PLL_DIV_INT	PLL integer portion of divide ratio. Integer portion of PLL feedback divider. 0100 0000 (Default)

7.2 PLL 寄存器

7.2.1 PLL 设置 1

地址 0x30001

读/写	7	6	5	4	—	3	2	1	0	PLL_START
默认	0	0	0	0	—	0	0	0	0	

位数	名称	描述
7:1	—	保留
0	PLL_START	PLL 启动位。PLL 配置完成后启用 PLL 输出。 0 (默认) PLL 未启动 1 个 PLL 已启动

7.2.2 PLL 设置 2

地址 0x30002

读/写	7	6	5	4	—	3	2	1	0	PLL_DIV_FRAC_0
默认	0	0	0	0	—	0	0	0	0	

位数	名称	描述
7:0	PLL_DIV_FRAC_0	PLL 分频比小数部分的最低有效位。PLL 反馈分频器的小数部分共有 3 个字节，此为最低有效位字节； 例如，0xFF 表示 $(2^{-17} + 2^{-18} + \dots + 2^{-24})$ 。 0000 0000 (默认)

7.2.3 PLL 设置 3

地址 0x30003

读/写	7	6	5	4	—	3	2	1	0	PLL_DIV_FRAC_1
默认	0	0	0	0	—	0	0	0	0	

位数	名称	描述
7:0	PLL_DIV_FRAC_1	PLL 分频比小数部分的中间字节；例如，0xFF 表示 $(2^{-9} + 2^{-10} + \dots + 2^{-16})$ 。 0000 0000 (默认)

7.2.4 PLL 设置 4

地址 0x30004

读/写	7	6	5	4	—	3	2	1	0	PLL_DIV_FRAC_2
默认	0	0	0	0	—	0	0	0	0	

位数	名称	描述
7:0	PLL_DIV_FRAC_2	PLL 分频比小数部分的最高有效位；例如，0xFF 表示 $(2^{-1} + 2^{-2} + \dots + 2^{-8})$ 。 0000 0000 (默认)

7.2.5 PLL 设置 5

地址 0x30005

读/写	7	6	5	4	—	3	2	1	0	PLL_DIV_INT
默认	0	1	0	0	—	0	0	0	0	

位数	名称	描述
7:0	PLL_DIV_INT	PLL 分频比的整数部分。PLL 反馈分频器的整数部分。 0100 0000 (默认)

7.2.6 PLL Setting 6

Address 0x30008

R/W	7	6	5	4		3	2	1	0
PLL_OUT_DIV									
Default	0	0	0	1		0	0	0	0

Bits	Name	Description
7:0	PLL_OUT_DIV	Final PLL clock output divide value. 0001 0000 (Default)

7.2.7 PLL Setting 7

Address 0x3000A

R/W	7	6	5	4		3	2	1	0
PLL_CAL_RATIO									
Default	1	0	0	0		0	0	0	0

Bits	Name	Description
7:0	PLL_CAL_RATIO	PLL calibration ratio. See Section 4.7.2 for configuration details. Target value for PLL VCO calibration. 1000 0000 (Default)

7.2.8 PLL Setting 8

Address 0x3001B

R/W	7	6	5	4		3	2	1	0
—									
Default	0	0	0	1		0	0	1	1

Bits	Name	Description
7:2	—	Reserved
1	PLL_MODE	500/512 factor used in PLL frequency calculation equation, Eq. 4-1 . 0 No bypass 1 (Default) Bypass
0	—	Reserved

7.2.9 PLL Setting 9

Address 0x40002

R/W	7	6	5	4		3	2	1	0
—									
Default	0	0	0	0		0	0	1	0

Bits	Name	Description
7:2	—	Reserved
1:0	PLL_REF_PREDIV	PLL reference divide select. 00 Divide by 1 01 Divide by 2 10 (Default) Divide by 4 11 Divide by 8

7.2.6 PLL设置6

地址 0x30008

读/写	7	6	5	4		3	2	1	0
PLL_OUT_DIV									
默认	0	0	0	1		0	0	0	0

位数	名称	描述
7:0	PLL_OUT_DIV	最终PLL时钟输出分频值。 0001 0000 (默认)

7.2.7 PLL设置7

地址 0x3000A

读/写	7	6	5	4		3	2	1	0
PLL_CAL_RATIO									
默认	1	0	0	0		0	0	0	0

位数	名称	描述
7:0	PLL_CAL_比率	PLL校准比率。配置详情见第4.7.2节。PLL VCO校准目标值。 1000 0000 (默认)

7.2.8 PLL设置8

地址 0x3001B

读/写	7	6	5	4		3	2	1	0
—									
默认	0	0	0	1		0	0	1	1

位数	名称	描述
7:2	—	保留
1	PLL_MODE	PLL频率计算公式（公式4-1）中使用的500/512因子。 0 无旁路 1 (默认) 旁路
0	—	保留

7.2.9 PLL 设置 9

地址 0x40002

读/写	7	6	5	4		3	2	1	0
—									
默认	0	0	0	0		0	0	1	0

位数	名称	描述
7:2	—	保留
1:0	PLL_REF_PREDIV	PLL 参考分频选择。 00 除以 1 01 除以 2 10 (默认) 除以 4 11 除以 8

7.3 ASP and XSP Registers

7.3.1 CLKOUT Control

Address 0x40004

R/W	7	6	5	4	3	2	1	0
	—	—	—	—	CLKOUT_DIV	—	—	CLKOUT_SEL
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4:2	CLKOUT_DIV	Divider setting on internal MCLK path to CLKOUT. 000 (Default) Divide by 2 001 Divide by 3 010 Divide by 4 011 Divide by 8 100–111 Reserved
1:0	CLKOUT_SEL	Select the source of CLKOUT. 00 (Default) XTAL/MCLK path 01 PLL output path 10–11 Reserved

7.3.2 ASP Numerator 1

Address 0x40010

R/W	7	6	5	4	3	2	1	0
	—	—	—	—	ASP_N_LSB	—	—	—
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:0	ASP_N_LSB	The value in this register cannot be changed while the serial port is powered up. ASP sample rate fractional divide numerator LSB. Along with ASP_M_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) ASP_N = 1

7.3.3 ASP Numerator 2

Address 0x40011

R/W	7	6	5	4	3	2	1	0
	—	—	—	—	ASP_N_MSB	—	—	—
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ASP_N_MSB	The value in this register cannot be changed while the serial port is powered up. ASP sample rate fractional divide numerator MSB. Along with ASP_M_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) ASP_N = 1

7.3.4 ASP Denominator 1

Address 0x40012

R/W	7	6	5	4	3	2	1	0
	—	—	—	—	ASP_M_LSB	—	—	—
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:0	ASP_M_LSB	The value in this register cannot be changed while the serial port is powered up. ASP sample rate fractional divide denominator LSB. Along with ASP_N_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) ASP_M = 8

7.3 ASP 和 XSP 寄存器

7.3.1 CLKOUT 控制

地址 0x40004

读/写	7	6	5	4	3	2	1	0
	—	—	—	—	CLKOUT_DIV			CLKOUT_SEL
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:5	—	保留
4:2	CLKOUT_DIV	内部 MCLK 路径至 CLKOUT 的分频设置。 000 (默认) 除以 2 001 除以 3 010 除以 4 011 除以 8 100–111 保留
1:0	CLKOUT_SEL	选择 CLKOUT 的信号源。 00 (默认) 晶体振荡器/MCLK 路径 01 PLL 输出路径 10–11 保留

7.3.2 ASP 分子 1

地址 0x40010

读/写	7	6	5	4	3	2	1	0
ASP_N_LSB								
默认	0	0	0	0	0	0	0	1

位数	名称	描述
7:0	ASP_N_LSB	串口上电时，寄存器值不可更改。 ASP 采样率分数除法分子最低有效位。与 ASP_M_MSB/LSB 一起选择用于设置 SCLK 频率的分数除法值。 (默认) ASP_N = 1

7.3.3 ASP 分子 2

地址 0x40011

读/写	7	6	5	4	3	2	1	0
ASP_N_MSB								
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:0	ASP_N_MSB	串口上电时，寄存器值不可更改。 ASP 采样率分数除法分子最高有效位。与 ASP_M_MSB/LSB 一起选择用于设置 SCLK 频率的分数除法值。 (默认) ASP_N = 1

7.3.4 ASP 分母 1

地址 0x40012

读/写	7	6	5	4	3	2	1	0
ASP_M_LSB								
默认	0	0	0	0	1	0	0	0

位数	名称	描述
7:0	ASP_M_LSB	串口上电时，寄存器值不可更改。 ASP 采样率分数除法分母最低有效位。与 ASP_N_MSB/LSB 一起选择用于设置 SCLK 频率的分数除法值。 (默认) ASP_M = 8

7.3.5 ASP Denominator 2

Address 0x40013

R/W	7	6	5	4		3	2	1	0
ASP_M_MSB									
Default	0	0	0	0		0	0	0	0

Bits	Name	Description							
7:0	ASP_M_MSB	The value in this register cannot be changed while the serial port is powered up. ASP sample rate fractional divide denominator LSB. Along with ASP_N_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) ASP_M = 8							

7.3.6 ASP LRCK High Time 1

Address 0x40014

R/W	7	6	5	4		3	2	1	0
ASP_LCHI_LSB									
Default	0	0	0	1		1	1	1	1

Bits	Name	Description							
7:0	ASP_LCHI_LSB	The value in this register cannot be changed while the serial port is powered up. ASP LRCK high duration, in units of ASP_SCLK periods stored in ASP_LCHI_MSB/LSB. This value must be less than ASP_LCPR. (Default) ASP_LCHI = 31							

7.3.7 ASP LRCK High Time 2

Address 0x40015

R/W	7	6	5	4		3	2	1	0
ASP_LCHI_MSB									
Default	0	0	0	0		0	0	0	0

Bits	Name	Description							
7:0	ASP_LCHI_MSB	The value in this register cannot be changed while the serial port is powered up. ASP LRCK high duration, in units of ASP_SCLK periods stored in ASP_LCHI_MSB/LSB. This value must be less than ASP_LCPR. (Default) ASP_LCHI = 31							

7.3.8 ASP LRCK Period 1

Address 0x40016

R/W	7	6	5	4		3	2	1	0
ASP_LCPR_LSB									
Default	0	0	1	1		1	1	1	1

Bits	Name	Description							
7:0	ASP_LCPR_LSB	The value in this register cannot be changed while the serial port is powered up. ASP LRCK period, in units of ASP_SCLK periods stored in ASP_LCPR_MSB/LSB. (Default) ASP_LCPR = 63							

7.3.9 ASP LRCK Period 2

Address 0x40017

R/W	7	6	5	4		3	2	1	0
ASP_LCPR_MSB									
Default	0	0	0	0		0	0	0	0

Bits	Name	Description							
7:0	ASP_LCPR_MSB	The value in this register cannot be changed while the serial port is powered up. ASP LRCK period, in units of ASP_SCLK periods stored in ASP_LCPR_MSB/LSB. (Default) ASP_LCPR = 63							

7.3.5 ASP 分母 2

地址 0x40013

读/写	7	6	5	4	3	2	1	0
ASP_M_MSB								
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:0	ASP_M_MSB	串口上电时，寄存器值不可更改。 ASP 采样率分数除法分母最低有效位。与 ASP_N_MSB/LSB 一起选择用于设置 SCLK 频率的分数除法值。 (默认) ASP_M = 8

7.3.6 ASP LRCK 高电平时间 1

地址 0x40014

读/写	7	6	5	4	3	2	1	0
ASP_LCHI LSB								
默认	0	0	0	1	1	1	1	1

位数	名称	描述
7:0	ASP_LCHI_ 最低有效位	串口上电时，寄存器值不可更改。 ASP LRCK 高电平持续时间，单位为 ASP_SCLK 周期，存储于 ASP_LCHI_MSB/LSB 中。该值必须小于 ASP_LCPR 。 (默认) ASP_LCHI = 31

7.3.7 ASP LRCK 高电平时间 2

地址 0x40015

读/写	7	6	5	4	3	2	1	0
ASP_LCHI_MSB								
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:0	ASP_LCHI_ 最高有效位	串口上电时，寄存器值不可更改。 ASP LRCK 高电平持续时间，单位为 ASP_SCLK 周期，存储于 ASP_LCHI_MSB/LSB 中。该值必须小于 ASP_LCPR 。 (默认) ASP_LCHI = 31

7.3.8 ASP LRCK 周期 1

地址 0x40016

读/写	7	6	5	4	3	2	1	0
ASP_LCPR LSB								
默认	0	0	1	1	1	1	1	1

位数	名称	描述
7:0	ASP_LCPR_ 最低有效位	串口上电时，寄存器值不可更改。 ASP LRCK 周期，单位为 ASP_SCLK 周期，存储于 ASP_LCPR_MSB/LSB 中。 (默认) ASP_LCPR = 63

7.3.9 ASP LRCK 周期 2

地址 0x40017

读/写	7	6	5	4	3	2	1	0
ASP_LCPR_MSB								
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:0	ASP_LCPR_ 最高有效位	串口上电时，寄存器值不可更改。 ASP LRCK 周期，单位为 ASP_SCLK 周期，存储于 ASP_LCPR_MSB/LSB 中。 (默认) ASP_LCPR = 63

7.3.10 ASP Clock Configuration

Address 0x40018

R/W	7	6	5	4	3	2	1	0
	—	—	ASP_M/SB	ASP_SCPOL_OUT	ASP_SCPOL_IN	ASP_LCPOL_OUT	ASP_LCPOL_IN	
Default	0	0	0	0	1	1	0	0

Bits	Name	Description
7:5	—	Reserved
4	ASP_M/SB	ASP port master or slave configuration. 0 (Default) Slave Mode (input) 1 Master Mode (output)
3	ASP_SCPOL_OUT	ASP SCLK output drive polarity. 0 Normal 1 (Default) Inverted
2	ASP_SCPOL_IN	ASP SCLK input polarity (pad to logic). 0 Normal 1 (Default) Inverted
1	ASP_LCPOL_OUT	ASP LRCK output drive polarity. 0 (Default) Normal 1 Inverted
0	ASP_LCPOL_IN	ASP LRCK input polarity (pad to logic). 0 (Default) Normal 1 Inverted

7.3.11 ASP Frame Configuration

Address 0x40019

R/W	7	6	5	4	3	2	1	0
	—	—	ASP_STP	ASP_5050	ASP_FSD			
Default	0	0	0	0	1	0	1	0

Bits	Name	Description
7:5	—	Reserved
4	ASP_STP	ASP start phase. Controls which LRCK/FSYNC phase starts a frame. 0 (Default) The frame begins when LRCK/FSYNC transitions from high to low 1 The frame begins when LRCK/FSYNC transitions from low to high
3	ASP_5050	ASP LRCK fixed 50/50 duty cycle. 0 Programmable duty cycle per ASP_LCHI and ASP_LCPR . 1 (Default) Fixed 50% duty cycle
2:0	ASP_FSD	ASP frame start delay (units of ASP_SCLK periods). 000 0 delay 001 0.5 delay 010 (Default) 1.0 delay ... 101 2.5 delay 110-111 Reserved

7.3.12 XSP Numerator 1

Address 0x40020

R/W	7	6	5	4	3	2	1	0
	—	—	—	XSP_N_LSB	—	—	—	—
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:0	XSP_N_LSB	The value in this register cannot be changed while the serial port is powered up. XSP sample rate fractional divide numerator LSB. Along with XSP_M_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) XSP_N = 1

7.3.10 ASP 时钟配置

地址 0x40018

读/写	7	6	5	4	3	2	1	0
	—	—	ASP_M/SB	ASP_SCPOL_输出	ASP_SCPOL_输入	ASP_LCPOL_输出	ASP_LCPOL_输入	
默认	0	0	0	0	1	1	0	0

位数	名称	描述
7:5	—	保留
4	ASP_M/SB	ASP 端口主从配置。 0 (默认) 从模式 (输入) 1 主模式 (输出)
3	ASP_SCPOL_输出	ASP SCLK 输出驱动极性。 0 正常 1 (默认) 反向
2	ASP_SCPOL_输入	ASP SCLK 输入极性 (引脚至逻辑)。 0 正常 1 (默认) 反向
1	ASP_LCPOL_输出	ASP LRCK 输出驱动极性。 0 (默认) 正常 1 反向
0	ASP_LCPOL_输入	ASP LRCK 输入极性 (引脚至逻辑)。 0 (默认) 正常 1 反向

7.3.11 ASP 帧配置

地址 0x40019

读/写	7	6	5	4	3	2	1	0
	—	—	ASP_STP	ASP_5050	ASP_FSD			
默认	0	0	0	0	1	0	1	0

位数	名称	描述
7:5	—	保留
4	ASP_STP	ASP 启动相位。控制哪个 LRCK/FSYNC 相位启动帧。 0 (默认) 帧在 LRCK/FSYNC 从高电平跳变至低电平时开始 1 帧在 LRCK/FSYNC 从低电平跳变至高电平时开始
3	ASP_5050	ASP LRCK 固定 50/50 占空比。 0 通过 ASP_LCHI 和 ASP_LCPR 可编程占空比。 1 (默认) 固定 50% 占空比
2:0	ASP_FSD	ASP 帧启动延迟 (单位为 ASP_SCLK 周期)。 000 0 延迟 001 0.5 延迟 010 (默认) 1.0 延迟 ... 101 2.5 延迟 110-111 保留

7.3.12 XSP 分子 1

地址 0x40020

读/写	7	6	5	4	3	2	1	0
XSP_N_LSB								
默认	0	0	0	0	0	0	0	1

位数	名称	描述
7:0	XSP_N_LSB	串口上电时, 寄存器值不可更改。 XSP 采样率分数除法分子最低有效位。与 XSP_M_MSB/LSB 一起, 用于选择设置 SCLK 频率的分数除法值。 (默认) XSP_N = 1

7.3.13 XSP Numerator 2

Address 0x40021

R/W	7	6	5	4		3	2	1	0
XSP_N_MSB									
Default	0	0	0	0		0	0	0	0

Bits	Name	Description							
7:0	XSP_N_MSB	The value in this register cannot be changed while the serial port is powered up. XSP sample rate fractional divide numerator MSB. Along with XSP_M_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) XSP_N = 1							

7.3.14 XSP Denominator 1

Address 0x40022

R/W	7	6	5	4		3	2	1	0
XSP_M_LSB									
Default	0	0	0	0		0	0	1	0

Bits	Name	Description							
7:0	XSP_M_LSB	The value in this register cannot be changed while the serial port is powered up. XSP sample rate fractional divide denominator LSB. Along with XSP_N_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) XSP_M = 2							

7.3.15 XSP Denominator 2

Address 0x40023

R/W	7	6	5	4		3	2	1	0
XSP_M_MSB									
Default	0	0	0	0		0	0	0	0

Bits	Name	Description							
7:0	XSP_M_MSB	The value in this register cannot be changed while the serial port is powered up. XSP sample rate fractional divide denominator MSB. Along with XSP_N_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) XSP_M = 2							

7.3.16 XSP LRCK High Time 1

Address 0x40024

R/W	7	6	5	4		3	2	1	0
XSP_LCHI_LSB									
Default	0	0	0	1		1	1	1	1

Bits	Name	Description							
7:0	XSP_LCHI_LSB	The value in this register cannot be changed while the serial port is powered up. XSP LRCK high duration, in units of XSP_SCLK periods stored in XSP_LCHI_LSB/MSB. This value must be less than XSP_LCPR. (Default) XSP_LCHI = 31							

7.3.17 XSP LRCK High Time 2

Address 0x40025

R/W	7	6	5	4		3	2	1	0
XSP_LCHI_MSB									
Default	0	0	0	0		0	0	0	0

Bits	Name	Description							
7:0	XSP_LCHI_MSB	The value in this register cannot be changed while the serial port is powered up. XSP LRCK high duration, in units of XSP_SCLK periods stored in XSP_LCHI_LSB/MSB. This value must be less than XSP_LCPR. (Default) XSP_LCHI = 31							

7.3.13 XSP 分子 2

地址 0x40021

读/写	7	6	5	4	3	2	1	0
XSP_N_MSB								
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:0	XSP_N_MSB	串口上电时，寄存器值不可更改。 XSP 采样率分数除法分子最高有效位。与 XSP_M_MSB/LSB 一起，用于选择设置 SCLK 频率的分数除法值。 (默认) XSP_N = 1

7.3.14 XSP 分母 1

地址 0x40022

读/写	7	6	5	4	3	2	1	0
XSP_M_LSB								
默认	0	0	0	0	0	0	1	0

位数	名称	描述
7:0	XSP_M_LSB	串口上电时，寄存器值不可更改。 XSP 采样率分数除法分母最低有效位。与 XSP_N_MSB/LSB 一起，用于选择设置 SCLK 频率的分数除法值。 (默认) XSP_M = 2

7.3.15 XSP 分母 2

地址 0x40023

读/写	7	6	5	4	3	2	1	0
XSP_M_MSB								
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:0	XSP_M_MSB	串口上电时，寄存器值不可更改。 XSP 采样率分数除法分母最高有效位。与 XSP_N_MSB/LSB 一起，用于选择设置 SCLK 频率的分数除法值。 (默认) XSP_M = 2

7.3.16 XSP LRCK 高电平时间 1

地址 0x40024

读/写	7	6	5	4	3	2	1	0
XSP_LCHI_LSB								
默认	0	0	0	1	1	1	1	1

位数	名称	描述
7:0	XSP_LCHI_ 最低有效位	串口上电时，寄存器值不可更改。 XSP LRCK 高电平持续时间，单位为存储于 XSP_LCHI_LSB/MSB 中的 XSP_SCLK 周期数。该值必须小于 XSP_LCPR 。 (默认) XSP_LCHI = 31

7.3.17 XSP LRCK 高电平时间 2

地址 0x40025

读/写	7	6	5	4	3	2	1	0
XSP_LCHI_MSB								
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:0	XSP_LCHI_ 最高有效位	串口上电时，寄存器值不可更改。 XSP LRCK 高电平持续时间，单位为存储于 XSP_LCHI_LSB/MSB 中的 XSP_SCLK 周期数。该值必须小于 XSP_LCPR 。 (默认) XSP_LCHI = 31

7.3.18 XSP LRCK Period 1

Address 0x40026

R/W	7	6	5	4	3	2	1	0
XSP_LCPR_LSB								
Default	0	0	1	1	1	1	1	1

Bits	Name	Description						
7:0	XSP_LCPR_LSB	The value in this register cannot be changed while the serial port is powered up. XSP LRCK period, in units of XSP_SCLK periods stored in XSP_LCPR_LSB/MSB. (Default) XSP_LCPR = 63						

7.3.19 XSP LRCK Period 2

Address 0x40027

R/W	7	6	5	4	3	2	1	0
XSP_LCPR_MSB								
Default	0	0	0	0	0	0	0	0

Bits	Name	Description						
7:0	XSP_LCPR_MSB	The value in this register cannot be changed while the serial port is powered up. XSP LRCK period, in units of XSP_SCLK periods stored in XSP_LCPR_LSB/MSB. (Default) XSP_LCPR = 63						

7.3.20 XSP Clock Configuration

Address 0x40028

R/W	7	6	5	4	3	2	1	0
			—	XSP_M/SB	XSP_SCPOL_OUT	XSP_SCPOL_IN	XSP_LCPOL_OUT	XSP_LCPOL_IN
Default	0	0	0	0	1	1	0	0

Bits	Name	Description						
7:5	—	Reserved						
4	XSP_M/SB	XSP port master or slave configuration. 0 (Default) Slave Mode (input) 1 Master Mode (output)						
3	XSP_SCPOL_OUT	XSP SCLK output drive polarity. 0 Normal 1 (Default) Inverted						
2	XSP_SCPOL_IN	XSP SCLK input polarity (pad to logic). 0 Normal 1 (Default) Inverted						
1	XSP_LCPOL_OUT	XSP LRCK output drive polarity. 0 (Default) Normal 1 Inverted						
0	XSP_LCPOL_IN	XSP LRCK input polarity (pad to logic). 0 (Default) Normal 1 Inverted						

7.3.21 XSP Frame Configuration

Address 0x40029

R/W	7	6	5	4	3	2	1	0
			—	XSP_STP	XSP_5050		XSP_FSD	
Default	0	0	0	0	1	0	1	0

Bits	Name	Description						
7:5	—	Reserved						
4	XSP_STP	XSP start phase. Controls which LRCK/FSYNC phase starts a frame. 0 (Default) The frame begins when LRCK/FSYNC transitions from high to low 1 The frame begins when LRCK/FSYNC transitions from low to high						
3	XSP_5050	XSP LRCK fixed 50/50 duty cycle. 0 Programmable duty cycle per XSP_LCHI and XSP_LCPR 1 (Default) Fixed 50% duty cycle						

7.3.18 XSP LRCK 周期 1

地址 0x40026

读/写	7	6	5	4	3	2	1	0
XSP_LCPR_LSB								
默认	0	0	1	1	1	1	1	1

位数	名称	描述						
7:0	XSP_LCPR_ 最低有效位	串口上电时，寄存器值不可更改。 XSP LRCK 周期，单位为存储于 XSP_LCPR_LSB/MSB 中的 XSP_SCLK 周期数。 (默认)XSP_LCPR = 63						

7.3.19 XSP LRCK 周期 2

地址 0x40027

读/写	7	6	5	4	3	2	1	0
XSP_LCPR_MSB								
默认	0	0	0	0	0	0	0	0

位数	名称	描述						
7:0	XSP_LCPR_ 最高有效位	串口上电时，寄存器值不可更改。 XSP LRCK 周期，单位为存储于 XSP_LCPR_LSB/MSB 中的 XSP_SCLK 周期数。 (默认)XSP_LCPR = 63						

7.3.20 XSP 时钟配置

地址 0x40028

读/写	7	6	5	4	3	2	1	0
	—		XSP_M/SB	XSP_SCPOL_ 输出	XSP_SCPOL_ 输入	XSP_LCPOL_ 输出	XSP_LCPOL_ 输入	
默认	0	0	0	0	1	1	0	0

位数	名称	描述						
7:5	—	保留						
4	XSP_M/SB	XSP 端口主从配置。 0 (默认) 从模式 (输入) 1 主模式 (输出)						
3	XSP_SCPOL_ 输出	XSP SCLK 输出驱动极性。 0 正常 1 (默认) 反向						
2	XSP_SCPOL_ 输入	XSP SCLK 输入极性 (引脚至逻辑)。 0 正常 1 (默认) 反向						
1	XSP_LCPOL_ 输出	XSP LRCK 输出驱动极性。 0 (默认) 正常 1 反向						
0	XSP_LCPOL_ 输入	XSP LRCK 输入极性 (引脚至逻辑)。 0 (默认) 正常 1 反向						

7.3.21 XSP 帧配置

地址 0x40029

读/写	7	6	5	4	3	2	1	0
	—		XSP_STP	XSP_5050		XSP_FSD		
默认	0	0	0	0	1	0	1	0

位数	名称	描述						
7:5	—	保留						
4	XSP_STP	XSP 启动相位。控制哪个 LRCK/FSYNC 相位启动帧。 0 (默认) 帧在 LRCK/FSYNC 从高电平跳变至低电平时开始 1 帧在 LRCK/FSYNC 从低电平跳变至高电平时开始						
3	XSP_5050	XSP LRCK 固定 50/50 占空比。 0 可编程占空比，基于 XSP_LCHI 和 XSP_LCPR 1 (默认) 固定 50% 占空比						

Bits	Name	Description
2:0	XSP_FSD	XSP frame start delay (units of XSP_SCLK periods). 000 0 delay 001 0.5 delay 010 (Default) 1.0 delay ... 101 2.5 delay 110–111 Reserved

7.3.22 ASP Channel 1 and 2 Location

Address 0x50000, 0x50001

R/W	7	6	5	4	3	2	1	0
					ASP_RX_CH1			
					ASP_RX_CH2			

Bits	Name	Description
7:0	ASP_RX_CHn	ASP Rx channel <i>n</i> location. Sets the location in ASP_SCLK periods of the ASP Rx channel <i>n</i> from the start of the TDM frame. 0x00 Start on SCLK 0 ... 0xFF Start on SCLK 255 Defaults are 0x00.

7.3.23 ASP Channel 1 Size and Enable

Address 0x5000A

R/W	7	6	5	4	3	2	1	0
			—		ASP_RX_CH1_AP	ASP_RX_CH1_EN	ASP_RX_CH1_RES	
Default	0	0	0	0	0	1	1	0

7.3.24 ASP Channel 2 Size and Enable

Address 0x5000B

R/W	7	6	5	4	3	2	1	0
			—		ASP_RX_CH2_AP	ASP_RX_CH2_EN	ASP_RX_CH2_RES	
Default	0	0	0	0	1	1	1	0

Bits	Name	Description
7:4	—	Reserved
3	ASP_RX_CHn_AP	ASP RX channel <i>n</i> active phase. Valid only in 50/50 mode (ASP_5050 = 1). 0 (Default when <i>n</i> = 1) In 50/50 mode, channel data is input when LRCK/FSYNC is low 1 (Default when <i>n</i> = 2) In 50/50 mode, channel data is input when LRCK/FSYNC is high
2	ASP_RX_CHn_EN	ASP RX channel <i>n</i> enable. Configures the state of the data for the ASP on channel <i>n</i> . The same rule applies to CHx_EN. 0 (Default) Input channel data is not propagated to the internal data path 1 Input channel data is propagated to the internal data path
1:0	ASP_RX_CHn_RES	ASP RX channel <i>n</i> size (in bits). Sets the output resolution of the ASP RX channel <i>n</i> samples. 00 8 bits per sample 01 16 bits per sample 10 (Default) 24 bits per sample 11 32 bits per sample

位数	名称	描述
2:0	XSP_FSD	XSP 帧启动延迟（以 XSP_SCLK 周期为单位）。 000 0 延迟 001 0.5 延迟 010 (默认) 1.0 延迟 ... 101 2.5 延迟 110-111 保留

7.3.22 ASP 通道 1 和 2 位置

地址 0x50000, 0x50001

读/写 默认	7	6	5	4	3	2	1	0
					ASP_RX_CH1			
					ASP_RX_CH2			

位数	名称	描述
7:0		帧开始的 ASP_SCLK 周期位置。 0x00 从 SCLK 0 开始 ... 0xFF 从 SCLK 255 开始 默认值为 0x00。

7.3.23 ASP 通道 1 大小及使能

地址 0x5000A

读/写 默认	7	6	5	4	3	2	1	0
			—		ASP_RX_CH1_AP	ASP_RX_CH1_EN	ASP_RX_CH1_RES	
	0	0	0	0	0	1	1	0

7.3.24 ASP 通道 2 大小及使能

地址 0x5000B

读/写 默认	7	6	5	4	3	2	1	0
			—		ASP_RX_CH2_AP	ASP_RX_CH2_EN	ASP_RX_CH2_RES	
	0	0	0	0	1	1	1	0

位数	名称	描述
7:4	—	保留
3	ASP_RX_CHn_AP	ASP 接收通道 n 活动相位。仅在 50/50 模式下有效 (ASP_5050 = 1)。 0 (当 $n=1$ 时为默认) 在 50/50 模式下, 通道数据在 LRCK/FSYNC 为低电平时输入。 1 (当 $n=2$ 时为默认) 在 50/50 模式下, 通道数据在 LRCK/FSYNC 为高电平时输入。
2	ASP_RX_CHn_EN	ASP 接收通道 n 使能。配置 ASP 通道 n 的数据状态。同样的规则适用于 CH x _EN。 0 (默认) 输入通道数据不传递至内部数据路径 1 输入通道数据传递至内部数据路径
1:0	ASP_RX_CHn_RES	ASP 接收通道 n 位宽 (位) 设置 ASP 接收通道 n 样本的输出分辨率 00 每样本 8 位 01 每样本 16 位 10 (默认) 每样本 24 位 11 每样本 32 位

7.3.25 XSP Channel 1 and 2 Location

Address 0x60000, 0x60001

R/W	7	6	5	4	3	2	1	0
				XSP_RX_CH1				
				XSP_RX_CH2				
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	XSP_RX_CHn	XSP Rx channel <i>n</i> location. Sets the location in XSP_SCLK periods of the XSP Rx channel <i>n</i> from the start of the TDM frame. 0x00 Start on SCLK 0 ... 0xFF Start on SCLK 255 Defaults are 0x00.

7.3.26 XSP Channel 1 Size and Enable

Address 0x6000A

R/W	7	6	5	4	3	2	1	0
				—	XSP_RX_CH1_AP	XSP_RX_CH1_EN		XSP_RX_CH1_RES
Default	0	0	0	0	0	1	1	0

7.3.27 XSP Channel 2 Size and Enable

Address 0x6000B

R/W	7	6	5	4	3	2	1	1
				—	XSP_RX_CH2_AP	XSP_RX_CH2_EN		XSP_RX_CH2_RES
Default	0	0	0	0	1	1	1	0

Bits	Name	Description
7:4	—	Reserved
3	XSP_RX_CHn_AP	XSP Rx channel <i>n</i> active phase. Valid only in 50/50 mode (XSP_5050 = 1). 0 (Default when <i>n</i> = 1) In 50/50 mode, channel data is input when LRCK/FSYNC is low 1 (Default when <i>n</i> = 2) In 50/50 mode, channel data is input when LRCK/FSYNC is high
2	XSP_RX_CHn_EN	XSP Rx channel <i>n</i> enable. Configures the state of the data for the XSP on channel <i>n</i> . The same rule applies to CHx_EN. 0 Input channel data is not propagated to the internal data path 1 (Default) Input channel data is propagated to the internal data path
1:0	XSP_RX_CHn_RES	XSP Rx channel <i>n</i> size (in bits). Sets the output resolution of the XSP Rx channel <i>n</i> samples. 00 8 bits per sample 01 16 bits per sample 10 (Default) 24 bits per sample 11 32 bits per sample

7.4 DSD Registers

7.4.1 DSD Volume B

Address 0x70000

R/W	7	6	5	4	3	2	1	0
				DSD_VOLUME_B				
Default	0	1	1	1	1	0	0	0

Bits	Name	Description
7:0	DSD_VOLUME_B	Digital volume control registers for DSD processor channel B. It allows independent control of the signal level in 1/2 dB increments from 0 dB. Volume settings are decoded as shown below. The volume changes are dictated by the DSD_SZC bit. The same condition applies to DSD_VOLUME_A setting. 0000 0000 0 dB 0000 0001 -0.5 dB ... 0111 1100 -60 dB (Default) ... 1111 1110 -127 dB 1111 1111 Digital mute

7.3.25 XSP 通道 1 和 2 位置

地址 0x60000, 0x60001

读/写	7	6	5	4	3	2	1	0
				XSP_RX_CH1				
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:0	XSP_RX_CH n	XSP 接收通道 n 位置设置 XSP 接收通道 n 相对于 TDM 帧起始的 XSP_SCLK 周期位置 0x00 从 SCLK 0 开始 ... 0xFF 从 SCLK 255 开始 默认值为 0x00。

7.3.26 XSP 通道 1 大小及使能

地址 0x6000A

读/写	7	6	5	4	3	2	1	0
			—	XSP_RX_CH1_AP	XSP_RX_CH1_使能	XSP_RX_CH1_RES		
默认	0	0	0	0	0	1	1	0

7.3.27 XSP 通道 2 大小及使能

地址 0x6000B

读/写	7	6	5	4	3	2	1	1
			—	XSP_RX_CH2_AP	XSP_RX_CH2_使能	XSP_RX_CH2_RES		
默认	0	0	0	0	1	1	1	0

位数	名称	描述
7:4	—	保留
3	XSP_RX_CH n _AP	XSP 接收通道 n 活动相位。仅在 50/50 模式下有效 (XSP_5050 = 1)。 0 (当 $n=1$ 时为默认) 在 50/50 模式下, 通道数据在 LRCK/FSYNC 为低电平时输入。 1 (当 $n=2$ 时为默认) 在 50/50 模式下, 通道数据在 LRCK/FSYNC 为高电平时输入。
2	XSP_RX_CH n 使能	XSP 接收通道 n 使能。配置通道 n 的 XSP 数据状态。同样的规则适用于 CH x _EN。 0 输入通道数据不传递至内部数据路径 1 (默认) 输入通道数据传递至内部数据路径
1:0	XSP_RX_CH n 分辨率	XSP 接收通道 n 大小 (位数)。设置 XSP 接收通道 n 样本的输出分辨率。 00 每样本 8 位 01 每样本 16 位 10 (默认) 每样本 24 位 11 每样本 32 位

7.4 DSD 寄存器

7.4.1 DSD 音量 B

地址 0x70000

读/写	7	6	5	4	3	2	1	0
				DSD_VOLUME_B				
默认	0	1	1	1	1	0	0	0

位数	名称	描述
7:0	DSD_VOLUME_B	DSD 处理器通道 B 的数字音量控制寄存器。允许从 0 dB 起以 1/2 dB 递增独立控制信号电平。音量设置的解码如下所示。 。音量变化由 DSD_SZC 位控制。DSD_VOLUME_A 设置同样适用此条件。 0000 0000 0 dB 0000 0001 -0.5 dB 0111 1100 -60 dB (默认) 1111 1110 -127 dB 1111 1111 数字静音

7.4.2 DSD Volume A

Address 0x70001

R/W	7	6	5	4	3	2	1	0
DSD_VOLUME_A								
Default	0	1	1	1	1	0	0	0

Bits	Name	Description
7:0	DSD_VOLUME_A	Digital volume control registers for channel A. See DSD_VOLUME_B for description.

7.4.3 DSD Processor Path Signal Control 1

Address 0x70002

R/W	7	6	5	4	3	2	1	0
	DSD_RAMP_UP	DSD_VOL_BEQA	DSD_SZC	—	DSD_AMUTE	DSD_AMUTE_BEQA	DSD_MUTE_A	DSD_MUTE_B
Default	1	0	1	0	1	0	0	0

Bits	Name	Description
7	DSD_RAMP_UP	Soft volume ramp-up after error. An unmute is performed after any error is recovered. 0 Immediate unmute is performed 1 (Default) Unmute behavior is controlled by DSD_SZC settings
6	DSD_VOL_BEQA	DSD_VOLUME_B equals DSD_VOLUME_A. 0 (Default) Volume setting of both channels in DSD processor are controlled independently 1 Volume setting of both channels are controlled by DSD_VOLUME_A. DSD_VOLUME_B is ignored
5	DSD_SZC	Soft ramp control. 0 Immediate change 1 (Default) Soft ramp
4	—	Reserved
3	DSD_AMUTE	DSD auto mute. 0 Function disabled 1 (Default) Mute occurs after reception of 256 repeated 8-bit DSD mute patterns. A single bit not fitting the repeated pattern releases the mute. Detection and muting is done independently for each channel.
2	DSD_AMUTE_BEQA	DSD Processor Auto mute channel B equals channel A. 0 (Default) Function disabled 1 Only mute when both channels AMUTE conditions are detected
1	DSD_MUTE_A	DSD Processor Channel A mute. 0 (Default) Function is disabled 1 Channel output is muted. Muting function is affected by the DSD_SZC bit
0	DSD_MUTE_B	DSD Processor Channel B mute. 0 (Default) Function is disabled. 1 Channel output is muted. Muting function is affected by the DSD_SZC bit.

7.4.4 DSD Interface Configuration

Address 0x70003

R/W	7	6	5	4	3	2	1	0
	—	—	—	—	DSD_M/SB	DSD_PM_EN	DSD_PM_SEL	—
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2	DSD_M/SB	DSD clock master or Slave Mode. 0 (Default) Slave Mode 1 Master Mode
1	DSD_PM_EN	DSD phase modulation mode. Can only be used when DSD_SPEED = 00 (64•Fs) or 01 (128•Fs). 0 (Default) this function is disabled (DSD normal mode) 1 DSD phase modulation input mode is enabled, and the DSD_PM_SEL bit must be set accordingly.
0	DSD_PM_SEL	DSD phase modulation mode select. 0 (Default) The 2x data rate (BCKA) clock must be input to DSD_SCLK for phase modulation mode. 1 The 1x data rate (BCKD) clock must be input to DSD_SCLK for phase modulation mode.

7.4.2 DSD 音量 A

地址 0x70001

读/写	7	6	5	4	3	2	1	0
	DSD_VOLUME_A							
默认	0	1	1	1	1	0	0	0
位数	名称	描述						
7:0	DSD_VOLUME_A	通道 A 的数字音量控制寄存器。详见 DSD_VOLUME_B 描述。						

7.4.3 DSD 处理器路径信号控制 1

地址 0x70002

读/写	7	6	5	4	3	2	1	0
	DSD_RAMP_UP	DSD_VOL_BEQA	DSD_SZC	—	DSD_AMUTE	DSD_AMUTE_BEQA	DSD_MUTE_A	DSD_MUTE_B
默认	1	0	1	0	1	0	0	0
位数	名称	描述						
7	DSD_RAMP_UP	错误后软音量渐增。错误恢复后执行取消静音。 0 立即取消静音 1 (默认) 取消静音行为由 DSD_SZC 设置控制						
6	DSD_VOL_BEQA	DSD_VOLUME_B 等同于 DSD_VOLUME_A。 0 (默认) DSD 处理器中两个通道的音量设置独立控制 1 两个通道的音量设置由 DSD_VOLUME_A 控制, DSD_VOLUME_B 被忽略						
5	DSD_SZC	软斜坡控制。 0 立即变化 1 (默认) 软斜坡						
4	—	保留						
3	DSD_AMUTE	DSD 自动静音。 0 功能禁用 1 (默认) 接收到 256 次重复的 8 位 DSD 静音模式后触发静音单个位不符合重复模式时解除静音。检测和静音独立针对每个通道进行。						
2	DSD_AMUTE_BEQA	DSD 处理器自动静音通道 B 等同于通道 A。 0 (默认) 功能禁用 1 仅当两个通道均检测到 AMUTE 条件时才静音						
1	DSD_MUTE_A	DSD 处理器通道 A 静音。 0 (默认) 功能禁用 1 通道输出静音。静音功能受 DSD_SZC 位影响						
0	DSD_MUTE_B	DSD 处理器通道 B 静音。 0 (默认) 功能禁用。 1 通道输出静音。静音功能受 DSD_SZC 位影响。						

7.4.4 DSD 接口配置

地址 0x70003

读/写	7	6	5	4	3	2	1	0
	—	—	—	—	DSD_M/SB	DSD_PM_EN	DSD_PM_SEL	—
默认	0	0	0	0	0	0	0	0
位数	名称	描述						
7:3	—	保留						
2	DSD_M/SB	DSD 时钟主或从模式。 0 (默认) 从模式 1 主模式						
1	DSD_PM_EN	DSD 相位调制模式。仅当 DSD_SPEED = 00 (64•Fs) 或 01 (128•Fs) 时可用。 0 (默认) 此功能禁用 (DSD 正常模式) 1 启用 DSD 相位调制输入模式, 且必须相应设置 DSD_PM_SEL 位。						
0	DSD_PM	SEL DSD 相位调制模式选择。 0 (默认) 相位调制模式下, 必须将 2 倍数据速率 (BCKA) 时钟输入至 DSD_SCLK。 1 相位调制模式下, 必须将 1 倍数据速率 (BCKD) 时钟输入至 DSD_SCLK。						

7.4.5 DSD Processor Path Signal Control 2

Address 0x70004

R/W	7	6	5	4	3	2	1	0
	—	DSD_PRC_SRC	DSD_EN		DSD_SPEED		STA_DSD_DET	INV_DSD_DET
Default	0	0	0	0	0	0	1	0

Bits	Name	Description
7	—	Reserved
6:5	DSD_PRC_SRC	Select the source for DSD processor. 00 (Default) DSD interface 01 Reserved 10 ASP 11 XSP
4	DSD_EN	Enable DSD playback. 0 (Default) Function disabled 1 DSD playback is enabled
3:2	DSD_SPEED	Setup DSD clock speed. 00 (Default) 64•Fs 01 128•Fs 10 256•Fs 11 Reserved
1	STA_DSD_DET	Static DSD detection. 0 Function disabled 1 (Default) Static DSD detection is enabled. The DSD processor checks for 28 consecutive zeros or ones and, if detected, sets the DSD_STUCK_INT interrupt status bit and mutes the output until the static condition is cleared. If DSD_AMUTE is enabled, AMUTE will be in effect in this scenario.
0	INV_DSD_DET	Invalid DSD detection. 0 (Default) Function disabled 1 Invalid DSD detection is enabled. The DSD processor checks for 25 out of 28 bits of the same value and, if detected, sets the DSD_INVAL_A_INT and/or DSD_INVAL_B_INT interrupt status bits.

7.4.6 DSD and PCM Mixing Control

Address 0x70005

R/W	7	6	5	4	3	2	1	0
	—				MIX_PCM_PREP		MIX_PCM_DSD	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1	MIX_PCM_PREP	Enable PCM playback path for PCM and DSD mixing. This bit must be set prior to setting MIX_PCM_DSD. Disable this bit after disabling MIX_PCM_DSD. This mode requires DSD_EN to be enabled and DSD_PRC_SRC set to receive DSD through either the DSD interface or XSP. 0 (Default) Function disabled 1 Enable PCM playback path for PCM and DSD mixing
0	MIX_PCM_DSD	Enable PCM stream mixing into DSD stream. This bit must be set only after MIX_PCM_PREP is enabled. Disable this bit prior to disabling MIX_PCM_PREP bit. This mode requires DSD_EN to be enabled and DSD_PRC_SRC set to receive DSD through either the DSD interface or XSP. 0 (Default) Function disabled 1 Enable PCM stream mixing into the DSD stream

7.4.7 DSD Processor Path Signal Control 3

Address 0x70006

R/W	7	6	5	4	3	2	1	0
	DSD_ZERODB	DSD_HPF_EN	—	SIGCTL_DSDEQPDM	DSD_INV_A	DSD_INV_B	DSD_SWAP_CHAN	DSD_COPY_CHAN
Default	0	1	0	0	0	0	0	0

Bits	Name	Description
7	DSD_ZERODB	Setting on DSD stream volume to match PCM stream volume. 0 (Default) The SACD +3.1-dB level (71% modulation index) matches PCM 0 dB full scale. 1 The SACD 0-dB reference level (50% modulation index) matches PCM 0 dB full scale.

7.4.5 DSD 处理器路径信号控制 2

地址 0x70004

读/写	7	6	5	4	3	2	1	0
	—	DSD_PRC_SRC	DSD_EN	DSD_SPEED	STA_DSD_DET	INV_DSD_DET		
默认	0	0	0	0	0	0	1	0

位数	名称	描述
7	—	保留
6:5	DSD_PRC_SRC	选择 DSD 处理器的信号源。 00 (默认) DSD 接口 01 保留 10 ASP 11 XSP
4	DSD_EN	启用 DSD 播放。 0 (默认) 功能禁用 1 启用 DSD 播放
3:2	DSD_SPEED	设置 DSD 时钟速度。 00 (默认) 64•采样频率 01 128•采样频率 10 256•采样频率 11 保留
1	STA_DSD_DET	静态 DSD 检测。 0 功能禁用 1 (默认) 启用静态 DSD 检测。DSD 处理器检测连续28个零或一，若检测到，则设置 DSD_STUCK_INT 中断状态位，并静音输出，直到静态状态解除。如果启用 DSD_AMUTE，则在此情况下 AMUTE 将生效。
0	INV_DSD_DET	无效的 DSD 检测。 0 (默认) 功能禁用 1 启用无效 DSD 检测。DSD 处理器检测28位中有25位相同的值，若检测到，则设置 DSD_INVAL_A_INT 和/或 DSD_INVAL_B_INT 中断状态位。

7.4.6 DSD 与 PCM 混合控制

地址 0x70005

读/写	7	6	5	4	3	2	1	0
	—				MIX_PCM_PREP	MIX_PCM_DSD		
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:2	—	保留
1	MIX_PCM_PREP	启用 PCM 播放路径以支持 PCM 与 DSD 混合。此位必须在设置 MIX_PCM_DSD 之前置位。禁用 MIX_PCM_DSD 后需禁用此位。该模式要求启用 DSD_EN，并将 DSD_PRC_SRC 设置为通过 DSD 接口或 XSP 接收 DSD。 0 (默认) 功能禁用 1 启用 PCM 播放路径以实现 PCM 与 DSD 混合
0	MIX_PCM_DSD	启用 PCM 流混合至 DSD 流。此位仅在启用 MIX_PCM_PREP 后设置。在禁用 MIX_PCM_PREP 位之前，必须先禁用此位。此模式要求启用 DSD_EN 并将 DSD_PRC_SRC 设置为通过 DSD 接口或 XSP 接收 DSD。 0 (默认) 功能禁用 1 启用 PCM 流混合至 DSD 流

7.4.7 DSD 处理器路径信号控制 3

地址 0x70006

读/写	7	6	5	4	3	2	1	0
	DSD_ZERO DB	DSD_HPF_EN	—	SIGCTL_DSDEQPCM	DSD_INV_A	DSD_INV_B	DSD_SWAP_CHAN	DSD_COPY_CHAN
默认	0	1	0	0	0	0	0	0

位数	名称	描述
7	DSD_ZERO DB	设置 DSD 流音量以匹配 PCM 流音量。 0 (默认) SACD +3.1 dB 电平 (71% 调制指数) 匹配 PCM 0 dB 满量程。 1 SACD 0 dB 参考电平 (50% 调制指数) 匹配 PCM 0 dB 满量程。

Bits	Name	Description
6	DSD_HPF_EN	Enable the high pass filter in the DSD processor. 0 HPF disabled 1 (Default) Enable HPF in the DSD processor
5	—	Reserved
4	SIGCTL_DSDEQPCM	Enable DSD signal path control register bits to be controlled by PCM setting. DSD setting is ignored. Register bits affected are the following: DSD_RAMP_UP, DSD_VOL_BEQA, DSD_SZC, DSD_AMUTE, DSD_AMUTE_BEQA, DSD_MUTE_A, DSD_MUTE_B, DSD_INV_A, DSD_INV_B, DSD_SWAP_CHAN, DSD_COPY_CHAN After set, each DSD_x register bit is equal to setting of PCM_x register bit. 0 (Default) Function is disabled 1 Function is enabled
3	DSD_INV_A	DSD Processor Channel A signal invert. 0 (Default) Function is disabled 1 Signal polarity of channel A is inverted
2	DSD_INV_B	DSD Processor Channel B signal invert 0 (Default) the function is disabled 1 Signal polarity of channel B is inverted
1	DSD_SWAP_CHAN	Swap channels A and B at the input. This bit takes effect before DSD_COPY_CHAN and DSD_INV_x. 0 (Default) Function disabled 1 Enable channel A and B swapping
0	DSD_COPY_CHAN	Copy channel A to channel B. This bit takes effect after DSD_SWAP_CHAN, but before DSD_INV_x. 0 (Default) Function disabled 1 Enable copy A to B function

7.5 Headphone and PCM Registers

7.5.1 HP Output Control 1

Address 0x80000

R/W	7	6	5	4	3	2	1	0
	HP_CLAMPA	HP_CLAMPB		OUT_FS	HP_IN_EN	HP_IN_LP	—	+1dB_EN
Default	0	0	1	1	0	0	0	0

Bits	Name	Description
7	HP_CLAMPA	Opt-out on clamping HPOUTA output to ground when PDN_HP is enabled. 0 (Default) Function disabled. HPOUTA is clamped when PDN_HP is set and HP_IN_EN is cleared. HPOUT is not clamped when PDN_HP is cleared. 1 HPOUTA clamp is released if and only if PDN_HP is set.
6	HP_CLAMPB	Opt-out on clamping HPOUTB output to ground when PDN_HP is enabled. 0 (Default) Function disabled. HPOUTB is clamped when PDN_HP is set and HP_IN_EN is cleared. HPOUT is not clamped when PDN_HP is cleared. 1 HPOUTB clamp is released if and only if PDN_HP is set.
5:4	OUT_FS	Output full scale setting. This setting must only be updated when PDN_HP is set. 00 0.5 V 01 1 V 10 1.41 V 11 (Default) 1.73 V
3	HP_IN_EN	HPIN switches enable. 0 (Default) Switch open 1 Switch closed
2	HP_IN_LP	When selected, HPIN mode is placed into low power mode. This setting is only in effect when HP_IN_EN = 1. It should only be set after HP_IN_EN = 1. It should be cleared before HP_IN_EN is cleared. When HP_IN_LP = 1, the maximum supported speed for I ² C is 400 kHz. 0 (Default) HPINx path is not in the power mode. 1 HPINx path is in the low power mode.
1	—	Reserved
0	+1dB_EN	If selected, output full scale voltage is at 2 V. This setting is only in effect when OUT_FS = 11 and HV_EN = 1. This setting is ignored if OUT_FS and HV_EN is set to any other settings. It should only be updated when PDN_HP is set. 0 (Default) Output full scale voltage is determined by OUT_FS setting. 1 Output full scale voltage is at 2 V.

位数	名称	描述
6	DSD_HPF_EN	启用 DSD 处理器中的高通滤波器。 0 禁用高通滤波器 1 (默认) 启用DSD处理器中的高通滤波器
5	—	保留
4	SIGCTL_DSDEQPCM	启用DSD信号路径控制寄存器位由PCM设置控制, DSD设置将被忽略。受影响的寄存器位如下: DSD_RAMP_UP、DSD_VOL_BEQA、DSD_SZC、DSD_AMUTE、DSD_AMUTE_BEQA、DSD_MUTE_A、DSD_MUTE_B、DSD_INV_A、DSD_INV_B、DSD_SWAP_CHAN、DSD_COPY_CHAN 设置后, 每个DSD_x寄存器位等同于对应PCM_x寄存器位的设置。 0 (默认) 功能禁用 1 功能已启用
3	DSD_INV_A	DSD处理器通道A信号反相。 0 (默认) 功能禁用 1 通道A信号极性反转
2	DSD_INV_B	DSD处理器通道B信号反相。 0 (默认) 功能禁用 1 通道B信号极性反转
1	DSD_SWAP_CHAN	交换输入端的通道A和通道B。该位在DSD_COPY_CHAN和DSD_INV_x之前生效。 0 (默认) 功能禁用 1 启用通道A和通道B交换
0	DSD_COPY_CHAN	将通道 A 复制到通道 B。该位在 DSD_SWAP_CHAN 之后、DSD_INV_x 之前生效。 0 (默认) 功能禁用 1 启用通道 A 复制到通道 B 功能

7.5 耳机和 PCM 寄存器

7.5.1 耳机输出控制 1

地址 0x80000

读/写	7	6	5	4	3	2	1	0
HP_CLAMPA	HP_CLAMPB		OUT_FS		HP_IN_EN	HP_IN_LP	—	+1dB_EN
默认	0	0	1	1	0	0	0	0

位数	名称	描述
7	HP_CLAMPA	当 PDN_HP 启用时, 选择是否将 HPOUTA 输出钳位至接地。 0 (默认) 功能禁用。当 PDN_HP 置位且 HP_IN_EN 清除时, HPOUTA 被钳位。当 PDN_HP 清除时, HPOUT 不被钳位。 1 仅当 PDN_HP 置位时, 释放 HPOUTA 钳位。
6	HP_CLAMPB	当 PDN_HP 启用时, 选择是否将 HPOUTB 输出钳位至接地。 0 (默认) 功能禁用。当 PDN_HP 置位且 HP_IN_EN 清除时, HPOUTB 被钳位。当 PDN_HP 清除时, HPOUT 不被钳位。 1 仅当 PDN_HP 置位时, 释放 HPOUTB 钳位。
5:4	OUT_FS	输出满量程设置。该设置仅能在 PDN_HP 置位时更新。 00 0.5 V 01 1 V 10 1.41 V 11 (默认)) 1.73 V
3	HP_IN_EN	HPIN 开关使能。 0 (默认) 开关断开 1 开关闭合
2	HP_IN_LP	选中时, HPIN 模式进入低功耗模式。此设置仅在 HP_IN_EN = 1 时生效。仅应在 HP_IN_EN = 1 后设置。应在清除 HP_IN_EN 之前清除此设置。当 HP_IN_LP = 1 时, I ² C 支持的最大速率为 400 kHz。 0 (默认) HPINx 路径不处于低功耗模式。 1 HPINx 路径处于低功耗模式。
1	—	保留
0	+1dB_EN	若选中, 输出满量程电压为 2 V。此设置仅在 OUT_FS = 11 且 HV_EN = 1 时生效。若 OUT_FS 和 HV_EN 设置为其他值, 则忽略此设置。仅应在 PDN_HP 设置时更新。 0 (默认) 输出满量程电压由 OUT_FS 设置决定。 1 输出满量程电压为 2 V。

7.5.2 PCM Filter Option

Address 0x90000

R/W	7	6	5	4	—	3	2	1	0
	FILTER_SLOW_FASTB	PHCOMP_LOWLATB	NOS		—	PCM_WBF_EN	HIGH_PASS	DEEMP_ON	
Default	0	0	0	0		0	0	1	0

Bits	Name	Description
7	FILTER_SLOW_FASTB	Fast and slow filter selection. 0 (Default) Fast filter is selected. 1 Slow filter is selected.
6	PHCOMP_LOWLATB	Low-latency and phase-compensated filter selection 0 (Default) Low-latency is selected. 1 Phase-compensated filter is selected.
5	NOS	Nonoversampling emulation mode on. When enabled, FILTER_SLOW_FASTB and PHCOMP_LOWLATB are ignored. 0 (Default) NOS emulation mode is off. 1 NOS emulation mode is on.
4:3	—	Reserved
2	PCM_WBF_EN	Wideband flatness mode enable. This should only be used in PCM playback when xSP sample rate is at 192 kHz. This bit must be changed while PDN_HP is set. 0 (Default) Wideband flatness mode disabled 1 Wideband flatness mode enabled
1	HIGH_PASS	High-pass filter enable. 0 High-pass filter is disabled. 1 (Default) High-pass filter is selected.
0	DEEMP_ON	Deemphasis filter on. 0 (Default) Deemphasis for 44.1 kHz is disabled. 1 Deemphasis for 44.1 kHz is enabled.

7.5.3 PCM Volume B

Address 0x90001

R/W	7	6	5	4	—	3	2	1	0
PCM_VOLUME_B									
Default	0	1	1	1		1	0	0	0

Bits	Name	Description
7:0	PCM_VOLUME_B	Digital volume control registers for PCM channel B. It allows independent control of the signal level in 1/2 dB increments from 0 to -127.5 dB. Volume settings are decoded as shown below. The volume changes are dictated by the PCM_SZC bits. The same rule applies to PCM_VOLUME_A setting. 0000 0000 0 dB 0000 0001 -0.5 dB ... 01111000 -60 dB (Default) ... 1111 1110 -127 dB 1111 1111 Digital mute

7.5.4 PCM Volume A

Address 0x90002

R/W	7	6	5	4	—	3	2	1	0
PCM_VOLUME_A									
Default	0	1	1	1		1	0	0	0

Bits	Name	Description
7:0	PCM_VOLUME_A	Digital volume control registers for channel A. See PCM_VOLUME_B for description.

7.5.2 PCM 滤波器选项

地址 0x90000

读/写	7	6	5	4	—	3	2	1	0
	FILTER_SLOW_FASTB	PHCOMP_LOWLATB	NOS		—	PCM_WBF_EN	HIGH_PASS	DEEMP_ON	
默认	0	0	0	0	—	0	0	1	0

位数	名称	描述
7	FILTER_SLOW_FASTB	快速和慢速滤波器选择。 0 (默认) 选择快速滤波器。 1 选择慢速滤波器。
6	PHCOMP_LOWLATB	低延迟与相位补偿滤波器选择 0 (默认) 选择低延迟。 1 选择相位补偿滤波器。
5	NOS	开启非过采样仿真模式。启用时, FILTER_SLOW_FASTB 和 PHCOMP_LOWLATB 将被忽略。 0 (默认) 非过采样仿真模式关闭。 1 非过采样仿真模式开启。
4:3	—	保留
2	PCM_WBF_EN	宽带平坦模式使能。仅在 PCM 播放且 xSP 采样率为 192 kHz 时使用。此位必须在 PDN_HP 置位时更改。 0 (默认) 宽带平坦模式禁用。 1 宽带平坦模式使能。
1	HIGH_PASS	高通滤波器使能。 0 高通滤波器已禁用。 1 (默认) 选择高通滤波器。
0	DEEMP_ON	去强调滤波器已开启。 0 (默认) 44.1 kHz 去强调功能已禁用。 1 44.1 kHz 去强调功能已启用。

7.5.3 PCM 音量 B

地址 0x90001

读/写	7	6	5	4	—	3	2	1	0
PCM_VOLUME_B									
默认	0	1	1	1	—	1	0	0	0

位数	名称	描述
7:0	PCM_VOLUME_B	PCM 通道 B 的数字音量控制寄存器, 允许以 0 至 -127.5 dB 范围内, 1/2 dB 递增独立控制信号电平。音量设置的解码如下所示。音量变化由 PCM_SZC 位控制。PCM_VOLUME_A 设置适用相同规则。 0000 0000 0 dB 0000 0001 -0.5 dB ... 01111000 -60 dB (默认) ... 1111 1110 -127 dB 1111 1111 数字静音

7.5.4 PCM 音量 A

地址 0x90002

读/写	7	6	5	4	—	3	2	1	0
PCM_VOLUME_A									
默认	0	1	1	1	—	1	0	0	0

位数	名称	描述
7:0	PCM_VOLUME_A	通道 A 的数字音量控制寄存器, 详见 PCM_VOLUME_B 描述。

7.5.5 PCM Path Signal Control 1

Address 0x90003

R/W	7	6	5	4	3	2	1	0
	PCM_RAMP_DOWN	PCM_VOL_BEQA	PCM_SZC		PCM_AMUTE	PCM_AMUTEBEQA	PCM_MUTE_A	PCM_MUTE_B
Default	1	0	1	0	1	0	0	0

Bits	Name	Description
7	PCM_RAMP_DOWN	Soft volume ramp-down before filter mode change. A mute is performed before filter mode change and an unmute is performed after executing the filter mode change. 0 Immediate mute is performed prior to executing a filter mode change 1 (Default) This mute and unmute is controlled by PCM_SZC.
6	PCM_VOL_BEQA	PCM_VOLUME_B equals PCM_VOLUME_A. 0 (Default) Volume setting of both channels are controlled independently. 1 Volume setting of both channels are controlled by PCM_VOLUME_A. PCM_VOLUME_B is ignored.
5:4	PCM_SZC	Soft ramp and zero cross control. 00 Immediate change 01 In PCM mode, zero cross change 10 (Default) Soft ramp 11 In PCM mode, soft ramp and zero crossings
3	PCM_AMUTE	PCM auto mute. 0 Function disabled 1 (Default) Mute occurs after reception of 8,192 consecutive audio samples of static +1, 0, or -1. A single sample of non-static data releases the mute. Detection and muting is done independently for each channel.
2	PCM_AMUTEBEQA	Auto mute channel B equals channel A. 0 (Default) Function disabled. 1 Only mute when both channels AMUTE conditions are detected.
1	PCM_MUTE_A	Channel A mute. 0 (Default) Function is disabled. 1 Channel output is muted. Muting function is affected by the PCM_SZC bits.
0	PCM_MUTE_B	Channel A mute. 0 (Default) Function is disabled. 1 Channel output is muted. Muting function is affected by the PCM_SZC bits.

7.5.6 PCM Path Signal Control 2

Address 0x90004

R/W	7	6	5	4	3	2	1	0
	—	—	—	—	PCM_INV_A	PCM_INV_B	PCM_SWAP_CHAN	PCM_COPY_CHAN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3	PCM_INV_A	Channel A signal invert. 0 (Default) Function is disabled 1 Signal polarity of channel A is inverted
2	PCM_INV_B	Channel B signal invert. 0 (Default) the function is disabled 1 Signal polarity of channel B is inverted
1	PCM_SWAP_CHAN	Swap channels A and B at the input. This bit takes effect before PCM_COPY_CHAN. 0 (Default) Function disabled 1 Enable channel A and B swapping
0	PCM_COPY_CHAN	Copy channel A to channel B. This bit takes effect after PCM_SWAP_CHAN. 0 (Default) Function disabled 1 Enable copy A to B function

7.5.5 PCM 路径信号控制 1

地址 0x90003

读/写	7	6	5	4	3	2	1	0
	PCM_RAMP_DOWN	PCM_VOL_BEQA	PCM_SZC		PCM_AMUTE	PCM_AMUTEBEQA	PCM_MUTE_A	PCM_MUTE_B
默认	1	0	1	0	1	0	0	0

位数	名称	描述
7	PCM_RAMP_DOWN	滤波器模式切换前的软音量渐降。滤波器模式切换前执行静音，滤波器模式切换后执行取消静音。 0 在执行滤波器模式切换前立即静音。 1 (默认) 该静音和取消静音由 PCM_SZC 控制。
6	PCM_VOL_BEQA	PCM_VOLUME_B 等于 PCM_VOLUME_A。 0 (默认) 两个通道的音量设置独立控制。 1 两个通道的音量设置由 PCM_VOLUME_A 控制，忽略 PCM_VOLUME_B。
5:4	PCM_SZC	软渐变和零交叉控制。 00 立即变化。 01 在 PCM 模式下，零交叉变化。 10 (默认) 软渐变。 11 在 PCM 模式下，软渐变和零交叉。
3	PCM_AMUTE	PCM 自动静音。 0 功能禁用 1 (默认) 接收连续 8,192 个静态 +1、0 或 -1 的音频样本后触发静音。单个非静态样本将解除静音。检测和静音独立针对每个通道进行。
2	PCM_AMUTEBEQA	自动静音通道 B 等同于通道 A。 0 (默认) 功能禁用。 1 仅当两个通道均检测到 AMUTE 条件时才静音。
1	PCM_ 静音_A	通道A静音。 0 (默认) 功能禁用。 1 通道输出静音。静音功能受PCM_SZC位控制。
0	PCM_ 静音_B	通道A静音。 0 (默认) 功能禁用。 1 通道输出静音。静音功能受PCM_SZC位控制。

7.5.6 PCM路径信号控制2

地址 0x90004

读/写	7	6	5	4	3	2	1	0
	—	—	—	—	PCM_INV_A	PCM_INV_B	PCM_SWAP_CHAN	PCM_COPY_CHAN
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:4	—	保留
3	PCM_INV_A	通道A信号反相。 0 (默认) 功能禁用。 1 通道A信号极性反转
2	PCM_INV_B	通道B信号反相。 0 (默认) 功能禁用。 1 通道B信号极性反转
1	PCM_SWAP_CHAN	交换输入端的通道A和通道B。该位在PCM_COPY_CHAN之前生效。 0 (默认) 功能禁用。 1 启用通道A和通道B交换
0	PCM_COPY_CHAN	将通道A复制到通道B。该位在PCM_SWAP_CHAN之后生效。 0 (默认) 功能禁用。 1 启用通道 A 复制到通道 B 功能

7.5.7 Programmable Filter Control 1

Address 0x9 000A

R/W	7	6	5	4	3	2	1	0
	SOS1_CTRL		SOS2_CTRL		FOS_CTRL		SOS3_ON	—
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	SOS1_CTRL	SOS1 filter control. 00 SOS1 filter disabled. 01 Reserved. 10 Reserved. 11 SOS1 filter enabled.
5:4	SOS2_CTRL	SOS2 filter control. 00 SOS2 filter disabled. 01 Reserved. 10 Reserved. 11 SOS2 filter enabled.
3:2	FOS_CTRL	FOS filter control. 00 FOS filter disabled. 01 Reserved. 10 Reserved. 11 FOS filter enabled.
1	SOS3_ON	SOS3 filter enable. 0 (default) SOS3 filter is disabled. 1 SOS3 filter is enabled.
0	—	Reserved

7.5.8 Programmable Filter Control 2

Address 0x9 000B

R/W	7	6	5	4	3	2	1	0
			—		SOS1_COEFF_CP	SOS2_COEFF_CP	FOS_COEFF_CP	—
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3	SOS1_COEFF_CP	Enable SOS1 coefficients from the control port. When the filter is not in use, this bit must be cleared to 0. 0 (default) SOS1 coefficients from the control port are not effective. 1 SOS1 coefficients from the control port are effective.
2	SOS2_COEFF_CP	Enable SOS2 coefficients from the control port. When the filter is not in use, this bit must be cleared to 0. 0 (default) SOS2 coefficients from the control port are not effective. 1 SOS2 coefficients from the control port are effective.
1	FOS_COEFF_CP	Enable FOS coefficients from the control port. When the filter is not in use, this bit must be cleared to 0. 0 (default) FOS coefficients from the control port are not effective. 1 FOS coefficients from the control port are effective.
0	—	Reserved

7.5.9 Programmable Filter Coefficients

Address 0x9000C–0x90041

R/W	7	6	5	4	3	2	1	0
				xOSx_COEFF_xx_LSBYTE				
				xOSx_COEFF_xx_MSBYTE				
				—				xOSx_COEFF_xx_SIGN
Default	See Quick Reference							

Bits	Name	Description
7:0	See Quick Reference	Refer to Section 4.14 for details. Format is Q1.17.

7.5.7 可编程滤波器控制1

地址 0x9000A

读/写	7	6	5	4	3	2	1	0
	SOS1_CTRL		SOS2_CTRL		FOS_CTRL		SOS3_ON	—
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:6	SOS1_CTRL	SOS1滤波器控制。 00 SOS1滤波器禁用。 01 保留。 10 保留。 11 SOS1滤波器启用。
5:4	SOS2_CTRL	SOS2滤波器控制。 00 SOS2 滤波器禁用。 01 保留。 10 保留。 11 SOS2 滤波器启用。
3:2	FOS_CTRL	FOS 滤波器控制。 00 FOS 滤波器禁用。 01 保留。 10 保留。 11 FOS 滤波器启用。
1	SOS3_ON	启用 SOS3 滤波器。 0 (默认) SOS3 滤波器禁用。 1 SOS3 滤波器启用。
0	—	保留

7.5.8 可编程滤波器控制 2

地址 0x9000B

读/写	7	6	5	4	3	2	1	0
			—		SOS1_系数_CP	SOS2_系数_CP	FOS_系数_CP	—
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:4	—	保留
3	SOS1_系数_CP	启用来自控制端口的 SOS1 系数。滤波器未使用时，此位必须清零。 0 (默认) 来自控制端口的 SOS1 系数无效。 1 来自控制端口的 SOS1 系数有效。
2	SOS2_系数_CP	启用来自控制端口的 SOS2 系数。滤波器未使用时，此位必须清零。 0 (默认) 来自控制端口的 SOS2 系数无效。 1 来自控制端口的 SOS2 系数有效。
1	FOS_系数_CP	启用来自控制端口的 FOS 系数。滤波器未使用时，此位必须清零。 控制端口的0 (默认) FOS系数无效。 控制端口的1 FOS系数有效。
0	—	保留

7.5.9 可编程滤波器系数

地址 0x9000C–0x90041

读/写	7	6	5	4	3	2	1	0
				xOSx_COEFF_xx_LSBYTE				
				xOSx_COEFF_xx_MSBYTE				
				—				xOSx_COEFF_xx_SIGN
默认	参见快速参考							

位数	名称	描述
7:0	参见快速参考	详情请参阅第4.14节。格式为Q1.17。

7.5.10 Class H Control

Address 0xB0000

R/W	7	6	5	4	3	2	1	0
	—	—	—	—	ADPT_PWR	—	HV_EN	EXT_VCPFILT
Default	0	0	0	1	1	1	1	0

Bits	Name	Description
7:5	—	Reserved
4:2	ADPT_PWR	Adaptive power adjustment. Configures how power to HP amplifiers adapts to the output signal level. 000 Reserved 001 Fixed, Mode 0 (\pm VP_LDO) 010 Fixed, Mode 1 (\pm VCP) 011–110 Reserved 111 (Default) Adapt to signal. The output signal dynamically determines the voltage level.
1	HV_EN	High voltage mode enable. 0 Function disabled (VP_LDO = 2.6V) 1 (Default) Function enabled (VP_LDO = 3.0 V). This requires VP min to be 3.3 V. Also, this mode only applies to load 600 Ω and above.
0	EXT_VCPFILT	External VCP_FILT \pm voltage mode. 0 (Default) Function disabled 1 When enabled, VCP_FILT \pm voltages can be provided externally at \pm 3.0 V. See power sequencing/timing requirement in related functional description.

7.5.11 HP Detect

Address 0xD0000

R/W	7	6	5	4	3	2	1	0
	HPDETECT_CTRL	HPDETECT_INV	HPDETECT_RISE_DBC_TIME	HPDETECT_FALL_DBC_TIME	—	—	—	—
Default	0	0	0	0	0	1	0	0

Bits	Name	Description
7:6	HPDETECT_CTRL	HP detect control. Configures operation of the HP detect circuit. The internal weak current source pull-up is enabled in all modes. 00 (Default) Disabled. The HP detect digital circuit is powered down and does not report to the status registers (HPDETECT_PLUG_INT and HPDETECT_UNPLUG_INT are also cleared). 01–10 Reserved 11 Enabled
5	HPDETECT_INV	HP detect invert. Can be used to invert the signal from the HP detect circuit. 0 (Default) Not inverted 1 Inverted
4:3	HPDETECT_RISE_DBC_TIME	Tip sense rising debounce time. 00 0 ms 01 250 ms 10 500 ms 11 1.0 s
2:1	HPDETECT_FALL_DBC_TIME	Tip sense falling debounce time. 00 0 ms 01 250 ms 10 (Default) 500 ms 11 1.0 s
0	—	Reserved

7.5.12 HP Status

Address 0xD0001

R/O	7	6	5	4	3	2	1	0
	—	HPDETECT_PLUG_DBC	HPDETECT_UNPLUG_DBC	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6	HPDETECT_PLUG_DBC	HPDETECT plug debounce status. Setting HPDETECT_INV reverses the meaning of this bit. 0 (Default) Condition is not present 1 Condition is present

7.5.10 Class H 控制

地址 0xB0000

读/写	7	6	5	4	3	2	1	0
	—	—	—	—	ADPT_PWR	—	HV_EN	EXT_VCPFILT
默认	0	0	0	1	1	1	1	0

位数	名称	描述
7:5	—	保留
4:2	ADPT_PWR	自适应功率调整。配置耳机放大器功率如何根据输出信号电平自适应。 000 保留 001 固定，模式0 ($\pm V_{P_LDO}$) 010 固定，模式1 ($\pm V_{CP}$) 011–110 保留 111 (默认) 根据信号自适应。输出信号动态决定电压等级。
1	HV_EN	高压模式使能。 0 功能禁用 ($V_{P_LDO} = 2.6\text{ V}$) 1 (默认) 功能启用 ($V_{P_LDO} = 3.0\text{ V}$)。此时 V_P 最小值需为 3.3 V 。此外，该模式仅适用于负载 $600\ \Omega$ 及以上。
0	EXT_VCPFILT	外部 VCP_FILT \pm 电压模式。 0 (默认) 功能禁用 1 启用时，VCP_FILT \pm 电压可由外部提供，电压为 $\pm 3.0\text{ V}$ 。详见相关功能描述中的电源时序要求。

7.5.11 耳机检测

地址 0xD0000

读/写	7	6	5	4	3	2	1	0
	HPDETECT_CTRL	HPDETECT_INV	HPDETECT_RISE_DBC_TIME	HPDETECT_FALL_DBC_TIME	—	—	—	—
默认	0	0	0	0	0	1	0	0

位数	名称	描述
7:6	HPDETECT_CTRL	耳机检测控制。配置耳机检测电路的操作方式。所有模式下均启用内部弱电流源上拉。 00 (默认) 禁用。耳机检测数字电路断电，不向状态寄存器报告 (HPDETECT_PLUG_INT 和 HPDETECT_UNPLUG_INT 也被清除)。 01–10 保留 11 启用
5	HPDETECT_INV	耳机检测信号反转。可用于反转耳机检测电路的信号。 0 (默认) 不反转 1 反向
4:3	HPDETECT_RISE_DBC_TIME	插头检测上升沿消抖时间。 00 (默认) 0 毫秒 01 250 毫秒 10 500 毫秒 11 1.0 秒
2:1	HPDETECT_FALL_DBC_TIME	插头检测下降沿消抖时间。 00 0 毫秒 01 250 毫秒 10 (默认) 500 毫秒 11 1.0 秒
0	—	保留

7.5.12 耳机状态

地址 0xD0001

只读	7	6	5	4	3	2	1	0
	—	HPDETECT_PLUG_DBC	HPDETECT_UNPLUG_DNC	—	—	—	—	—
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7	—	保留
6	HPDETECT_PLUG_DBC	HPDETECT 插入消抖状态。设置 HPDETECT_INV 可反转该位的含义。 0 (默认) 条件不存在 1 条件存在

Bits	Name	Description						
5	HPDETECT_UNPLUG_DBC	HPDETECT unplug debounce status. Setting HPDETECT_INV reverses the meaning of this bit. 0 (Default) Condition is not present 1 Condition is present						
4:0	—	Reserved						

7.5.13 HP Load 1

Address 0xE0000

R/W	7	6	5	4	3	2	1	0
	HPLOAD_EN	—	—	HPLOAD_CHN_SEL	—	—	HPLOAD_AC_START	HPLOAD_DC_START
Default	0	0	0	0	0	0	0	0

Bits	Name	Description						
7	HPLOAD_EN	HP load enable. 0 (Default) Function disabled 1 Function enabled						
6:5	—	Reserved						
4	HPLOAD_CHN_SEL	Select channel to perform HP load measurement. 0 (Default) HPOUTA 1 HPOUTB						
3:2	—	Reserved						
1	HPLOAD_AC_START	HP load AC measurement trigger. A change from 0 to 1 initiates the measurement process. After the measurement completes, this bit must be manually changed back to 0 before initiating another process. (Default) HPLOAD_AC_START = 0						
0	HPLOAD_DC_START	HP load DC measurement trigger. A change from 0 to 1 initiates the measurement process. After measurement complete, this bit must be manually changed back to 0 before initiating another process. (Default) HPLOAD_DC_START = 0						

7.5.14 HP Load Measurement 1

Address 0xE0003

R/W	7	6	5	4	3	2	1	0
HPOLOAD_MEAS_FREQ_LSB								
Default	0	0	0	0	0	0	0	0

Bits	Name	Description						
7:0	HPOLOAD_MEAS_FREQ_LSB	LSB of HP load measurement frequency selection for AC detect (5.86 Hz/lb when MCLK_INT = 24.576 MHz. 5.94 Hz/lb when MCLK_INT = 22.5792 MHz). Frequency range is 20 Hz to 20 kHz. Default: 0000 0000						

7.5.15 HP Load Measurement 2

Address 0xE0004

R/W	7	6	5	4	3	2	1	0
HPOLOAD_MEAS_FREQ_MSB								
Default	0	0	0	0	0	0	0	0

Bits	Name	Description						
7:0	HPOLOAD_MEAS_FREQ_MSB	MSB of HP load measurement frequency selection for AC detect (5.86 Hz/lb when MCLK_INT = 24.576 MHz. 5.94 Hz/lb when MCLK_INT = 22.5792 MHz). Frequency range is 20 Hz to 20 kHz. Default: 0000 0000						

位数	名称	描述
5	HPDETECT_UNPLUG_DBC	HPDETECT 拔出消抖状态。设置 HPDETECT_INV 可反转该位的含义。 0 (默认) 条件不存在 1 条件存在
4:0	—	保留

7.5.13 耳机负载 1

地址 0xE0000

读/写	7	6	5	4	3	2	1	0
	HPLOAD_EN	—	—	HPLOAD_CHN_SEL	—	—	HPLOAD_AC_START	HPLOAD_DC_START
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7	HPLOAD_EN	耳机负载使能。 0 (默认) 功能禁用 1 功能使能
6:5	—	保留
4	HPLOAD_CHN_SEL	选择通道以执行耳机负载测量。 0 (默认) HPOUTA 1 HPOUTB
3:2	—	保留
1	HPLOAD_AC_START	耳机负载交流测量触发。从 0 变为 1 启动测量过程。测量完成后，必须手动将该位改回 0，方可启动下一次测量。 (默认) HPLOAD_AC_START = 0
0	HPLOAD_DC_START	耳机负载直流测量触发。从 0 变为 1 启动测量过程。测量完成后，必须手动将此位清零，方可启动下一次测量。 (默认) HPLOAD_DC_START = 0

7.5.14 耳机负载测量 1

地址 0xE0003

读/写	7	6	5	4	3	2	1	0
	HPLOAD_MEAS_FREQ_LSB							
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:0	HPLOAD_MEAS_FREQ_LSB	用于交流检测的耳机负载测量频率选择的最低有效位 (当 MCLK_INT = 24.576 MHz 时, 5.86 Hz/最低有效位; 当 MCLK_INT = 22.5792 MHz 时, 5.94 Hz/最低有效位)。频率范围为 20 Hz 至 20 kHz。 默认值: 0000 0000

7.5.15 耳机负载测量 2

地址 0xE0004

读/写	7	6	5	4	3	2	1	0
	HPLOAD_MEAS_FREQ_MSB							
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:0	HPLOAD_MEAS_FREQ_MSB	用于交流检测的耳机负载测量频率选择的最高有效位 (当 MCLK_INT = 24.576 MHz 时, 5.86 Hz/最低有效位; 当 MCLK_INT = 22.5792 MHz 时, 5.94 Hz/最低有效位)。频率范围为 20 Hz 至 20 kHz。 默认值: 0000 0000

7.5.16 HP DC Load Status 0

Address 0xE000D

R/O	7	6	5	4	3	2	1	0
RL_DC_STAT_0								
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	RL_DC_STAT_0	Byte 0 of HP DC load measured in Ω . RL_DC_STAT_1[7:0] and RL_DC_STAT_0[7:3] represent integer portion of impedance value. RL_DC_STAT_0[2:0] represent fractional portion, with fractional weighting as follows: [2]: 0.5 [1]: 0.25 [0]: 0.125 Default: 0000000

7.5.17 HP DC Load Status 1

Address 0xE000E

R/O	7	6	5	4	3	2	1	0
RL_DC_STAT_1								
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	RL_DC_STAT_1	Byte 1 of HP DC load measured in Ω . Refer to RL_DC_STAT_0 for details of measurement interpretation. Default: 0000000

7.5.18 HP AC Load Status 0

Address 0xE0010

R/O	7	6	5	4	3	2	1	0
RL_AC_STAT_0								
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	RL_AC_STAT_0	Byte 0 of HP AC load measured in Ω . RL_AC_STAT_1[7:0] and RL_AC_STAT_0[7:3] represent integer portion of impedance value. RL_AC_STAT_0[2:0] represent fractional portion, with fractional weighting as follows: [2]: 0.5 [1]: 0.25 [0]: 0.125 Default: 0000000

7.5.19 HP AC Load Status 1

Address 0xE0011

R/O	7	6	5	4	3	2	1	0
RL_AC_STAT_1								
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	RL_AC_STAT_1	Byte 1 of HP AC load measured in Ω . Refer to RL_AC_STAT_0 for details of measurement interpretation. Default: 0000000

7.5.20 HP Load Status

Address 0xE001A

R/O	7	6	5	4	3	2	1	0
	HLOAD_DC_ONCE	HLOAD_BUSY	—	—	HLOAD_AC_DONE	HLOAD_AC_BUSY	HLOAD_DC_DONE	HLOAD_DC_BUSY
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	HLOAD_DC_ONCE	Status of HP load DC measurement been performed at least once. 0 Condition is not present 1 Condition is present
6	HLOAD_BUSY	Status of HP load measurement block state machine. 0 State machine is not busy 1 State machine is busy

7.5.16 耳机直流负载状态 0

地址 0xE000D

只读	7	6	5	4	3	2	1	0
RL_DC_STAT_0								
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:0	RL_DC_STAT_0	耳机直流负载测量的第 0 字节，单位为 Ω 。RL_DC_STAT_1[7:0] 和 RL_DC_STAT_0[7:3] 表示阻抗值的整数部分。 RL_DC_STAT_0[2:0] 表示小数部分，其小数权重如下： [2]: 0.5 [1]: 0.25 [0]: 0.125 默认值：0000000

7.5.17 耳机直流负载状态 1

地址 0xE000E

只读	7	6	5	4	3	2	1	0
RL_DC_STAT_1								
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:0	RL_DC_STAT_1	耳机直流负载测量的第 1 字节，单位为 Ω 。测量解释详情请参见 RL_DC_STAT_0。 默认值：0000000

7.5.18 耳机交流负载状态 0

地址 0xE0010

只读	7	6	5	4	3	2	1	0
RL_AC_STAT_0								
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:0	RL_AC_STAT_0	耳机交流负载测量的第 0 字节，单位为 Ω 。 RL_AC_STAT_1[7:0] 和 RL_AC_STAT_0[7:3] 表示阻抗值的整数部分。 RL_AC_STAT_0[2:0] 表示小数部分，其小数权重如下： [2]: 0.5 [1]: 0.25 [0]: 0.125 默认值：0000000

7.5.19 耳机交流负载状态 1

地址 0xE0011

只读	7	6	5	4	3	2	1	0
RL_AC_STAT_1								
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7:0	RL_AC_STAT_1	耳机交流负载测量的第 1 字节，单位为 Ω 。测量解释详情请参见 RL_AC_STAT_0。 默认值：0000000

7.5.20 耳机负载状态

地址 0xE001A

只读	7	6	5	4	3	2	1	0
	HLOAD_DC_ONCE	HLOAD_BUSY	—	—	HLOAD_AC_COMPLETE	HLOAD_AC_BUSY	HLOAD_DC_COMPLETE	HLOAD_DC_BUSY
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7	HLOAD_DC_ONCE	耳机负载直流测量至少执行一次的状态。 0 条件不存在 1 条件存在
6	HLOAD_BUSY	耳机负载测量模块状态机状态。 0 状态机空闲 1 状态机忙碌

Bits	Name	Description
5:4	—	Reserved
3	HPOLOAD_AC_DONE	HP load AC measurement is done status. 0 Condition is not present 1 Condition is present
2	HPOLOAD_AC_BUSY	HP AC load measurement is “in process” status. 0 Condition is not present 1 Condition is present
1	HPOLOAD_DC_DONE	HP load DC measurement is done status. 0 Condition is not present 1 Condition is present
0	HPOLOAD_DC_BUSY	HP DC load measurement is “in process” status. 0 Condition is not present 1 Condition is present

7.6 Interrupt Status and Mask Registers

7.6.1 Interrupt Status 1

Address 0xF0000

R/O	7	6	5	4	3	2	1	0
	DAC_OVFL_INT	HPDETECT_PLUG_INT	HPDETECT_UNPLUG_INT	XTAL_READY_INT	XTAL_ERROR_INT	PLL_READY_INT	PLL_ERROR_INT	PDN_DONE_INT
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	DAC_OVFL_INT	Status indicating DAC modulator overflow condition is detected. 0 Condition is not present 1 Condition is present
6	HPDETECT_PLUG_INT	Status indicating HP plug event is detected. 0 Condition is not present 1 Condition is present
5	HPDETECT_UNPLUG_INT	Status indicating HP unplug event is detected. 0 Condition is not present 1 Condition is present
4	XTAL_READY_INT	Status indicating XTAL is ready after PDN_XTAL is cleared. 0 Condition is not present 1 Condition is present
3	XTAL_ERROR_INT	Status indicating XTAL error condition is detected after PDN_XTAL is cleared. 0 Condition is not present 1 Condition is present
2	PLL_READY_INT	Status indicating PLL ready condition is detected after PLL_START is set. 0 Condition is not present 1 Condition is present
1	PLL_ERROR_INT	Status indicating PLL error condition is detected after PLL_START is set. 0 Condition is not present 1 Condition is present
0	PDN_DONE_INT	Status indicating PDN_HP process is completed after a request. 0 Condition is not present 1 Condition is present

7.6.2 Interrupt Status 2

Address 0xF0001

R/O	7	6	5	4	3	2	1	0
	ASP_OVFL_INT	ASP_ERROR_INT	ASP_LATE_INT	ASP_EARLY_INT	ASP_NOLRCK_INT	—	—	—
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	ASP_OVFL_INT	ASP RX request overload. 0 Condition is not present 1 Condition is present

位数	名称	描述
5:4	—	保留
3	HPOLOAD_AC_完成	耳机负载交流测量完成状态。 0 条件不存在 1 条件存在
2	HPOLOAD_AC_忙	耳机交流负载测量“进行中”状态。 0 条件不存在 1 条件存在
1	HPOLOAD_DC_DONE	耳机负载直流测量完成状态。 0 条件不存在 1 条件存在
0	HPOLOAD_DC_BUSY	耳机直流负载测量处于“进行中”状态。 0 条件不存在 1 条件存在

7.6 中断状态及屏蔽寄存器

7.6.1 中断状态 1 地址 0xF0000

只读	7	6	5	4	3	2	1	0
	DAC_OVFL_INT	HPDETECT_PLUG_INT	HPDETECT_UNPLUG_INT	XTAL_READY_INT	晶体振荡器_ERROR_INT	PLL_READY_INT	PLL_ERROR_INT	PDN_DONE_INT
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7	DAC_OVFL_INT	检测到 DAC 调制器溢出状态。 0 条件不存在 1 条件存在
6	HPDETECT_PLUG_INT	检测到耳机插入事件状态。 0 条件不存在 1 条件存在
5	HPDETECT_UNPLUG_INT	检测到耳机拔出事件状态。 0 条件不存在 1 条件存在
4	晶体振荡器_READY_INT	PDN_XTAL 清除后，晶体振荡器准备就绪状态。 0 条件不存在 1 条件存在
3	晶体振荡器_ERROR_INT	PDN_XTAL 清除后，检测到晶体振荡器错误状态。 0 条件不存在 1 条件存在
2	PLL_READY_INT	设置 PLL_START 后，检测到 PLL 准备就绪状态。 0 条件不存在 1 条件存在
1	PLL_ERROR_INT	设置 PLL_START 后，检测到 PLL 错误状态。 0 条件不存在 1 条件存在
0	PDN_DONE_INT	请求后，PDN_HP 处理完成状态。 0 条件不存在 1 条件存在

7.6.2 中断状态 2 地址 0xF0001

只读	7	6	5	4	3	2	1	0
	ASP_OVFL_INT	ASP_ERROR_INT	ASP_LATE_INT	ASP_EARLY_INT	ASP_NOLRCK_INT	—	—	—
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7	ASP_OVFL_INT	ASP 接收请求过载。 0 条件不存在 1 条件存在

Bits	Name	Description						
6	ASP_ERROR_INT	ASP RX LRCK error. Logical OR of LRCK early and LRCK late errors. 0 Condition is not present 1 Condition is present						
5	ASP_LATE_INT	ASP RX LRCK late. 0 Condition is not present 1 Condition is present						
4	ASP_EARLY_INT	ASP RX LRCK early. 0 Condition is not present 1 Condition is present						
3	ASP_NOLRCK_INT	ASP RX no LRCK. 0 Condition is not present 1 Condition is present						
2:0	—	Reserved						

7.6.3 Interrupt Status 3

Address 0xF0002

R/O	7	6	5	4	3	2	1	0
	XSP_OVFL_INT	XSP_ERROR_INT	XSP_LATE_INT	XSP_EARLY_INT	XSP_NOLRCK_INT	—	—	—
Default	0	0	0	0	0	0	0	0

Bits	Name	Description						
7	XSP_OVFL_INT	XSP RX request overload. 0 Condition is not present 1 Condition is present						
6	XSP_ERROR_INT	XSP RX LRCK error. Logical OR of LRCK early and LRCK late errors. 0 Condition is not present 1 Condition is present						
5	XSP_LATE_INT	XSP RX LRCK late. 0 Condition is not present 1 Condition is present						
4	XSP_EARLY_INT	XSP RX LRCK early. 0 Condition is not present 1 Condition is present						
3	XSP_NOLRCK_INT	XSP RX no LRCK. 0 Condition is not present 1 Condition is present						
2:0	—	Reserved						

7.6.4 Interrupt Status 4

Address 0xF0003

R/O	7	6	5	4	3	2	1	0
	HLOAD_NO_DC_INT	HLOAD_UNPLUG_INT	HLOAD_HPON_INT	HLOAD_OOR_INT	HLOAD_AC_DONE_INT	HLOAD_DC_DONE_INT	HLOAD_OFF_INT	HLOAD_ON_INT
Default	0	0	0	0	0	0	0	0

Bits	Name	Description						
7	HLOAD_NO_DC_INT	HP load error condition: AC load detection is performed without DC load detection done first. 0 Condition is not present 1 Condition is present						
6	HLOAD_UNPLUG_INT	HP load error condition: Unplug event happened during load detection process. 0 Condition is not present 1 Condition is present						
5	HLOAD_HPON_INT	HP load error condition: HLOAD_EN is set before PDN_HP is set and PDN_DONE_INT event is received. 0 Condition is not present 1 Condition is present						
4	HLOAD_OOR_INT	HP load error condition: HLOAD out of range result is measured. 0 Condition is not present 1 Condition is present						

位数	名称	描述
6	ASP_ERROR_INT	ASP 接收 LRCK 错误。LRCK 过早和 LRCK 过迟错误的逻辑或。 0 条件不存在 1 条件存在
5	ASP_LATE_INT	ASP 接收 LRCK 过迟。 0 条件不存在 1 条件存在
4	ASP_EARLY_INT	ASP 接收 LRCK 过早。 0 条件不存在 1 条件存在
3	ASP_NOLRCK_INT	ASP 接收无 LRCK。 0 条件不存在 1 条件存在
2:0	—	保留

7.6.3 中断状态 3

地址 0xF0002

只读	7	6	5	4	3	2	1	0
	XSP_OVFL_INT	XSP_ERROR_INT	XSP_LATE_INT	XSP_EARLY_INT	XSP_NOLRCK_INT	—	—	—
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7	XSP_OVFL_INT	XSP 接收请求过载。 0 条件不存在 1 条件存在
6	XSP_错误中断	XSP 接收 LRCK 错误。LRCK 过早和 LRCK 过迟错误的逻辑或。 0 条件不存在 1 条件存在
5	XSP_LATE_INT	XSP 接收 LRCK 过迟。 0 条件不存在 1 条件存在
4	XSP_EARLY_INT	XSP 接收 LRCK 过早。 0 条件不存在 1 条件存在
3	XSP_NOLRCK_INT	XSP 接收无 LRCK。 0 条件不存在 1 条件存在
2:0	—	保留

7.6.4 中断状态 4

地址 0xF0003

只读	7	6	5	4	3	2	1	0
	HLOAD_NO_DC_INT	HLOAD_UNPLUG_INT	HLOAD_HPON_INT	HLOAD_OOR_INT	HLOAD_AC_DONE_INT	HLOAD_DC_DONE_INT	HLOAD_OFF_INT	HLOAD_ON_中断
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7	HLOAD_无直流中断	耳机负载错误状态：在未先完成直流负载检测的情况下执行交流负载检测。 0 条件不存在 1 条件存在
6	HLOAD_UNPLUG_INT	耳机负载错误状态：负载检测过程中发生拔出事件。 0 条件不存在 1 条件存在
5	HLOAD_HPON_INT	耳机负载错误状态：在设置 PDN_HP 并接收到 PDN_DONE_INT 事件之前，已设置 HLOAD_EN。 0 条件不存在 1 条件存在
4	HLOAD_OOR_INT	耳机负载错误状态：测量到 HLOAD 超出范围的结果。 0 条件不存在 1 条件存在

Bits	Name	Description
3	HPOLOAD_AC_DONE_INT	Status indicating HP AC load measurement is completed. 0 Condition is not present 1 Condition is present
2	HPOLOAD_DC_DONE_INT	Status indicating HP DC load measurement is completed. 0 Condition is not present 1 Condition is present
1	HPOLOAD_OFF_INT	HP load state machine is properly shut down after HPOLOAD_EN is cleared. 0 Condition is not present 1 Condition is present
0	HPOLOAD_ON_INT	HP load state machine is properly turned on after HPOLOAD_EN is set. 0 Condition is not present 1 Condition is present

7.6.5 Interrupt Status 5

Address 0xF0004

R/O	7	6	5	4	3	2	1	0
	DSD_STUCK_INT	DSD_INVAL_A_INT	DSD_INVAL_B_INT	DSD_SILENCE_A_INT	DSD_SILENCE_B_INT	DSD_RATE_ERROR_INT	DOP_MRK_DET_INT	DOP_ON_INT
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	DSD_STUCK_INT	At least one DSD input channel is stuck at 0 or 1. 0 Condition is not present 1 Condition is present
6	DSD_INVAL_A_INT	Channel A input exceeds the max peak level of +3.1-dB SACD. 0 Condition is not present 1 Condition is present
5	DSD_INVAL_B_INT	Channel B input exceeds the max peak level of +3.1-dB SACD. 0 Condition is not present 1 Condition is present
4	DSD_SILENCE_A_INT	Channel A contains DSD silence pattern. 0 Condition is not present 1 Condition is present
3	DSD_SILENCE_B_INT	Channel B contains DSD silence pattern. 0 Condition is not present 1 Condition is present
2	DSD_RATE_ERROR_INT	DSD data rate related error is detected. The rate of the input DSD stream is not as described in DSD_SPEED setting. If missed DoP header(s) is detected, the interrupt will also be triggered. 0 Condition is not present 1 Condition is present
1	DOP_MRK_DET_INT	A valid sequence of DoP markers has been detected. 0 Condition is not present 1 Condition is present
0	DOP_ON_INT	The DoP decoder is powered up. 0 Condition is not present 1 Condition is present

7.6.6 Interrupt Mask 1

Address 0xF0010

R/W	7	6	5	4	3	2	1	0
	DAC_OVFL_INT_MASK	HPDETECT_PLUG_INT_MASK	HPDETECT_UNPLUG_INT_MASK	XTAL_READY_INT_MASK	XTAL_ERROR_INT_MASK	PLL_READY_INT_MASK	PLL_ERROR_INT_MASK	PDN_DONE_INT_MASK
Default	1	1	1	1	1	1	1	1

Bits	Name	Description
7	DAC_OVFL_INT_MASK	DAC_OVFL_INT mask. 0 Unmasked 1 (Default) Masked

位数	名称	描述
3	HLOAD_AC_DONE_INT	指示耳机交流负载测量完成的状态。 0 条件不存在 1 条件存在
2	HLOAD_DC_DONE_INT	指示耳机直流负载测量完成的状态。 0 条件不存在 1 条件存在
1	HLOAD_OFF_INT	在清除 HLOAD_EN 后，耳机负载状态机已正确关闭。 0 条件不存在 1 条件存在
0	HLOAD_ON_INT	在设置 HLOAD_EN 后，耳机负载状态机已正确开启。 0 条件不存在 1 条件存在

7.6.5 中断状态 5

地址 0xF0004

只读	7	6	5	4	3	2	1	0
	DSD_STUCK_中断	DSD_INVAL_A_中断	DSD_INVAL_B_中断	DSD_静音_A_中断	DSD_静音_B_中断	DSD_速率错误_中断	DOP_MRK_检测_中断	DOP_ON_INT
默认	0	0	0	0	0	0	0	0

位数	名称	描述
7	DSD_STUCK_中断	至少有一个 DSD 输入通道卡在 0 或 1。 0 条件不存在 1 条件存在
6	DSD_INVAL_A_中断	通道 A 输入超过 +3.1 dB SACD 的最大峰值电平。 0 条件不存在 1 条件存在
5	DSD_INVAL_B_中断	通道 B 输入超过 +3.1 dB SACD 的最大峰值电平。 0 条件不存在 1 条件存在
4	DSD_静音_A_中断	通道 A 包含 DSD 静音模式。 0 条件不存在 1 条件存在
3	DSD_静音_B_中断	通道 B 包含 DSD 静音模式。 0 条件不存在 1 条件存在
2	DSD_速率错误_中断	检测到与 DSD 数据速率相关的错误。输入的 DSD 流速率与 DSD_SPEED 设置描述不符。检测到缺失的DoP头时，也会触发中断。 0 条件不存在 1 条件存在
1	DOP_MRK_检测_中断	已检测到有效的DoP标记序列。 0 条件不存在 1 条件存在
0	DOP_ON_INT	DoP解码器已上电。 0 条件不存在 1 条件存在

7.6.6 中断屏蔽1

地址 0xF0010

读/写	7	6	5	4	3	2	1	0
	DAC_OVFL_中断屏蔽	HPDETECT_PLUG_INT_MASK	HPDETECT_UNPLUG_INT_MASK	XTAL_READY_INT_MASK	晶体振荡器ERROR_INT_MASK	PLL_READY_INT_MASK	PLL_ERROR_INT_MASK	PDN_DONE_INT_MASK
默认	1	1	1	1	1	1	1	1

位数	名称	描述
7	DAC_OVFL_中断屏蔽	DAC_OVFL_INT 屏蔽。 0 未屏蔽 1 (默认) 已屏蔽

Bits	Name	Description
6	HPDETECT_PLUG_INT_MASK	HP_DETECT_PLUG_INT mask. 0 Unmasked 1 (Default) Masked
5	HPDETECT_UNPLUG_INT_MASK	HP_DETECT_UNPLUG_INT mask. 0 Unmasked 1 (Default) Masked
4	XTAL_READY_INT_MASK	XTAL_READY_INT mask. 0 Unmasked 1 (Default) Masked
3	XTAL_ERROR_INT_MASK	XTAL_ERROR_INT mask. 0 Unmasked 1 (Default) Masked
2	PLL_READY_INT_MASK	PLL_READY_INT mask. 0 Unmasked 1 (Default) Masked
1	PLL_ERROR_INT_MASK	PLL_ERROR_INT mask. 0 Unmasked 1 (Default) Masked
0	PDN_DONE_INT_MASK	PDN_DONE_INT mask. 0 Unmasked 1 (Default) Masked

7.6.7 Interrupt Mask 2

Address 0xF0011

R/W	7	6	5	4	3	2	1	0
	ASP_OVFL_INT_MASK	ASP_ERROR_INT_MASK	ASP_LATE_INT_MASK	ASP_EARLY_INT_MASK	ASP_NOLRCK_INT_MASK	—	—	—
Default	1	1	1	1	1	0	0	0

Bits	Name	Description
7	ASP_OVFL_INT_MASK	ASP_OVFL_INT mask. 0 Unmasked 1 (Default) Masked
6	ASP_ERROR_INT_MASK	ASP_ERROR_INT mask. 0 Unmasked 1 (Default) Masked
5	ASP_LATE_INT_MASK	ASP_LATE_INT mask. 0 Unmasked 1 (Default) Masked
4	ASP_EARLY_INT_MASK	ASP_EARLY_INT mask. 0 Unmasked 1 (Default) Masked
3	ASP_NOLRCK_INT_MASK	ASP_NOLRCK_INT mask. 0 Unmasked 1 (Default) Masked
2:0	—	Reserved

7.6.8 Interrupt Mask 3

Address 0xF0012

R/W	7	6	5	4	3	2	1	0
	XSP_OVFL_INT_MASK	XSP_ERROR_INT_MASK	XSP_LATE_INT_MASK	XSP_EARLY_INT_MASK	XSP_NOLRCK_INT_MASK	—	—	—
Default	1	1	1	1	1	0	0	0

Bits	Name	Description
7	XSP_OVFL_INT_MASK	XSP_OVFL_INT mask. 0 Unmasked 1 (Default) Masked

位数	名称	描述
6	HPDETECT_PLUG_INT_MASK	HP_DETECT_PLUG_INT屏蔽。 0 未屏蔽 1 (默认) 已屏蔽
5	HPDETECT_UNPLUG_INT_MASK	HP_DETECT_UNPLUG_INT屏蔽。 0 未屏蔽 1 (默认) 已屏蔽
4	晶体振荡器_READY_INT_MASK	XTAL_READY_INT屏蔽。 0 未屏蔽 1 (默认) 已屏蔽
3	晶体振荡器_ERROR_INT_MASK	XTAL_ERROR_INT屏蔽。 0 未屏蔽 1 (默认) 已屏蔽
2	PLL_READY_INT_MASK	PLL_READY_INT屏蔽。 0 未屏蔽 1 (默认) 已屏蔽
1	PLL_ERROR_INT_MASK	PLL_ERROR_INT屏蔽。 0 未屏蔽 1 (默认) 已屏蔽
0	PDN_DONE_INT_MASK	PDN_DONE_INT 掩码。 0 未屏蔽 1 (默认) 已屏蔽

7.6.7 中断掩码 2

地址 0xF0011

读/写	7	6	5	4	3	2	1	0
	ASP_OVFL_INT_MASK	ASP_ERROR_INT_MASK	ASP_LATE_INT_MASK	ASP_EARLY_INT_MASK	ASP_NOLRCK_INT_掩码	—	—	—
默认	1	1	1	1	1	0	0	0

位数	名称	描述
7	ASP_OVFL_INT_掩码	ASP_OVFL_INT 掩码。 0 未屏蔽 1 (默认) 已屏蔽
6	ASP_ERROR_INT_掩码	ASP_ERROR_INT 掩码。 0 未屏蔽 1 (默认) 已屏蔽
5	ASP_LATE_INT_掩码	ASP_LATE_INT 掩码。 0 未屏蔽 1 (默认) 已屏蔽
4	ASP_EARLY_INT_掩码	ASP_EARLY_INT 掩码。 0 未屏蔽 1 (默认) 已屏蔽
3	ASP_NOLRCK_INT_掩码	ASP_NOLRCK_INT 掩码。 0 未屏蔽 1 (默认) 已屏蔽
2:0	—	保留

7.6.8 中断掩码 3

地址 0xF0012

读/写	7	6	5	4	3	2	1	0
	XSP_OVFL_INT_掩码	XSP_ERROR_INT_掩码	XSP_LATE_INT_MASK	XSP_EARLY_INT_MASK	XSP_NOLRCK_INT_MASK	—	—	—
默认	1	1	1	1	1	0	0	0

位数	名称	描述
7	XSP_OVFL_INT_MASK	XSP_OVFL_INT mask。 0 未屏蔽 1 (默认) 已屏蔽

Bits	Name	Description							
6	XSP_ERROR_INT_MASK	XSP_ERROR_INT mask. 0 Unmasked 1 (Default) Masked							
5	XSP_LATE_INT_MASK	XSP_LATE_INT mask. 0 Unmasked 1 (Default) Masked							
4	XSP_EARLY_INT_MASK	XSP_EARLY_INT mask. 0 Unmasked 1 (Default) Masked							
3	XSP_NOLRCK_INT_MASK	XSP_NOLRCK_INT mask. 0 Unmasked 1 (Default) Masked							
2:0	—	Reserved							

7.6.9 Interrupt Mask 4

Address 0xF0013

R/W	7	6	5	4	3	2	1	0
	HPLOAD_NO_DC_INT_MASK	HPLOAD_UNPLUG_INT_MASK	HPLOAD_HPON_INT_MASK	HPLOAD_OOR_INT_MASK	HPLOAD_AC_DONE_INT_MASK	HPLOAD_DC_DONE_INT_MASK	HPLOAD_OFF_INT_MASK	HPLOAD_ON_INT_MASK
Default	1	1	1	1	1	1	1	1

Bits	Name	Description							
7	HPLOAD_NO_DC_INT_MASK	HPLOAD_NO_DC_INT mask. 0 Unmasked 1 (Default) Masked							
6	HPLOAD_UNPLUG_INT_MASK	HPLOAD_UNPLUG_INT mask. 0 Unmasked 1 (Default) Masked							
5	HPLOAD_HPON_INT_MASK	HPLOAD_HPON_INT mask. 0 Unmasked 1 (Default) Masked							
4	HPLOAD_OOR_INT_MASK	HPLOAD_OOR_INT mask. 0 Unmasked 1 (Default) Masked							
3	HPLOAD_AC_DONE_INT_MASK	HPLOAD_AC_DONE_INT mask. 0 Unmasked 1 (Default) Masked							
2	HPLOAD_DC_DONE_INT_MASK	HPLOAD_DC_DONE_INT mask. 0 Unmasked 1 (Default) Masked							
1	HPLOAD_OFF_INT_MASK	HPLOAD_OFF_INT mask. 0 Unmasked 1 (Default) Masked							
0	HPLOAD_ON_INT_MASK	HPLOAD_ON_INT mask. 0 Unmasked 1 (Default) Masked							

7.6.10 Interrupt Mask 5

Address 0xF0014

R/W	7	6	5	4	3	2	1	0
	DSD_STUCK_INT_MASK	DSD_INVAL_A_INT_MASK	DSD_INVAL_B_INT_MASK	DSD_SILENCE_A_INT_MASK	DSD_SILENCE_B_INT_MASK	DSD_RATE_ERROR_INT_MASK	DOP_MRK_DET_INT_MASK	DOP_ON_INT_MASK
Default	1	1	1	1	1	1	1	1

Bits	Name	Description							
7	DSD_STUCK_INT_MASK	DSD_STUCK_INT mask. 0 Unmasked 1 (Default) Masked							

位数	名称	描述
6	XSP_ERROR_INT_MASK	XSP_ERROR_INT mask。 0 未屏蔽 1 (默认) 已屏蔽
5	XSP_LATE_INT_MASK	XSP_LATE_INT mask。 0 未屏蔽 1 (默认) 已屏蔽
4	XSP_EARLY_INT_MASK	XSP_EARLY_INT mask。 0 未屏蔽 1 (默认) 已屏蔽
3	XSP_NOLRCK_INT_MASK	XSP_NOLRCK_INT mask。 0 未屏蔽 1 (默认) 已屏蔽
2:0	—	保留

7.6.9 中断屏蔽 4

地址 0xF0013

读/写	7	6	5	4	3	2	1	0
	HPLOAD_NO_DC_INT_MASK	HPLOAD_UNPLUG_INT_MASK	HPLOAD_HPON_INT_MASK	HPLOAD_OOR_INT_MASK	HPLOAD_AC_DONE_INT_MASK	HPLOAD_DC_DONE_INT_MASK	HPLOAD_OFF_INT_MASK	HPLOAD_ON_INT_MASK
默认	1	1	1	1	1	1	1	1

位数	名称	描述
7	HPLOAD_NO_DC_INT_MASK	HPLOAD_NO_DC_INT 掩码。 0 未屏蔽 1 (默认) 已屏蔽
6	HPLOAD_UNPLUG_INT_MASK	HPLOAD_UNPLUG_INT 掩码 0 未屏蔽 1 (默认) 已屏蔽
5	HPLOAD_HPON_INT_MASK	HPLOAD_HPON_INT 掩码 0 未屏蔽 1 (默认) 已屏蔽
4	HPLOAD_OOR_INT_MASK	HPLOAD_OOR_INT 掩码 0 未屏蔽 1 (默认) 已屏蔽
3	HPLOAD_AC_DONE_INT_MASK	HPLOAD_AC_DONE_INT 掩码 0 未屏蔽 1 (默认) 已屏蔽
2	HPLOAD_DC_DONE_INT_MASK	HPLOAD_DC_DONE_INT 掩码 0 未屏蔽 1 (默认) 已屏蔽
1	HPLOAD_OFF_INT_MASK	HPLOAD_OFF_INT 掩码 0 未屏蔽 1 (默认) 已屏蔽
0	HPLOAD_ON_INT_MASK	HPLOAD_ON_INT 掩码 0 未屏蔽 1 (默认) 已屏蔽

7.6.10 中断掩码 5

地址 0xF0014

读/写	7	6	5	4	3	2	1	0
	DSD_STUCK_INT_MASK	DSD_INVAL_A_INT_MASK	DSD_INVAL_B_INT_MASK	DSD_SILENCE_A_INT_MASK	DSD_SILENCE_B_INT_MASK	DSD_RATE_ERROR_INT_MASK	DOP_MRK_DET_INT_MASK	DOP_ON_INT_MASK
默认	1	1	1	1	1	1	1	1

位数	名称	描述
7	DSD_STUCK_INT_MASK	DSD_STUCK_INT 掩码 0 未屏蔽 1 (默认) 已屏蔽

Bits	Name	Description							
6	DSD_INVAL_A_INT_MASK	DSD_INVAL_A_INT mask. 0 Unmasked 1 (Default) Masked							
5	DSD_INVAL_B_INT_MASK	DSD_INVAL_B_INT mask. 0 Unmasked 1 (Default) Masked							
4	DSD_SILENCE_A_INT_MASK	DSD_SILENCE_A_INT mask. 0 Unmasked 1 (Default) Masked							
3	DSD_SILENCE_B_INT_MASK	DSD_SILENCE_B_INT mask. 0 Unmasked 1 (Default) Masked							
2	DSD_RATE_ERROR_INT_MASK	DSD_RATE_ERROR_INT mask. 0 Unmasked 1 (Default) Masked							
1	DOP_MRK_DET_INT_MASK	DOP_MRK_DET_INT mask. 0 Unmasked 1 (Default) Masked							
0	DOP_ON_INT_MASK	DOP_ON_INT mask. 0 Unmasked 1 (Default) Masked							

7.6.11 ASP Master Mode Slew Rate Control

Address 0x10 0000

R/W	7	6	5	4	—	3	2	1	0
Default	0	0	1	0		SCLK1_SLEW_RATE		—	

Bits	Name	Description							
7:4	—	Reserved							
3:2	SCLK1_SLEW_RATE	SCLK1 slew rate control. 00 Reserved 01 Recommended drive strength for clock rate higher than 12.288 MHz 10 (Default) Recommended drive strength for clock rate 12.288 MHz or lower. 11 Reserved							
1:0	—	Reserved							

7.6.12 XSP Master Mode Slew Rate Control

Address 0x10 0001

R/W	7	6	5	4	—	3	2	1	0
Default	0	0	1	0		DSDCLK_SCLK2_SLEW_RATE		—	

Bits	Name	Description							
7:4	—	Reserved							
3:2	DSDCLK_SCLK2_SLEW_RATE	DSDCLK/SCLK2 slew rate control. 00 Reserved 01 Recommended drive strength for clock rate higher than 12.288 MHz 10 (Default) Recommended drive strength for clock rate 12.288 MHz or lower. 11 Reserved							
1:0	—	Reserved							

位数	名称	描述
6	DSD_INVAL_A_INT_MASK	DSD_INVAL_A_INT 掩码 0 未屏蔽 1 (默认) 已屏蔽
5	DSD_INVAL_B_INT_MASK	DSD_INVAL_B_INT 掩码 0 未屏蔽 1 (默认) 已屏蔽
4	DSD_SILENCE_A_INT_MASK	DSD_SILENCE_A_INT 掩码 0 未屏蔽 1 (默认) 已屏蔽
3	DSD_SILENCE_B_INT_MASK	DSD_SILENCE_B_INT 掩码 0 未屏蔽 1 (默认) 已屏蔽
2	DSD_RATE_ERROR_INT_MASK	DSD_RATE_ERROR_INT 掩码 0 未屏蔽 1 (默认) 已屏蔽
1	DOP_MRK_DET_INT_MASK	DOP_MRK_DET_INT 掩码。 0 未屏蔽 1 (默认) 已屏蔽
0	DOP_ON_INT_MASK	DOP_ON_INT 掩码。 0 未屏蔽 1 (默认) 已屏蔽

7.6.11 ASP 主模式转换速率控制

地址 0x10 0000

读/写	7	6	5	4	3	2	1	0
	—	—	—	—	SCLK1_SLEW_RATE	—	—	—
默认	0	0	1	0	1	0	1	0

位数	名称	描述
7:4	—	保留
3:2	SCLK1_SLEW_RATE	SCLK1 转换速率控制。 00 保留 01 推荐用于时钟频率高于 12.288 MHz 的驱动强度 10 (默认) 推荐用于时钟频率为 12.288 MHz 或更低的驱动强度。 11 保留
1:0	—	保留

7.6.12 XSP 主模式转换速率控制

地址 0x10 0001

读/写	7	6	5	4	3	2	1	0
	—	—	—	—	DSDCLK_SCLK2_SLEW_RATE	—	—	—
默认	0	0	1	0	1	0	1	0

位数	名称	描述
7:4	—	保留
3:2	DSDCLK_SCLK2_SLEW_RATE	DSDCLK/SCLK2 转换速率控制。 00 保留 01 推荐用于时钟频率高于 12.288 MHz 的驱动强度 10 (默认) 推荐用于时钟频率为 12.288 MHz 或更低的驱动强度。 11 保留
1:0	—	保留

8 PCB Layout Considerations

The following sections provide general guidelines for PCB layout to ensure the best performance of the CS43131.

8.1 Power Supply

As with any high-resolution converter, the CS43131 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. [Fig. 2-1](#) shows the recommended power arrangements with VA and VCP connected to independent clean supplies. VL and VD, which power the digital circuitry, may be run from the shared system logic supply.

8.2 Grounding

Note the following:

- Extensive use of power and ground planes, ground-plane fill in unused areas, and surface-mount decoupling capacitors are recommended.
- Decoupling capacitors must be as close as possible to the CS43131 pins.
- To minimize inductance effects, the low-value ceramic capacitor must be closest to the pin and mounted on the same side of the board as the CS43131.
- To avoid unwanted coupling into the modulators, all signals, especially clocks, must be isolated from the FILT+ and FILT- pins.
- The FILT+ capacitors must be positioned to minimize the electrical path from the pin to VA.
- The FILT- capacitors must be positioned to minimize the electrical path from the pin to -VA.
- The VCP_FILT+ and VCP_FILT- capacitors must be positioned to minimize the electrical path from each respective pin to GND_{CP}.

8.3 HPREFA and HPREFB Routing

For best interchannel isolation performance, HPREFA and HPREFB must be routed independently to the headphone connector reference pin. The HPREFA and HPREFB are electrically connected to system's ground plane through via at the headphone connector ground pin. [Fig. 2-1](#) illustrates the recommended arrangements.

For interfacing the HPREFA and HPREFB pins with an IC that performs alternate pinout headset detect functions, both signals must be routed independently to the CS43131's ground pin connecting the detected headset ground pole. Follow the recommended grounding scheme of the CS43131.

8.4 QFN Thermal Pad

The CS43131 comes in a compact QFN package, the underside of which reveals a large metal pad that serves as a thermal relief to provide maximum heat dissipation. This pad must mate with a matching copper pad on the PCB and must be electrically connected to ground. A series of vias must be used to connect this copper pad to one or more larger ground planes on other PCB layers. For best performance in split-ground systems, connect this thermal pad to GNDA.

8 PCB 布局注意事项

以下章节提供 PCB 布局的一般指导，以确保 CS43131 的最佳性能。

8.1 电源

与任何高分辨率转换器一样，CS43131 需要对电源和接地布置进行细致关注，才能实现其潜在性能。图 2-1 显示了推荐的电源布置，其中 VA 和 VCP 连接至独立的洁净电源。为数字电路供电的 VL 和 VD 可由共享的系统逻辑电源供电。

8.2 接地

请注意以下事项：

- 建议广泛采用电源和平面接地，未使用区域填充接地平面，并使用贴片去耦电容。
- 去耦电容必须尽可能靠近CS43131引脚。
- 为最小化电感效应，低值陶瓷电容必须最靠近引脚，并安装在与CS43131同侧的电路板上。
- 为避免信号对调制器产生非预期耦合，所有信号，尤其是时钟信号，必须与FILT+和FILT-引脚隔离。
- FILT+电容应布置以最小化从引脚到VA的电气路径。
- FILT-电容应布置以最小化从引脚到–VA的电气路径。
- VCP_FILT+和VCP_FILT-电容应布置以最小化各自引脚到GND_{CP}的电气路径。

8.3 HPREFA 和 HPREFB 布线

为实现最佳通道间隔离性能，HPREFA和HPREFB必须独立布线至耳机连接器参考引脚。HPREFA和HPREFB通过耳机连接器接地引脚的过孔电气连接至系统接地平面。图 2-1展示了推荐的布线方案。

为了将 HPREFA 和 HPREFB 引脚与执行交替引脚检测功能的 IC 连接，必须将这两个信号独立布线至 CS43131 的接地引脚，该引脚连接被检测耳机的接地极。请遵循 CS43131 推荐的接地方案。

8.4 QFN 散热焊盘

CS43131 采用紧凑型 QFN 封装，其底部设有大型金属散热垫，用于热缓解并提供最大散热效果。该散热垫必须与 PCB 上对应的铜箔垫匹配，并且必须电气连接至接地。必须使用一系列过孔将该铜箔垫连接至 PCB 其他层的一个或多个较大接地平面。在分割接地系统中，为获得最佳性能，应将该散热垫连接至 GND_A。

9 Performance Plots

9.1 Digital Filter Response

9.1.1 Combined Filter Response—Single Speed ($F_s = 32$ kHz, Slow Roll-Off)

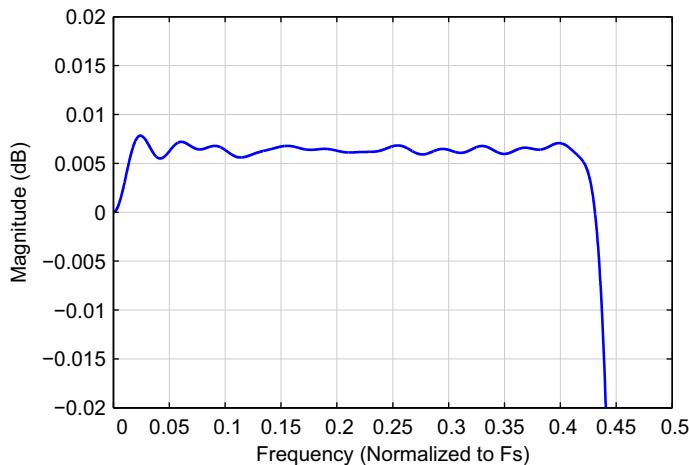


Figure 9-1. Passband Ripple

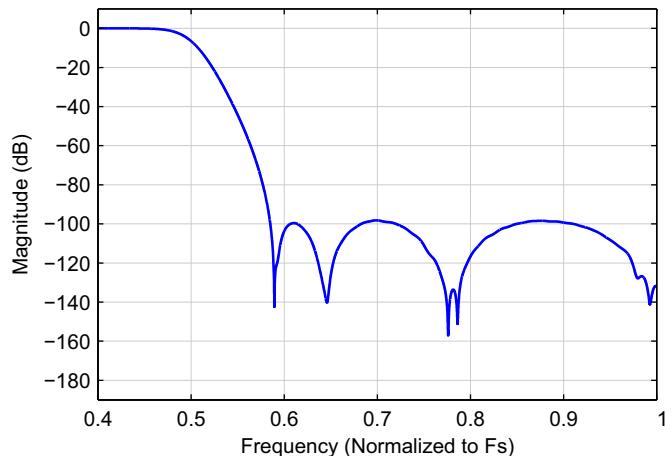


Figure 9-2. Stopband Attenuation

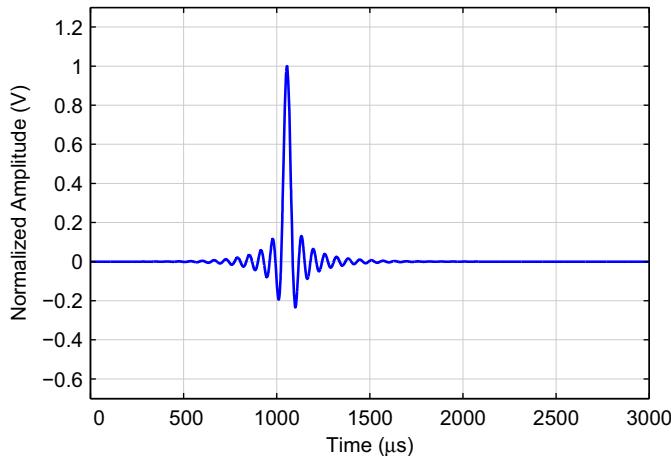


Figure 9-3. Impulse Response—Linear Phase

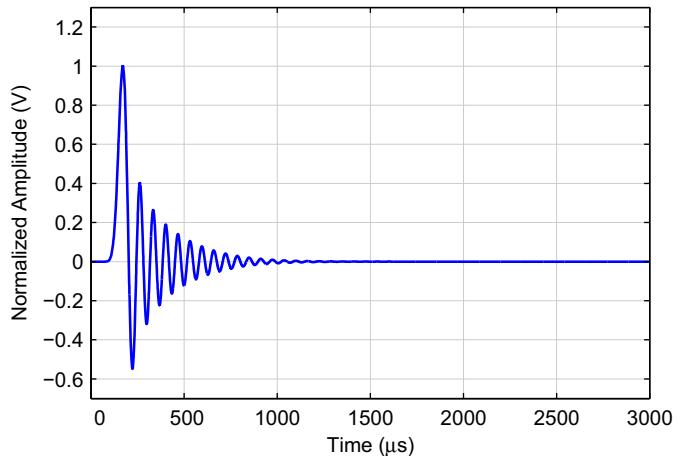


Figure 9-4. Impulse Response—Minimum Phase

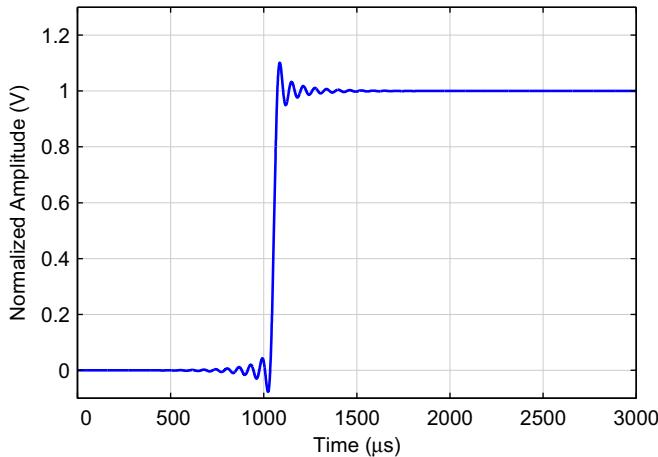


Figure 9-5. Step Response—Linear Phase

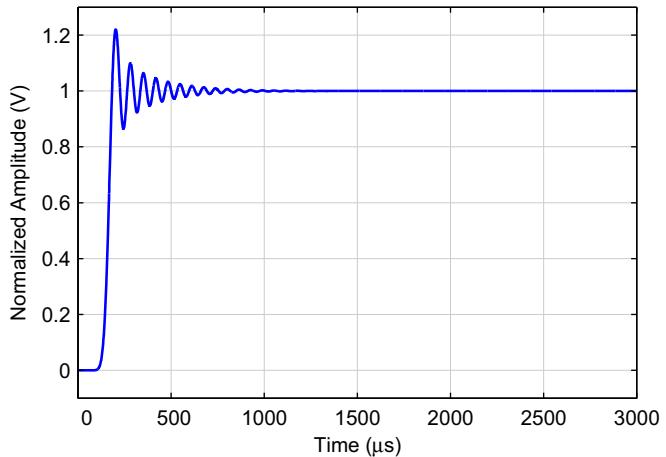


Figure 9-6. Step Response—Minimum Phase

9 性能曲线

9.1 数字滤波器响应

9.1.1 组合滤波器响应——单速率 ($F_s = 32 \text{ kHz}$, 缓慢滚降)

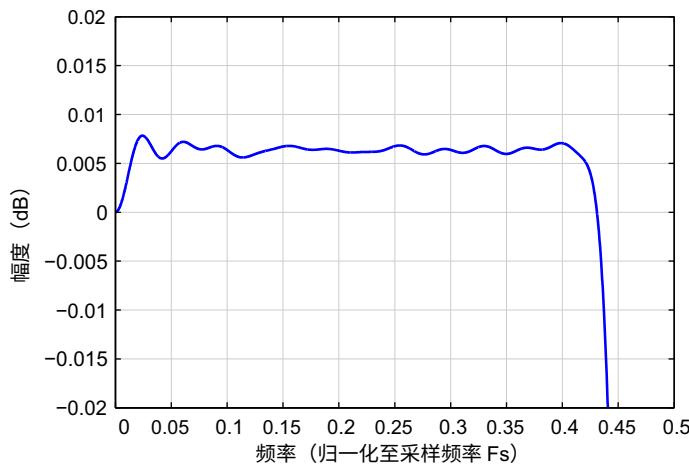


图 9-1. 通带波纹

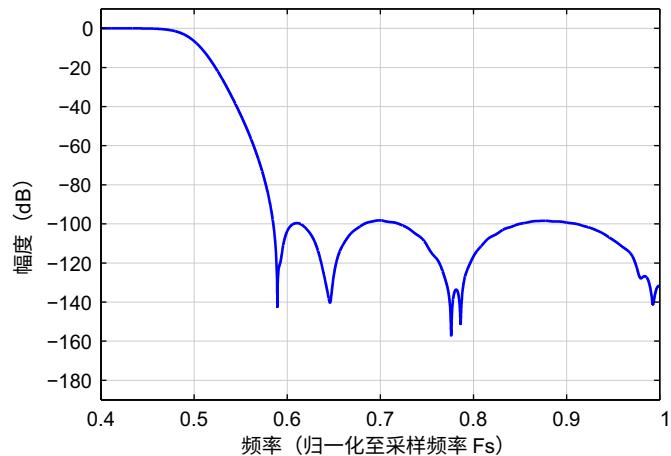


图 9-2. 阻带衰减

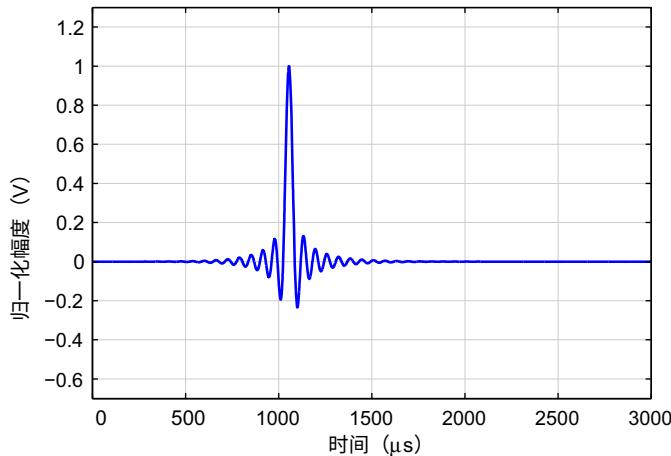


图 9-3. 脉冲响应—线性相位

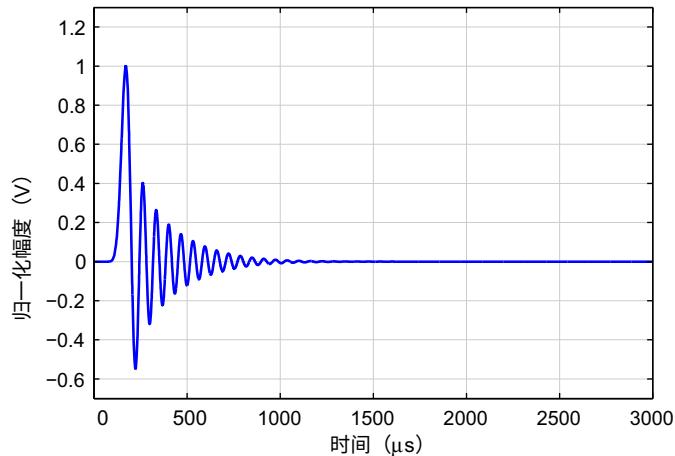


图 9-4. 脉冲响应—最小相位

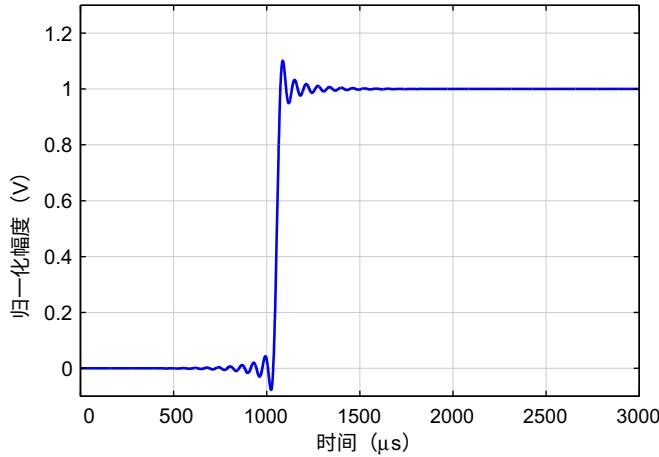


图 9-5. 阶跃响应—线性相位

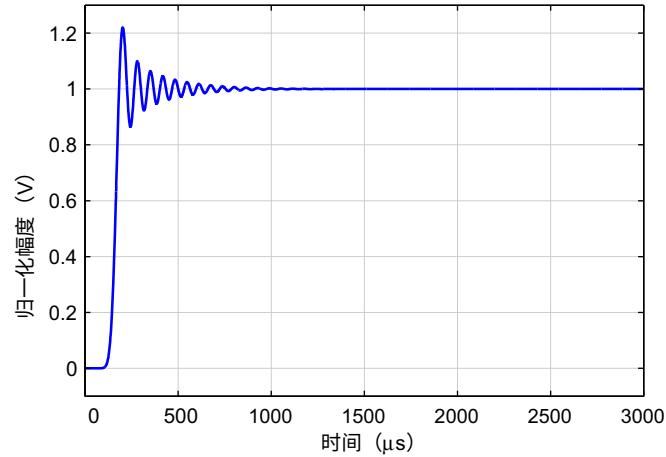


图 9-6. 阶跃响应—最小相位

9.1.2 Combined Filter Response—Single Speed ($F_s = 32$ kHz, Fast Roll-Off)

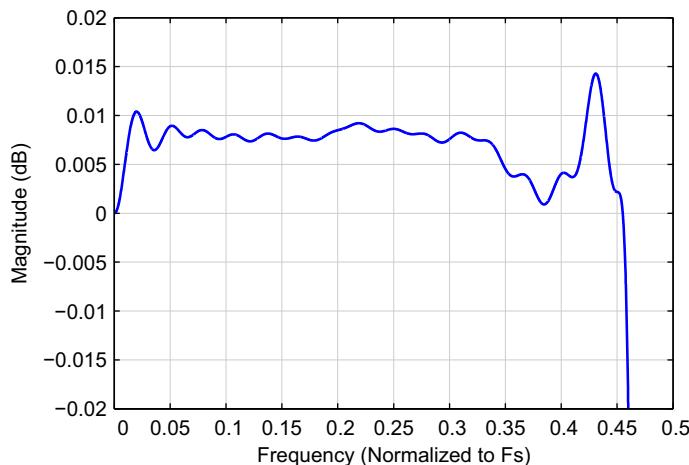


Figure 9-7. Passband Ripple

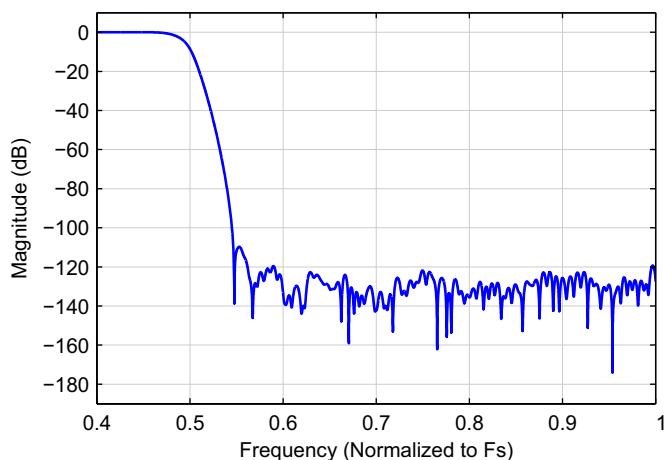


Figure 9-8. Stopband Attenuation

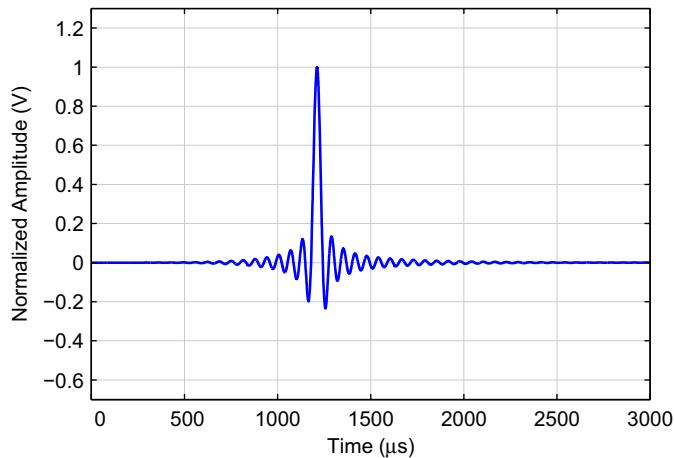


Figure 9-9. Impulse Response—Linear Phase

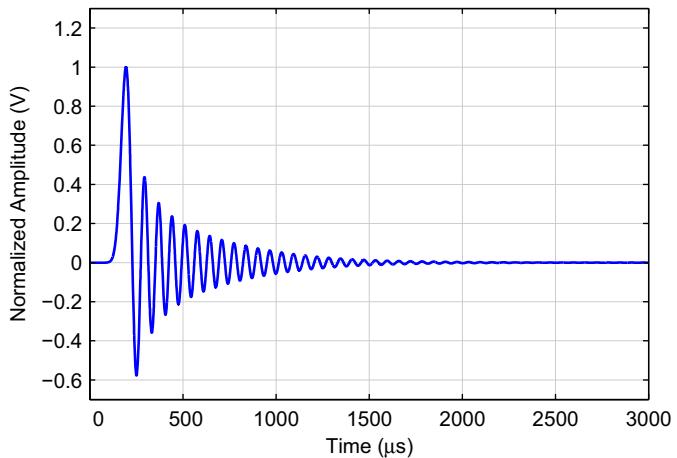


Figure 9-10. Impulse Response—Minimum Phase

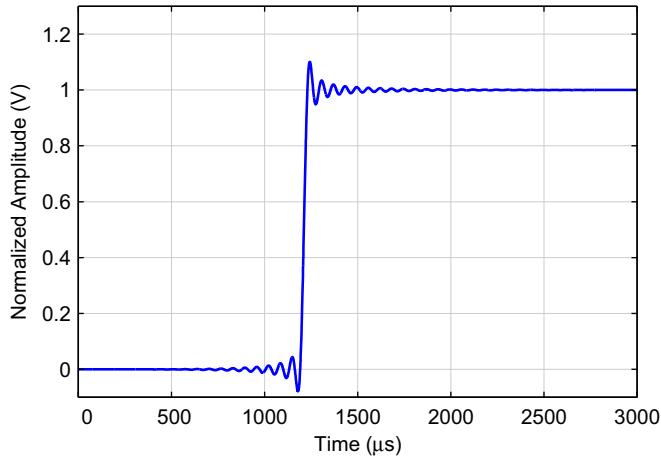


Figure 9-11. Step Response—Linear Phase

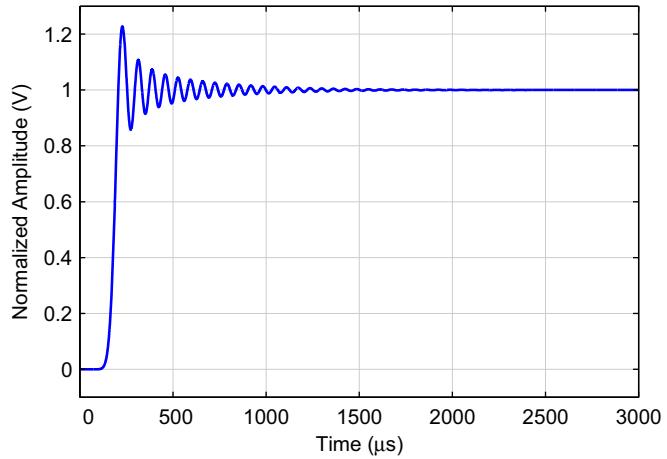


Figure 9-12. Step Response—Minimum Phase

9.1.2 组合滤波器响应—单速率 ($F_s = 32 \text{ kHz}$, 快速滚降)

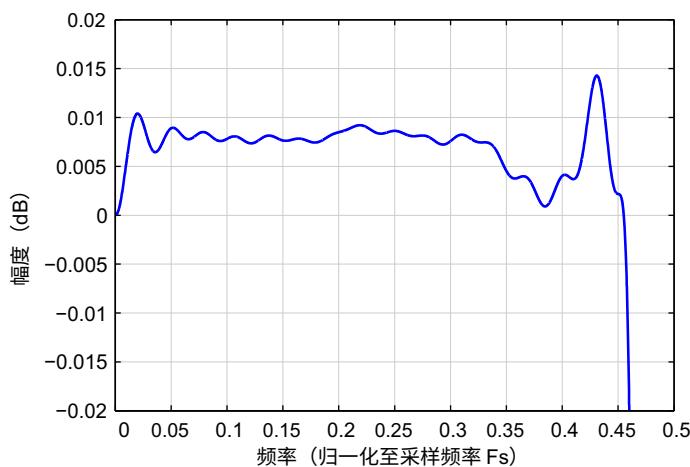


图 9-7。通带波纹

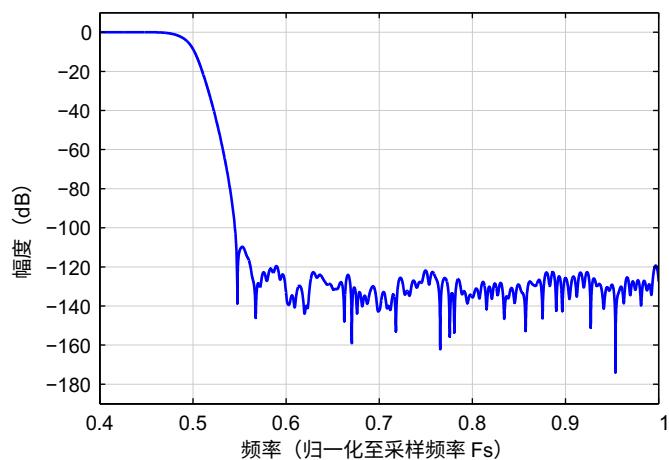


图 9-8。阻带衰减

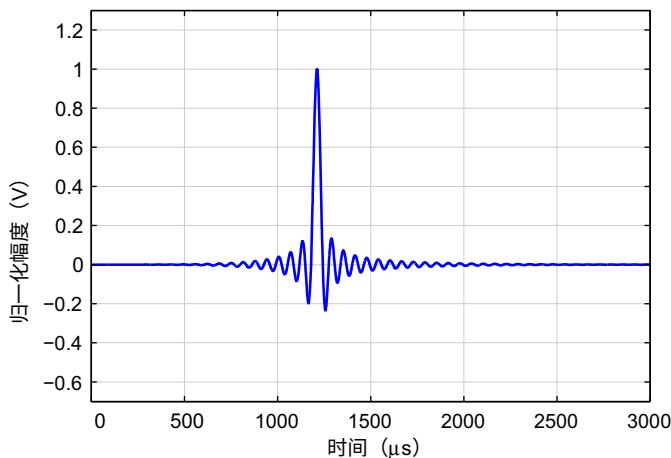


图 9-9。脉冲响应—线性相位

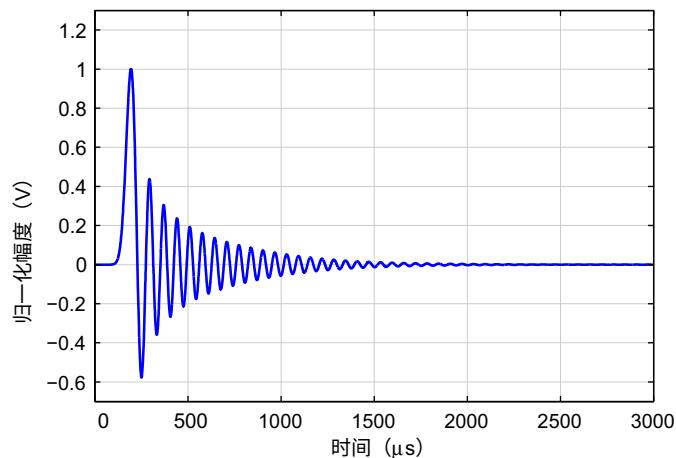


图 9-10。脉冲响应—最小相位

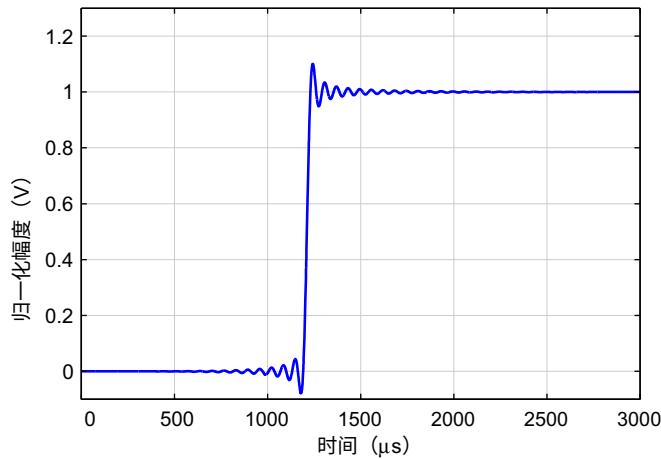


图 9-11。阶跃响应—线性相位

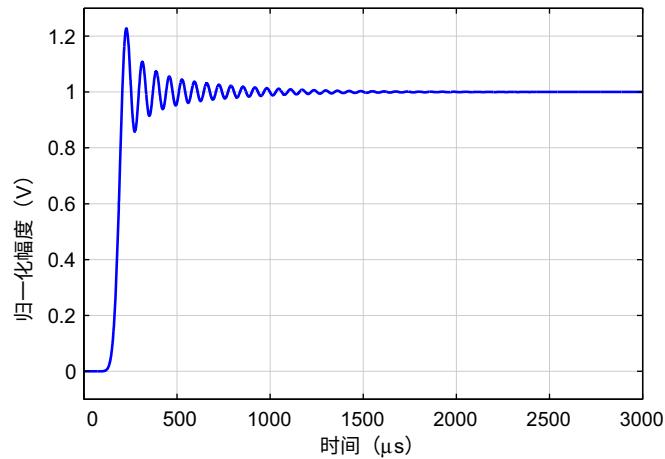


图 9-12。阶跃响应—最小相位

9.1.3 Combined Filter Response—Single Speed ($F_s = 44.1$ and 48 kHz, Slow Roll-Off)

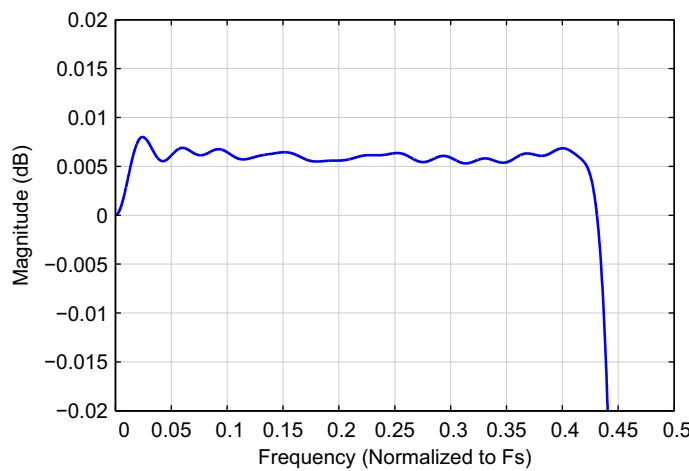


Figure 9-13. Passband Ripple

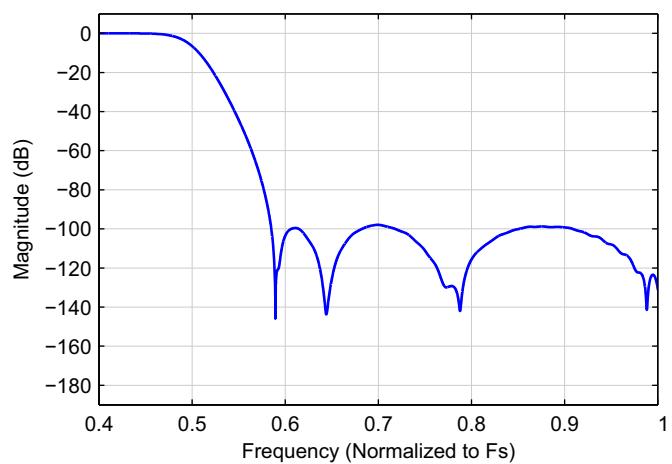


Figure 9-14. Stopband Attenuation

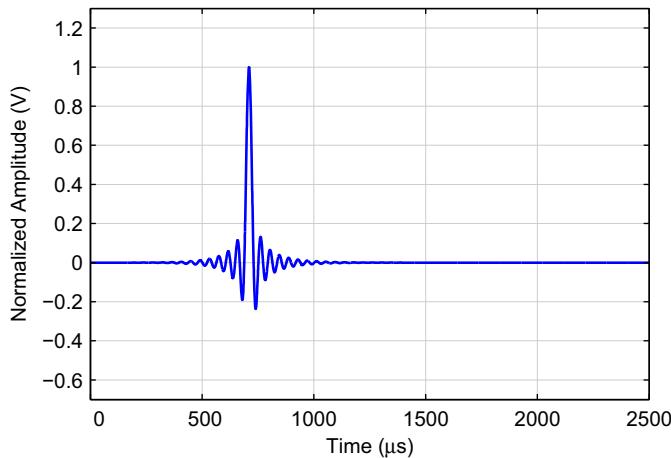


Figure 9-15. Impulse Response—Linear Phase

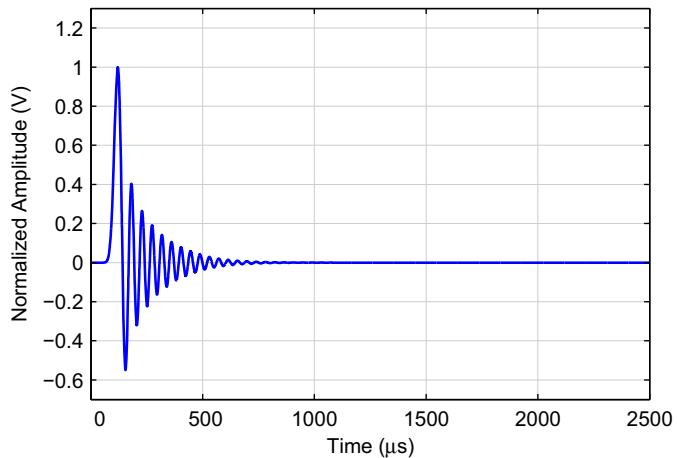


Figure 9-16. Impulse Response—Minimum Phase

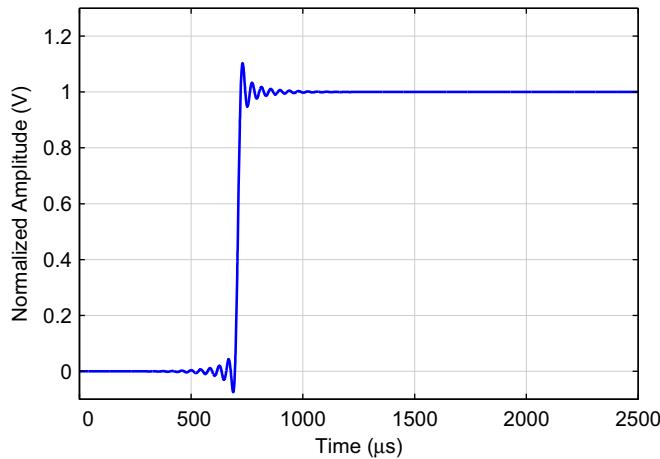


Figure 9-17. Step Response—Linear Phase

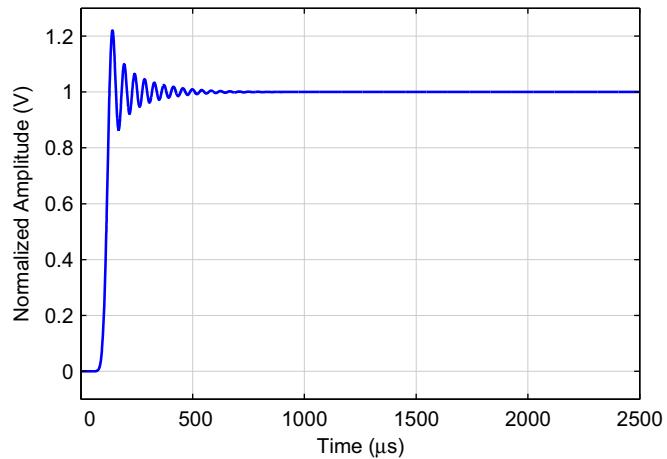


Figure 9-18. Step Response—Minimum Phase

9.1.3 组合滤波器响应——单速（采样频率 = 44.1 kHz 和 48 kHz，缓慢滚降）

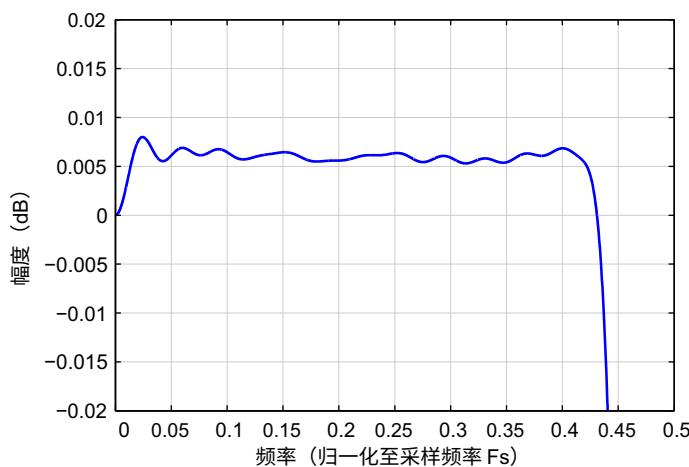


图 9-13。通带波纹

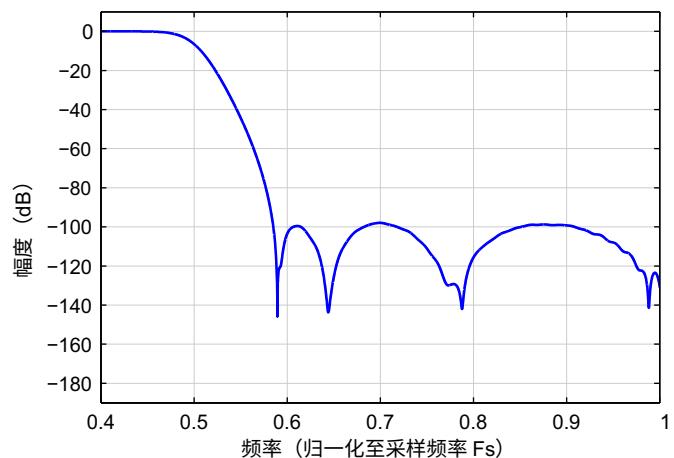


图 9-14。阻带衰减

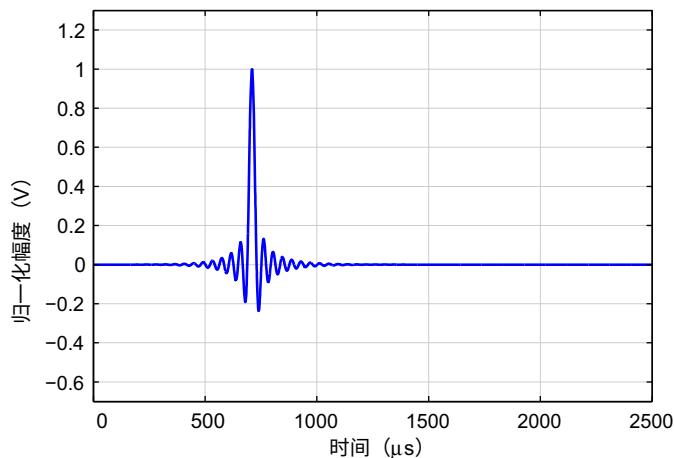


图 9-15。脉冲响应—线性相位

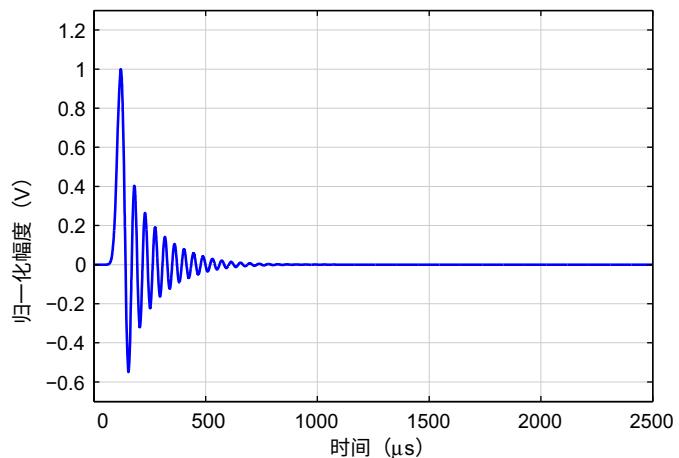


图 9-16。脉冲响应—最小相位

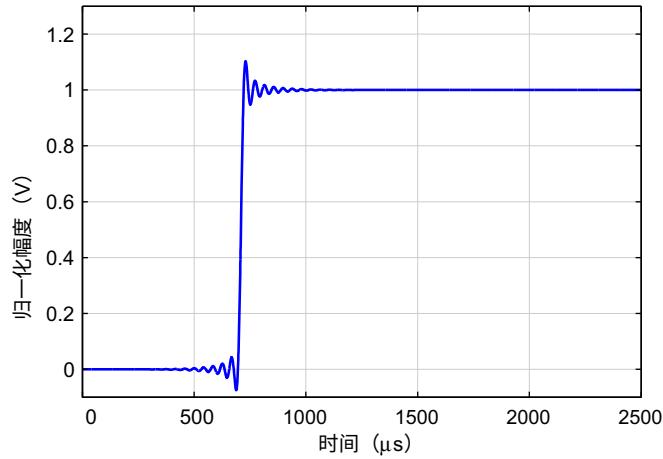


图 9-17。阶跃响应—线性相位

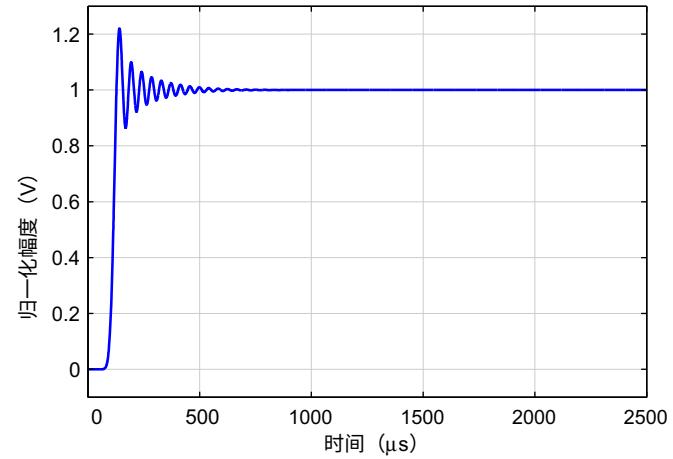


图 9-18。阶跃响应—最小相位

9.1.4 Combined Filter Response—Single Speed ($F_s = 44.1$ and 48 kHz, Fast Roll-Off)

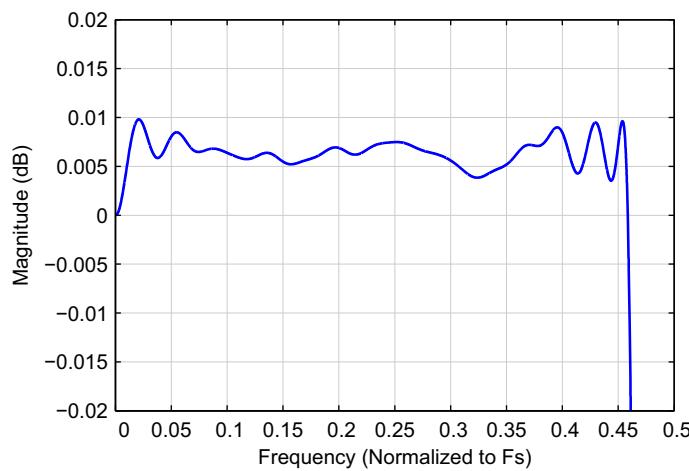


Figure 9-19. Passband Ripple

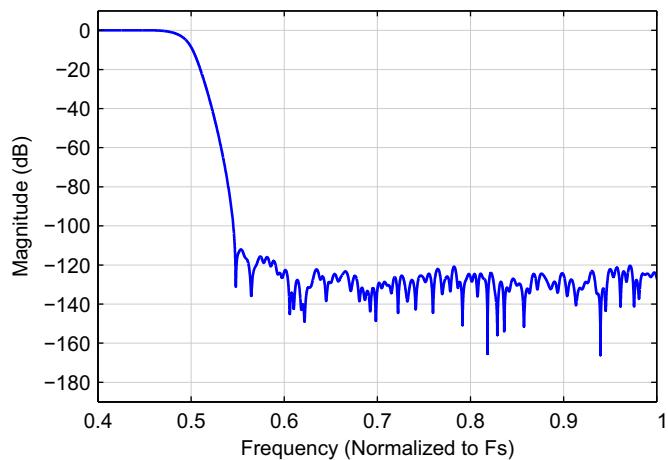


Figure 9-20. Stopband Attenuation

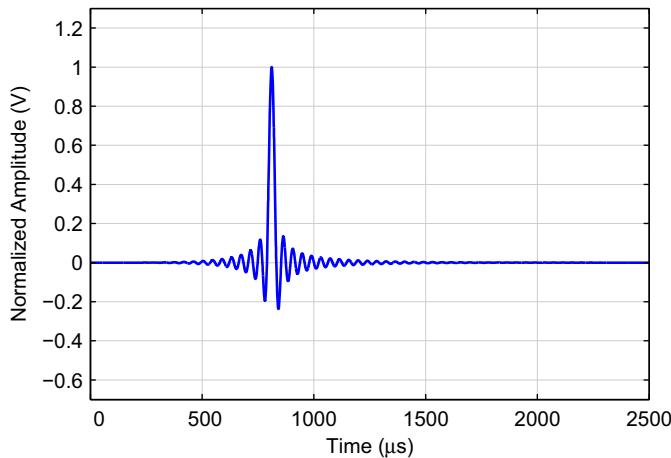


Figure 9-21. Impulse Response—Linear Phase

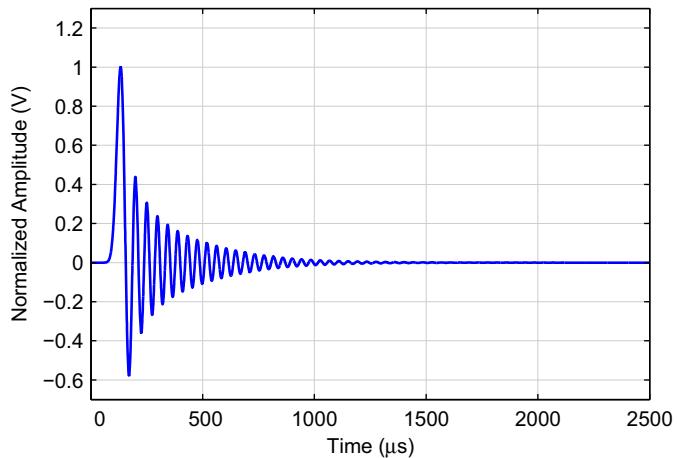


Figure 9-22. Impulse Response—Minimum Phase

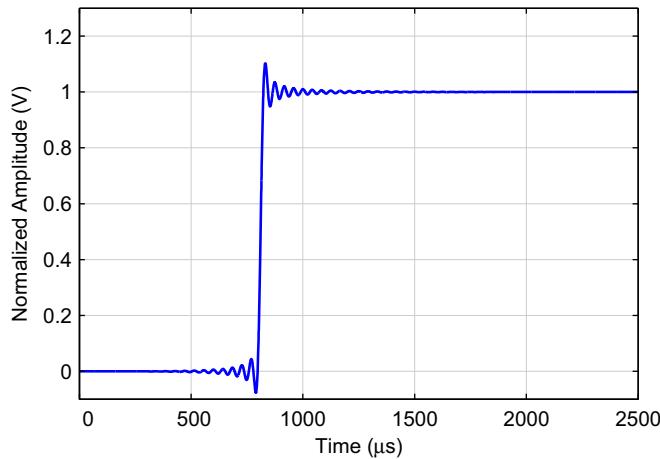


Figure 9-23. Step Response—Linear Phase

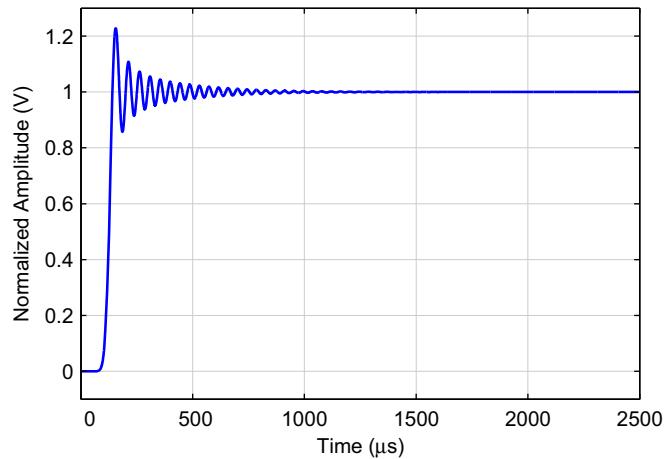


Figure 9-24. Step Response—Minimum Phase

9.1.4 组合滤波器响应——单速（采样频率 = 44.1 kHz 和 48 kHz，快速滚降）

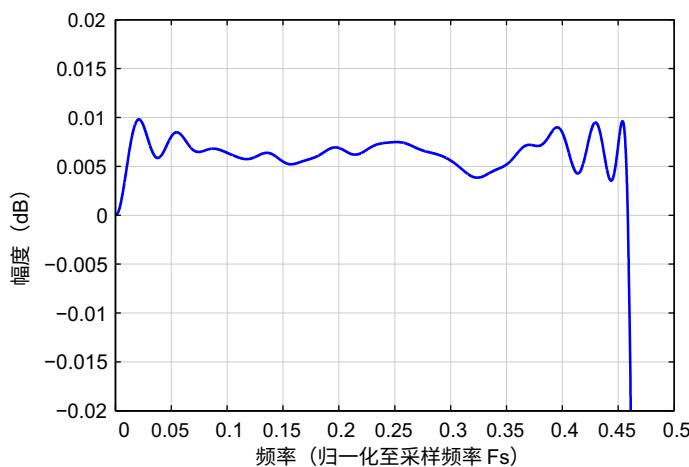


图 9-19。通带波纹

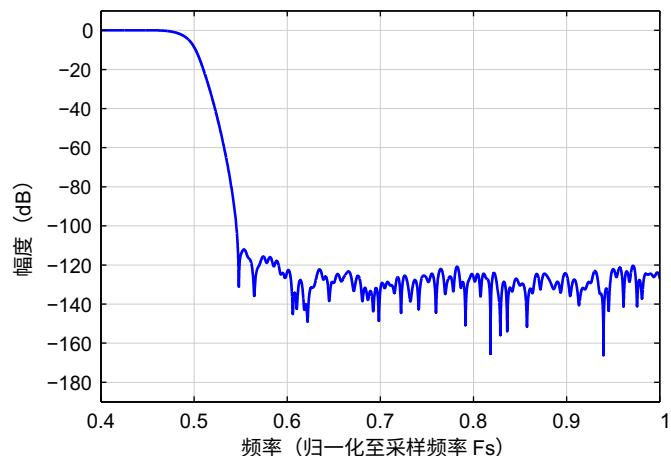


图 9-20。阻带衰减

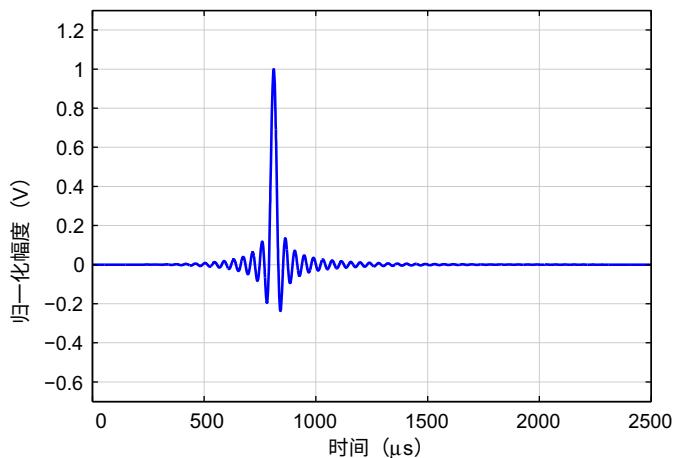


图 9-21。脉冲响应—线性相位

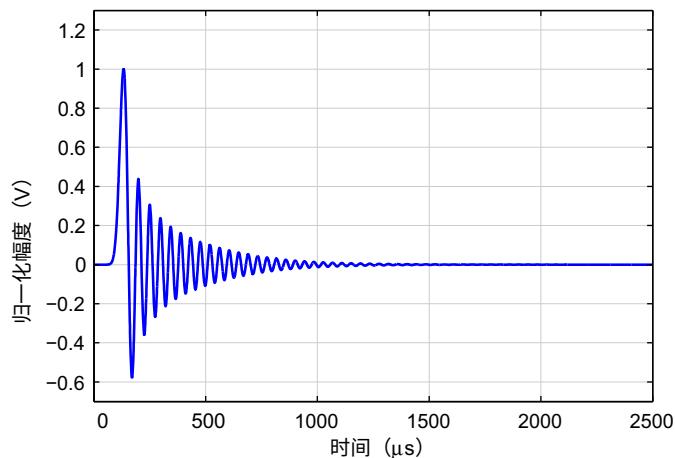


图 9-22。脉冲响应—最小相位

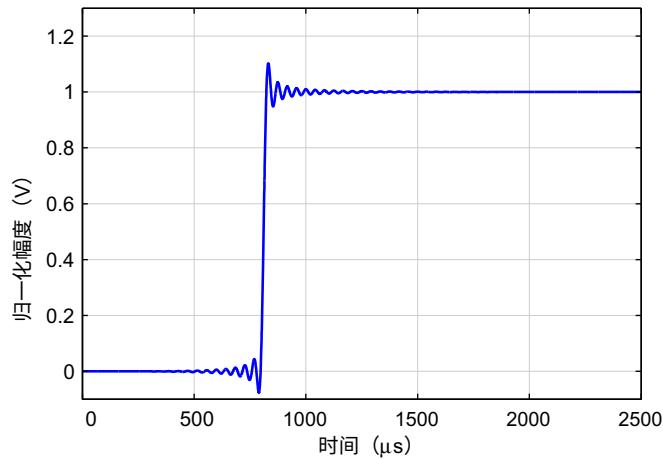


图 9-23。阶跃响应—线性相位

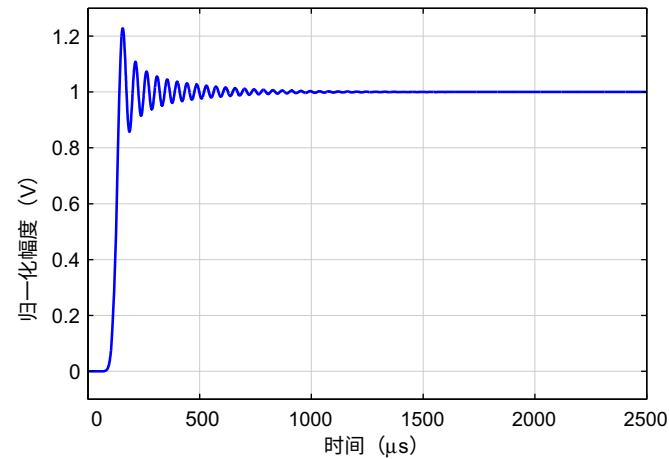


图 9-24。阶跃响应—最小相位

9.1.5 Combined Filter Response—Double Speed (Slow Roll-Off)

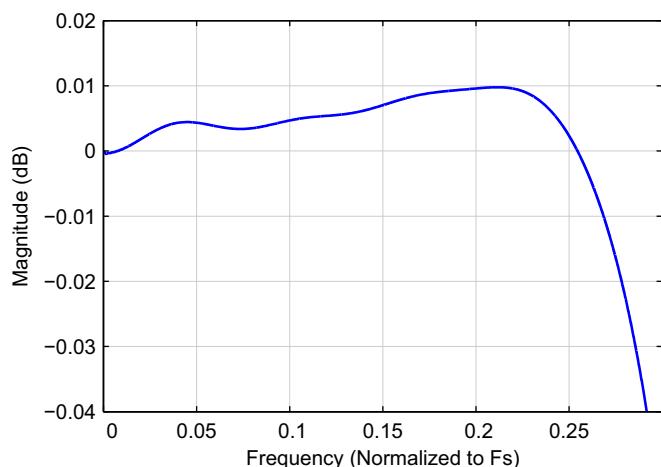


Figure 9-25. Passband Ripple

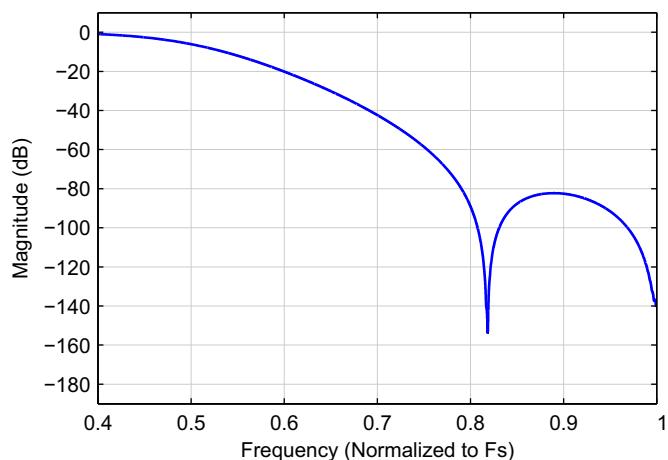


Figure 9-26. Stopband Attenuation

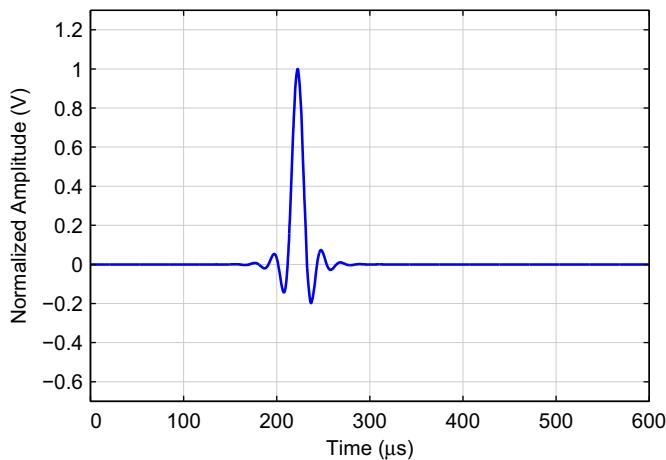


Figure 9-27. Impulse Response—Linear Phase

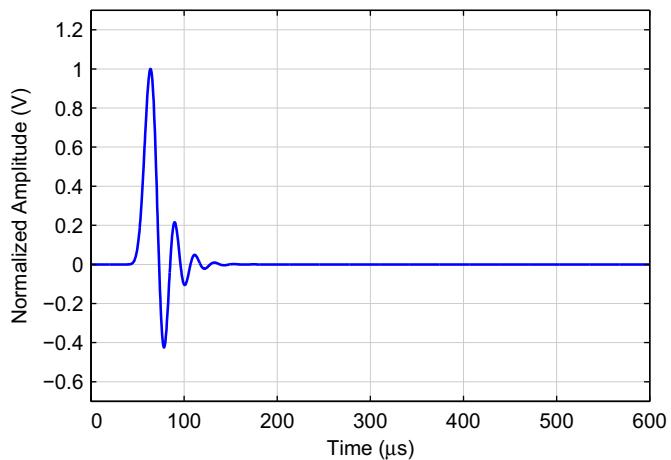


Figure 9-28. Impulse Response—Minimum Phase

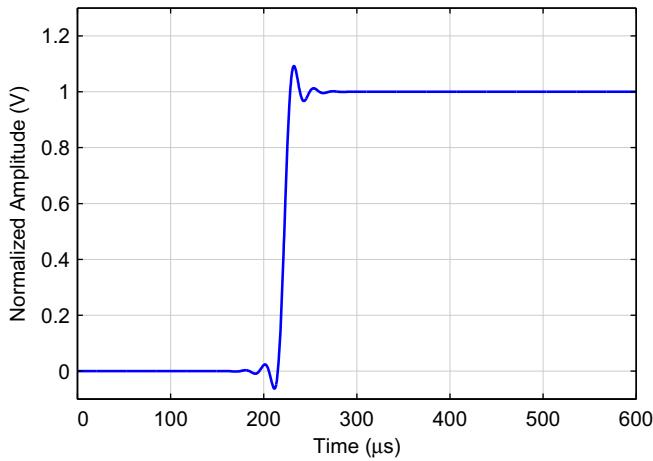


Figure 9-29. Step Response—Linear Phase

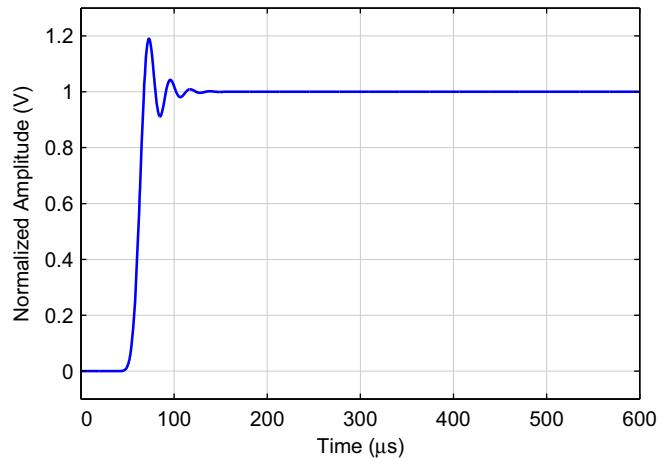


Figure 9-30. Step Response—Minimum Phase

9.1.5 组合滤波器响应——双速（缓慢滚降）

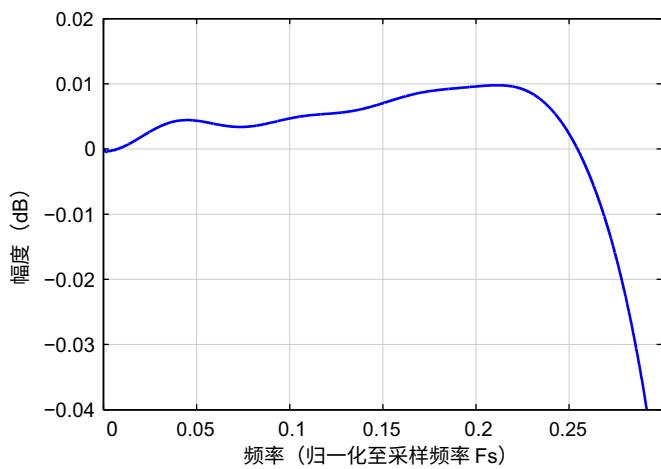


图 9-25。通带波纹

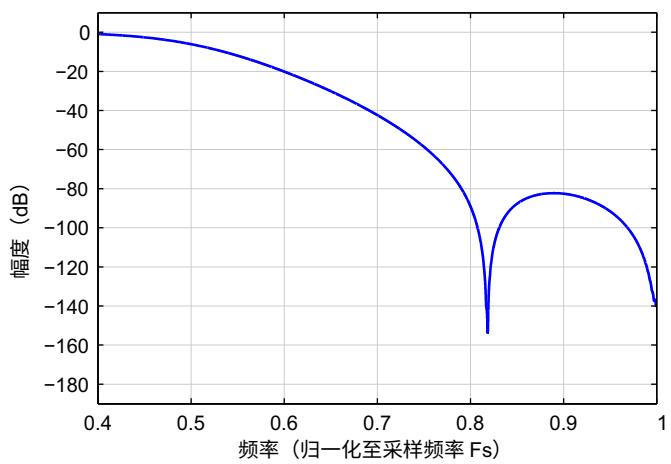


图 9-26。阻带衰减

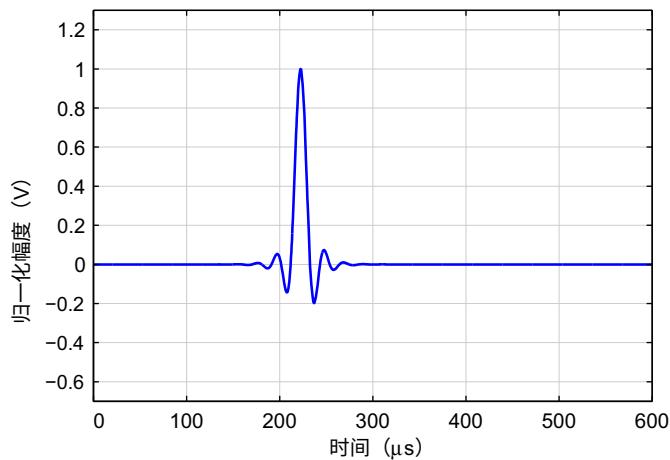


图 9-27。脉冲响应—线性相位

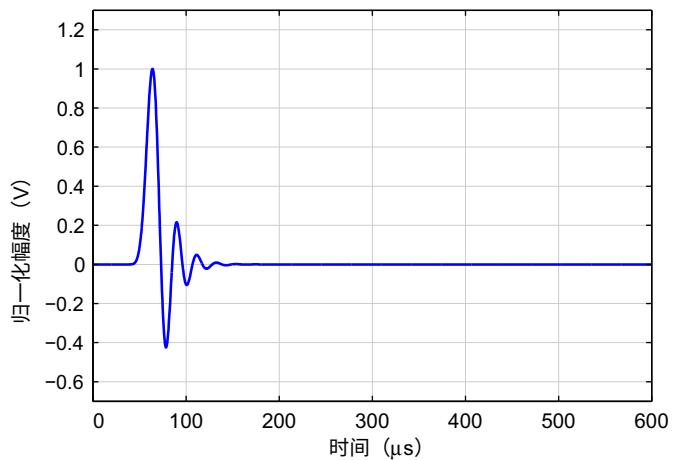


图 9-28。脉冲响应—最小相位

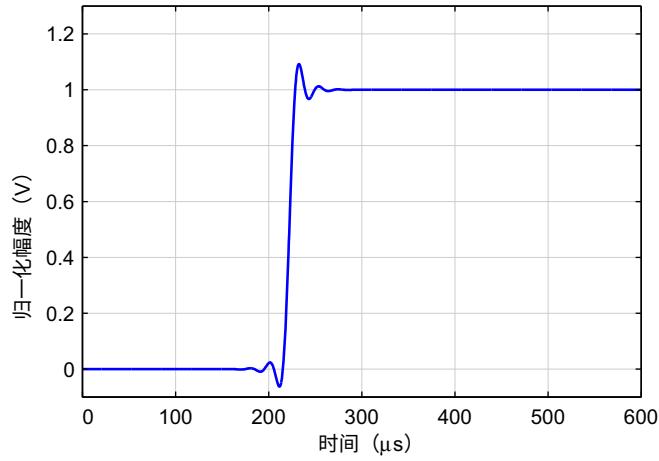


图 9-29。阶跃响应—线性相位

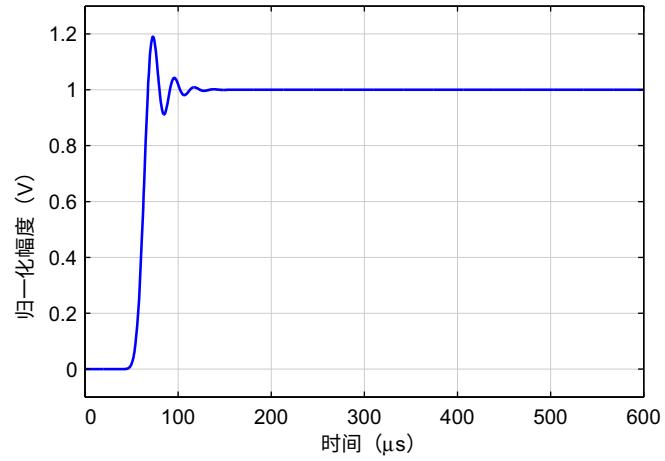


图 9-30。阶跃响应—最小相位

9.1.6 Combined Filter Response—Double Speed (Fast Roll-Off)

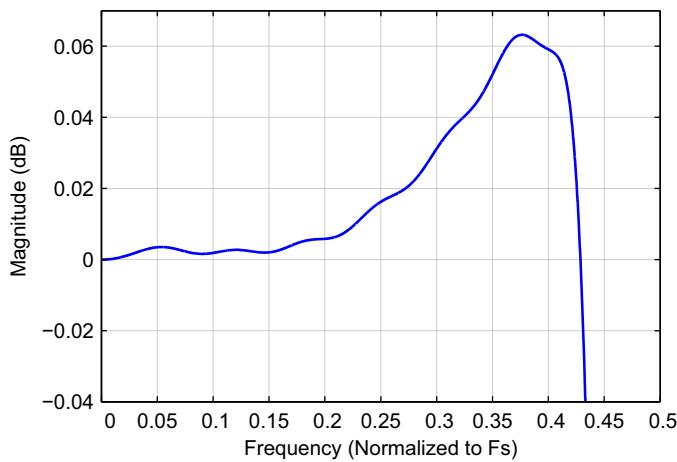


Figure 9-31. Passband Ripple

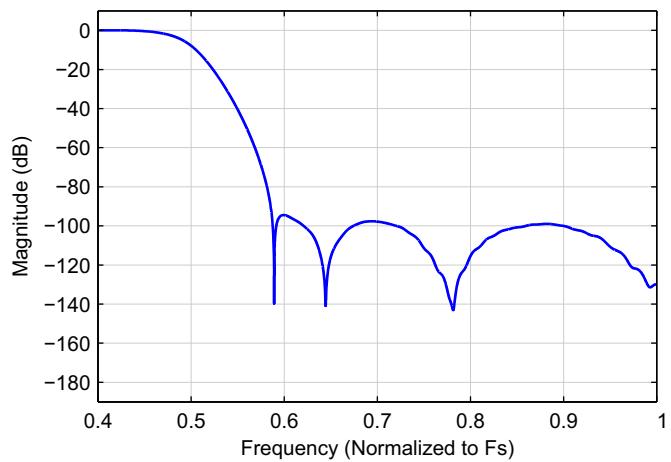


Figure 9-32. Stopband Attenuation

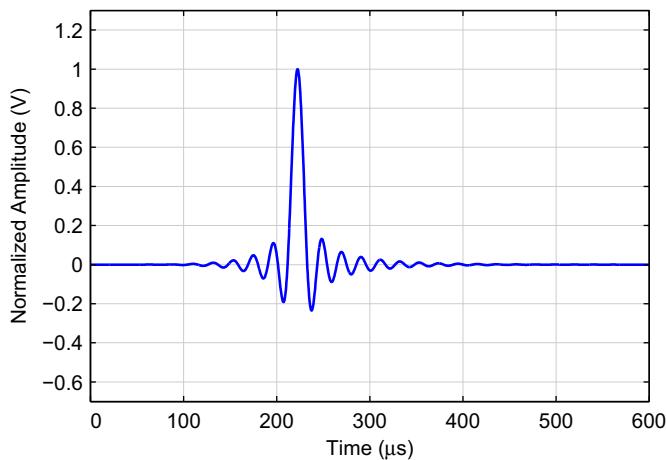


Figure 9-33. Impulse Response—Linear Phase

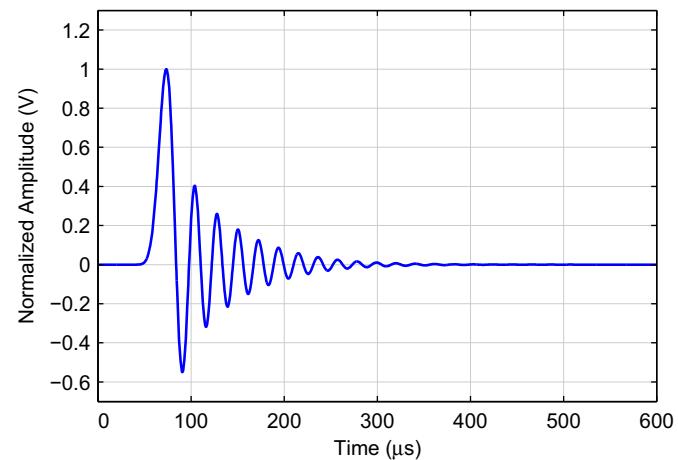


Figure 9-34. Impulse Response—Minimum Phase

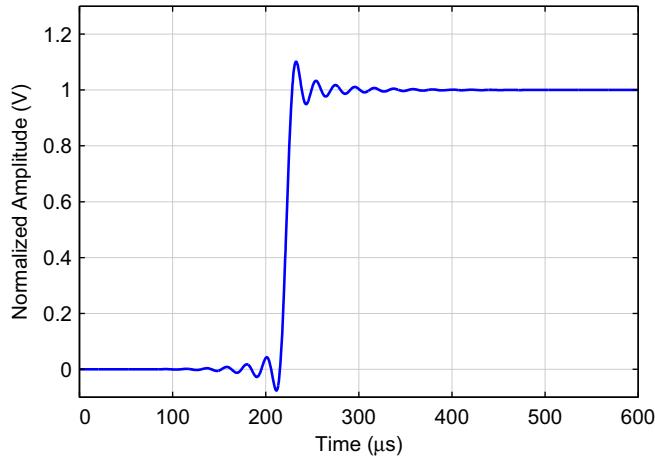


Figure 9-35. Step Response—Linear Phase

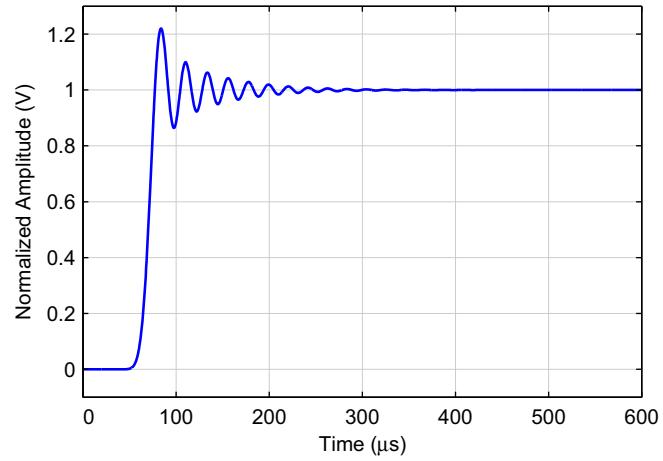


Figure 9-36. Step Response—Minimum Phase

9.1.6 组合滤波器响应——双倍速（快速滚降）

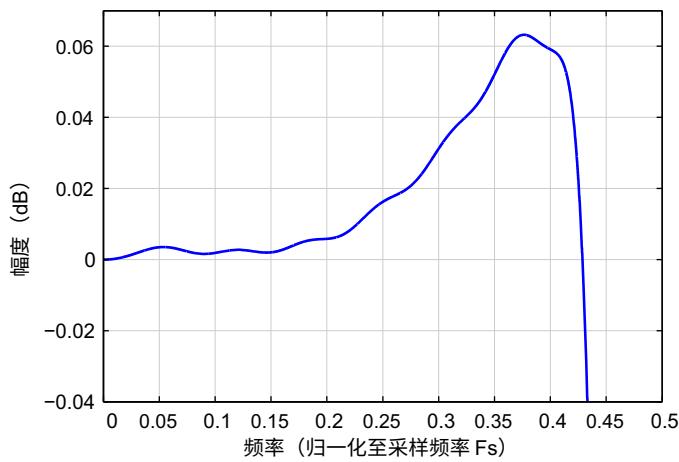


图 9-31。通带波纹

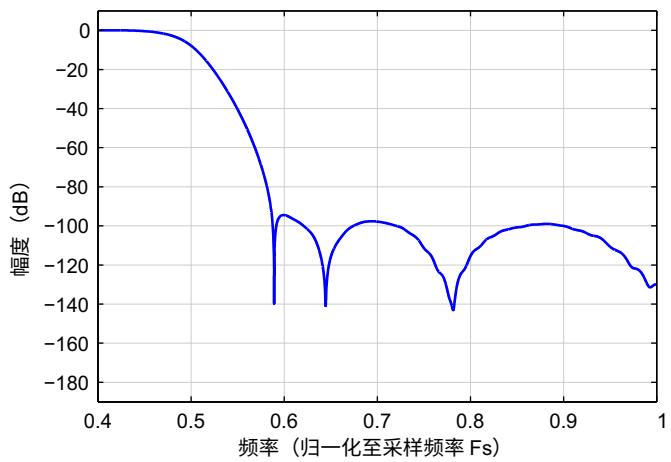


图 9-32。阻带衰减

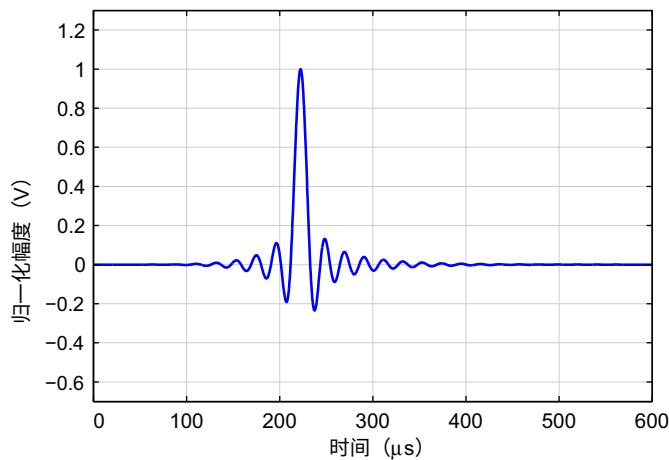


图 9-33。脉冲响应—线性相位

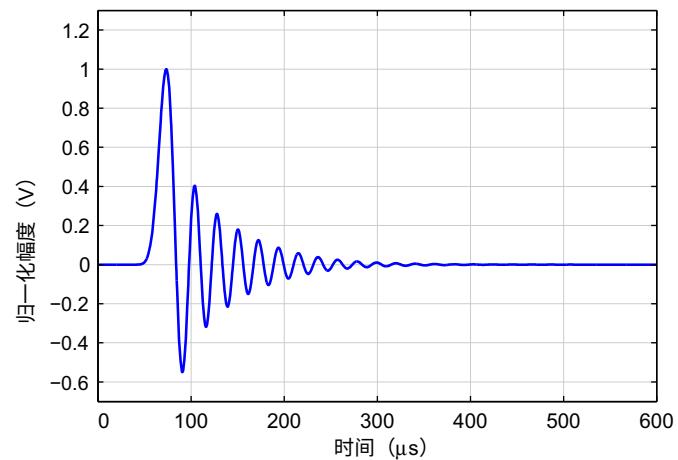


图 9-34。脉冲响应—最小相位

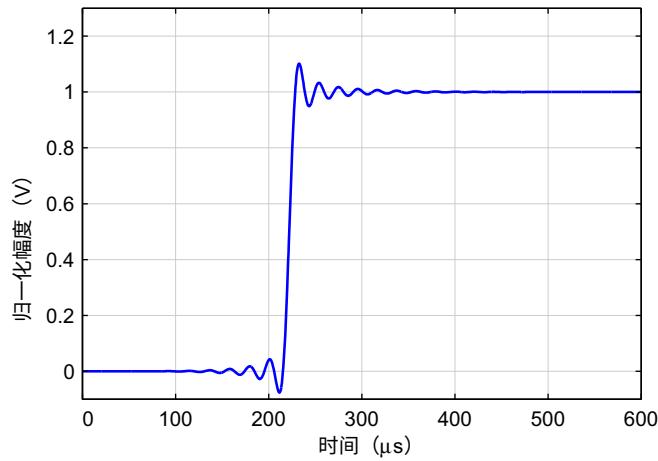


图 9-35。阶跃响应—线性相位

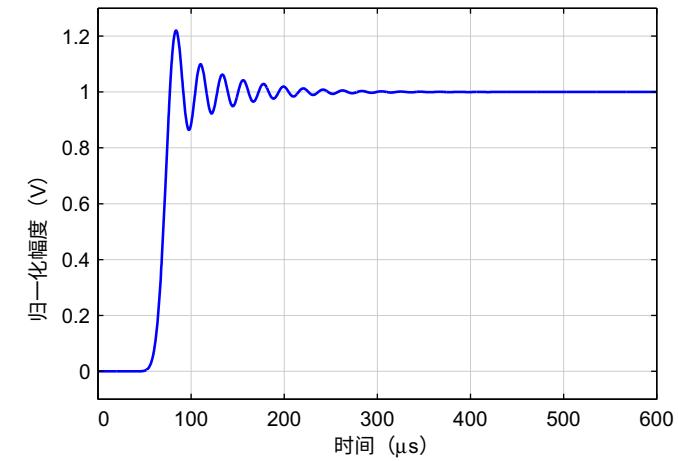


图 9-36。阶跃响应—最小相位

9.1.7 Combined Filter Response—Quad Speed (Slow Roll-Off)

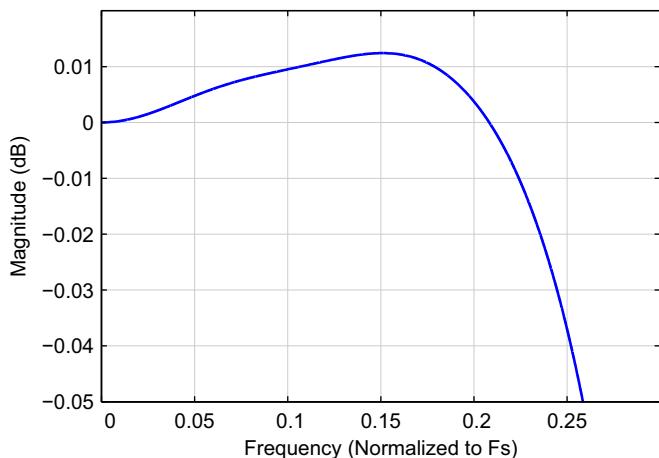


Figure 9-37. Passband Ripple

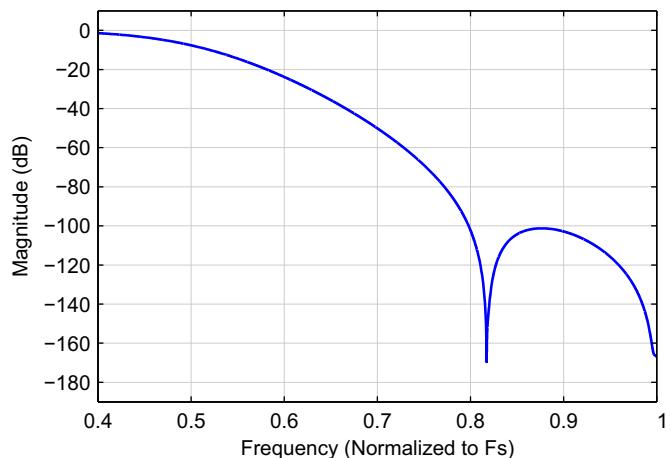


Figure 9-38. Stopband Attenuation

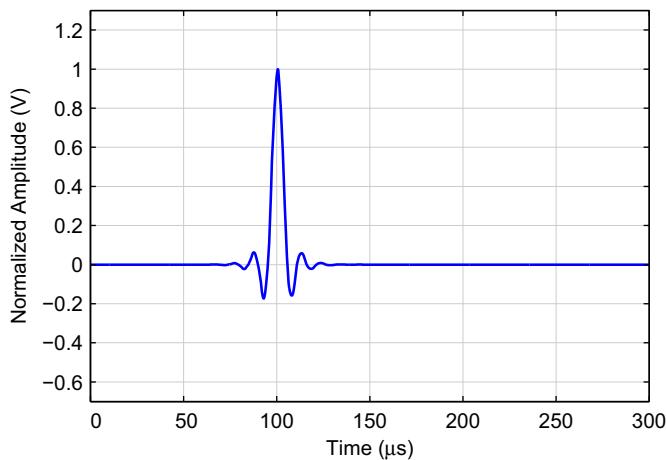


Figure 9-39. Impulse Response—Linear Phase

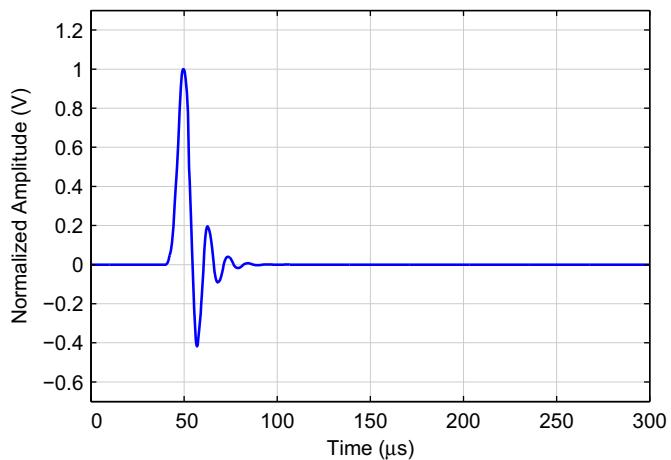


Figure 9-40. Impulse Response—Minimum Phase

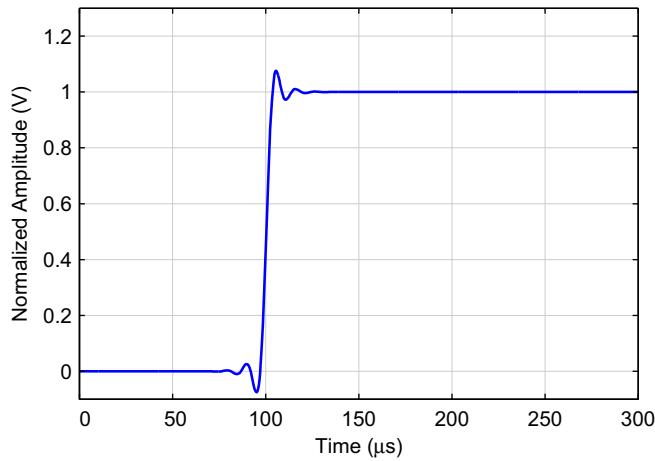


Figure 9-41. Step Response—Linear Phase

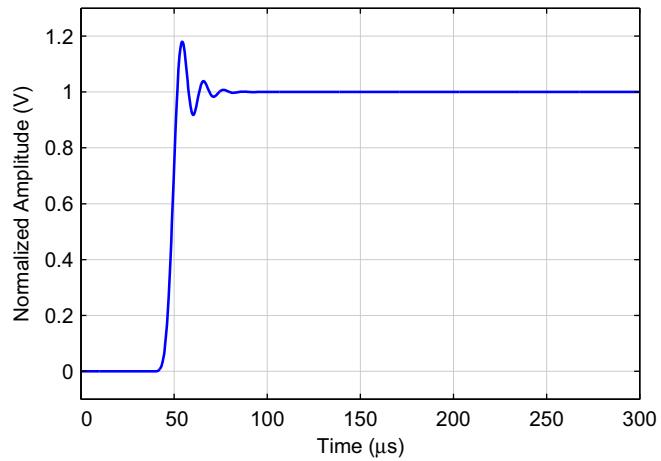


Figure 9-42. Step Response—Minimum Phase

9.1.7 组合滤波器响应——四倍速（慢速滚降）

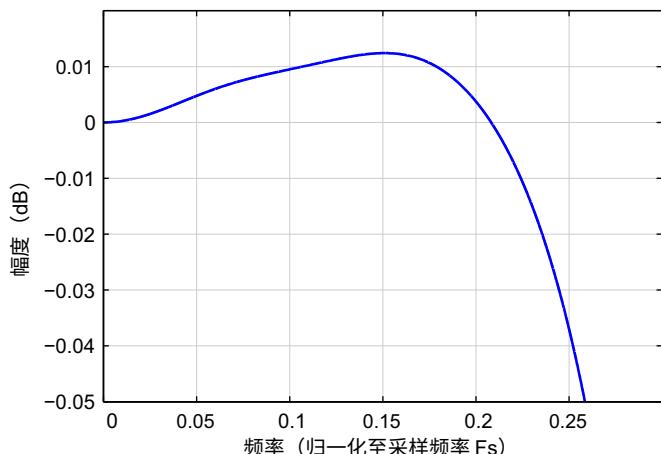


图 9-37。通带波纹

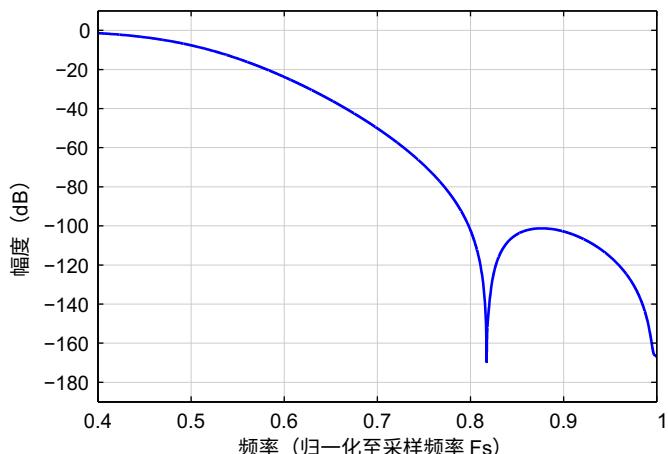


图 9-38。阻带衰减

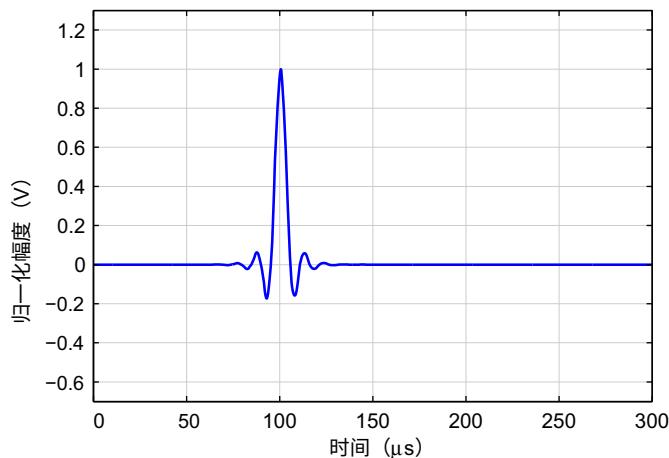


图 9-39。脉冲响应—线性相位

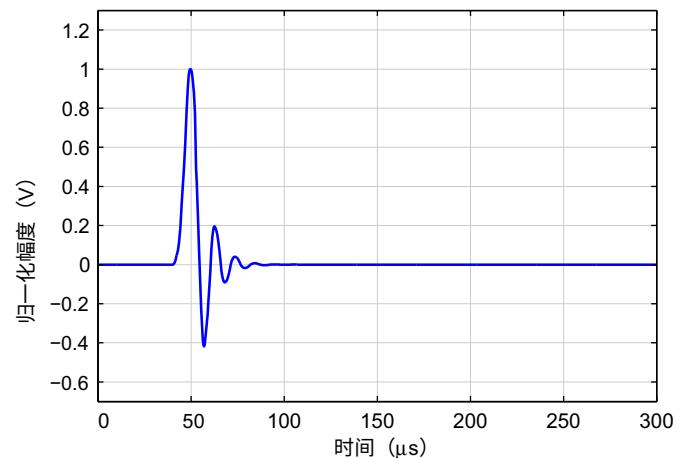


图 9-40。脉冲响应—最小相位

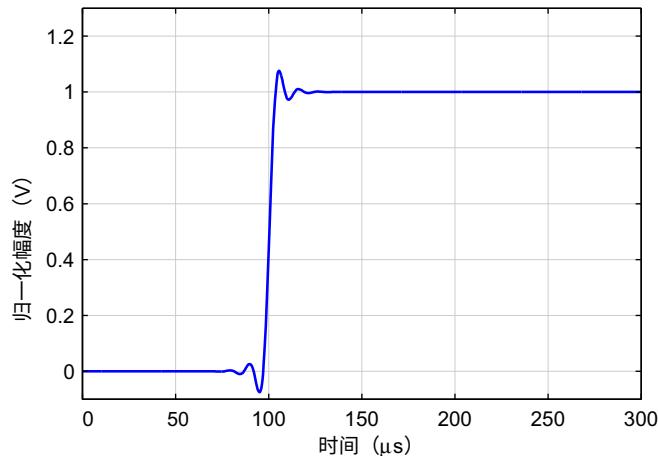


图 9-41。阶跃响应—线性相位

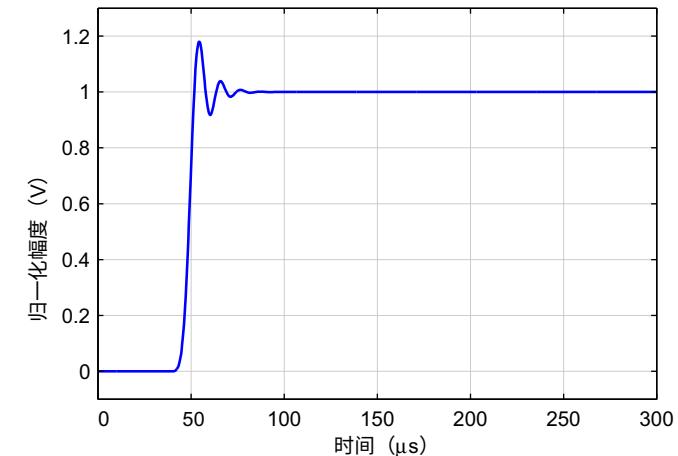


图 9-42。阶跃响应—最小相位

9.1.8 Combined Filter Response—Quad Speed (Fast Roll-Off)

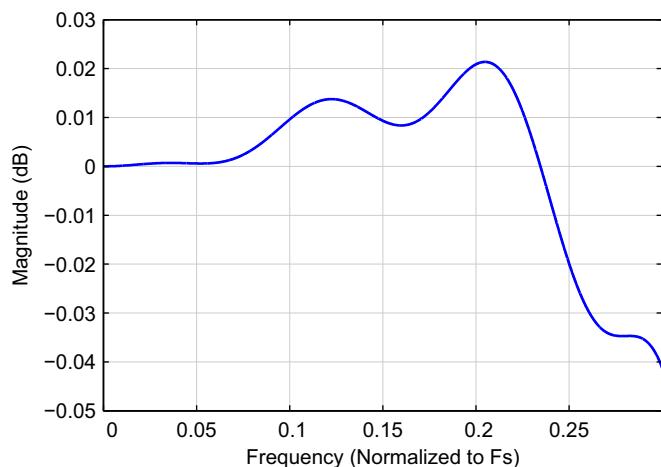


Figure 9-43. Passband Ripple

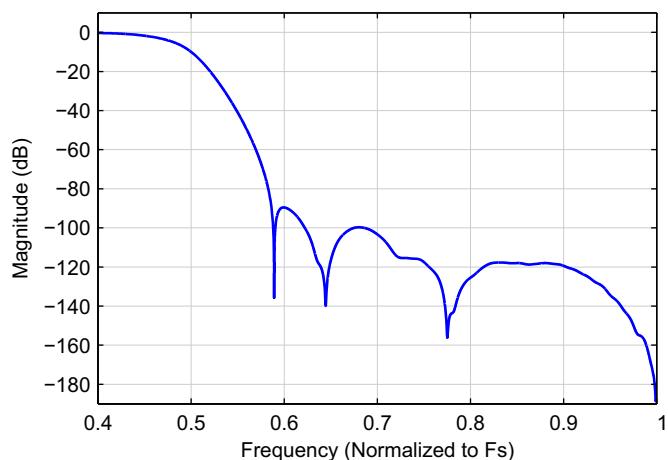


Figure 9-44. Stopband Attenuation

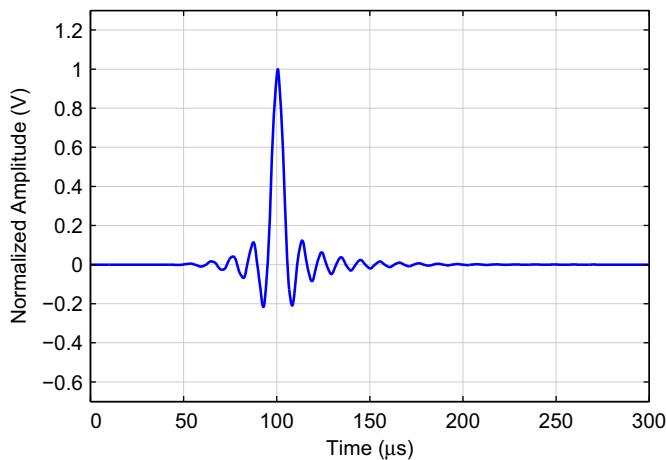


Figure 9-45. Impulse Response—Linear Phase

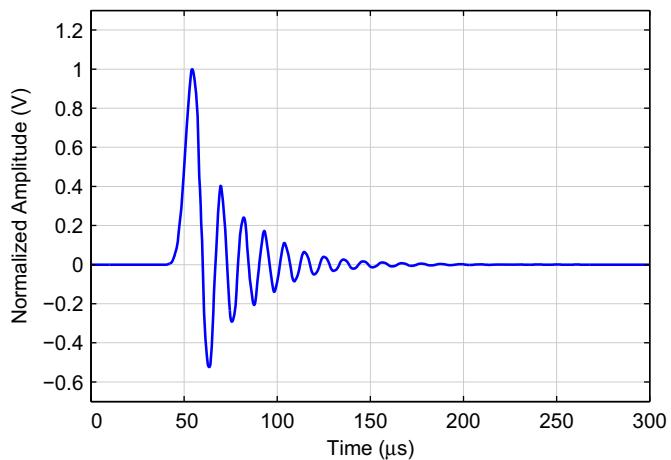


Figure 9-46. Impulse Response—Minimum Phase

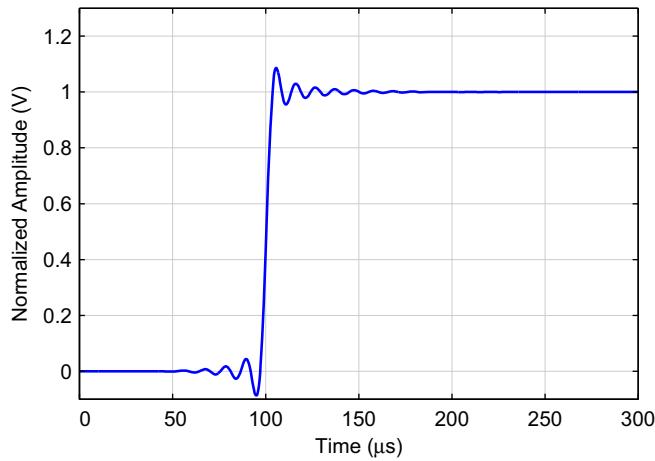


Figure 9-47. Step Response—Linear Phase

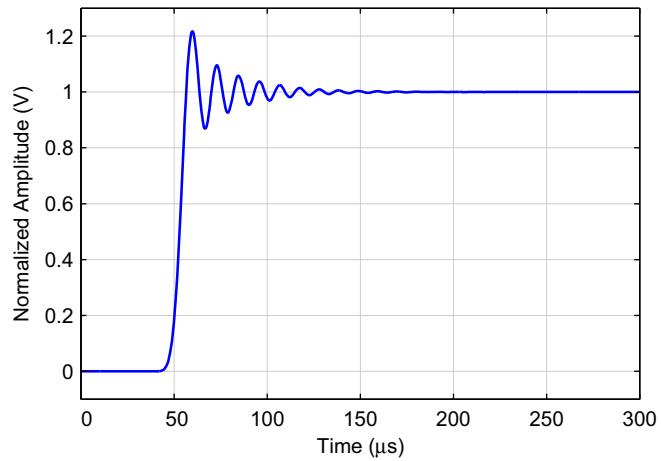


Figure 9-48. Step Response—Minimum Phase

9.1.8 组合滤波器响应—四倍速（快速滚降）

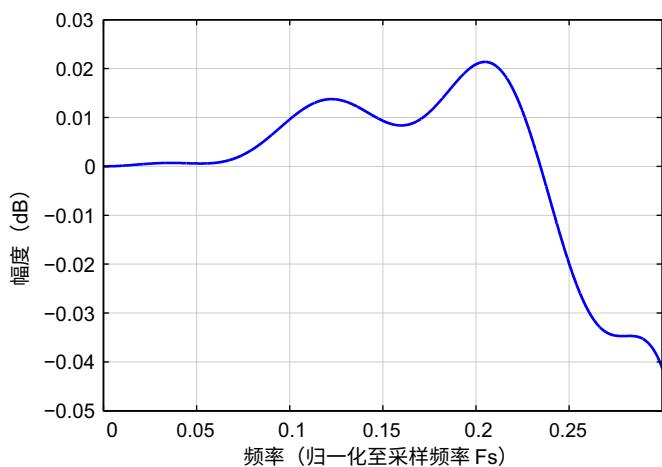


图 9-43. 通带波纹

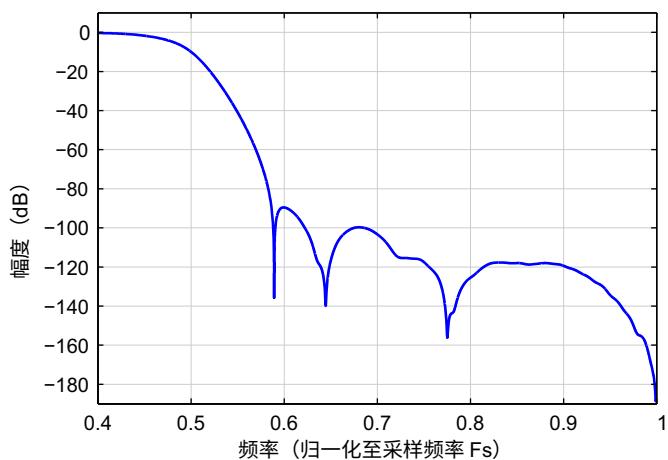


图 9-44. 阻带衰减

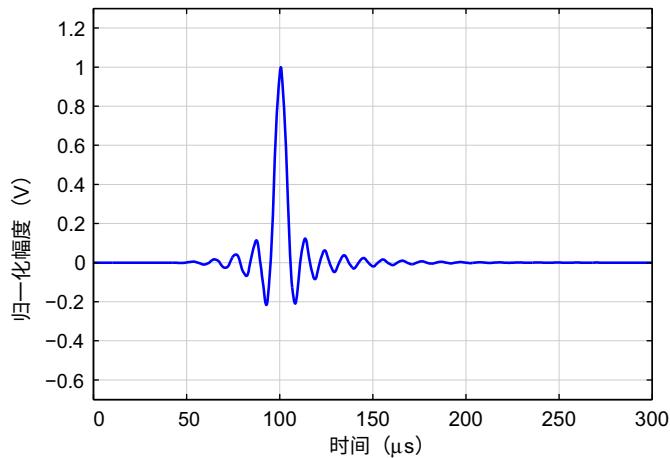


图 9-45. 脉冲响应—线性相位

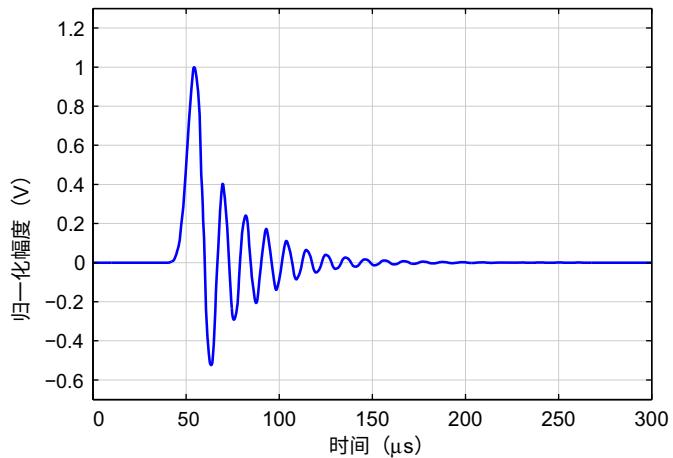


图 9-46. 脉冲响应—最小相位

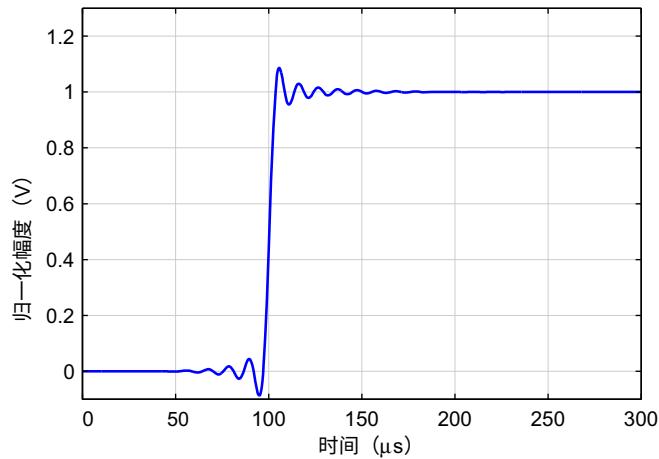


图 9-47. 阶跃响应—线性相位

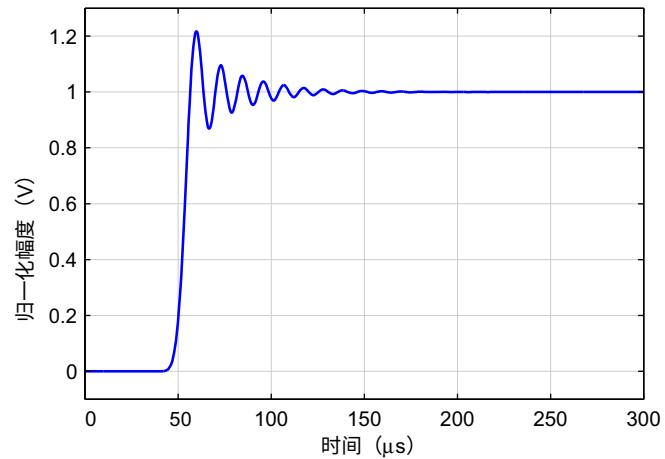


图 9-48. 阶跃响应—最小相位

9.1.9 Combined Filter Response—Octuple Speed

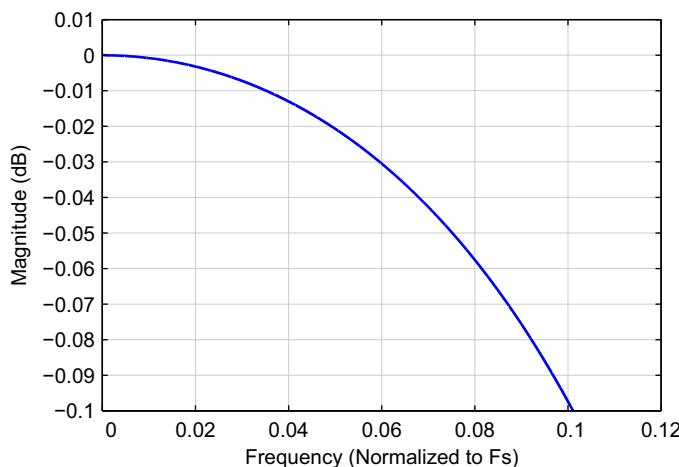


Figure 9-49. Passband Ripple

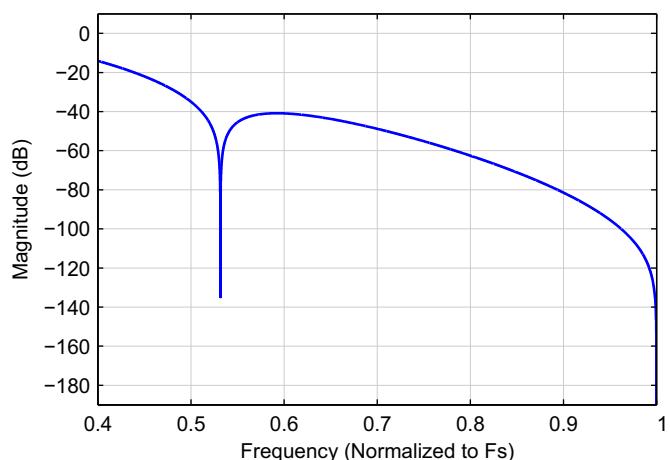


Figure 9-50. Stopband Attenuation

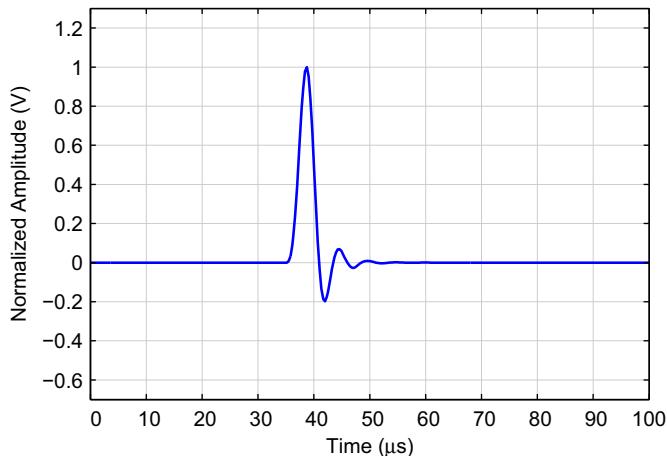


Figure 9-51. Impulse Response

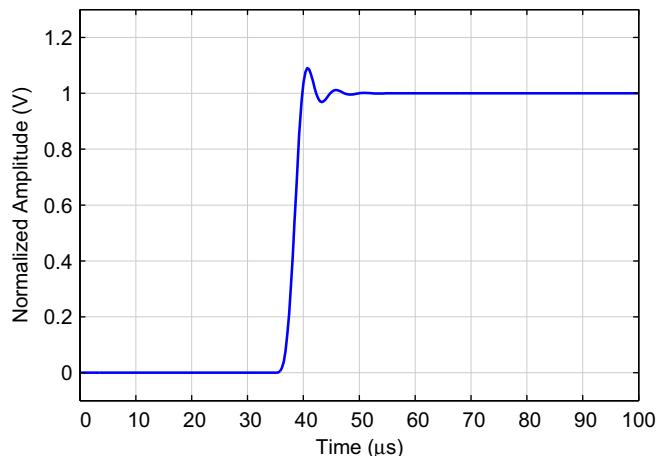


Figure 9-52. Step Response

9.1.10 Combined Filter Response—Single Speed (NOS = 1)

Note: 44.1 kHz and 48 kHz only.

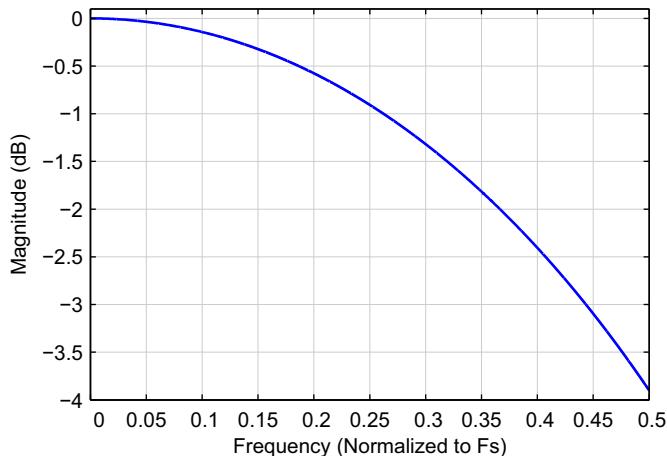


Figure 9-53. Passband Ripple

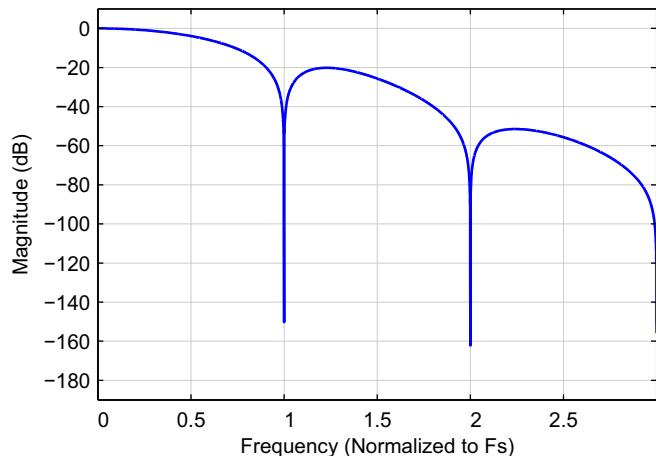


Figure 9-54. Stopband Attenuation

9.1.9 组合滤波器响应—八倍速

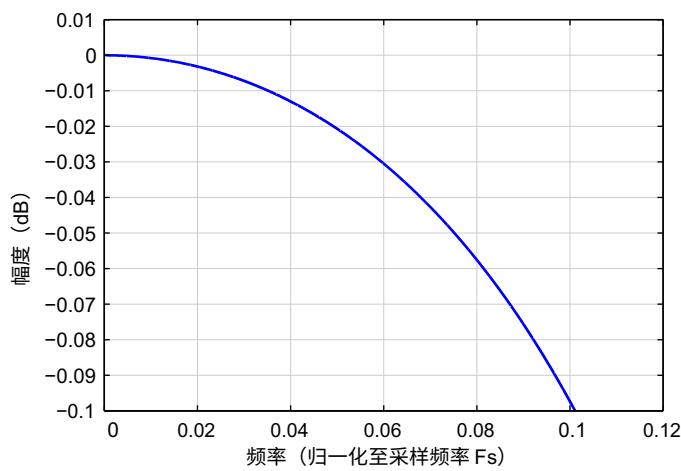


图 9-49. 通带波纹

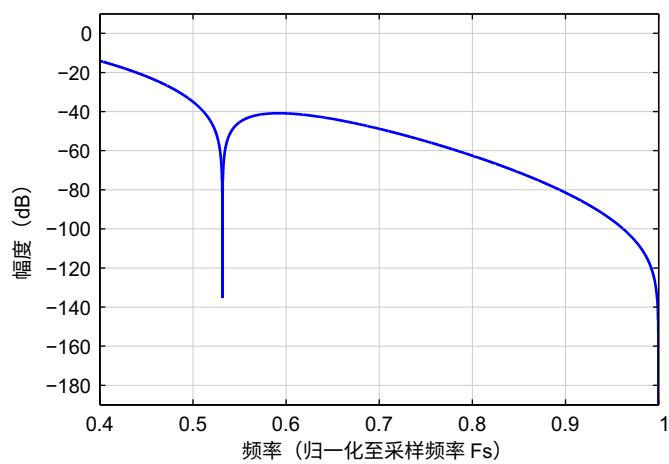


图 9-50. 阻带衰减

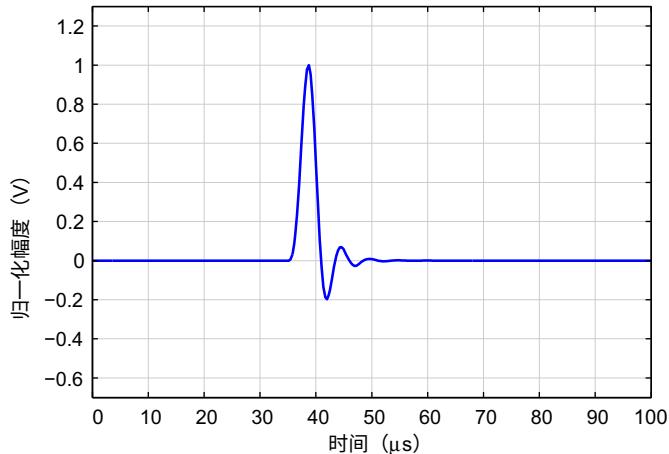


图 9-51. 脉冲响应

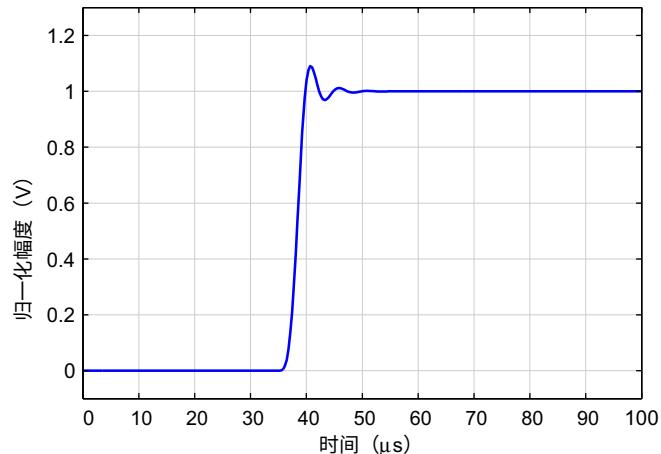


图 9-52. 阶跃响应

9.1.10 组合滤波器响应—单倍速 (NOS = 1)

注：仅适用于 44.1 kHz 和 48 kHz。

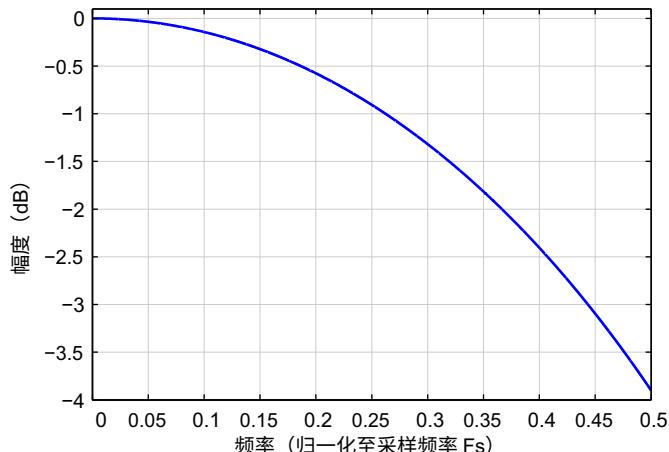


图 9-53. 通带波纹

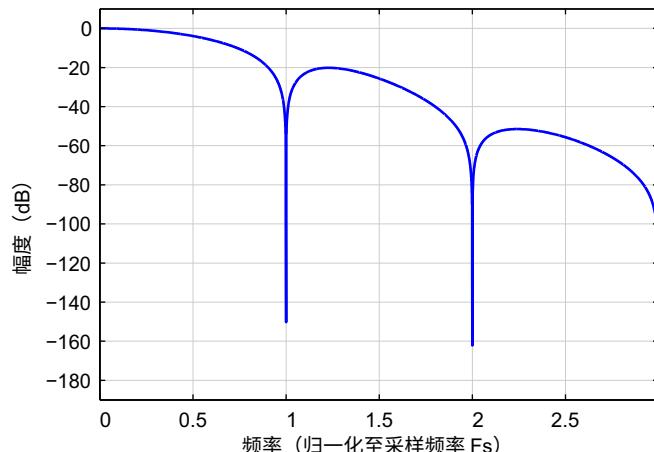


图 9-54. 阻带衰减

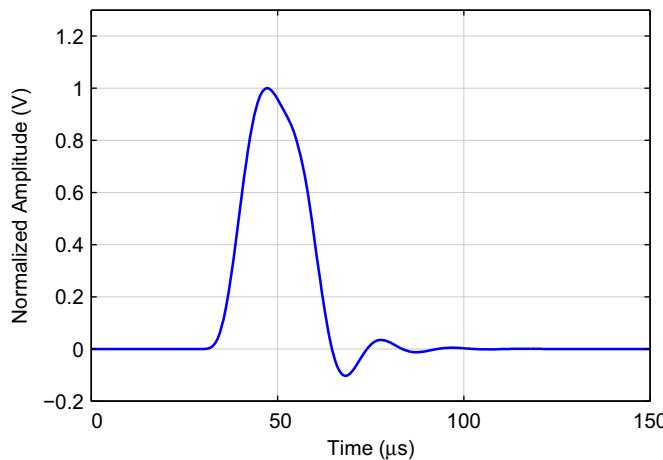


Figure 9-55. Impulse Response

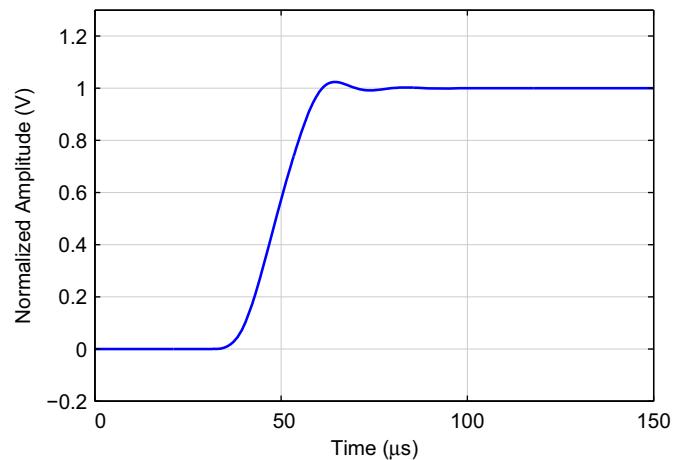


Figure 9-56. Step Response

9.1.11 Combined Filter Response—Double Speed (NOS = 1)

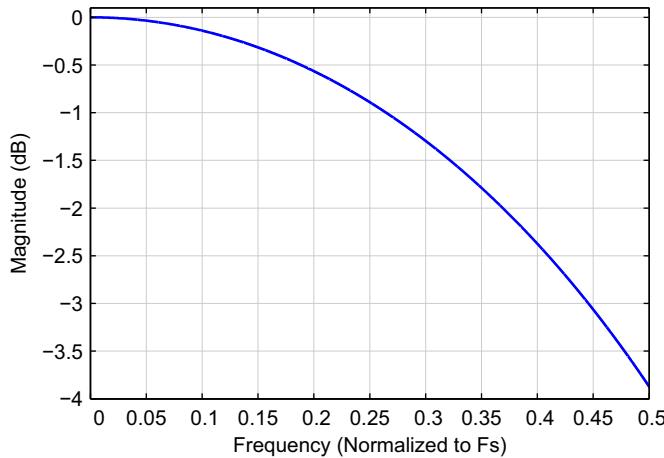


Figure 9-57. Passband Ripple

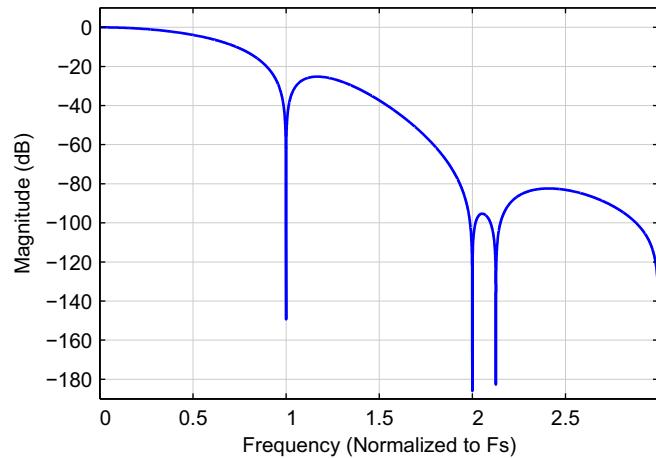


Figure 9-58. Stopband Attenuation

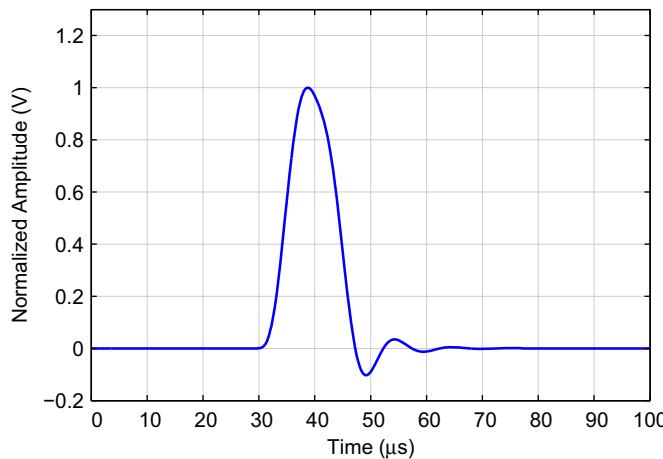


Figure 9-59. Impulse Response

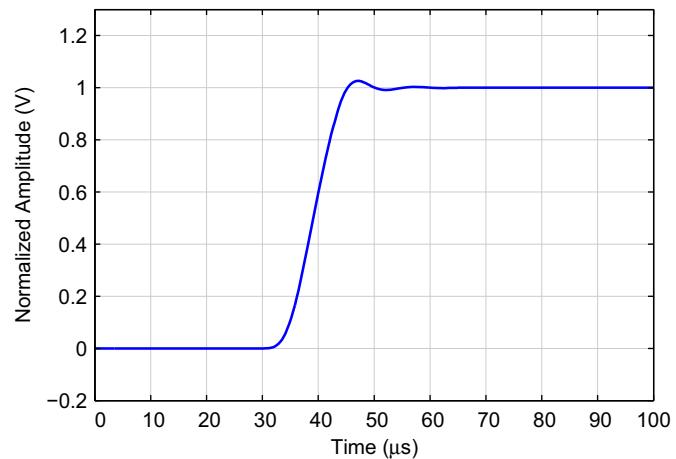


Figure 9-60. Step Response

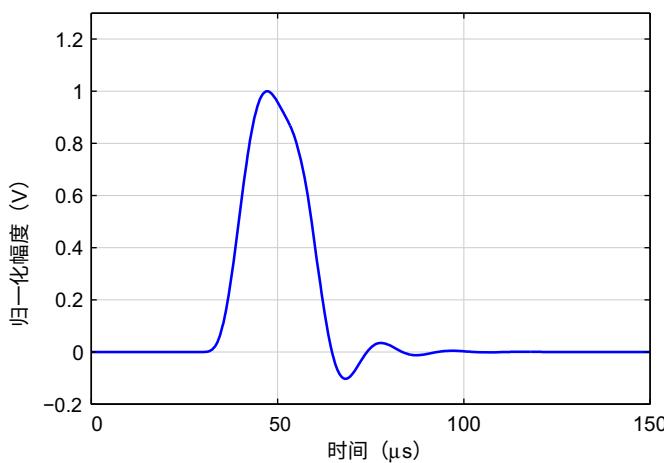


图 9-55. 脉冲响应

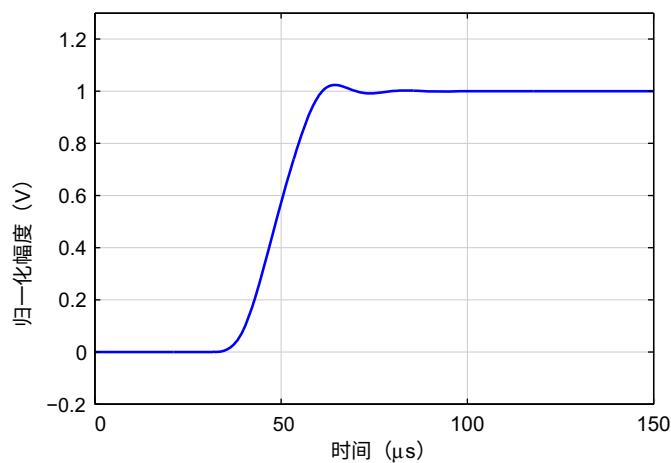


图 9-56 阶跃响应

9.1.11 组合滤波器响应—双倍速 (NOS = 1)

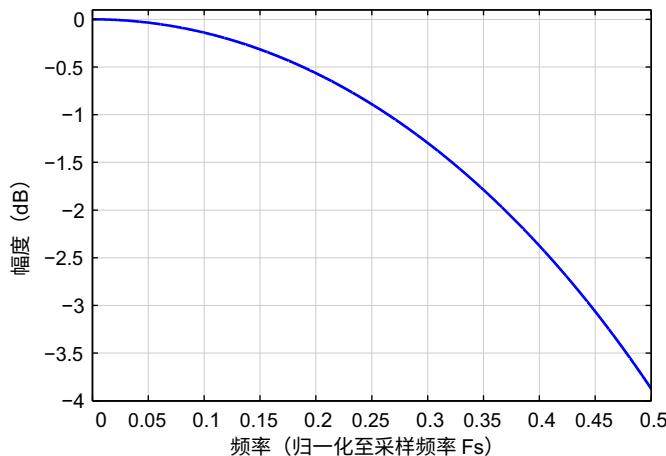


图 9-57 通带波纹

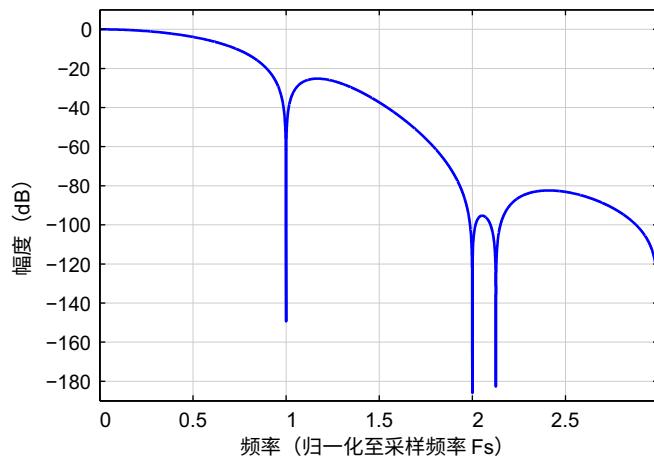


图 9-58 阻带衰减

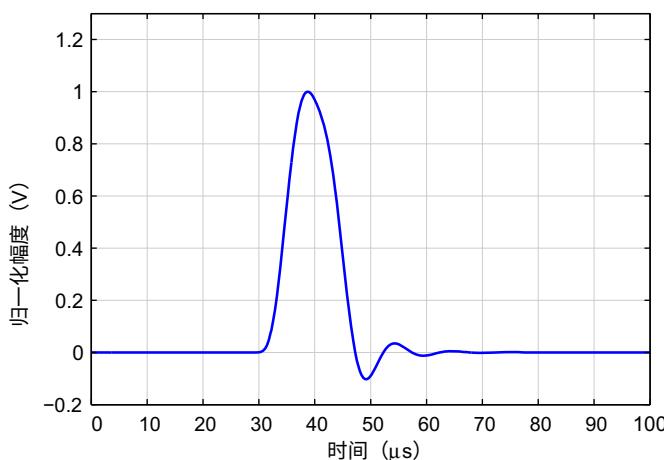


图 9-59 脉冲响应

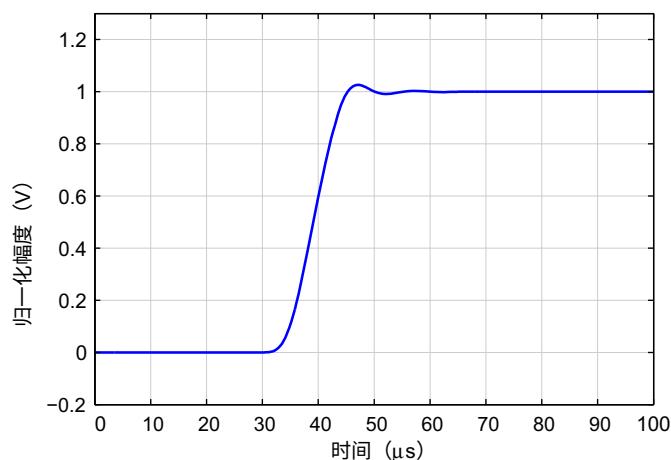


图 9-60 阶跃响应

9.1.12 Combined Filter Response—Quad Speed (NOS = 1)

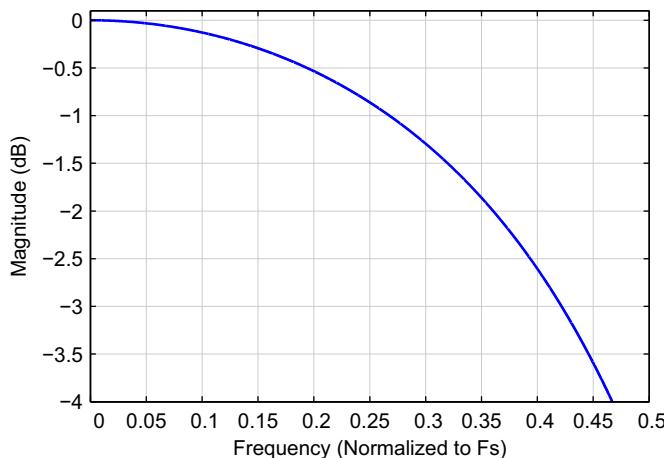


Figure 9-61. Passband Ripple

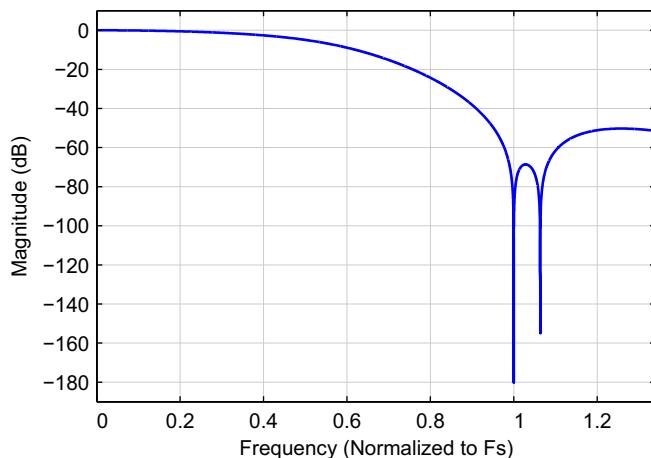


Figure 9-62. Stopband Attenuation

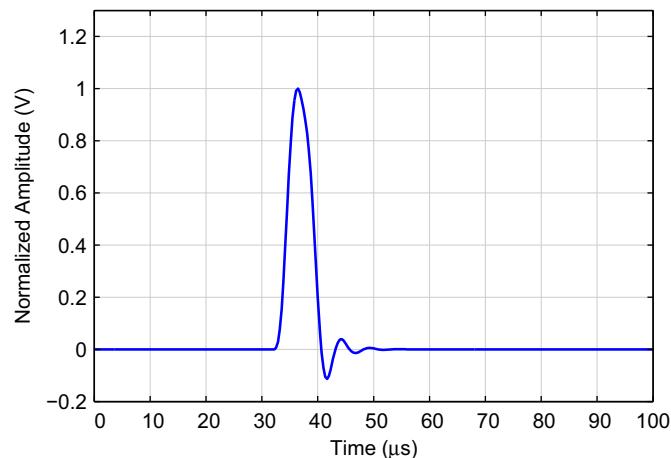


Figure 9-63. Impulse Response

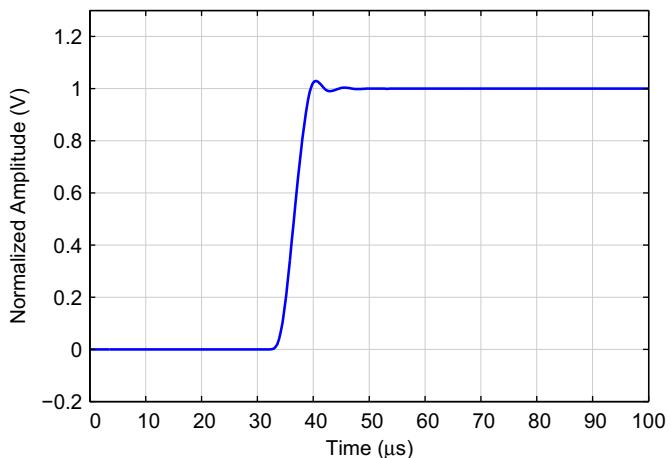


Figure 9-64. Step Response

9.1.13 Combined Filter Response—Wideband Flatness Mode

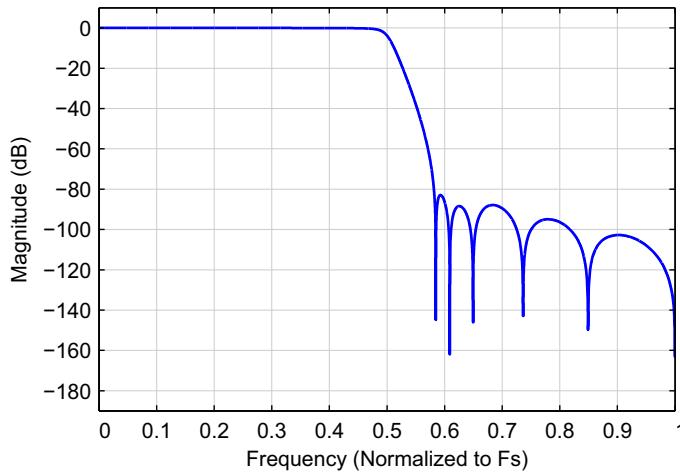


Figure 9-65. Magnitude Response

9.1.12 组合滤波器响应——四倍速 (NOS = 1)

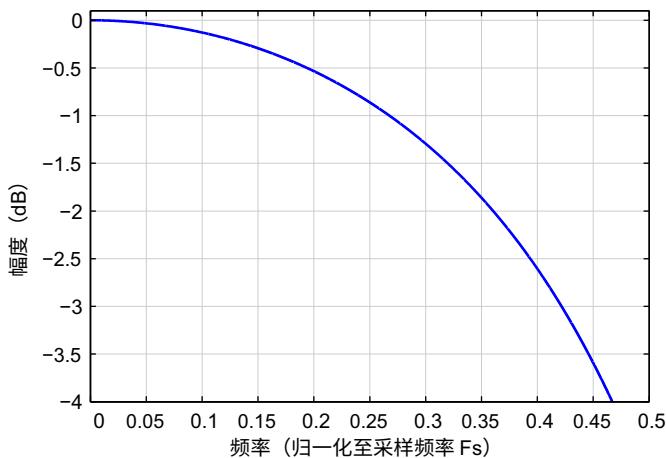


图 9-61 通带波纹

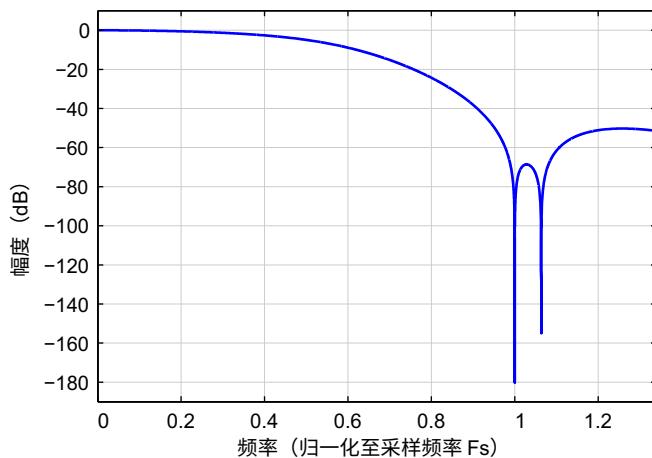


图 9-62 阻带衰减

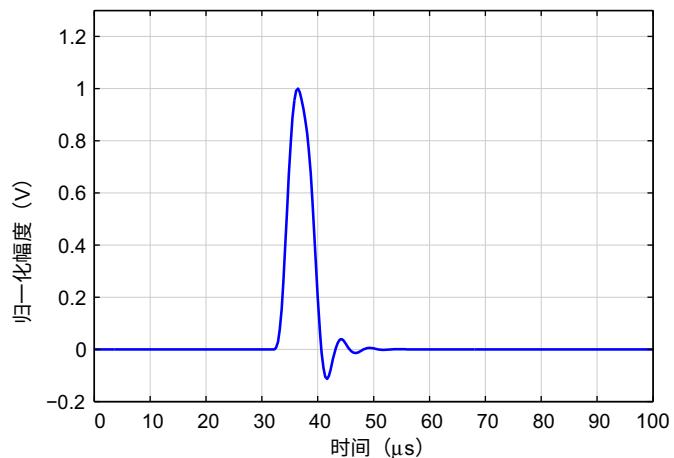


图 9-63 脉冲响应

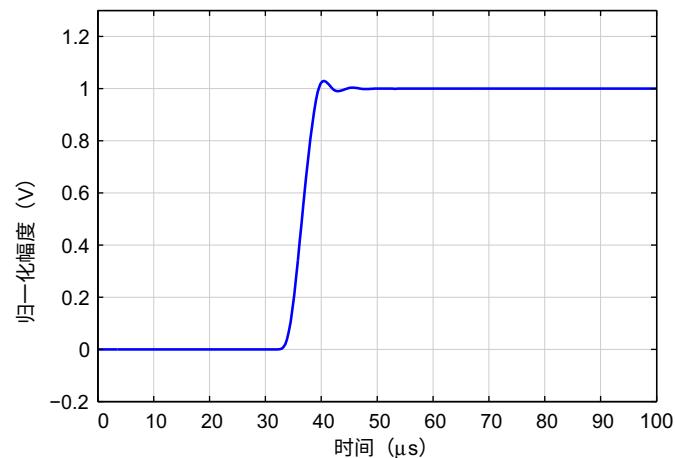


图 9-64 阶跃响应

9.1.13 组合滤波器响应——宽带平坦模式

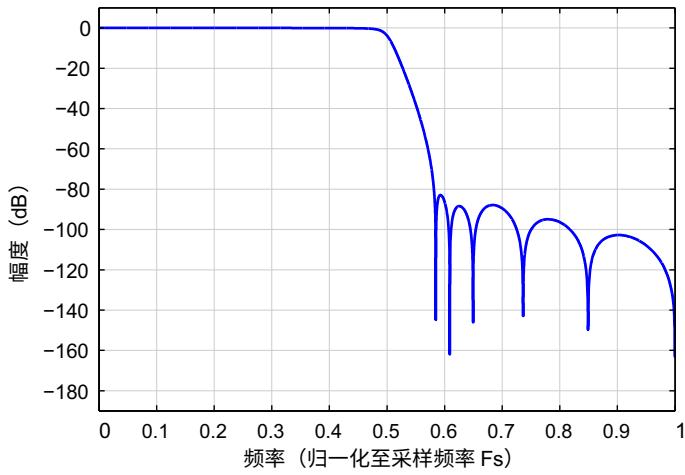


图 9-65 幅度响应

9.1.14 Combined Filter Response—DSD

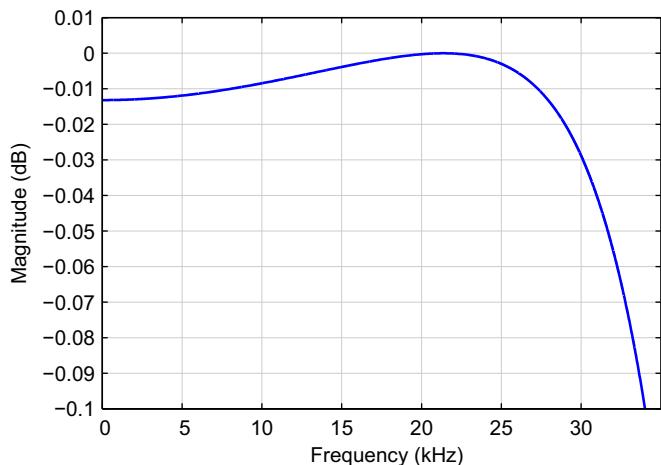


Figure 9-66. Passband Ripple

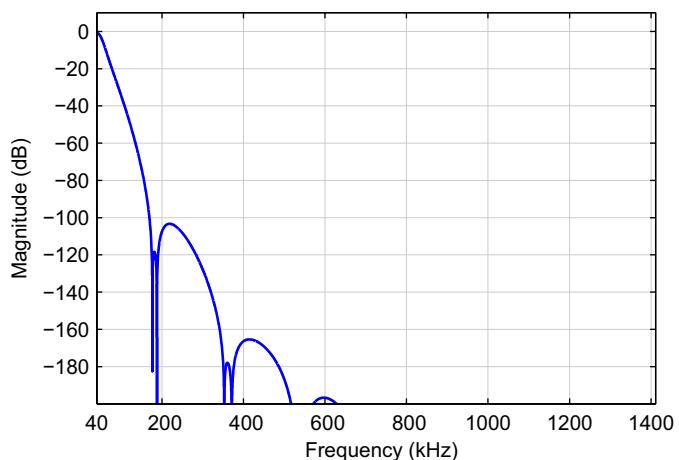


Figure 9-67. Stopband Attenuation

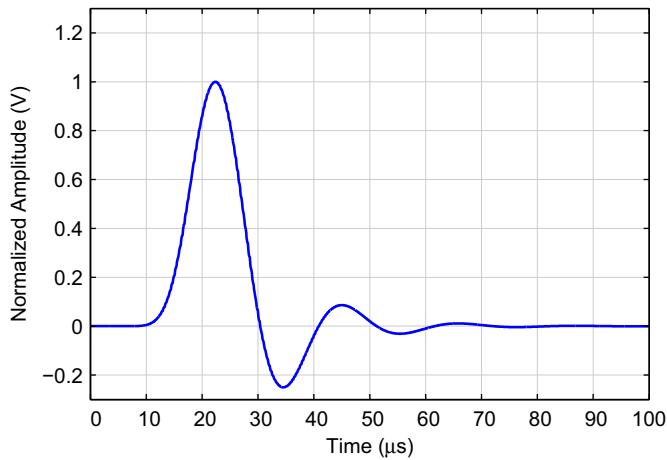


Figure 9-68. Impulse Response

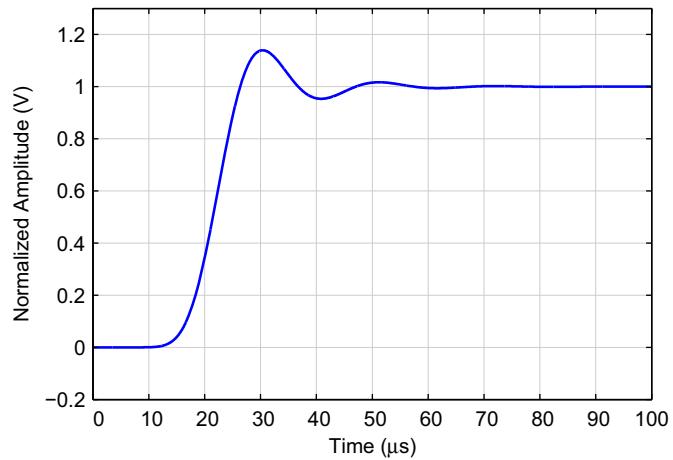


Figure 9-69. Step Response

9.1.15 Highpass Filter and Deemphasis

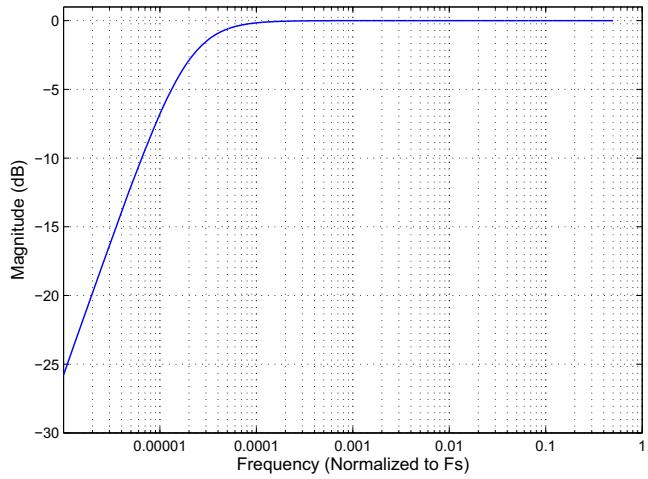


Figure 9-70. Highpass Filter for PCM and DSD Paths

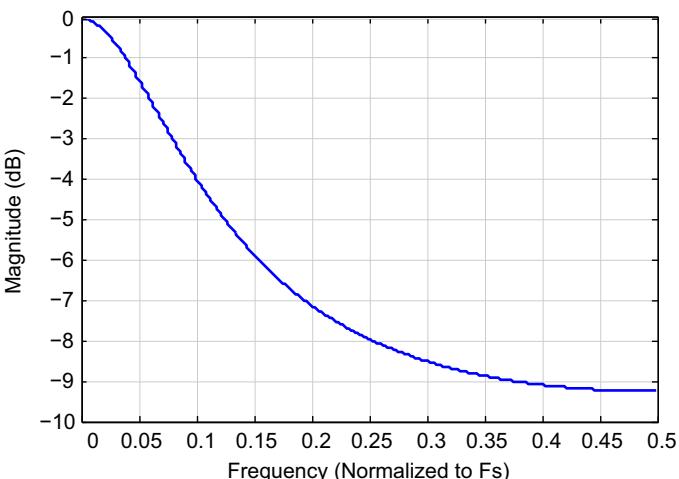


Figure 9-71. Deemphasis

9.1.14 组合滤波器响应——DSD

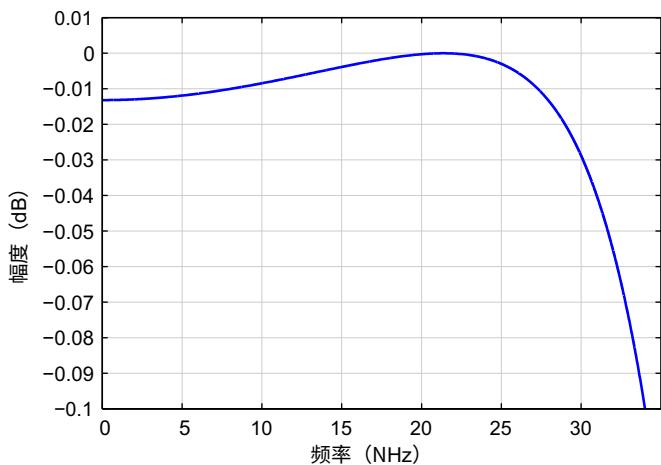


图 9-66 通带波纹

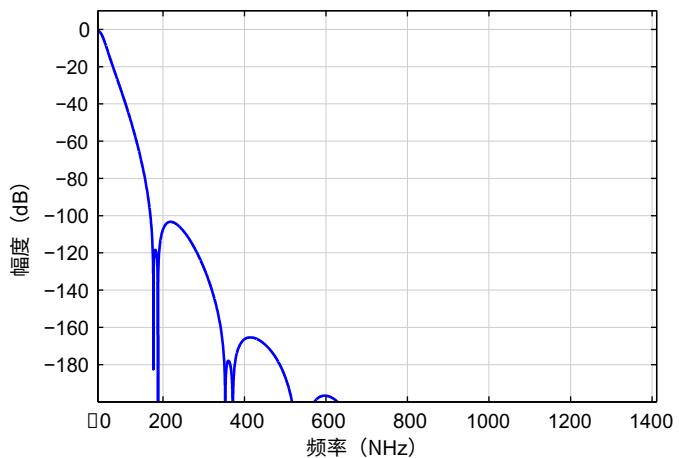


图 9-67 阻带衰减

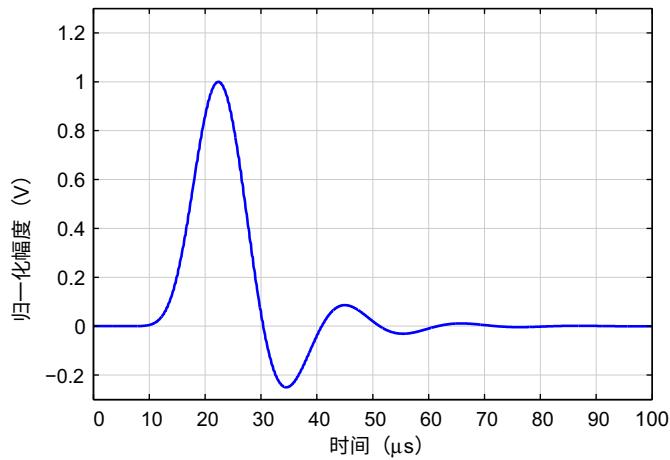


图 9-68 脉冲响应

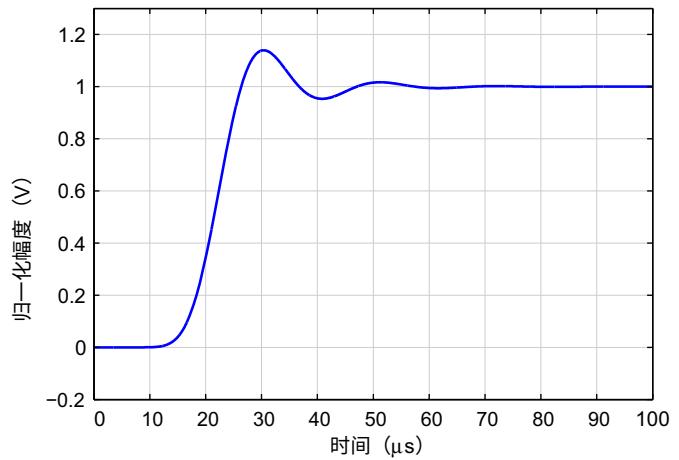


图 9-69 阶跃响应

9.1.15 高通滤波器与预加重

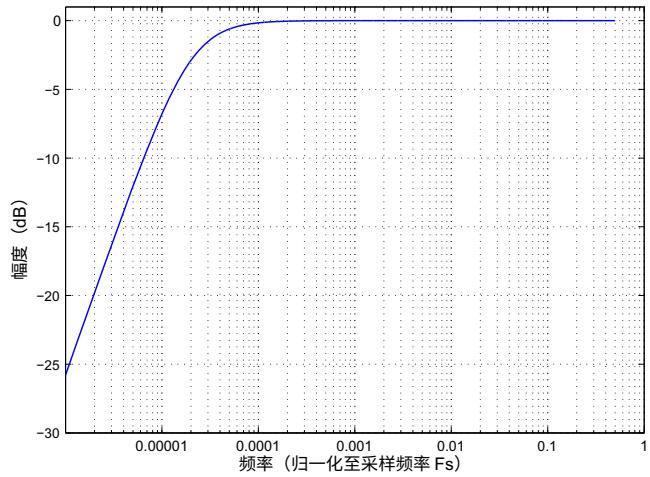


图 9-70。PCM 和 DSD 路径的高通滤波器

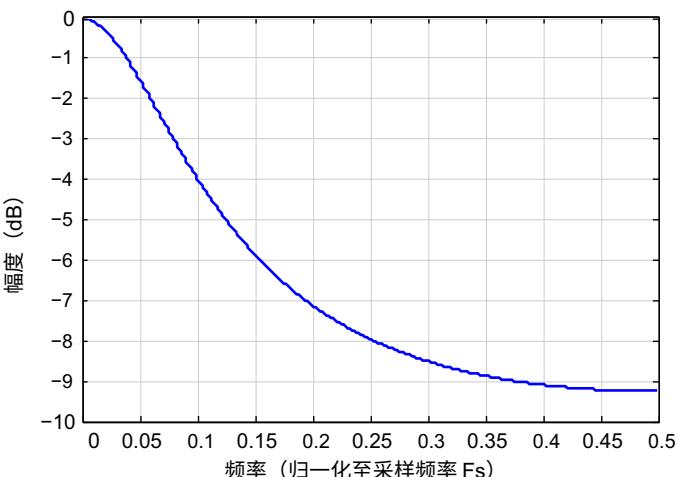


图 9-71。预加重

10 Package Dimensions

10.1 40-Pin QFN Package Dimensions

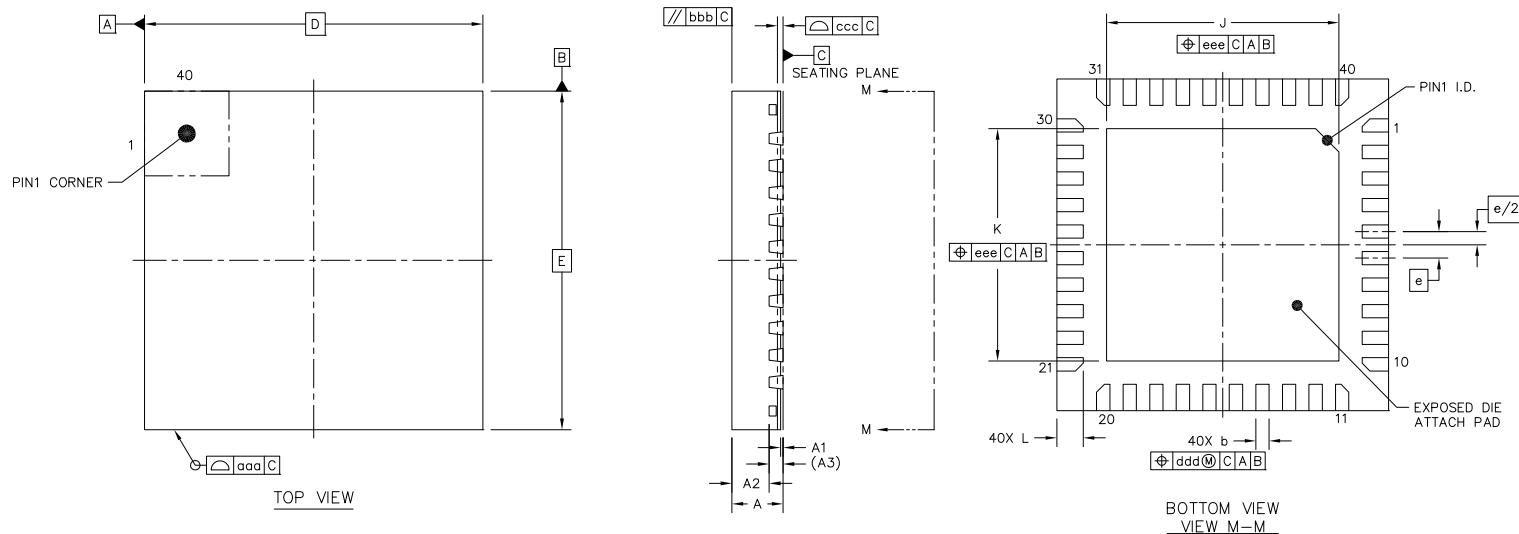


Figure 10-1. 40-Pin QFN Package Drawing

Table 10-1. 40-Pin QFN Package Dimensions

Description		Dim	Millimeters		
			Minimum	Nominal	Maximum
Total thickness		A	0.7	0.75	0.8
Stand off		A1	0	0.035	0.05
Mold thickness		A2	—	0.55	—
L/F thickness		A3		0.203 REF	
Lead width		b	0.15	0.2	0.25
Body size	X	D		5 BSC	
	Y	E		5 BSC	
Lead pitch		e		0.4 BSC	
EP size	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
Lead length		L	0.35	0.4	0.45
Package edge tolerance		aaa		0.1	
Mold flatness		bbb		0.1	
Coplanarity		ccc		0.08	
Lead offset		ddd		0.1	
Exposed pad offset		eee		0.1	

Notes:

- Dimensioning and tolerances per ASME Y 14.5M–1995.
- X/Y Dimensions are estimates.
- The Ball 1 location indicator shown above is for illustration purposes only and may not be to scale.
- Dimensioning and tolerances per ASME Y 14.5M–1994.
- Dimension “b” applies to the solder sphere diameter and is measured at the midpoint between the package body and the seating plane.

10 封装尺寸

10.1 40 引脚 QFN 封装尺寸

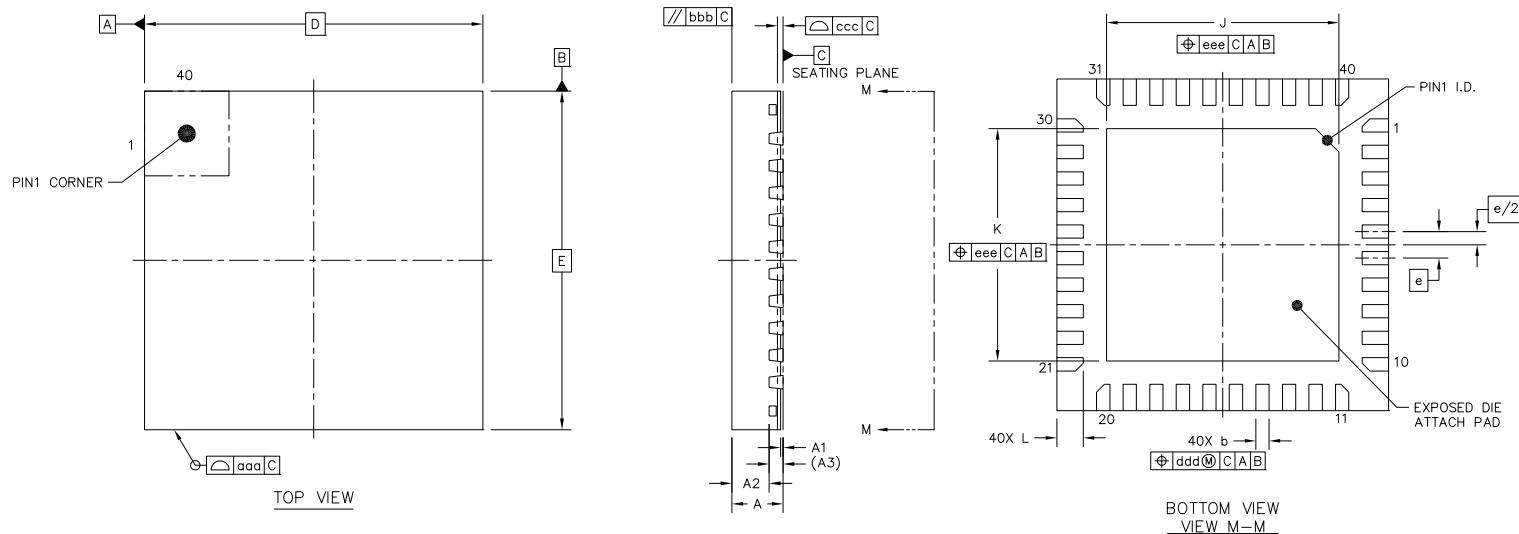


图 10-1。40 引脚 QFN 封装图

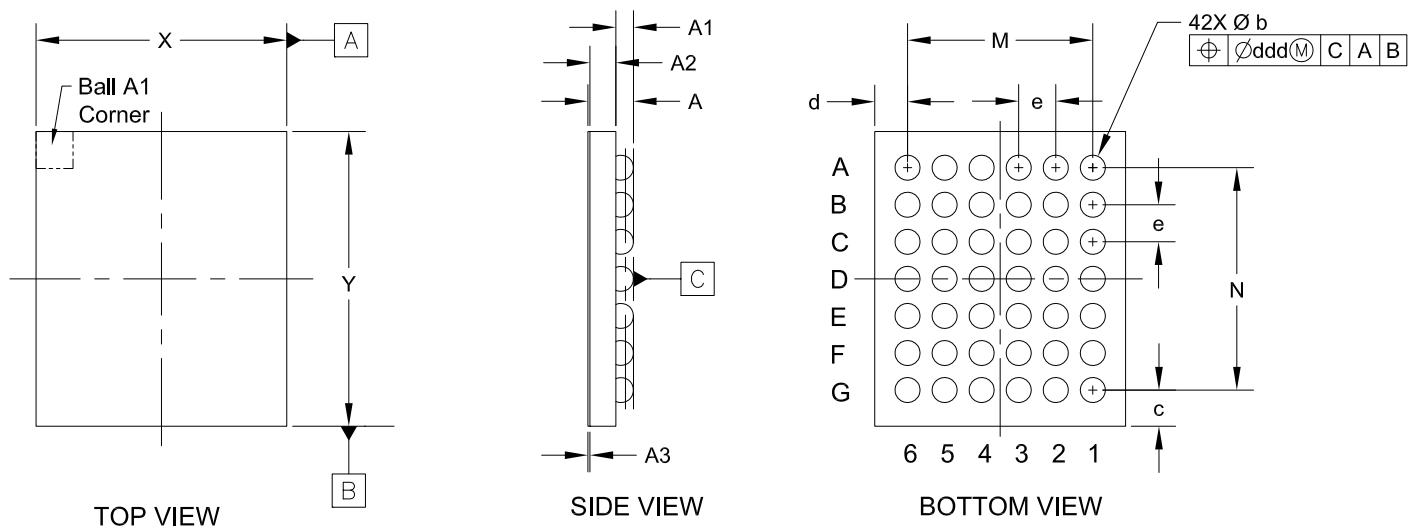
表 10-1。40 引脚 QFN 封装尺寸

描述	尺寸	毫米		
		最小值	标称值	最大值
总厚度	A	0.7	0.75	0.8
支撑高度	A1	0	0.035	0.05
模塑层厚度	A2	—	0.55	—
引脚/焊盘厚度	A3	0.203 参考		
引脚宽度	b	0.15	0.2	0.25
封装尺寸	X	D	5 BSC	
	Y	E	5 BSC	
引脚间距	e	0.4 BSC		
焊盘尺寸	X	J	3.4	3.5
	Y	K	3.4	3.5
引脚长度	L	0.35	0.4	0.45
封装边缘公差	aaa	0.1		
模具平整度	bbb	0.1		
共面度	ccc	0.08		
引脚偏移	ddd	0.1		
外露焊盘偏移	eee	0.1		

注释：

- 尺寸和公差依据 ASME Y14.5M-1995。
- X/Y 尺寸为估算值。
- 上述球1位置指示仅为示意，可能不按比例绘制。
- 尺寸和公差依据 ASME Y14.5M-1994。
- 尺寸“b”适用于焊球直径，测量位置为封装体与基准面之间的中点。

10.2 42-Ball WLCSP Package Dimensions



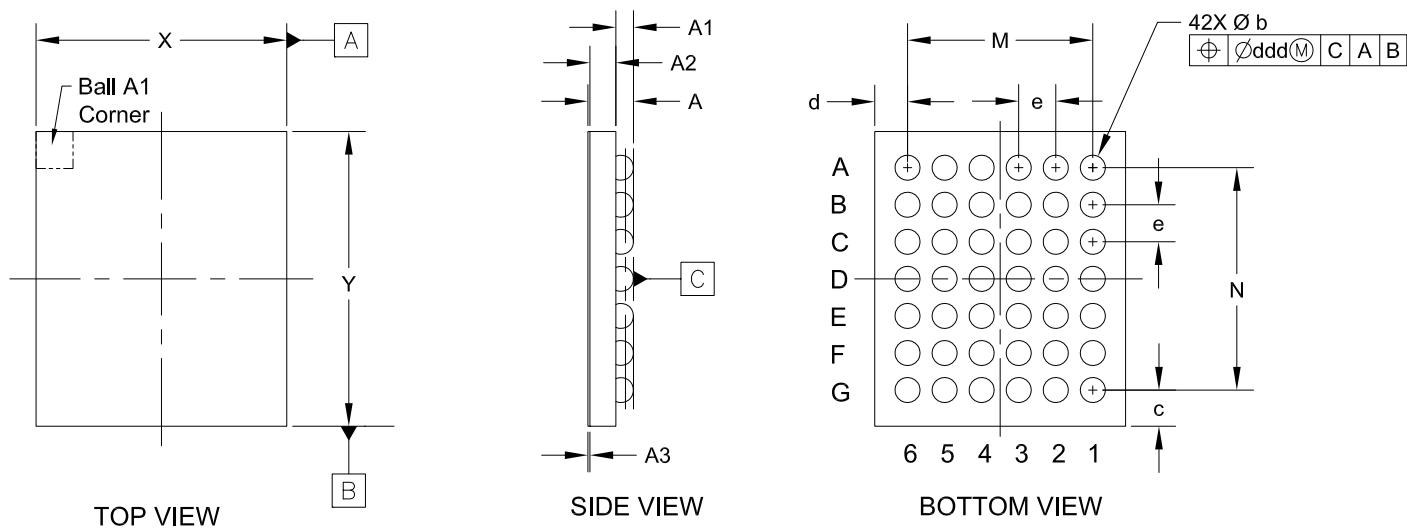
Dimension	Millimeters		
	Minimum	Nominal	Maximum
A	0.461	0.491	0.521
A1	0.175	0.19	0.205
A2	0.264	0.279	0.294
A3	REF	0.022	REF
b	0.24	0.27	0.3
c	0.3658	0.3908	0.4158
d	0.3286	0.3536	0.3786
e	BSC	0.4	BSC
M	BSC	2	BSC
N	BSC	2.4	BSC
X	2.6822	2.7072	2.7322
Y	3.1566	3.1816	3.2066
ddd=0.015			

Notes: Controlling dimension is millimeters.

Dimensioning and tolerances per ASME Y 14.5-2009. The Ball A1 position indicator is for illustration purposes only and may not be to scale.

Dimension "b" applies to the solder sphere diameter and is measured at the maximum solder sphere diameter, parallel to primary Datum C.

10.2 42 球 WLCSP 封装尺寸



Dimension	Millimeters		
	Minimum	Nominal	Maximum
A	0.461	0.491	0.521
A1	0.175	0.19	0.205
A2	0.264	0.279	0.294
A3	REF	0.022	REF
b	0.24	0.27	0.3
c	0.3658	0.3908	0.4158
d	0.3286	0.3536	0.3786
e	BSC	0.4	BSC
M	BSC	2	BSC
N	BSC	2.4	BSC
X	2.6822	2.7072	2.7322
Y	3.1566	3.1816	3.2066
ddd=0.015			

Notes: Controlling dimension is millimeters.

Dimensioning and tolerances per ASME Y 14.5-2009. The Ball A1 position indicator is for illustration purposes only and may not be to scale.

Dimension "b" applies to the solder sphere diameter and is measured at the maximum solder sphere diameter, parallel to primary Datum C.

11 Thermal Characteristics

Table 11-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter	Symbol	WLCSP	QFN	Units
Junction-to-ambient thermal resistance	θ_{JA}	42.3	32.7	°C/W
Junction-to-board thermal resistance	θ_{JB}	11.1	8.8	°C/W
Junction-to-case thermal resistance	θ_{JC}	0.22	0.92	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	11.0	8.8	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	0.09	0.23	°C/W

Notes:

- Natural convection at the maximum recommended operating temperature T_A (see [Table 3-2](#))
- Four-layer, 2s2p PCB as specified by JESD51-9 and JESD51-11; dimensions: 101.5 x 114.5 x 1.6 mm
- Thermal parameters as defined by JESD51-12

12 Ordering Information

Table 12-1. Ordering Information 1

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Order Number
CS43131	130-dB, 32-Bit High-Performance DAC with Integrated Headphone Driver and Impedance Detection	42-ball WLCSP	Yes	Commercial	−20°C to +70°C	Tape and Reel	CS43131-CWZR
		40-pin QFN	Yes	Commercial	−20°C to +70°C	Tray	CS43131-CNZ
						Tape and Reel	CS43131-CNZR

1. The Revision ID fields in [Section 7.1.4, “Revision ID,”](#) list the alpha (AREVID) and metal (MTLREVID) revisions.

13 References

- NXP Semiconductors, *The I²C-Bus Specification and User Manual (UM10204)*. <http://www.nxp.com/>

14 Revision History

Table 14-1. Revision History

Revision	Changes
F1 OCT 2017	Initial release
F2 DEC 2022	Updated reset values for Interrupt Mask 2 register Updated Ambient Temperature Minimum in Table 3-2 Recommended Operating Conditions from −10°C to −20°C Updated Temperature Range in Table 12-1 Ordering Information from −10°C to −20°C

Important: Please check with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

11 热特性

表 11-1。典型 JEDEC 四层 2s2p 电路板热特性

参数	符号	WLCSP	QFN	单位
结点至环境热阻	θ_{JA}	42.3	32.7	°C/W
结点至电路板热阻	θ_{JB}	11.1	8.8	°C/W
结点至封装热阻	θ_{JC}	0.22	0.92	°C/W
结点至电路板热特性参数	Ψ_{JB}	11.0	8.8	°C/W
结点至封装顶部热特性参数	Ψ_{JT}	0.09	0.23	°C/W

注释：

- 在最大推荐工作温度 T_A 下的自然对流（见表 3-2）
- 四层 2s2p PCB，符合 JESD51-9 和 JESD51-11 规范；尺寸：101.5 x 114.5 x 1.6 毫米
- 热参数依据 JESD51-12 定义。

12 订购信息

表 12-1。订购信息 1

产品	描述	封装	符合RoHS要求	等级	温度范围	包装容器	订单号
CS43131	130 dB、32 位高性能数模转换器，集成耳机驱动器及阻抗检测系统	42球 WLCSP	是	商业级	-20°C 至 +70°C	卷带包装	CS43131-CWZR
		40引脚 QFN	是	商业级	-20°C 至 +70°C	托盘	CS43131-CNZ
						卷带包装	CS43131-CNZR

1. 第 7.1.4 节“修订 ID”中列出了字母 (AREVID) 和金属 (MTLREVID) 修订版本。

13 参考文献

- 恩智浦半导体, I2C 总线规范及用户手册 (UM10204) 。<http://www.nxp.com/>

14 修订历史

表 14-1 修订历史

修订版	变更内容
F1 2017年10月	初始发布
F2 2022年12月	更新中断屏蔽寄存器2的复位值 表 3-2 推荐操作条件中环境温度最低值已由 -10°C 更新为 -20°C 表 12-1 订购信息中的温度范围已由 -10°C 更新为 -20°C

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