



# Raspberry Pi Compute Module 5

A Raspberry Pi for deeply embedded  
applications



# 树莓派 计算模块 5

## 针对深度嵌入式应用的树莓派

# Colophon

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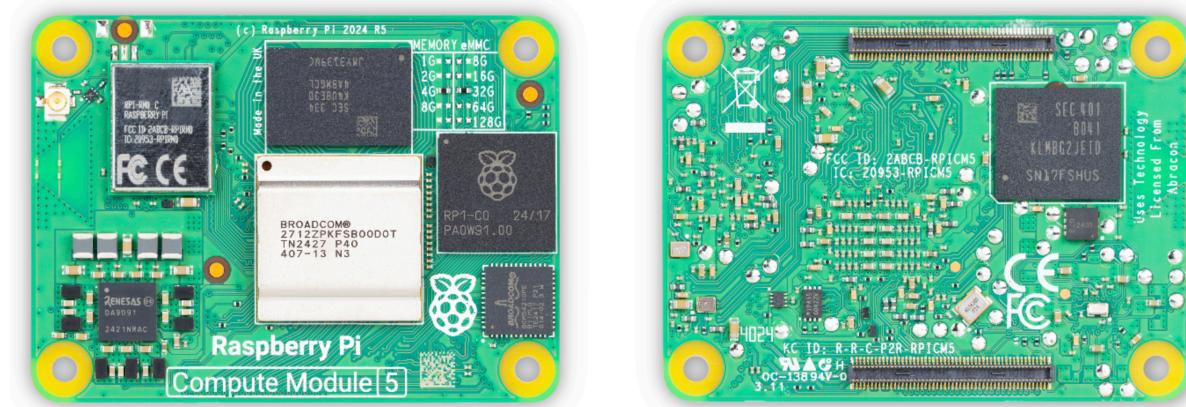
# 1. Introduction

**Raspberry Pi Compute Module 5 (CM5)** is a System on Module (SoM) designed to deliver the functionality of Raspberry Pi in a compact and flexible form factor suited to embedded and industrial applications. It enables developers and system designers to leverage the Raspberry Pi hardware and software stack in their own custom systems and designs.

CM5 includes a processor, memory (RAM), eMMC flash storage, and supporting power circuitry. It also provides I/O interfaces beyond those available on standard Raspberry Pi boards, offering expanded options for more complex systems and designs.

**Figure 1.**

The front (left) and back (right) of Raspberry Pi Compute Module 5 (CM5)



For support documentation for CM5, see the [Compute Module](#) section of <https://www.raspberrypi.com>. You can also post a question to the [Forum](#).

## 1.1. Connectors

CM5 includes two 100-pin high-density connectors, providing access to nearly all CM5 interfaces. Together, these connectors transmit power, data, and control signals to a carrier board. The top connector on CM5 contains pins 1 to 100; the bottom connector of CM5 contains pins 101 to 200. For information about each pin's assignment, see [Section 4.2. Pinout](#).

CM5 has a companion carrier board, the Raspberry Pi Compute Module 5 IO Board (CM5IO) board, which is designed to expose and enable CM5 interfaces. You can also design your own carrier board based on the CM5IO board. The CM5IO design files are freely available. For detailed specifications and pinout information about CM5IO, see the [Compute Module 5 IO board documentation](#).

## 1.2. Compatibility

CM5 and CM5Lite are mostly compatible with the previous generation of Compute Module. This means that CM5 can be used in many existing designs and carrier boards with minimal changes. For a list of specific differences between CM5 and CM4, see [Appendix B. CM4 and CM5 differences](#).

### Note

The previous generation of Compute Module (CM4) is still for sale and will remain in production until at least January 2034.

CM5 connects to carrier boards through its two 100-pin connectors. The main change in the pin layout (pinout) compared to the previous Compute Module is the addition of support for two USB 3.0 ports. For a list of pin differences between CM5 and CM4, see [Appendix B.1. Pinout changes](#).

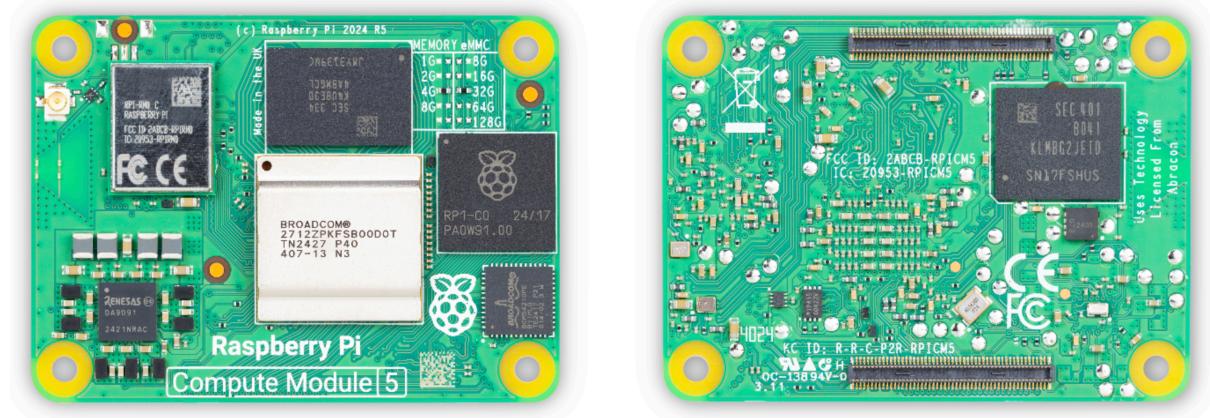
# 1. 介绍

**树莓派计算模块 5 (CM5)** 是一款系统模块 (SoM)，旨在以紧凑灵活的形态提供树莓派的功能，适用于嵌入式和工业应用。它使开发人员和系统设计师能够在自定义系统和设计中利用树莓派的硬件和软件堆栈。

CM5 包含处理器、内存 (RAM)、eMMC 闪存存储及辅助电源电路。它还提供了超出标准树莓派主板所具备的 I/O 接口，拓展了更复杂系统和设计的选择。

图 1。

树莓派计算模块 5 (CM5) 的正面 (左) 及背面 (右)



有关 CM5 的支持文档，请参阅 <https://www.raspberrypi.com> 的计算模块部分。您也可在论坛发帖提问。

## 1.1. 连接器

CM5 配备两个 100 引脚高密度连接器，可访问几乎所有 CM5 接口。这些连接器将电源、数据和控制信号传输至载板。CM5顶部连接器包含引脚1至100；CM5底部连接器包含引脚101至200。有关每个引脚的分配信息，请参见第4.2节 引脚分配。

CM5配备了配套载板——树莓派计算模块5 IO板 (CM5IO)，该板设计用于暴露并启用CM5的接口。您也可以基于CM5IO设计您自己的载板。CM5IO的设计文件可免费获取。有关CM5IO的详细规格和引脚分配信息，请参见计算模块5 IO板文档。

## 1.2. 兼容性

CM5和CM5Lite在很大程度上与上一代计算模块兼容，这意味着CM5可在许多现有设计和载板中仅需极少改动即可使用。有关CM5与CM4之间具体差异的列表，请参见附录B CM4与CM5的差异。

### 注意

上一代计算模块 (CM4) 仍在销售，且将至少持续生产至2034年1月。

CM5 通过其两个100针连接器连接到载板。相比之前的计算模块，引脚布局（引脚分配）的主要变化是增加了对两个USB 3.0端口的支持。关于CM5与CM4之间引脚差异的详细列表，请参见附录B.1 “引脚分配变更”。

## 1.3. Features

The design of CM5 is loosely based on Raspberry Pi 5. For cost-sensitive applications, CM5 is also available without the eMMC storage; this variant is called Raspberry Pi Compute Module 5 Lite (CM5Lite). Unless otherwise stated, within this document, CM5 also refers to CM5Lite.

Key features of CM5 are as follows:

- **High-performance SoC.** Broadcom BCM2712 quad-core Cortex-A76 (ARMv8) 64-bit processor running at 2.4 GHz.
- **Compact module design.** Small footprint of 55 mm × 40 mm × 4.7 mm module with four M2.5 mounting holes.
- **Video decoding.** Hardware-accelerated 4Kp60 HEVC video decoder.
- **Graphics support.** OpenGL ES 3.1 and Vulkan 1.2 for modern GPU acceleration.
- **Memory options.** Available with 2 GB, 4 GB, 8 GB, or 16 GB LPDDR4x-4267 SDRAM with ECC support. For more information about memory options, see [Section 6. Ordering information](#).
- **Flash storage.** Fast onboard eMMC flash storage with the following options:
  - **Speed.** An eMMC bandwidth of up to 400 MB/s, which is four times faster than previous compute modules.
  - **Storage.** Options for 16 GB, 32 GB, or 64 GB eMMC flash memory (for CM5), or no eMMC flash memory (CM5Lite). For more information about storage options, see [Section 6. Ordering information](#).
- **Additional SDIO interface for CM5Lite.** One SDIO 2.0 interface to provide external storage or peripheral expansion in place of onboard eMMC (CM5Lite only).
- **Optional certified wireless module.** Option (see [Section 6. Ordering information](#)) for certified radio module with:
  - Dual-band Wi-Fi (2.4 GHz and 5.0 GHz IEEE 802.11 b/g/n/ac).
  - Bluetooth 5.0 with BLE.
  - On-board electronic antenna switch that allows selection between PCB trace or external antenna.
- **Wired networking.** Integrated Gigabit Ethernet PHY with IEEE 1588 precision time protocol support.
- **PCIe expansion.** One-lane PCIe Gen 2 (5 Gb/s) host interface for high-speed peripherals.
- **USB connectivity.** USB options for both High-Speed and SuperSpeed peripherals:
  - One USB 2.0 high-speed port.
  - Two USB 3.0 (SuperSpeed) ports, supporting simultaneous 5 Gb/s data transfer.
- **Flexible GPIO and peripheral support.** Up to 30 GPIOs, supporting 1.8 V or 3.3 V signalling, with multiple peripheral interfaces:
  - Up to five UART
  - Up to five I2C
  - Up to five SPI
  - One SDIO interface
  - One DPI (parallel RGB display)
  - One I2S
  - Up to four PWM channels
  - Up to three GPCCLK outputs
- **Dual HDMI outputs.** Two HDMI 2.0 ports, each supporting up to 4Kp60 output simultaneously.
- **Dual 4-lane MIPI interfaces.** Two MIPI ports supporting both DSI (display port) and CSI-2 (camera port) functionality.
- **Power input.** Single 5 V power input with USB power delivery support for up to 5 A at 5 V.
- **Real-time clock (RTC).** Integrated RTC powered by an external battery for timekeeping when offline.
- **Fan control.** Dedicated 2-pin fan control with PWM for active thermal management.

## 1.3. 特性

CM5的设计部分基于树莓派5。针对成本敏感的应用场景，CM5也提供无eMMC存储的版本；该版本称为树莓派计算模块5 Lite（CM5Lite）。除非另有说明，本文件中“CM5”亦指CM5Lite。

CM5的主要特性如下：

- **高性能SoC。**采用Broadcom BCM2712 四核Cortex-A76（ARMv8）64位处理器，主频2.4 GHz。
- **紧凑的模块设计。**模块尺寸紧凑，大小为55 mm × 40 mm × 4.7 mm，配备四个M.2.5安装孔。
- **视频解码。**硬件加速的4Kp60 HEVC视频解码器。
- **图形支持。**支持OpenGL ES 3.1与Vulkan 1.2，实现现代GPU加速。
- **内存选项。**提供2 GB、4 GB、8 GB或16 GB带ECC支持的LPDDR4x-4267 SDRAM。有关内存选项的详细信息，请参见第6节订购信息。
- **闪存存储。**快速板载eMMC闪存存储，具备以下选项：
  - 速度。eMMC带宽高达400 MB/s，是之前计算模块的四倍。
  - 存储。提供16 GB、32 GB或64 GB eMMC闪存存储（适用于CM5），或无eMMC闪存存储（CM5Lite）。有关存储选项的详细信息，请参见第6节订购信息。
- **CM5Lite的额外SDIO接口。**提供一个SDIO 2.0接口，替代板载eMMC，实现外部存储或外围扩展（仅限CM5Lite）。
- **可选认证无线模块。**选项（详见第6节订购信息），提供认证无线电模块，具备：
  - 双频Wi-Fi（2.4 GHz和5.0 GHz，符合IEEE 802.11 b/g/n/ac标准）。
  - 蓝牙5.0及BLE支持。
  - 板载电子天线开关，可选择印刷电路板导线或外接天线。
- **有线网络。**集成千兆以太网PHY，支持IEEE 1588精确时间协议（PTP）。
- **PCIe扩展。**单通道PCIe代2（5 Gb/s）主机接口，支持高速外设。
- **USB连接。**USB接口，支持高速及超级速度外设：
  - 一个USB 2.0高速端口。
  - 两个USB 3.0（超级速度）端口，支持同步5 Gb/s数据传输。
- **灵活的GPIO及外设支持。**最多30个GPIO，支持1.8 V或3.3 V信号，多种外设接口：
  - 支持最多五个UART接口
  - 支持最多五个I2C接口
  - 支持最多五个SPI接口
  - 一个SDIO接口
  - 一个DPI（并行RGB显示）接口
  - 一个I2S接口
  - 支持最多四个PWM通道
  - 支持最多三个GPCLK输出
- **双HDMI输出。**两个HDMI 2.0端口，均支持同时输出4Kp60视频信号。
- **双4通道MIPI接口。**两个MIPI端口，支持DSI（显示接口）和CSI-2（摄像头接口）功能。
- **电源输入。**单个5 V电源输入，支持USB供电，可提供最高5 V 5 A电流。
- **实时时钟（RTC）。**集成实时时钟，由外部电池供电，确保离线时的时间保持。
- **风扇控制。**专用2针风扇控制接口，支持PWM，用于主动热管理。

# 2. Interfaces

CM5 includes a range of interfaces (physical connectors, control signals, and configuration mechanisms) to support diverse applications, from high-speed storage and networking to wireless communication, display outputs, and flexible GPIO expansion. These interfaces allow you to build connected and adaptable embedded systems. The following sections provide technical information on each available interface, including configuration options, routing guidelines, and design considerations.

## 2.1. Wireless

CM5 supports both Wi-Fi and Bluetooth functionality, allowing developers and system designers to flexibly manage wireless connectivity for a range of applications.

The wireless interfaces on CM5 are provided by the Cypress CYW43455 silicon, supporting both:

- 2.4 GHz and 5.0 GHz IEEE 802.11 b/g/n/ac Wi-Fi.
- Bluetooth 5.0 and BLE.

You can enable and disable these wireless functions independently as required. For example, in kiosk deployments, a service engineer might temporarily enable wireless to perform updates, then disable it for security and regulatory compliance.

CM5 has an on-board PCB antenna that should be positioned away from conductive materials, such as metal or ground planes. For more information, see [Section 4. Specifications](#). Alternatively, you can connect an external antenna through a standard U.FL connector. For the location of the connector, see the [CM5 mechanical diagram](#) in [Section 4.1.1. PCB dimensions](#).

Antenna selection (internal or external) is configured at boot time using the `config.txt` file. This selection can't be changed during operation. To select the antenna, append one of the following lines to `config.txt`:

- `dtparam=ant1` selects the internal PCB antenna.
- `dtparam=ant2` selects the external antenna through a U.FL connector.

Raspberry Pi Ltd offers a certified antenna kit for use with CM5. If you use a third-party antenna, you must obtain your own separate certification because Raspberry Pi Ltd doesn't support certification with non-approved antennas.

### Important

Raspberry Pi Ltd doesn't assist with certification for third-party antennas.

To support power savings and regulatory usage requirements, two control pins, wireless (Wi-Fi) disable (`WL_nDisable`) and Bluetooth disable (`BT_nDisable`), allow hardware-level shut down of Wi-Fi and Bluetooth, respectively. These pins are reserved on Compute Modules without wireless functionality.

### 2.1.1. Wi-Fi disable ( `WL_nDisable` )

The `WL_nDisable` pin indicates the enable/disable state of Wi-Fi and may also be used to disable Wi-Fi. This pin may only be driven low; it can't be driven high. The software driver drives it high internally when required.

- If the pin is high (logic 1), Wi-Fi is powered up. If Wi-Fi is enabled after being disabled, you must reinitialise the Wi-Fi driver.
- When driven or tied low (logic 0), the pin prevents Wi-Fi from powering up, helping to reduce power consumption or meet requirements to physically disable Wi-Fi.

### 2.1.2. Bluetooth disable ( `BT_nDisable` )

The `BT_nDisable` pin indicates the enable/disable state of Bluetooth and may also be used to disable Bluetooth. This pin may only be driven low; it can't be driven high. The software driver drives it high internally when required.

- If the pin is high (logic 1), Bluetooth is powered up. If Bluetooth is enabled after being disabled, you must reinitialise the Bluetooth driver.
- When driven or tied low (logic 0), the pin prevents Bluetooth from powering up, helping to reduce power consumption or meet requirements to physically disable Bluetooth.

## 2. 接口

CM5包含一系列接口（物理连接器、控制信号及配置机制），支持从高速存储和网络通信到无线通信、显示输出及灵活GPIO扩展的多种应用。这些接口使您能够构建互联且可适应的嵌入式系统。以下各节提供每个可用接口的技术信息，包括配置选项、布线指导和设计注意事项。

### 2.1. 无线

CM5支持Wi-Fi和蓝牙功能，允许开发人员和系统设计者灵活管理多种应用的无线连接。

CM5上的无线接口由Cypress CYW43455芯片提供，支持以下功能：

- 2.4 GHz和5.0 GHz IEEE 802.11 b/g/n/ac Wi-Fi。
- 蓝牙5.0和低功耗蓝牙（BLE）。

您可以根据需求独立启用或禁用这些无线功能。例如，在自助终端部署中，服务工程师可能暂时启用无线以进行更新，随后为了安全和法规合规而禁用。

CM5配备了板载印刷电路板天线，应远离导电材料，如金属或地线平面。

详情请参见第4节 规格说明。或者，您也可以通过标准 U.FL 连接器连接外部天线。连接器的位置请参阅第4.1.1节 CM5机械图，印刷电路板尺寸。

天线选择（内部或外部）在启动时通过

要选择天线，请在

`config.txt`文件进行配置。该选择无法在运行时更改

`config.txt` 文件中添加以下任一行：

- `dtparam=ant1` 选择内部印刷电路板天线。
- `dtparam=ant2` 选择通过 U.FL 连接器连接的外部天线。

树莓派有限公司提供了官方认证的 CM5 天线套件。如使用第三方天线，必须自行取得相应认证，因树莓派有限公司不支持使用未经批准的天线进行认证。

#### 重要

树莓派有限公司不提供第三方天线的认证支持。

为了支持节能和符合法规的使用要求，设有两个控制引脚，分别为无线（Wi-Fi）禁用（`WL_nDisable`）和蓝牙禁用（`BT_nDisable`），允许在硬件层面分别关闭 Wi-Fi 和蓝牙功能。对于不具备无线功能的计算模块，这些引脚将被保留。

#### 2.1.1. Wi-Fi禁用（`WL_nDisable`）

该 `WL_nDisable`引脚指示 Wi-Fi 的启用/禁用状态，也可用于禁用 Wi-Fi。此引脚仅能被拉低；不能被拉高。软件驱动程序在需要时会在内部将其拉高。

- 当引脚为高电平（逻辑1）时，Wi-Fi 通电。如 Wi-Fi 在被禁用后重新启用，必须重新初始化 Wi-Fi 驱动程序。
- 当引脚被拉低或接地（逻辑0）时，此引脚阻止 Wi-Fi 通电，有助于降低功耗或满足物理禁用 Wi-Fi 的要求。

#### 2.1.2. 蓝牙禁用（`BT_nDisable`）

该 `BT_nDisable`引脚指示蓝牙的启用/禁用状态，也可用于禁用蓝牙。此引脚仅能被拉低；不能被拉高。软件驱动程序在需要时会在内部将其拉高。

- 如果引脚为高电平（逻辑1），蓝牙处于通电状态。当蓝牙在被禁用后重新启用时，必须重新初始化蓝牙驱动程序。
- 当引脚被驱动或接地为低电平（逻辑0）时，将阻止蓝牙上电，有助于降低功耗或满足物理禁用蓝牙的要求。

## 2.2. Ethernet

Ethernet capabilities in CM5 provide reliable, high-throughput wired connectivity for applications requiring consistent network performance or time-synchronised operation. CM5 integrates a Gigabit Ethernet physical layer (PHY) device to provide high-performance, reliable wired networking: the Broadcom [BCM54210PE](#). Key features of this PHY include:

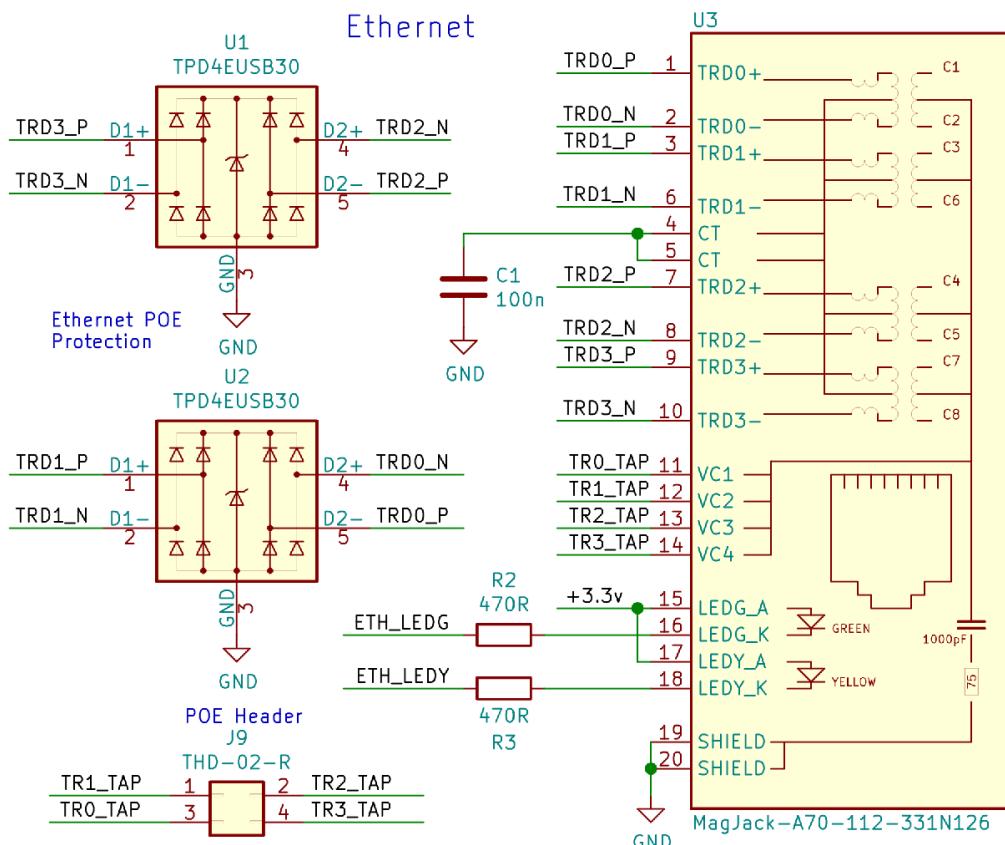
- Compliance with [IEEE 1588-2008](#) for PTP support, with an additional pin that can be an input or output.
- Automatic MDI crossover, pair skew correction, and pair polarity correction.

### 2.2.1. Connector and design guidance

Ethernet connects to CM5 using a standard 1:1 RJ45 MagJack. For designs supporting Power over Ethernet (PoE) and Electrostatic Discharge (ESD) protection, refer to the wiring example shown in [Figure 2](#).

**Figure 2.**

*Ethernet schematic interface for Raspberry Pi Compute Module 5 (CM5) supporting PoE, with added ESD protection*



Route the differential Ethernet signals as  $100\ \Omega$  differential pairs with appropriate spacing and clearances. Length matching between different pairs is generally not required if differences are less than 50 mm. However, the signals within each pair need to be length matched for optimal signal integrity, ideally within 0.15 mm.

### 2.2.2. Status LEDs and sync output

The Ethernet interface also supports up to two active-low LEDs to give status feedback. These LEDs can indicate various Ethernet link or activity states depending on operating system (OS) and driver support. To see which LED functions are supported, consult the Ethernet driver documentation for your OS.

The Ethernet interface also provides `SYNC_OUT` at 3.3 V signalling, supporting [IEEE 1588-2008](#) PTP. This pin can be optionally defined as an input.

## 2.2. 以太网

CM5 的以太网功能为需要稳定网络性能或时间同步操作的应用提供可靠的高吞吐量有线连接。CM5 集成了一款千兆以太网物理层 (PHY) 设备 Broadcom BCM54210PE，提供高性能、可靠的有线网络连接。该 PHY 的主要特性包括：

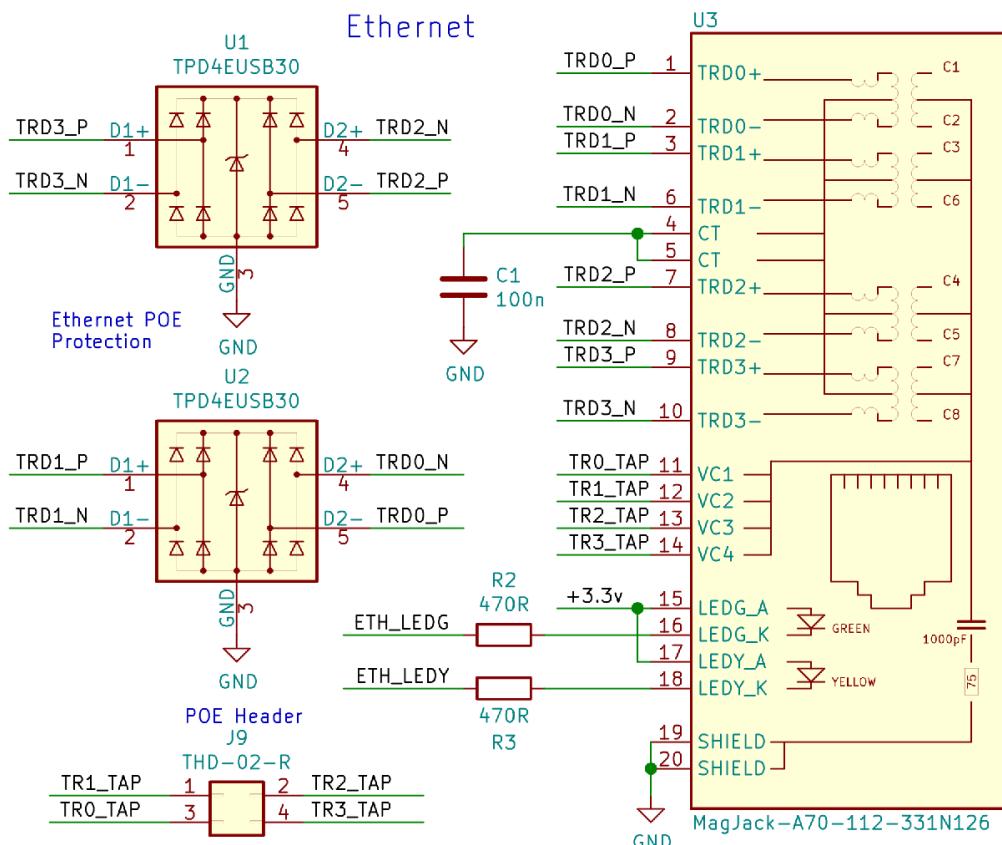
- 符合 IEEE 1588-2008 标准，支持 PTP，并配备一个可用作输入或输出的附加引脚。
- 支持自动 MDI 交叉、线对延迟校正及线对极性校正。

### 2.2.1. 连接器及设计指导

以太网通过标准 1:1 RJ45 MagJack 连接至 CM5。对于支持以太网供电 (PoE) 和静电放电 (ESD) 保护的设计，请参阅图 2 所示的接线示例。

图 2。

支持 PoE 并带额外 ESD 保护的树莓派计算模块 5 (CM5) 以太网接口原理图



将差分以太网信号布线为  $100\Omega$  差分对，保持适当的间距和净空。如果差异小于 50 毫米，不同对之间通常无需长度匹配。但每对内部信号需进行长度匹配以实现最佳信号完整性，理想差异不超过 0.15 毫米。

### 2.2.2. 状态指示灯和同步输出

以太网接口还支持最多两个低电平有效的 LED 用于状态反馈。这些 LED 可根据操作系统 (OS) 和驱动程序支持，指示各种以太网链路或活动状态。欲了解支持的 LED 功能，请查阅所用操作系统的以太网驱动文档。

以太网接口还提供  
定义为输入。

`SYNC_OUT` 采用 3.3 V 信号电平，支持 IEEE 1588-2008 PTP。该引脚可选定义为输入。

## 2.3. PCIe Gen 2

CM5 has an internal PCIe 2.0 host controller, offering high-speed expansion options for NVMe storage, networking cards, and other peripherals. Operation in PCIe Gen 3.0 mode is possible in some cases, but is unsupported and might not function reliably.

### Important

Ensure suitable OS driver support exists for your intended PCIe device (host controller) before prototyping.

Connecting a PCIe device follows the standard PCIe convention. CM5 includes on-board AC coupling capacitors for the `PCIe_TX` signals. However, external AC coupling capacitors are required for `PCIe_RX` signals, close to the driving source (the peripheral's `TX`). PCIe and NVMe cards include these capacitors on board.

To ensure reliable PCIe operation, follow the electrical routing guidance and connect all mandatory control signals outlined below.

### 2.3.1. Routing guidance

When designing with PCIe on CM5, observe the following conventions for signal routing and connection:

- **Direct IC connection.** If connecting directly to another IC, swap the transmit (TX) and receive (RX) differential pairs; this involves connecting TX to RX and RX to TX. Ensure each receive (`PCIe-Rx`) line has an AC coupling capacitor (220 nF) before it enters the IC.
- **Connector-based connection.** If using a PCIe connector, the signals are labelled from the host's point of view, so TX and RX lines don't need to be swapped.

PCIe differential signals should be routed as 90 Ω differential pairs with proper clearances. Length matching between pairs is unnecessary, but the signals within a pair must be length-matched, ideally within 0.1 mm, to preserve signal integrity. You may swap the positive (P) and negative (N) line within a pair.

### 2.3.2. Required signals

The following control and clock signals must be handled correctly for proper PCIe operation:

- `PCIe_CLK_nREQ` must be connected to enable clock output from CM5.
- `PCIe_nRST` is required for proper device reset during initialisation or reboot.
- `PCIe_nWAKE` is available, but currently unsupported in software.

## 2.4. USB interfaces

CM5 provides support for both USB 3.0 (SuperSpeed) and USB 2.0 (High-Speed) interfaces. Both USB 3.0 and USB 2.0 require 90 Ω differential impedance, with length matching within each pair. You may swap the positive (P) and negative (N) signals for USB 3.0 pairs; USB 2.0 pairs can't be P/N swapped.

### 2.4.1. USB 3.0 (SuperSpeed)

CM5 includes two USB 3.0 interfaces, each supporting up to 5 Gb/s signalling simultaneously. The USB differential pairs should be routed with 90 Ω differential impedance. Length matching between separate pairs is unnecessary, but the P and N signals within each differential pair must be length-matched, ideally within 0.1 mm.

### Note

P/N signal swapping is allowed for USB 3.0 pairs.

### 2.4.2. USB 2.0 (High-Speed)

The USB 2.0 interface supports up to 480 Mb/s signalling. The differential pair should be routed with a 90 Ω differential impedance. The P and N signals within each differential pair should be length-matched, ideally within 0.15 mm.

To enable USB 2.0 functionality, add the `dtoverlay=dwc2,dr_mode=host` overlay setting to your `config.txt` file.

## 2.3. PCIe 代2

CM5 内置 PCIe 2.0 主机控制器，提供针对 NVMe 存储、网络卡及其他外设的高速扩展选项。某些情况下可运行于 PCIe 代 3.0 模式，但该模式不受支持，且可能无法稳定工作。

### 重要

在原型设计前，请确保您的目标 PCIe 设备（主机控制器）具备相应的操作系统驱动程序支持。

连接 PCIe 设备时，请遵循标准 PCIe 规范。CM5 板载有信号的交流耦合电容。

PCIe\_TX

信号。但对于 PCIe\_RX 信号，需要在靠近驱动源（外设的 TX）处加装外部交流耦合电容。PCIe 和 NVMe 卡均在板载集成了这些电容。

为确保 PCIe 可靠运行，请遵循电气布线建议，连接下述所有必需的控制信号。

### 2.3.1. 布线指导

在 CM5 上设计 PCIe 时，请遵守以下信号布线与连接规范：

- **直接 IC 连接。**如果直接连接至另一 IC，请交换发送 (TX) 和接收 (RX) 差分对；即将 TX 连接至 RX，RX 连接至 TX。确保每个接收 (PCIe-Rx) 线路在进入 IC 前配备一个交流耦合电容 (220 nF)。
- **基于连接器的连接。**使用 PCIe 连接器时，信号标签以主机视角标注，因此无需交换 TX 与 RX 线路。

PCIe 差分信号应以  $90\Omega$  差分对进行布线，并保持合适间隙。不需要差分对之间长度匹配，但对内信号必须长度匹配，理想误差不超过 0.1 毫米，以保证信号完整性。可在差分对内部交换正 (P) 与负 (N) 线。

### 2.3.2. 必需信号

为保证 PCIe 正确操作，以下控制和时钟信号必须妥善处理：

- PCIe\_CLK\_nREQ 必须连接以启用 CM5 的时钟输出。
- PCIe\_nRST 用于设备在初始化或重启期间的正确复位，必不可少。
- PCIe\_nWAKE 可用，但当前软件尚不支持。

## 2.4. USB 接口

CM5 支持 USB 3.0（超高速）和 USB 2.0（高速）接口。USB 3.0 和 USB 2.0 均要求  $90\Omega$  差分阻抗，且每对线内必须进行长度匹配。USB 3.0 信号对可交换正 (P) 负 (N) 信号；USB 2.0 信号对不可交换正负极。

### 2.4.1. USB 3.0 (SuperSpeed)

CM5 包含两个 USB 3.0 接口，每个接口均支持最高 5 Gb/s 的信号传输速率。USB 差分对应以  $90\Omega$  差分阻抗进行布线。不同信号对之间无需长度匹配，但每对差分信号的正负极必须长度匹配，理想控制在 0.1 mm 以内。

### 注意

USB 3.0 信号对允许正负极交换。

### 2.4.2. USB 2.0 (高速)

USB 2.0 接口支持高达 480 Mb/s 的信号传输速率。差分对应按照  $90\Omega$  差分阻抗进行布线。

每对差分信号中的 P 和 N 信号应长度匹配，理想误差在 0.15 mm 以内。

若需启用 USB 2.0 功能，请添加 `dtoverlay=dwc2,dr_mode=host overlay` 设置到您的 `config.txt` 文件中。

**Note**

The USB 2.0 port can operate in USB On-The-Go (OTG) mode. While not officially documented, some users have successfully enabled this functionality. The `USB_OTG_ID` pin determines the role (host or device) and is typically connected to the ID pin of a Micro USB connector. To use OTG functionality, it must be enabled in the operating system (OS). For fixed-role use, tie the `USB_OTG_ID` pin to ground.

## 2.5. Video and display interfaces

CM5 supports a range of high-speed video interfaces for connecting both displays and cameras. It includes two HDMI 2.0 outputs, two 4-lane MIPI interfaces that can be used for DSI displays or CSI cameras, and support for parallel DPI displays through GPIO. CM5 can support up to three simultaneous displays of any type (HDMI, DSI, or DPI).

### 2.5.1. Dual HDMI 2.0

CM5 includes two HDMI 2.0 interfaces, each capable of supporting a 4K display. Consider the following to ensure reliable HDMI operation:

- HDMI signals must be routed as  $100\ \Omega$  differential pairs.
  - Within a pair, each signal should be length-matched within 0.15 mm.
  - Between pairs, length matching within 25 mm is sufficient.
- Consumer Electronics Control (CEC) is supported, with an internal  $27\ k\Omega$  pull-up resistor included in CM5.
- Hotplug Detect (HPD) is supported, with an internal  $100\ k\Omega$  pull-down resistor included in CM5.
- Extended Display Identification Data (EDID) signals have internal pull-up resistors in CM5.
- Like Raspberry Pi 5, CM5 doesn't have extra ESD protection on HDMI signals because it isn't typically required. Consider whether you might need extra ESD protection and then add it if required.

### 2.5.2. MIPI (CSI and DSI)

CM5 supports two 4-lane MIPI interfaces for connecting cameras (CSI) and displays (DSI). The MIPI signals must be routed as  $100\ \Omega$  differential pairs. Within a pair, the signals should be length-matched within 0.15 mm.

In addition to DSI, displays can also be connected using the parallel DPI interface, available using GPIO functions. For more information, see [Section 2.9.2. Alternative GPIO functions](#).

#### Camera Serial Interface (CSI-2)

CM5 supports camera modules through the CSI interface. For detailed information about the CSI interface, refer to the [Raspberry Pi documentation](#). The following camera sensors are supported by official Raspberry Pi firmware:

- OmniVision OV5647
- Sony IMX219
- Sony IMX296
- Sony IMX477
- Sony IMX708

No security device is required on Compute Module products to use these camera sensors.

#### Display Serial Interface (DSI)

The DSI interface supports connection to MIPI DSI-compatible displays. CM5 is compatible with displays supported either by:

- The official Raspberry Pi firmware.
- The mainline Linux kernel.

For third-party displays not officially supported, you must provide a custom driver.

**注意**

USB 2.0 端口可运行于 USB On-The-Go (OTG) 模式。尽管官方未有文档说明，但部分用户已成功启用该功能。

`USB_OTG_ID` 引脚决定设备角色（主机或从机），通常连接到 Micro USB 连接器的 ID 引脚。启用 OTG 功能时，必须在操作系统（OS）中进行设置。若为固定角色使用，应将 `USB_OTG_ID` 引脚接地。

## 2.5. 视频与显示接口

CM5 支持多种高速视频接口，用于连接显示器和摄像头。它包括两个 HDMI 2.0 输出，两个可用于 DSI 显示器或 CSI 摄像头的四通道 MIPI 接口，并支持通过 GPIO 的并行 DPI 显示。

CM5 可支持最多三路任意类型（HDMI、DSI 或 DPI）显示的同时输出。

### 2.5.1. 双 HDMI 2.0

CM5 包含两个 HDMI 2.0 接口，每个接口均支持 4K 显示。为确保 HDMI 可靠运行，请考虑以下事项：

- HDMI 信号必须作为  $100 \Omega$  差分对布线。
  - 同一差分对内，信号长度匹配应保持在 0.15 毫米以内。
  - 不同差分对之间，长度匹配控制在 25 毫米以内即可。
- 支持消费者电子控制（CEC），CM5 内部包含一个  $27 \text{ k}\Omega$  上拉电阻。
- 支持热插拔检测（HPD），CM5 内部包含一个  $100 \text{ k}\Omega$  下拉电阻。
- 扩展显示识别数据（EDID）信号在 CM5 内部具有上拉电阻。
- 与树莓派 5 类似，CM5 在 HDMI 信号线上未设额外 ESD 保护，因为通常无需此保护。请根据实际使用需求评估是否需要额外 ESD 保护，必要时予以添加。

### 2.5.2. MIPI (CSI 和 DSI)

CM5 支持两个 4 通道 MIPI 接口，用于连接摄像头（CSI）和显示屏（DSI）。MIPI 信号必须以  $100 \Omega$  差分对形式布线。同一对信号中，信号线长度应匹配，偏差不超过 0.15 毫米。

除 DSI 外，显示屏也可通过并行 DPI 接口连接，该接口可由 GPIO 功能提供支持。更多详情请参见第 2.9.2 节，替代 GPIO 功能。

#### 相机串行接口 (CSI-2)

CM5 通过 CSI 接口支持摄像头模块。有关 CSI 接口的详细信息，请参阅树莓派官方文档。官方树莓派固件支持以下摄像头传感器：

- OmniVision OV5647
- 索尼 IMX219
- 索尼 IMX296
- 索尼 IMX477
- 索尼 IMX708

计算模块产品使用这些摄像头传感器时，无需安全设备。

#### 显示串行接口 (DSI)

DSI 接口支持连接 MIPI DSI 兼容的显示屏。CM5 兼容以下方式支持的显示屏：

- 官方树莓派固件。
- 主线 Linux 内核。

对于未被官方支持的第三方显示屏，必须提供自定义驱动程序。

## 2.6. I2C interfaces

CM5 provides two I2C buses that can be repurposed depending on system configuration and peripheral usage.

### 2.6.1. MIPI I2C bus ( SDA0 and SCL0 )

The internal I2C bus is normally allocated to the `MIPI0` interface. However, it can be used as a general I2C bus or GPIO if the `MIPI0` interface isn't in use:

- The serial data pin ( `SDA0` ) within the `MIPI0` interface is connected to `GPIO038` on RP1.
- The serial clock pin ( `SCL0` ) within the `MIPI0` interface is connected to `GPIO039` on RP1.

### 2.6.2. HAT EEPROM identification I2C bus ( ID\_SD and ID\_SC )

CM5 includes another I2C bus, with signals exposed on the `ID_SD` (data) and `ID_SC` (clock) pins. This bus is typically reserved for identifying HATs and controlling MIPI1 devices.

If the firmware isn't using this I2C bus (for example, `MIPI1` isn't being used), then these pins can be repurposed as `GPIO00` and `GPIO01` if needed. When using these pins as GPIO pins, add `force_eeprom_read=0` to the `config.txt` file. This prevents the firmware from checking whether there's a HAT EEPROM available.

## 2.7. SDIO (CM5Lite only)

This section covers external storage options for **CM5Lite** with the SDIO interface.

CM5Lite doesn't include eMMC storage on board. However, it exposes **Secure Digital Input Output (SDIO)** interface for external storage through the connector: either an external eMMC or SD card (for removable storage).

Depending on the type of storage you use, consider the following configuration signals:

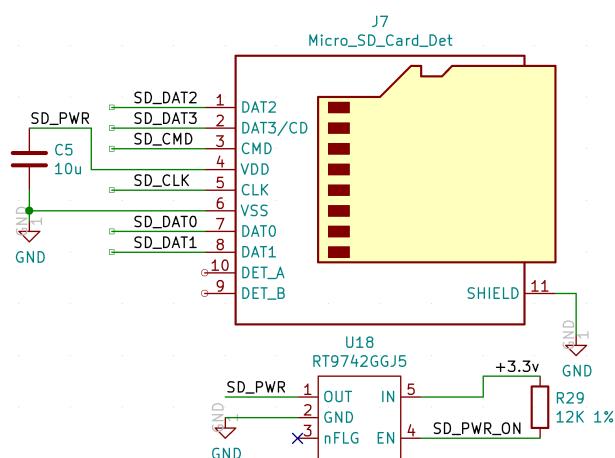
- **External eMMC.** Set `SD_VDD_OVERRIDE` to high ( `CM5_3.3V` ) to force 1.8 V signalling on the SDIO interface.
- **SD card.** Use the `SD_PWR_ON` signal to control an external power switch for an SD card. To enable SD card boot by default, add a pull-up resistor to keep the power switch on.

#### Note

SD cards require a power switch controlled by `SD_PWR_ON`; this is the only way to reset the SD card.

**Figure 3.**

CM5Lite SD card interface



## 2.6. I2C 接口

CM5 提供两个 I2C 总线，可根据系统配置和外设使用需求重新分配。

### 2.6.1. MIPI I2C 总线 ( SDA0 和 SCL0 )

内部 I2C 总线通常分配给  
接口未使用，

- 则可用作通用 I2C 总线或 GPIO： SDA0 在 MIPI0
- 串行时钟引脚（ SCL0 ）在 MIPI0

接口。但如果

MIPI0

接口连接至 RP1 上的 GPIO38。  
接口连接至 RP1 上的 GPIO39。

### 2.6.2. HAT EEPROM 识别 I2C 总线 ( ID\_SD 和 ID\_SC )

CM5 包含另一条 I2C 总线，信号引脚暴露在  
识别 HAT 及控制 MIPI1 设备。

ID\_SD (数据) 和 ID\_SC (时钟) 引脚上。该总线通常用于

如果固件未使用此 I2C 总线（例如，  
（如有需要）。使用这些引脚作为 GPIO 时，需要添加 force\_eeprom\_read=0 至 config.txt 文件进行配置。此操作阻止固件  
检测是否存在 HAT EEPROM。

GPIO0 和 GPIO1

## 2.7. SDIO (仅限 CM5Lite)

本节介绍带 SDIO 接口的 CM5Lite 的外部存储选项。

CM5Lite 不包含板载 eMMC 存储。但其通过连接器提供了安全数字输入输出 (SDIO) 接口，支持连接外部 eMMC 或 SD 卡（用于可拆卸存储）。

根据所用存储类型，请考虑以下配置信号：

- 外部 eMMC。需将 SD\_VDD\_OVERRIDE 设置为高电平 (CM5\_3.3V) 以强制 SDIO 接口使用 1.8 V 信号电平。
- SD 卡。使用 SD\_PWR\_ON 信号控制 SD 卡的外部电源开关。如需默认启用 SD 卡启动，请添加上拉电阻以保持电源开关常开。

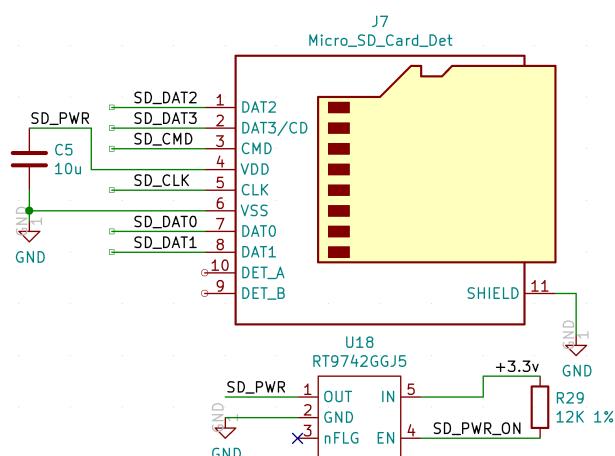
#### 注意

SD 卡要求电源开关由

SD\_PWR\_ON 信号控制；这是重置 SD 卡的唯一方法。

图 3。

CM5Lite SD 卡接口



## 2.8. Debug UART

There is space to fit a debug UART connector for troubleshooting and diagnosing. This connector provides the same functionality as Raspberry Pi 5. The connector is a three-pin, 1 mm pitch JST-SH connector (part number **BM03B-SRSS-TB**). The signals are replicated on the bottom as test points, allowing you access to the debug UART signals even if the main debug connector isn't fitted or available. For information about test points, see [Appendix A. Test Points](#).

## 2.9. GPIO

There are 28 general-purpose I/O (GPIO) pins available, which correspond to the GPIO pins on the Raspberry Pi 5 40-pin header. These pins have access to internal peripherals, such as DPI, I<sub>2</sub>C, PWM, SPI, and UART. Details about these features and the available multiplexing options are described in the [RP1 peripherals datasheet](#).

To minimise electromagnetic compatibility (EMC) issues, we recommend setting the drive strength and slew rate to the lowest levels necessary. GPIO2 and GPIO3 include 1.8 kΩ pull-up resistors.

The GPIO bank is powered by the `GPIO_VREF` supply. This can connect to `CM5_1.8V` for 1.8 V signalling, or `CM5_3.3V` for 3.3 V signalling. Don't exceed 50 mA for total current load on all 28 GPIO pins. `GPIO_VREF` must be connected to either `CM5_3.3v` or `CM5_1.8v`. It's possible to use 2.5 V signalling by supplying an external 2.5 V supply to `GPIO_VREF`. This external supply must only be active while `CM5_1.8v` is on and must be fully discharged within 1 ms after `CM5_1.8v` is going low.

### 2.9.1. Alternative function assignments

Up to nine alternative function assignments are available on the GPIO pins. The following table provides an overview of these alternative functions.

Each GPIO can have only one function at a time. Likewise, each peripheral input (for example, `I2C3_SCL`) must be assigned to only one GPIO pin. If the same peripheral input is connected to multiple GPIOs, the peripheral sees the logical OR of these GPIO inputs.

Function selections without a named function in the following table are reserved.

**Table 1.**  
*GPIO function selection*

GPIO	Function									
	a0	a1	a2	a3	a4	a5	a6	a7	a8	
0	SPI0_SIO[3]	DPI_PCLK	UART1_TX	I2C0_SDA		SYS_RIO[0]	PROC_RIO[0]	PIO[0]	SPI2_CS <sub>n</sub> [0]	
1	SPI0_SIO[2]	DPI_DE	UART1_RX	I2C0_SCL		SYS_RIO[1]	PROC_RIO[1]	PIO[1]	SPI2_SIO[1]	
2	SPI0_CS <sub>n</sub> [3]	DPI_VSYNC	UART1_CTS	I2C1_SDA	UART0_IR_RX	SYS_RIO[2]	PROC_RIO[2]	PIO[2]	SPI2_SIO[0]	
3	SPI0_CS <sub>n</sub> [2]	DPI_HSYNC	UART1 RTS	I2C1_SCL	UART0_IR_TX	SYS_RIO[3]	PROC_RIO[3]	PIO[3]	SPI2_SCLK	
4	GPCLK[0]	DPI_D[0]	UART2_TX	I2C2_SDA	UART0 RI	SYS_RIO[4]	PROC_RIO[4]	PIO[4]	SPI3_CS <sub>n</sub> [0]	
5	GPCLK[1]	DPI_D[1]	UART2_RX	I2C2_SCL	UART0_DTR	SYS_RIO[5]	PROC_RIO[5]	PIO[5]	SPI3_SIO[1]	
6	GPCLK[2]	DPI_D[2]	UART2_CTS	I2C3_SDA	UART0_DCD	SYS_RIO[6]	PROC_RIO[6]	PIO[6]	SPI3_SIO[0]	
7	SPI0_CS <sub>n</sub> [1]	DPI_D[3]	UART2_RTS	I2C3_SCL	UART0_DSR	SYS_RIO[7]	PROC_RIO[7]	PIO[7]	SPI3_SCLK	
8	SPI0_CS <sub>n</sub> [0]	DPI_D[4]	UART3_TX	I2C0_SDA		SYS_RIO[8]	PROC_RIO[8]	PIO[8]	SPI4_CS <sub>n</sub> [0]	
9	SPI0_SIO[1]	DPI_D[5]	UART3_RX	I2C0_SCL		SYS_RIO[9]	PROC_RIO[9]	PIO[9]	SPI4_MISO	
10	SPI0_SIO[0]	DPI_D[6]	UART3_CTS	I2C1_SDA		SYS_RIO[10]	PROC_RIO[10]	PIO[10]	SPI4_MOSI	
11	SPI0_SCLK	DPI_D[7]	UART3_RTS	I2C1_SCL		SYS_RIO[11]	PROC_RIO[11]	PIO[11]	SPI4_SCLK	
12	PWM0[0]	DPI_D[8]	UART4_TX	I2C2_SDA	AUDIO_OUT_L	SYS_RIO[12]	PROC_RIO[12]	PIO[12]	SPI5_CS <sub>n</sub> [0]	
13	PWM0[1]	DPI_D[9]	UART4_RX	I2C2_SCL	AUDIO_OUT_R	SYS_RIO[13]	PROC_RIO[13]	PIO[13]	SPI5_SIO[1]	
14	PWM0[2]	DPI_D[10]	UART4_CTS	I2C3_SDA	UART0_TX	SYS_RIO[14]	PROC_RIO[14]	PIO[14]	SPI5_SIO[0]	
15	PWM0[3]	DPI_D[11]	UART4_RTS	I2C3_SCL	UART0_RX	SYS_RIO[15]	PROC_RIO[15]	PIO[15]	SPI5_SCLK	
16	SPI1_CS <sub>n</sub> [2]	DPI_D[12]			UART0_CTS	SYS_RIO[16]	PROC_RIO[16]	PIO[16]		
17	SPI1_CS <sub>n</sub> [1]	DPI_D[13]			UART0_RTS	SYS_RIO[17]	PROC_RIO[17]	PIO[17]		

## 2.8. 调试 UART

预留了调试 UART 连接器位置，用于故障排查和诊断。该连接器提供与树莓派 5 相同的功能。该连接器为三针、1 mm 间距的 JST-SH 连接器（部件编号**BM03B-SRSS-TB**）。信号在底部以测试点形式复制，即使主调试连接器未安装或不可用，仍可访问调试 UART 信号。有关测试点的详细信息，请参见附录 A 测试点。

## 2.9. GPIO

共有 28 个通用输入输出（GPIO）引脚可用，分别对应树莓派 5 的 40 针 GPIO 接口。

这些引脚可访问内部外设，如 DPI、I2C、PWM、SPI 和 UART。有关这些功能及其可用复用选项的详细信息，请参阅 RP1 外设数据手册。

为最小化电磁兼容性（EMC）问题，建议将驱动强度及转换速率设置为必要的最低水平。GPIO2 与 GPIO3 内置 1.8 kΩ 上拉电阻。

GPIO 组由 **GPIO\_VREF** 电源供电，该电源可连接至 **CM5\_1.8V** 以实现 1.8 V 信号，或 **CM5\_3.3V** 以实现 3.3 V 信号。28 个 GPIO 引脚的总电流负载不应超过 50 mA。  
**GPIO\_VREF** 必须连接至 **CM5\_3.3V** 或 **CM5\_1.8V**。可通过向 **GPIO\_VREF** 提供外部 2.5 V 电源来实现 2.5 V 信号。该外部电源仅可在 **CMS\_1.8V** 工作时启用，且须在其关闭后 1 毫秒内完全放电。**CM5\_1.8V** 电平正在变低。

### 2.9.1. 备用功能分配

GPIO 引脚最多支持九种备用功能分配。下表提供了这些备用功能的概要。

每个 GPIO 引脚在任何时刻只能设置一种功能。同样，每个外设输入（例如，**I2C3\_SCL**）必须仅分配给一个 GPIO 引脚。如果同一外设输入连接到多个 GPIO 引脚，则外设会检测到这些 GPIO 输入的逻辑或（OR）状态。下表中未命名功能的选项为保留。

**表1。**  
GPIO 功能选择

GPIO	功能									
	a0	a1	a2	a3	a4	a5	a6	a7	a8	
0	SPI0_SIO[3]	DPI_PCLK	UART1_TX	I2C0_SDA		SYS_RIO[0]	PROC_RIO[0]	PIO[0]	SPI2_CS[0]	
1	SPI0_SIO[2]	DPI_DE	UART1_RX	I2C0_SCL		SYS_RIO[1]	PROC_RIO[1]	PIO[1]	SPI2_SIO[1]	
2	SPI0_CS[3]	DPI_VSYNC	UART1_CTS	I2C1_SDA	UART0_IR_RX	SYS_RIO[2]	PROC_RIO[2]	PIO[2]	SPI2_SIO[0]	
3	SPI0_CS[2]	DPI_HSYNC	UART1 RTS	I2C1_SCL	UART0_IR_TX	SYS_RIO[3]	PROC_RIO[3]	PIO[3]	SPI2_SCLK	
4	GPCLK[0]	DPI_D[0]	UART2_TX	I2C2_SDA	UART0_RI	SYS_RIO[4]	PROC_RIO[4]	PIO[4]	SPI3_CS[0]	
5	GPCLK[1]	DPI_D[1]	UART2_RX	I2C2_SCL	UART0_DTR	SYS_RIO[5]	PROC_RIO[5]	PIO[5]	SPI3_SIO[1]	
6	GPCLK[2]	DPI_D[2]	UART2_CTS	I2C3_SDA	UART0_DCD	SYS_RIO[6]	PROC_RIO[6]	PIO[6]	SPI3_SIO[0]	
7	SPI0_CS[1]	DPI_D[3]	UART2_RTS	I2C3_SCL	UART0_DSR	SYS_RIO[7]	PROC_RIO[7]	PIO[7]	SPI3_SCLK	
8	SPI0_CS[0]	DPI_D[4]	UART3_TX	I2C0_SDA		SYS_RIO[8]	PROC_RIO[8]	PIO[8]	SPI4_CS[0]	
9	SPI0_SIO[1]	DPI_D[5]	UART3_RX	I2C0_SCL		SYS_RIO[9]	PROC_RIO[9]	PIO[9]	SPI4_MISO	
10	SPI0_SIO[0]	DPI_D[6]	UART3_CTS	I2C1_SDA		SYS_RIO[10]	PROC_RIO[10]	PIO[10]	SPI4_MOSI	
11	SPI0_SCLK	DPI_D[7]	UART3_RTS	I2C1_SCL		SYS_RIO[11]	PROC_RIO[11]	PIO[11]	SPI4_SCLK	
12	PWM0[0]	DPI_D[8]	UART4_TX	I2C2_SDA	AUDIO_OUT_L	SYS_RIO[12]	PROC_RIO[12]	PIO[12]	SPI5_CS[0]	
13	PWM0[1]	DPI_D[9]	UART4_RX	I2C2_SCL	AUDIO_OUT_R	SYS_RIO[13]	PROC_RIO[13]	PIO[13]	SPI5_SIO[1]	
14	PWM0[2]	DPI_D[10]	UART4_CTS	I2C3_SDA	UART0_TX	SYS_RIO[14]	PROC_RIO[14]	PIO[14]	SPI5_SIO[0]	
15	PWM0[3]	DPI_D[11]	UART4_RTS	I2C3_SCL	UART0_RX	SYS_RIO[15]	PROC_RIO[15]	PIO[15]	SPI5_SCLK	
16	SPI1_CS[2]	DPI_D[12]			UART0_CTS	SYS_RIO[16]	PROC_RIO[16]	PIO[16]		
17	SPI1_CS[1]	DPI_D[13]			UART0_RTS	SYS_RIO[17]	PROC_RIO[17]	PIO[17]		

GPIO	Function									
18	SPI1_CSn[0]	DPI_D[14]	I2S0_SCLK	PWM0[2]	I2S1_SCLK	SYS_RIO[18]	PROC_RIO[18]	PIO[18]	GPCLK[1]	
19	SPI1_SIO[1]	DPI_D[15]	I2S0_WS	PWM0[3]	I2S1_WS	SYS_RIO[19]	PROC_RIO[19]	PIO[19]		
20	SPI1_SIO[0]	DPI_D[16]	I2S0_SDI[0]	GPCLK[0]	I2S1_SDI[0]	SYS_RIO[20]	PROC_RIO[20]	PIO[20]		
21	SPI1_SCLK	DPI_D[17]	I2S0_SDO[0]	GPCLK[1]	I2S1_SDO[0]	SYS_RIO[21]	PROC_RIO[21]	PIO[21]		
22	SDIO0_CLK	DPI_D[18]	I2S0_SDI[1]	I2C3_SDA	I2S1_SDI[1]	SYS_RIO[22]	PROC_RIO[22]	PIO[22]		
23	SDIO0_CMD	DPI_D[19]	I2S0_SDO[1]	I2C3_SCL	I2S1_SDO[1]	SYS_RIO[23]	PROC_RIO[23]	PIO[23]		
24	SDIO0_DAT[0]	DPI_D[20]	I2S0_SDI[2]		I2S1_SDI[2]	SYS_RIO[24]	PROC_RIO[24]	PIO[24]	SPI2_CSn[1]	
25	SDIO0_DAT[1]	DPI_D[21]	I2S0_SDO[2]	AUDIO_IN_CLK	I2S1_SDO[2]	SYS_RIO[25]	PROC_RIO[25]	PIO[25]	SPI3_CSn[1]	
26	SDIO0_DAT[2]	DPI_D[22]	I2S0_SDI[3]	AUDIO_IN_DAT0	I2S1_SDI[3]	SYS_RIO[26]	PROC_RIO[26]	PIO[26]	SPI5_CSn[1]	
27	SDIO0_DAT[3]	DPI_D[23]	I2S0_SDO[3]	AUDIO_IN_DAT1	I2S1_SDO[3]	SYS_RIO[27]	PROC_RIO[27]	PIO[27]	SPI1_CSn[1]	

## 2.9.2. Alternative GPIO functions

A variety of alternative GPIO functions accommodate diverse peripheral interfaces and communication protocols. The following list summarises the available peripherals and their supported configurations:

- Five UARTs, with standard and extended wiring options:
  - Four UARTs with 4-wire interfaces for serial communication ( TX , RX , CTS , RTS ).
  - One UART ( `UART0` ) with an 8-wire interface ( TX , RX , CTS , RTS , DTR , DCD , DSR , RI ) or an IrDA interface ( IR\_TX , IR\_RX ).
- One 4-bit SDIO for Secure Digital Input/Output.
- Four PWM channels for pulse-width modulation.
- One I2S Master interface ( `ISCO` ), quadruple lane.
- One I2S, Slave interface ( `ISC1` ), quadruple lane.
- Two `AUDIO_OUT` PWM audio outputs, which require buffering using a low-noise PSU buffer and filtering with a 22 KHz first-order RC network.
- Two `AUDIO_IN` digital PDM inputs.
- Two general-purpose clock (GPCLK) outputs.
- One DPI (Display Parallel Interface) with `PCLK` , `DE` , `VSYNC` , `HSYNC` , and up to 24-bit data.
- 28 GPIO ( `SYS_RIO` ) pins.
- Four I2C controllers ( `SDA` , `SCL` ).
- Six SPI controllers, detailed in [Table 2](#), below.

**Table 2.**

*SPI controller configuration*

Instance ID	Master/Slave	Chip-select count	Max I/O width
SPI0	M	4	Quad
SPI1	M	3	Dual
SPI2	M	2	Dual
SPI3	M	2	Dual
SPI4	S	1	Single
SPI5	M	2	Dual

For conventional SPI connections, the Serial Input/Output (SIO) pins numbered 0 and 1 have specific roles:

- `SIO0` is the `MOSI` pin (Master Out Slave In).
- `SIO1` is the `MISO` pin (Master In Slave Out).

The other SIO pins are required for the basic SPI communication to work.

GPIO	功能									
18	SPI1_CSn[0]	DPI_D[14]	I2S0_SCLK	PWM0[2]	I2S1_SCLK	SYS_RIO[18]	PROC_RIO[18]	PIO[18]	GPCLK[1]	
19	SPI1_SIO[1]	DPI_D[15]	I2S0_WS	PWM0[3]	I2S1_WS	SYS_RIO[19]	PROC_RIO[19]	PIO[19]		
20	SPI1_SIO[0]	DPI_D[16]	I2S0_SDI[0]	GPCLK[0]	I2S1_SDI[0]	SYS_RIO[20]	PROC_RIO[20]	PIO[20]		
21	SPI1_SCLK	DPI_D[17]	I2S0_SDO[0]	GPCLK[1]	I2S1_SDO[0]	SYS_RIO[21]	PROC_RIO[21]	PIO[21]		
22	SDIO0_CLK	DPI_D[18]	I2S0_SDI[1]	I2C3_SDA	I2S1_SDI[1]	SYS_RIO[22]	PROC_RIO[22]	PIO[22]		
23	SDIO0_CMD	DPI_D[19]	I2S0_SDO[1]	I2C3_SCL	I2S1_SDO[1]	SYS_RIO[23]	PROC_RIO[23]	PIO[23]		
24	SDIO0_DAT[0]	DPI_D[20]	I2S0_SDI[2]		I2S1_SDI[2]	SYS_RIO[24]	PROC_RIO[24]	PIO[24]	SPI2_CSn[1]	
25	SDIO0_DAT[1]	DPI_D[21]	I2S0_SDO[2]	AUDIO_IN_CLK	I2S1_SDO[2]	SYS_RIO[25]	PROC_RIO[25]	PIO[25]	SPI3_CSn[1]	
26	SDIO0_DAT[2]	DPI_D[22]	I2S0_SDI[3]	AUDIO_IN_DAT0	I2S1_SDI[3]	SYS_RIO[26]	PROC_RIO[26]	PIO[26]	SPI5_CSn[1]	
27	SDIO0_DAT[3]	DPI_D[23]	I2S0_SDO[3]	AUDIO_IN_DAT1	I2S1_SDO[3]	SYS_RIO[27]	PROC_RIO[27]	PIO[27]	SPI1_CSn[1]	

## 2.9.2. 备用 GPIO 功能

多种替代GPIO功能支持各种外设接口和通信协议。下列列表总结了可用外设及其支持的配置：

- 五个UART，具备标准及扩展接线选项：
  - 四个UART，采用4线接口用于串行通信（ TX , RX , CTS , RTS ）。
  - 一个UART（ UART0 ），采用8线接口（ TX , RX , CTS , RTS , DTR , DCD , DSR , RI ）或IrDA接口（ IR\_TX , IR\_RX ）。
- 一个4位SDIO，用于安全数字输入/输出。
- 四个PWM通道，用于脉宽调制。
- 一个I2S主接口（ ISCO0 ），四通道。
- 一个I2S从接口（ ISC1 ），四通道。
- 两个AUDIO\_OUT PWM音频输出，需使用低噪声电源缓冲器进行缓冲，并通过22 KHz一阶RC网络滤波。
- 两个AUDIO\_IN 数字PDM输入。
- 两个通用时钟（GPCLK）输出。
- 一个DPI（显示并行接口），包含 PCLK , DE , VSYNC , HSYNC ，最多支持24位数据。
- 28个GPIO（ SYS\_RIO ）引脚。
- 四个I2C控制器（ SDA , SCL ）。
- 六个SPI控制器，详见下表2。

表2。  
SPI控制器配置

实例ID	主/从	片选数量	最大I/O位宽
SPI0	主	4	四线
SPI1	主	3	两线
SPI2	主	2	两线
SPI3	主	2	两线
SPI4	S	1	单一
SPI5	主	2	两线

对于传统的SPI连接，编号为

0 和 1 的串行输入/输出(SIO)引脚具有特定功能：

- SIO0 是 MOSI 引脚（主设备输出，从设备输入）。
- SIO1 是 MISO 引脚（主设备输入，从设备输出）。

其他SIO引脚是基础SPI通信正常工作的必需部分。

### 2.9.3. Camera GPIOs ( CAM\_GPIO )

CM5 includes two GPIO control signals for the camera module: `CAM_GPIO00` and `CAM_GPIO01`.

- `CAM_GPIO00` is typically routed to pin 17 on the camera connector. This signal is used to control power to the camera module. `CAM_GPIO00` corresponds to `GPIO34` on RP1.
- `CAM_GPIO01` has been added to CM5 for future expansion, and isn't present on previous Compute Modules; we recommend routing this signal to pin 18 on the camera connector. `CAM_GPIO01` corresponds to `GPIO35` on RP1.

### 2.10. Status LEDs ( LED\_nACT and LED\_nPWR )

Status LEDs on CM5 provide visual feedback about the board's activity and power states. These signals replicate the green and red LEDs found on Raspberry Pi 5, helping users monitor eMMC activity, boot errors, and power status.

- `LED_nACT` : This pin drives an LED that indicates eMMC or SD card access, replicating the green LED on Raspberry Pi 5. Under Linux, the LED flashes to signify eMMC or SD card access. If a boot error occurs, the LED flashes an error pattern. To decode these patterns, see the [LED Flash codes](#) in the Raspberry Pi documentation.
- `LED_nPWR` : This pin controls an LED that indicates the board's power status, replicating the red LED on Raspberry Pi 5. When the board is powered but shut down, the LED lights up.

### 2.11. Fan control ( Fan\_PWM and Fan\_Tacho )

CM5 provides two pins for monitoring and controlling PWM fans, allowing for fan speed regulation and tachometer feedback.

- `Fan_PWM` : An open-collector output pin designed to drive a variety of PWM-controlled fans.
- `Fan_Tacho` : An input pin with internal pull-up to `CM5_3.3V` for reading tachometer output signals from many PWM fans.

During CM5 shutdown, power to the `Fan_PWM` signal is also stopped. If the fan is powered from a 5 V supply, the fan might still continue to run after power supply shutdown. To prevent this, turn off the supply to the fan simultaneously. For example, you could share power with the external USB ports controlled by `VBUS_EN`. Alternatively, you could use an open-collector buffer (such as a 74LVC1G07) powered from 5 V: connect its input to `CM5_3.3V` and wire the output in parallel with the PWM control line.

## 2.12. Power management and control

The following signals relate to power state management, power supply negotiation, and system-level control for CM5. Proper use of these signals ensures reliable power sequencing, system startup, shutdown, and battery-backed real-time clock (RTC) operation.

### 2.12.1. USB-C signals ( CC0 and CC1 )

The USB-C connector uses the `CC0` and `CC1` Configuration Channel (CC) signals to negotiate power delivery. On CM5, these signals enable the system to request up to 5 V at 5 A from the power source, ensuring efficient and safe power transfer over USB-C.

### 2.12.2. System control signals ( PMIC\_EN , PWR\_BUT , VBAT , nRPI\_BOOT , and EEPROM\_nWP )

[Table 3](#) lists key control pins that govern system behaviour during startup, shutdown, and battery-powered operation.

**Table 3.**

*System control signals*

Pin	Description	Usage
<code>PMIC_EN</code>	Controls the power-down state of CM5.	Pull low to put CM5 in the lowest power-down state. We recommend only pulling this pin low after OS shutdown.

## 2.9.3. 摄像头 GPIO ( CAM\_GPIO )

CM5 包含两个用于摄像头模块的 GPIO 控制信号：`CAM_GPIO00` 和 `CAM_GPIO1`。

- `CAM_GPIO00` 通常接至摄像头连接器的针脚17。该信号用于控制摄像头模块的电源。  
`CAM_GPIO00` 对应于 RP1 上的 GPIO34。
- `CAM_GPIO1` 已添加至 CM5 以支持未来扩展，之前的计算模块中未包含该信号；建议将该信号接至摄像头连接器的针脚18。  
`CAM_GPIO1` 对应于 RP1 上的 GPIO35。

## 2.10. 状态指示灯 ( LED\_nACT 和 LED\_nPWR )

CM5 上的状态指示灯提供主板活动和电源状态的视觉反馈。这些信号复制了树莓派 5 上的绿、红指示灯，协助用户监控 eMMC 活动、启动错误及电源状态。

- `LED_nACT`：该引脚驱动一个 LED，指示 eMMC 或 SD 卡访问，复制了树莓派 5 上的绿灯。  
在 Linux 环境下，该 LED 会闪烁以表示 eMMC 或 SD 卡的访问。如果发生启动错误，LED 会闪烁错误代码。欲解码这些代码，请参阅树莓派文档中的 LED 闪烁代码。
- `LED_nPWR`：该引脚控制一个指示板电源状态的 LED，类似于树莓派 5 上的红色 LED。当电路板已通电但处于关机状态时，LED 会点亮。

## 2.11. 风扇控制 ( Fan\_PWM 和 风扇转速传感 )

CM5 提供两个引脚用于监控和控制 PWM 风扇，支持风扇速度调节及转速反馈。

- `Fan_PWM`：一个开集电极输出引脚，用于驱动各种 PWM 控制风扇。
- 风扇转速传感：带内部上拉电阻的输入引脚，用于 CM5\_3.3V 读取多数 PWM 风扇的转速信号输出。

在 CM5 关机期间，`Fan_PWM` 信号的供电也会停止。如果风扇由 5V 电源供电，则在电源关闭后风扇可能仍会继续运转。为防止此情况，请同时关闭风扇电源。例如，您可以与由 `VBUS_EN` 控制的外部 USB 端口共享电源。或者，您可以使用由 5V 供电的开集电极缓冲器（如 74LVC1G07）：将其输入端连接至 CM5\_3.3V，输出端并联接入 PWM 控制线。

## 2.12. 电源管理与控制

以下信号涉及 CM5 的电源状态管理、电源协商及系统级控制。正确使用这些信号可确保可靠的电源顺序控制、系统启动、关机及电池备份实时时钟（RTC）正常运行。

### 2.12.1. USB-C 信号 ( CC0 和 CC1 )

USB-C 连接器使用 `CC0` 和 `CC1` 配置通道（CC）信号进行电源协商。在 CM5 上，这些信号允许系统向电源请求最高 5V、5A 电流，确保 USB-C 端口电力传输的高效与安全。

### 2.12.2. 系统控制信号 ( PMIC\_EN , PWR\_BUT , VBAT , nRPI\_BOOT , 和 EEPROM\_nWP )

表 3 列出了启动、关机及电池供电操作期间控制系统行为的关键控制引脚。

表 3.  
系统控制信号

引脚	描述	用途
<code>PMIC_EN</code>	控制 CM5 的电源关闭状态。	拉低此引脚可将 CM5 置于最低功耗关闭状态。建议仅在操作系统关机后拉低该引脚。

PWR_BUT	Acts as a power switch when connected to a button, controlling power on and off for CM5.	Pull low briefly to power on or off; hold low for more than 5 seconds to force CM5 to shut down.
VBAT	Supply 2.5 V to 3.5 V to power the on-board RTC. Provides backup power for RTC so that it can keep time even when the board is off.	When CM5 is powered on, RTC uses a small static load. When CM5 is powered off, the load increases to maintain RTC. A typical CR2032 lasts > 3 years when CM5 is unpowered.
nRPI_BOOT	Determines boot source during startup.	Hold low during boot to bypass eMMC and boot through USB 2.0 instead.
EEPROM_nWP	Enables hardware write protection on the EEPROM to prevent data modification.	Pull this pin low to prevent end users from changing the contents of on-board EEPROM. For software configuration instructions, see the <a href="#">EEPROM write protect documentation</a> .

PWR_BUT	连接按键时作为电源开关，控制 CM5 的电源开关。	短暂拉低以开机或关机；持续拉低超过 5 秒以强制 CM5 关机。
VBAT	供电电压为 2.5 V 至 3.5 V，用于为板载 RTC 供电。为 RTC 提供备份电源，使其即使在主板断电时也能保持计时。	当 CM5 通电时，RTC 仅消耗极小的静态电流。当 CM5 断电时，为维持 RTC，负载电流会增加。典型的 CR2032 电池在 CM5 无电状态下可持续使用超过 3 年。
nRPI_BOOT	确定启动期间的引导源。	启动时将此引脚保持低电平，可绕过 eMMC，并通过 USB 2.0 启动。
EEPROM_nWP	启用 EEPROM 的硬件写保护，以防止数据被修改。	将此引脚拉低以防止最终用户更改板载 EEPROM 的内容。关于软件配置指导，请参见 EEPROM 写保护文档。

# 3. Power

CM5 requires a regulated 5 V supply for operation. CM5 can also supply 600 mA at 3.3 V and 1.8 V to peripherals. The following sections describe the required power-up and power-down sequences, typical and maximum power consumption, and the capabilities of the on-board voltage regulators.

## 3.1. Power-up sequencing

The following list summarises the power-up conditions and sequencing necessary for proper power-up of CM5:

- No pins should be powered before the 5 V rail is active.
- For write-protection of the on-board boot EEPROM, the `EEPROM_NWP` pin must be low before power-up.
- To boot CM5 through USB, the `RPI_NBOOT` pin must be low within 2 ms after the 5 V rail rises.
- The 5 V rail should rise monotonically to at least 4.75 V and remain above this level during operation.
- The power-up sequence begins after the 5 V rail is above 4.75 V and the `PMIC_EN` signal rises.
- The power rails and signals rise in the following order:
  1. 5 V rises
  2. `PMIC_EN` rises
  3. `CM5_+3.3V` rises
  4. `CM5_+1.8V` rises at least 1 ms after `CM5_+3.3V`

## 3.2. Power-down sequencing

The following list summarises the recommended power-down procedure and considerations for CM5 to ensure safe shutdown and file system integrity:

- To ensure file system consistency, shut down the operating system before removing power.
- If controlled shutdown isn't possible, consider using file systems like `btrfs`, `f2fs`, or `overlayfs`, which can be enabled through `raspi-config`.
- After the operating system has shut down, the 5 V rail can be removed or the `PMIC_EN` pin can be taken low to put the CM5 into the lowest power mode.
- During the shutdown sequence, `CM5_+1.8V` will be discharged before the `CM5_3.3V` rail.

## 3.3. Power consumption

The exact power consumption of CM5 depends on the tasks being run on it. Typical values are summarised below:

- The lowest shutdown power consumption mode occurs when `PMIC_EN` is driven low, typically around 1.3  $\mu$ A.
- With `PMIC_EN` high but software shut down, the typical consumption is about 3  $\mu$ A.
- Idle power consumption is typically 400 mA, but this varies depending on the operating system.
- Operating power consumption is typically around 900 mA, but this depends on the operating system and running tasks.

## 3.4. Regulator outputs

CM5 has built-in voltage regulators that provide 3.3 V (`CM5_+3.3V`) and 1.8 V (`CM5_+1.8V`) power rails. These regulators can each deliver up to 600 mA of current to external devices or peripherals connected to the board. The current drawn by connected devices from these regulators isn't included in the overall power consumption figures; the reported power usage only accounts for the board itself, not the extra peripherals powered through these regulators.

# 3. 电源

CM5 需要受控的 5 V 电源以保证正常运行。CM5 同时可向外设提供 3.3 V 和 1.8 V，最大电流为 600 mA。以下章节介绍了所需的上电和断电顺序、典型及最大功耗，以及板载电压调节器的性能。

## 3.1. 上电顺序

以下列表概述了 CM5 正确上电所必需的条件和顺序：

- 在 5 V 电源轨激活之前，任何引脚均不应供电。
- 为对板载启动 EEPROM 进行写保护，`EEPROM_nWP` 引脚必须在上电前保持低电平。
- 若通过 USB 启动 CM5，`RPI_nBOOT` 引脚必须在 5 V 电源上线后 2 毫秒内保持低电平。
- 5 V 电源线应单调上升至至少 4.75 V，并在工作期间保持高于该电平。
- 上电序列始于 5 V 电源线高于 4.75 V 且 `PMIC_EN` 信号上升时。
- 电源线和信号的上升顺序如下：
  1. 5 V 上升
  2. `PMIC_EN` 上升
  3. `CM5_+3.3V` 上升
  4. `CM5_+1.8V` 应在 `CM5_+3.3V`

## 3.2. 断电顺序

之后至少 1 毫秒上升

- 为确保文件系统一致性，请在断电前关闭操作系统。
- 如果无法执行受控关机，可考虑使用如下文件系统：  
`btrfs`, `f2fs`, 或 `overlayfs`，且可通过  
`raspi-config` 启用。`raspi-config`。
- 操作系统关机后，可切断 5 V 电源轨，或将 `PMIC_EN` 引脚置低，使 CM5 进入最低功耗模式。  
进入最低功耗模式。
- 在关机序列期间，`CM5_+1.8V` 将先被放电，随后是 `CM5_3.3V` 轨电压。

## 3.3. 电源功耗

CM5 的具体功耗取决于所执行的任务。典型值总结如下：

- 最低关机功耗模式发生于 `PMIC_EN` 被拉低时，通常约为 1.3  $\mu$ A。
- 当 `PMIC_EN` 为高电平但软件处于关机状态时，典型功耗约为 3  $\mu$ A。
- 空闲功耗通常为 400 mA，但取决于操作系统。
- 工作功耗通常约为 900 mA，但受操作系统和运行任务的影响。

## 3.4. 稳压器输出

CM5 内置稳压器，提供 3.3 V (`CM5_+3.3V`) 与 1.8 V (`CM5_+1.8V`) 电源轨。这些稳压器各自能够向连接至电路板的外部设备或外围设备提供最多 600 mA 电流。连接设备从这些稳压器获取的电流不包含在总体功耗数据中；报告的功耗数据仅针对电路板本身，不包括通过这些稳压器供电的额外外围设备。

# 4. Specifications

This section includes technical descriptions of CM5's components and capabilities, including its dimensions, antenna, pinout, electrical specifications, and thermal characteristics.

## 4.1. Mechanical specifications

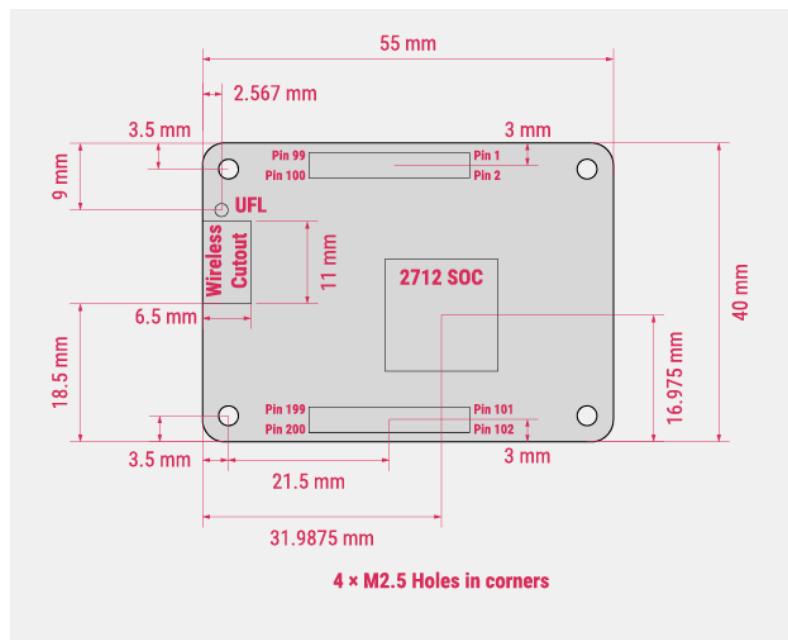
CM5 consists of a compact PCB and an optional wireless antenna. The physical features of CM5's components are summarised in [Section 4.1.1. PCB dimensions](#), which includes information about the module size, PCB thickness, SoC height, and stacking height options. Antenna orientation and clearance requirements are summarised in [Section 4.1.2. Wireless antenna](#).

For complete mechanical drawings and CAD models, see the [CM5 design files](#), included in the official design data package. These files are provided to help designers visualise and plan their hardware; they are for reference only and might change over time as the board design is updated or revised.

### 4.1.1. PCB dimensions

CM5 is a compact 40 mm × 55 mm module. The bare module is 4.6 mm deep; when mounted, the total height becomes either 4.94 mm or 7.44 mm, depending on the chosen stacking height. The mechanical diagram in [Figure 4](#) illustrates the approximate shape and dimensions of CM5 as viewed from the top.

**Figure 4.**  
Mechanical specification of Raspberry Pi Compute Module 5 viewed from the top



Key mechanical specifications of CM5 are as follows:

- **Mounting.** CM5 has four M2.5 mounting holes inset 3.5 mm from the module edge.
- **Thickness.** The PCB is 1.24 mm thick ± 10%.
- **SoC height.** BCM2712 SoC measures 2.2 mm ± 0.15 mm in height, including solder balls.
- **Stacking height.** Stacking height is determined by the connector used on the carrier board:
  - Amphenol connector part number, 10164227-1001A1RLF, results in a stacking height of 1.5 mm with no clearance underneath the CM5.
  - Amphenol connector part number, 10164227-1004A1RLF, results in a stacking height of 4.0 mm with 2.5 mm clearance underneath the CM5.

# 4. 规格

本节包含CM5组件及功能的技术描述，涵盖尺寸、天线、引脚分配、电气规格及热特性。

## 4.1. 机械规格

CM5由紧凑型印刷电路板和可选的无线天线组成。CM5组件的物理特征总结于第4.1.1节“PCB尺寸”，其中包含模块尺寸、PCB厚度、SoC高度及堆叠高度选项的相关信息。天线方向及间隙要求汇总见第4.1.2节“无线天线”。

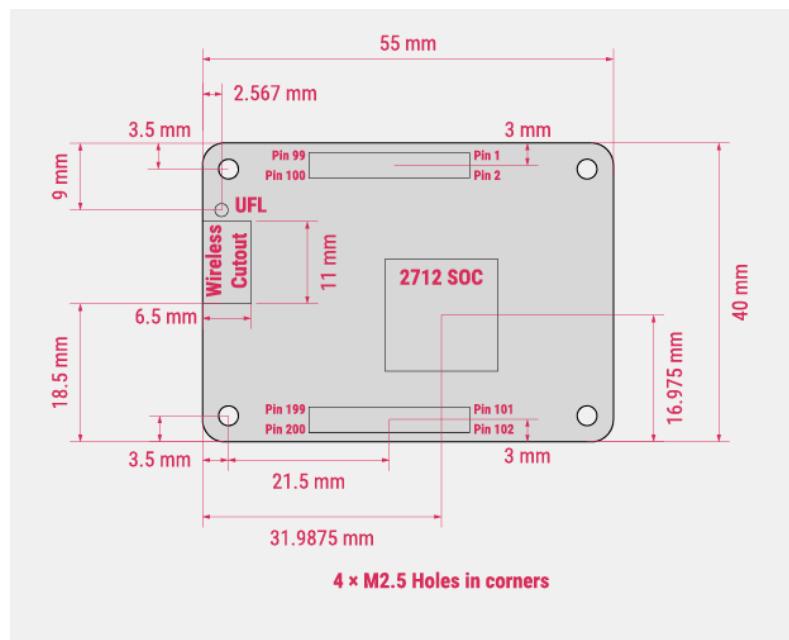
有关完整机械图纸和CAD模型，请参阅包含在官方设计数据包内的CM5设计文件。这些文件旨在帮助设计人员进行硬件可视化与规划；仅供参考，可能随电路板设计的更新或修改而变更。

### 4.1.1. 印刷电路板尺寸

CM5为一款紧凑型40 mm × 55 mm尺寸的模块。裸模块厚度为4.6 mm；安装后，根据所选堆叠高度，总高度为4.94 mm或7.44 mm。图4中的机械图示展示了从顶部视角观察CM5的大致形状与尺寸。

图4。

树莓派计算模块5的顶视机械规格



CM5的主要机械规格如下：

- 安装方式。CM5设有四个M2.5安装孔，孔距模块边缘内凹3.5 mm。
- 厚度。印刷电路板厚度为 1.24 毫米，公差  $\pm 10\%$ 。
- SoC 高度。BCM2712 SoC 高度为 2.2 毫米，公差  $\pm 0.15$  毫米（包括焊球）。
- 堆叠高度。堆叠高度取决于载板上所用连接器：
  - Amphenol 连接器零件号 10164227-1001A1RLF，堆叠高度为 1.5 毫米，CM5 下方无间隙。
  - Amphenol 连接器零件号 10164227-1004A1RLF，堆叠高度为 4.0 毫米，CM5 下方间隙为 2.5 毫米。

The location and arrangement of components on CM5 might change slightly over time due to revisions for cost and manufacturing considerations; however, the maximum component heights and PCB thickness will be kept as specified.

### 4.1.2. Wireless antenna

If using the on-board PCB antenna, we recommend adhering to the following guidelines:

- Position the on-board wireless antenna so that it faces the edge of the plastic enclosure.
- To avoid degrading wireless performance, ensure any nearby metal includes appropriate cut-outs.
- Maintain a minimum clearance of 10 mm around the PCB antenna; verify actual performance in the final enclosure.
- Don't place any metal, including ground planes, directly beneath the antenna.
- Provide a ground plane cut-out of at least 6.5 mm × 11 mm; ideally, 8 mm × 15 mm or larger.

If these requirements can't be met, wireless performance might be degraded, especially in the 2.4 GHz spectrum. We recommend using the external antenna is used where possible.

For more information about the on-board PCB antenna, see [Section 2.1. Wireless](#).

## 4.2. Pinout

CM5 includes 200 pins. Each pin is configured with default software function. [Table 4](#) provides a summary of each pin's assignment, including signal names and descriptions.

**Table 4.**  
Pinout for the Raspberry Pi Compute Module 5

Pin	Signal	Description
1	GND	Ground (0 V)
2	GND	Ground (0 V)
3	Ethernet_Pair3_P	Ethernet pair 3 positive (connect to transformer or MagJack)
4	Ethernet_Pair1_P	Ethernet pair 1 positive (connect to transformer or MagJack)
5	Ethernet_Pair3_N	Ethernet pair 3 negative (connect to transformer or MagJack)
6	Ethernet_Pair1_N	Ethernet pair 1 negative (connect to transformer or MagJack)
7	GND	Ground (0 V)
8	GND	Ground (0 V)
9	Ethernet_Pair2_N	Ethernet pair 2 negative (connect to transformer or MagJack)
10	Ethernet_Pair0_N	Ethernet pair 0 negative (connect to transformer or MagJack)
11	Ethernet_Pair2_P	Ethernet pair 2 positive (connect to transformer or MagJack)
12	Ethernet_Pair0_P	Ethernet pair 0 positive (connect to transformer or MagJack)
13	GND	Ground (0 V)
14	GND	Ground (0 V)
15	Ethernet_nLED3	Active-low Ethernet activity indicator ( <code>CM5_3.3V</code> signal): typically a green LED is connected to this pin; $I_{OL} = 8 \text{ mA}$ at $V_{OL} < 0.4 \text{ V}$
16	Fan_Tacho	Fan Tacho input pin internally pulled up with a $1.8 \text{ k}\Omega$ to <code>CM5_3.3V</code>
17	Ethernet_nLED2	Active-low Ethernet speed indicator ( <code>CM5_3.3V</code> signal): typically a yellow LED is connected to this pin; a low state indicates the 1 Gbit or 100 Mbit link: $I_{OL} = 8 \text{ mA}$ at $V_{OL} < 0.4 \text{ V}$
18	Ethernet_SYNC_OUT	IEEE1588 SYNC output pin, may be configured to be an input ( <code>CM5_3.3V</code> signal: $I_{OL} = 8 \text{ mA}$ at $V_{OL} < 0.4 \text{ V}$ )
19	Fan_PWM	Open drain output
20	EEPROM_nWP	Leave floating NB internally pulled up to <code>CM5_3.3V</code> through $100 \text{ k}\Omega$ ( $V_{IL} < 0.8 \text{ V}$ ); can be grounded to prevent writing to the on-board EEPROM that stores the boot code

由于成本和制造因素，CM5 上组件的位置和排列可能随版本略有调整；但最大组件高度及印刷电路板厚度将保持规范所述。

## 4.1.2. 无线天线

若使用板载 PCB 天线，建议遵循以下指引：

- 将板载无线天线定位，使其朝向塑料外壳的边缘。
- 为避免无线性能下降，确保附近的金属部件具有适当的开孔。
- 在印刷电路板天线周围保持至少10毫米的间距；并在最终外壳中验证实际性能。
- 不要在天线正下方放置任何金属，包括地线面。
- 至少提供6.5毫米×11毫米的地线面开孔；理想尺寸为8毫米×15毫米或更大。

如果无法满足这些要求，无线性能可能会被削弱，特别是在2.4 GHz频段。建议尽可能使用外置天线。

有关板载印刷电路板天线的更多信息，请参见第2.1节 无线。

## 4.2. 引脚分配

CM5包含200个引脚。每个引脚均配置有默认的软件功能。表4概述了每个引脚的分配情况，包括信号名称和描述。

**表 4.**

树莓派计算模块 5 引脚分配

引脚	信号	描述
1	GND	地线 (0 V)
2	GND	地线 (0 V)
3	Ethernet_Pair3_P	以太网对 3 正极 (连接至变压器或 MagJack)
4	Ethernet_Pair1_P	以太网对 1 正极 (连接至变压器或 MagJack)
5	Ethernet_Pair3_N	以太网对 3 负极 (连接至变压器或 MagJack)
6	Ethernet_Pair1_N	以太网对 1 负极 (连接至变压器或 MagJack)
7	GND	地线 (0 V)
8	GND	地线 (0 V)
9	Ethernet_Pair2_N	以太网对 2 负极 (连接至变压器或 MagJack)
10	Ethernet_Pair0_N	以太网对 0 负极 (连接至变压器或 MagJack)
11	Ethernet_Pair2_P	以太网对 2 正极 (连接至变压器或 MagJack)
12	Ethernet_Pair0_P	以太网对 0 正极 (连接至变压器或 MagJack)
13	GND	地线 (0 V)
14	GND	地线 (0 V)
15	Ethernet_nLED3	低电平以太网活动指示 ( CM5_3.3V 信号)：通常连接一个绿色 LED 于该引脚; $I_{OL} = 8 \text{ mA}$ , $V_{OL} < 0.4 \text{ V}$
16	Fan_Tacho	风扇转速输入引脚，内部上拉电阻为 $1.8 \text{ k}\Omega$ ，连接至 CM5_3.3V
17	Ethernet_nLED2	低电平有效以太网速率指示灯 ( CM5_3.3 V信号)：通常此引脚连接黄色LED；低电平表示1 Gbit或100 Mbit链路； $I_{OL} = 8 \text{ mA}$ , $V_{OL} < 0.4 \text{ V}$
18	Ethernet_SYNC_OUT	IEEE1588 SYNC输出引脚，可配置为输入 ( CM5_3.3V 信号: $I_{OL} = 8 \text{ mA}$ , $V_{OL} < 0.4 \text{ V}$ )
19	Fan_PWM	开漏输出
20	EEPROM_nWP	悬空，内部通过 CM5_3.3 V经 $100 \text{ k}\Omega$ 上拉 ( $V_{IL} < 0.8 \text{ V}$ )；可接地以防止写入存储引导代码的板载EEPROM

Pin	Signal	Description
21	LED_nACT	Active-low Pi activity LED; 20 mA max, 5 V tolerant ( $V_{OL} < 0.4$ V); this signal drives the green LED on Raspberry Pi 5
22	GND	Ground (0 V)
23	GND	Ground (0 V)
24	GPIO26	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
25	GPIO21	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
26	GPIO19	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
27	GPIO20	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
28	GPIO13	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
29	GPIO16	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
30	GPIO6	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
31	GPIO12	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
32	GND	Ground (0 V)
33	GND	Ground (0 V)
34	GPIO5	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
35	ID_SC	(RP1 GPIO 1) GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
36	ID_SD	(RP1 GPIO 0) GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
37	GPIO7	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
38	GPIO11	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
39	GPIO8	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
40	GPIO9	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
41	GPIO25	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
42	GND	Ground (0 V)
43	GND	Ground (0 V)
44	GPIO10	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
45	GPIO24	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
46	GPIO22	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
47	GPIO23	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
48	GPIO27	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
49	GPIO18	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
50	GPIO17	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
51	GPIO15	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
52	GND	Ground (0 V)
53	GND	Ground (0 V)
54	GPIO4	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
55	GPIO14	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V
56	GPIO3	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V ; internal 1.8 kΩ pull-up to GPIO_VREF
57	SD_CLK	SD card clock signal (only available on CM5Lite)
58	GPIO2	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM5_1.8V ; internal 1.8 kΩ pull-up to GPIO_VREF

引脚	信号	描述
21	LED_nACT	低电平有效Pi活动LED；最大20 mA，支持5 V耐受 ( $V_{OL} < 0.4$ V)；该信号驱动树莓派5上的绿灯
22	GND	地线 (0 V)
23	GND	地线 (0 V)
24	GPIO26	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
25	GPIO21	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
26	GPIO19	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
27	GPIO20	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
28	GPIO13	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
29	GPIO16	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
30	GPIO6	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
31	GPIO12	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
32	GND	地线 (0 V)
33	GND	地线 (0 V)
34	GPIO5	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
35	ID_SC	(RP1 GPIO 1) GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
		连接至 CM5_1.8V
36	ID_SD	(RP1 GPIO 0) GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
		连接至 CM5_1.8V
37	GPIO7	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
38	GPIO11	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
39	GPIO8	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
40	GPIO9	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
41	GPIO25	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
42	GND	地线 (0 V)
43	GND	地线 (0 V)
44	GPIO10	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
45	GPIO24	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
46	GPIO22	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
47	GPIO23	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
48	GPIO27	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
49	GPIO18	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
50	GPIO17	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
51	GPIO15	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
52	GND	地线 (0 V)
53	GND	地线 (0 V)
54	GPIO4	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
55	GPIO14	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号
56	GPIO3	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号 内部 1.8 kΩ 上拉电阻至 GPIO_VREF
57	SD_CLK	SD卡时钟信号（仅限 CM5Lite）
58	GPIO2	GPIO：通常为3.3 V信号，但可通过连接设为CM5_1.8 V信号 内部 1.8 kΩ 上拉电阻至 GPIO_VREF

Pin	Signal	Description
59	GND	Ground (0 V)
60	GND	Ground (0 V)
61	SD_DAT3	SD card/eMMC Data3 signal (only available on CM5Lite)
62	SD_CMD	SD card/eMMC Command signal (only available on CM5Lite)
63	SD_DAT0	SD card/eMMC Data0 signal (only available on CM5Lite)
64	SD_DAT5	SD card/eMMC Data5 signal (only available on CM5Lite)
65	GND	Ground (0 V)
66	GND	Ground (0 V)
67	SD_DAT1	SD card/eMMC Data1 signal (only available on CM5Lite)
68	SD_DAT4	SD card/eMMC Data4 signal (only available on CM5Lite)
69	SD_DAT2	SD card/eMMC Data2 signal (only available on CM5Lite)
70	SD_DAT7	SD card/eMMC Data7 signal (only available on CM5Lite)
71	GND	Ground (0 V)
72	SD_DAT6	SD card/eMMC Data6 signal (only available on CM5Lite)
73	SD_VDD_OVERRIDE	Connect to CM5_3.3V to force SD card/eMMC interface to 1.8 V signalling instead of 3.3 V, otherwise leave unconnected. Typically only used if external eMMC is connected.
74	GND	Ground (0 V)
75	SD_PWR_ON	Output to power switch for the SD card; CM5 sets this pin high (3.3 V) to signal that power to the SD card should be turned on; internally pulled up to CM5_3.3V with a 4.53 kΩ resistor (only available on CM5Lite)
76	VBAT	RTC battery input 2.5 V to 3.5 V; typically 3 V
77	5V (Input)	4.75 V to 5.25 V main power input
78	GPIO_VREF	Must be connected to CM5_3.3V (pins 84 and 86) for 3.3 V GPIO0-27 or CM5_1.8V (pins 88 and 90) for 1.8 V GPIO0-27 ; this pin can't be floating or connected to ground
79	5V (Input)	4.75 V to 5.25 V; main power input
80	SCL0	I2C clock pin (GPIO39); typically used for camera and display; internal 1.8 kΩ pull-up to CM5_3.3V
81	5V (Input)	4.75 V to 5.25 V; main power input
82	SDA0	I2C data pin (GPIO38); typically used for camera and display; internal 1.8 kΩ pull-up to CM5_3.3V
83	5V (Input)	4.75 V to 5.25 V; main power input
84	CM5_3.3V (Output)	3.3 V ± 5%. Power output max 300 mA per pin for a total of 600 mA; powered down during power-off or when PMIC_Enable set low
85	5V (Input)	4.75 V to 5.25 V; main power input
86	CM5_3.3V (Output)	3.3 V ± 5%. Power output max 300 mA per pin for a total of 600 mA; powered down during power-off or when PMIC_Enable set low
87	5V (Input)	4.75 V to 5.25 V; main power input
88	CM5_1.8V (Output)	1.8 V ± 5%. Power output max 300 mA per pin for a total of 600 mA; powered down during power-off or when PMIC_Enable set low
89	WL_nDisable	Can be left floating; if driven low, the Wi-Fi interface will be disabled. Internally pulled up through 1.8 kΩ to CM5_3.3V
90	CM5_1.8V (Output)	1.8 V ± 5%. Power output max 300 mA per pin for a total of 600 mA; powered down during power-off or when PMIC_Enable set low
91	BT_nDisable	Can be left floating; if driven low, the Bluetooth interface will be disabled; internally pulled up through 1.8 kΩ to CM5_3.3V
92	PWR_Button	Pull low to force power off or power on from previous software powered off state; internally pulled up to 5 V through 10 kΩ

引脚	信号	描述
59	GND	地线 (0 V)
60	GND	地线 (0 V)
61	SD_DAT3	SD卡/eMMC Data3 信号 (仅限 CM5Lite)
62	SD_CMD	SD卡/eMMC 命令信号 (仅适用于 CM5Lite)
63	SD_DAT0	SD卡/eMMC 数据0信号 (仅适用于 CM5Lite)
64	SD_DAT5	SD卡/eMMC 数据5信号 (仅适用于 CM5Lite)
65	GND	地线 (0 V)
66	GND	地线 (0 V)
67	SD_DAT1	SD卡/eMMC 数据1信号 (仅适用于 CM5Lite)
68	SD_DAT4	SD卡/eMMC 数据4信号 (仅适用于 CM5Lite)
69	SD_DAT2	SD卡/eMMC 数据2信号 (仅适用于 CM5Lite)
70	SD_DAT7	SD卡/eMMC 数据7信号 (仅适用于 CM5Lite)
71	GND	地线 (0 V)
72	SD_DAT6	SD卡/eMMC 数据6信号 (仅适用于 CM5Lite)
73	SD_VDD_OVERRIDE	连接至 CM5_3.3 V用于强制 SD卡/eMMC 接口采用 1.8 V 信号电平，非 3.3 V，否则保持悬空。通常仅在连接外部 eMMC 时使用。
74	GND	地线 (0 V)
75	SD_PWR_ON	输出至 SD卡 电源开关；CM5 将此引脚置高电平 (3.3 V)，表示应开启 SD卡 电源；内部上拉至 CM5_3.3 V 配合4.53 kΩ 电阻 (仅限 CM5Lite适用)
76	VBAT	RTC电池输入2.5 V至3.5 V；典型值为3 V
77	5V (输入)	4.75 V至5.25 V主电源输入
78	GPIO_VREF	必须连接至 CM5_3.3V (引脚84和86) 用于3.3 V GPIO0-27 或 CM5_1.8V (引脚88和90) 用于1.8 V GPIO0-27；该引脚不得悬空或接地
79	5V (输入)	4.75 V至5.25 V；主电源输入
80	SCL0	I2C时钟引脚 (GPIO39)：通常用于摄像头和显示屏；内部 1.8 kΩ 上拉电阻至 CM5_3.3V
81	5V (输入)	4.75 V至5.25 V；主电源输入
82	SDA0	I2C数据引脚 (GPIO38)：通常用于摄像头和显示屏；内部 1.8 kΩ 上拉电阻至 CM5_3.3V
83	5V (输入)	4.75 V至5.25 V；主电源输入
84	CM5_3.3V (输出)	3.3 V ± 5%。每个引脚最大输出电流为300 mA，总计600 mA；断电或在以下情况下断电；PMIC_Enable 置为低电平
85	5V (输入)	4.75 V至5.25 V；主电源输入
86	CM5_3.3V (输出)	3.3 V ± 5%。每个引脚最大输出电流为300 mA，总计600 mA；断电或在以下情况下断电；PMIC_Enable 置为低电平
87	5V (输入)	4.75 V至5.25 V；主电源输入
88	CM5_1.8V (输出)	1.8 V ± 5%。每个引脚最大输出电流为300 mA，总计600 mA；断电或在以下情况下断电；PMIC_Enable 置为低电平
89	WL_nDisable	可保持悬空；若拉低，Wi-Fi 接口将被禁用。内部通过1.8 kΩ上拉至 CM5_3.3V
90	CM5_1.8V (输出)	1.8 V ± 5%。每个引脚最大输出电流为300 mA，总计600 mA；断电或在以下情况下断电；PMIC_Enable 置为低电平
91	BT_nDisable	可保持悬空；若拉低，蓝牙接口将被禁用；内部通过1.8 kΩ上拉至 CM5_3.3V
92	PWR_Button	拉低以强制关机或从先前软件关机状态开机；通过10 kΩ电阻内部上拉至5 V

Pin	Signal	Description
93	nRPIBOOT	A low on this pin forces booting from an RPI server (for example, PC or a Raspberry Pi); if not used, leave floating; internally pulled up through 10 kΩ to CM5_3.3V
94	CC1	USB PSU PD signal; wire to a USB-C connector to enable 5 A at 5 V negotiation.
95	LED_nPWR	3.3 V signal: active-low output to drive Power On LED; this signal needs to be buffered
96	CC2	USB PSU PD signal; wire to a USB-C connector to enable 5 A at 5 V negotiation.
97	CAM_GPIO0	3.3 V signal: can be a GPIO ( GPIO34 ) or part of the bus with pin 100
98	GND	Ground (0 V)
99	PMIC_Enable	Input; drive low to power off CM5 internally pulled up with a 100 kΩ to 5 V
100	CAM_GPIO1	3.3 V signal ( GPIO35 ): internally pulled up with 15 kΩ to CM5_3.3V
101	USB_OTG_ID	Input (3.3 V signal): USB OTG pin; internally pulled up; when grounded, CM5 becomes a USB host but the correct OS driver must also be used
102	PCIe_CLK_nREQ	Input (3.3 V signal): PCIe clock request pin (low to request PCI clock); internally pulled up
103	USB_N	USB 2.0 D-
104	PCIE_nWAKE	3.3 V signal: PCIe WAKE# signal can be left unconnected if wake up isn't required; internally pulled up
105	USB_P	USB 2.0 D+
106	PCIE_PWR_EN	3.3 V signal: active high, used to signal that a PCIe device can be powered down when low
107	GND	Ground (0 V)
108	GND	Ground (0 V)
109	PCIE_nRST	Output (3.3 V signal): PCIe reset active-low
110	PCIE_CLK_P	PCIe clock-out positive (100 MHz)
111	VBUS_EN	3.3 V signal: active high to signal USB 3.0 ports should be powered
112	PCIE_CLK_N	PCIe clock out negative (100 MHz)
113	GND	Ground (0 V)
114	GND	Ground (0 V)
115	MIPI0_D0_N	MIPI0 D0 negative
116	PCIE_RX_P	Input PCIe GEN 2 RX positive NB external AC coupling capacitor required
117	MIPI0_D0_P	MIPI0 D0 positive
118	PCIE_RX_N	Input PCIe GEN 2 RX negative NB external AC coupling capacitor required
119	GND	Ground (0 V)
120	GND	Ground (0 V)
121	MIPI0_D1_N	MIPI0 D1 negative
122	PCIE_TX_P	Output PCIe GEN 2 TX positive NB AC coupling capacitor included on CM5
123	MIPI0_D1_P	MIPI0 D1 positive
124	PCIE_TX_N	Output PCIe GEN 2 TX positive NB AC coupling capacitor included on CM5
125	GND	Ground (0 V)
126	GND	Ground (0 V)
127	MIPI0_C_N	MIPI0 clock negative
128	USB3-0-RX_N	USB 3.0 port 0 RX input negative
129	MIPI0_C_P	MIPI0 clock positive
130	USB3-0-RX_P	USB 3.0 port 0 RX input positive
131	GND	Ground (0 V)
132	GND	Ground (0 V)

引脚	信号	描述
93	nRPIBOOT	该引脚低电平时强制从RPI服务器（例如PC或树莓派）启动；若不使用，请保持悬空；内部通过10 kΩ电阻上拉至 CM5_3.3V
94	CC1	USB电源供应单元PD信号；连接到USB-C接口以启用5A, 5V电压协商。
95	LED_nPWR	3.3V信号：低电平有效输出，用于驱动电源指示灯；该信号需要经过缓冲。
96	CC2	USB电源供应单元PD信号；连接到USB-C接口以启用5A, 5V电压协商。
97	CAM_GPIO0	3.3V信号：可作为GPIO（GPIO34）或总线的一部分，与引脚100相连
98	GND	地线(0V)
99	PMIC_Enable	输入；拉低信号可关闭CM5，内部通过100 kΩ上拉至5V。
100	CAM_GPIO1	3.3V信号（GPIO35）：内部通过15 kΩ上拉至 CM5_3.3V
101	USB_OTG_ID	输入(3.3V信号)：USB OTG引脚；内部上拉；接地时，CM5作为USB主机。但必须使用正确的操作系统驱动程序。
102	PCIe_CLK_nREQ	输入(3.3V信号)：PCIe时钟请求引脚(拉低请求PCI时钟)；内部上拉。
103	USB_N	USB 2.0 D-
104	PCIE_nWAKE	3.3V信号：PCIe WAKE#信号，如不需要唤醒功能可不连接；内部上拉。
105	USB_P	USB 2.0 D+
106	PCIE_PWR_EN	3.3V信号：高电平有效，表示PCIe设备在低电平时可以断电
107	GND	地线(0V)
108	GND	地线(0V)
109	PCIe_nRST	输出(3.3V信号)：PCIe复位，低电平有效
110	PCIe_CLK_P	PCIe时钟输出正极(100MHz)
111	VBUS_EN	3.3V信号：高电平有效，表示USB 3.0端口应通电
112	PCIe_CLK_N	PCIe时钟输出负极(100MHz)
113	GND	地线(0V)
114	GND	地线(0V)
115	MIPI0_D0_N	MIPI0 D0负极
116	PCIe_RX_P	输入PCIe代2RX正极，注意需外接交流耦合电容
117	MIPI0_D0_P	MIPI0 D0正极
118	PCIe_RX_N	输入PCIe代2RX负极，注意需外接交流耦合电容
119	GND	地线(0V)
120	GND	地线(0V)
121	MIPI0_D1_N	MIPI0 D1负极
122	PCIe_TX_P	输出PCIe代2TX正极，CM5已包含交流耦合电容
123	MIPI0_D1_P	MIPI0 D1正极
124	PCIe_TX_N	输出PCIe代2TX正极，CM5已包含交流耦合电容
125	GND	地线(0V)
126	GND	地线(0V)
127	MIPI0_C_N	MIPI0时钟负极
128	USB3-0-RX_N	USB 3.0端口0RX输入负极
129	MIPI0_C_P	MIPI0时钟正极
130	USB3-0-RX_P	USB 3.0端口0RX输入正极
131	GND	地线(0V)
132	GND	地线(0V)

Pin	Signal	Description
133	MIPI0_D2_N	MIPI0 D2 negative
134	USB3-0-DP	USB 3.0 port 0 DP
135	MIPI0_D2_P	MIPI0 D2 positive
136	USB3-0-DM	USB 3.0 port 0 DM
137	GND	Ground (0 V)
138	GND	Ground (0 V)
139	MIPI0_D3_N	MIPI0 D3 negative
140	USB3-0-TX_N	USB 3.0 port 0 TX output negative NB AC coupling capacitor included on CM5
141	MIPI0_D3_P	MIPI0 D3 positive
142	USB3-0-TX_P	USB 3.0 port 0 TX output positive NB AC coupling capacitor included on CM5
143	HDMI1_HOTPLUG	Input HDMI1 hotplug; internally pulled down with a 100 kΩ. 5 V tolerant. Can be connected directly to a HDMI connector.
144	GND	Ground (0 V)
145	HDMI1_SDA	Bidirectional HDMI1 SDA; internally pulled up with a 1.8 kΩ. 5 V tolerant; can be connected directly to a HDMI connector
146	HDMI1_TX2_P	Output HDMI1 TX2 positive
147	HDMI1_SCL	Bidirectional HDMI1 SCL; internally pulled up with a 1.8 kΩ. 5 V tolerant; can be connected directly to a HDMI connector
148	HDMI1_TX2_N	Output HDMI1 TX2 negative
149	HDMI1_CEC	Input HDMI1 CEC; internally pulled up with a 27 kΩ. 5 V tolerant; can be connected directly to a HDMI connector
150	GND	Ground (0 V)
151	HDMI0_CEC	Input HDMI0 CEC; internally pulled up with a 27 kΩ. 5 V tolerant; can be connected directly to a HDMI connector
152	HDMI1_TX1_P	Output HDMI1 TX1 positive
153	HDMI0_HOTPLUG	Input HDMI0 hotplug; internally pulled down 100 kΩ. 5 V tolerant; can be connected directly to a HDMI connector
154	HDMI1_TX1_N	Output HDMI1 TX1 negative
155	GND	Ground (0 V)
156	GND	Ground (0 V)
157	USB3-1-RX_N	USB 3.0 port 1 RX input negative
158	HDMI1_TX0_P	Output HDMI1 TX0 positive
159	USB3-1-RX_P	USB 3.0 port 1 RX input positive
160	HDMI1_TX0_N	Output HDMI1 TX0 negative
161	GND	Ground (0 V)
162	GND	Ground (0 V)
163	USB3-1-DP	USB 3.0 port 1 DP
164	HDMI1_CLK_P	Output HDMI1 clock positive
165	USB3-1-DM	USB 3.0 port 1 DM
166	HDMI1_CLK_N	Output HDMI1 clock negative
167	GND	Ground (0 V)
168	GND	Ground (0 V)
169	USB3-1-TX_N	USB 3.0 Port 1 TX output negative NB AC coupling capacitor included on CM5

引脚	信号	描述
133	MIPI0_D2_N	MIPI0 D2 负极
134	USB3-0-DP	USB 3.0 端口 0 DP
135	MIPI0_D2_P	MIPI0 D2 正极
136	USB3-0-DM	USB 3.0 端口 0 DM
137	GND	地线 (0 V)
138	GND	地线 (0 V)
139	MIPI0_D3_N	MIPI0 D3 负极
140	USB3-0-TX_N	USB 3.0 端口 0 TX 输出负极, CM5 上包含 NB 交流耦合电容
141	MIPI0_D3_P	MIPI0 D3 正极
142	USB3-0-TX_P	USB 3.0 端口 0 TX 输出正极, CM5 上包含 NB 交流耦合电容
143	HDMI1_HOTPLUG	输入 HDMI1 热插拔信号; 内部带有 100 kΩ 下拉电阻。耐受 5 V。可直接连接至 HDMI 接口。
144	GND	地线 (0 V)
145	HDMI1_SDA	双向 HDMI1 SDA; 内部带有 1.8 kΩ 上拉电阻。耐受 5 V; 可直接连接至 HDMI 连接器
146	HDMI1_TX2_P	输出 HDMI1 TX2 正极
147	HDMI1_SCL	双向 HDMI1 SCL; 内部带有 1.8 kΩ 上拉电阻。耐受 5 V; 可直接连接至 HDMI 连接器
148	HDMI1_TX2_N	输出 HDMI1 TX2 负极
149	HDMI1_CEC	输入 HDMI1 CEC; 内部上拉 27 kΩ, 支持 5 V 容忍; 可直接连接至 HDMI 连接器
150	GND	地线 (0 V)
151	HDMI0_CEC	输入 HDMI0 CEC; 内部上拉 27 kΩ, 支持 5 V 容忍; 可直接连接至 HDMI 连接器
152	HDMI1_TX1_P	输出 HDMI1 TX1 正极
153	HDMI0_HOTPLUG	输入 HDMI0 热插拔; 内部下拉 100 kΩ, 支持 5 V 容忍; 可直接连接至 HDMI 连接器
154	HDMI1_TX1_N	输出 HDMI1 TX1 负极
155	GND	地线 (0 V)
156	GND	地线 (0 V)
157	USB3-1-RX_N	USB 3.0 端口 1 RX 输入负极
158	HDMI1_TX0_P	输出 HDMI1 TX0 正极
159	USB3-1-RX_P	USB 3.0 端口 1 RX 输入正极
160	HDMI1_TX0_N	输出 HDMI1 TX0 负极
161	GND	地线 (0 V)
162	GND	地线 (0 V)
163	USB3-1-DP	USB 3.0 端口 1 DP
164	HDMI1_CLK_P	输出 HDMI1 时钟正端
165	USB3-1-DM	USB 3.0 端口 1 DM
166	HDMI1_CLK_N	输出 HDMI1 时钟负端
167	GND	地线 (0 V)
168	GND	地线 (0 V)
169	USB3-1-TX_N	USB 3.0 端口 1 TX 输出负端, CM5 上包含 NB AC 耦合电容

Pin	Signal	Description
170	HDMI0_TX2_P	Output HDMI0 TX2 positive
171	USB3-1-TX_P	USB 3.0 Port 1 TX output positive NB AC coupling capacitor included on CM5
172	HDMI0_TX2_N	Output HDMI0 TX2 negative
173	GND	Ground (0 V)
174	GND	Ground (0 V)
175	MIPI1_D0_N	MIPI1 D0 negative
176	HDMI0_TX1_P	Output HDMI0 TX1 positive
177	MIPI1_D0_P	MIPI1 D0 positive
178	HDMI0_TX1_N	Output HDMI0 TX1 negative
179	GND	Ground (0 V)
180	GND	Ground (0 V)
181	MIPI1_D1_N	MIPI1 D1 negative
182	HDMI0_TX0_P	Output HDMI0 TX0 positive
183	MIPI1_D1_P	MIPI1 D1 positive
184	HDMI0_TX0_N	Output HDMI0 TX0 negative
185	GND	Ground (0 V)
186	GND	Ground (0 V)
187	MIPI1_C_N	MIPI1 clock negative
188	HDMI0_CLK_P	Output HDMI0 clock positive
189	MIPI1_C_P	MIPI1 clock positive
190	HDMI0_CLK_N	Output HDMI0 clock negative
191	GND	Ground (0 V)
192	GND	Ground (0 V)
193	MIPI1_D2_N	MIPI1 D2 negative
194	MIPI1_D3_N	MIPI1 D3 negative
195	MIPI1_D2_P	MIPI1 D2 positive
196	MIPI1_D3_P	MIPI1 D3 positive
197	GND	Ground (0 V)
198	GND	Ground (0 V)
199	HDMI0_SDA	Bidirectional HDMI0 SDA; internally pulled up with a 1.8 kΩ. 5 V tolerant; can be connected directly to an HDMI connector
200	HDMI0_SCL	Bidirectional HDMI0 SCL; internally pulled up with a 1.8 kΩ. 5 V tolerant; can be connected directly to an HDMI connector

### 4.2.1. Pin guidelines

The following instructions provide guidance for grounding, connector usage, voltage limits, and power rail considerations, and precautions against improper voltage application.

- **Grounding.** Always connect all ground pins on any connector in use. If none of the signals on the second connector (pins 101 to 200) are in use, then you may omit the connector (including its ground pins) to reduce costs; however, omitting the second connector can affect mechanical stability.
- **GPIO voltage limits.** GPIO pins 0 to 27 are the same as the 40-pin connector on Raspberry Pi 5. Depending on your signalling, their voltage must not exceed:
  - 3.3 V ( CM5\_3.3V ) when using 3.3 V signalling.

引脚	信号	描述
170	HDMI0_TX2_P	输出 HDMI0 TX2 正端
171	USB3-1-TX_P	USB 3.0 端口 1 TX 输出正端, CM5 上包含 NB AC 耦合电容
172	HDMI0_TX2_N	输出 HDMI0 TX2 负端
173	GND	地线 (0 V)
174	GND	地线 (0 V)
175	MIPI1_D0_N	MIPI1 D0 负端
176	HDMI0_TX1_P	输出 HDMI0 TX1 正端
177	MIPI1_D0_P	MIPI1 D0 正端
178	HDMI0_TX1_N	输出 HDMI0 TX1 负端
179	GND	地线 (0 V)
180	GND	地线 (0 V)
181	MIPI1_D1_N	MIPI1 D1 负端
182	HDMI0_TX0_P	输出 HDMI0 TX0 正端
183	MIPI1_D1_P	MIPI1 D1 正端
184	HDMI0_TX0_N	输出 HDMI0 TX0 负极
185	GND	地线 (0 V)
186	GND	地线 (0 V)
187	MIPI1_C_N	MIPI1 时钟负极
188	HDMI0_CLK_P	输出 HDMI0 时钟正极
189	MIPI1_C_P	MIPI1 时钟正极
190	HDMI0_CLK_N	输出 HDMI0 时钟负极
191	GND	地线 (0 V)
192	GND	地线 (0 V)
193	MIPI1_D2_N	MIPI1 D2 负极
194	MIPI1_D3_N	MIPI1 D3 负极
195	MIPI1_D2_P	MIPI1 D2 正极
196	MIPI1_D3_P	MIPI1 D3 正极
197	GND	地线 (0 V)
198	GND	地线 (0 V)
199	HDMI0_SDA	双向 HDMI0 SDA; 内部带有 $1.8\text{ k}\Omega$ 上拉电阻。耐受 5 V; 可直接连接至 HDMI 接口
200	HDMI0_SCL	双向 HDMI0 SCL; 内部带有 $1.8\text{ k}\Omega$ 上拉电阻。耐受 5 V; 可直接连接至 HDMI 接口

### 4.2.1. 引脚使用准则

以下说明针对接地、连接器使用、电压限制、电源轨注意事项及防止不当电压应用提供指导。

- **接地。** 应始终连接所使用连接器上的所有地线引脚。如第二连接器（引脚 101 至 200）上的信号未使用，可省略该连接器（含其地线引脚）以降低成本；但省略第二连接器可能影响机械稳定性。
- **GPIO 电压限制。** GPIO 引脚 0 至 27 与树莓派 5 的 40 针连接器相同。根据您的信号类型，其电压不得超过：
  - 3.3 V ( CM5\_3.3V )，当使用 3.3 V 信号时。

- 1.8 V ( `CM5_1.8V` ) when using 1.8 V signalling.
- **Power rails.** If you use power rails `CM5_3.3V` or `CM5_1.8V` to supply devices other than the GPIO reference voltage (`GPIO_VREF`), you must design for safe behaviour during unexpected power loss (for example, the 5 V line falls below 4.5 V):
  - If you use the 1.8 V rail ( `CM5_1.8V` ), ensure that the current draw goes down to zero (no load) if power suddenly drops.
  - If you use the 3.3 V rail ( `CM5_3.3V` ), ensure that the 3.3 V rail voltage never falls below the 1.8 V rail voltage if power suddenly drops. The 3.3 V rail voltage usually stays above the 1.8 V rail voltage during power-down, but verify your design. If the 3.3 V rail does fall below 1.8 V, add circuitry to disconnect 3.3 V devices to prevent damage.
- **Reverse voltage.** Don't apply reverse voltage on any pin. This means that when CM5 is powered-down or off, there must be no external voltage applied to any pin, otherwise CM5 might not power up again.

## 4.2.2. Differential pairs

We recommend that positive and negative (P/N) signals within a differential pair are length-matched to within 0.15 mm. Depending on the interface, the matching tolerance can be more relaxed between different pairs. For example, HDMI pair-to-pair matching can typically be within 25 mm, so no extra matching is required on a typical board.

### 100 Ω differential pair signal lengths

All 100 Ω differential pairs on CM5 are length-matched to less than 0.05 mm for P/N signals. We recommend that pairs are also matched on the interface board. On CM5, pair-to-pair length matching isn't always maintained because many interfaces don't require precise matching between different pairs. [Table 5](#) lists the track-length differences within each differential pair group on CM5. A non-zero value represents how much longer in millimetres (mm) that track is when compared to the signal with zero length difference in the group.

**Table 5.**

100 Ω differential pair signal lengths

Signal	Length
<b>MIPI0</b>	
MIPI0_C_N	0.78
MIPI0_C_P	0.78
MIPI0_D0_N	0.01
MIPI0_D0_P	0.02
MIPI0_D1_N	0.4
MIPI0_D1_P	0.4
MIPI0_D2_N	0.04
MIPI0_D2_P	0.03
MIPI0_D3_N	0.01
MIPI0_D3_P	0
<b>MIPI1</b>	
MIPI1_C_N	1.28
MIPI1_C_P	1.27
MIPI1_D0_N	0
MIPI1_D0_P	0
MIPI1_D1_N	1.06
MIPI1_D1_P	1.05
MIPI1_D2_N	0.83
MIPI1_D2_P	0.84
MIPI1_D3_N	3.79
MIPI1_D3_P	3.79
<b>HDMI0</b>	

- 1.8 V ( CM5\_1.8V )，当使用 1.8 V 信号时。
- **电源轨。**如果您使用电源轨 CM5\_3.3V 或 CM5\_1.8V 为除 GPIO 参考电压外的设备供电，( GPIO\_VREF )，必须设计以确保在意外断电时安全运行（例如，当 5 V 线路电压低于 4.5 V）：
  - 如果您使用 1.8 V 轨 ( CM5\_1.8V )，确保在电源突然断电时电流降为零（无负载）。
  - 如果您使用 3.3 V 轨 ( CM5\_3.3V )，确保在电源突然断电时，3.3 V 轨电压不低于 1.8 V 轨电压。3.3 V 轨电压在断电时通常会保持高于 1.8 V 轨电压，但请务必验证您的设计。如若 3.3 V 轨电压低于 1.8 V，应增加断开 3.3 V 设备电源的电路，以防止损坏。
- **反向电压。**请勿对任何引脚施加反向电压。这意味着当 CM5 断电或关闭时，任何引脚上不得施加外部电压，否则 CM5 可能无法重新启动。

## 4.2.2. 差分对

我们建议差分对中的正负 (P/N) 信号长度匹配控制在 0.15 毫米以内。根据接口类型，不同差分对之间的匹配公差可以更宽松。例如，HDMI 差分对之间的匹配通常可达 25 毫米，因此在典型电路板上无需额外匹配。

### 100 Ω 差分对信号长度

CM5 上所有 100 Ω 差分对的 P/N 信号长度误差均小于 0.05 毫米。我们建议接口板上的差分对也应保持长度匹配。在 CM5 上，不同差分对之间的长度匹配并非始终保持，因为许多接口不要求不同差分对之间的精确匹配。表 5 列出了 CM5 上每组差分对中信号轨迹长度的差异。非零值表示该轨迹相比组内长度差为零的信号轨迹的长度差（单位：毫米）。

**表 5.**

100 Ω 差分对信号长度

信号	长度
<b>MIPI0</b>	
MIPI0_C_N	0.78
MIPI0_C_P	0.78
MIPI0_D0_N	0.01
MIPI0_D0_P	0.02
MIPI0_D1_N	0.4
MIPI0_D1_P	0.4
MIPI0_D2_N	0.04
MIPI0_D2_P	0.03
MIPI0_D3_N	0.01
MIPI0_D3_P	0
<b>MIPI1</b>	
MIPI1_C_N	1.28
MIPI1_C_P	1.27
MIPI1_D0_N	0
MIPI1_D0_P	0
MIPI1_D1_N	1.06
MIPI1_D1_P	1.05
MIPI1_D2_N	0.83
MIPI1_D2_P	0.84
MIPI1_D3_N	3.79
MIPI1_D3_P	3.79
<b>HDMI0</b>	

Signal	Length
HDMI0_CLK_N	0.91
HDMI0_CLK_P	0.91
HDMI0_TX0_N	0.18
HDMI0_TX0_P	0.18
HDMI0_TX1_N	0
HDMI0_TX1_P	0
HDMI0_TX2_N	0.25
HDMI0_TX2_P	0.25
<b>HDMI1</b>	
HDMI1_CLK_N	2.99
HDMI1_CLK_P	2.99
HDMI1_TX0_N	4.76
HDMI1_TX0_P	4.75
HDMI1_TX1_N	5.18
HDMI1_TX1_P	5.18
HDMI1_TX2_N	0
HDMI1_TX2_P	0
<b>Ethernet</b>	
Ethernet_Pair0_P	2.92
Ethernet_Pair0_N	2.93
Ethernet_Pair1_P	0
Ethernet_Pair1_N	0
Ethernet_Pair2_P	0.59
Ethernet_Pair2_N	0.60
Ethernet_Pair3_P	0.38
Ethernet_Pair3_N	0.38

## 90 Ω differential pair signal lengths

All 90 Ω differential pairs on CM5 (including USB pairs) are length-matched to less than 0.01 mm for P/N signals. USB 3.0 pairs don't require pair-to-pair matching within a port group. We recommend that pairs are also matched on the interface board. On CM5, pair-to-pair length matching isn't always maintained because many interfaces don't require precise matching between different pairs. [Table 6](#) lists the track-length differences within each differential pair group on CM5. A non-zero value represents how much longer in millimetres (mm) that track is when compared to the signal with zero length difference in the group.

**Table 6.**

*90 Ω differential pair signal lengths*

Signal	Length
PCIe_CLK_P	0.00
PCIe_CLK_N	0.01
PCIe_TX_P	3.71
PCIe_TX_N	3.72
PCIe_RX_P	0.84
PCIe_RX_N	0.84

信号	长度
HDMI0_CLK_N	0.91
HDMI0_CLK_P	0.91
HDMI0_TX0_N	0.18
HDMI0_TX0_P	0.18
HDMI0_TX1_N	0
HDMI0_TX1_P	0
HDMI0_TX2_N	0.25
HDMI0_TX2_P	0.25
<b>HDMI1</b>	
HDMI1_CLK_N	2.99
HDMI1_CLK_P	2.99
HDMI1_TX0_N	4.76
HDMI1_TX0_P	4.75
HDMI1_TX1_N	5.18
HDMI1_TX1_P	5.18
HDMI1_TX2_N	0
HDMI1_TX2_P	0
<b>以太网</b>	
Ethernet_Pair0_P	2.92
Ethernet_Pair0_N	2.93
Ethernet_Pair1_P	0
Ethernet_Pair1_N	0
Ethernet_Pair2_P	0.59
Ethernet_Pair2_N	0.60
Ethernet_Pair3_P	0.38
Ethernet_Pair3_N	0.38

### 90 Ω 差分对信号长度

CM5 上所有 90 Ω 差分对（包括 USB 差分对）在 P/N 信号上长度匹配误差均小于 0.01 毫米。USB 3.0 差分对在端口组内不要求对间长度匹配。我们建议接口板上的差分对也应保持长度匹配。在 CM5 上，不同差分对之间的长度匹配并非始终保持，因为许多接口不要求不同差分对之间的精确匹配。表 6 列出了 CM5 上各差分对组内轨迹长度的差异。非零值表示该轨迹比组内零长度差信号轨迹多出的毫米数（mm）。

**表 6.**  
90 Ω 差分对信号长度

信号	长度
PCIe_CLK_P	0.00
PCIe_CLK_N	0.01
PCIe_TX_P	3.71
PCIe_TX_N	3.72
PCIe_RX_P	0.84
PCIe_RX_N	0.84

## 4.3. Electrical specifications

For safe and reliable operation of CM5, observe the following electrical parameters and limitations.

### 4.3.1. Absolute maximum ratings

#### Warning

Stresses above those listed in [Table 7](#) can cause permanent damage to the device. This is a stress rating only; functional operation of the device under these or any other conditions above those listed in the operational sections of this specification isn't implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

[Table 7](#) lists the absolute maximum ratings for key voltage parameters on the CM5. These values represent the limits beyond which damage to the device can occur and shouldn't be exceeded.

**Table 7.**

Absolute maximum ratings

Symbol	Parameter	Minimum	Maximum	Unit
$V_{IN}$	5 V input voltage	-0.5	6.0	V
$V_{GPIO\_VREF}$	GPIO voltage	-0.5	3.6	V
$V_{gpio}$	GPIO input voltage	-0.5	$V_{GPIO\_VREF} + 0.5$	V

$V_{GPIO\_VREF}$  is the GPIO bank voltage, which must be tied to either the 3.3 V or the 1.8 V rail of CM5.

### 4.3.2. DC characteristics

[Table 8](#) details the DC electrical characteristics of the GPIO pins on CM5. It describes how the GPIO pins perform under different conditions (such as different reference voltages) and provides the expected ranges for each parameter (minimum, typical, and maximum values). For the electrical details of other interfaces in CM5, see [Section 2. Interfaces](#).

**Table 8.**

DC characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{IL(gpio)}$	Input low voltage	$V_{GPIO\_VREF} = 3.3 \text{ V}$	0	-	0.8	V
$V_{IH(gpio)}$	Input high voltage	$V_{GPIO\_VREF} = 3.3 \text{ V}$	2.0	-	$V_{GPIO\_VREF}$	V
$V_{IL(gpio)}$	Input low voltage	$V_{GPIO\_VREF} = 2.5 \text{ V}$	0	-	0.7	V
$V_{IH(gpio)}$	Input high voltage	$V_{GPIO\_VREF} = 2.5 \text{ V}$	1.7	-	$V_{GPIO\_VREF}$	V
$V_{IL(gpio)}$	Input low voltage	$V_{GPIO\_VREF} = 1.8 \text{ V}$	0	-	$0.35 * V_{GPIO\_VREF}$	V
$V_{IH(gpio)}$	Input high voltage	$V_{GPIO\_VREF} = 1.8 \text{ V}$	$0.65 * V_{GPIO\_VREF}$	-	$V_{GPIO\_VREF}$	V
$I_{IL(gpio)}$	Input leakage current	$V_{GPIO\_VREF} = 3.3 \text{ V}$	-	-	3	$\mu\text{A}$
$I_{IL(gpio)}$	Input leakage current	$V_{GPIO\_VREF} = 2.5 \text{ V}$	-	-	5	$\mu\text{A}$
$I_{IL(gpio)}$	Input leakage current	$V_{GPIO\_VREF} = 1.8 \text{ V}$	-	-	7	$\mu\text{A}$
$V_{OL(gpio)}$	Output low voltage	-	-	-	0.4	V
$V_{OH(gpio)}$	Output high voltage	$V_{GPIO\_VREF} = 3.3 \text{ V}$	$V_{GPIO\_VREF} - 0.4$	-	-	V
$V_{OH(gpio)}$	Output high voltage	$V_{GPIO\_VREF} = 2.5 \text{ V}$	$V_{GPIO\_VREF} - 0.5$	-	-	V
$V_{OH(gpio)}$	Output high voltage	$V_{GPIO\_VREF} = 1.8 \text{ V}$	$V_{GPIO\_VREF} - 0.4$	-	-	V
$I_{OL(gpio)}$	Output current	$2 \text{ mA}, V_{GPIO\_VREF} = 3.3 \text{ V}$	6.1	9.6	13.5	$\text{mA}$
$I_{OL(gpio)}$	Output current	$4 \text{ mA}, V_{GPIO\_VREF} = 3.3 \text{ V}$	9.2	14.3	20.2	$\text{mA}$
$I_{OL(gpio)}$	Output current	$8 \text{ mA}, V_{GPIO\_VREF} = 3.3 \text{ V}$	15.3	23.9	33.7	$\text{mA}$

## 4.3. 电气规格

为确保 CM5 的安全可靠运行, 请遵守以下电气参数和限制。

### 4.3.1. 绝对最大额定值

#### 警告

超过表 7 所列应力等级可能导致器件永久损坏。该数值仅为应力极限; 不表示器件在本规范操作部分以外的任何条件下均可正常工作。长期暴露在绝对最大额定值条件下可能会影响器件的可靠性。

表7列出了CM5关键电压参数的绝对最大额定值。这些数值代表设备可能受损的极限, 严禁超出。

表7。

绝对最大额定值

符号	参数	最小值	最大值	单位
$V_{IN}$	5 V 输入电压	-0.5	6.0	V
$V_{GPIO\_VREF}$	GPIO 电压	-0.5	3.6	V
$V_{gpio}$	GPIO 输入电压	-0.5	$V_{GPIO\_VREF} + 0.5$	V

$V_{GPIO\_VREF}$  是 GPIO 组电压, 必须连接至 CM5 的 3.3 v 或 1.8 v 电源轨之一。

### 4.3.2. 直流特性

表 8 详细说明了 CM5 上 GPIO 引脚的直流电气特性。它描述了 GPIO 引脚在不同条件 (例如不同参考电压) 下的性能表现, 并提供了各项参数的预期范围 (最小值、典型值和最大值)。有关 CM5 其他接口的电气详细信息, 请参见第 2 节 “接口”。

表 8。

直流特性

符号	参数	条件	最小值	典型值	最大值	单位
$V_{IL(gpio)}$	输入低电压	$V_{GPIO\_VREF} = 3.3 \text{ V}$	0	-	0.8	V
$V_{IH(gpio)}$	输入高电压	$V_{GPIO\_VREF} = 3.3 \text{ V}$	2.0	-	$V_{GPIO\_VREF}$	V
$V_{IL(gpio)}$	输入低电压	$V_{GPIO\_VREF} = 2.5 \text{ V}$	0	-	0.7	V
$V_{IH(gpio)}$	输入高电压	$V_{GPIO\_VREF} = 2.5 \text{ V}$	1.7	-	$V_{GPIO\_VREF}$	V
$V_{IL(gpio)}$	输入低电压	$V_{GPIO\_VREF} = 1.8 \text{ V}$	0	-	$0.35 * V_{GPIO\_VREF}$	V
$V_{IH(gpio)}$	输入高电压	$V_{GPIO\_VREF} = 1.8 \text{ V}$	$0.65 * V_{GPIO\_VREF}$	-	$V_{GPIO\_VREF}$	V
$I_{IL(gpio)}$	输入漏电流	$V_{GPIO\_VREF} = 3.3 \text{ V}$	-	-	3	$\mu\text{A}$
$I_{IL(gpio)}$	输入漏电流	$V_{GPIO\_VREF} = 2.5 \text{ V}$	-	-	5	$\mu\text{A}$
$I_{IL(gpio)}$	输入漏电流	$V_{GPIO\_VREF} = 1.8 \text{ V}$	-	-	7	$\mu\text{A}$
$V_{OL(gpio)}$	输出低电压	-	-	-	0.4	V
$V_{OH(gpio)}$	输出高电压	$V_{GPIO\_VREF} = 3.3 \text{ V}$	$V_{GPIO\_VREF} - 0.4$	-	-	V
$V_{OH(gpio)}$	输出高电压	$V_{GPIO\_VREF} = 2.5 \text{ V}$	$V_{GPIO\_VREF} - 0.5$	-	-	V
$V_{OH(gpio)}$	输出高电压	$V_{GPIO\_VREF} = 1.8 \text{ V}$	$V_{GPIO\_VREF} - 0.4$	-	-	V
$I_{OL(gpio)}$	输出电流	$2 \text{ mA}, V_{GPIO\_VREF} = 3.3 \text{ V}$	6.1	9.6	13.5	$\text{mA}$
$I_{OL(gpio)}$	输出电流	$4 \text{ mA}, V_{GPIO\_VREF} = 3.3 \text{ V}$	9.2	14.3	20.2	$\text{mA}$
$I_{OL(gpio)}$	输出电流	$8 \text{ mA}, V_{GPIO\_VREF} = 3.3 \text{ V}$	15.3	23.9	33.7	$\text{mA}$

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$I_{OL(gpio)}$	Output current	$12 \text{ mA}, V_{GPIO\_VREF} = 3.3 \text{ V}$	18.4	28.7	40.5	mA
$I_{OH(gpio)}$	Output current	$2 \text{ mA}, V_{GPIO\_VREF} = 3.3 \text{ V}$	4.5	6.3	8.4	mA
$I_{OH(gpio)}$	Output current	$4 \text{ mA}, V_{GPIO\_VREF} = 3.3 \text{ V}$	6.8	9.5	12.6	mA
$I_{OH(gpio)}$	Output current	$8 \text{ mA}, V_{GPIO\_VREF} = 3.3 \text{ V}$	11.4	15.8	21	mA
$I_{OH(gpio)}$	Output current	$12 \text{ mA}, V_{GPIO\_VREF} = 3.3 \text{ V}$	13.6	19	25.2	mA
$I_{OL(gpio)}$	Output current	$2 \text{ mA}, V_{GPIO\_VREF} = 2.5 \text{ V}$	4.7	8	12.2	mA
$I_{OL(gpio)}$	Output current	$4 \text{ mA}, V_{GPIO\_VREF} = 2.5 \text{ V}$	7.1	12	18.2	mA
$I_{OL(gpio)}$	Output current	$8 \text{ mA}, V_{GPIO\_VREF} = 2.5 \text{ V}$	11.8	20	30.4	mA
$I_{OL(gpio)}$	Output current	$12 \text{ mA}, V_{GPIO\_VREF} = 2.5 \text{ V}$	14.1	24	36.4	mA
$I_{OH(gpio)}$	Output current	$2 \text{ mA}, V_{GPIO\_VREF} = 2.5 \text{ V}$	3.5	5.1	7	mA
$I_{OH(gpio)}$	Output current	$4 \text{ mA}, V_{GPIO\_VREF} = 2.5 \text{ V}$	5.2	7.6	10.5	mA
$I_{OH(gpio)}$	Output current	$8 \text{ mA}, V_{GPIO\_VREF} = 2.5 \text{ V}$	8.7	12.7	17.6	mA
$I_{OH(gpio)}$	Output current	$12 \text{ mA}, V_{GPIO\_VREF} = 2.5 \text{ V}$	10.4	15.2	21.1	mA
$I_{OL(gpio)}$	Output current	$2 \text{ mA}, V_{GPIO\_VREF} = 1.8 \text{ V}$	4.4	8.1	13.6	mA
$I_{OL(gpio)}$	Output current	$4 \text{ mA}, V_{GPIO\_VREF} = 1.8 \text{ V}$	8.8	16.3	27.2	mA
$I_{OL(gpio)}$	Output current	$8 \text{ mA}, V_{GPIO\_VREF} = 1.8 \text{ V}$	11.8	21.7	36.3	mA
$I_{OL(gpio)}$	Output current	$12 \text{ mA}, V_{GPIO\_VREF} = 1.8 \text{ V}$	16.2	29.2	49.9	mA
$I_{OH(gpio)}$	Output current	$2 \text{ mA}, V_{GPIO\_VREF} = 1.8 \text{ V}$	3.4	5.3	7.7	mA
$I_{OH(gpio)}$	Output current	$4 \text{ mA}, V_{GPIO\_VREF} = 1.8 \text{ V}$	6.9	10.5	15.4	mA
$I_{OH(gpio)}$	Output current	$8 \text{ mA}, V_{GPIO\_VREF} = 1.8 \text{ V}$	9.1	14	20.6	mA
$I_{OH(gpio)}$	Output current	$12 \text{ mA}, V_{GPIO\_VREF} = 1.8 \text{ V}$	12.6	19.3	28.3	mA
$R_{PU(gpio)}$	Pull-up resistor	$V_{GPIO\_VREF} = 3.3 \text{ V}$	37	55	86	kΩ
$R_{PD(gpio)}$	Pull-down resistor	$V_{GPIO\_VREF} = 3.3 \text{ V}$	35	55	98	kΩ
$R_{PU(gpio)}$	Pull-up resistor	$V_{GPIO\_VREF} = 2.5 \text{ V}$	49	77	123	kΩ
$R_{PD(gpio)}$	Pull-down resistor	$V_{GPIO\_VREF} = 2.5 \text{ V}$	49	84	155	kΩ
$R_{PU(gpio)}$	Pull-up resistor	$V_{GPIO\_VREF} = 1.8 \text{ V}$	38	64	106	kΩ
$R_{PU(gpio)}$	Pull-down resistor	$V_{GPIO\_VREF} = 1.8 \text{ V}$	58	103	189	kΩ

### 4.3.3. Current consumption

Table 9 presents key current consumption characteristics for CM5 under various operating conditions. It details the typical shutdown, idle, operational, and RTC currents measured with different input voltages and control signals. Actual figures greatly depend on the end application.

**Table 9.**

*Current consumption characteristics for Raspberry Pi Compute Module 5 (CM5)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$I_{shutdown}$	Shutdown current	$\text{PMIC\_ENABLE} < 0.4 \text{ V}$	-	1.3	-	mA
$I_{shutdown}$	Shutdown current	$\text{PMIC\_ENABLE} > 2 \text{ V}$	-	3	-	mA
$I_{idle}$	Idle current	$\text{PMIC\_ENABLE} > 2 \text{ V}$	-	400	-	mA
$I_{load}$	Operation current	$\text{PMIC\_ENABLE} > 2 \text{ V}$	-	900	-	mA
$I_{VBAT}$	RTC current	$V_{in} = 5 \text{ V}$	-	1.7	-	µA
$I_{VBAT}$	RTC current	$V_{in} = 0 \text{ V}$	-	6	-	µA

符号	参数	条件	最小值	典型值	最大值	单位
$I_{OL(gpio)}$	输出电流	$12 \text{ mA}, V_{\text{GPIO\_VREF}} = 3.3 \text{ V}$	18.4	28.7	40.5	mA
$I_{OH(gpio)}$	输出电流	$2 \text{ mA}, V_{\text{GPIO\_VREF}} = 3.3 \text{ V}$	4.5	6.3	8.4	mA
$I_{OH(gpio)}$	输出电流	$4 \text{ mA}, V_{\text{GPIO\_VREF}} = 3.3 \text{ V}$	6.8	9.5	12.6	mA
$I_{OH(gpio)}$	输出电流	$8 \text{ mA}, V_{\text{GPIO\_VREF}} = 3.3 \text{ V}$	11.4	15.8	21	mA
$I_{OH(gpio)}$	输出电流	$12 \text{ mA}, V_{\text{GPIO\_VREF}} = 3.3 \text{ V}$	13.6	19	25.2	mA
$I_{OL(gpio)}$	输出电流	$2 \text{ mA}, V_{\text{GPIO\_VREF}} = 2.5 \text{ V}$	4.7	8	12.2	mA
$I_{OL(gpio)}$	输出电流	$4 \text{ mA}, V_{\text{GPIO\_VREF}} = 2.5 \text{ V}$	7.1	12	18.2	mA
$I_{OL(gpio)}$	输出电流	$8 \text{ mA}, V_{\text{GPIO\_VREF}} = 2.5 \text{ V}$	11.8	20	30.4	mA
$I_{OL(gpio)}$	输出电流	$12 \text{ mA}, V_{\text{GPIO\_VREF}} = 2.5 \text{ V}$	14.1	24	36.4	mA
$I_{OH(gpio)}$	输出电流	$2 \text{ mA}, V_{\text{GPIO\_VREF}} = 2.5 \text{ V}$	3.5	5.1	7	mA
$I_{OH(gpio)}$	输出电流	$4 \text{ mA}, V_{\text{GPIO\_VREF}} = 2.5 \text{ V}$	5.2	7.6	10.5	mA
$I_{OH(gpio)}$	输出电流	$8 \text{ mA}, V_{\text{GPIO\_VREF}} = 2.5 \text{ V}$	8.7	12.7	17.6	mA
$I_{OH(gpio)}$	输出电流	$12 \text{ mA}, V_{\text{GPIO\_VREF}} = 2.5 \text{ V}$	10.4	15.2	21.1	mA
$I_{OL(gpio)}$	输出电流	$2 \text{ mA}, V_{\text{GPIO\_VREF}} = 1.8 \text{ V}$	4.4	8.1	13.6	mA
$I_{OL(gpio)}$	输出电流	$4 \text{ mA}, V_{\text{GPIO\_VREF}} = 1.8 \text{ V}$	8.8	16.3	27.2	mA
$I_{OL(gpio)}$	输出电流	$8 \text{ mA}, V_{\text{GPIO\_VREF}} = 1.8 \text{ V}$	11.8	21.7	36.3	mA
$I_{OL(gpio)}$	输出电流	$12 \text{ mA}, V_{\text{GPIO\_VREF}} = 1.8 \text{ V}$	16.2	29.2	49.9	mA
$I_{OH(gpio)}$	输出电流	$2 \text{ mA}, V_{\text{GPIO\_VREF}} = 1.8 \text{ V}$	3.4	5.3	7.7	mA
$I_{OH(gpio)}$	输出电流	$4 \text{ mA}, V_{\text{GPIO\_VREF}} = 1.8 \text{ V}$	6.9	10.5	15.4	mA
$I_{OH(gpio)}$	输出电流	$8 \text{ mA}, V_{\text{GPIO\_VREF}} = 1.8 \text{ V}$	9.1	14	20.6	mA
$I_{OH(gpio)}$	输出电流	$12 \text{ mA}, V_{\text{GPIO\_VREF}} = 1.8 \text{ V}$	12.6	19.3	28.3	mA
$R_{PU(gpio)}$	上拉电阻	$V_{\text{GPIO\_VREF}} = 3.3 \text{ V}$	37	55	86	kΩ
$R_{PD(gpio)}$	下拉电阻	$V_{\text{GPIO\_VREF}} = 3.3 \text{ V}$	35	55	98	kΩ
$R_{PU(gpio)}$	上拉电阻	$V_{\text{GPIO\_VREF}} = 2.5 \text{ V}$	49	77	123	kΩ
$R_{PD(gpio)}$	下拉电阻	$V_{\text{GPIO\_VREF}} = 2.5 \text{ V}$	49	84	155	kΩ
$R_{PU(gpio)}$	上拉电阻	$V_{\text{GPIO\_VREF}} = 1.8 \text{ V}$	38	64	106	kΩ
$R_{PU(gpio)}$	下拉电阻	$V_{\text{GPIO\_VREF}} = 1.8 \text{ V}$	58	103	189	kΩ

### 4.3.3. 电流功耗

表 9 展示了 CM5 在各种工作条件下的关键电流消耗特性。详细说明了在不同输入电压和控制信号下测得的典型关机、待机、运行及 RTC 电流。实际数值在很大程度上取决于最终应用。

表 9。

树莓派计算模块 5 (CM5) 电流消耗特性

符号	参数	条件	最小值	典型值	最大值	单位
$I_{shutdown}$	关机电流	$\text{PMIC\_ENABLE} < 0.4 \text{ V}$	-	1.3	-	mA
$I_{shutdown}$	关机电流	$\text{PMIC\_ENABLE} > 2 \text{ V}$	-	3	-	mA
$I_{空闲}$	空闲电流	$\text{PMIC\_ENABLE} > 2 \text{ V}$	-	400	-	mA
$I_{负载}$	工作电流	$\text{PMIC\_ENABLE} > 2 \text{ V}$	-	900	-	mA
$I_{VBAT}$	RTC电流	$V_{in} = 5 \text{ V}$	-	1.7	-	μA
$I_{VBAT}$	RTC电流	$V_{in} = 0 \text{ V}$	-	6	-	μA

## 4.4. Thermal characteristics

CM5 contains less metal in the PCB and fewer connectors than Raspberry Pi 5, which means that it has less passive heat sinking than Raspberry Pi 5.

The BCM2712 SoC on CM5 has built-in thermal management that reduces its clock speed to keep the SoC temperature below 85°C. To avoid overheating, the SoC might automatically throttle its performance in high ambient temperatures. If the SoC can't reduce its temperature enough through throttling, its case temperature can exceed 85°C. Any thermal management solution must ensure that the ambient temperatures of the other silicon components on the board stay within their safe operating range.

CM5's overall operating temperature range is from -20°C to +85°C (non-condensing). Wireless RF performance is best within -20°C to +75°C.

## 4.5. Mean time between failure (MTBF)

Mean time between failure (MTBF) measures how long, on average, each device is expected to operate before failure. [Table 10](#) shows the MTBF for CM5 and CM5Lite, which varies depending on environmental conditions.

**Table 10.**

*Mean time between failure (MTBF) for Raspberry Pi Compute Module 5 (CM5)*

Environment	Description	CM5 MTBF	CM5Lite MTBF
<b>Ground, benign</b>	A stable, non-mobile environment where temperature and humidity are controlled, such as laboratories, business and scientific computer complexes, and medical equipment rooms. In these environments, devices generally last longer.	143 000 hours	168 000 hours
<b>Ground, mobile</b>	A high-stress environment with vibration, temperature swings, humidity variations, and frequent movement, such as equipment in vehicles and handheld communication devices. In these environments, life expectancy drops.	16 000 hours	16 000 hours

## 4.4. 热特性

CM5的印刷电路板金属含量和连接器数量均少于树莓派5，这意味着其被动散热能力低于树莓派5。

CM5上的BCM2712 SoC内置热管理功能，可降低时钟频率以保持SoC温度低于85°C。为防止过热，SoC可能在高环境温度下自动降频以降低性能。如果SoC通过降频仍无法有效降低温度，其封装温度可能超过85°C。任何热管理解决方案必须确保印刷电路板上其他硅元件的环境温度保持在其安全工作范围内。

CM5的整体工作温度范围为-20°C至+85°C（无冷凝）。无线射频性能在-20°C至+75°C范围内最佳。

## 4.5. 平均故障间隔时间（MTBF）

平均故障间隔时间（MTBF）衡量设备平均预期的运行时间直至故障。表10显示了CM5和CM5Lite的MTBF，数值因环境条件而异。

**表10。**

树莓派计算模块5（CM5）的平均无故障时间（MTBF）

环境	描述	CM5 MTBF	CM5Lite MTBF
地线，良性环境	稳定且非移动的环境，温度和湿度受控，例如实验室、商务及科研计算机综合体和医疗设备室。在此类环境中，设备通常寿命较长。	143 000 小时	168 000 小时
地线，移动环境	高应力环境，存在振动、温度波动、湿度变化及频繁移动，例如车辆设备和手持通信设备。在此类环境下，使用寿命缩短。	16 000 小时	16 000 小时

# 5. Troubleshooting

CM5 has a number of power-up and boot stages before it starts. If an error occurs at any of these stages, CM5 might fail to start or run as expected. The following sections help you to diagnose and resolve the issue by:

- Checking hardware power rails and signals for proper voltages and load behaviour.
- Verifying bootloader firmware operation and enabling diagnostics or alternate boot modes.
- Managing EEPROM firmware updates and write protection for boot reliability.

We also recommend avoiding known issues by ensuring the system software (firmware and kernel) are up to date. Keeping your firmware up to date can resolve many system issues and improve stability because newer versions contain improvements to the system. Similarly, new kernel releases often include important security patches and performance improvements.

## 5.1. Hardware power rails

CM5 requires stable power to start up. Check key power rails (5 V, 3.3 V, and 1.8 V) to verify power enable signals and identify any back-feeding caused by external devices or wiring.

1. **Test the 5 V supply under load:** Pull `PMIC_EN` low and apply an external 2 A load to the 5 V supply. The voltage should remain above 4.75 V (including noise), ideally, staying above 4.9 V.
2. **Check for back-feeding on 3.3 V and 1.8 V rails:** Remove the external 2 A load, but keep `PMIC_EN` pulled low. If the voltage for 3.3 V and 1.8 V exceeds 200 mV, there might be an external power path back-feeding the board, possibly through digital pins such as Ethernet.
3. **Check `PMIC_EN` goes high:** Remove the pull-down on `PMIC_EN` and then check that `PMIC_EN` now goes high; measure the voltage on this pin or check its logic state to confirm it goes high.
4. **Confirm that the voltage rails rise correctly:**
  - Check the 3.3 V supply rises to more than 3.15 V. If it doesn't, this suggests there is too much load on the 3.3 V rail.
  - Check the 1.8 V supply rises to more than 1.71 V. If it doesn't, this suggests there is too much load on the 1.8 V rail.
5. **Check the activity LED (`LED_nACT`) to verify the boot process:** The LED should oscillate to indicate booting; check it isn't flashing an error code. To decode error code patterns, see the [LED Flash codes](#) in the Raspberry Pi documentation.

## 5.2. Bootloader firmware

The bootloader firmware manages the initial startup of CM5. If your CM5 fails to start correctly, verify bootloader operation, then enable diagnostic modes. To verify bootloader operation:

- Connect an HDMI cable. The bootloader has started and is running correctly if the HDMI diagnostics screen appears.
- Connect a USB serial cable to GPIO pins 14 and 15. This allows you to receive bootloader output logs (through UART), which help verify what stage the bootloader is at and diagnose any issues. For more information, see [Configure UARTs](#).

If the bootloader isn't running as expected, enable diagnostic modes: short the `nRPIBOOT` pin to ground to force USB boot mode. The CM5IO board has a jumper for `nRPIBOOT` that you can use to enable different boot modes (for example, network boot) and UART logging. For more information, see [Flash an image to a Compute Module](#).

## 5.3. EEPROM management and firmware updates

For reliable startup and system stability on your CM5, keep the bootloader EEPROM up to date, including correct management of write protection.

- **Check EEPROM write-protection.** The on-board EEPROM can be write-protected by shorting the `EEPROM_nWP` pin to ground. The CM5IO board provides a jumper for `EEPROM_nWP` to enable or disable write protection.
- **If necessary, update or repair EEPROM.** CM5 won't run `recovery.bin` from the eMMC (or SD card on CM5Lite); update or repair the bootloader EEPROM on your CM5 through `usbboot` or self-update. Ensure write protection is disabled before attempting to update the EEPROM. For more information, see [Boot EEPROM](#).

# 5. 故障排除

CM5在启动和运行之前经历多个上电及引导阶段。若任一阶段发生错误，CM5可能无法按预期启动或运行。以下章节将帮助您通过以下方式诊断并解决问题：

- 检查硬件电源轨和信号是否具有正确的电压及负载表现。
- 验证引导加载程序固件的运行，并启用诊断或备用引导模式。
- 管理 EEPROM 固件更新及写保护以确保引导可靠性。

我们还建议确保系统软件（固件和内核）保持最新，从而避免已知问题。保持固件更新能够解决许多系统问题并提升稳定性，因为新版本包含系统改进。同样，新的内核版本通常包括重要的安全补丁和性能提升。

## 5.1. 硬件电源轨

CM5 启动需要稳定的电源。请检查关键电源轨（5 V、3.3 V 和 1.8 V），以确认电源使能信号，并识别外部设备或布线导致的反向供电。

- 1. 在负载条件下测试 5 V 电源：**拉 `PMIC_EN` 置低，并对 5 V 电源施加外部 2 A 负载。电压应保持在 4.75 V 以上（含噪声），理想情况下应高于 4.9 V。
- 2. 检查3.3 V和1.8 V电源轨的反向馈电：**移除外部2 A负载，但保持 `PMIC_EN` 保持拉低。如果3.3 V和1.8 V的电压超过200 mV，可能存在通过数字引脚（如以太网）等途径的外部电源反向馈电。
- 3. 检查 `PMIC_EN` 变高时：**移除 `PMIC_EN` 上的下拉 `PMIC_EN`，然后确认 `PMIC_EN` 已经变高；测量该引脚的电压或检测其逻辑状态以确认其变高。
- 4. 确认电压轨正确升起：**
  - 检查3.3 V电源是否升至高于3.15 V。如未达到，表示3.3 V电源轨负载过重。
  - 检查1.8 V电源是否升至高于1.71 V。如未达到，表示1.8 V电源轨负载过重。
- 5. 检查活动指示灯（`LED_nACT`）** 以验证启动过程：指示灯应闪烁以显示启动中；请确认其未闪烁错误代码。有关错误代码模式的解码，请参见树莓派文档中的 LED 闪烁代码。

## 5.2. 引导加载程序固件

引导加载程序固件负责管理 CM5 的初始启动。如 CM5 启动异常，请先确认引导加载程序运行情况，再启用诊断模式。验证引导加载程序运行的方法：

- 连接 HDMI 线缆。出现 HDMI 诊断屏幕即表示引导加载程序已启动并正常运行。
- 将 USB 串行线连接到 GPIO 14 和 15 脚。该操作允许通过 UART 接收引导加载程序输出日志，帮助确认引导进度及诊断问题。详情请参见配置 UART。

若引导加载程序未按预期运行，请启用诊断模式：将 `nRPIBOOT` 引脚短接至地线以强制进入 USB 启动模式。CM5IO 扩展板设有用于该功能的跳线。`nRPIBOOT` 可用于启用不同的启动模式（例如网络启动）和 UART 日志记录。有关详细信息，请参见向计算模块刷新映像。

## 5.3. EEPROM 管理与固件更新

为确保您的CM5可靠启动及系统稳定，请保持引导加载程序EEPROM的最新状态，包括正确管理写保护。

- **请检查EEPROM写保护状态。** 板载EEPROM可通过短接 `EEPROM_nWP` 引脚至地线来实现写保护。CM5IO板提供跳线以控制 `EEPROM_nWP`，从而启用或禁用写保护。
- **如有必要，请更新或修复EEPROM。** CM5将无法运行 存储于eMMC（或CM5Lite上的SD卡）中的recovery.bin文件；您需通过 `usbboot`或自我更新程序更新或修复CM5上的引导加载程序EEPROM。在尝试更新EEPROM前，请确保写保护已被禁用。有关详情，请参见引导EEPROM部分。

# 6. Ordering information

CM5 comes in a range of variants distinguished by wireless capability, RAM size, and eMMC storage capacity. Each CM5 variant is identified by a unique order code (part number). The available product variants are detailed in the tables below. Custom configurations can also be arranged to suit specific requirements.

## 6.1. Order quantity and packaging

You can order a specific number of one or more CM5 devices that will arrive individually boxed, or you can make a bulk order that will come in a single shipper. Small quantities supplied in individual cardboard boxes have an internal ESD coating so that a separate ESD bag isn't required. This packaging is recyclable to reduce waste.

## 6.2. Part number codes

[Table 11](#) explains the structure of part numbers for CM5 variants. It details how the model, wireless capability, RAM size, and eMMC storage capacity are encoded within the part number.

**Table 11.**

*Part number information for Raspberry Pi Compute Module 5 (CM5)*

Model	Wireless	RAM LPDDR4x	eMMC storage
CM5	0 = No	01 = 1 GB	000 = 0 GB (Lite)
	1 = Yes	02 = 2 GB	008 = 8 GB
		04 = 4 GB	016 = 16 GB
		08 = 8 GB	032 = 32 GB
		16 = 16 GB	064 = 64 GB
<b>Example part number</b>			
CM5	1	02	032

## 6.3. Product variants

[Table 12](#) shows available variants for CM5 by part number, detailing wireless support, RAM size, eMMC storage capacity and RPL numbers. Other configurations can be custom ordered.

**Table 12.**

*Available product variants for Raspberry Pi Compute Module 5 (CM5)*

Part number	Wireless	RAM LPDDR4x	Storage eMMC	RPL number
CM5002000	-	2 GB	Lite (0 GB)	SC1556
CM5002016	-	2 GB	16 GB	SC1558
CM5002032	-	2 GB	32 GB	SC1559
CM5002064	-	2 GB	64 GB	SC1560
CM5102000	Yes	2 GB	Lite (0 GB)	SC1586
CM5102016	Yes	2 GB	16 GB	SC1588
CM5102032	Yes	2 GB	32 GB	SC1589
CM5102064	Yes	2 GB	64 GB	SC1590

# 6. 订购信息

CM5有多种型号，区分为无线功能、内存容量及eMMC存储容量。每个树莓派计算模块 5 变体均由唯一的订单代码（零件编号）标识。下表详细列出了可用的产品变体。也可根据具体需求安排定制配置。

## 6.1. 订购数量与包装

您可以订购一定数量的一个或多个 CM5 设备，设备将单独包装；也可以批量订购，产品将放置于单一外箱中。小批量以单个纸盒包装的产品内部设有静电放电（ESD）涂层，因此无需额外防静电袋。该包装材料可回收利用，以减少废弃物。

## 6.2. 零件编号代码

[表 11 说明了 CM5 变体零件编号的构成。详细介绍型号、无线功能、RAM 容量及 eMMC 存储容量在零件编号中的编码方式。](#)

**表 11。**

树莓派计算模块 5（CM5）零件编号信息

型号	无线	RAM LPDDR4x	eMMC 存储
CM5	0 = 无	01 = 1 GB	000 = 0 GB (Lite)
	1 = 是	02 = 2 GB	008 = 8 GB
		04 = 4 GB	016 = 16 GB
		08 = 8 GB	032 = 32 GB
		16 = 16 GB	064 = 64 GB
<b>示例零件编号</b>		128 = 128 GB	
CM5	1	02	032

## 6.3. 产品变体

[表12展示了CM5各零件编号的可用变体，详细说明了无线支持、RAM容量、eMMC存储容量及RPL编号。其他配置可按需定制。](#)

**表12。**

树莓派计算模块5（CM5）可用产品变体

零件编号	无线	RAM LPDDR4x	存储 (eMMC)	RPL编号
CM5002000	-	2 GB	Lite (0 GB)	SC1556
CM5002016	-	2 GB	16 GB	SC1558
CM5002032	-	2 GB	32 GB	SC1559
CM5002064	-	2 GB	64 GB	SC1560
CM5102000	是	2 GB	Lite (0 GB)	SC1586
CM5102016	是	2 GB	16 GB	SC1588
CM5102032	是	2 GB	32 GB	SC1589
CM5102064	是	2 GB	64 GB	SC1590

Part number	Wireless	RAM LPDDR4x	Storage eMMC	RPL number
CM5004000	-	4 GB	Lite (0 GB)	SC1562
CM5004016	-	4 GB	16 GB	SC1564
CM5004032	-	4 GB	32 GB	SC1565
CM5004064	-	4 GB	64 GB	SC1566
CM5104000	Yes	4 GB	Lite (0 GB)	SC1592
CM5104016	Yes	4 GB	16 GB	SC1594
CM5104032	Yes	4 GB	32 GB	SC1595
CM5104064	Yes	4 GB	64 GB	SC1596
CM5008000	-	8 GB	Lite (0 GB)	SC1568
CM5008016	-	8 GB	16 GB	SC1570
CM5008032	-	8 GB	32 GB	SC1571
CM5008064	-	8 GB	64 GB	SC1572
CM5108000	Yes	8 GB	Lite (0 GB)	SC1598
CM5108016	Yes	8 GB	16 GB	SC1600
CM5108032	Yes	8 GB	32 GB	SC1601
CM5108064	Yes	8 GB	64 GB	SC1602
CM5016000	-	16 GB	Lite (0 GB)	SC1574
CM5016016	-	16 GB	16 GB	SC1576
CM5016032	-	16 GB	32 GB	SC1577
CM5016064	-	16 GB	64 GB	SC1578
CM5116000	Yes	16 GB	Lite (0 GB)	SC1604
CM5116016	Yes	16 GB	16 GB	SC1606
CM5116032	Yes	16 GB	32 GB	SC1607
CM5116064	Yes	16 GB	64 GB	SC1608

零件编号	无线	RAM LPDDR4x	存储 (eMMC)	RPL编号
CM5004000	-	4 GB	Lite (0 GB)	SC1562
CM5004016	-	4 GB	16 GB	SC1564
CM5004032	-	4 GB	32 GB	SC1565
CM5004064	-	4 GB	64 GB	SC1566
CM5104000	是	4 GB	Lite (0 GB)	SC1592
CM5104016	是	4 GB	16 GB	SC1594
CM5104032	是	4 GB	32 GB	SC1595
CM5104064	是	4 GB	64 GB	SC1596
CM5008000	-	8 GB	Lite (0 GB)	SC1568
CM5008016	-	8 GB	16 GB	SC1570
CM5008032	-	8 GB	32 GB	SC1571
CM5008064	-	8 GB	64 GB	SC1572
CM5108000	是	8 GB	Lite (0 GB)	SC1598
CM5108016	是	8 GB	16 GB	SC1600
CM5108032	是	8 GB	32 GB	SC1601
CM5108064	是	8 GB	64 GB	SC1602
CM5016000	-	16 GB	Lite (0 GB)	SC1574
CM5016016	-	16 GB	16 GB	SC1576
CM5016032	-	16 GB	32 GB	SC1577
CM5016064	-	16 GB	64 GB	SC1578
CM5116000	是	16 GB	Lite (0 GB)	SC1604
CM5116016	是	16 GB	16 GB	SC1606
CM5116032	是	16 GB	32 GB	SC1607
CM5116064	是	16 GB	64 GB	SC1608

# Appendix A. Test Points

CM5 contains test points: pins on the board that you can use to power the board, program it, or debug it without needing to use the main 100-pin connectors.

## A.1. Test point map

**Table 13** lists the coordinates (**X** and **Y**) of tests points on CM5 and what each test point is used for. Most signals replicate pins on the 100-pin connectors of CM5.

**Table 13.**

*Test points for Raspberry Pi Compute Module 5 (CM5)*

Reference	X	Y	Name
MH4	51.5	36.5	Mounting Hole
MH3	3.5	36.5	Mounting Hole
MH2	51.5	3.5	Mounting Hole
MH1	3.5	3.5	Mounting Hole
TP1	14.34	17.54	5 V
TP2	8.8	1.3	RUN
TP3	51.2	32.6	GND
TP4	4.8	13	reserved
TP7	24.2	7.5	GND
TP8	1.65	15.05	GND
TP9	1.5	10.5	reserved
TP10	48.4	15.1	reserved
TP13	42.6	7.3	GND
TP15	14.7	6.6	reserved
TP16	9.3	34.9	nRPIBOOT
TP17	37.4	8.1	reserved
TP18	23.4	23.55	reserved
TP21	24.5125	14.025	nRESET_OUT
TP22	13.0875	11.225	reserved
TP26	17.7	20.2	GND
TP27	43.6	22.3	reserved
TP28	15.4	16	reserved
TP29	23.65	21.55	reserved
TP30	37.2	34.9	reserved
TP31	9.1	3.2	reserved
TP32	1.5	13	reserved
TP33	47	36	CM5_3V3
TP34	50.5	15.5	CM5_1V8
TP35	11	37.8	DEBUG_UART_TX
TP36	8.5	37.1	DEBUG_UART_RX
TP39	22.1	6.1	reserved

# 附录 A. 测试点

计算模块5（CM5）包含测试点：板上的引脚，您可以利用这些引脚为开发板供电、编程或调试，而无需使用主100针连接器。

## A.1. 测试点布局

[表13列出了CM5测试点的坐标（X和Y）及其用途。大多数信号与CM5的100针连接器引脚相对应。](#)

表 13。

树莓派计算模块5 (CM5) 测试点

参考	X	Y	名称
MH4	51.5	36.5	安装孔
MH3	3.5	36.5	安装孔
MH2	51.5	3.5	安装孔
MH1	3.5	3.5	安装孔
TP1	14.34	17.54	5 V
TP2	8.8	1.3	RUN
测试点3	51.2	32.6	GND
测试点4	4.8	13	保留
测试点7	24.2	7.5	GND
测试点8	1.65	15.05	GND
测试点9	1.5	10.5	保留
测试点10	48.4	15.1	保留
测试点13	42.6	7.3	GND
测试点15	14.7	6.6	保留
测试点16	9.3	34.9	nRPIBOOT
测试点17	37.4	8.1	保留
测试点18	23.4	23.55	保留
测试点21	24.5125	14.025	nRESET_OUT
测试点22	13.0875	11.225	保留
测试点26	17.7	20.2	GND
测试点27	43.6	22.3	保留
测试点28	15.4	16	保留
测试点29	23.65	21.55	保留
测试点30	37.2	34.9	保留
测试点31	9.1	3.2	保留
测试点32	1.5	13	保留
测试点33	47	36	CM5_3V3
测试点34	50.5	15.5	CM5_1V8
测试点35	11	37.8	DEBUG_UART_TX
测试点36	8.5	37.1	DEBUG_UART_RX
测试点39	22.1	6.1	保留

Reference	X	Y	Name
TP40	6.7	15.2	reserved
TP41	8.7	15.3	reserved
TP42	11.4	34.9	PWR_BUT
TP44	51.7	30.2	reserved
TP45	53.1	28.7	reserved
TP46	7	34.7	GND
TP48	21.6	15.4	SOC_TRST_N
TP49	21.6	13.3	SOC_TDI
TP50	20.4	17.2	SOC_TDO
TP51	20.3	8.8	SOC_TMS
TP52	19.9	11.9	SOC_TCK
TP57	53.2	32	reserved
TP60	48	38.7	GND
TP61	6.575	1.225	GND
TP62	22.2	31.6	GND
TP63	8.7	18.2	5v_Sense
TP64	47.3	5.4	reserved
TP65	28.2	7.5	USBC_D_N
TP66	26.1	7.5	USBC_D_P
TP67	7	38.6	LED_nPWR
TP68	13	37.5	LED_nACT
TP69	38.8	25.9	ETH0_P
TP70	39.6	24.2	ETH0_N
TP71	43.8	14.1	ETH1_N
TP72	45.6	13.1	ETH1_P
TP73	42.4	31.7	ETH2_P
TP74	42.6	33.7	ETH2_N
TP75	41.6	37.8	ETH3_P
TP76	42.9	36.1	ETH3_N
TP77	45	37	GPIO_VREF
TP78	14.37	19.52	5 V

## A.2. Test point connections for power and programming

Use the following test points to power, program, and boot CM5 without using the main 100-pin connectors:

- **Power (Vin).** Use test points TP1 and TP78 to supply 5 V power to CM5. At a minimum, connect ground to test points TP26, TP61, and TP8. If possible, use more ground points.
- **Debug UART.** Test points TP35 ( TX ) and TP36 ( RX ) provide serial debug communication lines. Use TP46 for ground. This is useful for programming and debugging during boot.
- **Raspberry Pi boot mode.** Pins TP65 and TP66 serve as USB data lines. Connect TP7 as ground, and also ground TP16 ( nRPI\_BOOT ) to force the board into Raspberry Pi boot mode.
- **Ethernet boot.** Connect test points TP69 and TP76 to an external Ethernet MagJack (the Ethernet connector with magnetics).

参考	X	Y	名称
测试点40	6.7	15.2	保留
测试点41	8.7	15.3	保留
测试点42	11.4	34.9	PWR_BUT
测试点44	51.7	30.2	保留
测试点45	53.1	28.7	保留
测试点46	7	34.7	GND
测试点48	21.6	15.4	SOC_TRST_N
测试点49	21.6	13.3	SOC_TDI
测试点50	20.4	17.2	SOC_TDO
TP51	20.3	8.8	SOC_TMS
TP52	19.9	11.9	SOC_TCK
TP57	53.2	32	保留
TP60	48	38.7	GND
TP61	6.575	1.225	GND
TP62	22.2	31.6	GND
TP63	8.7	18.2	5v_Sense
TP64	47.3	5.4	保留
TP65	28.2	7.5	USBC_D_N
TP66	26.1	7.5	USBC_D_P
TP67	7	38.6	LED_nPWR
TP68	13	37.5	LED_nACT
TP69	38.8	25.9	ETH0_P
TP70	39.6	24.2	ETH0_N
TP71	43.8	14.1	ETH1_N
TP72	45.6	13.1	ETH1_P
TP73	42.4	31.7	ETH2_P
TP74	42.6	33.7	ETH2_N
测试点75	41.6	37.8	ETH3_P
测试点76	42.9	36.1	ETH3_N
测试点77	45	37	GPIO_VREF
测试点78	14.37	19.52	5 V

## A.2. 电源与编程的测试点连接

使用以下测试点，为 CM5 供电、编程及启动，无需使用主 100 针连接器：

- **电源 (Vin)**。使用测试点 测试点1 和 测试点78 向 CM5 供给 5 V 电源。最少连接地线至测试点 测试点26， 测试点61 和 测试点8。如可能，请使用更多地线测试点。
- **调试 UART**。测试点 测试点35 ( TX ) 和 测试点36 ( RX ) 提供串行调试通信线路。使用 测试点46 作为地线。对启动过程中的编程和调试非常有用。
- **树莓派启动模式。引脚** 测试点65 和 测试点66 作为USB数据信号线。连接 测试点7 作为地线，同时也是地线 测试点16 ( nRPI\_BOOT ) 以强制板卡进入树莓派启动模式。
- **以太网启动**。连接测试点 测试点69 和 测试点76 连接到外部以太网MagJack（带磁性元件的以太网连接器）。

# Appendix B. CM4 and CM5 differences

This section describes the differences between Raspberry Pi Compute Module 5 (CM5) and the previous module, Raspberry Pi Compute Module 4 (CM4).

## B.1. Pinout changes

CM5 introduces specific pin-level changes from CM4, including updated pin functions and signal repurposing to support new hardware features.

### B.1.1. Per-pin differences

[Table 14](#) compares the exact per-pin changes between CM4 and CM5. It highlights updated functions and signal repurposing to reflect the new hardware capabilities and interfaces.

**Table 14.**

*Pin changes between Raspberry Pi Compute Module 4 (CM4) and Raspberry Pi Compute Module 5 (CM5)*

Pin	CM4	CM5	Details
16	SYNC_IN	Fan_tacho	Fan tacho input
19	Ethernet nLED1	Fan_PWM	Fan PWM output
76	Reserved	VBAT	RTC battery (there's a constant load of a few uA even if CM5 is powered)
92	RUN_PG	PWR_Button	Replicates the power button on Raspberry Pi 5: a short press signals that the device should wake up or shut down; a long press forces shutdown
93	nRPIBOOT	nRPIBOOT	
94	AnalogIP1	CC1	Connects to the CC1 line of a USB-C connector so the PMIC to negotiate 5 A
96	AnalogIP0	CC2	Connects to the CC2 line of a USB-C connector so the PMIC to negotiate 5 A
99	Global_EN	PMIC_ENABLE	No external change
100	nEXTRST	CAM_GPIO1	Pulled up on CM5, but driven low during boot to emulate a nRESET signal
104	Reserved	PCIE_DET_nWAKE	PCIE nWAKE; pull-up to CM5_3v3 with an 8.2 kΩ
106	Reserved	PCIE_PWR_EN	Signals if the PCIe device can be powered up or down; active high
111	VDAC_COMP	VBUS_EN	Output to signal USB VBUS should be enabled
128	CAM0_D0_N	USB3-0-RX_N	May be P/N swapped
130	CAM0_D0_P	USB3-0-RX_P	May be P/N swapped
134	CAM0_D1_N	USB3-0-DP	USB 2.0 signal
136	CAM0_D1_P	USB3-0-DM	USB 2.0 signal
140	CAM0_C_N	USB3-0-TX_N	May be P/N swapped
142	CAM0_C_P	USB3-0-TX_P	May be P/N swapped
157	DSI0_D0_N	USB3-1-RX_N	May be P/N swapped
159	DSI0_D0_P	USB3-1-RX_P	May be P/N swapped
163	DSI0_D1_N	USB3-1-DP	USB 2.0 signal
165	DSI0_D1_P	USB3-1-DM	USB 2.0 signal
169	DSI0_C_N	USB3-1-TX_N	May be P/N swapped
171	DSI0_C_P	USB3-1-TX_P	May be P/N swapped

# 附录 B. CM4 与 CM5 差异

本节介绍了树莓派计算模块5（CM5）与上一代模块树莓派计算模块4（CM4）之间的差异。

## B.1. 引脚分配变更

CM5引入了与CM4不同的引脚级变更，包括更新的引脚功能和信号重用，以支持新的硬件特性。

### B.1.1. 各引脚差异

表14比较了CM4与CM5之间的逐引脚变化，突出显示了更新的功能和信号重用，以反映新的硬件能力和接口。

**表14。**

树莓派计算模块4（CM4）与树莓派计算模块5（CM5）之间的引脚变更

引脚	CM4	CM5	详细信息
16	SYNC_IN	Fan_tacho	风扇转速输入
19	以太网 nLED1	Fan_PWM	风扇 PWM 输出
76	保留	VBAT	RTC 电池（即使 CM5 供电，仍有数微安的持续负载）
92	RUN_PG	PWR_Button	模拟树莓派 5 的电源按钮：短按表示设备应唤醒或关机；长按则强制关机
93	nRPIBOOT	nRPIBOOT	
94	AnalogIP1	CC1	连接至 USB-C 连接器的 CC1 线，以便 PMIC 协商 5 A 电流
96	AnalogIP0	CC2	连接至 USB-C 连接器的 CC2 线，以便 PMIC 协商 5 A 电流
99	Global_EN	PMIC_ENABLE	无外部变化
100	nEXTRST	CAM_GPIO1	CM5 内部上拉，但启动时拉低以模拟 nRESET 信号
104	保留	PCIE_DET_nWAKE	PCIE nWAKE；上拉至 CM5_3v3 并联 8.2 kΩ 电阻
106	保留	PCIE_PWR_EN	指示PCIe设备是否可以开机或关机；高电平有效
111	VDAC_COMP	VBUS_EN	输出信号，指示应启用USB VBUS
128	CAM0_D0_N	USB3-0-RX_N	可能存在P/N交换
130	CAM0_D0_P	USB3-0-RX_P	可能存在P/N交换
134	CAM0_D1_N	USB3-0-DP	USB 2.0信号
136	CAM0_D1_P	USB3-0-DM	USB 2.0信号
140	CAM0_C_N	USB3-0-TX_N	可能存在P/N交换
142	CAM0_C_P	USB3-0-TX_P	可能存在P/N交换
157	DSI0_D0_N	USB3-1-RX_N	可能存在P/N交换
159	DSI0_D0_P	USB3-1-RX_P	可能存在P/N交换
163	DSI0_D1_N	USB3-1-DP	USB 2.0信号
165	DSI0_D1_P	USB3-1-DM	USB 2.0信号
169	DSI0_C_N	USB3-1-TX_N	可能存在P/N交换
171	DSI0_C_P	USB3-1-TX_P	可能存在P/N交换

## B.1.2. Summary of functional and hardware changes

In addition to the above, there have been broader design changes. The following list summarises the functional consequences of these changes, as well as the impact of some of the above pin changes:

- **Connectors.** The connectors have changed brand and have been tested to higher currents to support CM5.
- **Thickness.** The PCB for CM5 is 0.04 mm thicker than CM4, but the main processor is thinner.
- **PCIe clock.** PCIe CLK signals are no longer capacitively coupled.
- **ESD protection.** CM4 has extra ESD protection on the HDMI, SDA, SCL, HPD, and CEC signals. This is removed from CM5.
- **Dual-purpose DSI and CSI signals.** `CAM1` and `DSI1` signals became dual-purpose and can be used for either a CSI camera or a DSI display. For more information, see [Section 2.5. Video and display interfaces](#).
- **USB ports.** For more information about USB ports on CM5, see [Section 2.4. USB interfaces](#).
  - The `CAM0` port (pins 128 to 142) on CM4 is a USB 3.0 port on CM5.
  - The `DSI0` port (pins 157 to 171) on CM4 is a USB 3.0 port on CM5.
- **VBUS enable pin.** Pin 111 (`VDAC_COMP` on CM4) has been repurposed as a VBUS enable pin controlling power to the two USB 3.0 ports on CM5. Power to the USB 3.0 ports is enabled when the pin is active high.
- **PD CC signals.** Pins 94 and 96, the two ADC channels on CM4, have become the Power Delivery (PD) Configuration Channel (CC) signals within the USB-C connector.

## B.2. Track lengths

CM5 has updated HDMI and Ethernet track lengths compared to CM4. These changes improve pair-to-pair skew and remain well within tolerances, so no functional impact is expected for previous Compute Modules.

- **HDMI0** : P/N pairs remain length-matched, but the skew between pairs is now less than 1 mm. This is unlikely to make a difference because the skew between pairs can be up to 25 mm on previous Compute Modules.
- **HDMI1** : P/N pairs remain length-matched, but the skew between pairs is now less than 5 mm. This is unlikely to make a difference because the skew between pairs can be up to 25 mm on previous Compute Modules.
- **Ethernet**: P/N pairs remain length-matched, but the skew between pairs is now less than 4 mm. This is unlikely to make a difference because the skew between pairs can be up to 12 mm on previous Compute Modules.

## B.3. Power budget

CM5 delivers significantly more performance than CM4, and therefore consumes more power. Power supply designs should accommodate 5 V at up to 2.5 A. If this creates an issue with an existing board design, lowering the CPU clock rate can reduce the peak power consumption.

For more information about power requirements for CM5, see [Section 3.3. Power consumption](#).

## B.1.2. 功能及硬件变更汇总

除上述内容外，设计方面还进行了更为广泛的变更。以下列表总结了这些变更的功能影响及部分引脚变更的影响：

- **连接器。** 连接器更换了品牌，并经过更高电流测试以支持CM5。
- **厚度。** CM5的印刷电路板比CM4厚0.04毫米，但主处理器更薄。
- **PCIe时钟。** PCIe CLK信号不再采用电容耦合方式。
- **ESD保护。** CM4在HDMI、SDA、SCL、HPD和CEC信号上增加了额外的ESD保护。CM5已取消这些额外的ESD保护。
- **DSI和CSI信号的双重用途。** CAM1 和 DSI1信号变为双重用途，可用于CSI摄像头或DSI显示器。更多信息，请参见第2.5节 视频及显示接口。
- **USB端口。** 有关CM5上USB端口的详细信息，请参见第2.4节 USB接口。
  - 该 CM4上的CAM0端口（引脚128至142）在CM5上为USB 3.0端口。
  - 该 CM4上的DSI0端口（引脚157至171）在CM5上为USB 3.0端口。
- **VBUS使能引脚。** 引脚111（CM4上的VDAC\_COMP引脚）已重新定义为VBUS使能引脚，用于控制CM5上两个USB 3.0端口的供电。该引脚高电平时，USB 3.0端口供电被使能。
- **PD CC信号。** CM4上的引脚94和96，两个ADC通道，已转为USB-C连接器内的电源传输（PD）配置通道（CC）信号。

## B.2. 走线长度

计算模块5相较于计算模块4对 HDMI 和以太网的走线长度进行了更新。这些更改改善了对间的时序偏差，且均远低于容差范围，因此预计不会对之前的计算模块产生功能性影响。

- **HDMI0 :P/N** 对保持长度匹配，但对间的时序偏差现已低于 1 毫米。这不太可能产生差异，因为之前的计算模块中对间时序偏差可达 25 毫米。
- **HDMI1 :P/N** 对保持长度匹配，但对间的时序偏差现已低于 5 毫米。这不太可能产生差异，因为之前的计算模块中对间时序偏差可达 25 毫米。
- 以太网:P/N 对保持长度匹配，但对间的时序偏差现已低于 4 毫米。这不太可能产生差异，因为之前的计算模块中对间时序偏差可达 12 毫米。

## B.3. 电源预算

计算模块5 的性能显著优于计算模块4，因此功耗也相应更高。电源设计应支持最高 2.5 A 的 5 V 电压。如现有电路板设计出现问题，可通过降低 CPU 时钟频率来降低峰值功耗。

有关 CM5 电源需求的详细信息，请参见第 3.3 节 电力消耗。

## Appendix C. Documentation history

Date	Changes
6 October, 2025	Minor additions and fixes.
28 August, 2025	Updated structure, grammar, and wording for clarity and style. Made minor corrections. Added information about 16 GB memory and 64 GB storage eMMC. Added information about CM5 connectors. Updated diagrams.
21 July, 2025	Update to new company format.
27 November, 2024	Initial release of Raspberry Pi Compute Module 5 (CM5).

## 附录 C. 文档历史

日期	变更
2025 年 10 月 6 日	小幅新增与修正。
2025 年 8 月 28 日	更新结构、语法及措辞以提高清晰度和风格，进行了小幅修正。新增关于 16 GB 内存和 64 GB 存储 eMMC 的信息。新增关于 CM5 连接器的信息，更新示意图。
2025 年 7 月 21 日	更新至新公司格式。
2024 年 11 月 27 日	树莓派计算模块 5 (CM5) 初始发布。



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