

PCA9306 Dual Bidirectional I²C Bus and SMBus Voltage-Level Translator

1 Features

- 2-Bit bidirectional translator for SDA and SCL lines in mixed-mode I²C Applications
- I²C and SMBus compatible
- Less than 1.5-ns maximum propagation delay to accommodate standard-mode and fast-mode I²C devices and multiple controllers
- Allows voltage-level translation between
 - 1.2-V V_{REF1} and 1.8-V, 2.5-V, 3.3-V, or 5-V V_{REF2}
 - 1.8-V V_{REF1} and 2.5-V, 3.3-V, or 5-V V_{REF2}
 - 2.5-V V_{REF1} and 3.3-V or 5-V V_{REF2}
 - 3.3-V V_{REF1} and 5-V V_{REF2}
- Provides bidirectional voltage translation with no direction pin
- Low 3.5- Ω ON-state resistance between input and output ports provides less signal distortion
- Open-drain I²C I/O ports (SCL1, SDA1, SCL2, and SDA2)
- 5-V Tolerant I²C I/O ports to support mixed-mode signal operation
- High-impedance SCL1, SDA1, SCL2, and SDA2 pins for EN = low
- Lockup-free operation for isolation when EN = low
- Flow-through pinout for ease of printed-circuit-board trace routing
- Latch-up performance exceeds 100 mA Per JESD 78, class II
- ESD protection exceeds JESD 22
 - 2000-V Human-body model (A114-A)
 - 1000-V Charged-device model (C101)

2 Applications

- I²C, SMBus, PMBus, MDIO, UART, low-speed SDIO, GPIO, and other two-signal interfaces
- Servers
- Routers (telecom switching equipment)
- Personal Computers
- Industrial Automation

3 Description

The PCA9306 device is a dual bidirectional I²C and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.2-V to 3.3-V V_{REF1} and 1.8-V to 5.5-V V_{REF2}.

The PCA9306 device allows bidirectional voltage translations between 1.2 V and 5 V, without the use of a direction pin. The low ON-state resistance (R_{ON}) of the switch allows connections to be made with minimal propagation delay. When EN is high, the translator switch is ON, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is low, the translator switch is off, and a high-impedance state exists between ports.

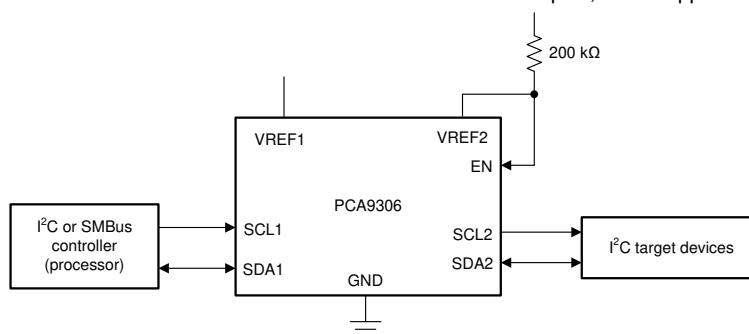
In addition to voltage translation, the PCA9306 device can be used to isolate a 400-kHz bus from a 100-kHz bus by controlling the EN pin to disconnect the slower bus during fast-mode communication.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
PCA9306	SSOP (8)	2.95 mm x 4 mm
	VSSOP (8)	2.3 mm x 3.1 mm
	X2SON (8)	1.4 mm x 1 mm
	DSBGA (8)	1.98 mm x 0.98 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

(2) The package size (length x width) is a nominal value and includes pins, where applicable.



Simplified Application Diagram



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PCA9306 双向双路 I²C 总线及 SMBus 电压电平转换器

1 特性

- 用于混合模式 I²C 应用中 SDA 和 SCL 线的 2 位双向转换器
- 兼容 I²C 和 SMBus
- 最大传播延迟小于 1.5 纳秒，适用于标准模式和快速模式 I²C 设备及多控制器环境
- 支持以下电压电平之间的转换
 - 1.2 V V_{REF1} 与 1.8 V、2.5 V、3.3 V 或 5 V V_{REF2}
 - 1.8 V V_{REF1} 与 2.5 V、3.3 V 或 5 V V_{REF2}
 - 2.5 V V_{REF1} 与 3.3 V 或 5 V V_{REF2}
 - 3.3 V V_{REF1} 与 5 V V_{REF2}
- 提供无方向引脚的双向电压转换
- 输入端与输出端之间低至 3.5 Ω 的导通电阻，减少信号失真
- 开漏式 I²C 输入/输出端口（SCL1、SDA1、SCL2 和 SDA2）
- 支持 5 V 容忍的 I²C 输入/输出端口，支持混合模式信号操作
- 当 EN 为低电平时，SCL1、SDA1、SCL2 和 SDA2 引脚呈高阻抗状态
- 当 EN 为低电平时，实现无锁定隔离操作
- 直通式引脚排列，便于印刷电路板走线
- 锁存性能超过 100 mA，符合 JESD 78 II 类标准
- ESD 保护性能超过 JESD 22 标准
 - 2000 V 人体模型 (A114-A)
 - 1000 V 带电器件模型 (C101)

2 应用

- I²C、SMBus、PMBus、MDIO、UART、低速 SDIO、GPIO 及其他双信号接口
- 服务器
- 路由器（电信交换设备）
- 个人计算机
- 工业自动化

3 描述

PCA9306 器件是一款带使能 (EN) 输入的双路双向 I²C 及 SMBus 电压电平转换器，工作电压范围为 1.2 V 至 3.3 V 的 V_{REF1} 和 1.8 V 至 5.5 V 的 V_{REF2}。

PCA9306 器件支持 1.2 V 至 5 V 之间的双向电压转换，无需使用方向引脚。开关的低导通电阻 (RON) 确保连接时具有极小的传播延迟。当 EN 为高电平时，转换器开关闭合，SCL1 和 SDA1 I/O 分别与 SCL2 和 SDA2 I/O 连接，实现端口间的双向数据流。当 EN 为低电平时，转换器开关断开，端口间处于高阻抗状态。

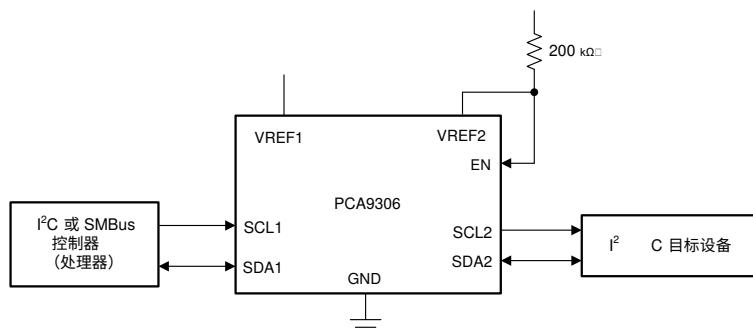
除了电压转换功能外，PCA9306 器件还可通过控制 EN 引脚，在快速模式通信期间断开较慢的总线，实现 400 kHz 总线与 100 kHz 总线的隔离。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
PCA9306	SSOP (8)	2.95 mm x 4 mm
	VSSOP (8)	2.3 mm x 3.1 mm
	X2SON (8)	1.4 mm x 1 mm
	DSBGA (8)	1.98 mm x 0.98 mm

(1) 有关所有可用封装，请参见数据手册末尾的可订购附录。

(2) 封装尺寸 (长×宽) 为标称值，包含引脚 (如适用)。



简化应用示意图



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (October 2021) to Revision O (September 2023)	Page
• Changed Device Information table to the <i>Package Information</i> table	1
• Changed the <i>Thermal Information</i> table values for the DQE package.....	6

Changes from Revision M (April 2019) to Revision N (October 2021)	Page
• Globally changed instances of legacy terminology to controller and target where I2C is mentioned.....	1
• Changed the <i>Thermal Information</i> table values for the DCT and DCU packages.....	6
• Changed the MIN and MAX values of V_{IK} in the <i>Electrical Characteristics</i> table.....	6
• Changed t_{PHL} to show the package values in the <i>Switching Characteristics AC Performance (Translating Down) (EN = 3.3 V)</i> table.....	7
• Changed t_{PHL} to show the package values in the <i>Switching Characteristics AC Performance (Translating Down) (EN = 2.5 V)</i> table.....	7
• Changed t_{PHL} to show the package values in the <i>Switching Characteristics AC Performance (Translating Up) (EN = 3.3 V)</i> table.....	7
• Changed t_{PHL} to show the package values in the <i>Switching Characteristics AC Performance (Translating Up) (EN = 2.5 V)</i> table.....	7

Changes from Revision L (April 2016) to Revision M (April 2019)	Page
• Changed the DQE package family From: VSSON to X2SON.....	4
• Added new section to <i>Overview</i>	10
• Changed the labels in Figure 9-4 . The red curve is > 2 V, the black curve is ≤ 2 V.	20

Changes from Revision K (October 2014) to Revision L (April 2016)	Page
• Changed "ON-State Connection " to "ON-state Resistance".....	1
• Deleted machine model ESD rating	1
• Added "bus" following "100-kHz" in the last sentence of the <i>Description</i> section.....	1
• Changed body-size dimensions in the <i>Device Information</i> table	1
• Replaced pinout diagrams.....	4
• Added I/O column to the <i>Pin Functions</i> table	4

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4 修订历史

注：先前版本的页码可能与当前版本不同。

从修订版N（2021年10月）到修订版O（2023年9月）的变更

页码

• 将器件信息表更改为封装信息表	1
• 更改DQE封装的热特性信息表中的数值	6

从修订版M（2019年4月）至修订版N（2021年10月）的变更

页码

• 在提及 I _C 时，全球范围内将旧术语统一更改为控制器和目标	1
• 更改了 DCT 和 DCU 封装的热特性信息表中的数值	6
• 更改了电气特性表中 V_{IK} 的最小值和最大值	6
• 更改了 t_{PHL} 以显示开关特性交流性能 (向下转换) ($EN = 3.3\text{ V}$) 表中的封装数值 (向下转换) ($EN = 3.3\text{ V}$) 表	7
• 更改了 t_{PHL} 以显示开关特性交流性能 (向下转换) ($EN = 3.3\text{ V}$) 表中的封装数值 (向下转换) ($EN = 2.5\text{ V}$) 表	7
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• 更改了 t_{PHL} 以显示开关特性交流性能 (向上转换) ($EN = 3.3\text{ V}$) 表中的封装数值 ($EN = 2.5\text{ V}$) 表	7

从修订版L（2016年4月）至修订版M（2019年4月）的变更

页码

• 将 DQE 封装系列由 VSSON 更改为 X2SON	4
• 在概述章节中新增内容	10
• 更改了图 9-4 中的标签。红色曲线表示 $> 2\text{ V}$ ，黑色曲线表示 $\leq 2\text{ V}$	20

从修订版K（2014年10月）到修订版L（2016年4月）的变更

页码

• 将 “ON-State Connection” 更改为 “ON-state Resistance”	1
• 删除了机器模型 ESD 额定值	1
• 在 Description 部分最后一句中的 “100-kHz” 后添加了 “bus”	1
• 更改了 Device Information 表中的封装尺寸	1
• 替换了引脚排列图	4
• 在 Pin Functions 表中添加了 I/O 列	4

• Deleted RVH package from <i>Pin Configuration and Functions</i> section	4
• Moved T_{stg} from <i>Handling Ratings</i> to <i>Absolute Maximum Ratings</i>	5
• Added a note following the <i>Electrical Characteristics</i> table.....	6
• Added Figure 7-1 to the <i>Parameter Measurement Information</i> section.....	9
• Changed Figure 7-2	9
• Changed "repeater" to "level shifter" in second paragraph of the <i>Overview</i> section	10
• Deleted the last row of the Design Requirements table.	18
• Corrected equation from $f_{knee} = 0.5 / RT$ (10%–80%) to $f_{knee} = 0.5 / RT$ (10%–90%).....	19

Changes from Revision J (October 2010) to Revision K (December 2012)	Page
• Added <i>Pin Configuration and Functions</i> section, <i>Handling Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

• 从Pin Configuration and Functions部分删除了 RVH 封装.....	4
• 将 T _{stg} 从 Handling Ratings 移至绝对最大额定值.....	5
• 在 Electrical Characteristics 表后添加了注释.....	6
• 在 Parameter Measurement Information 部分添加了图 7-1.....	9
• 更改了 图 7-2	9
• 在 Overview 部分第二段中将 “repeater” 更改为 “level shifter”	10
• 删除了 Design Requirements 表的最后一行。	18
• 将公式从 f _{knee} = 0.5 / RT (10%–80%) 修正为 f _{knee} = 0.5 / RT (10%–90%).....	19

从修订版 J (2010年10月) 到修订版 K (2012年12月) 的变更

页码

• 新增了引脚配置及功能部分、Handling Rating表、Feature Description部分、Device Functional Modes、Application and Implementation部分、Power Supply Recommendations部分、Layout部分、Device and Documentation Support部分及Mechanical, Packaging, and Orderable Information 部分.....	1
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5 Pin Configuration and Functions

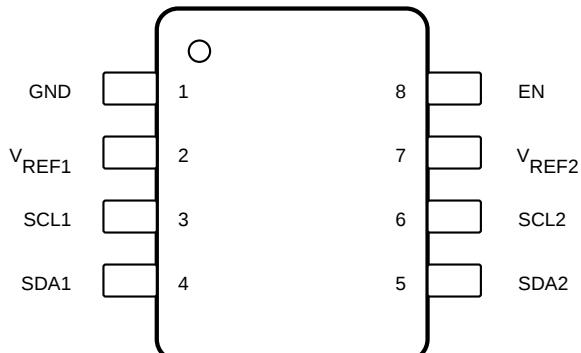


Figure 5-1. DCT Package 8-Pin SSOP (Top View)



Figure 5-2. DCU Package 8-Pin VSSOP (Top View)

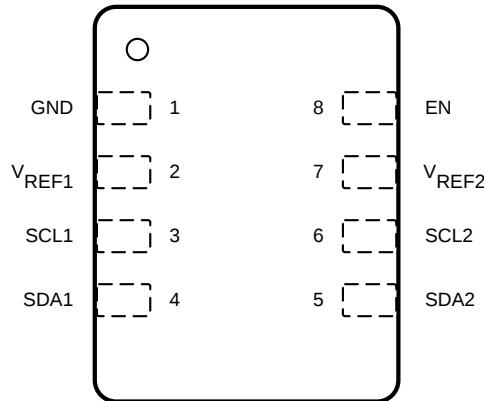


Figure 5-3. DQE Package 8-Pin X2SON (Top View)

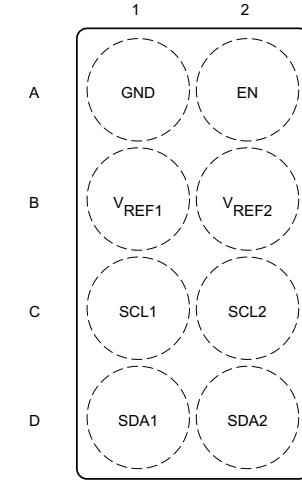


Figure 5-4. YZT Package 8-Pin DSBGA (Top View)

Table 5-1. Pin Functions

NAME	PIN		I/O	DESCRIPTION		
	NO.					
	DCT, DCU, DQE	YZT				
EN	8	A2	I	Switch enable input		
GND	1	A1	—	Ground, 0 V		
SCL1	3	C1	I/O	Serial clock, low-voltage side		
SCL2	6	C2	I/O	Serial clock, high-voltage side		
SDA1	4	D1	I/O	Serial data, low-voltage side		
SDA2	5	D2	I/O	Serial data, high-voltage side		
V _{REF1}	2	B1	I	Low-voltage-side reference supply voltage for SCL1 and SDA1		
V _{REF2}	7	B2	I	High-voltage-side reference supply voltage for SCL2 and SDA2		

5 引脚配置及功能

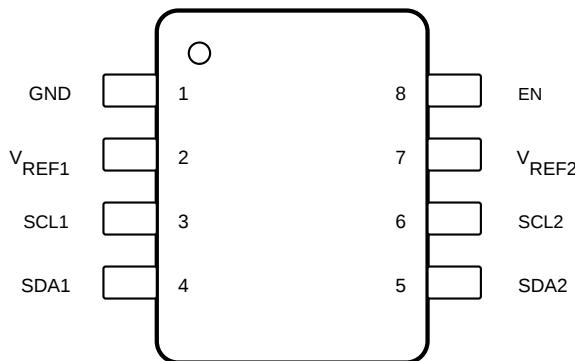


图 5-1. DCT 封装 8 引脚 SSOP (顶视图)



图 5-2. DCU 封装 8 引脚 VSSOP (顶视图)

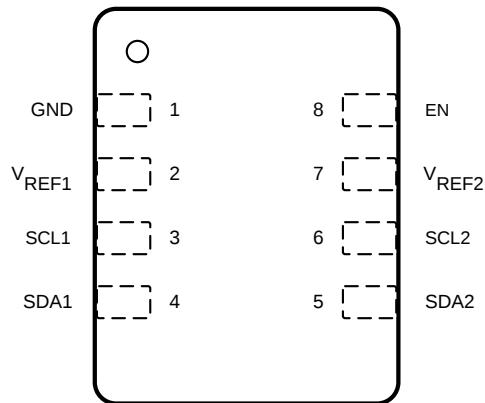


图 5-3. DQE 封装 8 引脚 X2SON (顶视图)

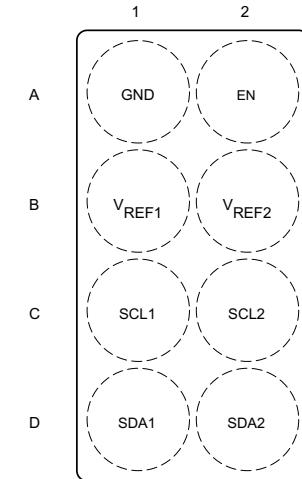


图 5-4. YZT 封装 8 引脚 DSBGA (顶视图)

表 5-1. 引脚功能

名称	引脚		输入输出	描述		
	编号					
	DCT, DCU, DQE	YZT				
EN	8	A2	I	开关使能输入		
GND	1	A1	—	接地, 0 V		
SCL1	3	C1	输入/输出	串行时钟, 低电压侧		
SCL2	6	C2	输入/输出	串行时钟, 高电压侧		
SDA1	4	D1	输入/输出	串行数据, 低电压侧		
SDA2	5	D2	输入/输出	串行数据, 高电压侧		
V _{REF1}	2	B1	I	SCL1 和 SDA1 的低电压侧参考电源电压		
V _{REF2}	7	B2	I	SCL2 和 SDA2 的高电压侧参考电源电压		

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) see ⁽¹⁾

		MIN	MAX	UNIT
V_{REF1}	DC reference voltage range	-0.5	7	V
V_{REF2}	DC reference bias voltage range	-0.5	7	V
V_I	Input voltage range ⁽²⁾	-0.5	7	V
$V_{I/O}$	Input/output voltage range ⁽²⁾	-0.5	7	V
	Continuous channel current		128	mA
I_{IK}	Input clamp current $V_I < 0$		-50	mA
$T_{j(max)}$	Maximum junction temperature		125	°C
T_{stg}	Storage temperature range	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and input/output negative voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	± 2000
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-0011, all pins ⁽²⁾	± 1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	5.5	V
V_{REF1} ⁽¹⁾	Reference voltage	0	5.5	V
V_{REF2} ⁽¹⁾	Reference voltage	0	5.5	V
EN	Enable input voltage	0	5.5	V
I_{PASS}	Pass switch current		64	mA
T_A	Operating ambient temperature	-40	85	°C

- (1) To support translation, V_{REF1} supports 1.2 V to $V_{REF2} - 0.6$ V. V_{REF2} must be between $V_{REF1} + 0.6$ V to 5.5 V. See [Section 9.2](#) for more information.

6 规格

6.1 绝对最大额定值

在工作环境温度范围内（除非另有说明），见 [\(1\)](#)

		最小值	最大值	单位
V_{REF1}	直流参考电压范围	-0.5	7	V
V_{REF2}	直流参考偏置电压范围	-0.5	7	V
V_I	输入电压范围 ⁽²⁾	-0.5	7	V
$V_{I/O}$	输入/输出电压范围 ⁽²⁾	-0.5	7	V
	连续通道电流		128	mA
I_{IK}	输入钳位电流 $V_I < 0$		-50	mA
$T_{j(max)}$	最大结温		125	°C
T_{stg}	存储温度范围	-65	150	°C

(1) 在绝对最大额定值之外操作可能导致器件永久损坏。绝对最大额定值并不意味着器件在这些或任何超出推荐工作条件的条件下能够正常工作。

如果短时间在推荐工作条件之外但在绝对最大额定值范围内操作，器件可能不会损坏，但可能无法完全正常工作。以此方式操作可能影响器件的可靠性、功能、性能，并缩短器件寿命。

(2) 若遵守输入和输入/输出电流额定值，输入和输入/输出负电压额定值可被超越。

6.2 静电放电 (ESD) 额定值

		数值	单位
$V_{(ESD)}$	静电放电	人体模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001，所有引脚 ⁽¹⁾	± 2000
		带电器件模型 (CDM)，符合 ANSI/ESDA/JEDEC JS-0011，所有引脚 ⁽²⁾	± 1000

(1) JEDEC 文档 JEP155 规定 500-V HBM 允许采用标准静电放电控制工艺进行安全制造。

(2) JEDEC 文档 JEP157 规定 250-V CDM 允许采用标准静电放电控制工艺进行安全制造。

6.3 推荐工作条件

		最小值	最大值	单位
$V_{I/O}$	输入/输出电压	SCL1, SDA1, SCL2, SDA2	0	5.5
V_{REF1} ⁽¹⁾	参考电压		0	5.5
V_{REF2} ⁽¹⁾	参考电压		0	5.5
EN	使能输入电压		0	5.5
I_{PASS}	通断开关电流		64	mA
T_A	工作环境温度	-40	85	°C

(1) 为支持电平转换， V_{REF1} 支持 1.2 V 至 V_{REF2} - 0.6 V。 V_{REF2} 必须在 $V_{REF1} + 0.6$ V 至 5.5 V 之间。详见章节 [9.2](#) 了解更多信息。

[9.2](#) 了解更多

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	PCA9306				UNIT
	DCT	DCU	DQE	YZT	
	8 PINS	8 PINS	8 PINS	8 PINS	
R _{θJA} Junction-to-ambient thermal resistance	254.1	275.5	299.3	125.5	°C/W
R _{θJC(top)} Junction-to-case (top) thermal resistance	148.6	127.1	166.9	1	°C/W
R _{θJB} Junction-to-board thermal resistance	168.8	186.9	188.30	62.7	°C/W
Ψ _{JT} Junction-to-top characterization parameter	70.1	65.7	18.0	3.4	°C/W
Ψ _{JB} Junction-to-board characterization parameter	167.4	185.9	187.4	62.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{IK}	Input clamp voltage	I _I = -18 mA,	EN = 0 V	-1.2	0	0	V	
I _{IH}	Input leakage current	V _I = 5 V,	EN = 0 V		5	5	µA	
C _i (EN)	Input capacitance	V _I = 3 V or 0			11	11	pF	
C _{io(off)}	Off capacitance	SCLn, SDAn	V _O = 3 V or 0, EN = 0 V		4	6	pF	
C _{io(on)}	On capacitance	SCLn, SDAn	V _O = 3 V or 0, EN = 3 V		10.5	12.5	pF	
R _{ON} ⁽²⁾	On-state resistance	SCLn, SDAn	V _I = 0	I _O = 64 mA	EN = 4.5 V	3.5	5.5	Ω
					EN = 3 V	4.7	7	
					EN = 2.3 V	6.3	9.5	
			V _I = 2.4 V ⁽³⁾	I _O = 15 mA	EN = 1.5 V	25.5	32	
					EN = 4.5 V	1	6	
			V _I = 1.7 V ⁽³⁾	I _O = 15 mA	EN = 3 V	20	60	
					EN = 2.3 V	20	60	

(1) All typical values are at T_A = 25°C.

(2) Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals, at the indicated current through the switch. Minimum ON-state resistance is determined by the lowest voltage of the two terminals.

(3) Measured in current sink configuration only (See [Figure 7-1](#))

6.4 热特性信息

热特性指标 ⁽¹⁾	PCA9306				单位
	DCT	DCU	DQE	YZT	
	8 引脚	8 引脚	8 引脚	8 引脚	
R _{θJA} 结点到环境的热阻	254.1	275.5	299.3	125.5	°C/W
R _{θJC(top)} 结点到封装顶部的热阻	148.6	127.1	166.9	1	°C/W
R _{θJB} 结点到电路板的热阻	168.8	186.9	188.30	62.7	°C/W
Ψ _{JT} 结点到顶部的特征参数	70.1	65.7	18.0	3.4	°C/W
Ψ _{JB} 结点到电路板的特征参数	167.4	185.9	187.4	62.7	°C/W

(1) 有关传统及新型热特性指标的更多信息，请参见《半导体与集成电路封装热特性指标》应用报告。

6.5 电气特性

超过推荐的工作环境温度范围（除非另有说明）

参数		测试条件		最小值	典型值 ⁽¹⁾	最大值	单位
V _{IK}	输入钳位电压	I _I = -18 mA,	EN = 0 V	-1.2	0	0	V
I _{IH}	输入漏电流	V _I = 5 V,	EN = 0 V		5	μA	
C _{i (EN)}	输入电容	V _I = 3 V 或 0		11		pF	
C _{io(off)}	断开电容	SCLn, SDAn	V _O = 3 V 或 0, EN = 0 V	4	6	6	pF
C _{io(on)}	导通电容	SCLn, SDAn	V _O = 3 V 或 0, EN = 3 V	10.5	12.5	12.5	pF
R _{ON} ⁽²⁾ 导通电阻	SCLn, SDAn	V _I = 0	I _O = 64 mA	EN = 4.5 V	3.5	5.5	Ω
				EN = 3 V	4.7	7	
				EN = 2.3 V	6.3	9.5	
		V _I = 2.4 V ⁽³⁾	I _O = 15 mA	EN = 1.5 V	25.5	32	
				EN = 4.5 V	1	6	
		V _I = 1.7 V ⁽³⁾	I _O = 15 mA	EN = 3 V	20	60	
				EN = 2.3 V	20	60	

(1) 所有典型值均在 T_A = 25°C 下测量。

(2) 通过开关时的指定电流，在 SCL1 和 SCL2 端子或 SDA1 和 SDA2 端子之间的电压降测量所得。

最小导通电阻由两个端子中较低电压决定。

(3) 仅在电流吸收配置下测量（参见图 7-1）

6.6 Switching Characteristics AC Performance (Translating Down) (EN = 3.3 V)

over recommended operating ambient temperature range, EN = 3.3 V, $V_{IH} = 3.3$ V, $V_{IL} = 0$, $V_M = 1.15$ V (unless otherwise noted) (see [Figure 7-1](#)).

PARAMETER ⁽¹⁾	FROM (INPUT)	TO (OUTPUT)	Package	$C_L = 50$ pF		$C_L = 30$ pF		$C_L = 15$ pF		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	YZT, DQE	0	0.8	0	0.6	0	0.3	ns
t_{PHL}				0	1.2	0	1	0	0.5	
								0	0.75	

(1) Translating down: the high-voltage side driving toward the low-voltage side

6.7 Switching Characteristics AC Performance (Translating Down) (EN = 2.5 V)

over recommended operating ambient temperature range, EN = 2.5 V, $V_{IH} = 3.3$ V, $V_{IL} = 0$, $V_M = 0.75$ V (unless otherwise noted) (see [Figure 7-1](#)).

PARAMETER ⁽¹⁾	FROM (INPUT)	TO (OUTPUT)	Package	$C_L = 50$ pF		$C_L = 30$ pF		$C_L = 15$ pF		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	YZT, DQE	0	1	0	0.7	0	0.4	ns
t_{PHL}				0	1.3	0	1	0	0.6	
								0	0.75	

(1) Translating down: the high-voltage side driving toward the low-voltage side

6.8 Switching Characteristics AC Performance (Translating Up) (EN = 3.3 V)

over recommended operating ambient temperature range, EN = 3.3 V, $V_{IH} = 2.3$ V, $V_{IL} = 0$, $V_T = 3.3$ V, $V_M = 1.15$ V, $R_L = 300$ Ω (unless otherwise noted) (see [Figure 7-1](#)).

PARAMETER ⁽¹⁾	FROM (INPUT)	TO (OUTPUT)	Packages	$C_L = 50$ pF		$C_L = 30$ pF		$C_L = 15$ pF		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL1 or SDA1	SCL2 or SDA2	YZT, DQE	0	0.9	0	0.6	0	0.4	ns
t_{PHL}				0	1.4	0	1.1	0	0.7	
					1.7			0	1.0	

(1) Translating up: the low-voltage side driving toward the high-voltage side

6.9 Switching Characteristics AC Performance (Translating Up) (EN = 2.5 V)

over recommended operating ambient temperature range, EN = 2.5 V, $V_{IH} = 2.3$ V, $V_{IL} = 0$, $V_T = 3.3$ V, $V_M = 0.75$ V, $R_L = 300$ Ω (unless otherwise noted) (see [Figure 7-1](#)).

PARAMETER ⁽¹⁾	FROM (INPUT)	TO (OUTPUT)	Packages	$C_L = 50$ pF		$C_L = 30$ pF		$C_L = 15$ pF		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL1 or SDA1	SCL2 or SDA2	YZT, DQE	0	1	0	0.6	0	0.4	ns
t_{PHL}				0	1.3	0	1.3	0	0.8	
					2.1			0	1.3	

(1) Translating up: the low-voltage side driving toward the high-voltage side

6.6 开关特性 交流性能（向下转换）（EN = 3.3 V）

在推荐的工作环境温度范围内，EN = 3.3 V, V_{IH} = 3.3 V, V_{IL} = 0, V_M = 1.15 V（除非另有说明）（参见图 7-1）。

参数	(1)	来自 (输入)	至 (输出)	封装	C _L = 50 pF		C _L = 30 pF		C _L = 15 pF					
					最小值	最大值	最小值	最大值	最小值	最大值				
t _{PLH}	SCL2 或 SDA2	SCL1 或 SDA1			0	0.8	0	0.6	0	0.3				
t _{PHL}					YZT, DQE	0	1.2	0	1	0.5				
					DCU, DCT					0.75				

(1) 向下转换：高电压侧驱动至低电压侧

6.7 开关特性 交流性能（向下转换）（EN = 2.5 V）

在推荐的工作环境温度范围内，EN = 2.5 V, V_{IH} = 3.3 V, V_{IL} = 0, V_M = 0.75 V（除非另有说明）（参见图 7-1）。

参数	(1)	来自 (输入)	至 (输出)	封装	C _L = 50 pF		C _L = 30 pF		C _L = 15 pF					
					最小值	最大值	最小值	最大值	最小值	最大值				
t _{PLH}	SCL2 或 SDA2	SCL1 或 SDA1			0	1	0	0.7	0	0.4				
t _{PHL}					YZT, DQE	0	1.3	0	1	0.6				
					DCT, DCU					0.75				

(1) 向下转换：高电压侧驱动至低电压侧

6.8 开关特性 交流性能（向上转换）（EN = 3.3 V）

在推荐的工作环境温度范围内，EN = 3.3 V, V_{IH} = 2.3 V, V_{IL} = 0, V_T = 3.3 V, V_M = 1.15 V, R_L = 300 Ω（除非另有说明）（参见图 7-1）。

参数	(1)	来自 (输入)	至 (输出)	封装	C _L = 50 pF		C _L = 30 pF		C _L = 15 pF					
					最小值	最大值	最小值	最大值	最小值	最大值				
t _{PLH}	SCL1 或 SDA1	SCL2 或 SDA2			0	0.9	0	0.6	0	0.4				
t _{PHL}					YZT, DQE	0	1.4	0	1.1	0.7				
					DCU, DCT					1.0				

(1) 向上转换：低电压侧驱动至高电压侧

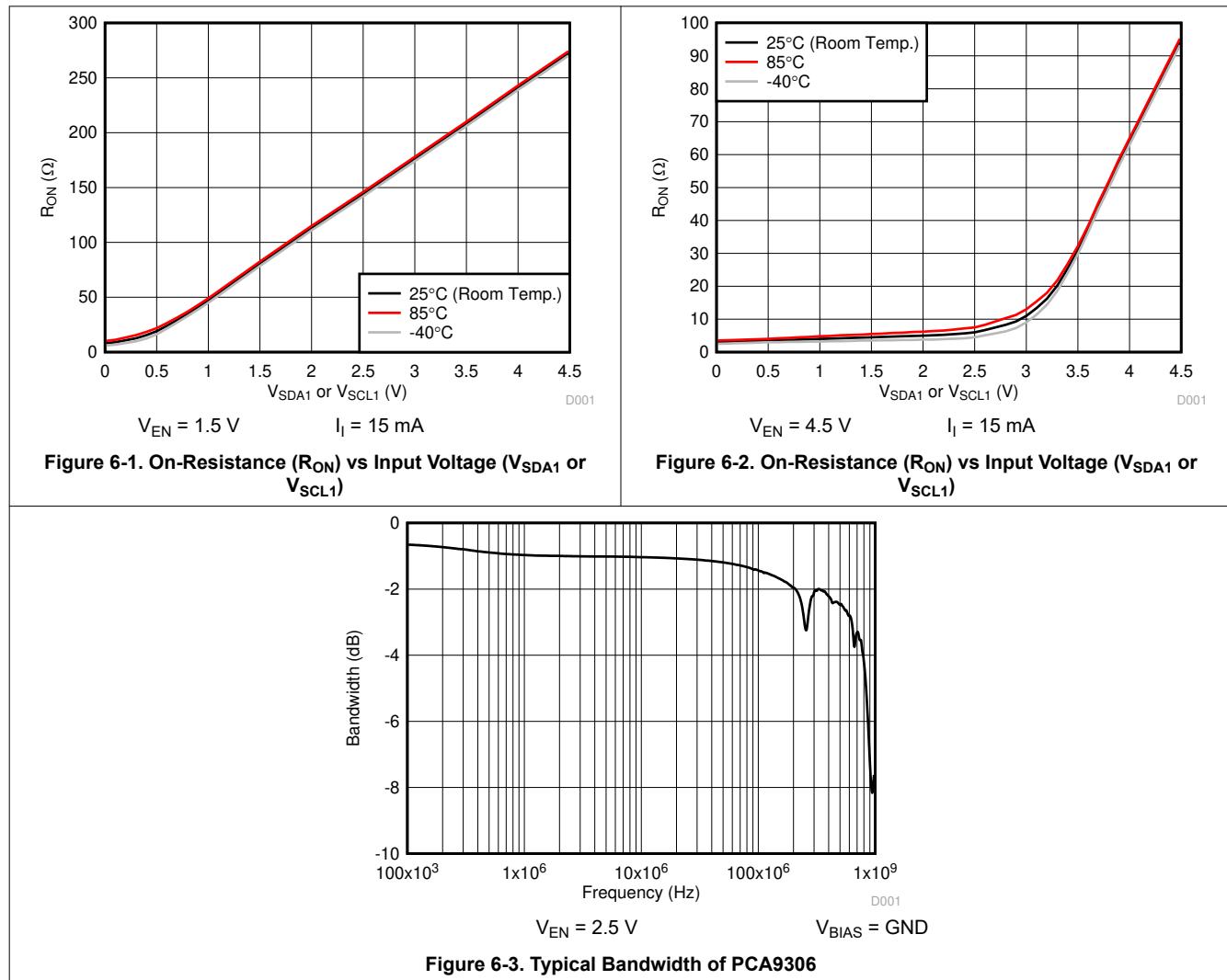
6.9 开关特性 交流性能（向上转换）（EN = 2.5 V）

在推荐的工作环境温度范围内，EN = 2.5 V, V_{IH} = 2.3 V, V_{IL} = 0, V_T = 3.3 V, V_M = 0.75 V, R_L = 300 Ω（除非另有说明）（参见图 7-1）。

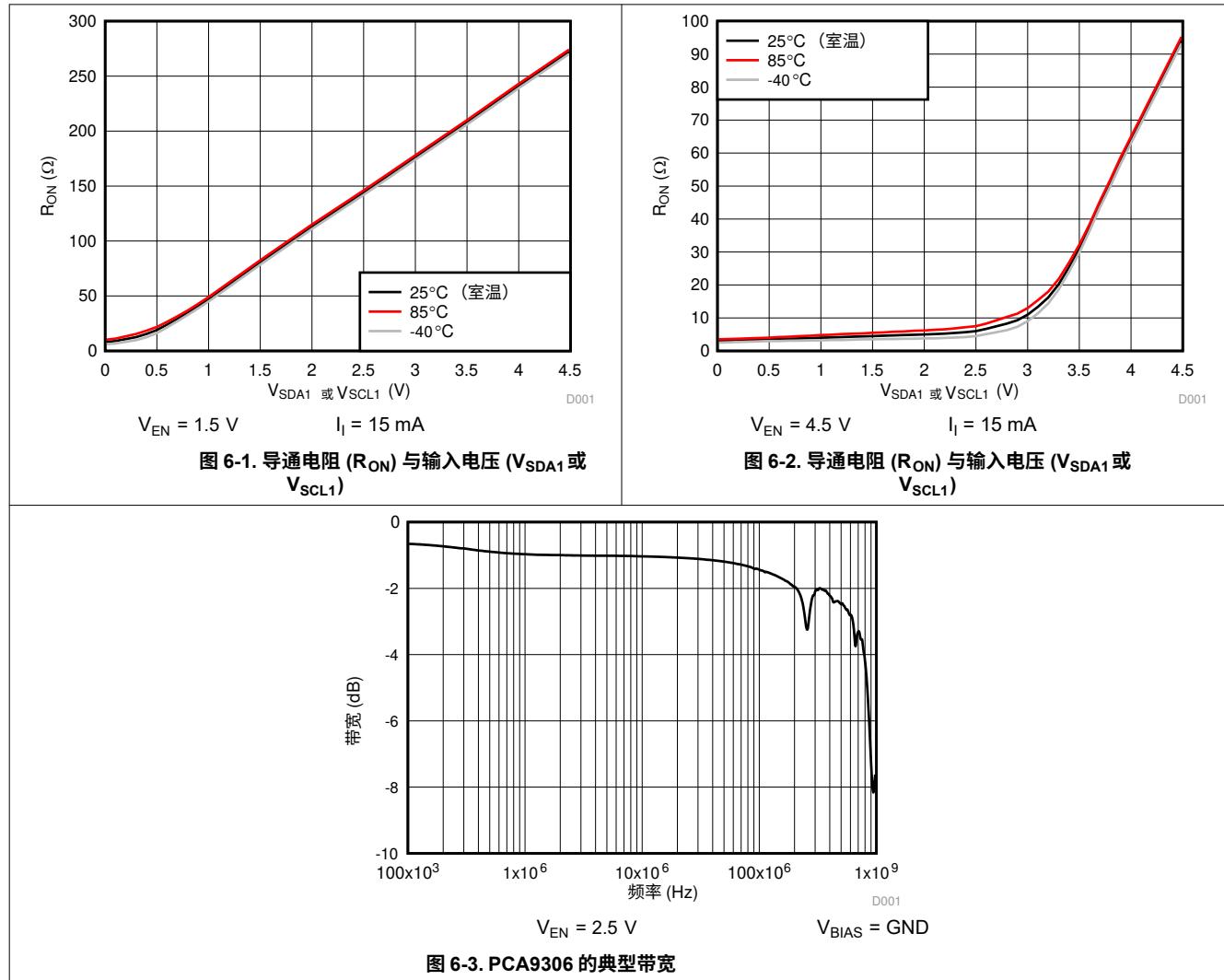
参数	(1)	来自 (输入)	至 (输出)	封装	C _L = 50 pF		C _L = 30 pF		C _L = 15 pF					
					最小值	最大值	最小值	最大值	最小值	最大值				
t _{PLH}	SCL1 或 SDA1	SCL2 或 SDA2			0	1	0	0.6	0	0.4				
t _{PHL}					YZT, DQE	0	1.3	0	1.3	0.8				
					DCT, DCU					1.3				

(1) 向上转换：低电压侧驱动至高电压侧

6.10 Typical Characteristics



6.10 典型特性



7 Parameter Measurement Information

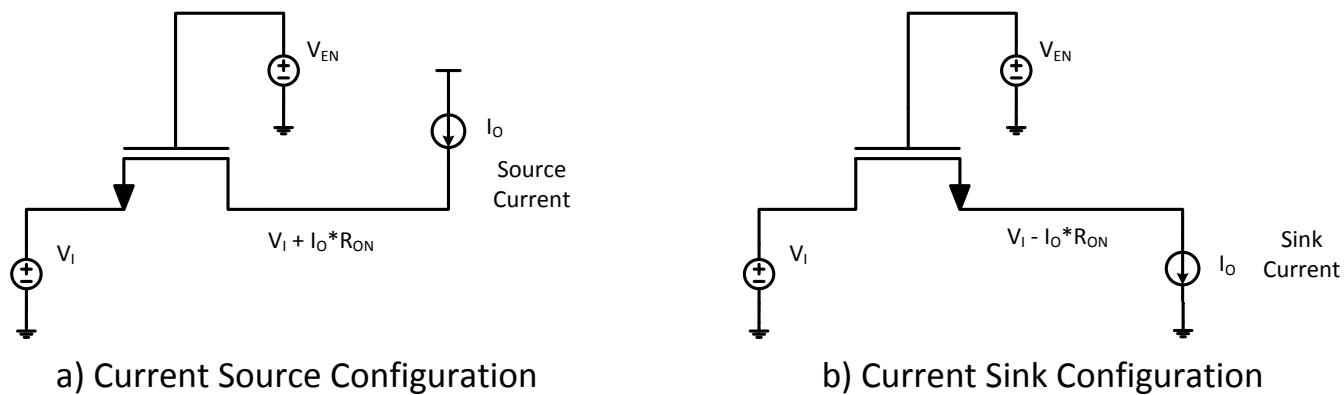
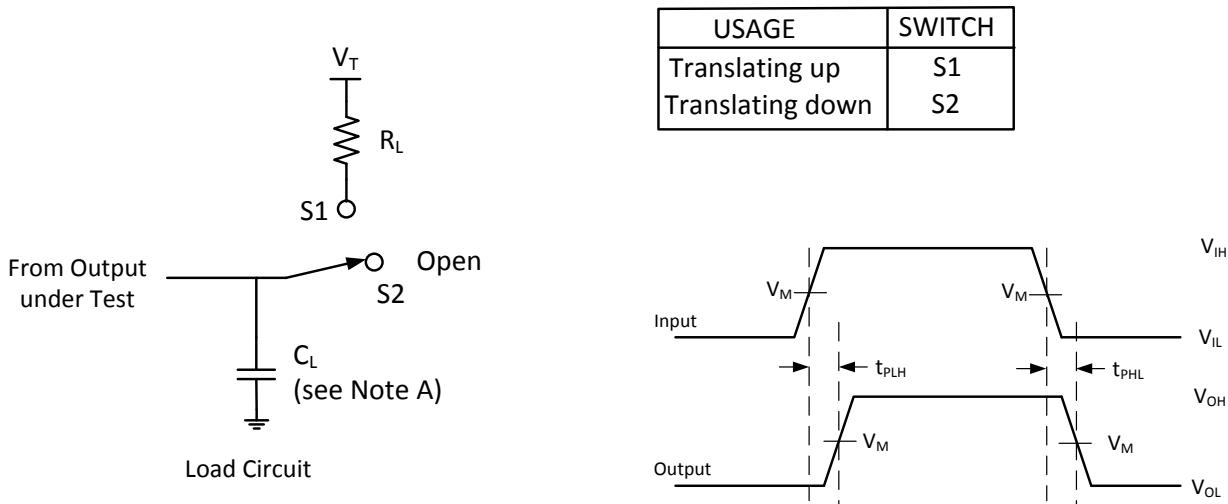


Figure 7-1. Current Source and Current Sink Configurations for R_{ON} Measurements



NOTES: A. C_L includes probe and jig capacitance

B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 7-2. Load Circuit for Outputs

7 参数测量信息

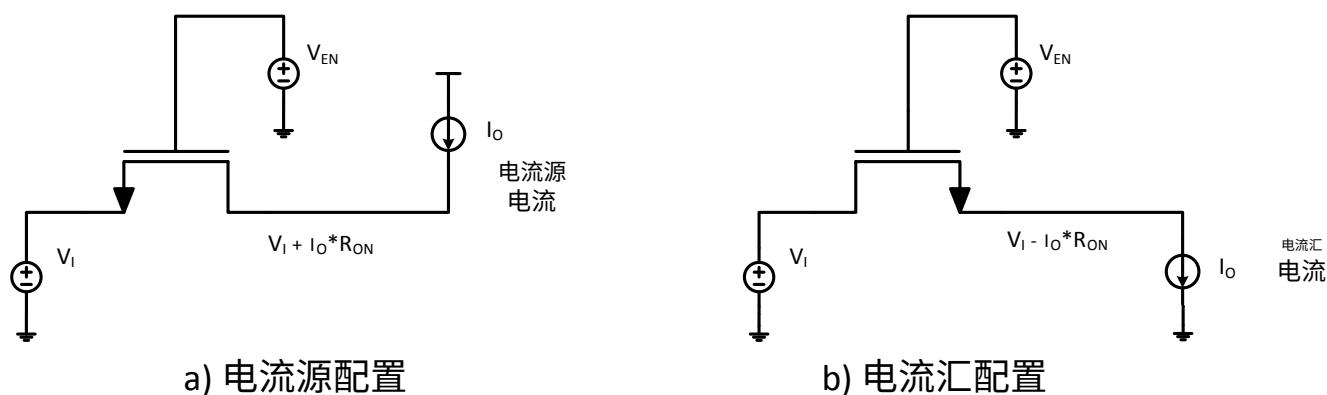
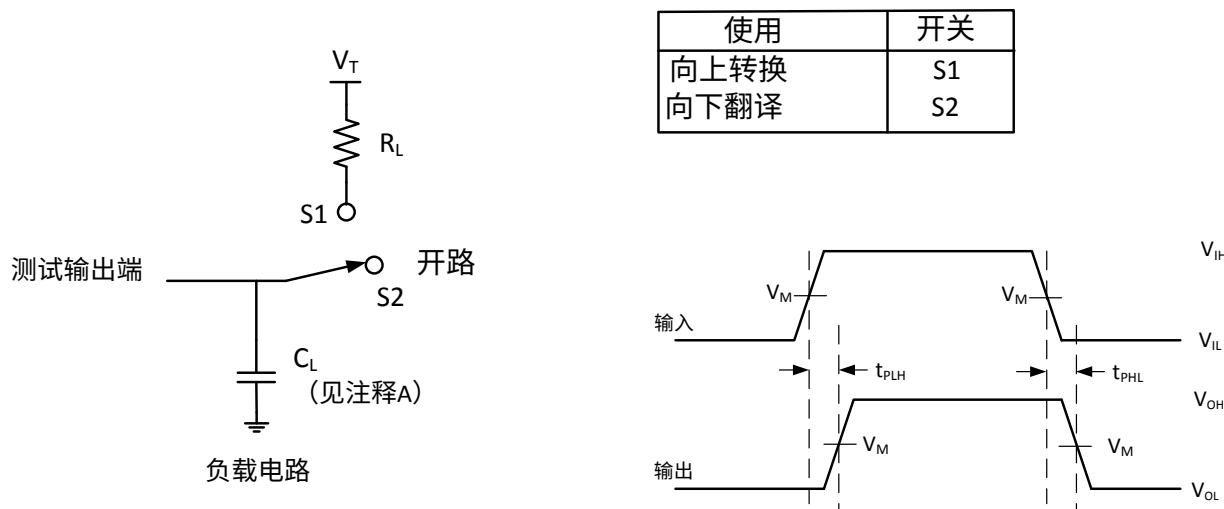


图 7-1. R_{ON} 测量的电流源和电流汇配置



注释：A. C_L 包括探头和夹具电容
 B. 所有输入脉冲均由具有以下特性的信号发生器提供：PRR ≤ 10 MHz, $Z_0 = 50\Omega$, trG 2 ns, tfG 2 ns。
 C. 输出逐个测量，每次测量包含一次转换。

图 7-2. 输出负载电路

8 Detailed Description

8.1 Overview

The PCA9306 device is a dual bidirectional I²C and SMBus voltage-level translator with an enable (EN) input and operates without use of a direction pin. The voltage supply range for V_{REF1} is 1.2 V to 3.3 V and the supply range for V_{REF2} is 1.8 V to 5.5 V.

The PCA9306 device can also be used to run two buses, one at 400-kHz operating frequency and the other at 100-kHz operating frequency. If the two buses are operating at different frequencies, the 100-kHz bus must be disconnected by using the EN pin when the 400-kHz operation of the main bus is required. If the controller is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the level shifter.

In I²C applications, the bus capacitance limit of 400 pF restricts the number of devices and bus length. The capacitive load on both sides of the PCA9306 device must be taken into account when approximating the total load of the system, ensuring the sum of both sides is under 400 pF.

Both the SDA and SCL channels of the PCA9306 device have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete-transistor voltage-translation solutions, because the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower-voltage devices and at the same time protects less-ESD-resistant devices.

8.1.1 Definition of threshold voltage

This document references a threshold voltage denoted as V_{th}, which appears multiple times throughout this document when discussing the NFET between V_{REF1} and V_{REF2}. The value of V_{th} is approximately 0.6 V at room temperature.

8.1.2 Correct Device Set Up

In a normal set up shown in [Figure 8-1](#), the enable pin and V_{REF2} are shorted together and tied to a 200-kΩ resistor, and a reference voltage equal to V_{REF1} plus the FET threshold voltage is established. This reference voltage is used to help pass lows from one side to another more effectively while still separating the different pull up voltages on both sides.

8 详细描述

8.1 概述

PCA9306 器件是一款带使能 (EN) 输入的双路双向 I²C 和 SMBus 电压电平转换器，无需使用方向引脚。V_{REF1} 的电压供电范围为 1.2 V 至 3.3 V，V_{REF2} 的供电范围为 1.8 V 至 5.5 V。

PCA9306 器件还可用于驱动两条总线，一条工作频率为 400 kHz，另一条工作频率为 100 kHz。如果两条总线工作于不同频率，当主总线需要 400 kHz 工作时，必须通过 EN 引脚断开 100 kHz 总线。如果控制器以 400 kHz 运行，由于电平转换器引入的延迟，系统最大工作频率可能低于 400 kHz。

在 I²C 应用中，400 pF 的总线电容限制了设备数量和总线长度。在估算系统总负载时，必须考虑 PCA9306 器件两侧的电容负载，确保两侧负载之和低于 400 pF。

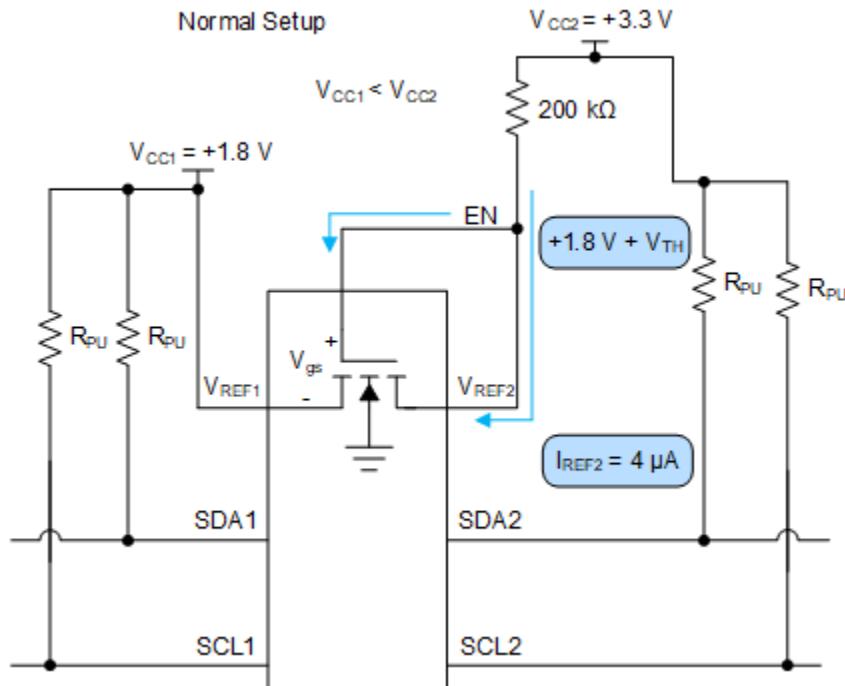
PCA9306 器件的 SDA 和 SCL 通道具有相同的电气特性，且各输出之间的电压或传播延迟偏差极小。这相较于分立晶体管电压转换方案具有优势，因为开关的制造工艺是对称的。该转换器为低电压器件提供优异的静电放电 (ESD) 保护，同时也保护了抗静电能力较弱的器件。

8.1.1 阈值电压的定义

本文档中多次提及的阈值电压记作 V_{th}，指的是 V_{REF1} 和 V_{REF2} 之间的 N 沟场效应晶体管。V_{th} 的值在室温下约为 0.6 V。

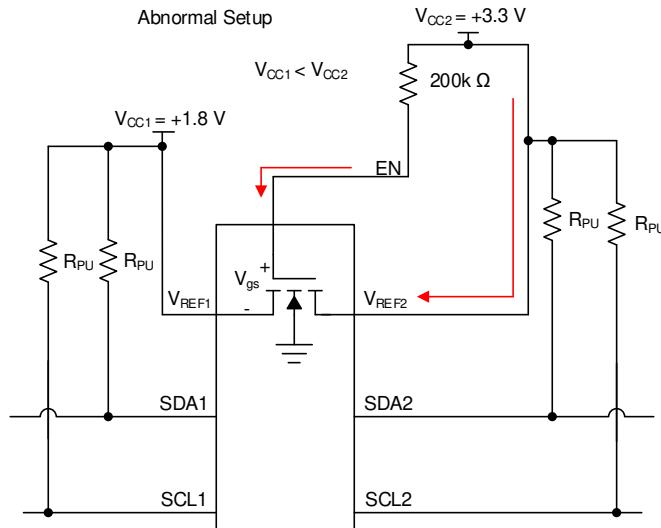
8.1.2 正确的器件设置

在图 8-1 所示的正常设置中，使能引脚和 V_{REF2} 短接并通过一个 200 kΩ 电阻连接，同时建立一个等于 V_{REF1} 加 FET 阈值电压的参考电压。该参考电压用于更有效地传递低电平信号，同时仍隔离两侧不同的上拉电压。

**Figure 8-1. Normal Setup**

Care should be taken to make sure V_{REF2} has an external resistor tied between it and V_{CC2} . If V_{REF2} is tied directly to the V_{CC2} rail without a resistor, then there is no external resistance from the V_{CC2} to V_{CC1} to limit the current such as in [Figure 8-2](#). This effectively looks like a low impedance path for current to travel through and potentially break the pass FET if the current flowing through the pass FET is larger than the absolute maximum continuous channel current specified in section 6.1. The continuous channel current is larger with a higher voltage difference between V_{CC1} and V_{CC2} .

[Figure 8-2](#) shows an improper set up. If V_{CC2} is larger than V_{CC1} but less than V_{th} , the impedance between V_{CC1} and V_{CC2} is high resulting in a low drain to source current, which does not cause damage to the device. Concern arises when V_{CC2} becomes larger than V_{CC1} by V_{th} . During this event, the NFET turns on and begin to conduct current. This current is dependent on the gate to source voltage and drain to source voltage.

**Figure 8-2. Abnormal Setup**

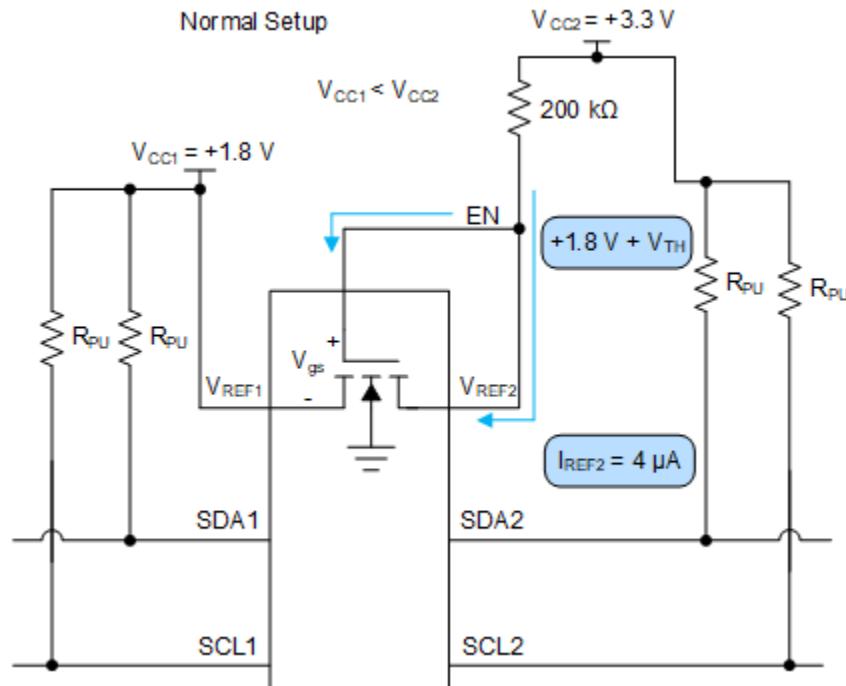


图8-1 正常设置

应确保 V_{REF2} 与 V_{CC2} 之间连接有外部电阻。如果 V_{REF2} 直接连接至 V_{CC2} 轨且无电阻，则如图8-2所示， V_{CC2} 到 V_{CC1} 之间无外部电阻限制电流。这实际上表现为一个低阻抗路径，电流可以通过该路径流动，且如果流经通道场效应晶体管的电流超过第6.1节中规定的绝对最大连续通道电流，可能会损坏通道场效应晶体管。连续通道电流随着 V_{C1} 和 V_{CC2} 之间电压差的增大而增大。

图8-2显示了一个不正确的设置。如果 V_{CC2} 大于 V_{CC1} 但小于 V_{th} ， V_{CC1} 与 V_{CC2} 之间的阻抗较高，导致漏极到源极电流较低，不会对器件造成损害。当 V_{CC2} 比 V_{CC1} 大 V_{th} 时，会引发关注。在此情况下，N沟场效应晶体管导通并开始传导电流。该电流取决于栅极到源极电压和漏极到源极电压。

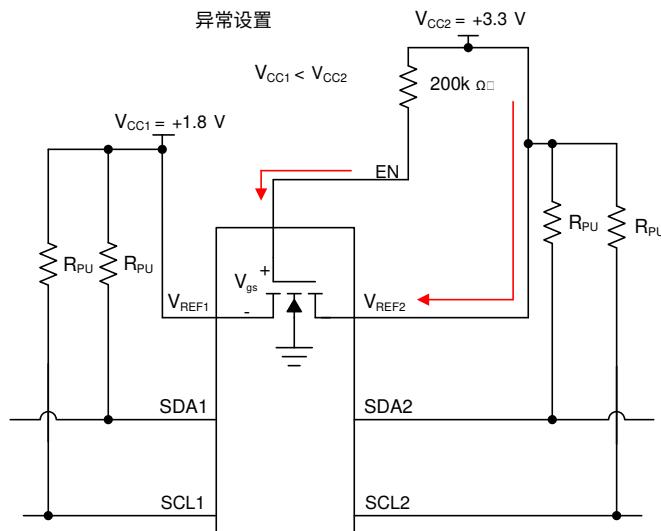


图8-2. 异常设置

8.1.3 Disconnecting an I²C target from the Main I²C Bus Using the EN Pin

PCA9306 can be used as a switch to disconnect one side of the device from the main I²C bus. This can be advantageous in multiple situations. One instance of this situation is if there are devices on the I²C bus which only supports fast mode (400 kHz) while other devices on the bus support fast mode plus (1 MHz). An example of this is displayed in [Figure 8-3](#).

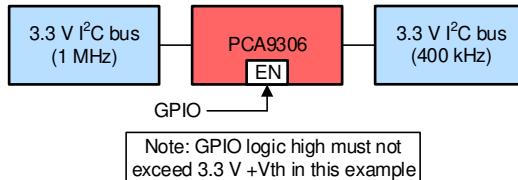


Figure 8-3. Example of an I²C bus with multiple supported frequencies

In this situation, if the controller is on the 1 MHz side then communicating at 1 MHz should not be attempted if PCA9306 were enabled. It needs to be disabled for PCA9306 to avoid possibly glitching state machines in devices which were designed to operate correctly at 400 kHz or slower. When PCA9306 is disabled, the controller can communicate with the 1 MHz devices without disturbing the 400 kHz bus. When the PCA9306 is enabled, communication across both sides at 400 kHz is acceptable.

8.1.4 Supporting Remote Board Insertion to Backplane with PCA9306

Another situation where PCA9306 is advantageous when using its enable feature is when a remote board with I²C lines needs to be attached to a main board (backplane) with an I²C bus such as in [Figure 8-4](#). If connecting a remote board to a backplane is not done properly, the connection could result in data corruption during a transaction or the insertion could generate an unintended pulse on the SCL line. Which could glitch an I²C device state machine causing the I²C bus to get stuck.

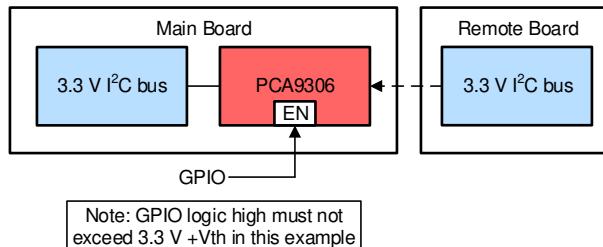


Figure 8-4. An example of connecting a remote board to a main board (backplane)

PCA9306 can be used to support this application because it can be disabled while making the connection. Then it is enabled once the remote board is powered on and the buses on both sides are IDLE.

8.1.5 Switch Configuration

PCA9306 has the capability of being used with its V_{REF1} voltage equal to V_{REF2} . This essentially turns the device from a translator to a device which can be used as a switch, and in some situations this can be useful. The switch configuration is shown in [Figure 8-5](#) and translation mode is shown in [Figure 8-6](#).

8.1.3 使用 EN 引脚断开 I2C 目标与主 I2C 总线的连接

PCA9306 可用作开关，将器件一侧从主 I2C 总线断开，这在多种情况下具有优势。一种情况是，I2C 总线上存在仅支持快速模式（400 kHz）的设备，而总线上其他设备支持快速模式增强（1 MHz）。示例见图 8-3。

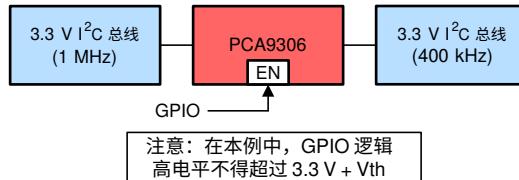


图 8-3. 支持多种频率的 I2C 总线示例

在这种情况下，如果控制器位于 1 MHz 侧，则不应尝试以 1 MHz 进行通信。

如果启用了 PCA9306。必须禁用它，以避免 PCA9306 可能导致设计用于在 400 kHz 或更低速率下正常工作的设备中的状态机出现毛刺。当 PCA9306 被禁用时，控制器可以与 1 MHz 设备通信而不会干扰 400 kHz 总线；当 PCA9306 被启用时，允许两侧以 400 kHz 进行通信。

8.1.4 使用 PCA9306 支持远程板插入背板

PCA9306 启用功能的另一个优势是在需要将带有 I2C 线路的远程板连接到带有 I2C 总线的主板（背板）时，如图 8-4 所示。如果远程板与背板的连接不当，可能导致事务期间数据损坏，或插入时在 SCL 线上产生意外脉冲。这可能导致 I2C 设备状态机出现毛刺，进而使 I2C 总线卡死。

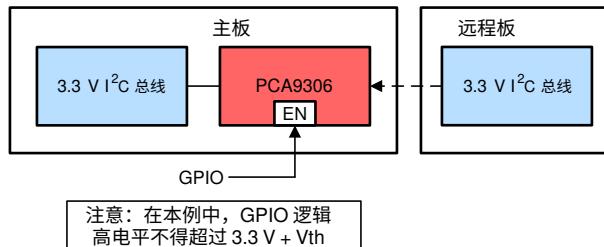
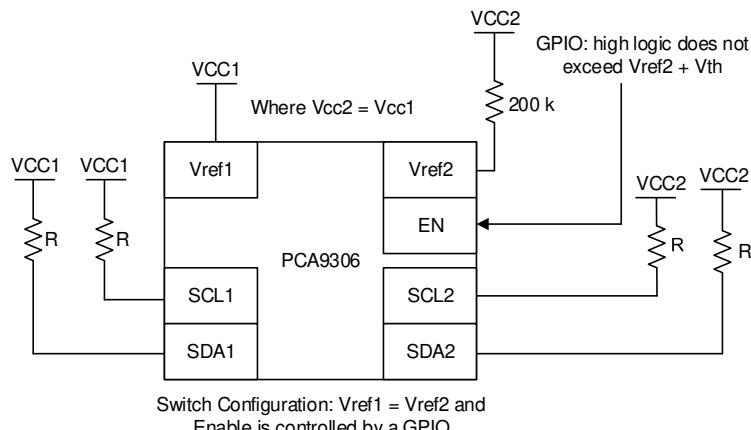
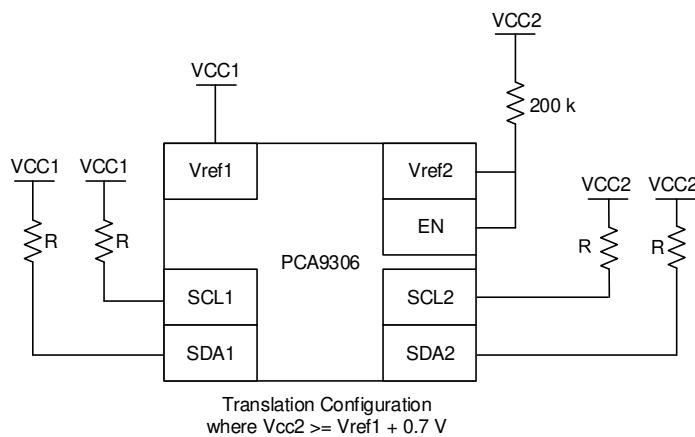


图 8-4. 将远程板连接至主板（背板）的示例

PCA9306 可用于支持此应用，因为它在连接时可以被禁用。然后，一旦远程板上电且两侧总线均处于空闲状态，设备即被启用。

8.1.5 开关配置

PCA9306 具备在 V_{REF1} 电压等于 V_{REF2} 时使用的能力。这本质上将器件从电平转换器变为可用作开关的器件，在某些情况下非常有用。开关配置如图 8-5 所示，转换模式如图 8-6 所示。

**Figure 8-5. Switch Configuration****Figure 8-6. Translation Configuration**

When PCA9306 is in the switch configuration ($V_{REF1} = V_{REF2}$), the propagation delays are different compared to the translator configuration. Taking a look at the propagation delays, if the pull up resistance and capacitance on both sides of the bus are equal, then in switch mode the PCA9306 has the same propagation delay from side one to two and side two to one. The propagation delays become lower when V_{CC1}/V_{CC2} is larger. For example, the propagation delay at 1.8 V is longer than at 5 V in the switching configuration. When PCA9306 is in translation mode, side one propagate lows to side two faster than side two can propagate lows to side 1. This time difference becomes larger the larger the difference between V_{CC2} and V_{CC1} becomes.

8.1.6 Controller on Side 1 or Side 2 of Device

I2C and SMBus are bidirectional protocol meaning devices on the bus can both transmit and receive data. PCA9306 was designed to allow for signals to be able to be transmitted from either side, thus allowing for the controller to be able to placed on either side of the device. [Figure 8-7](#) shows the controller on side two as opposed to the diagram on page 1 of this data sheet.

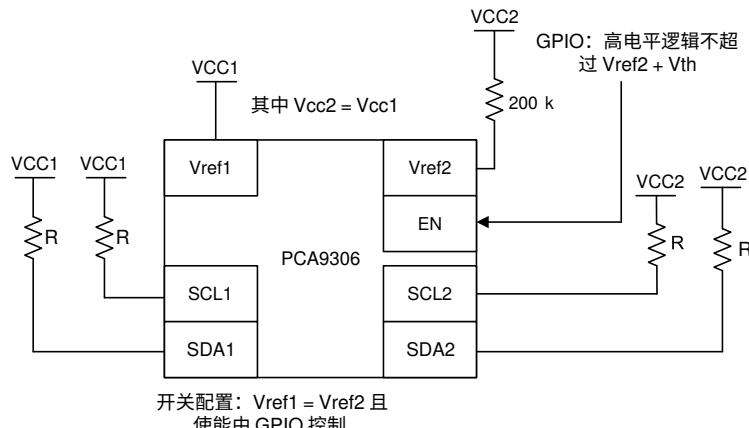


图 8-5. 开关配置

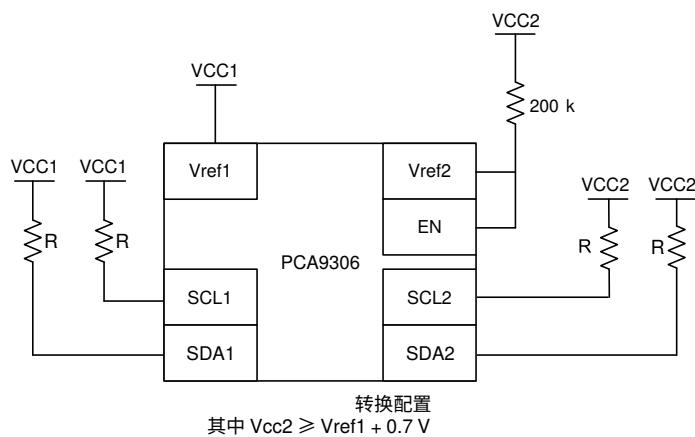


图 8-6. 转换配置

当 PCA9306 处于开关配置 ($V_{REF1}=V_{REF2}$) 时，传播延迟与转换器配置相比有所不同。观察传播延迟，如果总线两侧的上拉电阻和电容相等，则在开关模式下，PCA9306 从侧一到侧二和从侧二到侧一的传播延迟相同。当 V_{CC_1}/V_{CC_2} 较大时，传播延迟降低。例如，在开关配置中，1.8 V 下的传播延迟比 5 V 下更长。当 PCA9306 处于电平转换模式时，侧一传递低电平到侧二的速度快于侧二传递低电平到侧一的速度。随着 V_{CC_2} 与 V_{CC_1} 之间差异的增大，该时间差也随之增大。

8.1.6 设备侧一或侧二的控制器

I2C 和 SMBus 是双向协议，意味着总线上的设备既可发送也可接收数据。

PCA9306 设计允许信号从任一侧传输，从而使控制器能够放置于设备的任一侧。图 8-7 显示了控制器位于侧二，与本数据手册第 1 页的示意图不同。

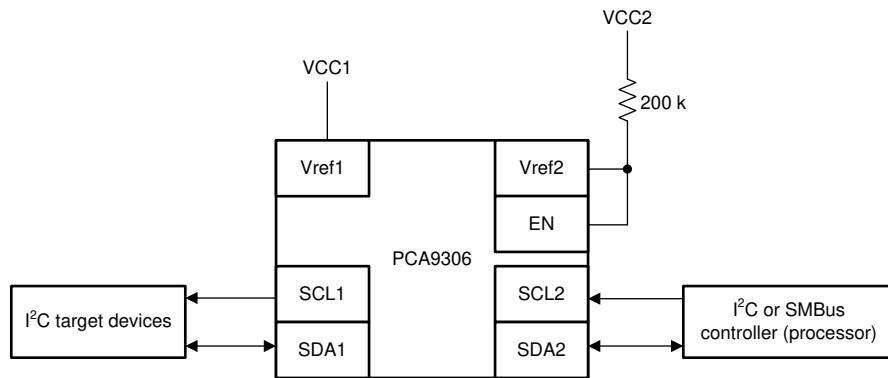


Figure 8-7. Controller on side 2 of PCA9306

8.1.7 LDO and PCA9306 Concerns

The V_{REF1} pin can be supplied by a low-dropout regulator (LDO), but in some cases the LDO may lose its regulation because of the bias current from V_{REF2} to V_{REF1} . If the LDO cannot sink the bias current, then the current has no other paths to ground and instead charges up the capacitance on the V_{REF1} node (both external and parasitic). This results in an increase in voltage on the V_{REF1} node. If no other paths for current to flow are established (such as back biasing of body diodes or clamping diodes through other devices on the V_{REF1} node), then the V_{REF1} voltage ends up stabilizing when V_{gs} of the pass FET is equal to V_{th} . This means V_{REF1} node voltage is $V_{CC2} - V_{th}$. Note that any targets/controllers running off of the LDO now see the $V_{CC2} - V_{th}$ voltage which may cause damage to those targets/controllers if they are not rated to handle the increased voltage.

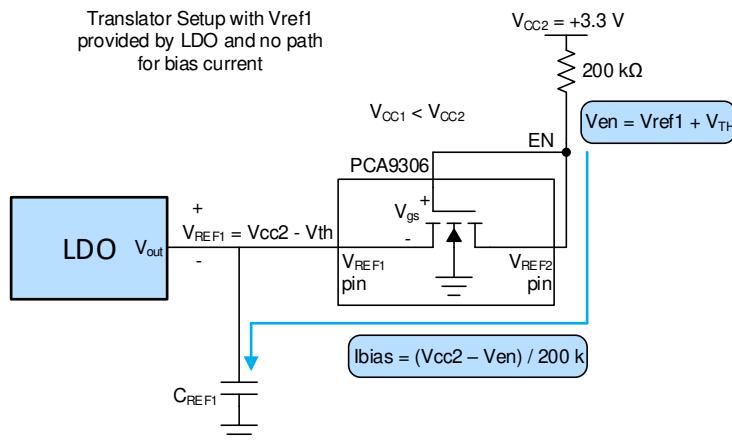


Figure 8-8. Example of no leakage current path when using LDO

To make sure the LDO does not lose regulation due to the bias current of PCA9306, a weak pull down resistor can be placed on V_{REF1} to ground to provide a path for the bias current to travel. The recommended pull down resistor is calculated by [Equation 4](#) where 0.75 gives about 25% margin for error incase bias current increases during operation.

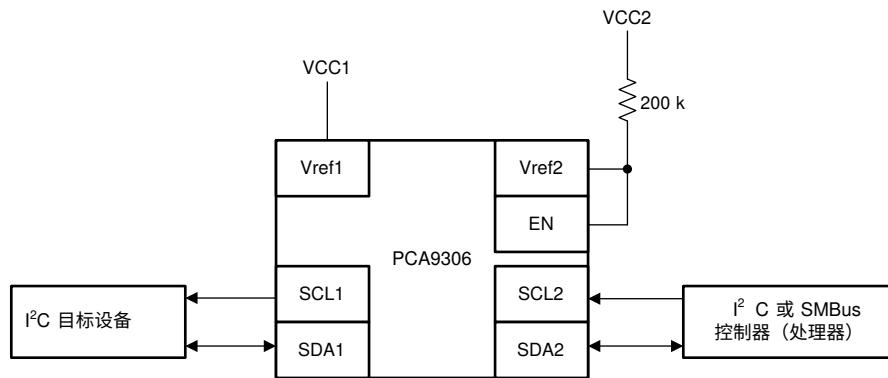


图 8-7。PCA9306 侧二的控制器 8.1.7 LDO 与 PCA9306 相关问题

PCA9306 相关问题

V_{REF1} 引脚可以由低压差线性稳压器 (LDO) 供电，但在某些情况下，由于从 V_{REF2} 到 V_{REF1} 的偏置电流，LDO 可能失去稳压功能。如果 LDO 无法吸收偏置电流，则该电流无其他路径流向地，而是对 V_{REF1} 节点上的电容（包括外部电容和寄生电容）充电。这导致 V_{REF1} 节点电压升高。如果未建立其他电流流动路径（例如通过 V_{REF1} 节点上其他器件的体二极管反向偏置或箝位二极管），则当通断场效应晶体管 (pass FET) 的 V_{gs} 等于阈值电压 V_{th} 时， V_{REF1} 电压最终稳定。这意味着 V_{REF1} 节点电压为 V_{CC2} 减 V_{th} 。请注意，任何由 LDO 供电的目标设备或控制器现在将看到 V_{CC2} 减 V_{th} 的电压，若这些目标设备或控制器未额定承受该升高电压，可能会导致损坏。

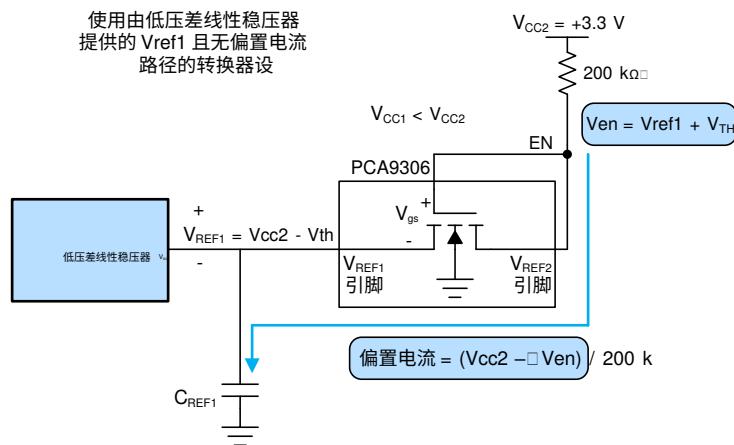


图 8-8。使用低压差线性稳压器时无泄漏电流路径的示例

为确保低压差线性稳压器不会因 PCA9306 的偏置电流而失去调节，可在 V_{REF1} 端接一个弱下拉电阻至地，为偏置电流提供路径。推荐的下拉电阻通过方程 4 计算，其中 0.75 提供约 25% 的误差裕度，以防偏置电流在运行期间增加。

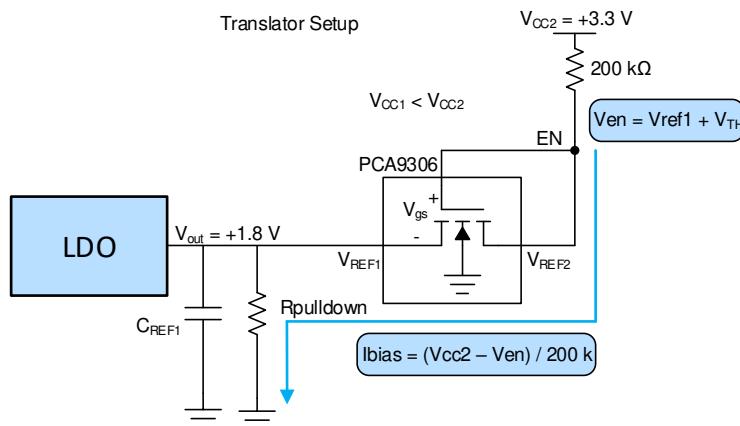


Figure 8-9. Example with Leakage current path when using an LDO

$$V_{en} = V_{REF1} + V_{th} \quad (1)$$

where

- V_{th} is approximately 0.6 V

$$I_{bias} = (V_{CC2} - V_{en})/200\text{k} \quad (2)$$

$$R_{pulldown} = V_{OUT}/I_{bias} \quad (3)$$

$$\text{Recommended } R_{pulldown} = R_{pulldown} \times 0.75 \quad (4)$$

8.1.8 Current Limiting Resistance on V_{REF2}

The resistor is used to limit the current between V_{REF2} and V_{REF1} (denoted as R_{CC}) and helps to establish the reference voltage on the enable pin. The 200k resistor can be changed to a lower value; however, the bias current proportionally increases as the resistor decreases.

$$I_{bias} = (V_{CC2} - V_{en})/R_{CC} : V_{en} = V_{REF1} + V_{th} \quad (5)$$

where

- V_{th} is approximately 0.6V

Keep in mind R_{CC} should not be sized low enough that I_{CC} exceeds the absolute maximum continuous channel current specified in section 6.1 which is described in [Equation 6](#).

$$R_{CC(\min)} \geq (V_{CC2} - V_{en})/0.128 : V_{en} = V_{REF1} + V_{th} \quad (6)$$

where

- V_{th} is approximately 0.6V

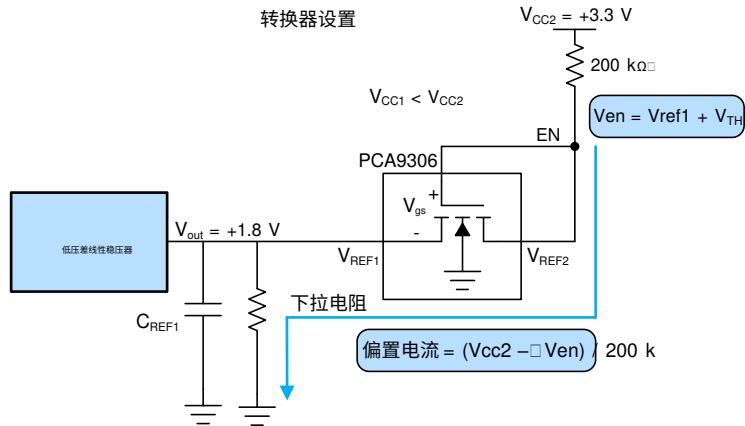


图 8-9。使用低压差线性稳压器时的泄漏电流路径示例

$$V_{en} = V_{REF1} + V_{th} \quad (1)$$

其中

- V_{th} 约为 0.6 V

$$I_{bias} = (V_{CC2} - V_{en}) / 200k \quad (2)$$

$$R_{pulldown} = V_{OUT} / I_{bias} \quad (3)$$

$$\text{推荐的} R_{pulldown} = R_{pulldown} \times 0.75 \quad (4)$$

8.1.8 V_{REF2} 上的限流电阻

该电阻用于限制 V_{REF2} 与 V_{REF1} 之间的电流（记为 R_{CC} ），并有助于在使能引脚上建立参考电压。200k 电阻可更改为更低数值；但随着电阻减小，偏置电流按比例增加。

$$I_{bias} = (V_{CC2} - V_{en}) / R_{CC}; V_{en} = V_{REF1} + V_{th} \quad (5)$$

其中

- V_{th} 约为 0.6 V

请注意， R_{CC} 不应设置得过低，以免 I_{CC} 超过第 6.1 节中规定的绝对最大连续通道电流，该电流在 [方程 6](#) 中描述。

$$R_{CC} (\text{最小}) \geq (V_{CC2} - V_{en}) / 0.128; V_{en} = V_{REF1} + V_{th} \quad (6)$$

其中

- V_{th} 约为 0.6 V

8.2 Functional Block Diagram

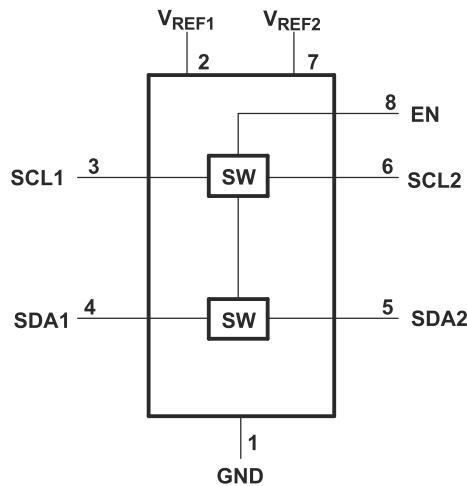


Figure 8-10. Block Diagram of PCA9306

8.3 Feature Description

8.3.1 Enable (EN) Pin

The PCA9306 device is a double-pole, single-throw switch in which the gate of the transistors is controlled by the voltage on the EN pin. In [Figure 9-1](#), the PCA9306 device is always enabled when power is applied to V_{REF2} . In [Figure 9-2](#), the device is enabled when a control signal from a processor is in a logic-high state.

8.3.2 Voltage Translation

The primary feature of the PCA9306 device is translating voltage from an I²C bus referenced to V_{REF1} up to an I²C bus referenced to V_{DPU} , to which V_{REF2} is connected through a 200-kΩ pullup resistor. Translation on a standard, open-drain I²C bus is achieved by simply connecting pullup resistors from SCL1 and SDA1 to V_{REF1} and connecting pullup resistors from SCL2 and SDA2 to V_{DPU} . Information on sizing the pullup resistors can be found in the [Sizing Pullup Resistors](#) section.

8.4 Device Functional Modes

INPUT EN ⁽¹⁾	TRANSLATOR FUNCTION
H	Logic Lows are propagated from one side to the other, Logic Highs blocked (independent pull up resistors passively drive the line high)
L	Disconnect

(1) The SCL switch conducts if EN is ≥ 0.6 V higher than SCL1 or SCL2. The same is true of SDA.

8.2 功能框图

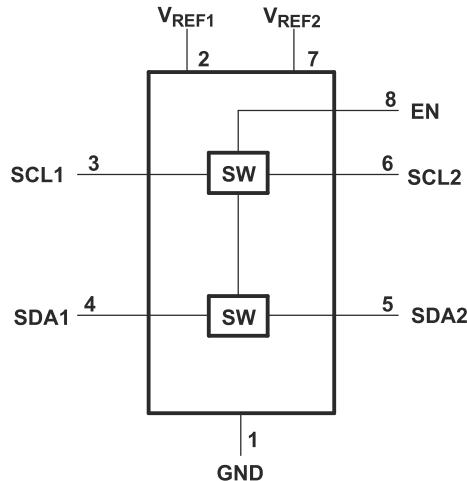


图 8-10. PCA9306 的框图

8.3 特性描述

8.3.1 使能 (EN) 引脚

PCA9306 器件为双刀单掷开关，其晶体管的栅极由 EN 引脚上的电压控制。在图 9-1 中，当 V_{REF2} 加电时，PCA9306 器件始终处于使能状态。在图 9-2 中，当处理器的控制信号处于逻辑高电平时，器件被使能。

8.3.2 电压转换

PCA9306 器件的主要特性是将参考于 V_{REF1} 的 I²C 总线电压转换为参考于 V_{DPU} 的 I²C 总线电压，其中 V_{REF2} 通过 $200\text{ k}\Omega$ 上拉电阻连接。在标准开漏 I²C 总线上实现电压转换，只需将上拉电阻分别从 SCL1 和 SDA1 连接至 V_{REF1} ，且将上拉电阻分别从 SCL2 和 SDA2 连接至 V_{DPU} 。有关上拉电阻选型的信息，请参见“上拉电阻选型”章节。

8.4 器件功能模式

输入 EN ⁽¹⁾	转换器功能
高	逻辑低电平从一侧传递到另一侧，逻辑高电平被阻断（独立上拉电阻被动地将线路拉高）
低	断开

(1) 当 EN 电压比 SCL1 或 SCL2 高出 $\geq 0.6\text{ V}$ 时，SCL 开关导通。SDA 亦同理。

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 General Applications of I²C

As with the standard I²C system, pullup resistors are required to provide the logic-high levels on the translator bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with standard-mode and fast-mode I²C devices in addition to SMBus devices. Standard-mode I²C devices only specify 3 mA in a generic I²C system where standard-mode devices and multiple controllers are possible. Under certain conditions, high termination currents can be used. When the SDA1 or SDA2 port is low, the clamp is in the ON state, and a low-resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is high, the voltage on the SDA1 port is limited to the voltage set by V_{REF1}. When the SDA1 port is high, the SDA2 port is pulled to the pullup supply voltage of the drain (V_{DPU}) by the pullup resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control. The SCL1-SCL2 channel also functions in the same way as the SDA1-SDA2 channel.

9.2 Typical Application

Figure 9-1 and Figure 9-2 show how these pullup resistors are connected in a typical application, as well as two options for connecting the EN pin.

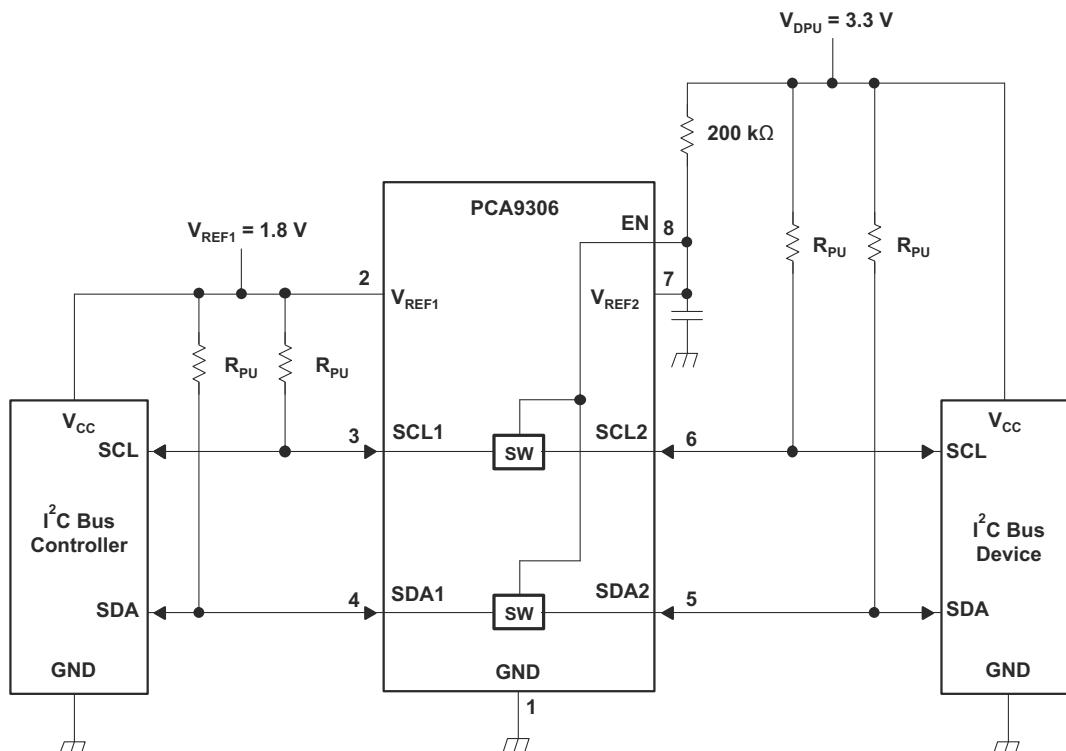


Figure 9-1. Typical Application Circuit (Switch Always Enabled)

9 应用与实现

注意

以下应用部分的信息不属于TI组件规格，TI不保证其准确性或完整性。TI的客户负责确定组件是否适合其用途，并验证和测试其设计实现以确认系统功能。

9.1 应用信息

9.1.1 I²C的一般应用

与标准I²C系统一样，翻译器总线上需要上拉电阻以提供逻辑高电平。这些上拉电阻的大小取决于系统，但中继器的每一侧都必须配备上拉电阻。该器件设计用于支持标准模式和快速模式的I²C器件以及SMBus器件。标准模式I²C器件仅在通用I²C系统中规定3 mA，其中可能存在标准模式器件和多个控制器。在某些条件下，可以使用较高的终端电流。当 SDA1 或 SDA2 端口为低电平时，钳位处于导通状态，SDA1 和 SDA2 端口之间存在低阻抗连接。假设 SDA2 端口电压较高，当 SDA2 端口为高电平时，SDA1 端口的电压被限制在由 V_{REF1} 设定的电压值。当 SD A1 端口为高电平时，SDA2 端口通过上拉电阻被拉至漏极的上拉电源电压 (V_{DPU})。该功能允许用户选择的高低电压之间实现无缝转换，无需方向控制。SCL1-SCL2 通道的功能与 SDA1-SDA2 通道相同。

9.2 典型应用

图 9-1 和 图 9-2 展示了这些上拉电阻在典型应用中的连接方式，以及 EN 引脚的两种连接选项。

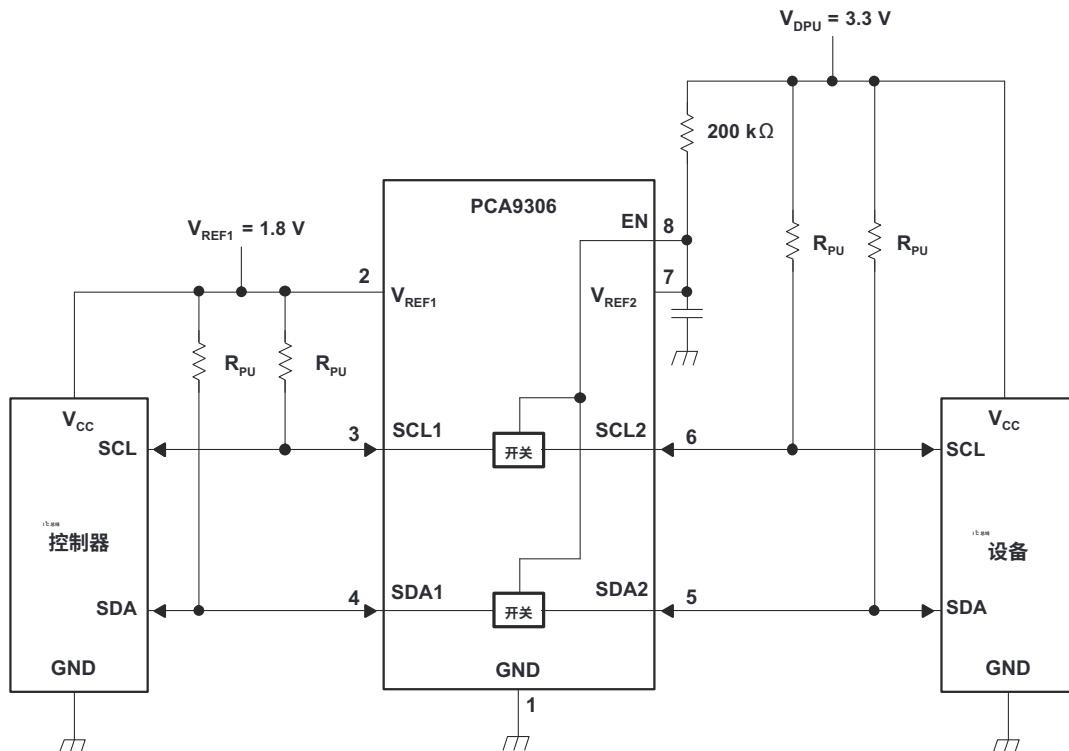


图 9-1. 典型应用电路 (开关始终使能)

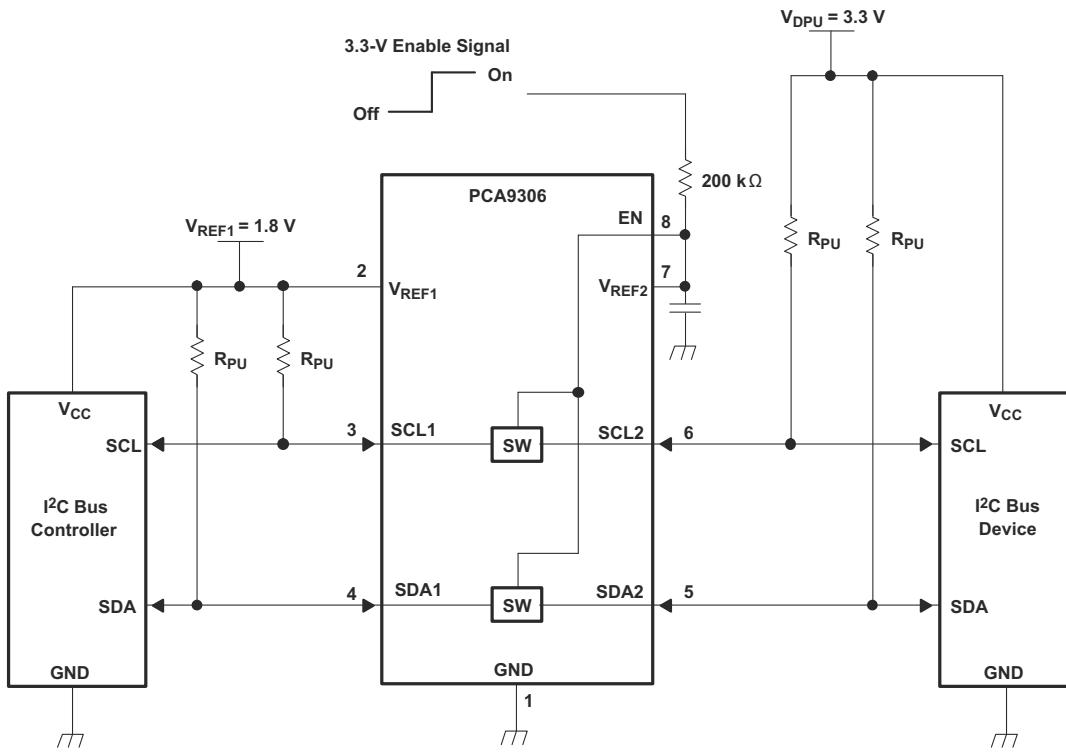


Figure 9-2. Typical Application Circuit (Switch Enable Control)

9.2.1 Design Requirements

		MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{REF2}	Reference voltage		V _{REF1} + 0.6	2.1	5	V
EN	Enable input voltage		V _{REF1} + 0.6	2.1	5	V
V _{REF1}	Reference voltage	1.2	1.5	4.4	V	
I _{PASS}	Pass switch current			6	mA	
I _{REF}	Reference-transistor current			5	µA	

(1) All typical values are at $T_A = 25^\circ\text{C}$.

9.2.2 Detailed Design Procedure

9.2.2.1 Bidirectional Voltage Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to V_{REF2} and both pins pulled to high-side V_{DPU} through a pullup resistor (typically 200 kΩ). This allows V_{REF2} to regulate the EN input. A 100-pF filter capacitor connected to V_{REF2} is recommended. The I²C bus controller output can be push-pull or open-drain (pullup resistors may be required) and the I²C bus device output can be open-drain (pullup resistors are required to pull the SCL2 and SDA2 outputs to V_{DPU}). However, if either output is push-pull, data must be unidirectional or the outputs must be 3-state capable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction. If both outputs are open-drain, no direction control is needed.

9.2.2.2 Sizing Pullup Resistors

To get an estimate for the range of values that can be used for the pullup resistor, please refer to the application note [SLVA689](#). [Figure 9-3](#) and [Figure 9-4](#) respectively show the maximum and minimum pullup resistance allowable by the I²C specification for standard-mode (100 kHz) and fast-mode (400 kHz) operation.

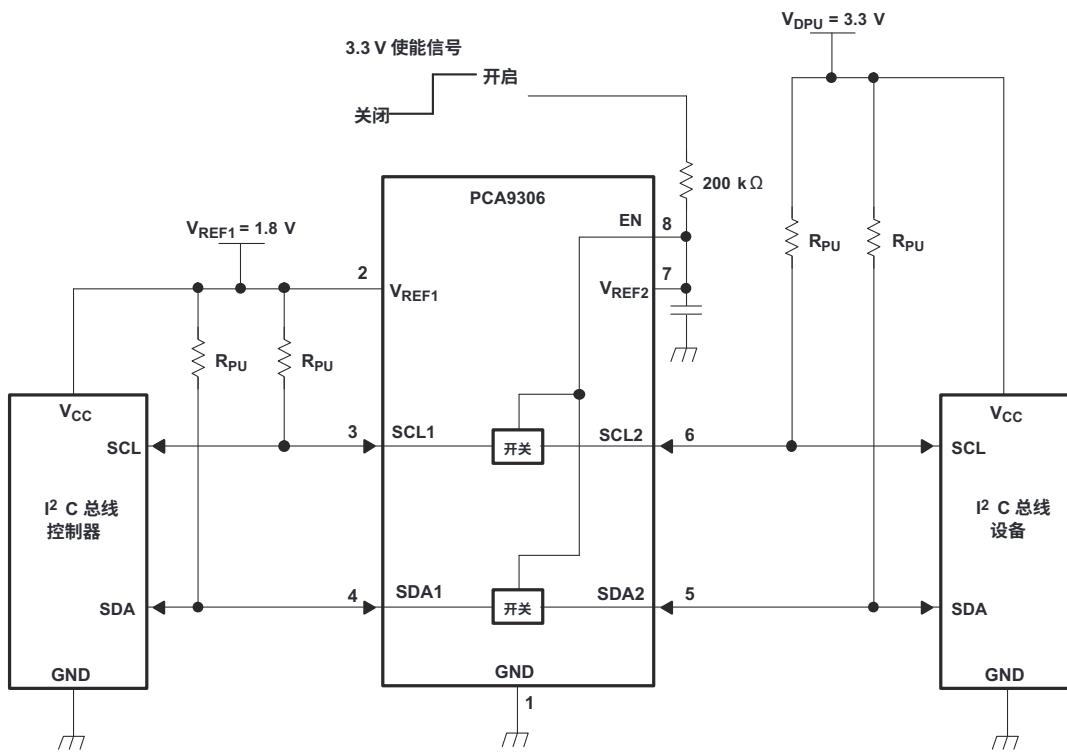


图 9-2. 典型应用电路 (开关使能控制)

9.2.1 设计要求

		最小值	典型值 ⁽¹⁾	最大值	单位	
V _{REF2}	参考电压		V _{REF1} + 0.6	2.1	5	V
EN	使能输入电压		V _{REF1} + 0.6	2.1	5	V
V _{REF1}	参考电压		1.2	1.5	4.4	V
I _{PASS}	通断开关电流			6	mA	
I _{REF}	参考晶体管电流			5	μA	

(1) 所有典型值均在 T_A = 25°C 下测量。

9.2.2 详细设计流程

9.2.2.1 双向电压转换

对于双向钳位配置（高电压至低电压或低电压至高电压），EN 输入必须连接至 V_{REF2}，且两个引脚均通过上拉电阻（典型值为 200 kΩ）拉至高端 V_{DPU}。这使 V_{REF2} 能够调节 EN 输入。建议在 V_{REF2} 端连接一个 100 pF 滤波电容。I²C 总线控制器输出可以是推挽式或开漏式（可能需要上拉电阻），而 I²C 总线设备输出为开漏式（需上拉电阻将 SCL2 和 SDA2 输出拉至 V_{DPU}）。然而，如果任一输出为推挽式，则数据必须是单向的，或者输出必须具备三态能力，并通过某种方向控制机制进行控制，以防止任一方向的高低电平冲突。如果两个输出均为开漏式，则无需方向控制。

9.2.2.2 上拉电阻的选取

欲估算可用于上拉电阻的阻值范围，请参阅应用说明 SLVA689。图 9-3 和 图 9-4 分别显示了符合 I²C 规范的标准模式（100 kHz）和快速模式（400 kHz）操作所允许的最大和最小上拉电阻。

9.2.2.3 PCA9306 Bandwidth

The maximum frequency of the PCA9306 device depends on the application. The device can operate at speeds of > 100 MHz given the correct conditions. The maximum frequency is dependent upon the loading of the application.

Figure 6-3 shows a bandwidth measurement of the PCA9306 device using a two-port network analyzer.

However, this is an analog type of measurement. For digital applications, the signal should not degrade up to the fifth harmonic of the digital signal. As a rule of thumb, the frequency bandwidth should be at least five times the maximum digital clock rate. This component of the signal is very important in determining the overall shape of the digital signal. In the case of the PCA9306 device, digital clock frequency of >100 MHz can be achieved.

The PCA9306 device does not provide any drive capability like the PCA9515 or PCA9517 series of devices. Therefore, higher-frequency applications require higher drive strength from the host side. No pullup resistor is needed on the host side (3.3 V) if the PCA9306 device is being driven by standard CMOS push-pull output driver. Ideally, it is best to minimize the trace length from the PCA9306 device on the sink side (1.8 V) to minimize signal degradation.

You can then use a simple formula to compute the maximum *practical* frequency component or the *knee* frequency (f_{knee}). All fast edges have an infinite spectrum of frequency components. However, there is an inflection (or *knee*) in the frequency spectrum of fast edges where frequency components higher than f_{knee} are insignificant in determining the shape of the signal.

To calculate f_{knee} :

$$f_{knee} = 0.5 / RT \text{ (10\%--90\%)} \quad (7)$$

$$f_{knee} = 0.4 / RT \text{ (20\%--80\%)} \quad (8)$$

For signals with rise-time characteristics based on 10- to 90-percent thresholds, f_{knee} is equal to 0.5 divided by the rise time of the signal. For signals with rise-time characteristics based on 20- to 80-percent thresholds, which is very common in many current device specifications, f_{knee} is equal to 0.4 divided by the rise time of the signal.

Some guidelines to follow that help maximize the performance of the device:

- Keep trace length to a minimum by placing the PCA9306 device close to the I²C output of the processor.
- The trace length should be less than half the time of flight to reduce ringing and line reflections or non-monotonic behavior in the switching region.
- To reduce overshoots, a pullup resistor can be added on the 1.8 V side; be aware that a slower fall time is to be expected.

9.2.2.3 PCA9306 带宽

PCA9306 器件的最大工作频率取决于具体应用。在适当条件下，该器件可支持超过 100 MHz 的工作速度。最大频率取决于应用的负载情况。

图 6-3 显示了使用双端口网络分析仪对 PCA9306 器件进行带宽测量的结果。

然而，这是一种模拟测量方法。对于数字应用，信号在数字信号的第五次谐波频率范围内不应发生衰减。经验法则是，频率带宽应至少为最大数字时钟频率的五倍。信号的这一分量对于确定数字信号的整体波形非常重要。对于 PCA9306 器件，可实现超过 100 MHz 的数字时钟频率。

PCA9306 器件不具备类似 PCA9515 或 PCA9517 系列器件的驱动能力。

因此，更高频率的应用需要主机端提供更强的驱动能力。如果 PCA9306 器件由标准 CMOS 推挽输出驱动，则主机端 (3.3 V) 无需上拉电阻。理想情况下，应尽量缩短来自接收端 (1.8 V) PCA9306 器件的走线长度，以减少信号衰减。

然后，您可以使用一个简单的公式来计算最大实际频率分量或拐点频率 (f_{knee})。所有快速上升沿都具有无限的频率分量谱。然而，快速上升沿的频率谱中存在一个拐点（或 *knee*），高于 f_{knee} 的频率分量在决定信号形状时不再显著。

计算 f_{knee} 的方法如下：

$$f_{knee} = 0.5 / RT \quad (10\% \text{--} 90\%) \quad (7)$$

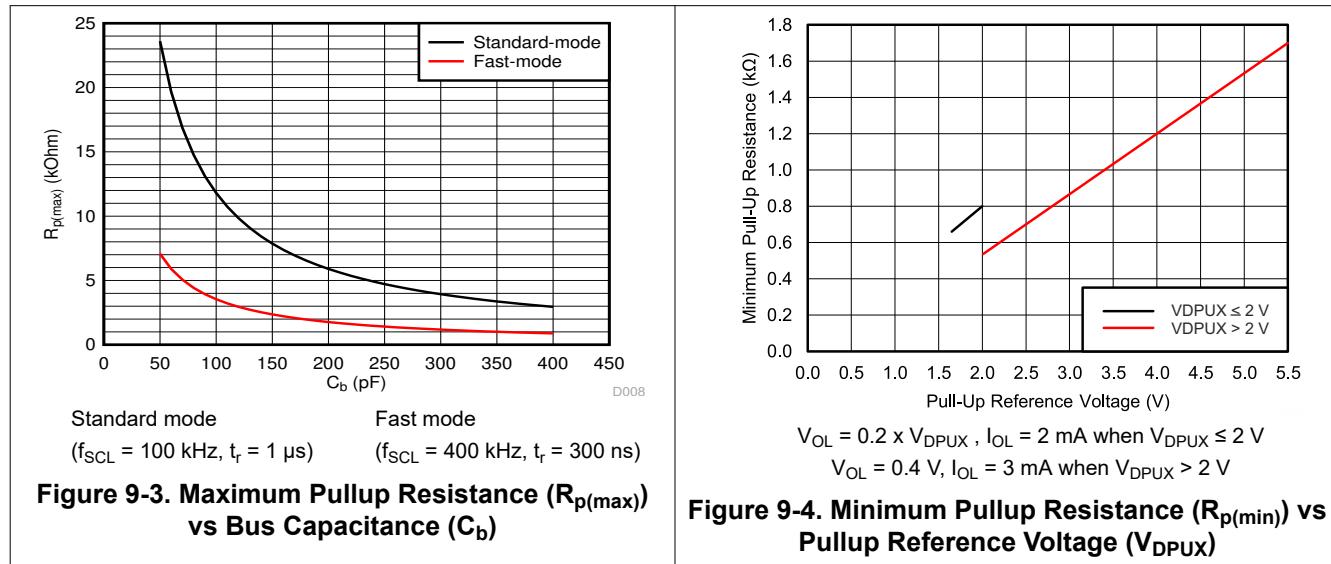
$$f_{knee} = 0.4 / RT \quad (20\% \text{--} 80\%) \quad (8)$$

对于基于 10% 至 90% 阈值的上升时间特性的信号， f_{knee} 等于 0.5 除以上升时间。对于基于 20% 至 80% 阈值的上升时间特性信号（这在许多现有器件规格中非常常见）， f_{knee} 等于 0.4 除以上升时间。

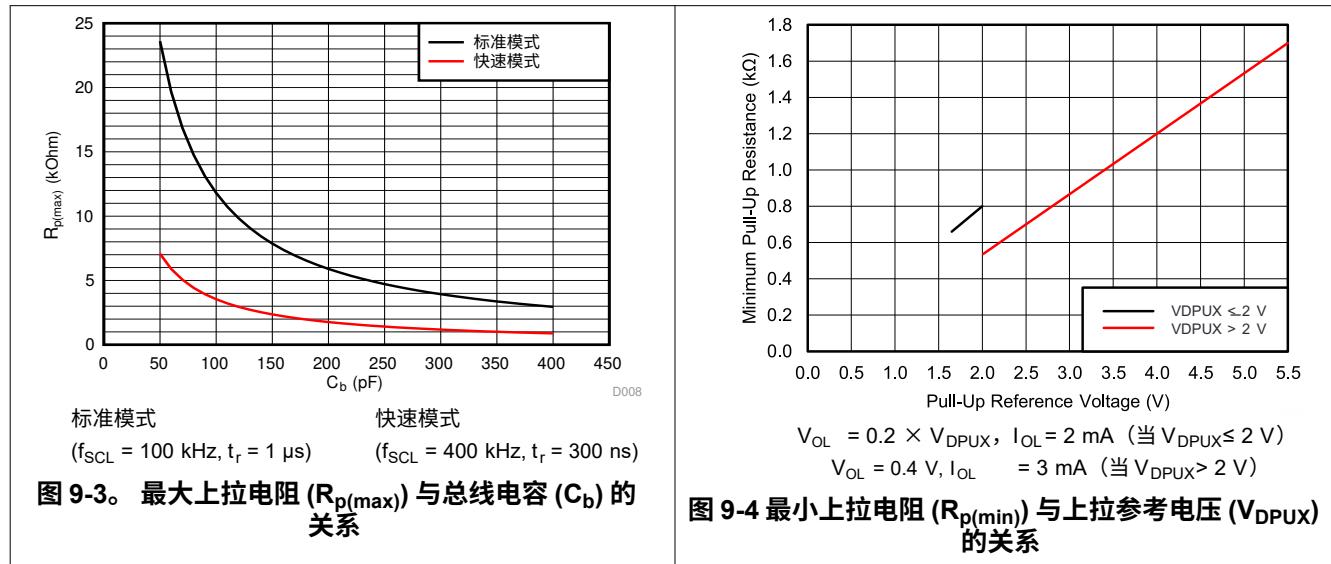
以下是一些有助于最大化器件性能的指导原则：

- 通过将 PCA9306 器件放置在处理器的 I²C 输出端附近，尽量缩短走线长度。
- 走线长度应小于信号传播时间的一半，以减少振铃、线路反射或开关区域的非单调行为。
- 为减少过冲，可在 1.8 V 侧添加上拉电阻；但需注意，下降时间会相应变慢。

9.2.3 Application Curve



9.2.3 应用曲线



10 Power Supply Recommendations

For supplying power to the PCA9306 device, the V_{REF1} pin can be connected directly to a power supply. The V_{REF2} pin must be connected to the V_{DPU} power supply through a 200-k Ω resistor. Failure to have a high-impedance resistor between V_{REF2} and V_{DPU} results in excessive current draw and unreliable device operation. It is also worth noting, that in order to support voltage translation, the PCA9306 must have the EN and VREF2 pins shorted and then pulled up to V_{DPU} through a high-impedance resistor.

10 电源建议

为 PCA9306 器件供电时, V_{REF1} 引脚可直接连接至电源。

V_{REF2} 引脚必须通过 $200\text{ k}\Omega$ 电阻连接至 V_{DPU} 电源。若 V_{REF2} 与 V_{DPU} 之间未设置高阻抗电阻, 将导致过大电流消耗及器件工作不可靠。同样值得注意的是, 为了支持电压转换, PCA9306 器件必须将 EN 和 V_{REF2} 引脚短接, 然后通过高阻抗电阻上拉至 V_{DPU} 。

11 Layout

11.1 Layout Guidelines

For printed-circuit board (PCB) layout of the PCA9306 device, common PCB layout practices should be followed, but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I²C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other on leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. The 100-pF filter capacitor should be placed as close to V_{REF2} as possible. A larger decoupling capacitor can also be used, but a longer time constant of two capacitors and the 200-kΩ resistor results in longer turnon and turnoff times for the PCA9306 device. These best practices are shown in [Figure 11-1](#).

For the layout example provided in [Figure 11-1](#), it would be possible to fabricate a PCB with only two layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a four-layer board is preferable for boards with higher-density signal routing. On a four-layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface-mount component pad, which must attach to V_{CC} or GND, and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace must be routed to the opposite side of the board, but this technique is not demonstrated in [Figure 11-1](#).

11.2 Layout Example

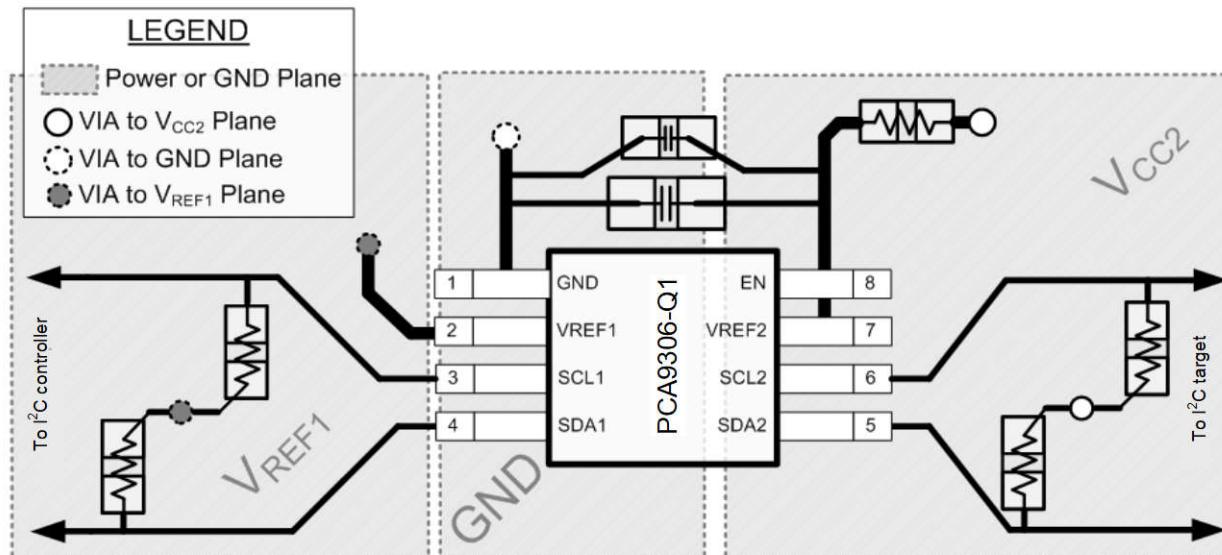


Figure 11-1. PCA9306 Layout Example

11 布局

11.1 布局指南

对于 PCA9306 器件的印刷电路板 (PCB) 布局，应遵循常见的 PCB 布局规范，但与高速数据传输相关的匹配阻抗和差分对等额外考虑，对于 I²C 信号速率而言并不重要。

在所有 PCB 布局中，避免信号线出现直角、在信号线离开集成电路 (IC) 附近时分散开来，以及使用较宽的线宽以承载通常通过电源和地线的较大电流，均为最佳实践。100 pF 滤波电容应尽可能靠近 V_{REF2} 引脚放置。也可以使用更大的去耦电容，但两个电容与 200 kΩ 电阻形成的较长时间常数会导致 PCA9306 器件的开启和关闭时间延长。

这些最佳实践如图11-1所示。

对于图11-1中提供的布局示例，通过使用顶层进行信号布线，底层作为电源 (V_{CC}) 和接地 (GND) 的分割平面，可以制造出仅两层的PCB。

然而，对于信号布线密度较高的电路板，建议采用四层板。在四层PCB中，通常在顶层和底层布置信号，一层内部层作为接地平面，另一层内部层作为电源平面。在使用电源和平面或分割平面作为接地的板布局中，过孔直接放置在必须连接到V_{CC}或GND的贴片元件焊盘旁，且该过孔在电气上连接到内部层或板的另一侧。当信号线必须布线到板的另一侧时，也会使用过孔，但该技术未在图中演示。

11-1.

11.2 布局示例

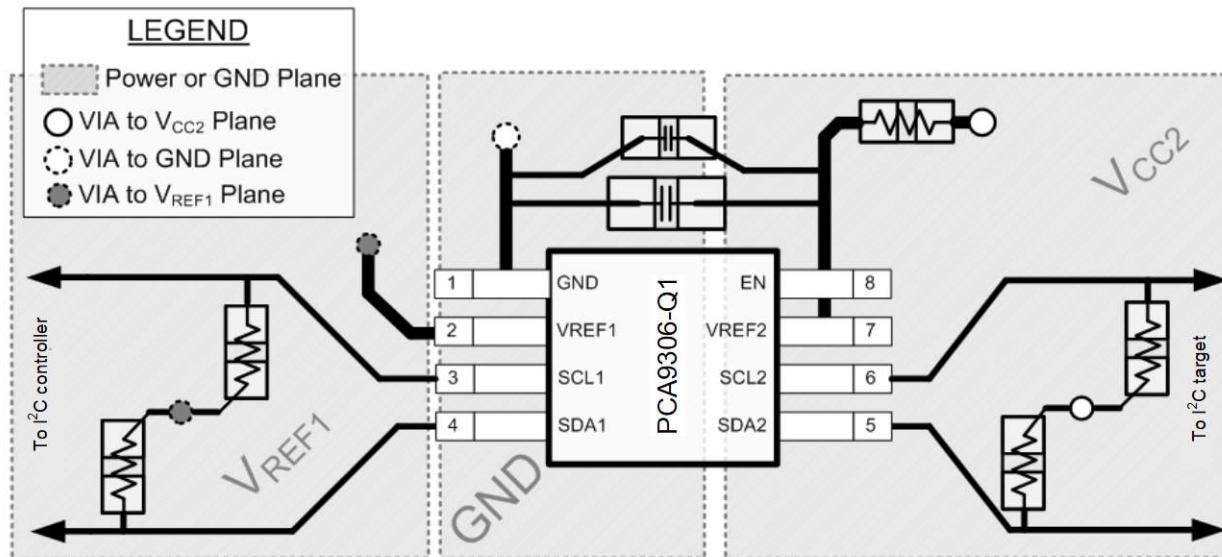


图 11-1. PCA9306 布局示例

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.3 Trademarks

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

12 器件及文档支持

12.1 接收文档更新通知

要接收文档更新通知，请访问 ti.com 上的器件产品文件夹。在右上角，点击提醒我以注册并每周接收任何产品信息变更的摘要。有关变更详情，请查阅任何修订文档中包含的修订历史。

12.2 支持资源

[TI E2E™支持论坛](#)是工程师获取快速、经过验证的答案和设计帮助的首选来源——直接来自专家。搜索现有答案或提出您自己的问题，以获得所需的快速设计帮助。

链接内容由各自贡献者“按原样”提供。这些内容不构成 TI 规格，也不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

12.3 商标

TI E2E™ 是 Texas Instruments 的商标。

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12.4 静电放电注意事项

该集成电路可能因静电放电（ESD）而损坏。德州仪器建议所有集成电路在操作时采取适当的防护措施。未遵守正确的操作和安装程序可能导致损坏。



静电放电损坏可能表现为性能轻微下降，甚至导致器件完全失效。精密集成电路更易受损，因为极小的参数变化可能导致器件无法满足其公布的规格。

12.5 术语表

[TI 术语表](#)本术语表列出并解释术语、缩略语及定义。

机械、封装及可订购信息

以下页面包含机械、封装及可订购信息。此信息为指定器件的最新数据。本数据如有更改，恕不另行通知且不更新本文件。有关基于浏览器版本的数据表，请参见左侧导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCA9306DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7BD (G, S, Y)
PCA9306DCTR.A	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7BD (G, S, Y)
PCA9306DCTT	Active	Production	SSOP (DCT) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7BD (G, S, Y)
PCA9306DCTT.A	Active	Production	SSOP (DCT) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7BD (G, S, Y)
PCA9306DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU SN NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(29O4, 7BDP, 7BDS, 7BDY)
PCA9306DCUR.A	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(29O4, 7BDP, 7BDS, 7BDY)
PCA9306DCUT	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU SN NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(29O4, 7BDP, 7BDS, 7BDY)
PCA9306DCUT.A	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(29O4, 7BDP, 7BDS, 7BDY)
PCA9306DQER	Active	Production	X2SON (DQE) 8	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(3M, 7F)
PCA9306DQER.A	Active	Production	X2SON (DQE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(3M, 7F)
PCA9306DQER.B	Active	Production	X2SON (DQE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(3M, 7F)
PCA9306YZTR	Active	Production	DSBGA (YZT) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	7F
PCA9306YZTR.B	Active	Production	DSBGA (YZT) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	7F

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

封装信息

可订购零件编号	状态 (1)	材料类型 (2)	封装 引脚数	包装数量 承载器	RoHS (3)	引线表面处理/ 球体材料 (4)	湿敏等级/ 峰值回流温度 (5)	工作温度 (°C)	器件标记 (6)
PCA9306DCTR	激活	生产	SSOP (DCT) 8	3000 大型托盘与回流	是	无铅无卤素无卤聚合物	等级-1-260°C-无限制	-40 至 85	7BD (G, S, Y)
PCA9306DCTR.A	激活	生产	SSOP (DCT) 8	3000 大型托盘与回流	是	无铅无卤素无卤聚合物	等级-1-260°C-无限制	-40 至 85	7BD (G, S, Y)
PCA9306DCTT	激活	生产	SSOP (DCT) 8	250 小型托盘与回流	是	无铅无卤素无卤聚合物	等级-1-260°C-无限制	-40 至 85	7BD (G, S, Y)
PCA9306DCTT.A	激活	生产	SSOP (DCT) 8	250 小型托盘与回流	是	无铅无卤素无卤聚合物	等级-1-260°C-无限制	-40 至 85	7BD (G, S, Y)
PCA9306DCUR	激活	生产	VSSOP (DCU) 8	3000 大型托盘与回流	是	无铅无卤素无卤聚合物 SN 无铅无卤素无卤聚合物增强型	等级-1-260°C-无限制	-40 至 85	(29O4, 7BDP, 7BDS, 7BDY)
PCA9306DCUR.A	激活	生产	VSSOP (DCU) 8	3000 大型托盘与回流	是	SN	等级-1-260°C-无限制	-40 至 85	(29O4, 7BDP, 7BDS, 7BDY)
PCA9306DCUT	激活	生产	VSSOP (DCU) 8	250 小型托盘与回流	是	无铅无卤素无卤聚合物 SN 无铅无卤素无卤聚合物增强型	等级-1-260°C-无限制	-40 至 85	(29O4, 7BDP, 7BDS, 7BDY)
PCA9306DCUT.A	激活	生产	VSSOP (DCU) 8	250 小型托盘与回流	是	SN	等级-1-260°C-无限制	-40 至 85	(29O4, 7BDP, 7BDS, 7BDY)
PCA9306DQER	激活	生产	X2SON (DQE) 8	5000 大型托盘与回流	是	无铅无卤素无卤聚合物 无铅无卤素无卤聚合物增强型	等级-1-260°C-无限制	-40 至 85	(3M, 7F)
PCA9306DQER.A	激活	生产	X2SON (DQE) 8	5000 大型托盘与回流	是	无铅无卤素无卤聚合物增强型	等级-1-260°C-无限制	-40 至 85	(3M, 7F)
PCA9306DQER.B	激活	生产	X2SON (DQE) 8	5000 大型托盘与回流	是	无铅无卤素无卤聚合物增强型	等级-1-260°C-无限制	-40 至 85	(3M, 7F)
PCA9306YZTR	激活	生产	DSBGA (YZT) 8	3000 大型托盘与回流	是	SNAGCU	等级-1-260°C-无限制	-40 至 85	7F
PCA9306YZTR.B	激活	生产	DSBGA (YZT) 8	3000 大型托盘与回流	是	SNAGCU	等级-1-260°C-无限制	-40 至 85	7F

⁽¹⁾ 状态：有关状态的更多详细信息，请参阅我们的产品生命周期。

⁽²⁾ **材料类型：**指定时，预生产零件为原型/实验器件，尚未获得批准或发布用于全面生产。测试和最终工艺，包括但不限于质量保证、可靠性性能测试和/或工艺认证，可能尚未完成，该项目可能会有进一步更改或可能停产。如果可供订购，购买时将需额外签署豁免协议，且仅用于早期内部评估目的。这些产品不附带任何形式的保证。

⁽³⁾ **RoHS 值：**是、否、RoHS 免除。有关更多信息及值定义，请参阅 TI RoHS 声明。

⁽⁴⁾ **引线表面处理/球体材料：**零件可能具有多种材料表面处理选项。引线表面处理选项以竖线分隔。引线表面处理/球体材料值若超过最大列宽，可能换行显示为两行。

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF PCA9306 :

- Automotive : [PCA9306-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

⁽⁵⁾ **湿敏等级/峰值回流温度：**湿敏等级评级及峰值焊接（回流）温度。若器件具有多个湿敏等级，则仅显示符合JEDEC标准的最低等级。
实际用于将器件安装至印刷电路板的回流温度，请参阅运输标签。

⁽⁶⁾ **器件标记：**可能存在额外标记，涉及标志、批次追踪代码信息或器件的环境类别。

多个器件标记将置于括号内。每个器件上仅显示一个括号内且用“~”分隔的器件标记。若某行缩进，则表示该行为上一行的延续，两行合并构成该器件的完整标记。

重要信息及免责声明：本页所提供的信息代表TI截至提供之日的知识和信念。TI基于第三方提供的信息建立其知识和信念，但不对该等信息的准确性作出任何陈述或保证。正在努力更好地整合来自第三方的信息。TI已采取并将继续采取合理措施以提供具有代表性和准确性的信息，但可能未对进料材料和化学品进行破坏性测试或化学分析。TI及其供应商将某些信息视为专有信息，因此CAS号及其他有限信息可能无法公开。

在任何情况下，TI因该等信息产生的责任均不超过TI每年向客户销售的相关TI器件的总购买价格。

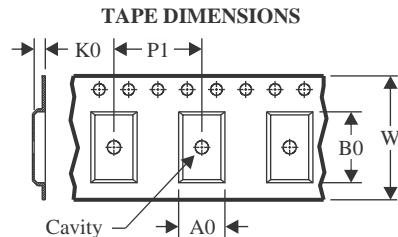
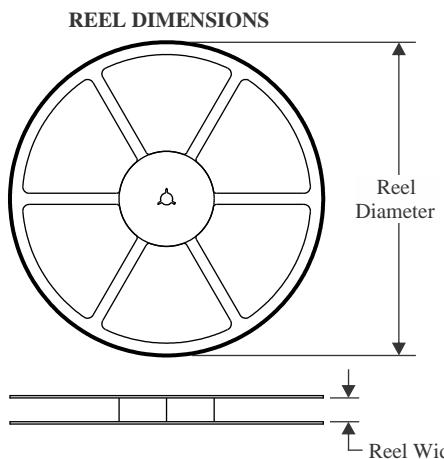
PCA9306的其他合格版本：

- 汽车级：PCA9306-Q1

注：合格版本定义：

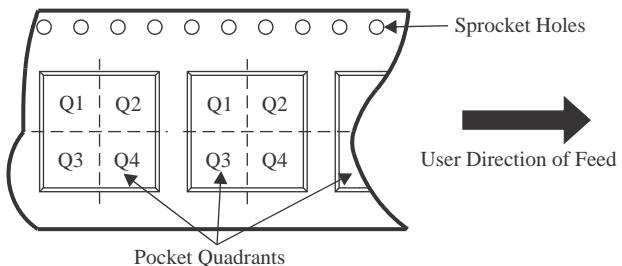
- 汽车级 - Q100器件，针对零缺陷的高可靠性汽车应用进行认证

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

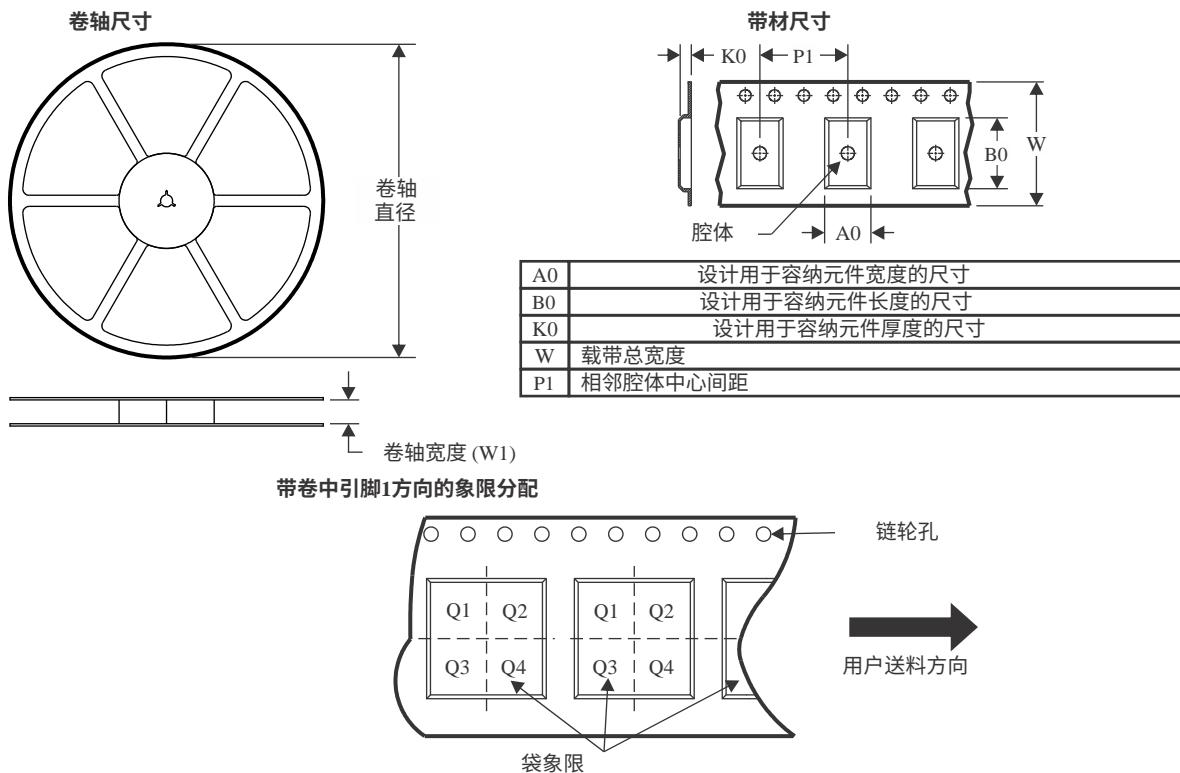
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

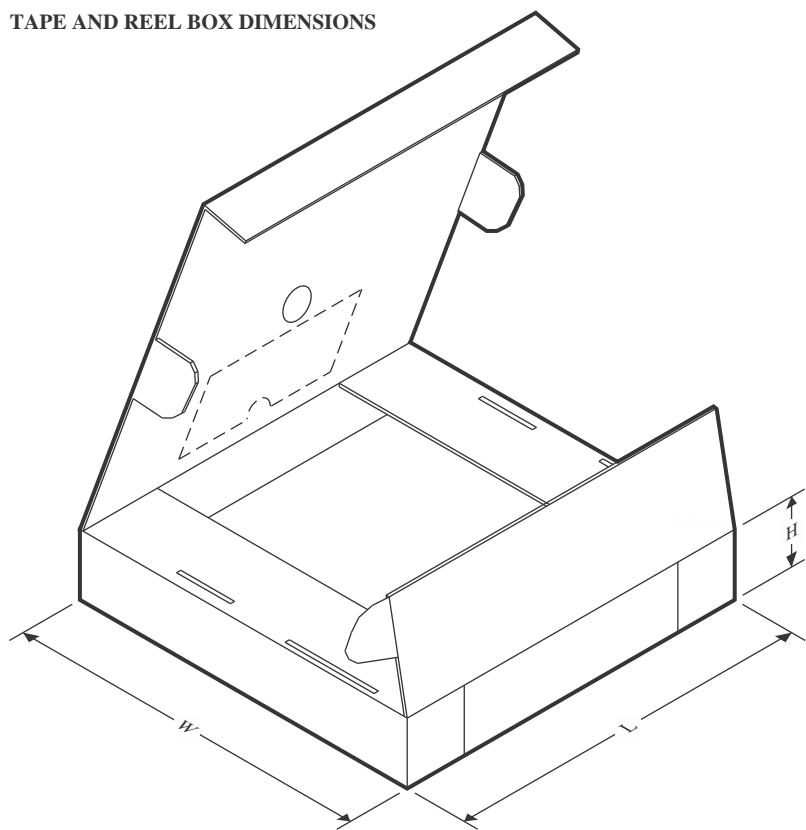
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9306DCTR	SSOP	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
PCA9306DCTT	SSOP	DCT	8	250	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
PCA9306DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
PCA9306DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
PCA9306DQER	X2SON	DQE	8	5000	180.0	9.5	1.15	1.6	0.5	4.0	8.0	Q1
PCA9306YZTR	DSBGA	YZT	8	3000	180.0	8.4	1.02	2.02	0.75	4.0	8.0	Q1

卷带信息



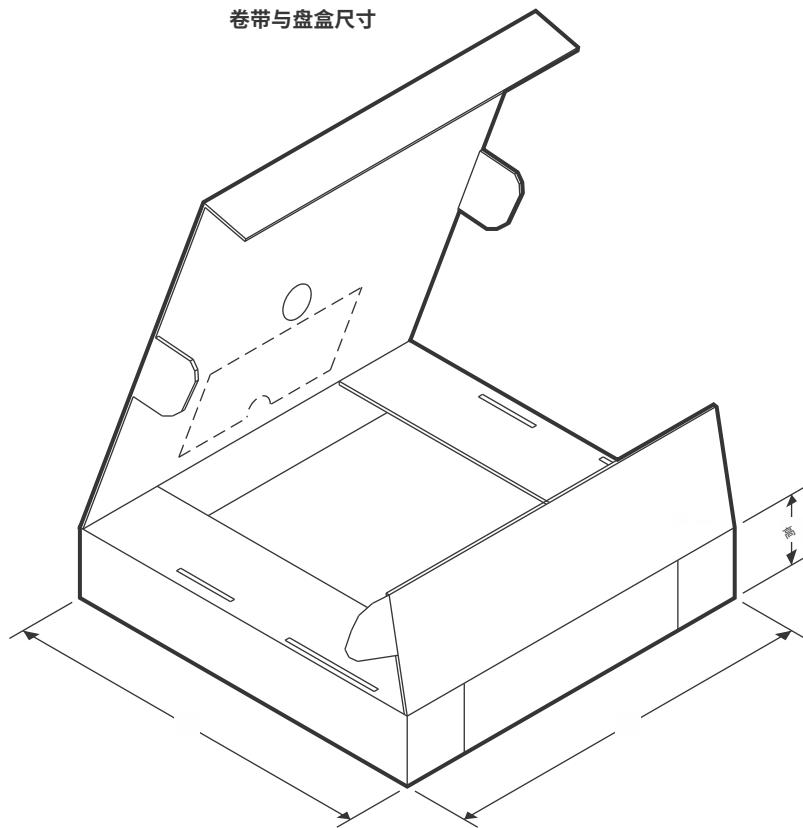
*所有尺寸均为标称值

器件	封装类型	封装图纸	引脚数	每卷数量	卷轴直径 (mm)	卷轴宽度 W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	引脚1 象限
PCA9306DCTR	SSOP	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
PCA9306DCTT	SSOP	DCT	8	250	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
PCA9306DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
PCA9306DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
PCA9306DQER	X2SON	DQE	8	5000	180.0	9.5	1.15	1.6	0.5	4.0	8.0	Q1
PCA9306YZTR	DSBGA	YZT	8	3000	180.0	8.4	1.02	2.02	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9306DCTR	SSOP	DCT	8	3000	183.0	183.0	20.0
PCA9306DCTT	SSOP	DCT	8	250	183.0	183.0	20.0
PCA9306DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
PCA9306DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
PCA9306DQER	X2SON	DQE	8	5000	184.0	184.0	19.0
PCA9306YZTR	DSBGA	YZT	8	3000	182.0	182.0	20.0

卷带与盘盒尺寸


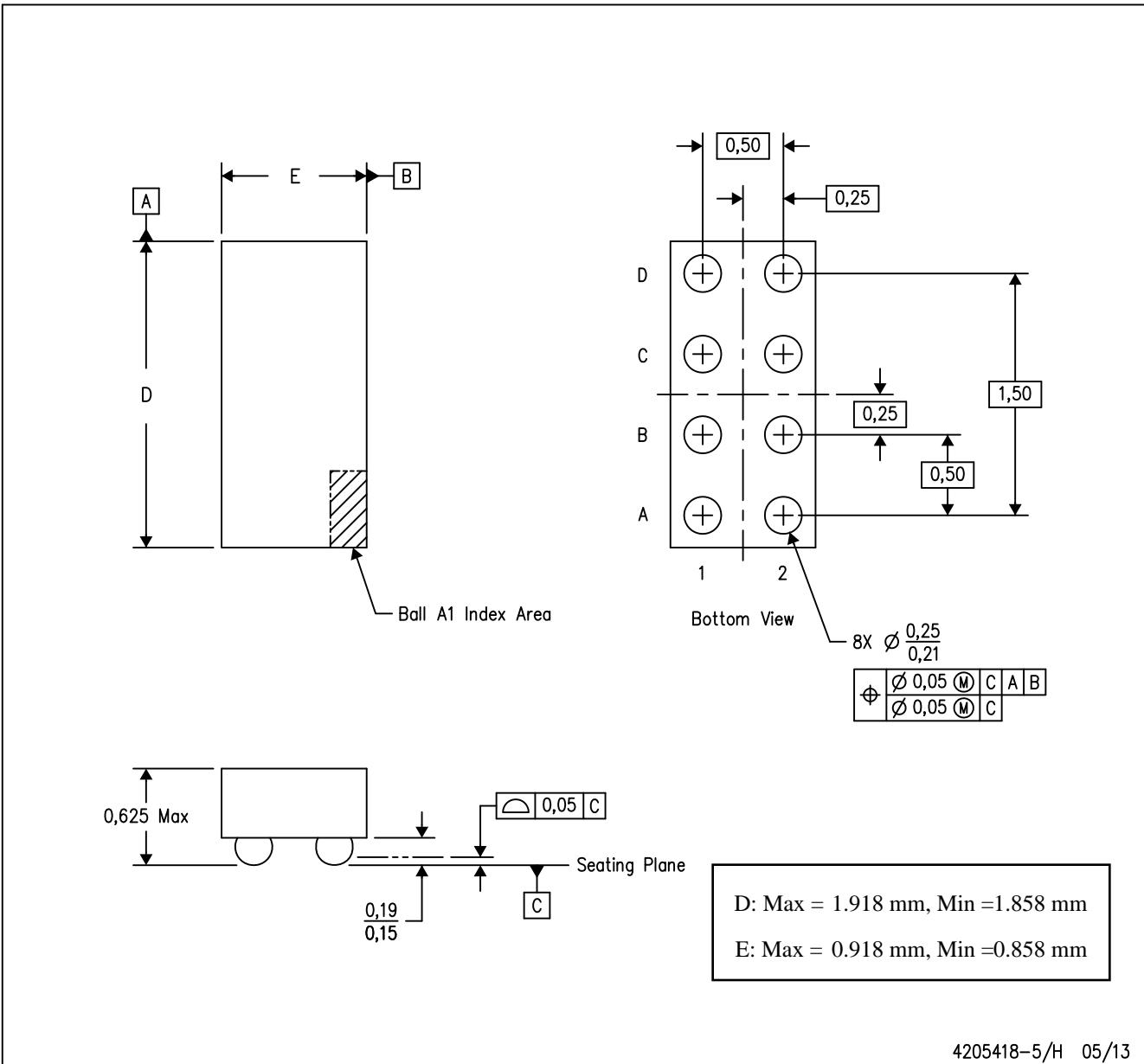
*所有尺寸均为标称值

器件	封装类型	封装图纸	引脚数	每卷数量	长度 (mm)	宽度 (mm)	高度 (mm)
PCA9306DCTR	SSOP	DCT	8	3000	183.0	183.0	20.0
PCA9306DCTT	SSOP	DCT	8	250	183.0	183.0	20.0
PCA9306DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
PCA9306DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
PCA9306DQER	X2SON	DQE	8	5000	184.0	184.0	19.0
PCA9306YZTR	DSBGA	YZT	8	3000	182.0	182.0	20.0

MECHANICAL DATA

YZT (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



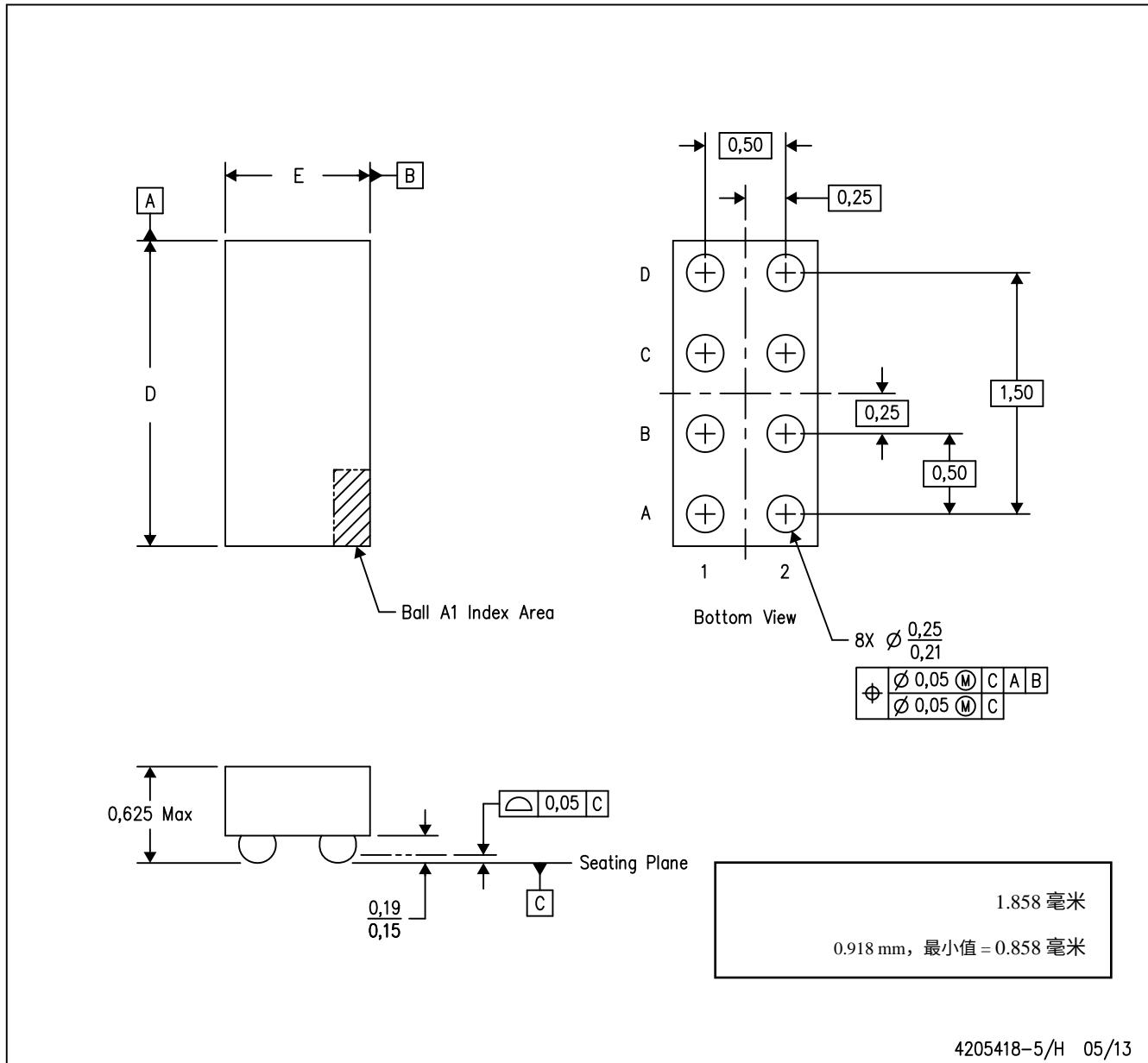
- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

MECHANICAL DATA

YZT (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

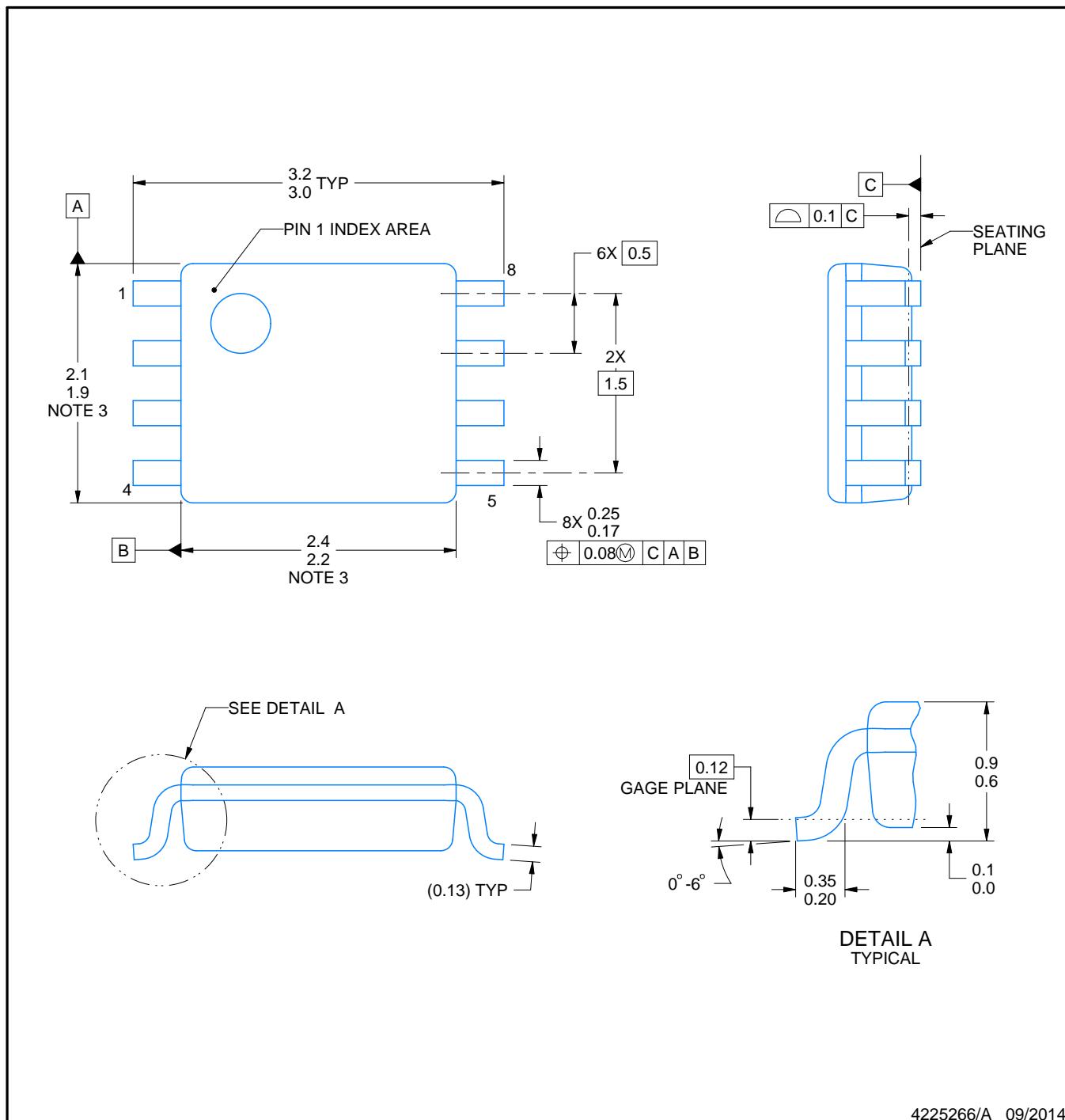
PACKAGE OUTLINE

DCU0008A



VSSOP - 0.9 mm max height

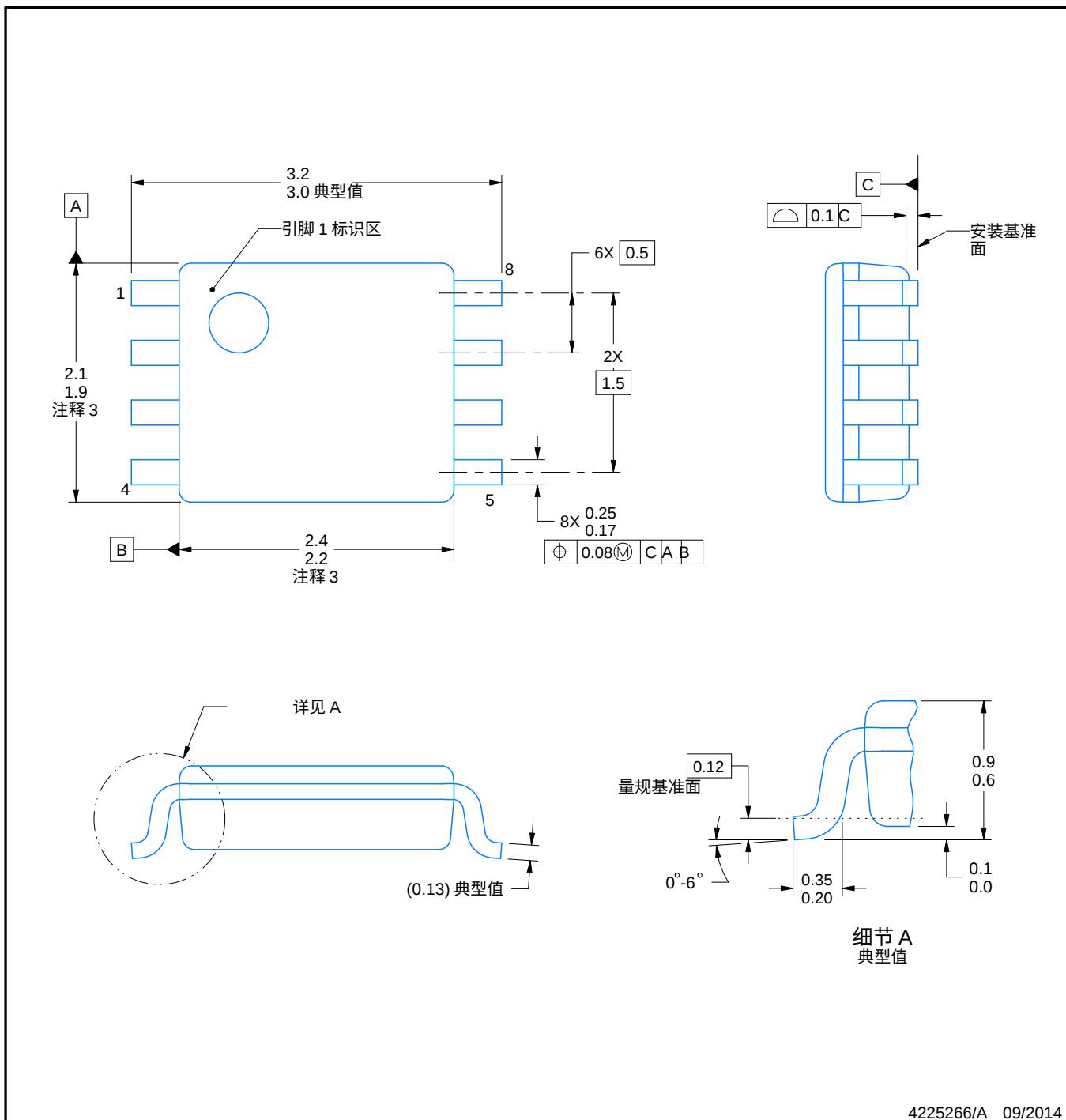
SMALL OUTLINE PACKAGE



4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



注释：

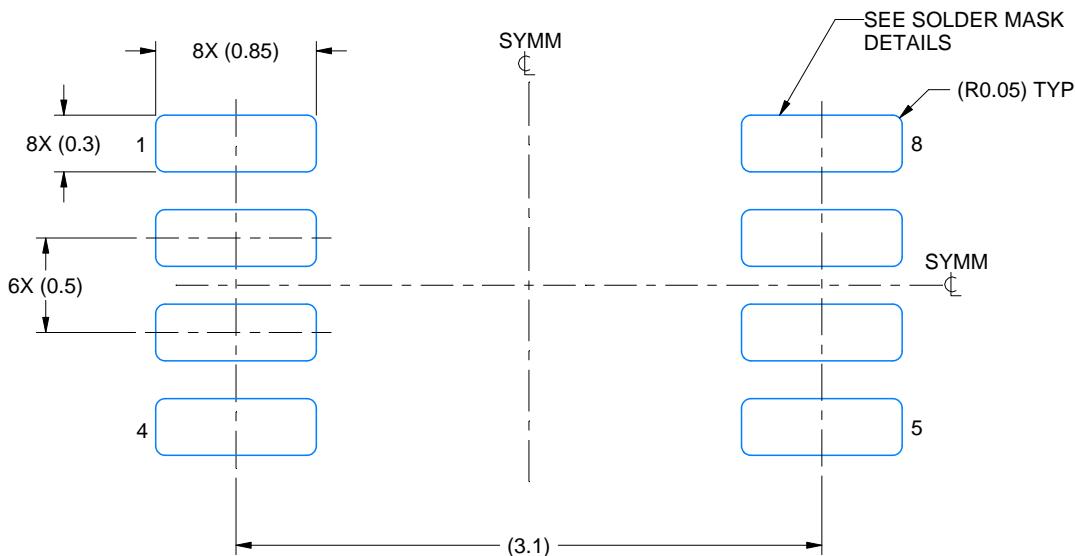
- 所有线性尺寸均以毫米为单位。括号内尺寸仅供参考。尺寸标注及公差符合 ASME Y14.5M 标准。
- 本图纸如有更改，恕不另行通知。
- 此尺寸不包括模具飞边、凸起或浇口毛刺。模具飞边、凸起或浇口毛刺每侧不得超过 0.15 毫米。
- 参考 JEDEC 注册 MO-187 变体 CA。

EXAMPLE BOARD LAYOUT

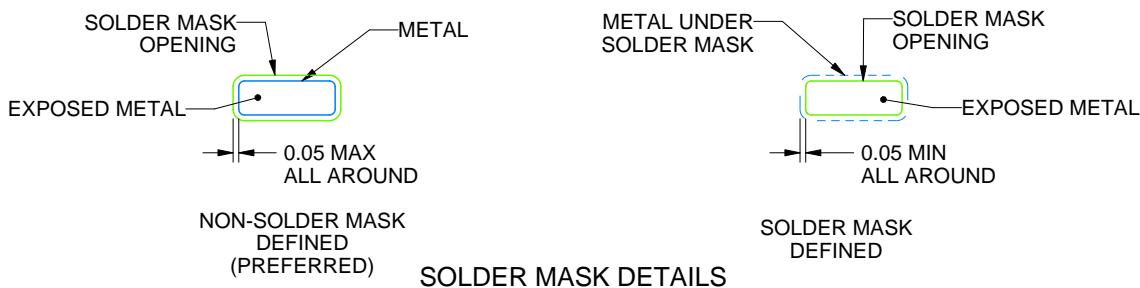
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



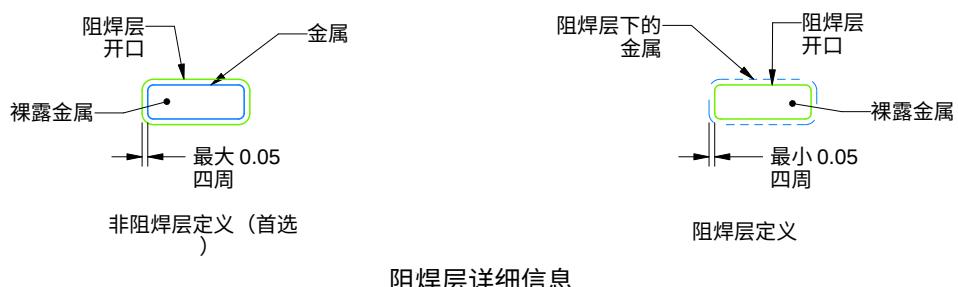
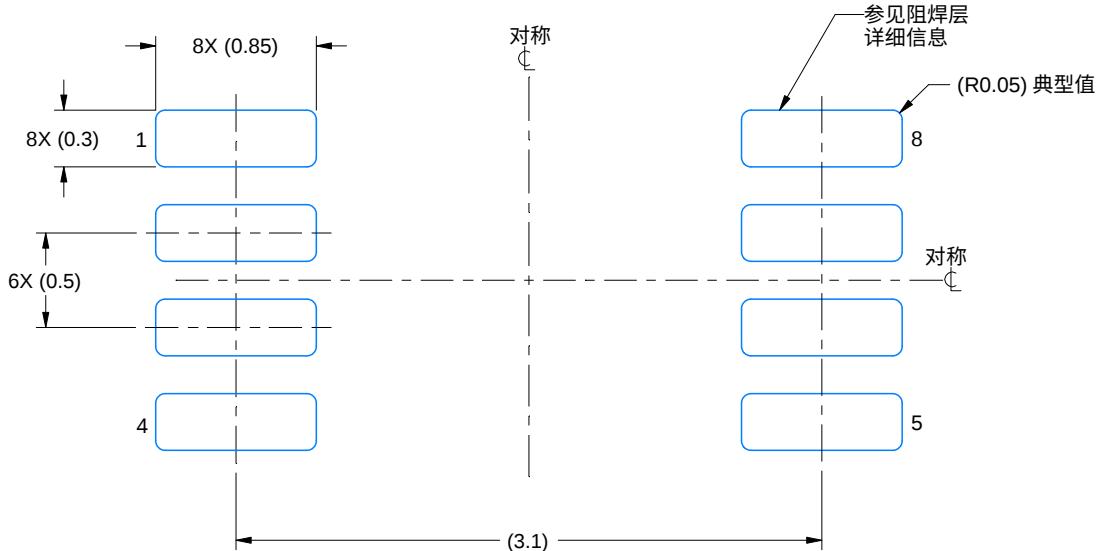
SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



4225266/A 09/2014

注释：（续）

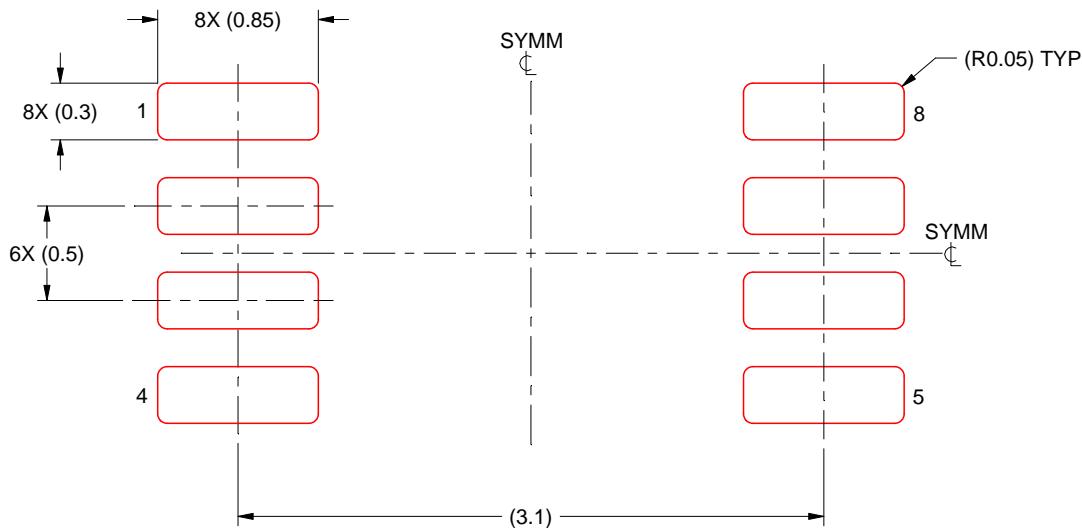
5. IPC-7351 出版物可能包含替代设计。
6. 阻焊层在信号焊盘之间及周围的公差可能因电路板制造地点而异。

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

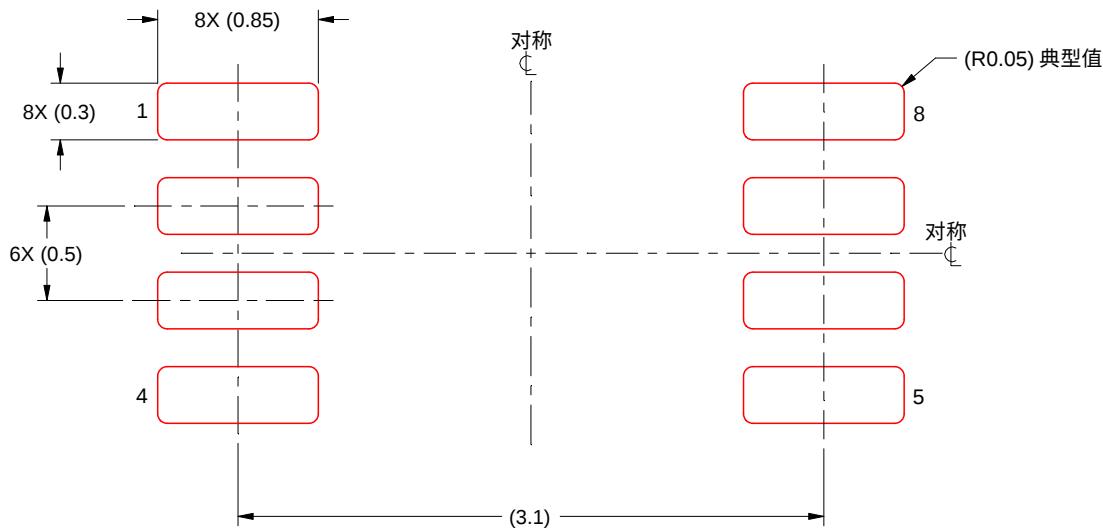


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4225266/A 09/2014

注释: (续)

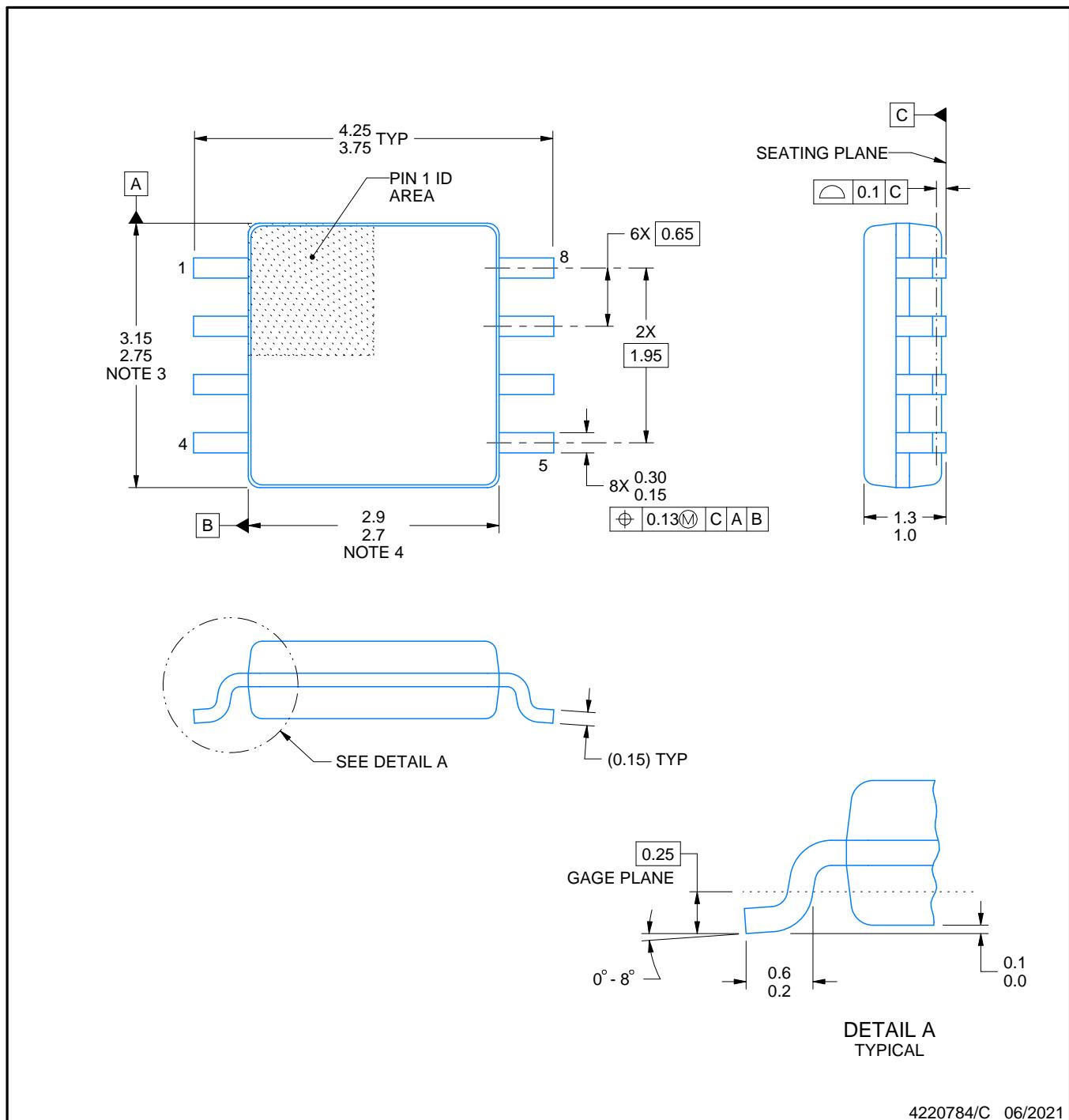
7. 采用梯形壁和圆角的激光切割开孔可实现更佳的焊膏释放效果。IPC-7525 可能提供替代的设计建议。
8. 电路板组装现场可能对模板设计有不同的建议。



PACKAGE OUTLINE

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

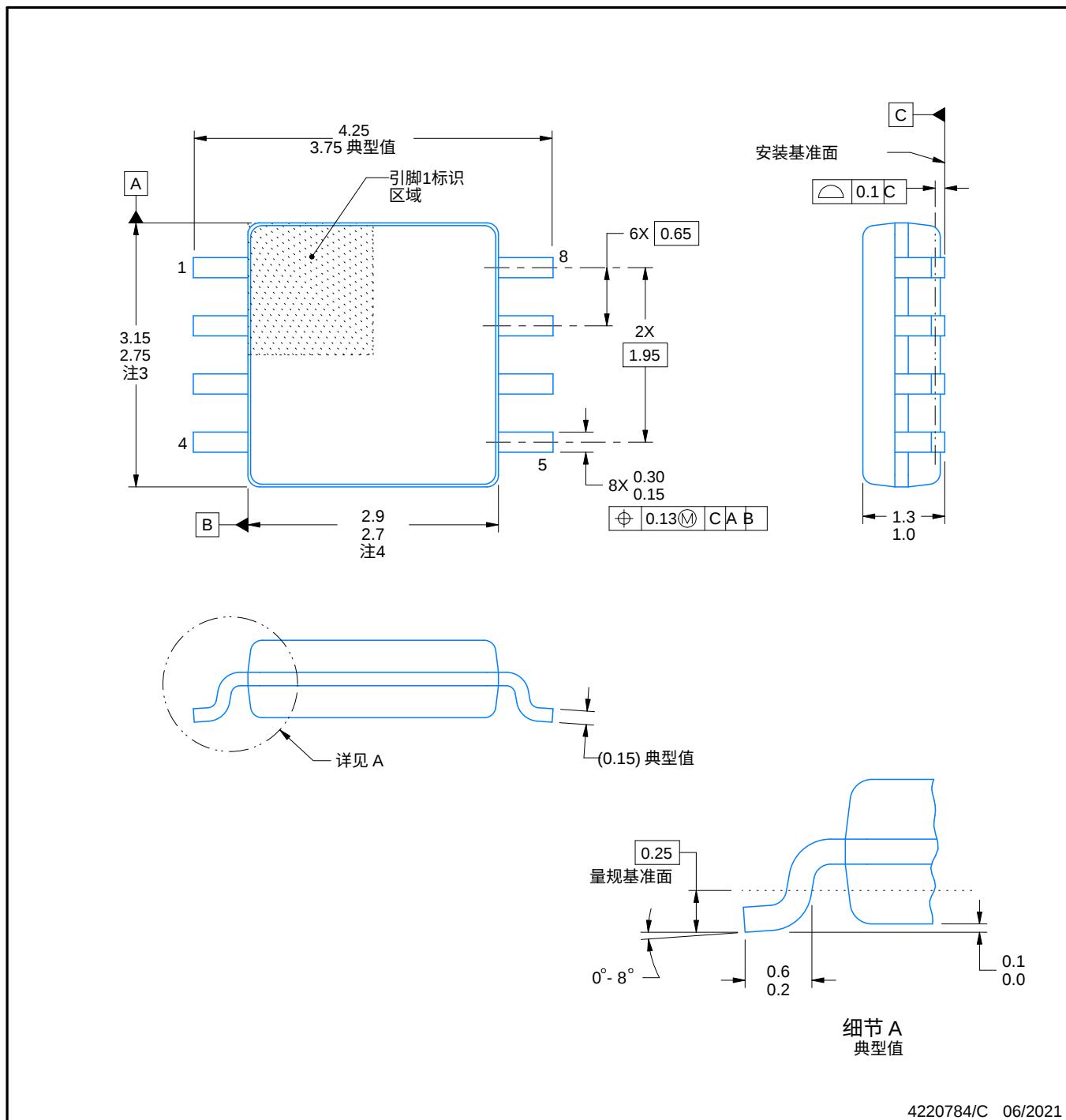
封装轮廓

DCT0008A



SSOP - 最大高度1.3毫米

小型轮廓封装



注释:

- 所有线性尺寸均以毫米为单位。括号内尺寸仅供参考。尺寸标注及公差符合 ASME Y14.5M 标准。
- 本图纸如有更改，恕不另行通知。
- 此尺寸不包括模具飞边、凸起或浇口毛刺。模具飞边、凸起或浇口毛刺每侧不得超过 0.15 毫米。
- 此尺寸不包括引脚间毛刺。引脚间毛刺每侧不得超过 0.25 毫米。

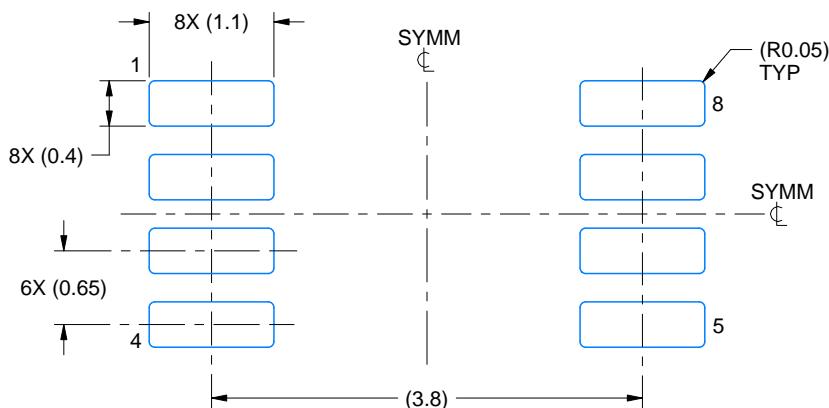
4220784/C 06/2021

EXAMPLE BOARD LAYOUT

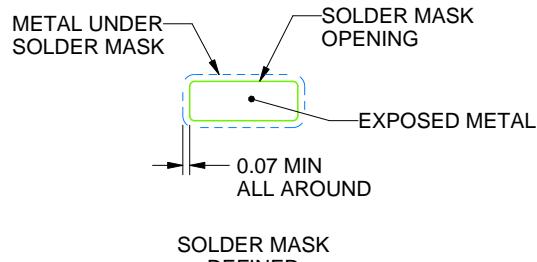
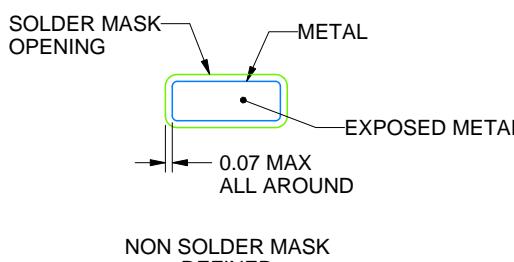
DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

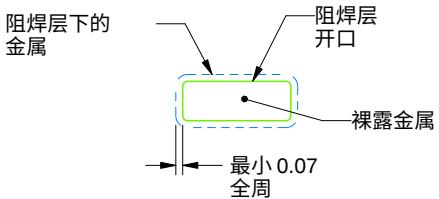
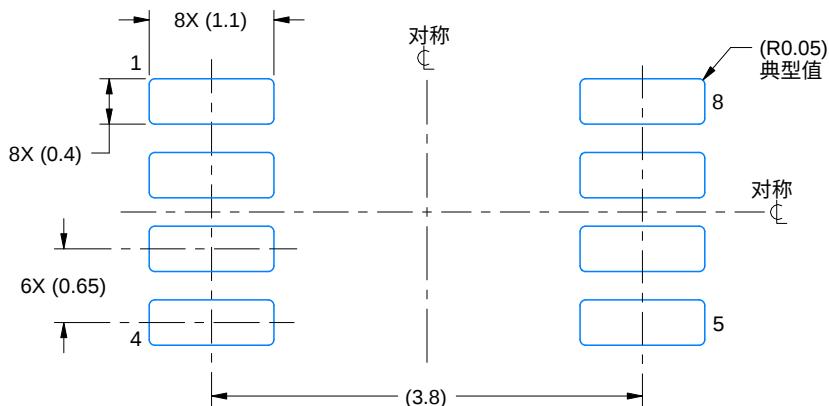
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

示例电路板布局

DCT0008A

SSOP - 最大高度1.3毫米

小型轮廓封装



阻焊层详细信息

4220784/C 06/2021

注释： (续)

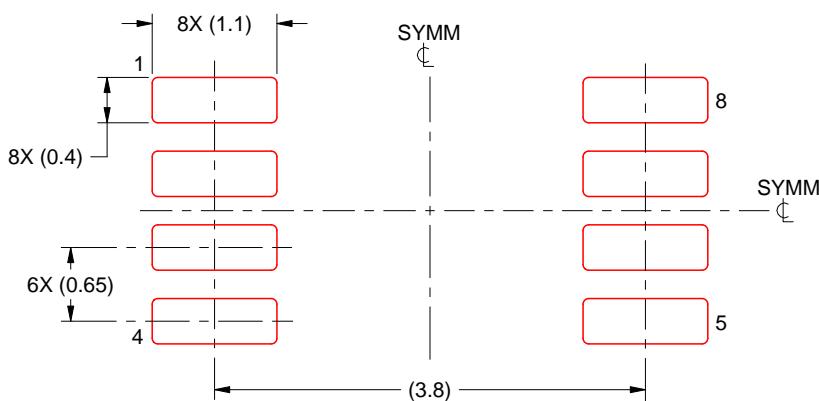
5. IPC-7351 出版物可能包含替代设计。
6. 阻焊层在信号焊盘之间及周围的公差可能因电路板制造地点而异。

EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

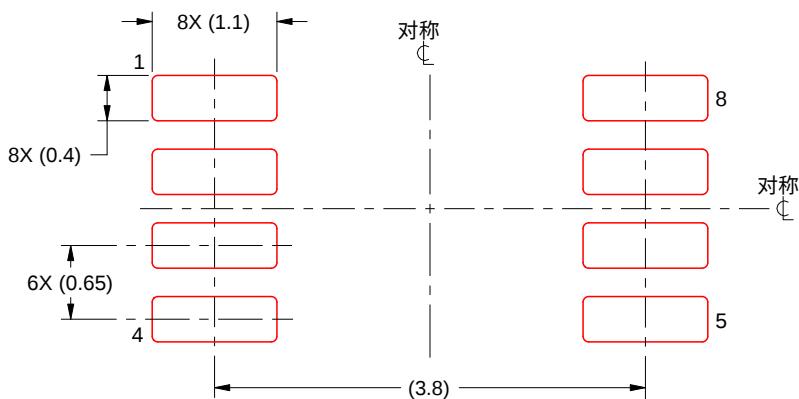
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

焊膏模板设计示例

DCT0008A

SSOP - 最大高度1.3毫米

小型轮廓封装



焊膏示例
基于0.125毫米厚模板
比例: 15X

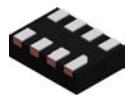
4220784/C 06/2021

注释: (续)

7. 采用梯形壁和圆角的激光切割开孔可实现更佳的焊膏释放效果。IPC-7525 可能提供替代的设计建议。
8. 电路板组装现场可能对模板设计有不同的建议。

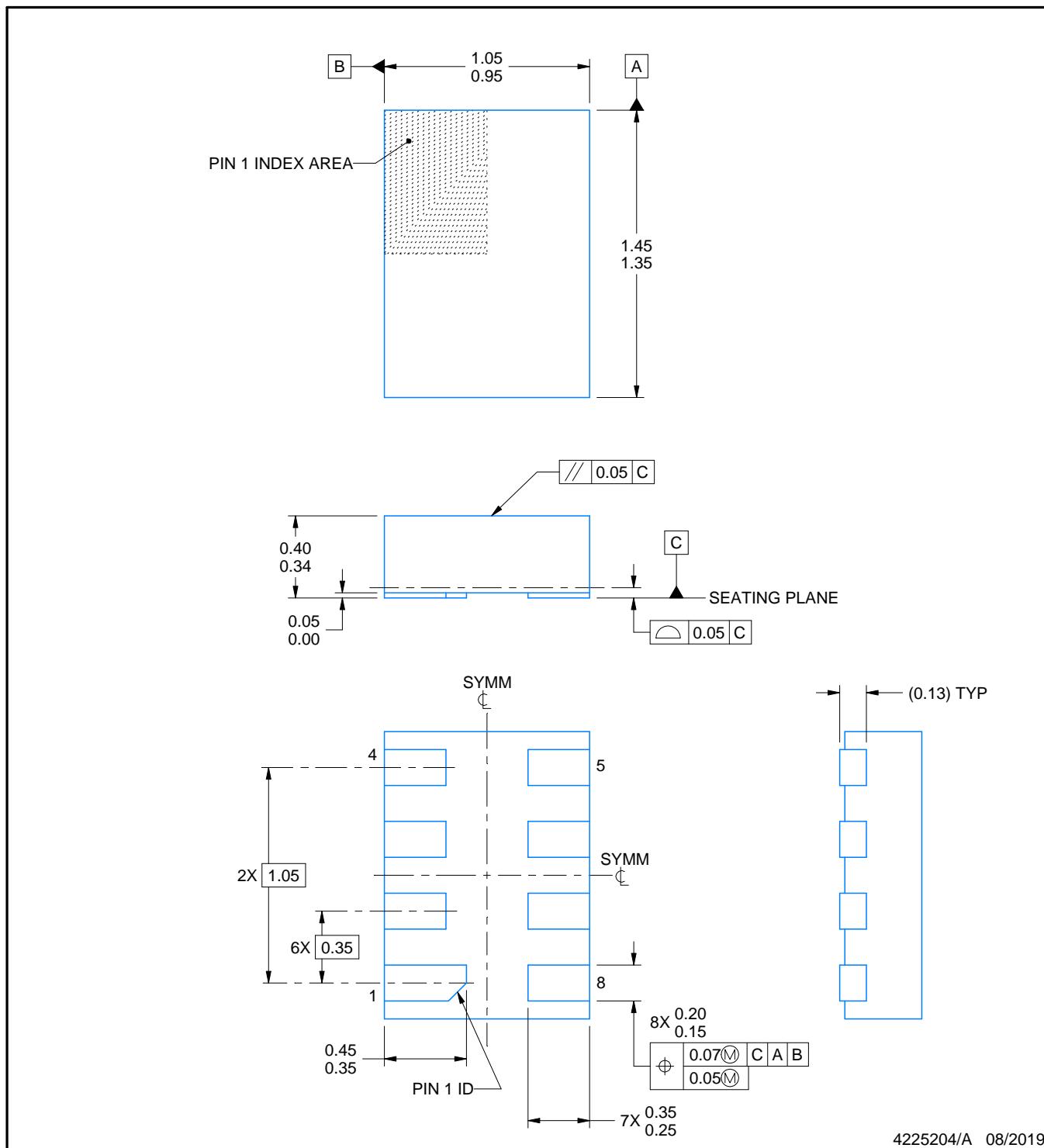
PACKAGE OUTLINE

DQE0008A



X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4225204/A 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-287 variation X2EAF.

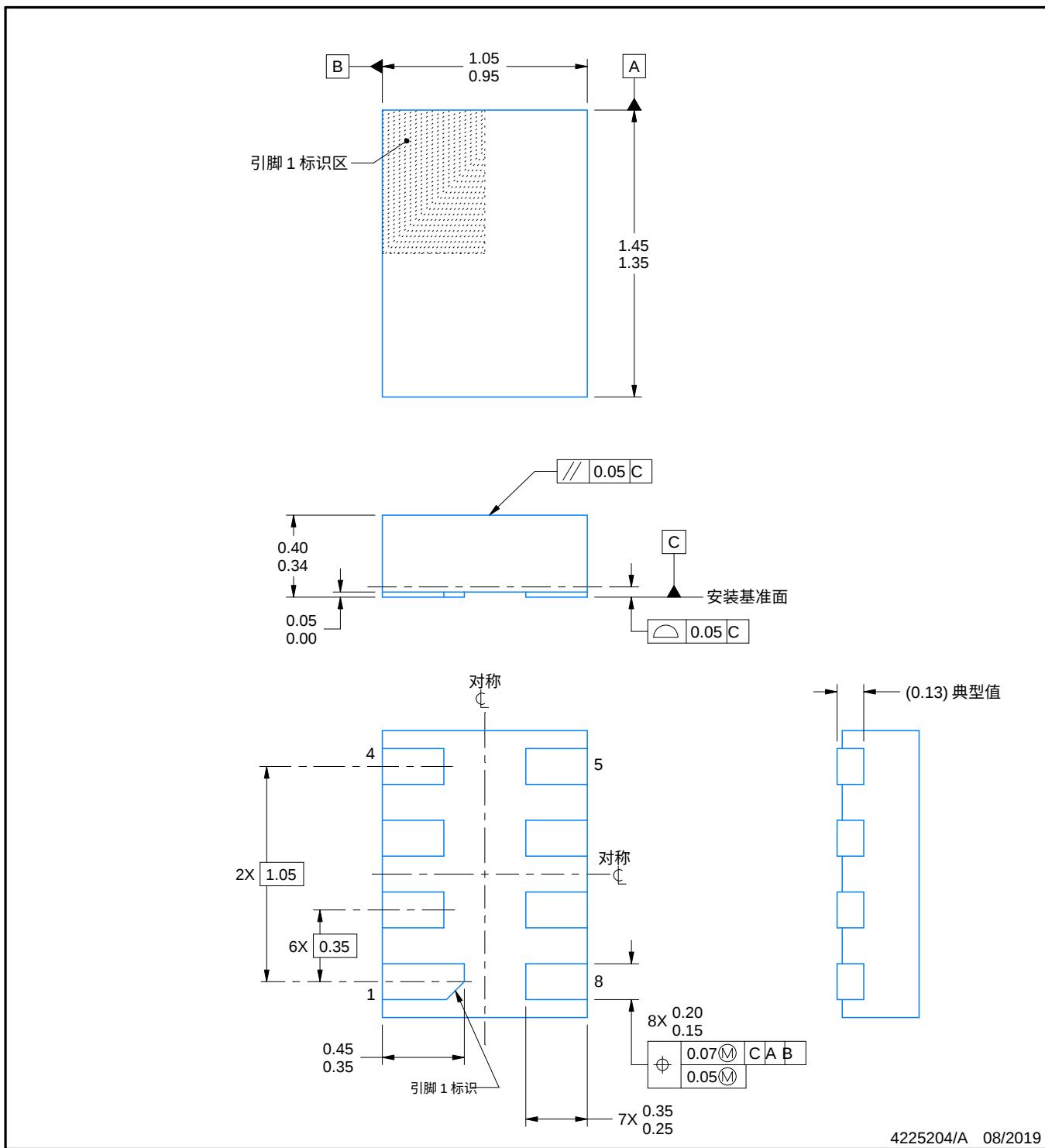
DQE0008A



封装轮廓

X2SON - 最大高度 0.4 mm

塑料小外形 - 无引脚



注释:

1. 所有线性尺寸均以毫米为单位。括号内尺寸仅供参考。尺寸标注及公差符合 ASME Y14.5M 标准。

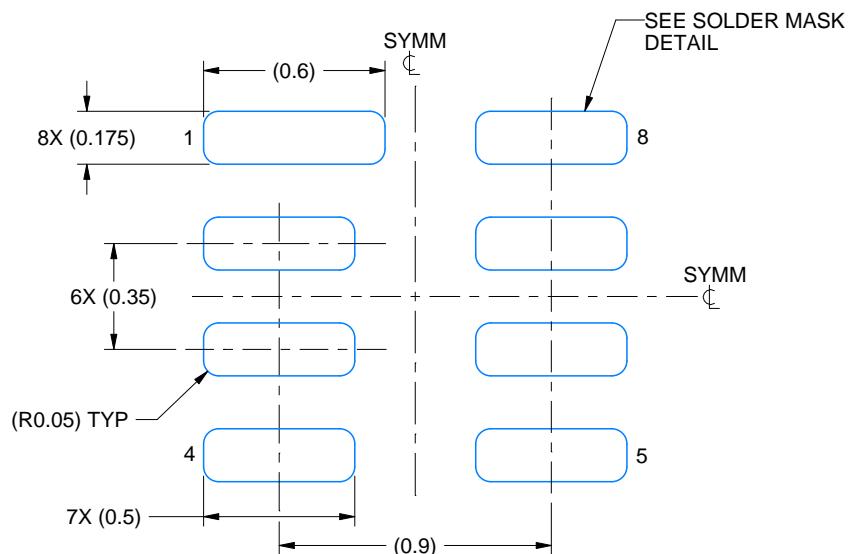
2. 本图纸如有更改，恕不另行通知。
3. 该封装符合 JEDEC MO-287 变体 X2EAF。

EXAMPLE BOARD LAYOUT

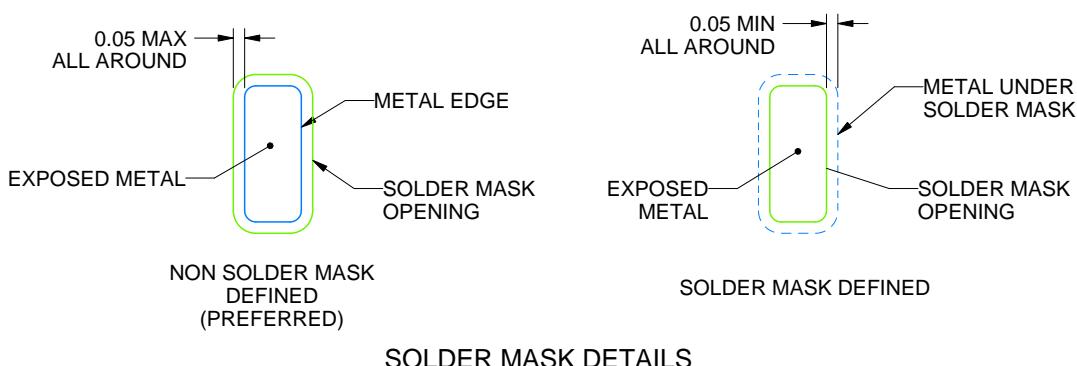
DQE0008A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



4225204/A 08/2019

NOTES: (continued)

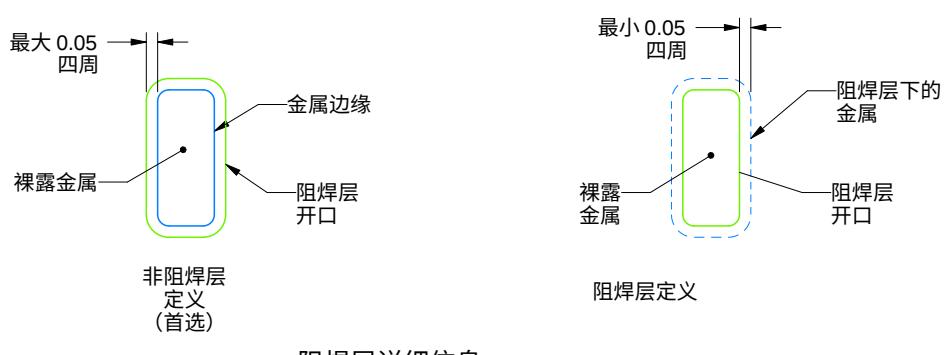
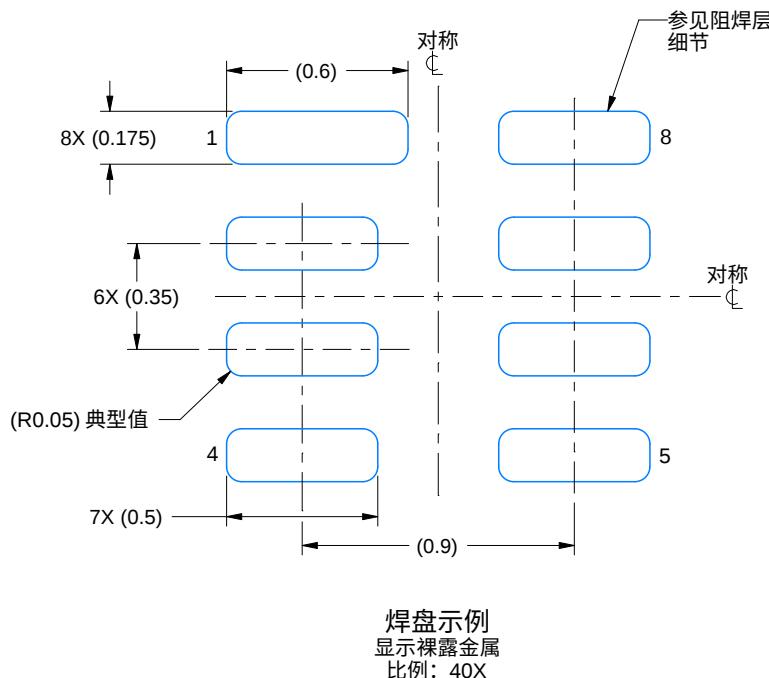
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

示例电路板布局

DQE0008A

X2SON - 最大高度 0.4 mm

塑料小外形 - 无引脚



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注释: (续)

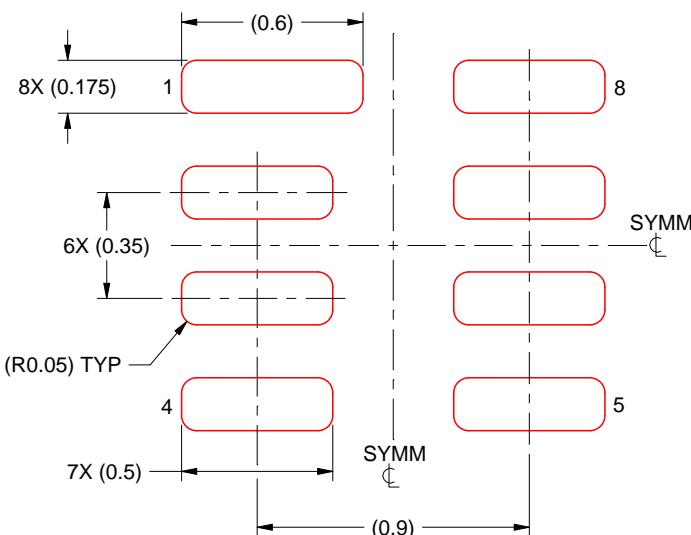
4. 该封装设计用于焊接至电路板上的散热焊盘。更多信息, 请参见德州仪器文献编号 SLUA271 (www.ti.com/lit/slua271)。

EXAMPLE STENCIL DESIGN

DQE0008A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 MM THICK STENCIL
SCALE: 40X

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NOTES: (continued)

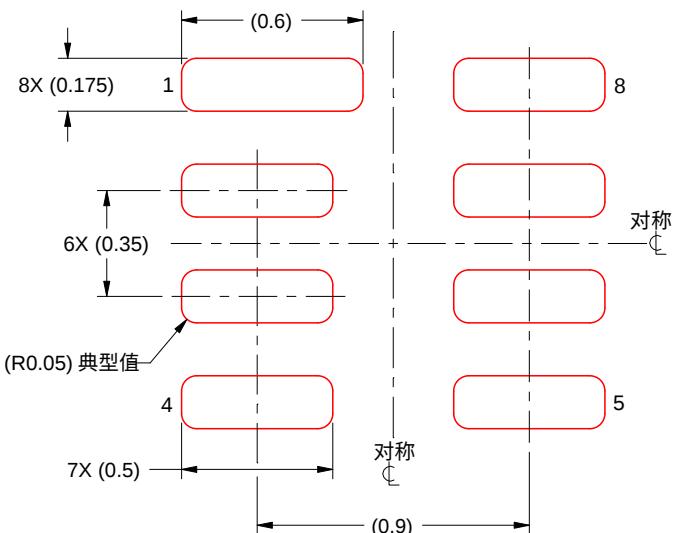
- Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

焊膏模板设计示例

DQE0008A

X2SON - 最大高度 0.4 mm

塑料小外形 - 无引脚



焊膏示例
基于 0.075 毫米厚钢网
比例: 40X

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注释: (续)

5. 采用梯形壁和圆角的激光切割开孔可实现更佳的焊膏释放效果。IPC-7525 可能提供替代的设计建议。

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