GENERAL DESCRIPTION

The CT7601 is a single chip audio USB 2.0/1.1 payback and record bridge.

FEATURES

- 2 playback port, and 1 record port

    PLAY 0: 8-channel I2S, 6-channel DSD, 2-channel SPDIF

    PLAY 1: 2-channel I2S, 2-channel DSD, 2-channel SPDIF

    RECORD: 8-channel I2S, 6-channel DSD, 2-channel SPDIF

    The clock systems are independent

- I2S Interface

    PLAY port supports standard/left justified format, master mode.

    RECORD port supports standard/left justified, master/slave mode.

- Audio transmission

    PCM support up to 768K/32bit through USB, I2S, SPDIF ports.

    DSD (PDM) support 1x/2x/4x/8x bandwidth through DSD(PDM) port.

    DSD (Native) support 1x/2x/4x/8x bandwidth through USB, I2S, DSD(PDM) , SPDIF ports.

    DoP support 1x/2x/4x bandwidth through USB, I2S, SPDIF ports.

- Interface

    Up to 16 GPIOs configurable as input or output.

    Master / Slave I^{2}C interface.

    Interrupt function.

    PWM-LED.

- Format auto detecting

    Auto detecting PCM / DoP format.

    Auto detecting I2S / DSD interface.

- Misc

    Embeded 8051 controller

    UART interface

    Volume control with fading in/out function.

    Playback basic auto De-pop function.

    One 12MHz crystal requirement only.

Table of Contents

FUNCTION BLOCK

CT7601 FAMILY

Description	CT7601PH	CT7601CH	CT7601PR	CT7601CR	CT7601SR
USB Port PLAY / RECORD					
USB PCM (Stereo)	768kHz / 32-bit	384kHz / 32-bit	768kHz / 32-bit	384kHz / 32-bit	192kHz / 32-bit
USB PCM (8 channel)	192K / 32-bit	96K / 32-bit	-	-	-
USB DoP	4x	2x	4x	2x	1x
USB DSD (Stereo)	8x	4x	8x	4x	2x
USB DSD (6 channel)	2x	1x	-	-	-
I2S Port					
I2S PCM (Stereo)	768kHz / 32-bit	384kHz / 32-bit	768kHz / 32-bit	384kHz / 32-bit	192kHz / 32-bit
I2S PCM (8 channel)	192K / 32-bit	96K / 32-bit	-	-	-
I2S DoP (Stereo)	4x	2x	4x	2x	1x
I2S Dop (8 channel)	1x	-	-	-	-
Native DSD (Stereo)	8x	4x	8x	4x	2x
Native DSD (6 channel)	2x	1x	-	-	-
SPDIF Port					
SPDIF PCM	768kHz / 32-bit	384kHz / 32-bit	768kHz / 32-bit	384kHz / 32-bit	192kHz / 32-bit
SPDIF DoP	4x	2x	4x	2x	1x
SPDIF native DSD	8x	4x	8x	4x	2x
Package					
Package	LQFP 80(H)	LQFP 80(H)	QFN 48(R)	QFN 48(R)	QFN 48(R)
GPIO	8+8	8+8	8	8	8
I2S Play 0 ch PCM	8	8	2	2	2
I2S Play 0 ch DSD	6	6	2	2	2
I2S Play 1 channel	2	2	-	-	-
I2S Record ch PCM	8	8	2	2	2
I2S Record ch DSD	6	6	2	2	2
SPDIF Play0 channel	2	2	2	2	2
SPDIF Play1 channel	2	2	-	-	-
SPDIF Record channel	2	2	2	2	2

** CT7601P is only for professional engineering design.

Package LQFP-80 (Top View) CT7601xL

Pin assignments (top side, left to right, pins 80–61):

Pin	Signal
80	SPDIF_C_EXT
79	SPDIF_IN
78	AVDD_33_SPDIF_RX
77	AVSS_SPDIF_RX
76	DVSS_CORE
75	DVDD_12_CORE
74	SPDIF_1_OUT
73	GPIO_B7
72	GPIO_B6
71	SPDIF_0_OUT
70	DVDD_33_PAD_D
69	DVSS_PAD_D
68	SPI_CS_Z_AND_POR_3
67	SPI_DATA_R
66	SPI_WP_Z_AND_POR_2
65	SPI_DATA_W_AND_POR_1
64	SPI_CLK_AND_POR_0
63	GPIO_B5
62	PWM_LIGHT_RIGHT
61	PWM_LIGHT_LEFT

Left side (pins 1–20):

Pin	Signal
1	USB_R_EXT
2	AVDD_33_USB_PHY
3	AVSS_USB_PHY
4	USB_DM
5	USB_DP
6	AVSS_USB_PLL
7	AVDD_12_USB_PLL
8	XTAL_IN_12MHZ
9	XTAL_OUT
10	DVDD_33_XTAL
11	DVSS_XTAL
12	CLK_REF_12MHZ
13	GPIO_B0
14	GPIO_B1
15	INTERRUPT_Z
16	DVSS_PAD_A
17	DVDD_33_PAD_A
18	GPIO_B2
19	I2C_SLAVE_SCLK_GPIO_A0
20	I2C_SLAVE_SDATA_GPIO_A1

Right side (pins 60–41):

Pin	Signal
60	GPIO_B4
59	GPIO_B3
58	CODEC_POWER_DOWN
57	UART_RX_GPIO_A7
56	UART_TX_GPIO_A6
55	AVDD_12_LPLL
54	AVSS_LPLL
53	DVSS_PAD_C2
52	DVDD_33_PAD_C2
51	I2S0_MCLK_DAC
50	I2S0_SCLK_OR_DSD0_SCLK_OUT
49	I2S0_SDATA_0_OR_DSD0_RIGHT_SDATA_OUT
48	I2S0_SDATA_1_OR_DSD0_2_OUT
47	I2S0_SDATA_2_OR_DSD0_3_OUT
46	I2S0_SDATA_3_OR_DSD0_4_OUT
45	DSD0_5_OUT
44	I2S0_SLR_OR_DSD0_LEFT_SDATA_OUT
43	DVDD_33_PAD_C1
42	DVSS_PAD_C1
41	I2S1_MCLK_DAC

Bottom side (pins 21–40):

Pin	Signal
21	PWM_LIGHT_GPIO_A2
22	I2C_MASTER_SDATA_GPIO_A3
23	I2C_MASTER_SCLK_GPIO_A4
24	DVDD_33_PAD_B
25	DVSS_PAD_B
26	AVSS_MPLL
27	AVDD_12_MPLL
28	I2S_SCLK_OR_DSD_SCLK_IN
29	I2S_SDATA_0_OR_DSD_RIGHT_SDATA_IN
30	I2S_SDATA_1_OR_DSD_2_IN
31	I2S_SDATA_2_OR_DSD_3_IN
32	I2S_SDATA_3_OR_DSD_4_IN
33	DSD_5_IN
34	I2S_SLR_OR_DSD1_LEFT_SDATA_IN
35	I2S_MCLK_ADC_GPIO_A5
36	DVDD_33_PAD_B
37	DVSS_PAD_B
38	I2S1_SLR_OR_DSD1_LEFT_SDATA_OUT
39	I2S1_SDATA_OR_DSD1_RIGHT_SDATA_OUT
40	I2S1_SCLK_OR_DSD1_SCLK_OUT

Package QFN-48 (Top View) CT7601xR

Pin	Signal
48	SPDIF_C_EXT
47	SPDIF_IN
46	AVDD_33_SPDIF_RX
45	AVSS_SPDIF_RX
44	DVDD_12_CORE
43	SPDIF_0_OUT
42	DVDD_33_PAD_D
41	SPI_CS_Z_AND_POR_3
40	SPI_DATA_R
39	SPI_WP_Z_AND_POR_2
38	SPI_DATA_W_AND_POR_1
37	SPI_CLK_AND_POR_0

Pin	Left signal		Right signal	Pin
1	USB_R_EXT		UART_RX_GPIO_A7	36
2	AVDD_33_USB_PHY		UART_TX_GPIO_A6	35
3	AVSS_USB_PHY		AVDD_12_LPLL	34
4	USB_DM		AVSS_LPLL	33
5	USB_DP		DVSS_PAD_C2	32
6	AVSS_USB_PLL		DVDD_33_PAD_C2	31
7	AVDD_12_USB_PLL		I2S0_MCLK_DAC	30
8	XTAL_IN_12MHZ		I2S0_SCLK_OR_DSD0_SCLK_OUT	29
9	XTAL_OUT		I2S0_SDATA_0_OR_DSD0_RIGHT_SDATA_OUT	28
10	DVDD_33_XTAL		I2S0_SLR_OR_DSD0_LEFT_SDATA_OUT	27
11	DVSS_XTAL		DVDD_33_PAD_C1	26
12	I2C_SLAVE_SCLK_GPIO_A0		DVSS_PAD_C1	25

Pin	Signal
13	I2C_SLAVE_SDATA_GPIO_A1
14	PWM_LIGHT_GPIO_A2
15	I2C_MASTER_SDATA_GPIO_A3
16	I2C_MASTER_SCLK_GPIO_A4
17	AVSS_MPLL
18	AVDD_12_MPLL
19	I2S_SCLK_OR_DSD_SCLK_IN
20	I2S_SDATA_0_OR_DSD_RIGHT_SDATA_IN
21	I2S_SLR_OR_DSD_LEFT_SDATA_IN
22	I2S_MCLK_ADC_GPIO_A5
23	DVDD_33_PAD_B
24	DVSS_PAD_B

LQFP 48/80 PIN DESCRIPTION

Pin Name	80Pin No.	48Pin No.	Type	Description
USB_R_EXT	1	1	I	*USB external resistor :* 1.8k ohm (1%) pull low
AVDD_33_USB_PHY	2	2	P	*3.3V Pad Power Connection:* Power supply for USB physical layer. Connect to 3.3V.
AVSS_USB_PHY	3	3	G	*Ground Connections:* Connect all ground pins to the common system ground plane.
USB_DM	4	4	I/O	*USB D - :* refer to USB Specification.
USB_DP	5	5	I/O	*USB D + :* refer to USB Specification.
AVSS_USB_PLL	6	6	G	*Ground Connections:* Connect all ground pins to the common system ground plane.
AVDD_12_USB_PLL	7	7	P	*1.2V Core Power Connection:* Power supply for USB PLL function. Connect to 1.2V.
XTAL_IN_12MHZ	8	8	I	*External Crystal input:* Connect to external crystal pin. Or external clock input. Selection : 12 MHz
XTAL_OUT	9	9	O	*External Crystal output:* Connect to external crystal pin
DVDD_33_XTAL	10	10	P	*3.3V Pad Power Connection:* Power supply for I/O buffer. Connect to 3.3V.
DVSS_XTAL	11	11	G	*Ground Connections:* Connect all ground pins to the common system ground plane.
CLK_REF_12MHZ	12		O	*Reference clock output:* Crystal clock output with buffer pad.
GPIO_B0	13		I/O	*General purpose input/output pin bank_B[0] :* 3.3V TTL input/output pin, define by internal control register.
GPIO_B1	14		I/O	*General purpose input/output pin bank_B[1] :* 3.3V TTL input/output pin, define by internal control register.
INTERRUPT_Z*	15		I/O	*Interrupt open drain input/output:* Internal pull high 120k-ohm.
DVSS_PAD_A	16		G	*Ground Connections:* Connect all ground pins to the common system ground plane.
DVDD_33_PAD_A	17		P	*3.3V Pad Power Connection:* Power supply for I/O buffer. Connect to 3.3V.
GPIO_B2	18		I/O	*General purpose input/output pin bank_B[2] :* 3.3V TTL input/output pin, define by internal control register.
I2C_SLAVE_SCLK _GPIO_A0	19	12	I/O	*I2C slave serial clock :* Clock pin for serial interface. Refer to I2C specification. *General purpose input/output pin bank_A[0] :* 3.3V TTL input/output pin, define by internal control register.
I2C_SLAVE_SDATA _GPIO_A1	20	13	I/O	*I2C slave serial data :* Data pin for serial interface. Refer to I2C specification. *General purpose input/output pin bank_A[1] :* 3.3V TTL input/output pin, define by internal control register.
PWM_LIGHT _GPIO_A2	22	14	I/O	*USB Play channel 0 audio left/right channel PWM light control output :* refer to programming guide *General purpose input/output pin bank_A[2] :* 3.3V TTL input/output pin, define by internal control register.
I2C_MASTER_SDATA _GPIO_A3	22	15	I/O	*I2C master serial data :* Data pin for serial interface. Refer to I2C specification. *General purpose input/output pin bank_A[3] :* 3.3V TTL input/output pin, define by internal control register.
I2C_MASTER_SCLK _GPIO_A4	23	16	I/O	*I2C master serial clock :* Clock pin for serial interface. Refer to I2C specification.

Pin Name	80Pin No.	48Pin No.	Type	Description
				General purpose input/output pin bank_A[4] : 3.3V TTL input/output pin, define by internal control register.
DVDD_33_PAD_B	24		P	**3.3V Pad Power Connection:** Power supply for I/O buffer. Connect to 3.3V.
DVSS_PAD_B	25		G	**Ground Connections:** Connect all ground pins to the common system ground plane.
AVSS_MPLL	26	17	G	**Ground Connections:** Connect all ground pins to the common system ground plane.
AVDD_12_MPLL	27	18	P	**1.2V MPLL Connection:** Power supply for all digital and MPLL function. Connect to 1.2V.
I2S_SCLK_OR _DSD_SCLK_IN	28	19	I/O	**I2S serial clock input :** 3.3V TTL input, refer to I2S Specification. **DSD serial clock input :** 3.3V TTL input, refer to DSD Specification.
I2S_SDATA_0_OR _DSD_RIGHT_SDATA_IN	29	20	I/O	**I2S serial data0 input :** 3.3V TTL input, refer to I2S Specification. **DSD serial right data (channel 1) input:** 3.3V TTL input, refer to DSD Specification.
I2S_SDATA_1_OR _DSD_2_IN	30		I/O	**I2S serial data1 input :** 3.3V TTL input, refer to I2S Specification. **DSD serial data2 input:** 3.3V TTL input, refer to DSD Specification.
I2S_SDATA_2_OR _DSD_3_IN	31		I/O	**I2S serial data2 input :** 3.3V TTL input, refer to I2S Specification. **DSD serial data3 input:** 3.3V TTL input, refer to DSD Specification.
I2S_SDATA_3_OR _DSD_4_IN	32		I/O	**I2S serial data3 input :** 3.3V TTL input, refer to I2S Specification. **DSD serial data4 input:** 3.3V TTL input, refer to DSD Specification.
DSD_5_IN	33		I/O	**DSD serial data5 input:** 3.3V TTL input, refer to DSD Specification.
I2S_SLR_OR _DSD_LEFT_SDATA_IN	34	21	I/O	**I2S left/right input :** 3.3V TTL input, refer to I2S Specification. **DSD serial left data (channel 0) input:** 3.3V TTL input, refer to DSD Specification.
I2S_MCLK_ADC _GPIO_A5	35	22	I/O	**I2S master clock output:** 3.3V TTL output, refer to ADC Document. **General purpose input/output pin bank_A[5] :** 3.3V TTL input/output pin, define by internal control register.
DVDD_33_PAD_B	36	23	P	**3.3V Pad Power Connection:** Power supply for I/O buffer. Connect to 3.3V.
DVSS_PAD_B	37	24	G	**Ground Connections:** Connect all ground pins to the common system ground plane.
I2S1_SLR_OR _DSD1_LEFT_SDATA_OUT	38		O	**I2S1 left/right output :** 3.3V TTL output, refer to I2S Specification. **DSD1 serial left data (channel 0) output:** 3.3V TTL output, refer to DSD Specification.
I2S1_SDATA_OR _DSD1_RIGHT_SDATA_OUT	39		O	**I2S1 serial data0 output :** 3.3V TTL output, refer to I2S Specification. **DSD1 serial right data (channel 1) output:** 3.3V TTL output, refer to DSD Specification.
I2S1_SCLK_OR _DSD1_SCLK_OUT	40		O	**I2S1 serial clock output:** 3.3V TTL output, refer to I2S Specification. **DSD1 serial clock output:** 3.3V TTL output, refer to DSD Specification.
I2S1_MCLK_DAC	41		O	**I2S1 master clock output:** 3.3V TTL output, refer to DAC Document.
DVSS_PAD_C1	42	25	G	**Ground Connections:** Connect all ground pins to the common system ground plane.
DVDD_33_PAD_C1	43	26	P	**3.3V Pad Power Connection:** Power supply for I/O buffer. Connect to 3.3V.
I2S0_SLR_OR _DSD0_LEFT_SDATA_OUT	44	27	O	**I2S0 left/right output :** 3.3V TTL output, refer to I2S Specification. **DSD0 serial left data (channel 0) output:** 3.3V TTL output, refer to DSD Specification.
DSD0_5_OUT	45		O	**DSD0 serial data 5 output:** 3.3V TTL output, refer to DSD Specification.
I2S0_SDATA_3 _OR_DSD0_4_OUT	46		O	**I2S0 serial data 3 output :** 3.3V TTL output, refer to I2S Specification. **DSD0 serial data 4 output:** 3.3V TTL output, refer to DSD

Pin Name	80Pin No.	48Pin No.	Type	Description
				Specification.
I2S0_SDATA_2 _OR_DSD0_3_OUT	47		O	**I2S0 serial data 2 output :** 3.3V TTL output, refer to I2S Specification. **DSD0 serial data 3 output:** 3.3V TTL output, refer to DSD Specification.
I2S0_SDATA_1 _OR_DSD0_2_OUT	48		O	**I2S0 serial data 1 output :** 3.3V TTL output, refer to I2S Specification. **DSD0 serial data 2 output:** 3.3V TTL output, refer to DSD Specification.
I2S0_SDATA_0_OR _DSD0_RIGHT_SDATA_OUT	49	28	O	**I2S0 serial data 0 output :** 3.3V TTL output, refer to I2S Specification. **DSD0 serial right data (channel 1) output:** 3.3V TTL output, refer to DSD Specification.
I2S0_SCLK_OR _DSD0_SCLK_OUT	50	29	O	**I2S0 serial clock output:** 3.3V TTL output, refer to I2S Specification. **DSD0 serial clock output:** 3.3V TTL output, refer to DSD Specification.
I2S0_MCLK_DAC	51	30	O	**I2S0 master clock output:** 3.3V TTL output, refer to DAC Document.
DVDD_33_PAD_C2	52	31	P	**3.3V Pad Power Connection:** Power supply for I/O buffer. Connect to 3.3V.
DVSS_PAD_C2	53	32	G	**Ground Connections:** Connect all ground pins to the common system ground plane.
AVSS_LPLL	54	33	G	**Ground Connections:** Connect all ground pins to the common system ground plane.
AVDD_12_LPLL	55	34	P	**1.2V Core Power Connection:** Power supply for all digital and audio PLL function. Connect to 1.2V.
UART_TX _GPIO_A6	56	35	I/O	**UART transmitter output:** 3.3V TTL output, refer to RS232 Specification. **General purpose input/output pin bank_A[6] :** 3.3V TTL input/output pin, define by internal control register.
UART_RX _GPIO_A7	57	36	I/O	**UART receiver input:** 3.3V TTL input, refer to RS232 Specification. **General purpose input/output pin bank_A[7] :** 3.3V TTL input/output pin, define by internal control register.
CODEC_POWER_DOWN	58		O	**Play 0 or Play 1kernel fast mute control to next device:** 3.3V TTL output
GPIO_B3	59		I/O	**General purpose input/output pin bank_B[3] :** 3.3V TTL input/output pin, define by internal control register.
GPIO_B4	60		I/O	**General purpose input/output pin bank_B[4] :** 3.3V TTL input/output pin, define by internal control register.
PWM_LIGHT_LEFT	61		O	**USB Play channel 0 audio left channel PWM light control output :** refer to programming guide
PWM_LIGHT_RIGHT	62		O	**USB Play channel 0 audio right channel PWM light control output :** refer to programming guide
GPIO_B5	63		I/O	**General purpose input/output pin bank_B[5] :** 3.3V TTL input/output pin, define by internal control register.
SPI_CLK_AND _POR_0	64	37	I/O	**SPI interface clock :** 3.3V TTL output, refer to SPI flash memory Specification. **Power on latch selection pin 0:** 3.3V TTL input, reserved for internal software
SPI_DATA_W_AND _POR_1	65	38	I/O	**SPI interface data output :** 3.3V TTL output, refer to SPI flash memory Specification. **Power on latch selection pin 1:** 3.3V TTL input, reserved for internal software
SPI_WP_Z_AND _POR_2	66	39	I/O	**SPI interface write protected (low active):** 3.3V TTL output, refer to SPI flash memory Specification. **Power on latch selection pin 2:** 3.3V TTL input, reserved for internal software

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Aspalathus

CT7601 audio USB bridge

| Pin Name	80Pin No.	48Pin No.	Type	Description
SPI_DATA_R	67	40	I	**SPI interface data input:** 3.3V TTL input, refer to SPI flash memory Specification.
SPI_CS_Z_AND _POR_3	68	41	I/O	**SPI interface chip selection (low active):** 3.3V TTL output, refer to SPI flash memory Specification. **Power on latch selection pin 3:** 3.3V TTL input, reserved for internal software
DVSS_PAD_D	69		G	**Ground Connections:** Connect all ground pins to the common system ground plane.
DVDD_33_PAD_D	70	42	P	**3.3V Pad Power Connection:** Power supply for I/O buffer. Connect to 3.3V.
SPDIF_0_OUT	71	43	O	**SPDIF play channel 0 output:** 3.3V TTL output, refer to SPDIF Specification.
GPIO_B6	72		I/O	**General purpose input/output pin bank_B[6] :** 3.3V TTL input/output pin, define by internal control register.
GPIO_B7	73		I/O	**General purpose input/output pin bank_B[7] :** 3.3V TTL input/output pin, define by internal control register.
SPDIF_1_OUT	74		O	**SPDIF play channel 1 output:** 3.3V TTL output, refer to SPDIF Specification.
DVDD_12_CORE	75	44	P	**1.2V Core Power Connection:** Power supply for all digital function. Connect to 1.2V.
DVSS_CORE	76		G	**Ground Connections:** Connect all ground pins to the common system ground plane.
AVSS_SPDIF_RX	77	45	G	**Ground Connections:** Connect all ground pins to the common system ground plane.
AVDD_33_SPDIF_RX	78	46	P	**3.3V Pad Power Connection:** Power supply for I/O buffer. Connect to 3.3V.
SPDIF_IN	79	47	I	**SPDIF input channel 4P:** 200mV ~ 3.3 V differential input, refer to SPDIF Specification.
SPDIF_C_EXT	80	48	I	**SPDIF input channel 4N:** 200mV ~ 3.3 V differential input, refer to SPDIF Specification **SPDIF input Vref :** internal SPDIF Vref. While CR1A.6 = 1.

Note: Internal 120K *pull-up or #pull down resistors present on inputs marked with *# respectively. Design should not rely solely on internal pull-up or pull down resistor to set I/O pins high or low respectively.

Version 0.3   - 10 -   4/7/2017

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ELECTRICAL CHARACTERISTICS

DC specifications

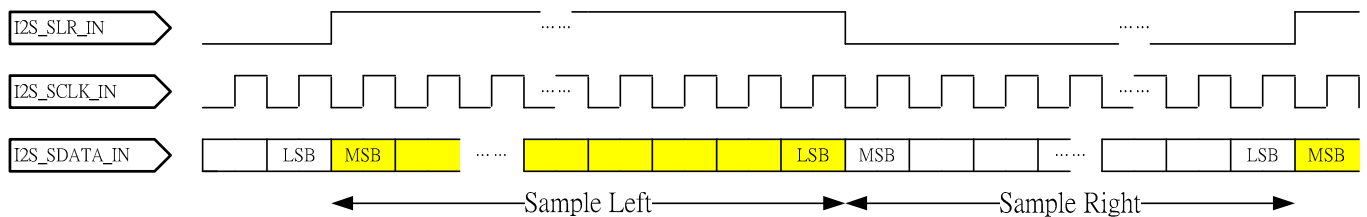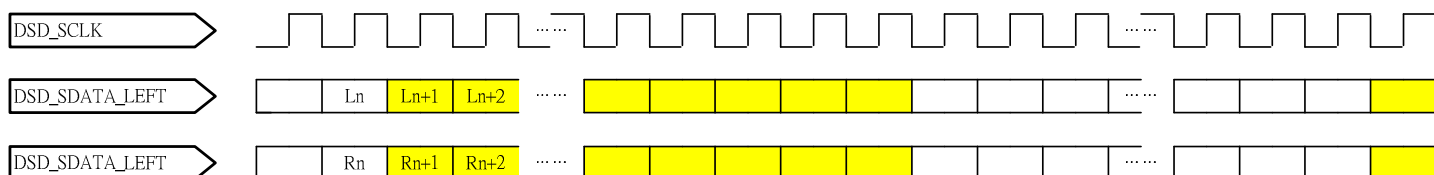| Symbol	Parameter	Min.	Max.	Units	Notes
Absolute VDD CORE	1.2V core supply Voltage	-0.5	1.32	V	
Absolute VDD I/O	3.3V I/O supply Voltage	-0.5	3.6	V	
Ts	Storage Temperature	-65	150	°C	
Ta	Ambient Temperature	0	70	°C	
Absolute Vih	3.3V input high voltage	-0.5	3.6	V	
Absolute Vil	3.3V input low voltage	-0.5		V	
ESD	Input ESD protection	2		KV	Human body mode
Operating Vdd CORE	1.2V core supply Voltage	1.08	1.32	V	
Operating Vdd I/O	3.3V I/O supply Voltage	3.135	3.465	V	
Operating Vih	3.3V input high voltage	2.0	Vdd+0.3	V	
Operating Vil	3.3V input low voltage	Vss-0.3	0.8	V	
Operating Iil	Input leakage current	-5	+5	uA	
Operating Voh	3.3V output high voltage	2.4		V	Ioh=-1mA
Operating Vol	3.3V output low voltage		0.4	V	Iol=1mA
Cin	Input pin capacitance		5	pF	
Cxtal	XTAL pin capacitance	13.5	22.5	pF	17..20 pF
Cout	Output pin capacitance		6	pF	
Lpin	Pin inductance		7	nH	
Operating Current	3.3V active supply current		17	mA	PCM 768K/32bit In/Out
	1.2V active supply current		33	mA	PCM 768K/32bit In/Out
Power down	3.3V supply current		0.29	mA	
	1.2V supply current		0.18	mA	
SPDIF Rx Input Sensitivity		0.100	1.500	3.300	V

SPDIF interface
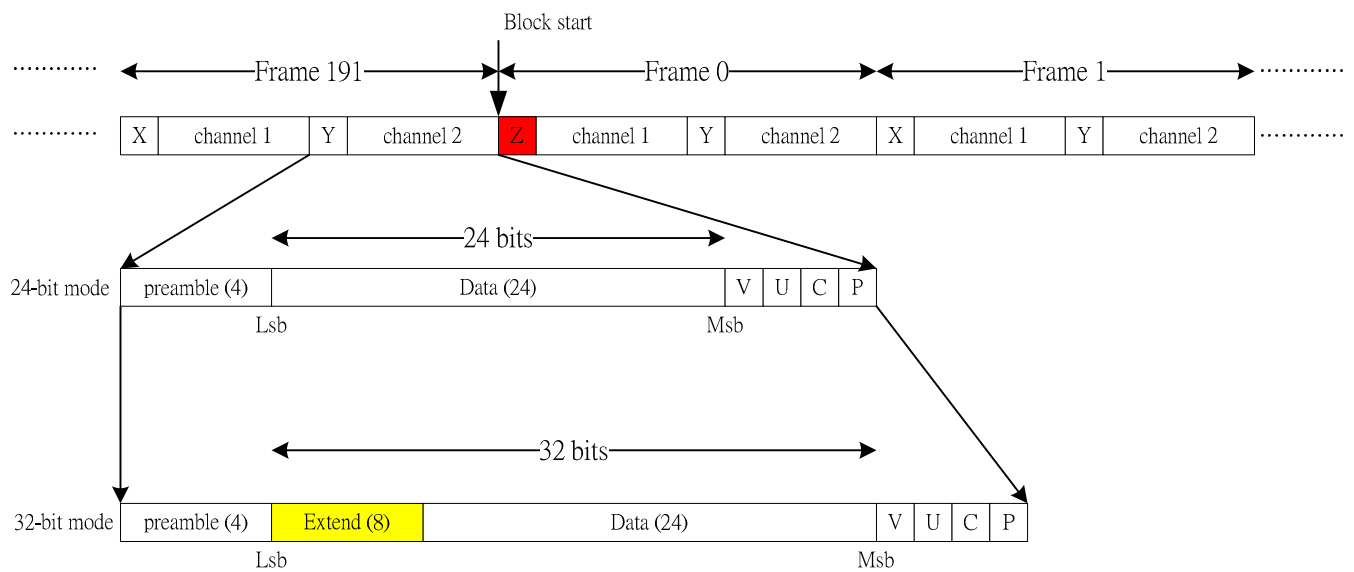
I2S interface

I2S standard format
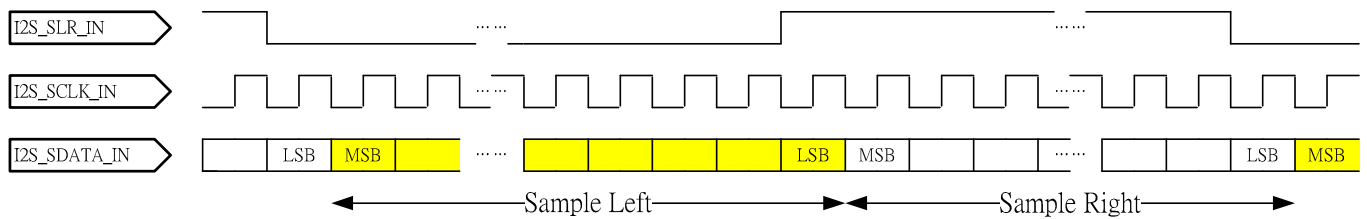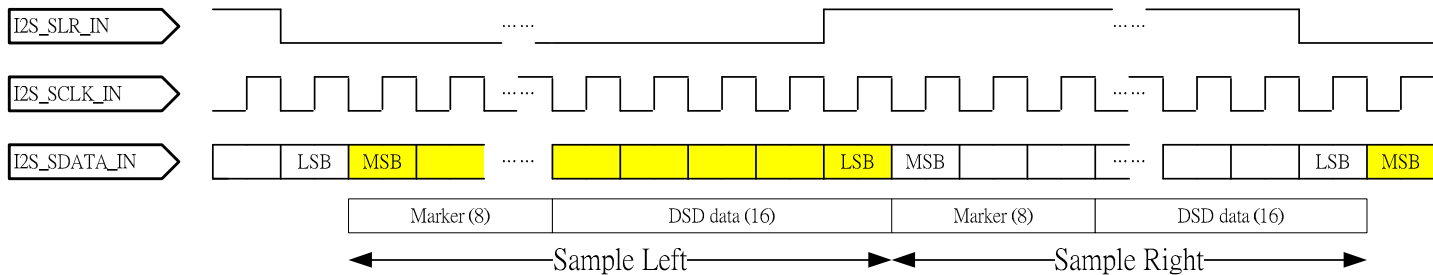

I2S left justified format

DSD interface

DoP interface

DSD over PCM through SPDIF

Block start

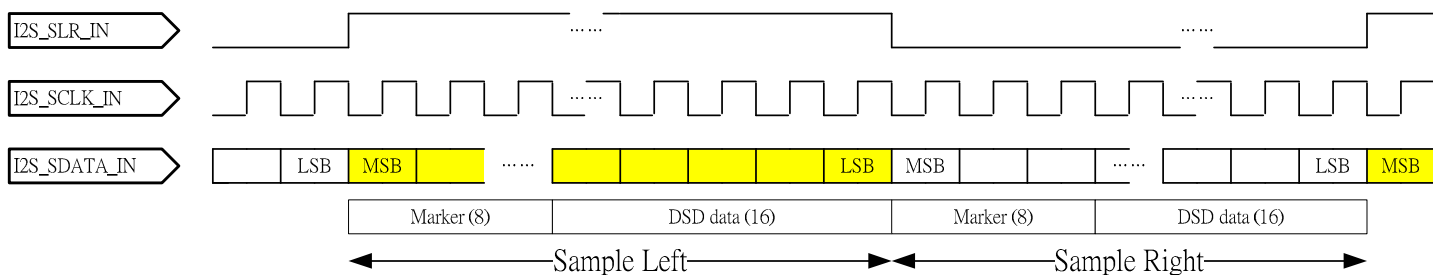············ ◄——————Frame 191——————► ◄——————Frame 0——————► ◄——————Frame 1——————► ············

············ | X | channel 1 | Y | channel 2 | Z | channel 1 | Y | channel 2 | X | channel 1 | Y | channel 2 | ············

◄——————24 bits——————►

| 24-bit mode | preamble (4) | Data (24) | V | U | C | P |

| DSD data (16) | Marker (8) |

Lsb   Msb

◄——————32 bits——————►

| 32-bit mode | preamble (4) | Extend (8) | Data (24) | V | U | C | P |
| | | Un-used (8) | DSD data (16) | Marker (8) | | | | |

Lsb   Msb
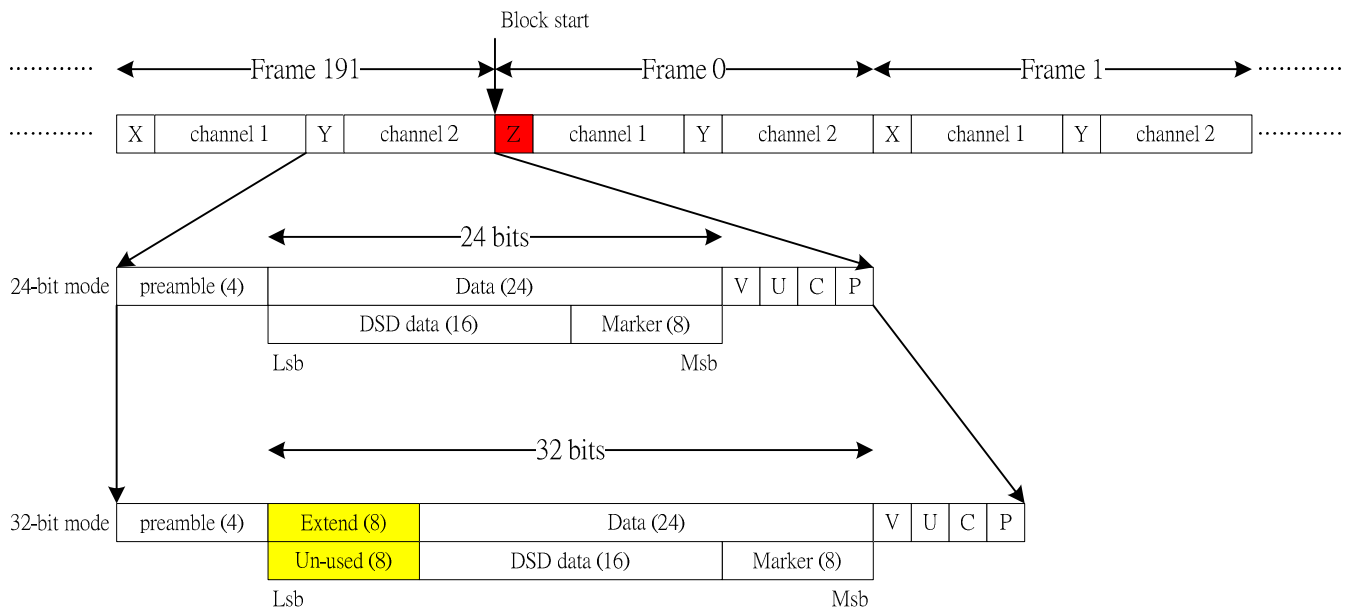
DSD over PCM through I2S

I2S standard format

I2S_SLR_IN

I2S_SCLK_IN

I2S_SDATA_IN | LSB | MSB | ...... | LSB | MSB | ...... | LSB | MSB |

| Marker (8) | DSD data (16) | Marker (8) | DSD data (16) |

◄——————Sample Left——————► ◄——————Sample Right——————►

I2S left justified format

I2S_SLR_IN

I2S_SCLK_IN

I2S_SDATA_IN | LSB | MSB | ...... | LSB | MSB | ...... | LSB | MSB |

| Marker (8) | DSD data (16) | Marker (8) | DSD data (16) |

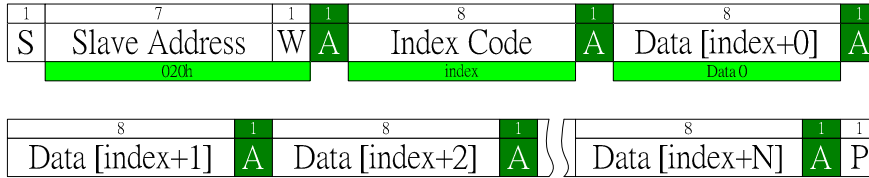◄——————Sample Left——————► ◄——————Sample Right——————►
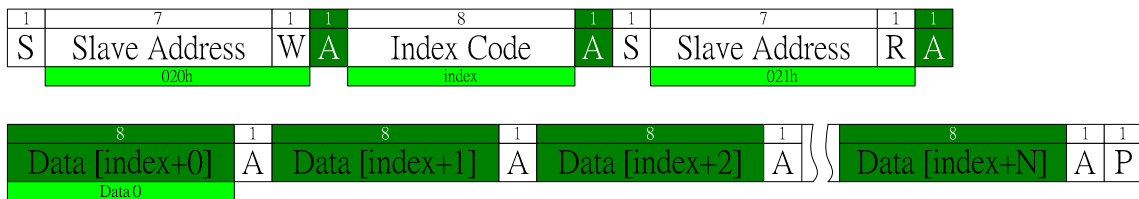
Comtrue Inc.

I2C interface

Register write command :

Slave address = 0x28

Register read command :

Slave address = 0x29

Block Write

Block Read

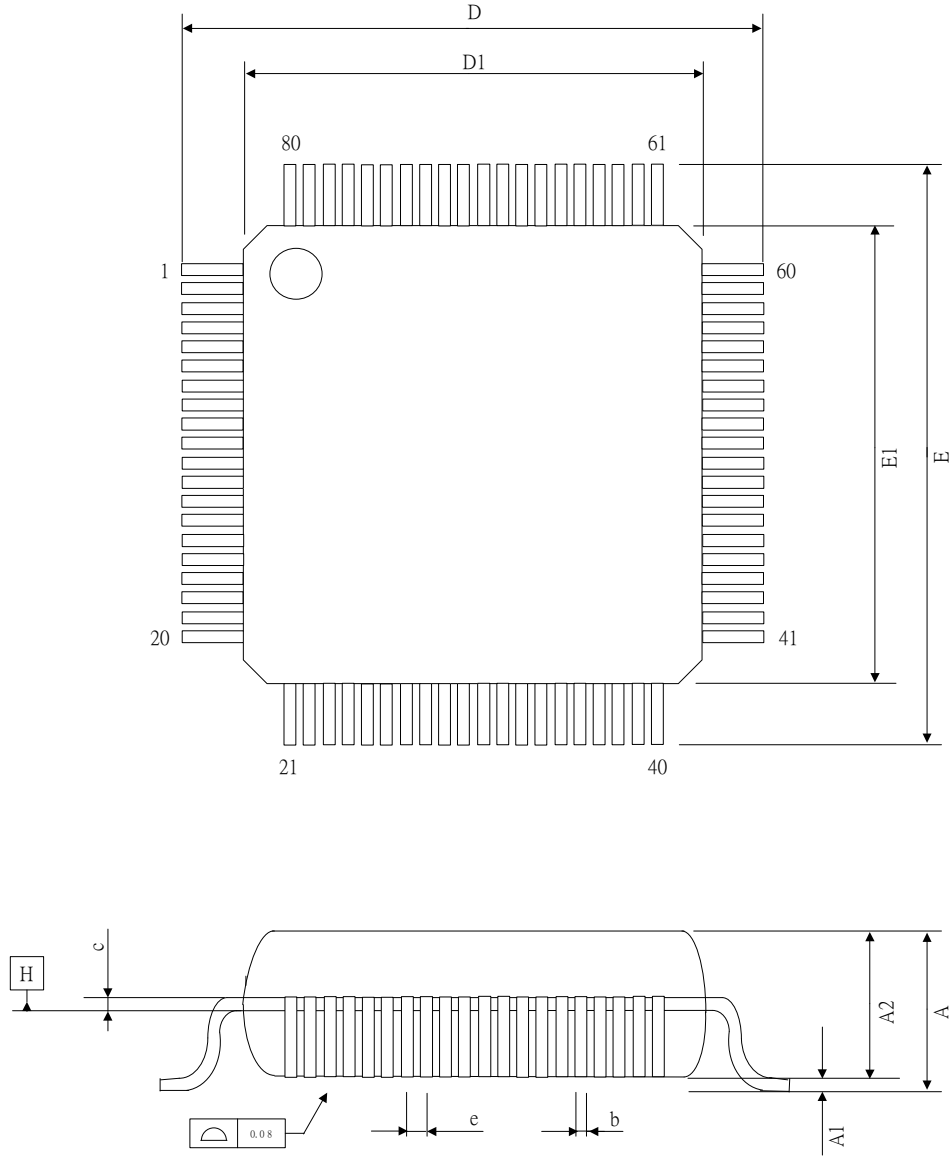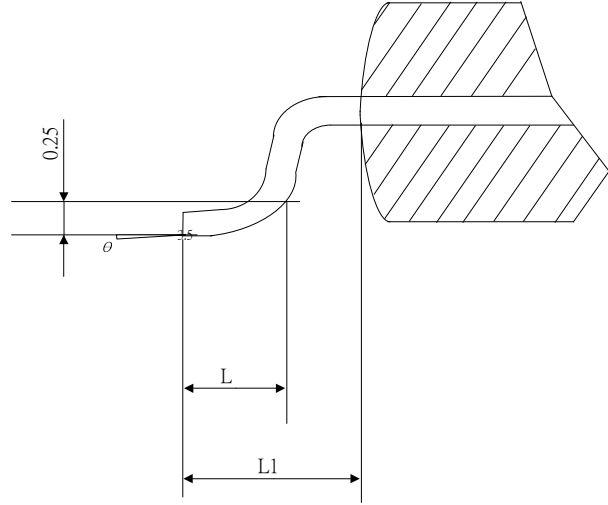Aspalathus

Comtrue Inc.
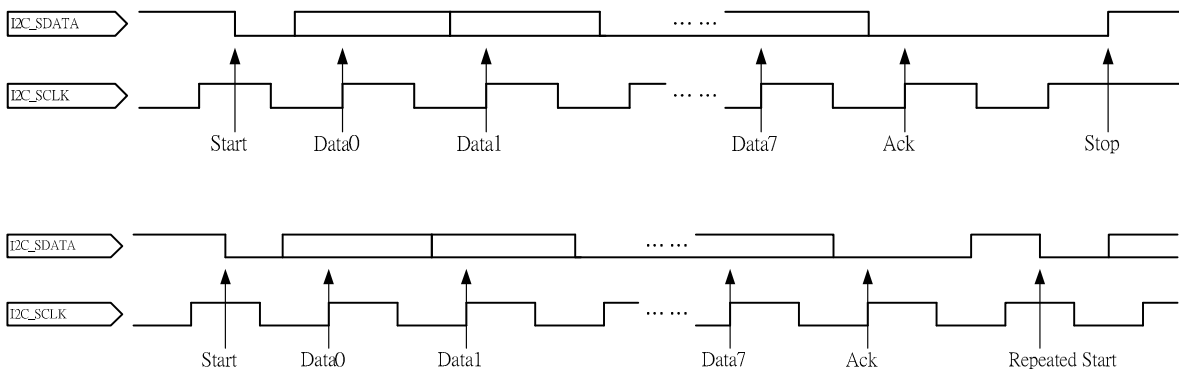
Package outline LQFP 80 pins

Version 0.3

VARIATIONS (All Dimensions Shown in mm)

Symbols	Min.	Nom.	Max.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	--	0.20
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

C0.35X45°

PAD SIZE : 185x18*MIL

0.08 MAX. C
SEATING PLANE
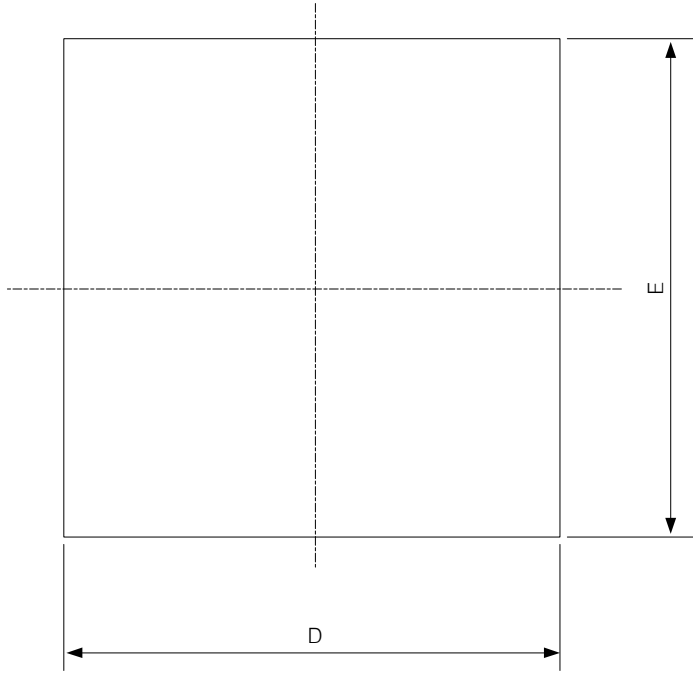
VARIATIONS (All Dimensions Shown in mm)

Symbols	Min.	Nom.	Max.
PKG CODE		WQFN(X648)	
Symbols	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		6.00 BSC	
E		6.00 BSC	
e		0.40 BSC	
K	0.20	-	-

PAD SIZE	D2			E2			L		
	Min.	Nom.	Max.	Min.	Nom.	Max.	Min.	Nom.	Max.
185X18*MIL	4.45	4.50	4.55	4.45	4.50	4.55	0.35	0.40	0.45

4/7/2017

Version 0.3