STM6600, STM6601

Smart push-button on/off controller with Smart Reset™ and power-on lockout

Datasheet - production data

TDFN12

Features

- Operating voltage 1.6 V to 5.5 V
- Low standby current of 0.6 µA
- Adjustable Smart Reset™ assertion delay time driven by external C_{SRD}
- Power-up duration determined primarily by push-button press (STM6600) or by fixed time period, t_{ON_BLANK} (STM6601)
- Debounced $\overline{PB}$ and $\overline{SR}$ inputs
- $\overline{PB}$ and $\overline{SR}$ ESD inputs withstand voltage up to ±15 kV (air discharge) ±8 kV (contact discharge)
- Active high or active low enable output option ($\overline{EN}$ or EN) provides control of MOSFET, DC-DC converter, regulator, etc.
- Secure startup, interrupt, Smart Reset™ or power-down driven by push-button
- Precise 1.5 V voltage reference with 1% accuracy
- Industrial operating temperature –40 to +85 °C
- Available in TDFN12 2 x 3 mm package

Applications

- Portable devices
- Terminals
- Audio and video players
- Cell phones and smart phones
- PDAs, palmtops, organizers

Table 1. Device summary

Device	$\overline{RST}$	C_{SRD}	$\overline{PB}$ / $\overline{SR}$	EN or $\overline{EN}$	$\overline{INT}$	Startup process
STM6600	open drain (1)	✓	✓	Push-pull	Open drain (1)	$\overline{PB}$ must be held low until the PS_{HOLD} (2) confirmation
STM6601	open drain (1)	✓	✓	Push-pull	Open drain (1)	PB can be released before the PS_{HOLD} (2) confirmation

1. External pull-up resistor needs to be connected to open drain outputs.
2. For a successful startup, the PS_{HOLD} (power supply hold) needs to be pulled high within specific time, t_{ON_BLANK}.

STM6600, STM6601

具备Smart Reset™和上电锁定功能的智能按键开关控制器

数据手册 -生产数据

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特性

- 工作电压范围1.6 V至5.5 V
- 低待机电流0.6 µA
- 由外部电容驱动的可调Smart Reset™断言延迟时间SRD
- 上电持续时间主要由按键按下时间决定（STM6600）或由固定时间t_{ON_BLANK}决定（STM6601）
- 按键和SR输入去抖动处理
- $\overline{PB}$和$\overline{SR}$ESD输入端可承受高达±15 kV（空气放电）和±8 kV（接触放电）的电压
- 支持高电平或低电平使能输出选项（EN或$\overline{EN}$）用于控制MOSFET，DC-DC转换器、稳压器等
- 通过按键实现安全启动、中断、Smart Reset™或断电控制
- 精确的1.5 V电压基准，精度为1%
- 工业级工作温度范围 –40 至 +85 °C
- 提供TDFN12 2 x 3 mm封装

应用

- 便携式设备
- 终端
- 音频和视频播放器
- 手机和智能手机
- PDA、掌上电脑、组织器

表1. 器件概要

器件	$\overline{RST}$	C_{SRD}	$\overline{PB}$ / $\overline{SR}$	使能（EN）或使能（$\overline{EN}$）	$\overline{中断}$	启动过程
STM6600	开漏 (1)	✓	✓	推挽	开漏 (1)	$\overline{PB}$必须保持低电平，直到$PS_{HOLD(2)}$确认
STM6601	开漏 (1)	✓	✓	推挽	开漏 (1)	PB可在$PS_{HOLD(2)}$确认之前释放

1. 开漏输出需外接上拉电阻。

2. 为确保成功启动，PS_{HOLD}（电源保持）需在特定时间t开机空白内被拉高。

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1 Description

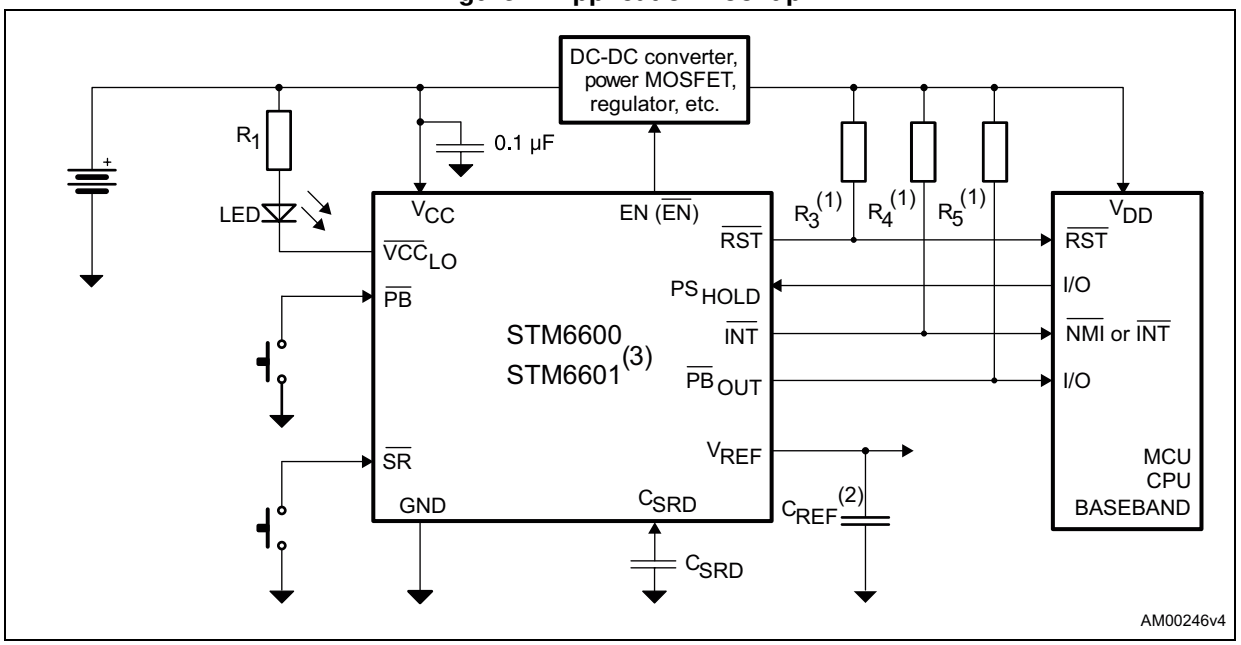
The STM6600-01 devices monitor the state of connected push-button(s) as well as sufficient supply voltage. An enable output controls power for the application through the MOSFET transistor, DC-DC converter, regulator, etc. If the supply voltage is above a precise voltage threshold, the enable output can be asserted by a simple press of the button. Factory-selectable supply voltage thresholds are determined by highly accurate and temperature-compensated references. An interrupt is asserted by pressing the push-button during normal operation and can be used to request a system power-down. The interrupt is also asserted if undervoltage is detected. By a long push of one button ($\overline{PB}$) or two buttons ($\overline{PB}$ and $\overline{SR}$) either a reset is asserted or power for the application is disabled depending on the option used.

The device also offers additional features such as precise 1.5 V voltage reference with very tight accuracy of 1%, separate output indicating undervoltage detection and separate output for distinguishing between interrupt by push-button or undervoltage.

The device consumes very low current of 6 µA during normal operation and only 0.6 µA current during standby.

The STM6600-01 is available in the TDFN12 package and is offered in several options among features such as selectable threshold, hysteresis, timeouts, output types, etc.

Figure 1. Application hookup



1. A resistor is required for open drain output type only. A 10 kΩ pull-up is sufficient in most applications.
2. Capacitor C_{REF} is mandatory on V_{REF} output (even if V_{REF} is not used). Capacitor value of 1 µF is recommended.
3. For the STM6601 the processor has to confirm the proper power-on during the fixed time period, t_{ON_BLANK}. This failsafe feature prevents the user from turning on the system when there is a faulty power switch or an unresponsive microprocessor.

1 描述

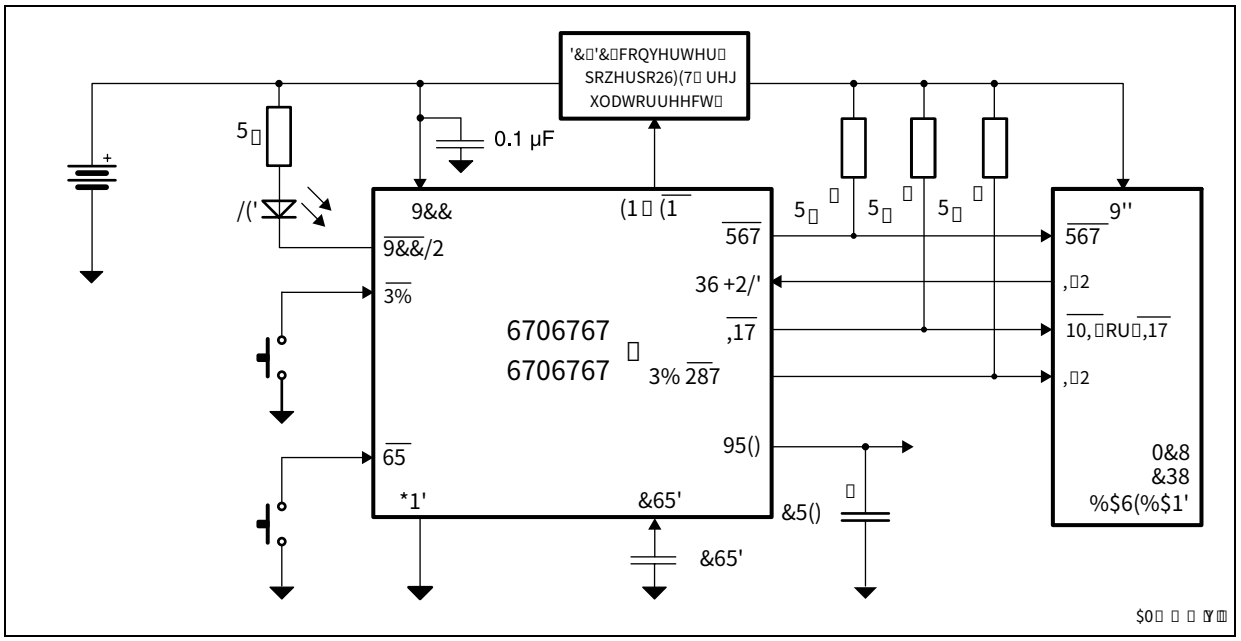
STM6600-01 器件监测连接的按键状态及供电电压是否充足。使能输出通过 MOSF ET 晶体管、DC-DC 转换器、稳压器等控制应用电源。当供电电压高于精确的电压阈值时，按键的简单按压即可使能输出被置位。工厂可选的供电电压阈值由高精度且温度补偿的基准电压确定。在正常操作期间按下按键会触发中断，该中断可用于请求系统断电。检测到欠压时也会触发中断。通过长按一个按键（PB）或两个按键（PB和SR），根据所选选项，可触发复位或关闭应用电源。

该器件还提供额外功能，如精确的1.5 V电压基准，精度高达1%，独立输出指示欠压检测，以及独立输出区分按键中断和欠压中断。

器件在正常工作时电流极低，仅为6 µA，待机时电流仅为0.6 µA。

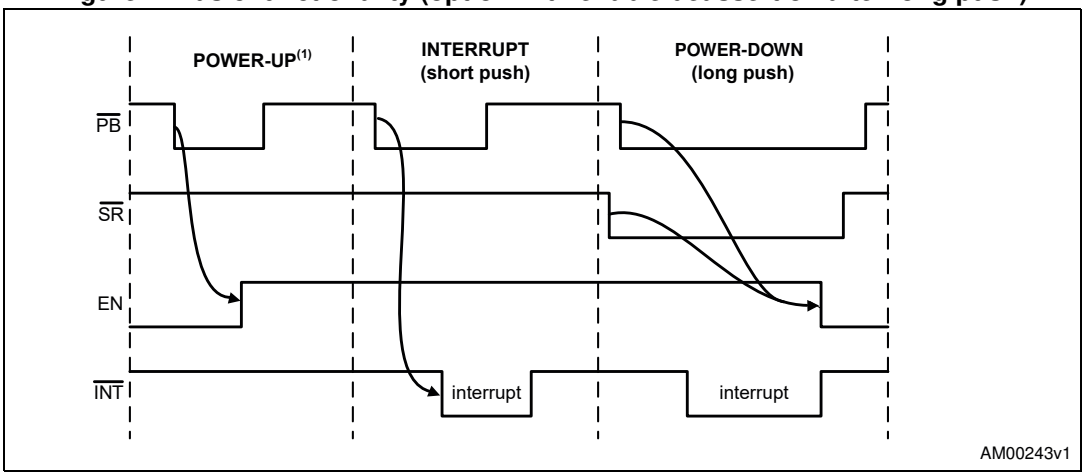
STM6600-01采用TDFN12封装，提供多种选项，包括可选阈值、迟滞、超时和输出类型等功能。

图1. 应用接线



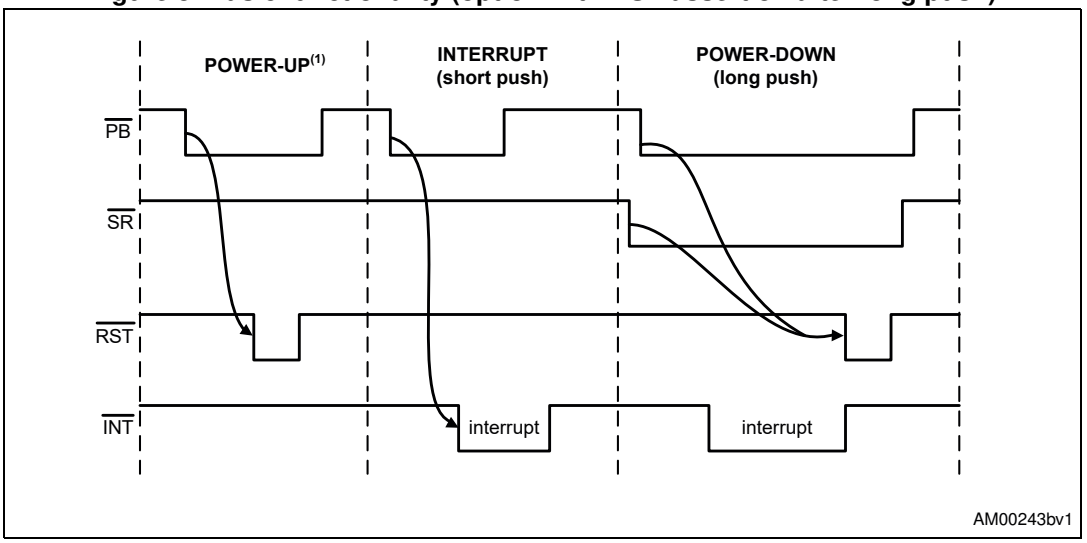
1. 仅开漏输出类型需要电阻。大多数应用中，10 kΩ上拉电阻足够。
2. V_{REF}输出端必须连接电容C_{REF}（即使不使用V_{REF}）。 建议电容值为1 µF。
3. 对于STM6601，处理器必须在固定时间段t_{ON_BLANK}内确认正确上电。此安全功能防止在电源开关故障或微处理器无响应时用户开启系统。

Figure 2. Basic functionality (option with enable deassertion after long push)



1. For power-up the battery voltage has to be above V_{TH+} threshold.

Figure 3. Basic functionality (option with $\overline{RST}$ assertion after long push)



1. For power-up the battery voltage has to be above V_{TH+} threshold.

Figure 4. Logic diagram

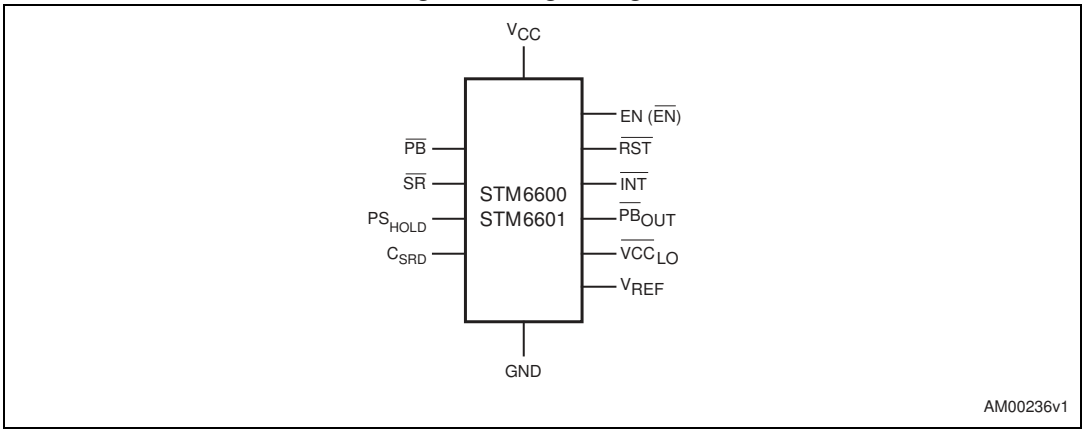
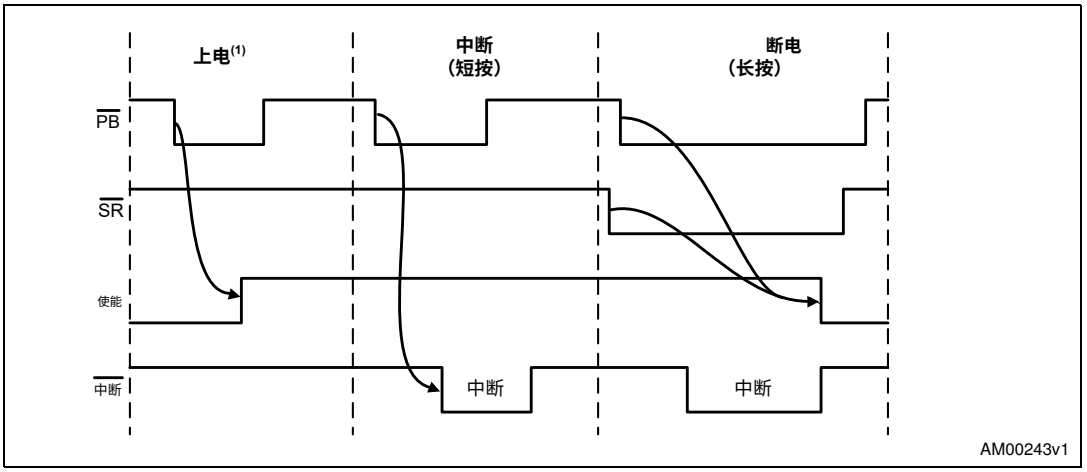
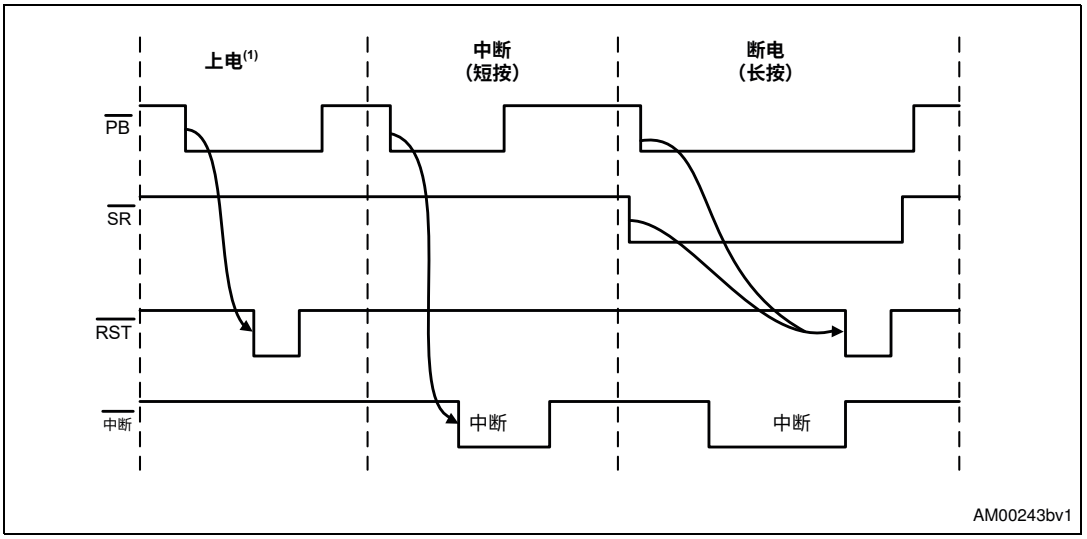


图 2. 基本功能（长按后使能取消选项）



1. 上电时电池电压必须高于V_{TH+}阈值。

图 3. 基本功能（长按后带$\overline{RST}$断言选项）



1. 上电时电池电压必须高于V_{TH+}阈值。

图4. 逻辑图

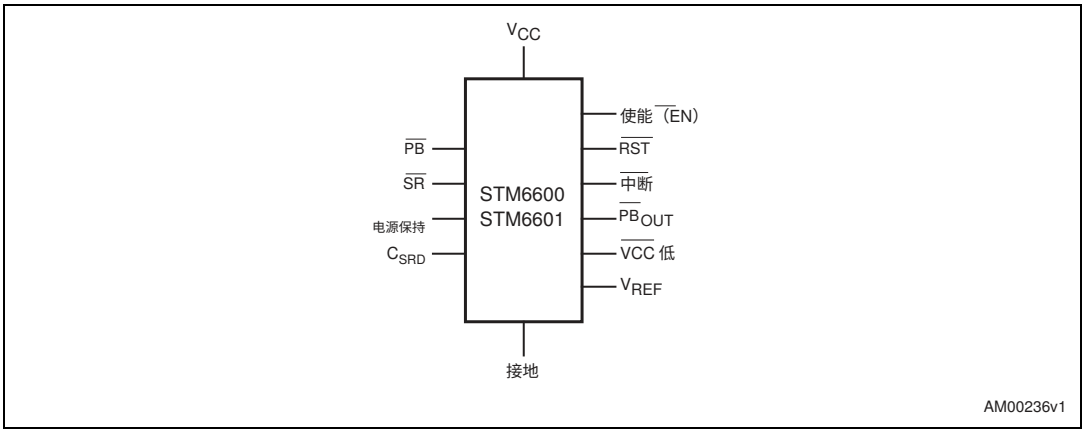


Table 2. Pin descriptions

Pin number	Symbol	Function
1	V_{CC}	Power supply input
2	$\overline{SR}$	Smart Reset™ button input
3	V_{REF}	Precise 1.5 V voltage reference
4	PS_{HOLD}	PS_{HOLD} input
5	C_{SRD}	Adjustable Smart Reset™ delay time input
6	$\overline{PB}$	Push-button input
7	$\overline{VCC}_{LO}$	Output for high threshold comparator output (V_{TH+})
8	PB_{OUT}	Status of $\overline{PB}$ push-button input
9	EN or $\overline{EN}$	Enable output
10	$\overline{RST}$	Reset output
11	$\overline{INT}$	Interrupt output
12	GND	Ground

Figure 5. TDFN12 pin connections

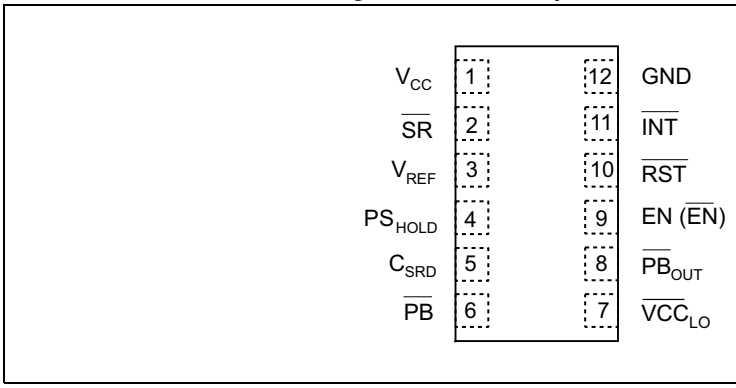


表2. 引脚描述

引脚编号	符号	功能
1	V_{CC}	电源输入
2	$\overline{SR}$	Smart Reset™ 按键输入
3	V_{REF}	精确1.5 V电压基准
4	电源保持	PS_{HOLD} 输入
5	C_{SRD}	可调Smart Reset™延时输入
6	$\overline{PB}$	按键输入
7	$\overline{VCC}_{LO}$	高阈值比较器输出（V_{TH+}）
8	PB_{OUT}	PB按键输入状态
9	使能（EN）或使能（EN）	使能输出
10	$\overline{RST}$	复位输出
11	中断	中断输出
12	接地	接地

图5. TDFN12封装引脚连接

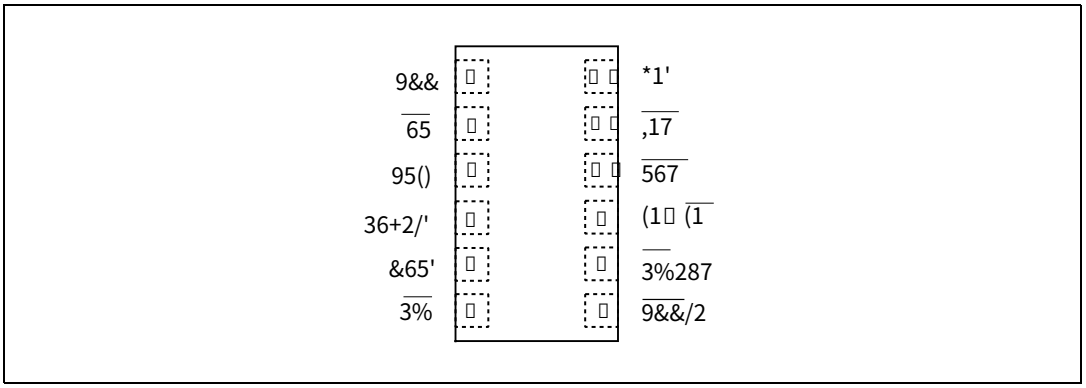
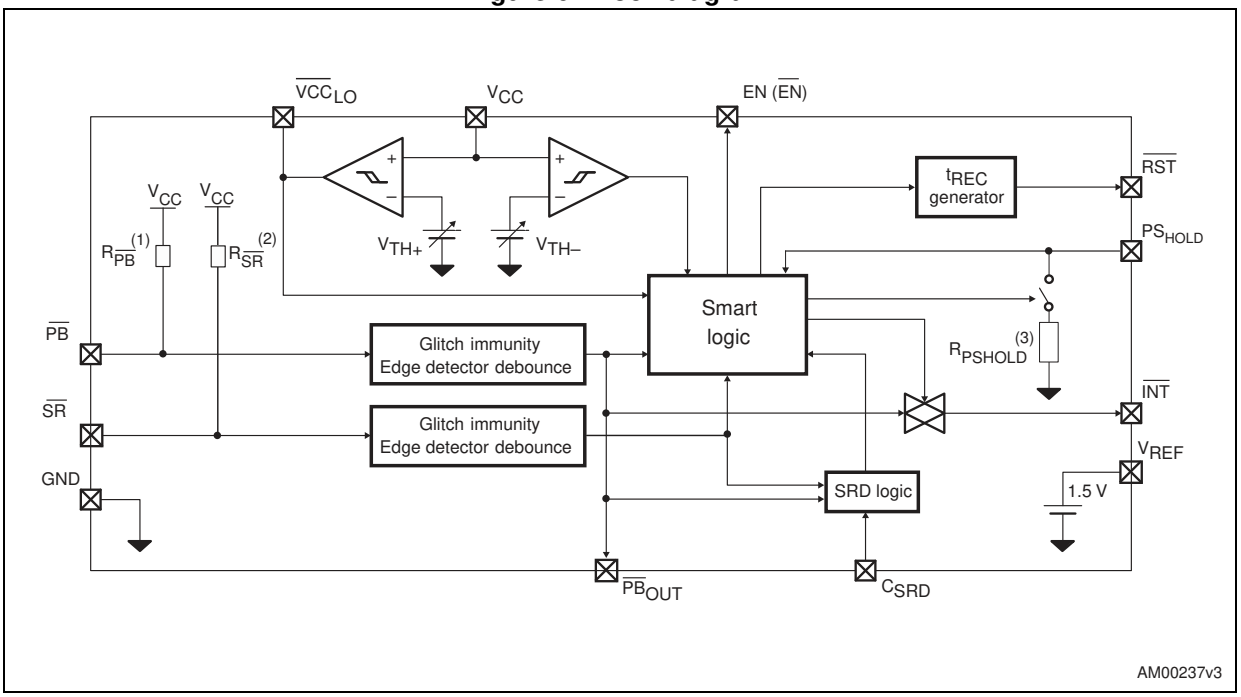
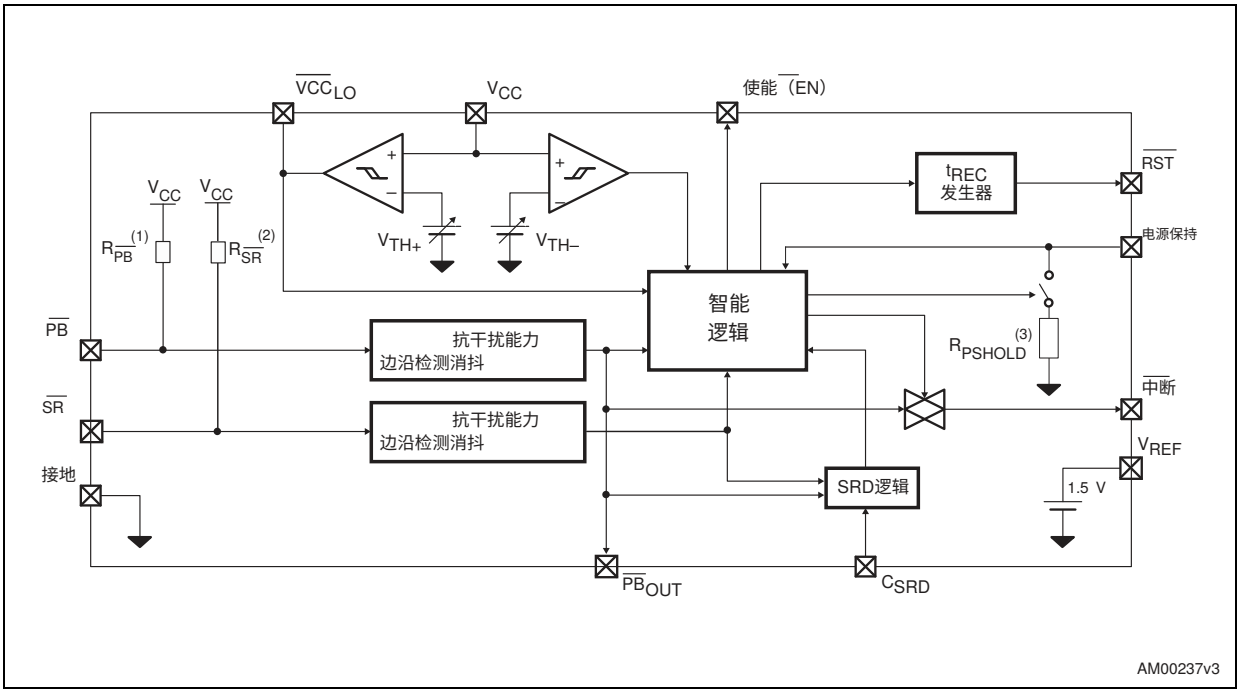


Figure 6. Block diagram



1. Internal pull-up resistor connected to $\overline{PB}$ input (see *Table 5* for precise specifications).
2. Optional internal pull-up resistor connected to $\overline{SR}$ input (see *Table 5* for precise specifications and *Table 10* for detailed device options).
3. Internal pull-down resistor is connected to PS_{HOLD} input only during startup (see *Figure 7*, *8*, *9*, *10*, *11*, *12*, *13*, and *18*).

图6. 框图



1. 内部上拉电阻连接至PB输入（详见表5具体规格）。
2. 可选内部上拉电阻连接至SR输入（详见表5具体规格及表10详细器件选项）。
3. 内部下拉电阻仅在启动期间连接至PS_{HOLD}输入（详见图7，8, 9, 10, 11, 12, 13，以及 18).

2 Pin descriptions

V_{CC} - power supply input

V_{CC} is monitored during startup and normal operation for sufficient voltage level. Decouple the V_{CC} pin from ground by placing a 0.1 µF capacitor as close to the device as possible.

$\overline{SR}$ - Smart Reset™ button input

This input is equipped with voltage detector with a factory-trimmed threshold and has ±8 kV HBM ESD protection.

Both $\overline{PB}$ and $\overline{SR}$ buttons have to be pressed and held for t_{SRD} period so the long push is recognized and the reset is asserted (or the enable output is deasserted depending on the option) - see *Figure 15*, *16*, and *17*.

Active low $\overline{SR}$ input is usually connected to GND through the momentary push-button (see *Figure 2*) and it has an optional 100 kΩ pull-up resistor. It is also possible to drive this input using an external device with either open drain (recommended) or push-pull output. Open drain output can be connected in parallel with push-button or other open drain outputs, which is not possible with push-pull output. $\overline{SR}$ input is monitored for falling edge after power-up and must not be grounded permanently.

V_{REF} - external precise 1.5 V voltage reference

This 1.5 V voltage reference is specified with very tight accuracy of 1% (see *Table 5*). It has proper output voltage as soon as the reset output is deasserted (i.e. after t_{REC} expires) and it is disabled when the device enters standby mode. A mandatory capacitor needs to be connected to V_{REF} output (even if V_{REF} is not used). Capacitor value of 1 µF is recommended.

PS_{HOLD} input

This input is equipped with a voltage detector with a factory-trimmed threshold. It is used to confirm correct power-up of the device (if EN or $\overline{EN}$ is not asserted) or to initiate a shutdown (if EN or $\overline{EN}$ is asserted).

Forcing PS_{HOLD} high during power-up confirms the proper start of the application and keeps enable output asserted. Because most processors have outputs in high-Z state before initialization, an internal pull-down resistor is connected to PS_{HOLD} input during startup (see *Figure 7*, *8*, *9*, *10*, *11*, *12*, *13*, and *18*).

Forcing the PS_{HOLD} signal low during normal operation deasserts the enable output (see *Figure 14*). Input voltage on this pin is compared to an accurate voltage reference.

C_{SRD} - Smart Reset™ delay time input

A capacitor to ground determines the additional time (t_{SRD}) that $\overline{PB}$ with $\overline{SR}$ must be pressed and held before a long push is recognized. The connected C_{SRD} capacitor is charged with I_{SRD} current. Additional Smart Reset™ delay time t_{SRD} ends when voltage on the C_{SRD} capacitor reaches the V_{SRD} voltage threshold. It is recommended to use a low ESR capacitor (e.g. ceramic). If the capacitor is not used, leave the C_{SRD} pin open. If no capacitor is connected, there is no t_{SRD} and a long push is recognized right after $t_{\overline{INT}\_Min}$ expires (see *Figure 18* and *19*).

2 引脚描述

V_{CC} - 电源输入

V_{CC}在启动和正常运行期间监测以确保电压水平充足。通过在器件附近尽可能靠近地放置一个0.1 µF电容，实现V_{CC}引脚的去耦。

$\overline{SR}$ - Smart Reset™ 按键输入

该输入配备有工厂校准阈值的电压检测器，并具备±8 kV HBM静电放电保护。

PB和$\overline{SR}$按键必须同时按下并保持t_{SRD}时间，以识别长按并触发复位（或根据选项取消使能输出）— 参见图*15*、*16*和*17*。

低电平有效的$\overline{SR}$输入通常通过瞬时按键连接至接地（见图*2*），并可选配100 kΩ上拉电阻。也可以使用外部器件驱动此输入，输出方式可以是开漏（推荐）或推挽输出。开漏输出可以与按键或其他开漏输出并联连接，而推挽输出则不支持此连接方式。SR 输入在上电后监测下降沿，且不得永久接地。

V_{REF} - 外部精密1.5 V电压基准

该1.5 V电压基准的精度非常高，误差仅为1%（见表*5*）。 复位输出取消断言（即t_{REC}到期后）时，电压基准即具有适当的输出电压；当器件进入待机模式时，该输出被禁用。必须在V_{REF}输出端连接一个电容（即使不使用V_{REF}）。 建议电容值为1 µF。

PS_{HOLD} 输入

该输入配备了具有出厂校准阈值的电压检测器。用于确认器件正确上电（当EN或EN未断言时）或启动关断（当EN或EN断言时）。

在上电期间强制将PS_{HOLD}置高，可确认应用程序的正确启动并保持使能输出有效。由于大多数处理器在初始化前输出处于高阻态，启动期间PS_{HOLD}输入端连接了内部下拉电阻（见图*7*）。

8, *9*, *10*, *11*, *12*, *13*，以及 *18*).

在正常操作期间强制将PS_{HOLD}信号置低，会使使能输出失效（见图*14*）。 该引脚的输入电压与精确的电压参考进行比较。

C_{SRD}- Smart Reset™延时输入

接地电容决定了带SR的PB必须按住的额外时间（t_{SRD}），以识别长按。连接的C_{SRD}电容由I_{SRD}电流充电。当CSRD电容上的电压达到V_{SRD}电压阈值时，额外的Smart Reset™延时t_{SRD}结束。建议使用低等效串联电阻（ESR）电容（例如陶瓷电容）。 如果不使用电容，请将C_{SRD}引脚悬空。如果未连接电容，则不存在tSRD，长按将在tINT_Min到期后立即被识别（参见图*18*和图*19*）。

$\overline{PB}$ - power ON switch

This input is equipped with a voltage detector with a factory-trimmed threshold and has ± 8 kV HBM ESD protection.

When the $\overline{PB}$ button is pressed and held, the battery voltage is detected and EN (or $\overline{EN}$) is asserted if the battery voltage is above the threshold V_{TH+} during the whole $t_{DEBOUNCE}$ period (see *Figure 13*).

A short push of the push-button during normal operation can initiate an interrupt through debounced $\overline{INT}$ output (see *Figure 14*) and a long push of $\overline{PB}$ and $\overline{SR}$ simultaneously can either assert reset output $\overline{RST}$ (see *Figure 18*) or deassert the EN or $\overline{EN}$ output (see *Figure 19*) based on the option used.

Note: A switch to GND must be connected to this input (e.g. mechanical push-button, open drain output of external circuitry, etc.), see Figure 2. This ensures a proper startup signal on $\overline{PB}$ (i.e. a transition from full V_{CC} below specified V_{IL}). $\overline{PB}$ input has an internal 100 kΩ pull-up resistor connected.

$\overline{VCC_{LO}}$ - high threshold detection output

During power-up, $\overline{VCC_{LO}}$ is low when V_{CC} supply voltage is below the V_{TH+} threshold. After successful power-up (i.e. during normal operation) $\overline{VCC_{LO}}$ is low anytime undervoltage is detected (see *Figure 13*).

Output type is active low and open drain by default. Open drain output type requires a pull-up resistor. A 10 kΩ is sufficient in most applications.

$\overline{VCC_{LO}}$ is floating when STM660x is in standby mode.

$\overline{PB_{OUT}}$ - $\overline{PB}$ input state

If the push-button $\overline{PB}$ is pressed, the pin stays low during the $t_{DEBOUNCE}$ time period. If $\overline{PB}$ is asserted for the entire $t_{DEBOUNCE}$ period, $\overline{PB_{OUT}}$ will then stay low for at least $t_{\overline{INT}\_Min}$. If $\overline{PB}$ is asserted after $t_{\overline{INT}\_Min}$ expires, $\overline{PB_{OUT}}$ will return high as soon as $\overline{PB}$ is deasserted (see *Figure 22*). $\overline{PB_{OUT}}$ ignores $\overline{PB}$ assertion during an undervoltage condition. At startup on the STM6601 $\overline{PB_{OUT}}$ will respond only to the first $\overline{PB}$ assertion and any other assertion will be ignored until t_{ON_BLANK} expires. This output is active low and open drain by default. Open drain output type requires a pull-up resistor. A 10 kΩ is sufficient in most applications.

$\overline{PB}$ - 上电开关

该输入配备了具有出厂校准阈值的电压检测器，并具备
±8 kV HBM 静电放电保护。

当按下并保持$\overline{PB}$按键时，如果电池电压在整个$t_{DEBOUNCE}$期间均高于阈值V_{TH+}，则检测到电池电压并使能输出EN（或$\overline{EN}$）被置位（参见图*13*）。

在正常操作期间，按键的短按可通过消抖后的中断输出$\overline{INT}$触发中断（参见图*14*）；而$\overline{PB}$和SR同时长按则可根据所选选项，触发复位输出$\overline{RST}$（参见图*18*）或取消使能输出EN或$\overline{EN}$（参见图*19*）。

注意： 必须将一个开关接地连接到此输入端（例如机械按键、外部电路的开漏输出等），见图*2*。这确保*PB*端有正确的启动信号（即从满V_{CC}转换到低于规定V_{IL}的状态）。*PB*输入端内部带有一个*100 k*Ω的上拉电阻。

$\overline{VCC}_{LO}$ - 高阈值检测输出

在上电过程中，当$\overline{VCC}$供电电压低于VTH+阈值时，$\overline{VCC}$LO为低电平。成功上电后（即正常工作期间），任何检测到欠压时，VCC_{LO}均为低电平（见图*13*）。

输出类型默认为低有效开漏。开漏输出类型需要外接上拉电阻。大多数应用中，10 kΩ的电阻足够。

当$\overline{STM660x}$处于待机模式时，VCC_{LO}处于悬空状态。

$\overline{PB}_{OUT}$ - $\overline{PB}$ 输入状态

如果按键 $\overline{PB}$ 被按下，针脚在 $t_{DEBOUNCE}$时间内保持低电平。
如果 $\overline{PB}$ 在整个 $t_{DEBOUNCE}$期间被断言，PB_{OUT}随后将至少保持低电平持续 t_{INT_Min}。
如果 $\overline{PB}$ 在 t_{INT_Min}到期后被断言，PB_{OUT}将在 $\overline{PB}$ 解除断言后立即返回高电平（见图 *22*）。PB_{OUT}在欠压条件下忽略 $\overline{PB}$ 的断言。
在 STM6601 启动时，PB_{OUT}仅响应第一次 $\overline{PB}$ 断言，其他断言将在 t_{ON_BLANK}到期前被忽略。该输出默认为低电平有效且开漏输出。开漏输出类型需要上拉电阻。大多数应用中，10 kΩ的电阻足够。

EN or $\overline{EN}$ - enable output

This output is intended to enable system power (see *Figure 2*). EN is asserted **high** after a valid turn-on event has been detected and confirmed (i.e. push-button has been pressed and held for $t_{DEBOUNCE}$ or more and $V_{CC} > V_{TH+}$ voltage level has been detected - see *Figure 13*). EN is released **low** if any of the conditions below occur:

a) the push-button is released before PS_{HOLD} is driven high (valid for STM6600, see *Figure 9*) or t_{ON_BLANK} expires before PS_{HOLD} is driven high during startup (valid for both STM6600 and STM6601, see *Figure 10* and *12*).

b) PS_{HOLD} is driven low during normal operation (see *Figure 14*).

c) an undervoltage condition is detected for more than $t_{SRD} + t_{\overline{INT}\_Min} + t_{DEBOUNCE}$ (see *Figure 21*).

d) a long push of the buttons is detected (only for the device with option “EN deasserted by long push” - see *Figure 19*) or PS_{HOLD} is not driven high during t_{ON_BLANK} after a long push of the buttons (only for the device with option “$\overline{RST}$ asserted by long push” - see *Figure 18*).

Described logic levels are inverted in case of $\overline{EN}$ output. Output type is push-pull by default.

$\overline{RST}$ - reset output

This output pulls low for t_{REC}:

a) during startup. $\overline{PB}$ has been pressed (falling edge on the $\overline{PB}$ detected) and held for at least $t_{DEBOUNCE}$ and $V_{CC} > V_{TH+}$ (see *Figure 7*, *8*, *9*, *10*, *11*, *12* and *13* for more details).

b) after long push detection (valid only for the device with option “$\overline{RST}$ asserted by long push”). $\overline{PB}$ has been pressed (falling edge on the $\overline{PB}$ detected) and held for more than $t_{DEBOUNCE} + t_{SRD}$ (additional Smart Reset™ delay time can be adjusted by the external capacitor C_{SRD}) - see *Figure 18*.

Output type is active low and open drain by default. Open drain output type requires a pull-up resistor. A 10 kΩ is sufficient in most applications.

$\overline{INT}$ - interrupt output

While the system is under normal operation (PS_{HOLD} is driven high, power for application is asserted), the $\overline{INT}$ is driven **low** if:

a) V_{CC} falls below V_{TH-} threshold (i.e. undervoltage is detected - see *Figure 20* and *21*).

b) the falling edge on the $\overline{PB}$ is detected and the push-button is held for $t_{DEBOUNCE}$ or more. $\overline{INT}$ is driven low after $t_{DEBOUNCE}$ and stays low as long as $\overline{PB}$ is held. The $\overline{INT}$ signal is held high during power-up.

The state of the $\overline{PB}_{OUT}$ output can be used to determine if the interrupt was caused by either the assertion of the $\overline{PB}$ input, or was due to the detection of an undervoltage condition on V_{CC}.

$\overline{INT}$ output is asserted low for at least $t_{\overline{INT}\_Min}$.

Output type is active low and open drain by default. Open drain output type requires a pull-up resistor. A 10 kΩ is sufficient in most applications.

GND - ground

EN 或 $\overline{EN}$ - 使能输出

该输出用于使能系统电源（见图 2）。 在检测并确认有效的开机事件后（即按键被按下并保持 tDEBOUNCE或更长时间且 V_{CC}> VTH+电压水平被检测到——见图 13），EN 被断言为高电平。当满足以下任一条件时，EN被释放为低电平：

a) 按键在PS_{HOLD}被拉高之前释放（仅适用于STM6600，见图9），或启动期间tON_BLANK到期前PSHOLD未被拉高（适用于STM6600和STM6601，见图10和图12）。

b) 正常操作期间PS_{HOLD}被拉低（见图14）。

c) 欠压状态持续时间超过t_{SRD}+ t_{INT_Min}+ $t_{DEBOUNCE}$（见图21）。

d) 检测到按键长按（仅适用于带“EN由长按释放”选项的器件，见图19），或按键长按后tON_BLANK期间PS_{HOLD}未被拉高（仅适用于带“RST由长按置位”选项的器件，见图18）。

当使能输出（EN输出）时，逻辑电平为反向。输出类型默认为推挽式。

$\overline{RST}$ - 复位输出

该输出在以下时间内拉低：t_{REC}：

a) 启动期间。检测到PB的下降沿且PB被按下并保持至少$t_{DEBOUNCE}$且V_{CC}> V_{TH+}（参见图7，8, 9, 10, 11, 12 及 13 用于更多细节）。

b) 长按检测后（仅适用于带有“长按触发复位”选项的器件）。检测到PB的下降沿且PB被按下并保持时间超过$t_{DEBOUNCE}$+ t_{SRD}（额外的Smart Reset™延迟时间可通过外部电容CSRD调整）—参见图18。

输出类型默认为低有效开漏。开漏输出类型需要外接上拉电阻。大多数应用中，10 kΩ的电阻足够。

$\overline{INT}$ - 中断输出

当系统处于正常工作状态（PS_{HOLD}被拉高，应用电源被断言）时，若满足以下条件，INT输出被拉低：

a) V_{CC}下降至 V_{TH-}阈值以下（即检测到欠压——参见图20和图21）。

b) 检测到按键的下降沿且按键保持时间达到 t消抖时间或更长。经过 t消抖时间后，INT 输出被拉低，并在按键保持按下期间保持低电平。上电期间，INT 信号保持高电平。

PB_{OUT}输出状态可用于判断中断是由 PB 输入断言引起，还是由 V_{CC}欠压检测引起。

$\overline{INT}$ 输出至少保持低电平时间为 t_{INT_Min}。

输出类型默认为低有效开漏。开漏输出类型需要外接上拉电阻。大多数应用中，10 kΩ的电阻足够。

GND - 接地

3 Operation

The STM6600-STM6601 simplified smart push-button on/off controller with Smart Reset™ and power-on lockout enables and disables power for the application depending on push-button states, signals from the processor, and battery voltage.

Power-on

Because most of the processors have outputs in high-Z state before initialization, an internal pull-down resistor is connected to PS_{HOLD} input during startup (see *Figure 7*, *8*, *9*, *10*, *11*, *12*, *13*, and *18*).
To power up the device the push-button $\overline{PB}$ has to be pressed for at least $t_{DEBOUNCE}$ and V_{CC} has to be above V_{TH+} for the whole $t_{DEBOUNCE}$ period. If the battery voltage drops below V_{TH+} during the $t_{DEBOUNCE}$, the counter is reset and starts to count again when $V_{CC} > V_{TH+}$ (see *Figure 13*). After $t_{DEBOUNCE}$ the enable signal is asserted (EN goes high, $\overline{EN}$ goes low), reset output $\overline{RST}$ is asserted for t_{REC} and then the startup routine is performed by the processor. During initialization, the processor sets the PS_{HOLD} signal high.

On the STM6600 the PS_{HOLD} signal has to be set high prior to push-button release and t_{ON_BLANK} expiration, otherwise the enable signal is deasserted (EN goes low, $\overline{EN}$ goes high) - see *Figure 7*, *8*, *9*, and *10*. The time up to push-button release represents the maximum time allowed for the system to power up and initialize the circuits driving the PS_{HOLD} input. If the PS_{HOLD} signal is low at push-button release, the enable output is deasserted immediately, thus turning off the system power. If t_{ON_BLANK} expires prior to push-button release, the PS_{HOLD} state is checked at its expiration. This safety feature disables the power and prevents discharging the battery if the push-button is stuck or it is held for an unreasonable period of time and the application is not responding (see *Figure 8* and *10*). $\overline{PB}$ status, $\overline{INT}$ status and V_{CC} undervoltage detection are not monitored until power-up is completed.

On the STM6601 the PS_{HOLD} signal has to be set high before t_{ON_BLANK} expires, otherwise the enable signal is deasserted - see *Figure 11* and *12*. In this case the t_{ON_BLANK} period is the maximum time allowed for the power switch and processor to perform the proper power-on. If the PS_{HOLD} signal is low at the end of the blanking period, the enable output is released immediately, thus turning off the system power. $\overline{PB}$ status, $\overline{INT}$ status and V_{CC} undervoltage detection are not monitored during the entire t_{ON_BLANK} period. This failsafe feature prevents the user from turning on the system when there is a faulty power switch or an unresponsive microprocessor.

Push-button interrupt

If the device works under normal operation (i.e. PS_{HOLD} is high) and the push-button $\overline{PB}$ is pressed for more than $t_{DEBOUNCE}$, a negative pulse with minimum $t_{\overline{INT}\_Min}$ width is generated on the $\overline{INT}$ output. By connecting $\overline{INT}$ to the processor interrupt input ($\overline{INT}$ or $\overline{NMI}$) a safeguard routine can be performed and the power can be shut down by setting PS_{HOLD} low - see *Figure 14*.

Forced power-down mode

The PS_{HOLD} output can be forced low anytime during normal operation by the processor and can deassert the enable signal - see *Figure 14*.

3 操作

STM6600-STM6601 简化型智能按键开关控制器，具备 Smart Reset™ 和上电锁定功能，根据按键状态、处理器信号及电池电压控制应用电源的开启与关闭。

上电

由于大多数处理器在初始化之前输出处于高阻态，启动期间在PS_{HOLD}输入端连接了内部下拉电阻（参见图7、8、9、10、11、12、13和18）。

要使设备上电，必须按下按键PB至少持续t消抖期，且V_{CC}在整个t消抖期内必须高于VTH+。如果电池电压在t消抖期内降至低于VTH+，计数器将被复位，并在V

V_{TH+}（参见图13）。经过t消抖期后，使能信号被置位（$_{EN}$变高，$_{EN}$变低），复位输出$_{CC}$ > RST被断言持续tREC，随后处理器执行启动程序。在初始化过程中，处理器将PSH_OL_D信号置高。

在STM6600上，PS_{HOLD}信号必须在按键释放和t开机空白时间到期之前置高，否则使能信号将被取消（EN变低，EN变高）——参见图7、图8、图9和图10。按键释放之前的时间表示系统允许上电并初始化驱动PS_{HOLD}输入电路的最长时间。如果按键释放时PS_{HO} $_{LD}$信号为低电平，使能输出将立即被取消，从而关闭系统电源。如果t开机空白在按键释放之前到期，将在其到期时检查PS_{HOLD}状态。该安全功能在按键卡住或长时间按住且应用无响应时禁用电源，防止电池放电（参见图8和图10）。按键状态、中断状态和V_C $_C$欠压检测在上电完成之前不被监测。

在STM6601中，PS_{HOLD}信号必须在t_{ON_BLANK}到期之前置高，否则使能信号将被取消——参见图11和图12。在此情况下，t_{ON_BLANK}周期是电源开关和处理器完成正确上电的最长允许时间。如果PS_{HOLD}信号在消隐期结束时为低电平，使能输出将立即释放，从而关闭系统电源。按键状态、中断状态和V_{CC}欠压检测在整个tON_BLANK周期内均不被监测。此安全功能防止在电源开关故障或微处理器无响应时用户开启系统。

按键中断

如果设备在正常工作状态下（即PS_{HOLD}为高电平）且按键PB被按下时间超过$t_{DEBOUNCE}$，则在INT输出端会产生一个宽度不小于t_{INT_Min}的负脉冲。通过将INT连接到处理器中断输入（INT或NMI），可以执行保护程序，并通过将PS_{HOLD}置低来关闭电源——参见图14。

强制断电模式

处理器可以在正常操作期间随时强制将PS_{HOLD}输出置低，从而取消使能信号——参见图14。

Undervoltage detection

If V_{CC} voltage drops below V_{TH-} voltage threshold during normal operation, the $\overline{INT}$ output is driven low (see *Figure 20* and *Figure 21*).

If an undervoltage condition is detected for $t_{DEBOUNCE} + t_{\overline{INT}\_Min} + t_{SRD}$, the enable output is deasserted (see *Figure 21*).

Hardware reset or power-down while system not responding

If the system is not responding and the system hangs, the $\overline{PB}$ and $\overline{SR}$ push-buttons can be pressed simultaneously longer than $t_{DEBOUNCE} + t_{\overline{INT}\_Min} + t_{SRD}$, and then

a) either the reset output $\overline{RST}$ is asserted for t_{REC} and the processor is reset (valid only for the device with option “$\overline{RST}$ asserted by long push”) – see *Figure 18*

b) or the power is disabled by EN or $\overline{EN}$ signal (valid only for the device with option “EN deasserted by long push”) – see *Figure 19*

The t_{SRD} is set by the external capacitor connected to the C_{SRD} pin. $\overline{SR}$ input is monitored for falling edge after power-up and must not be grounded permanently.

Standby

If the enable output is deasserted (i.e. EN is low or $\overline{EN}$ is high), the STM660x device enters standby mode with low current consumption (see *Table 5*). In standby mode $\overline{PB}$ input is only monitored for the falling edge. The external 1.5 V voltage reference is also disabled in standby mode.

欠压检测

如果V_{CC}电压在正常操作期间降至低于V_{TH-}电压阈值，INT输出将被拉低（参见图*20*和图*21*）。

如果欠压状态持续时间达到$t_{DEBOUNCE}$+ t_{INT_Min}+ t_{SRD}，启用输出将被取消（参见图*21*）。

系统无响应时的硬件复位或断电

如果系统无响应且挂起，PB和SR按键可同时按下超过$t_{DEBOUNCE}$+ t_{INT_Min}+ t_{SRD}，然后

a) 复位输出 RST 被断言持续时间为 tREC，且处理器被复位（仅适用于带有“长按断言 RST”选项的器件）– 见图 *18*

b) 或电源被 EN 或 EN 信号禁用（仅适用于带有“长按取消断言 EN”选项的器件）– 见图 *19*

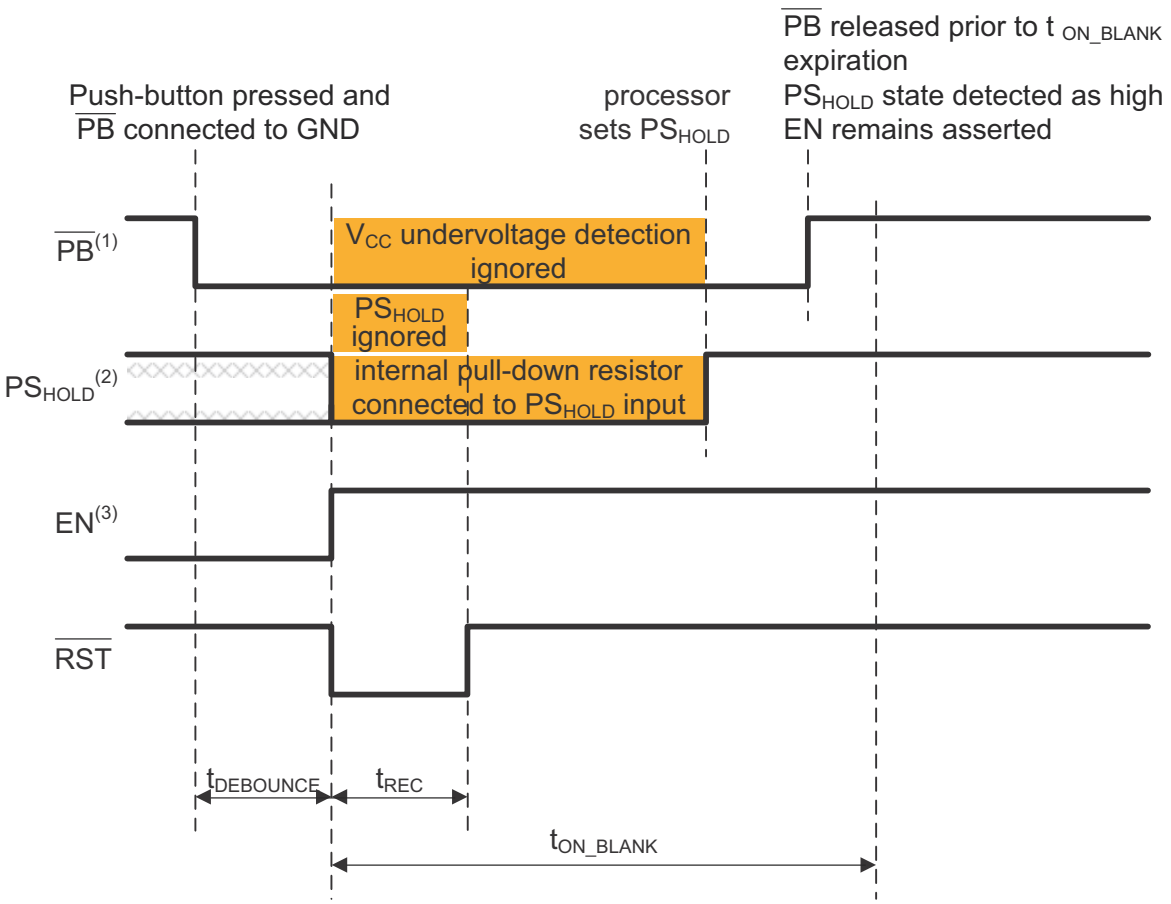
t_{SRD} 由连接至 C_{SRD} 引脚的外部电容设定。$_{SR}$ 输入在上电后监测下降沿，且不得永久接地。

待机模式

如果使能输出被取消断言（即 EN 为低或 EN 为高），STM660x 器件进入低电流消耗的待机模式（见表 *5*）。 在待机模式下，PB 输入仅监测下降沿。外部 1.*5* V 电压基准在待机模式下也被禁用。

4 Waveforms

Figure 7. Successful power-up on STM6600 ($\overline{PB}$ released prior to t_{ON_BLANK} expiration)



Note: $\overline{INT}$ signal is held high during power-up (i.e. until $\overline{PB}$ release in this case).

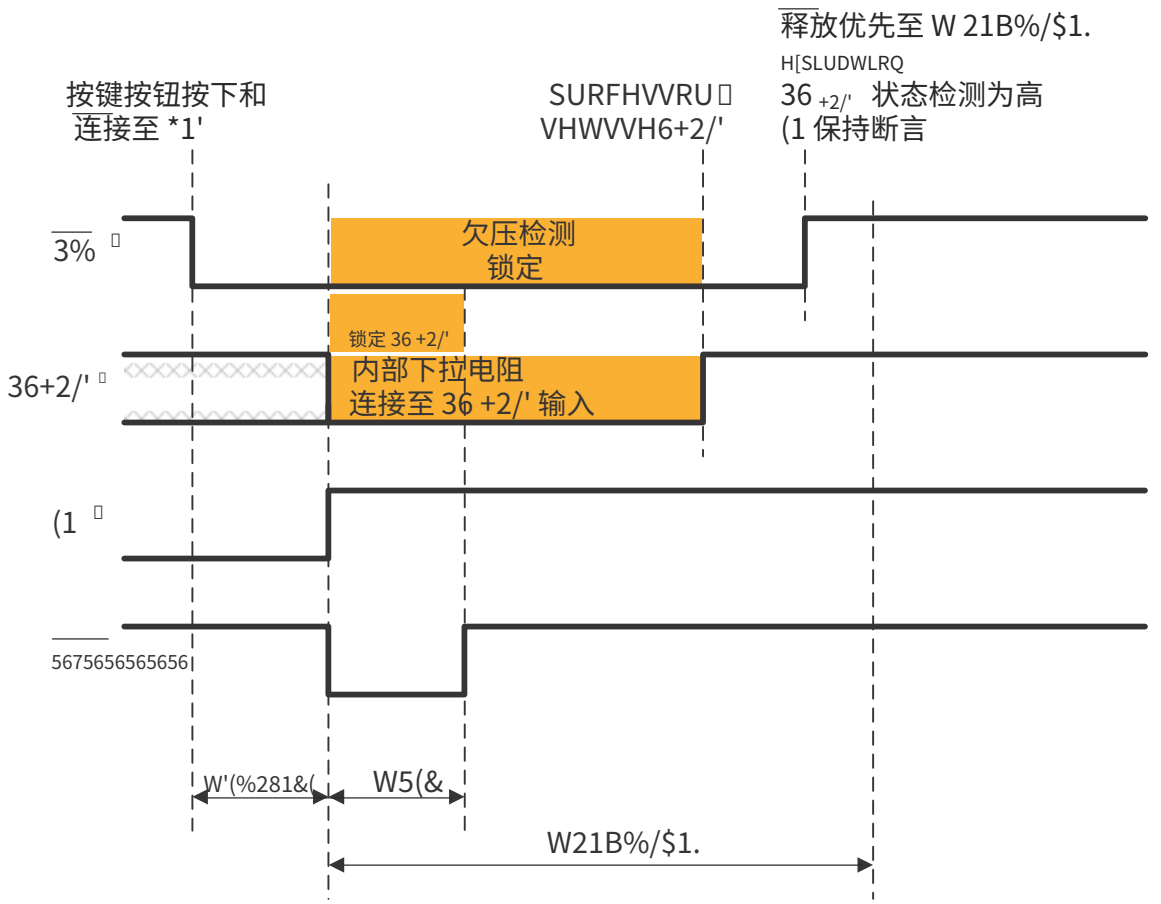
V_{CC} is considered $V_{CC} > V_{TH+}$.

AM00247v3

1. $\overline{PB}$ detection on falling and rising edges.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. EN signal is high even after $\overline{PB}$ release, because processor sets PS_{HOLD} signal high before $\overline{PB}$ is released.

4 波形

图 7. STM6600 成功上电（PB 在 t开机空白 到期前释放）

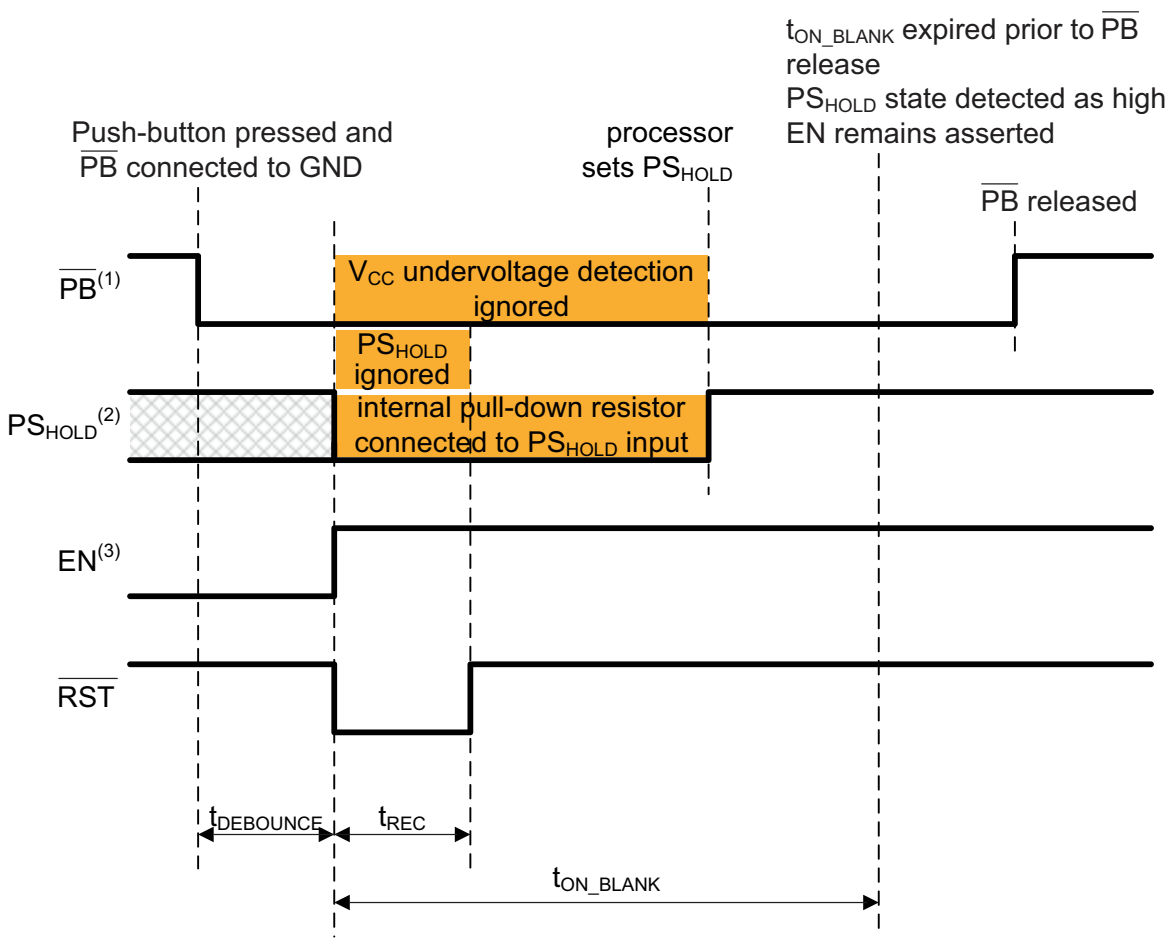


注意 ,17 信号在上电期间保持高，关闭直到在此情况下释放

9 && 被认为为39 && !39 7+

1. 按键检测在下降沿和上升沿。
2. 上电期间，内部下拉电阻300 kΩ连接至PS HOLD输入端。
3. 使能信号在按键释放后仍为高电平，因为处理器在按键释放前将PS HOLD信号置高。

Figure 8. Successful power-up on STM6600 (t_{ON_BLANK} expires prior to $\overline{PB}$ release)

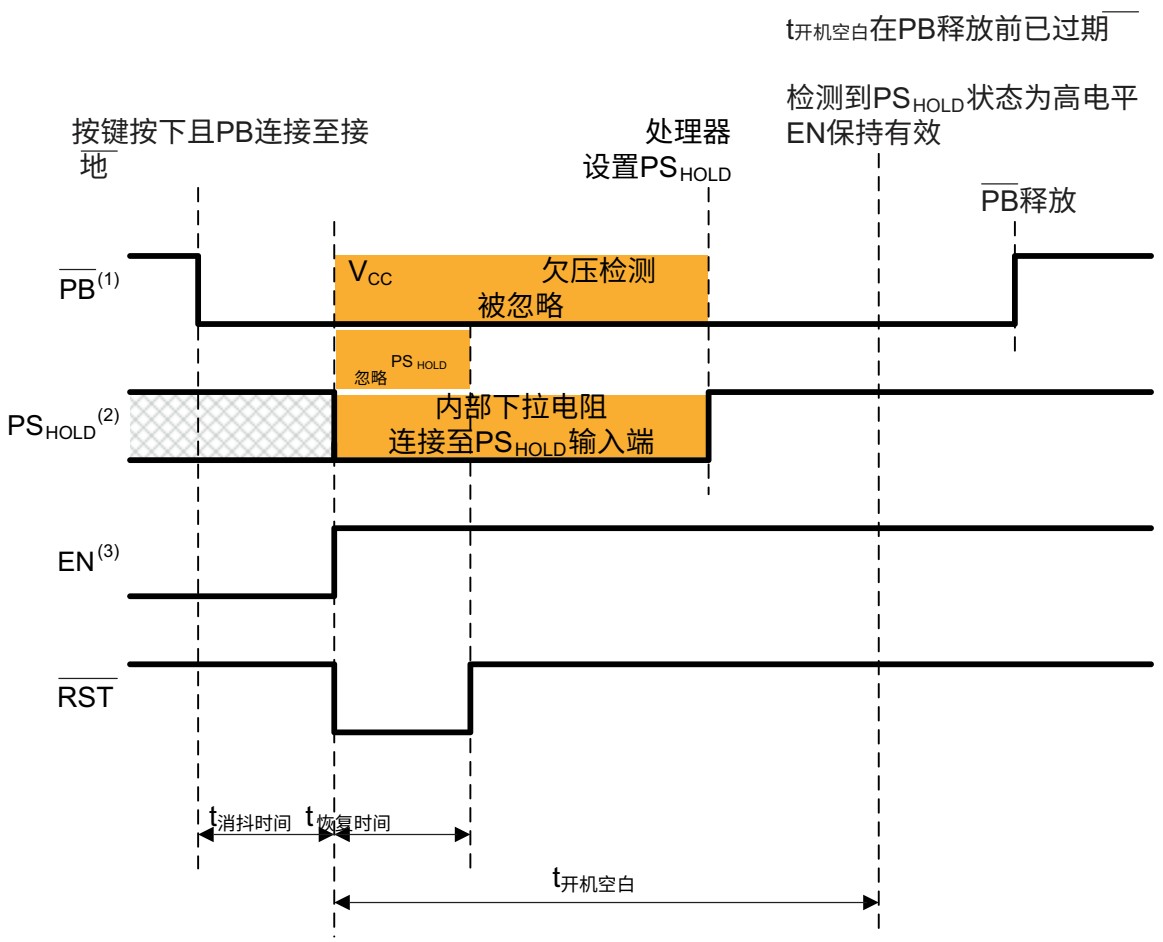


Note: $\overline{INT}$ signal is held high during power-up (i.e. until t_{ON_BLANK} expires in this case).
V_{CC} is considered $V_{CC} > V_{TH+}$.

AM00247bv2

1. $\overline{PB}$ detection on falling and rising edges.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. t_{ON_BLANK} expires prior to $\overline{PB}$ release so PS_{HOLD} is checked at its expiration.

图8。 STM6600 上电成功（开机空白在按键释放前到期）

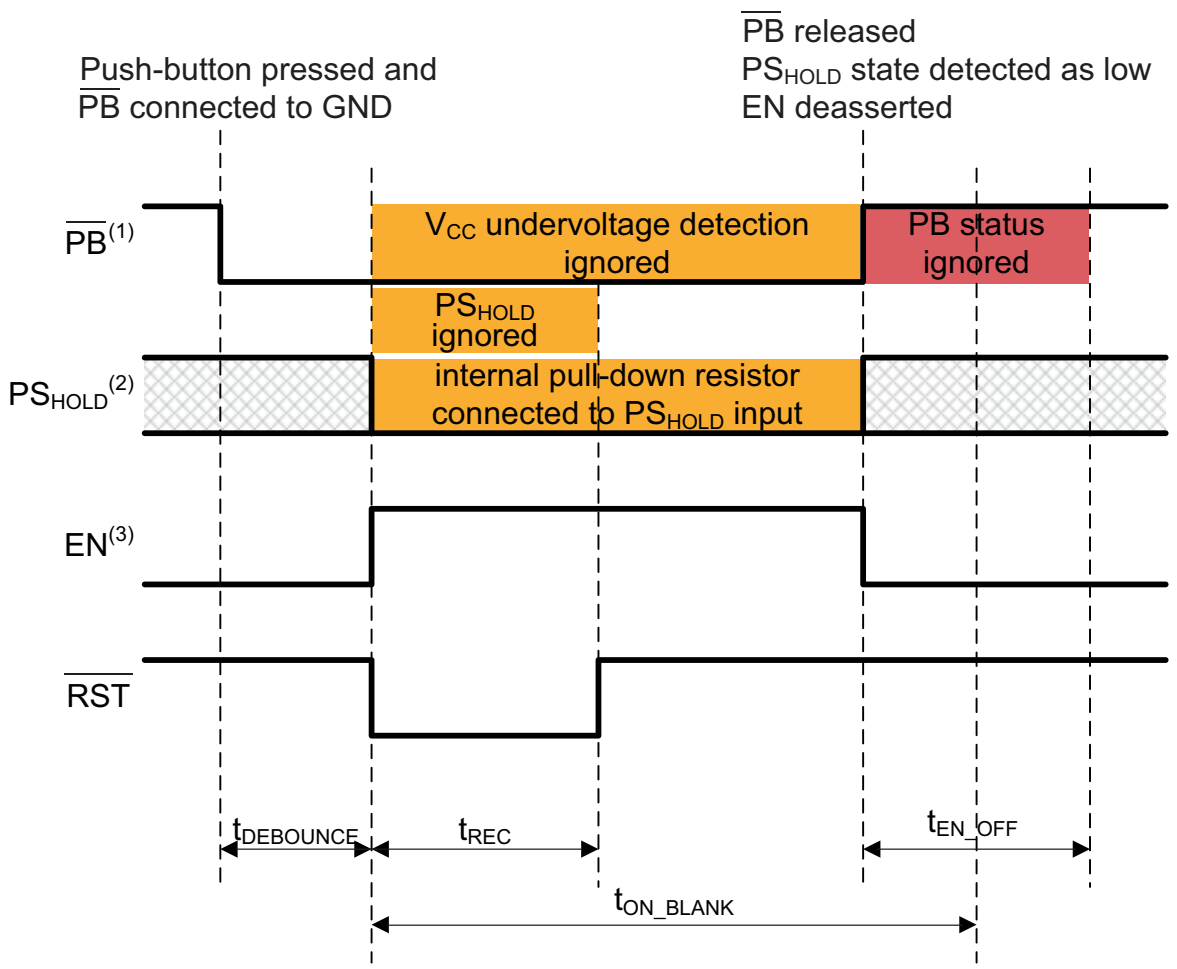


注意： 中断信号在上电期间保持高电平（即在本例中直到t开机空白过期）。
V_{CC} 被视为V_{CC}> V_{TH+}。

AM00247bv2

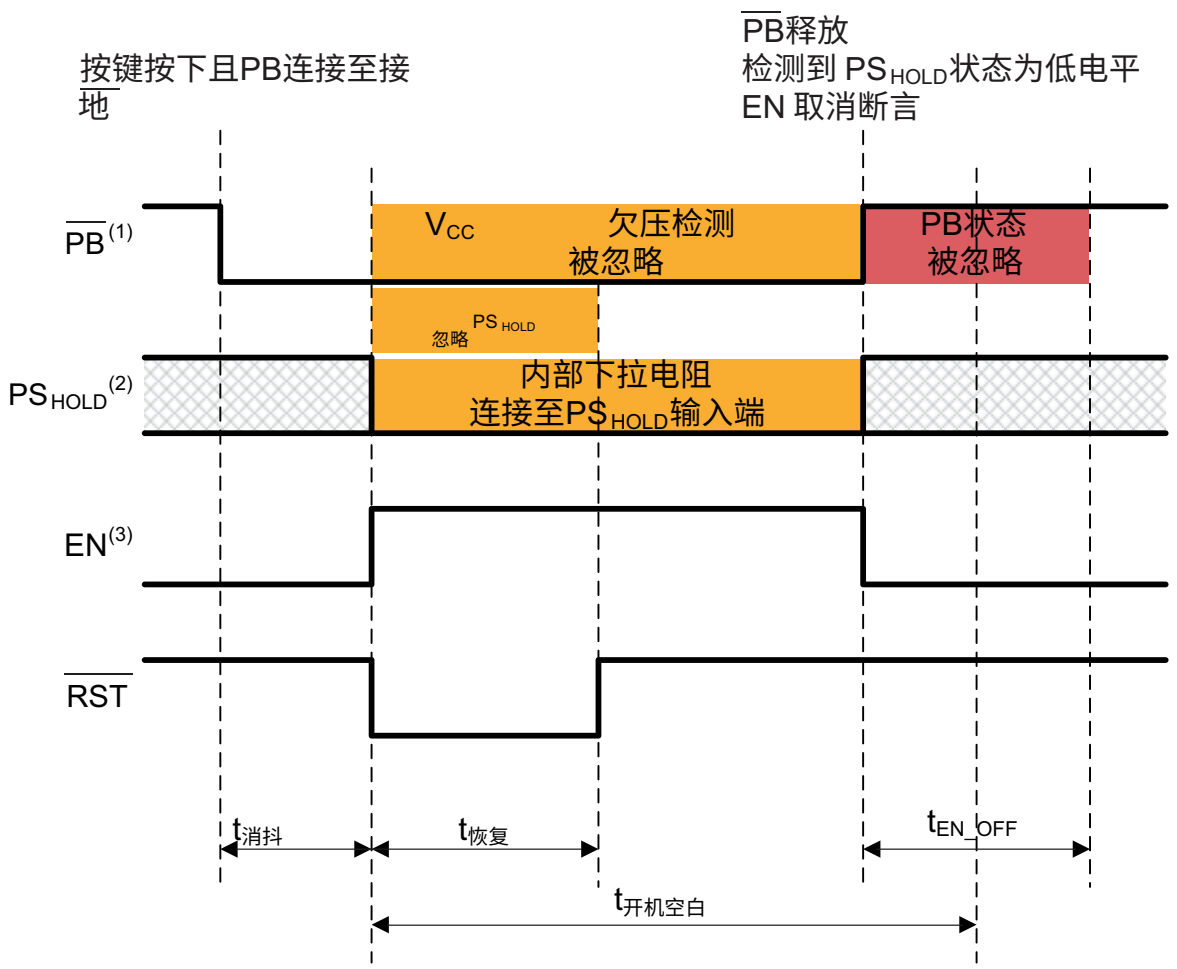
1. 按键检测在下降沿和上升沿。
2. 上电期间，内部下拉电阻300 kΩ连接至PS HOLD输入端。
3. 开机空白在按键释放前到期，因此在其到期时检查 PS HOLD。

Figure 9. Unsuccessful power-up on STM6600 ($\overline{PB}$ released prior to t_{ON_BLANK})



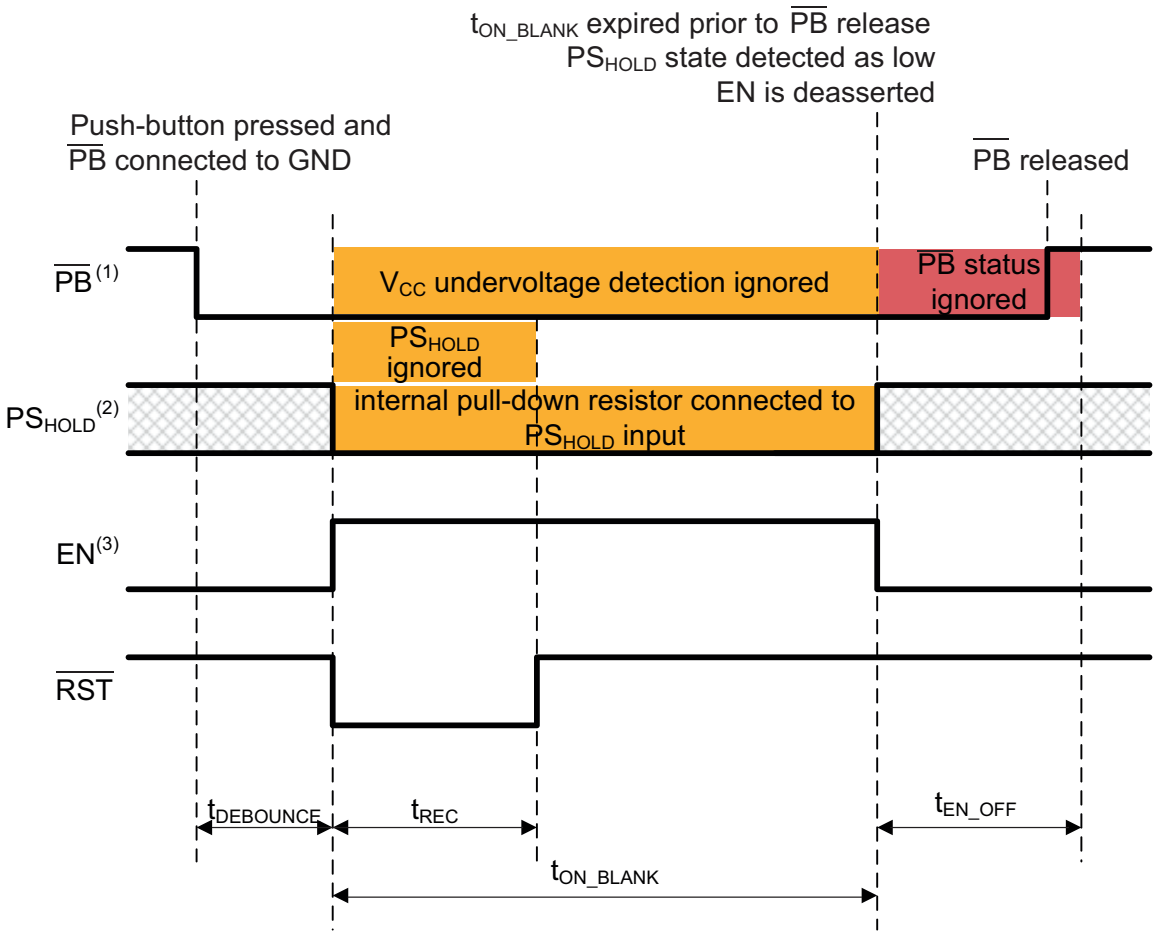
1. $\overline{PB}$ detection on falling and rising edges.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. EN signal goes low with $\overline{PB}$ release, because processor did not force PS_{HOLD} signal high.

图9。 STM6600上电失败（PB在t开机空白之前释放）



1. 按键检测在下降沿和上升沿。
2. 上电期间，内部下拉电阻300 kΩ连接至PS HOLD输入端。
3. PB释放时EN信号变低，因为处理器未将PSHOLD信号强制为高电平。

Figure 10. Unsuccessful power-up on STM6600 (t_{ON_BLANK} expires prior to $\overline{PB}$ release)

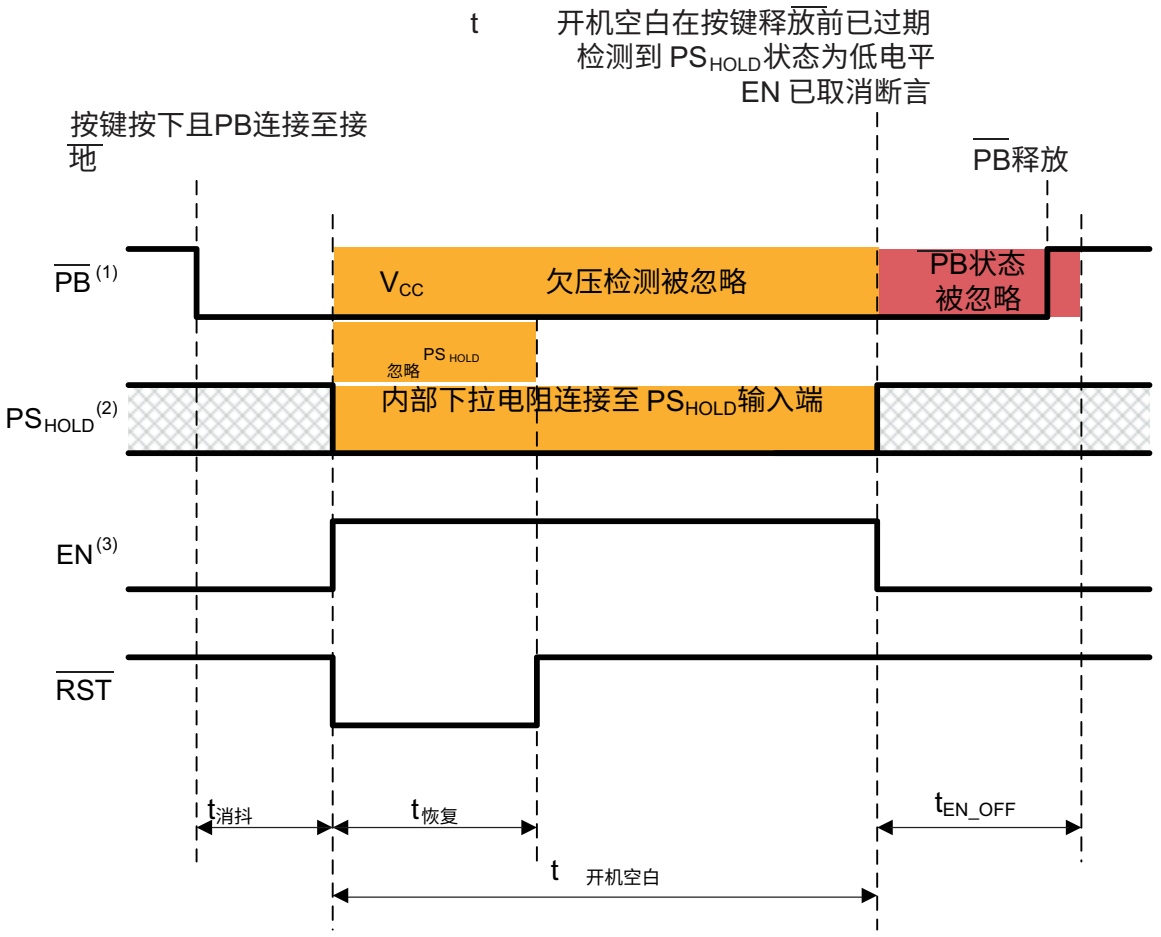


Note: $\overline{INT}$ signal is held high during power-up (i.e. until t_{ON_BLANK} expires in this case).
V_{CC} is considered $V_{CC} > V_{TH+}$.

AM00248bv2

1. $\overline{PB}$ detection on falling and rising edges.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. t_{ON_BLANK} expires prior to $\overline{PB}$ release so PS_{HOLD} is checked at its expiration.

图10。 STM6600 上电失败（$t_{ON\ BLANK}$到期早于 PB 释放）

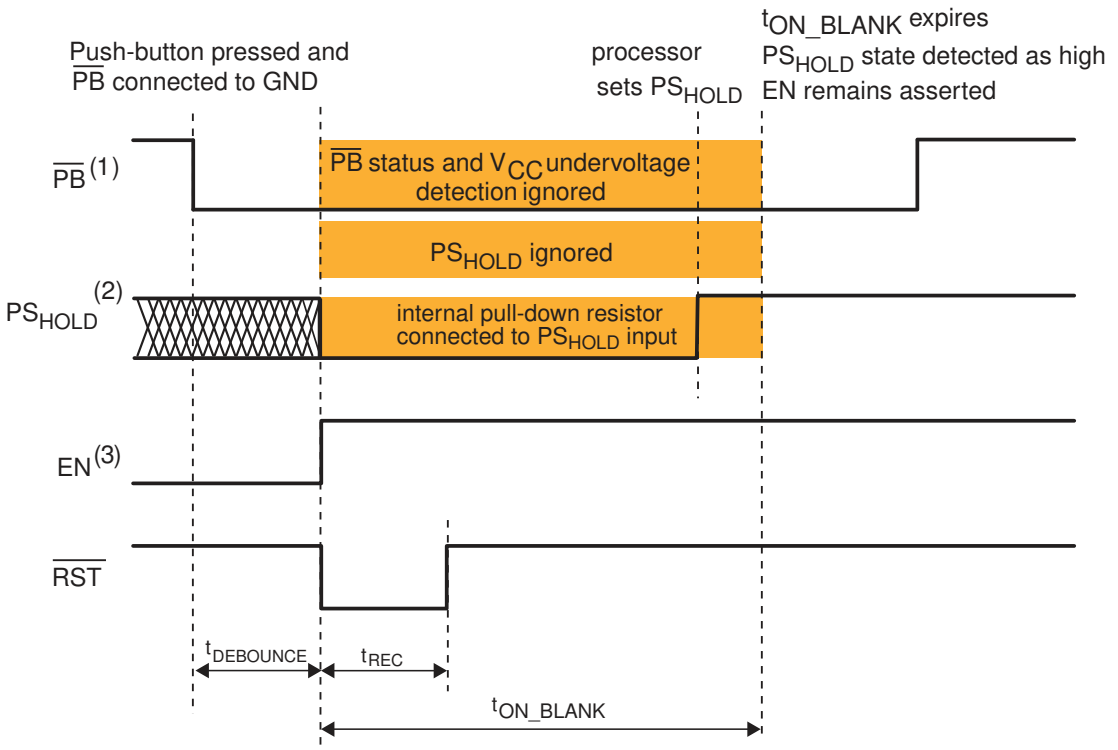


注意： 中断信号在上电期间保持高电平（即在本例中直到t开机空白过期）。
V_{CC} 被视为V_{CC}> V_{TH+}。

AM00248bv2

1. 按键检测在下降沿和上升沿。
2. 上电期间，内部下拉电阻300 kΩ连接至PS_{HOLD}输入端。
3. 开机空白在按键释放前到期，因此在其到期时检查 PS_{HOLD}。

Figure 11. Successful power-up on STM6601

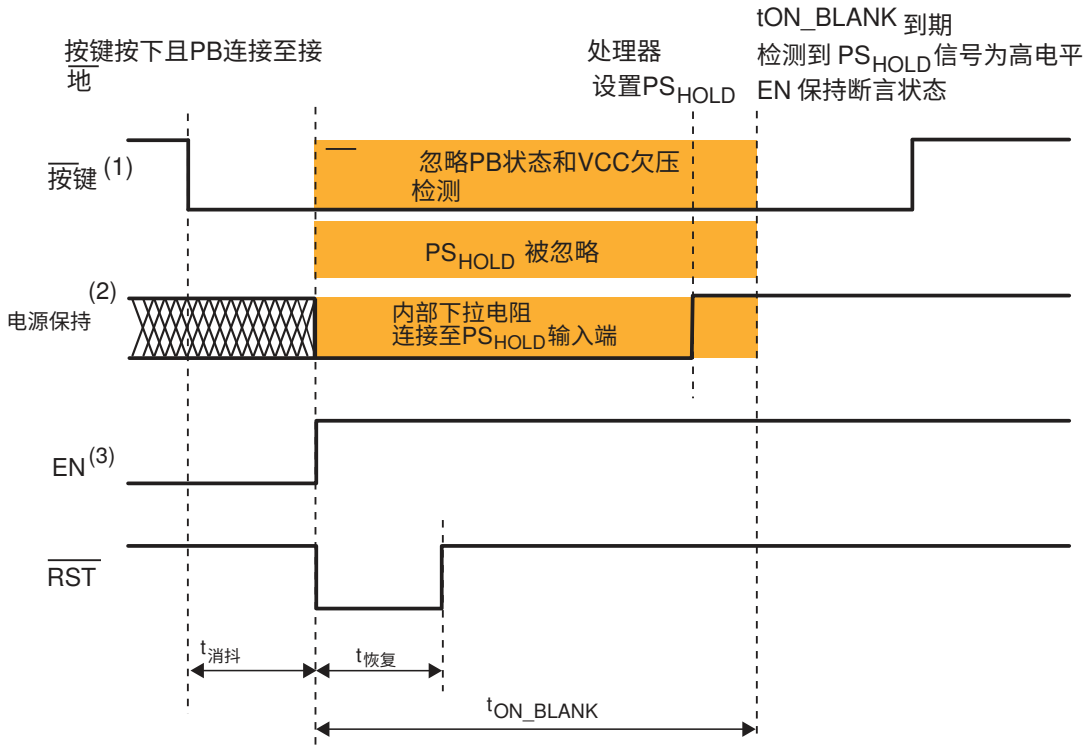


Note: INT signal is held high during power-up (i.e. until t_{ON_BLANK} expires in the case of the STM6601). V_{CC} is considered $V_{CC} > V_{TH+}$.

AM00250v2

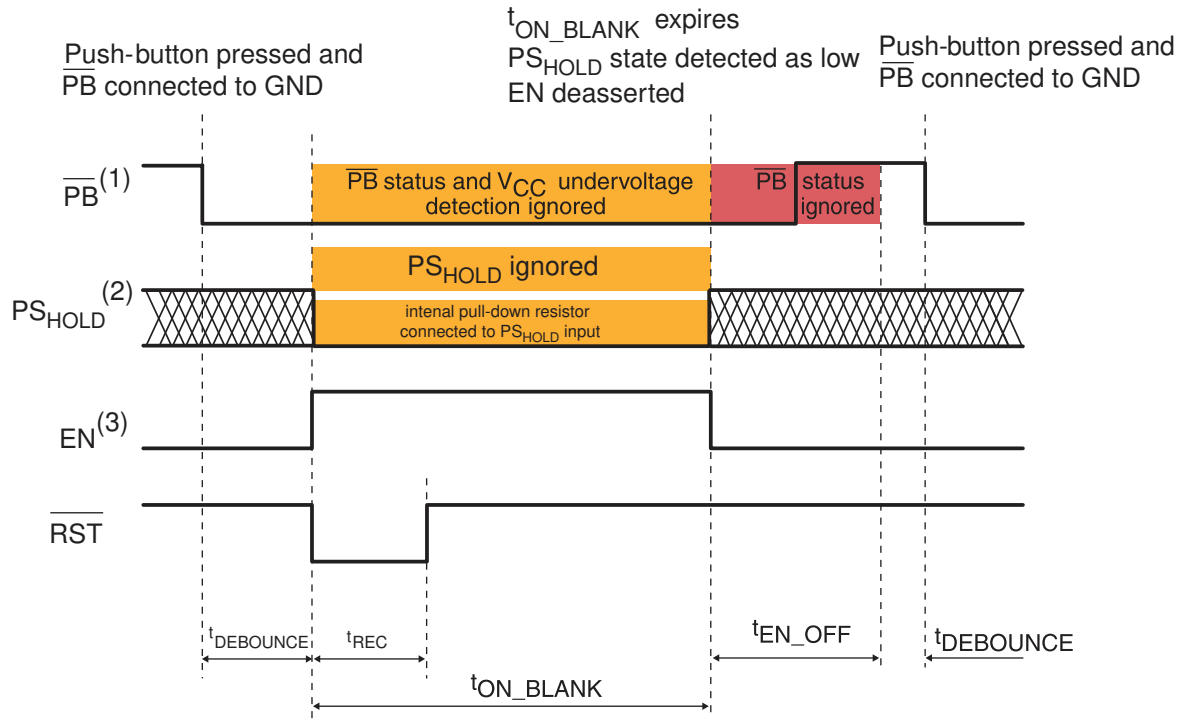
1. $\overline{PB}$ detection on falling edge.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. PS_{HOLD} signal is ignored during t_{ON_BLANK}. When t_{ON_BLANK} expires, the level of the PS_{HOLD} signal is high therefore the EN signal remains asserted.

图11。 STM6601 上电成功



1. 按键检测在下降沿触发。
2. 上电期间，内部下拉电阻300 kΩ连接至PS HOLD输入端。
3. t开机空白期间忽略 PSHOLD信号。当 t开机空白过期时，PSHOLD信号为高电平，因此 EN 信号保持断言。

Figure 12. Unsuccessful power-up on STM6601

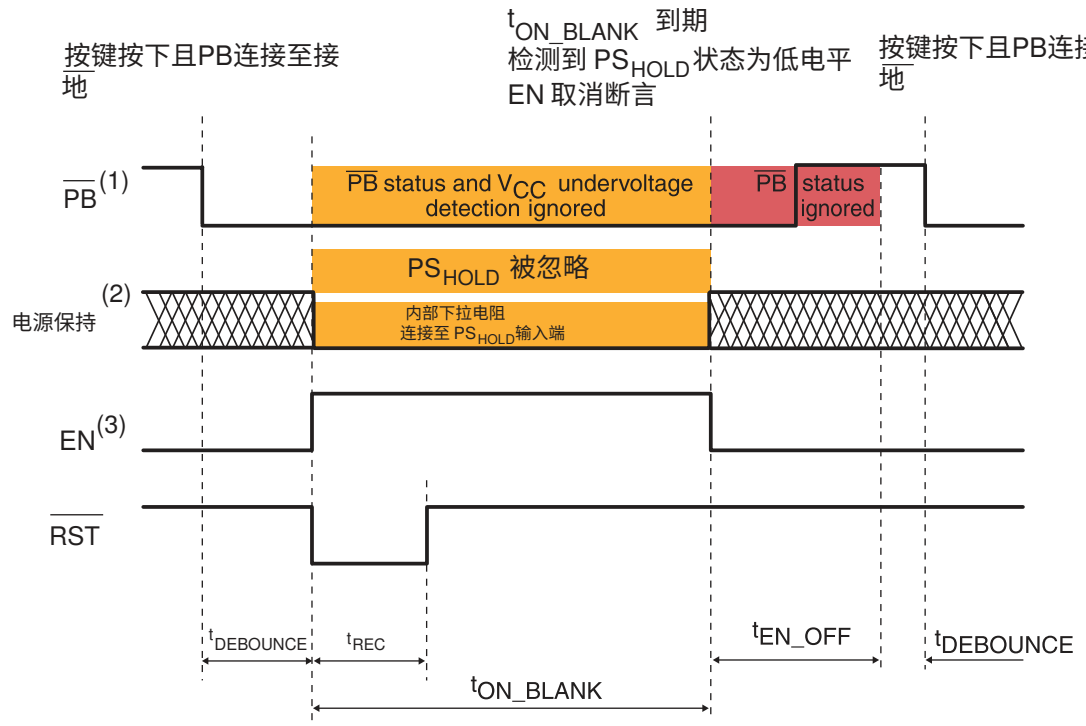


Note: INT signal is held high during power-up (i.e. until t_{ON_BLANK} expires in the case of the STM6601).
V_{CC} is considered $V_{CC} > V_{TH+}$.

AM00238v2

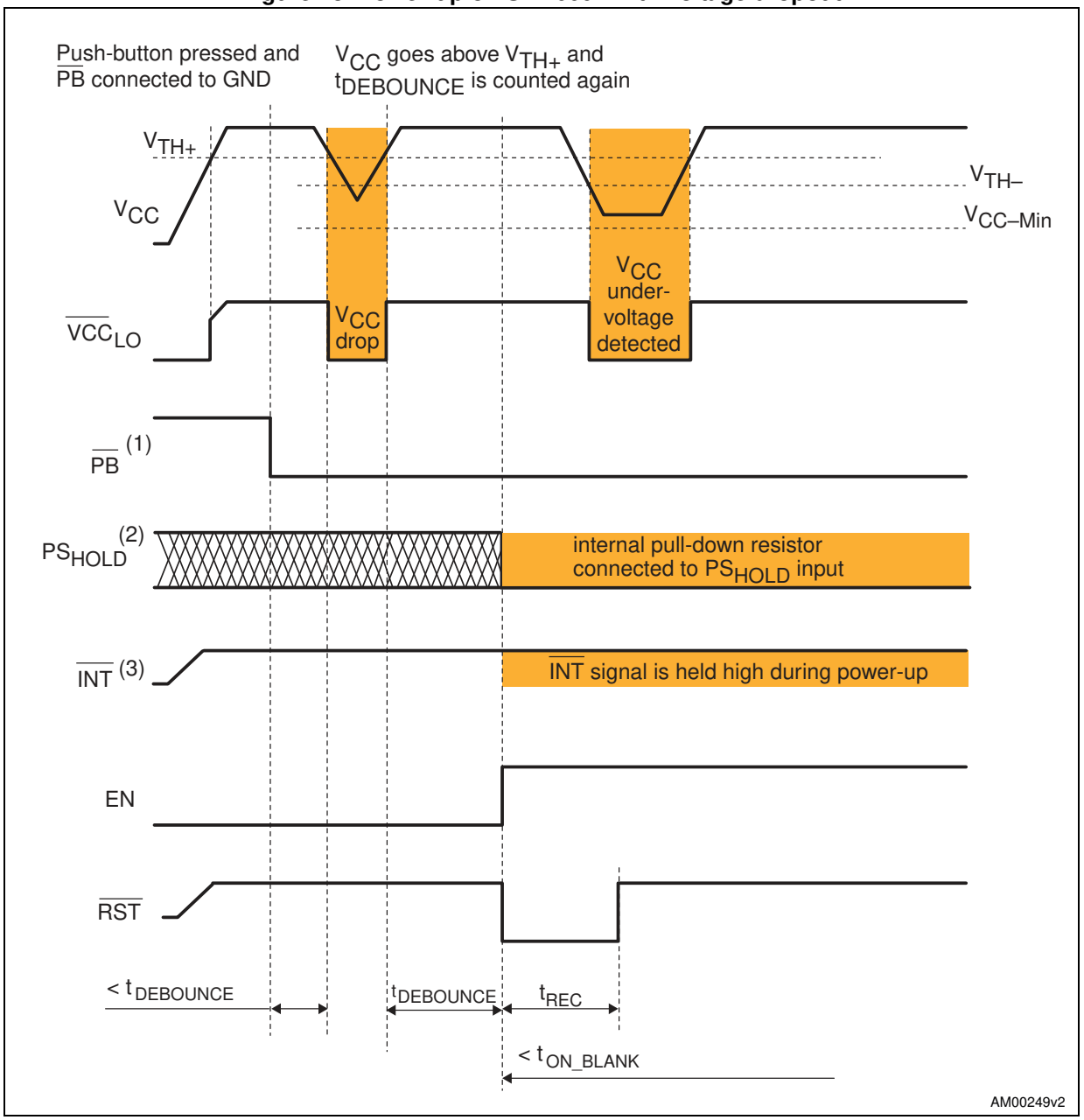
1. PB detection on falling edge.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. PS_{HOLD} signal is ignored during t_{ON_BLANK}. When t_{ON_BLANK} expires, the level of the PS_{HOLD} signal is not high therefore the EN signal goes low. Even releasing the PB button after the t_{ON_BLANK} will not prevent this.

图12。 STM6601 上电失败



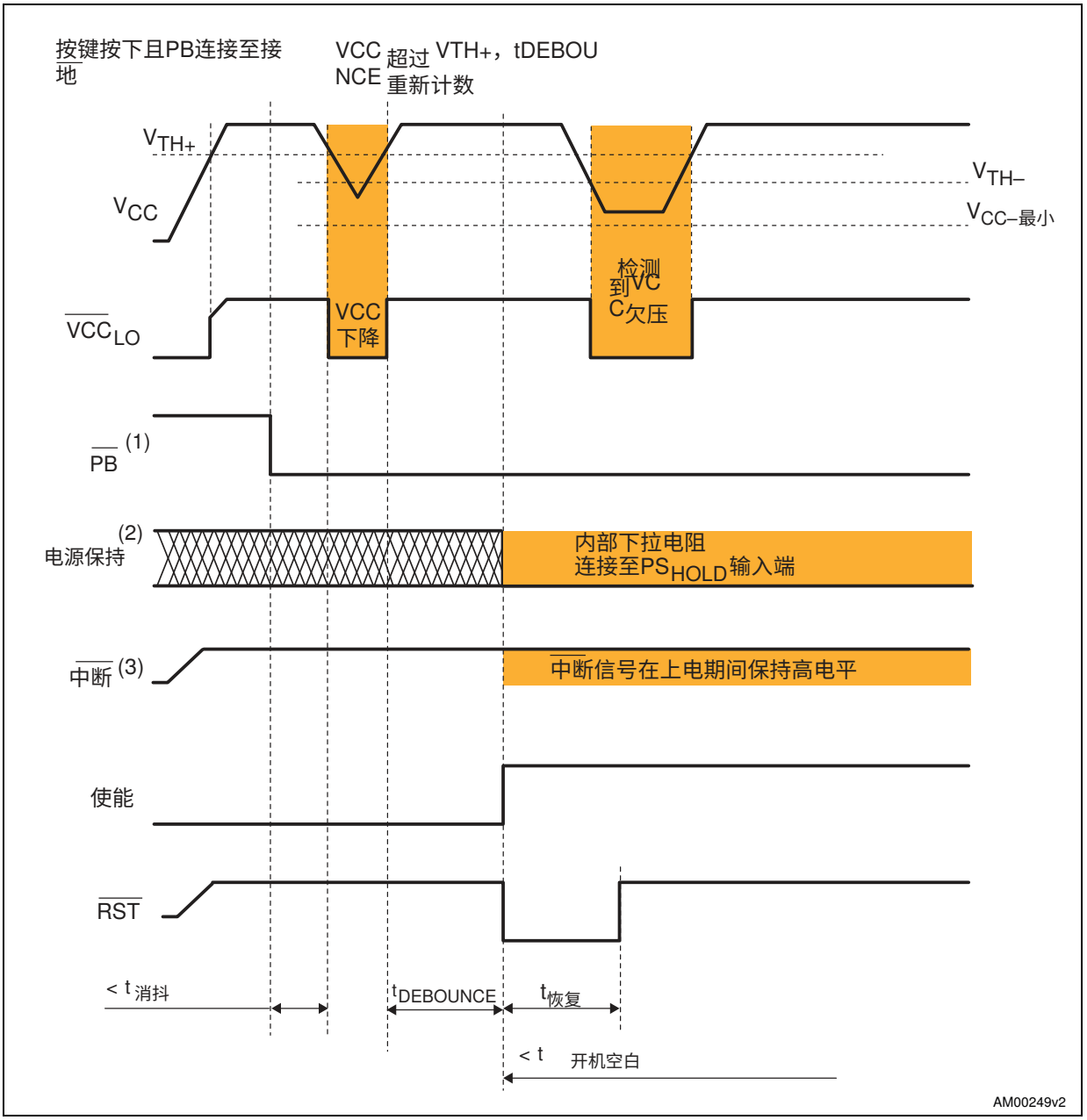
1. 按键检测在下降沿触发。
2. 上电期间，内部下拉电阻300 kΩ连接至PS HOLD输入端。
3. t开机空白期间忽略 PSHOLD信号。当 tON_BLANK到期时，PSHOLD信号电平不为高，导致 EN 信号变为低电平。即使在 tON_BLANK之后释放 PB 按钮，也无法阻止此情况。

Figure 13. Power-up on STM660x with voltage dropout



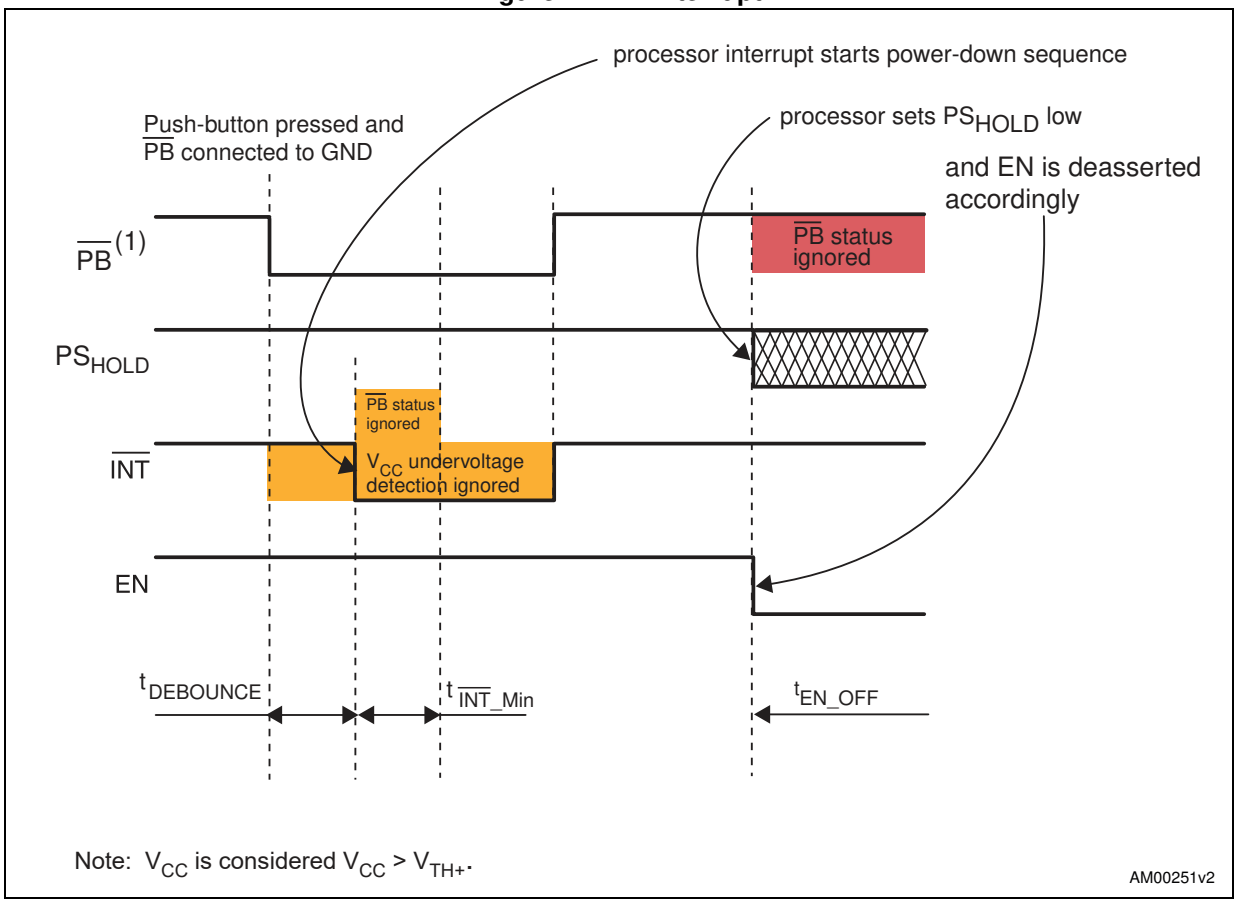
1. $\overline{PB}$ detection on falling and rising edges.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. $\overline{INT}$ signal is held high during power-up.

图13。 STM660x 电压掉电时的上电



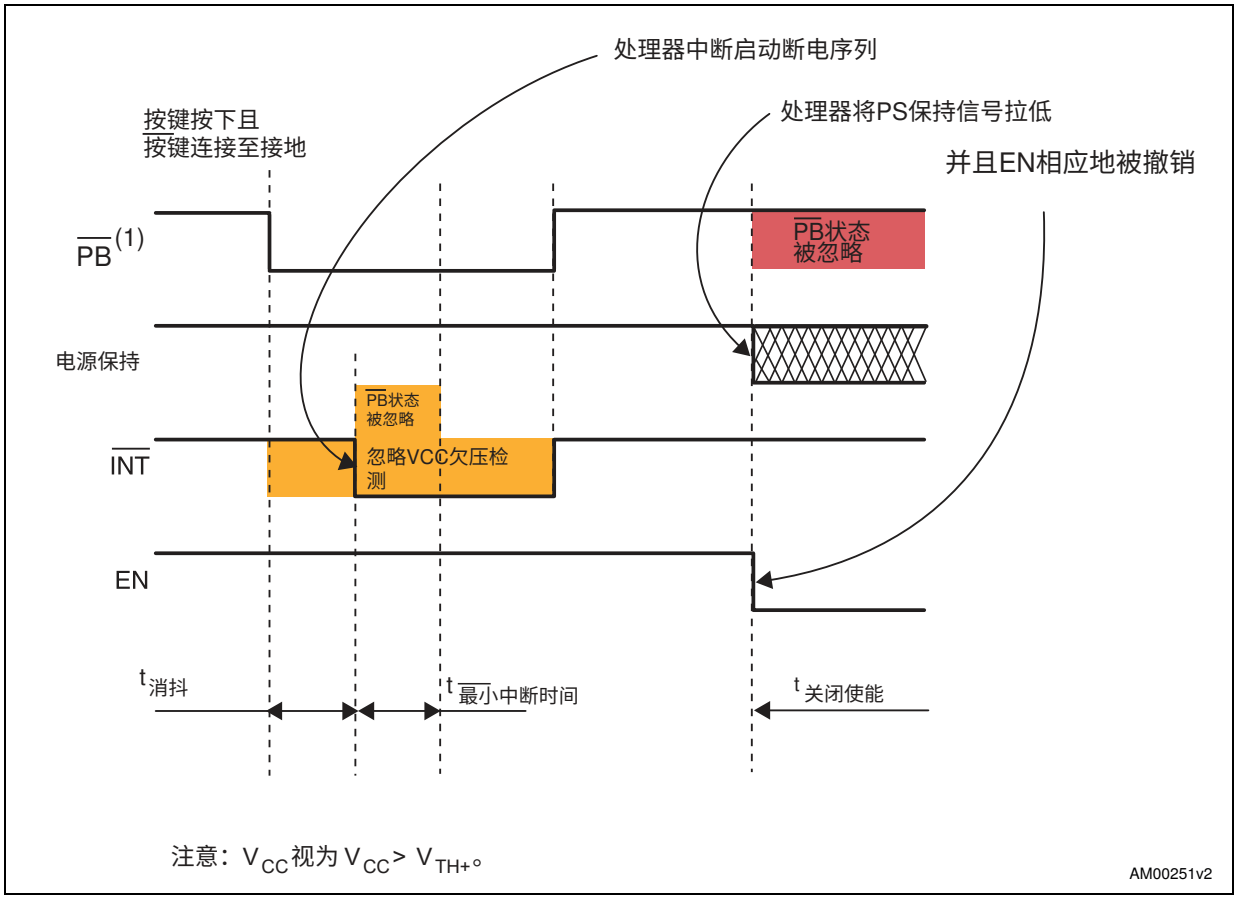
1. 按键检测在下降沿和上升沿。
2. 上电期间，内部下拉电阻300 kΩ连接至PS $_{HOLD}$输入端。
3. 上电期间中断信号保持高电平。

Figure 14. $\overline{PB}$ interrupt



1. $\overline{PB}$ detection on falling edge.

图14。$\overline{PB}$中断



1. 按键检测在下降沿触发。

Figure 15. Long push, $\overline{PB}$ pressed first

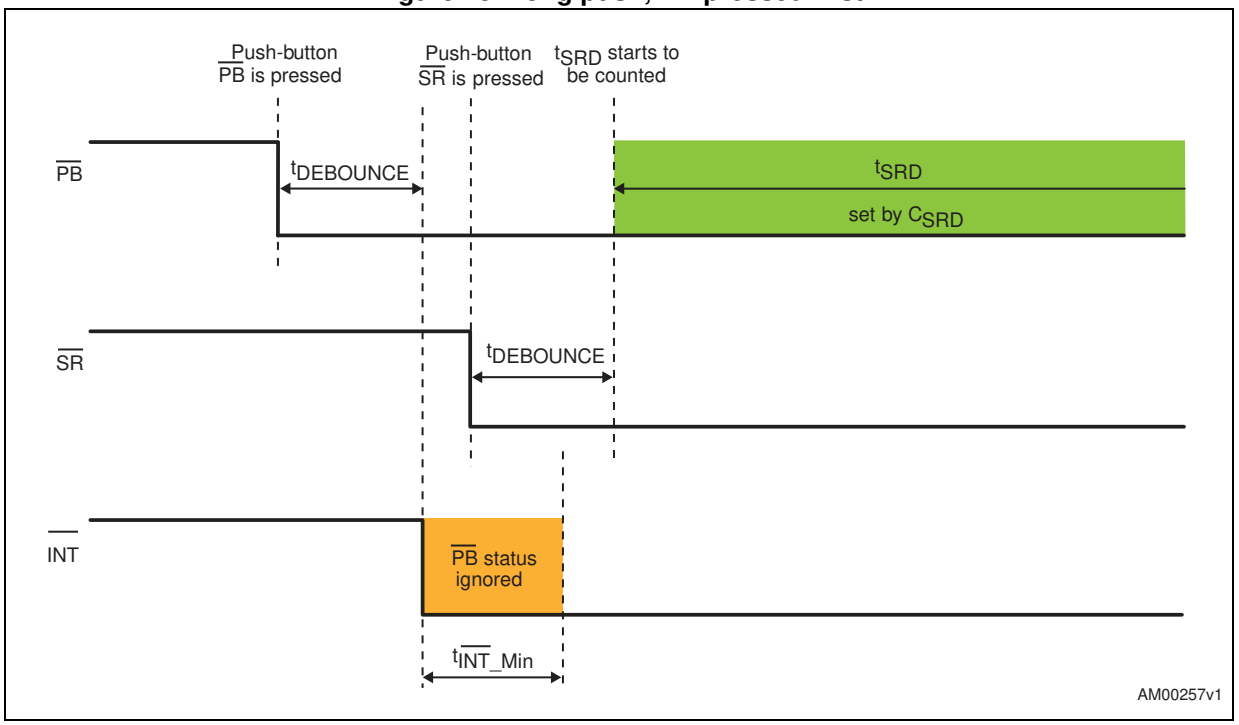


Figure 16. Long push, $\overline{SR}$ pressed first

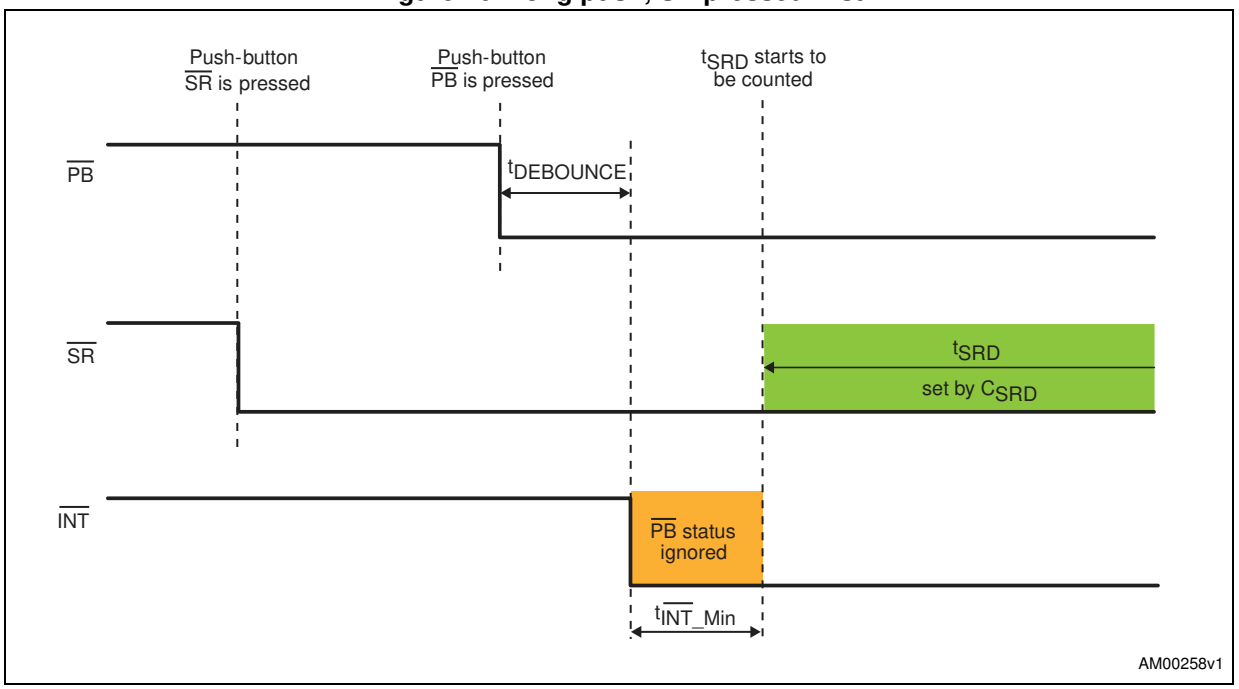


图15。 长按，$\overline{PB}$ 先按下

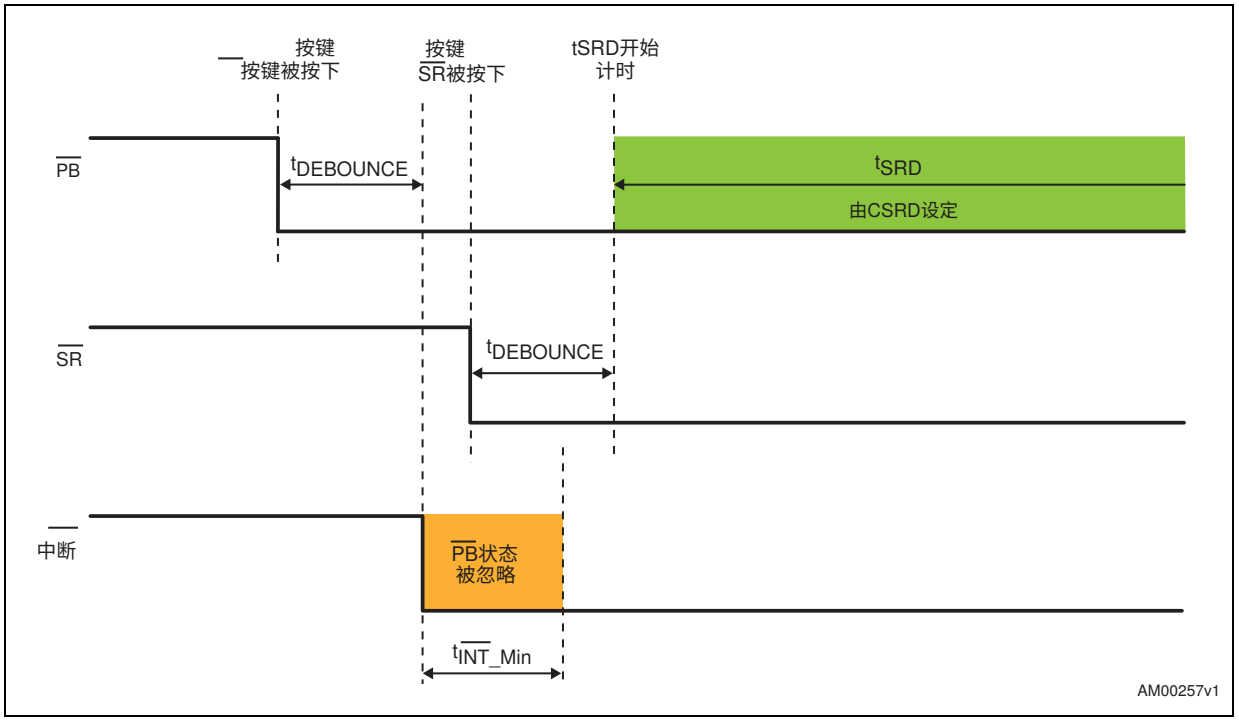


图16。 长按，$\overline{SR}$ 先按下

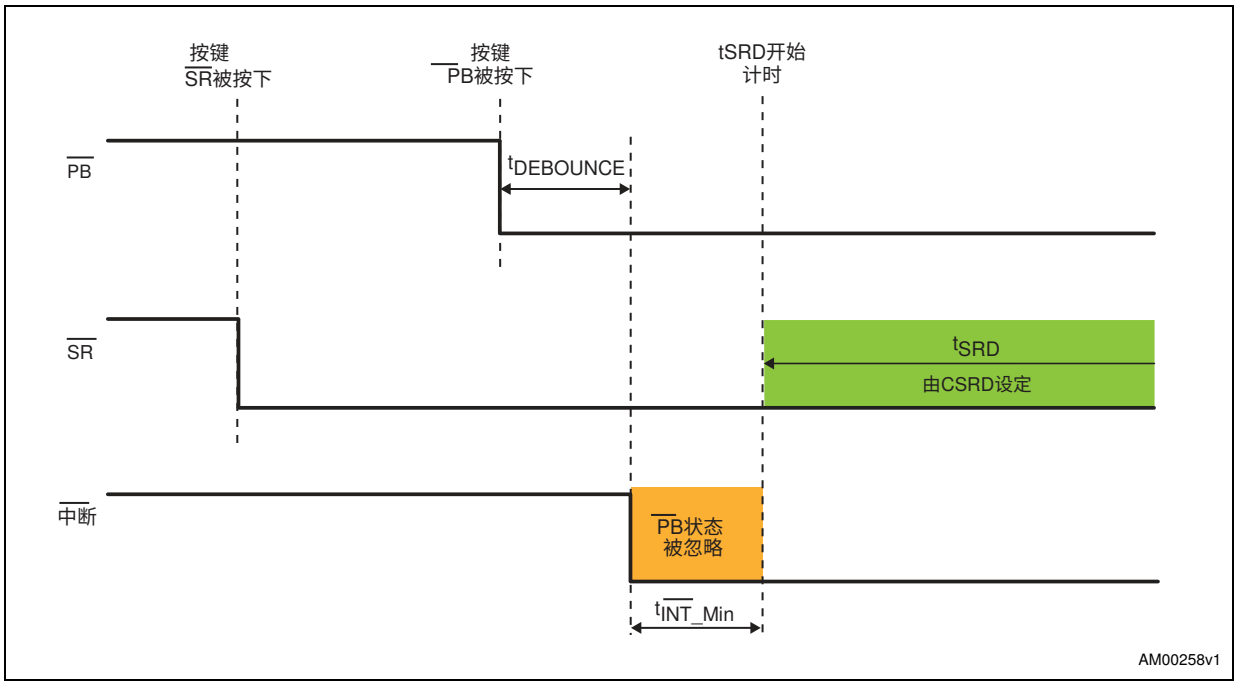


Figure 17. Invalid long push

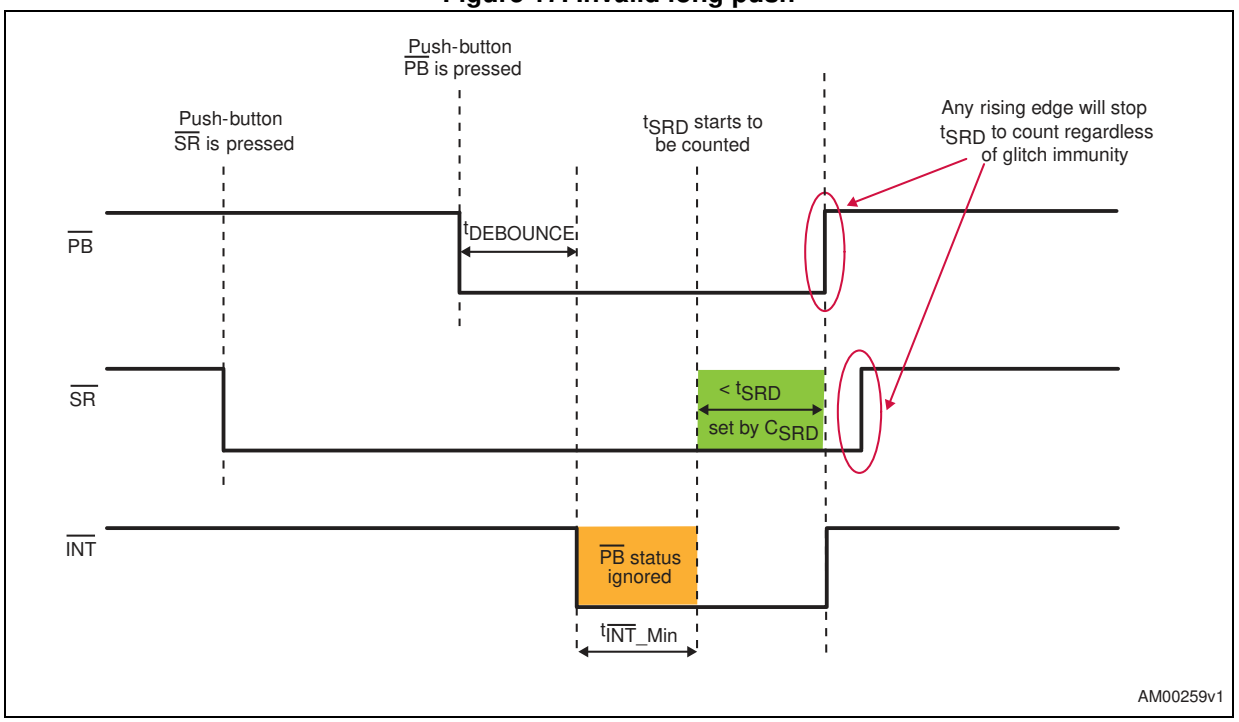


图17. 无效长按

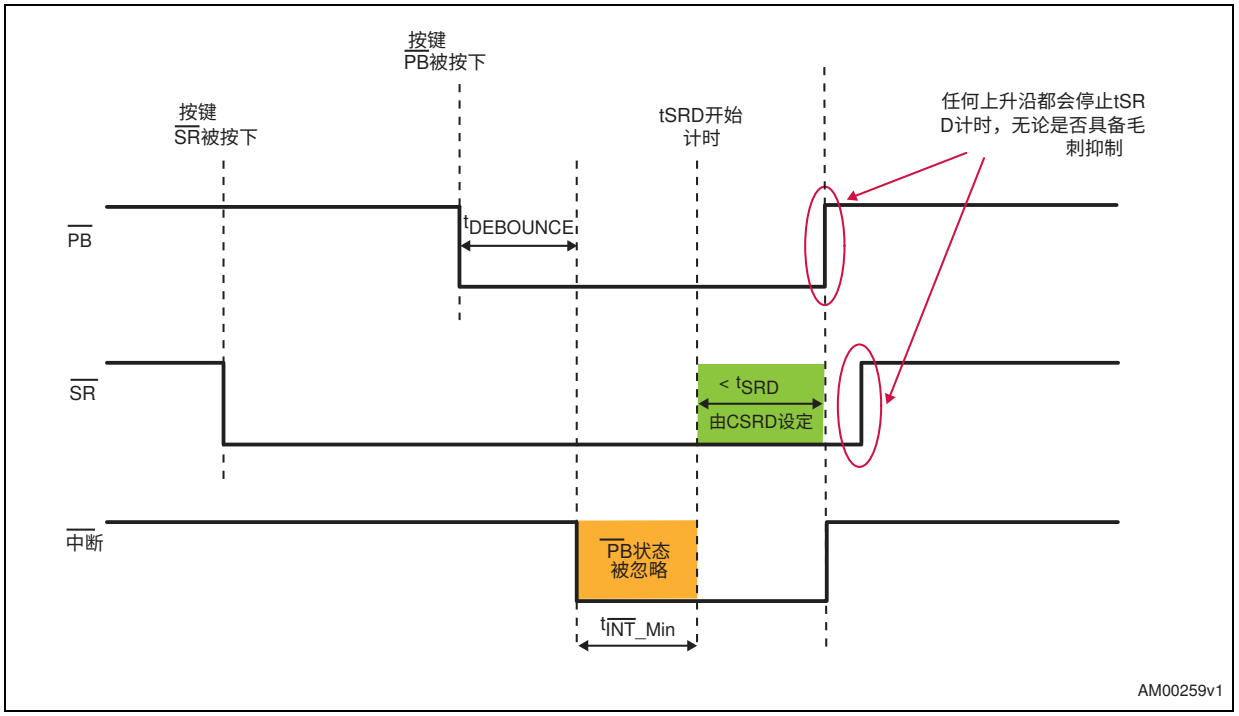
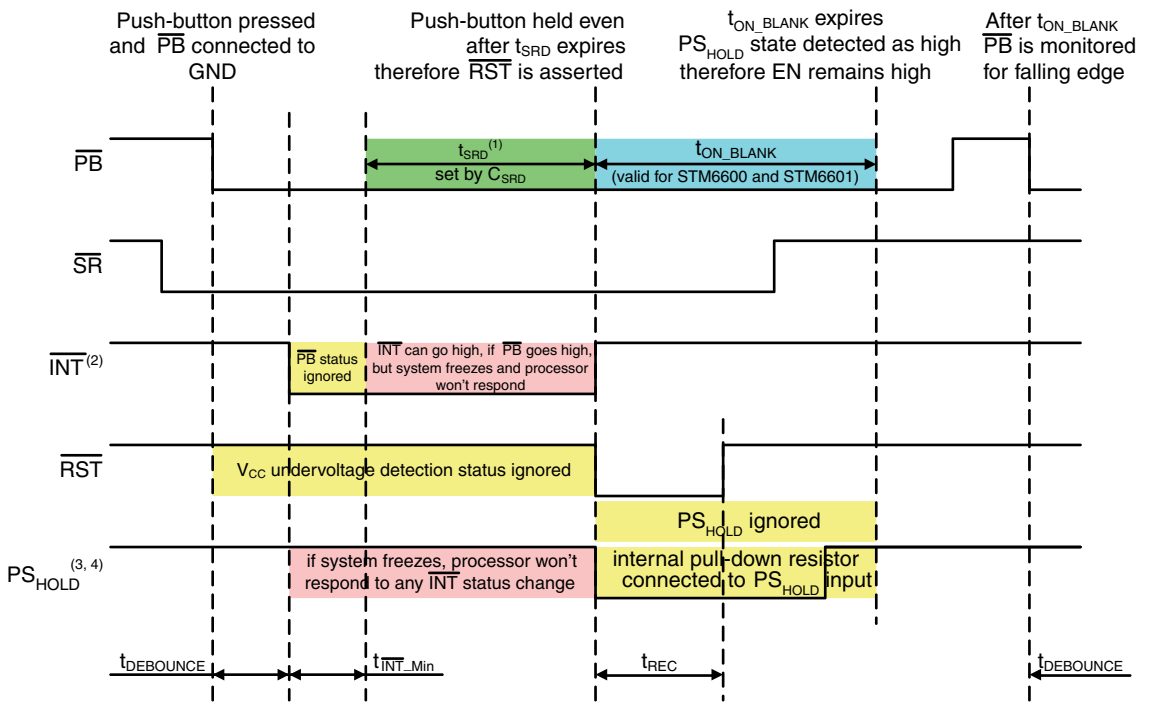
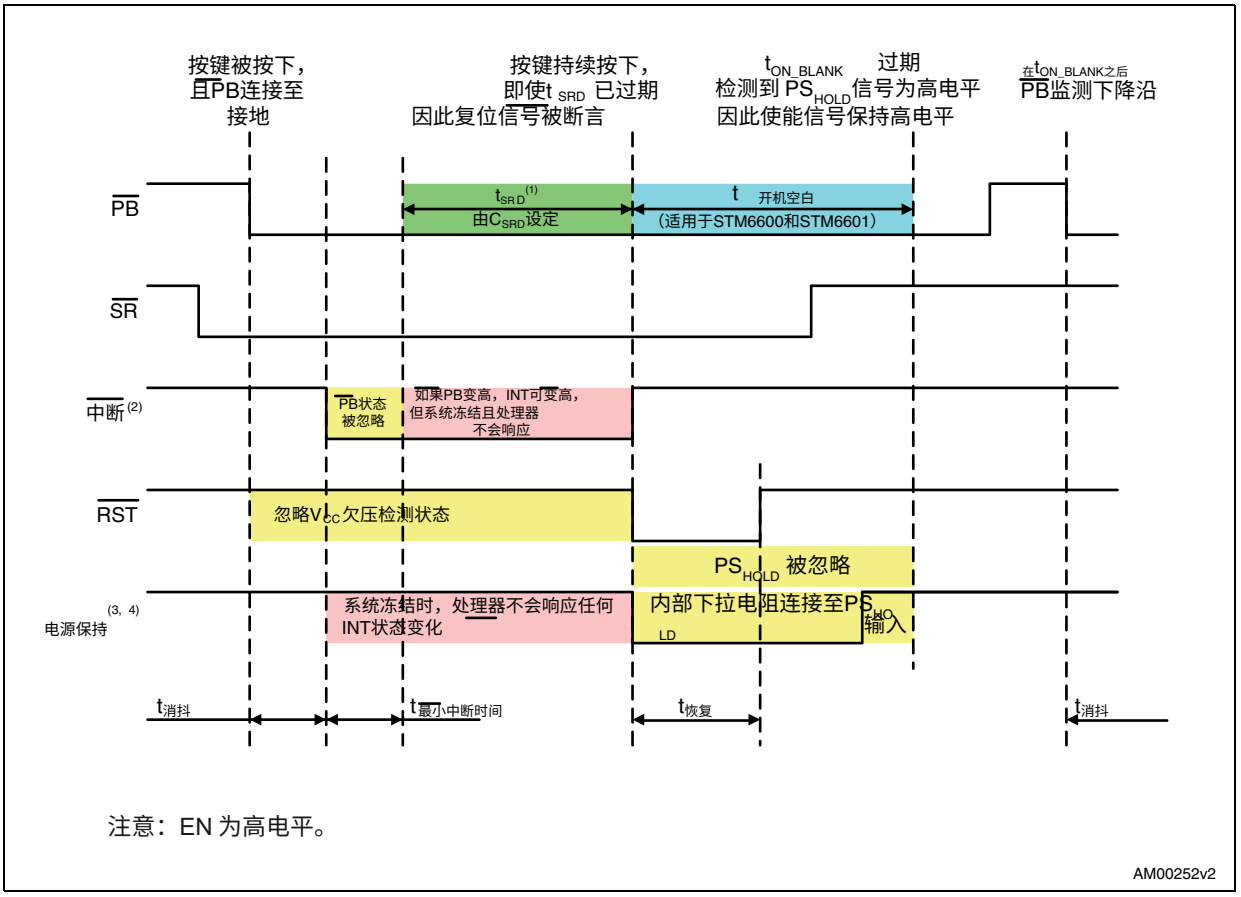

按键
PB被按下
按键
SR被按下
tSRD开始
计时
任何上升沿都会停止tSR
D计时，无论是否具备毛
刺抑制
PB
tDEBOUNCE
SR
< tSRD
由CSRD设定
中断
PB状态
被忽略
tINT_Min
AM00259v1

Figure 18. Long push (option with $\overline{RST}$ assertion)



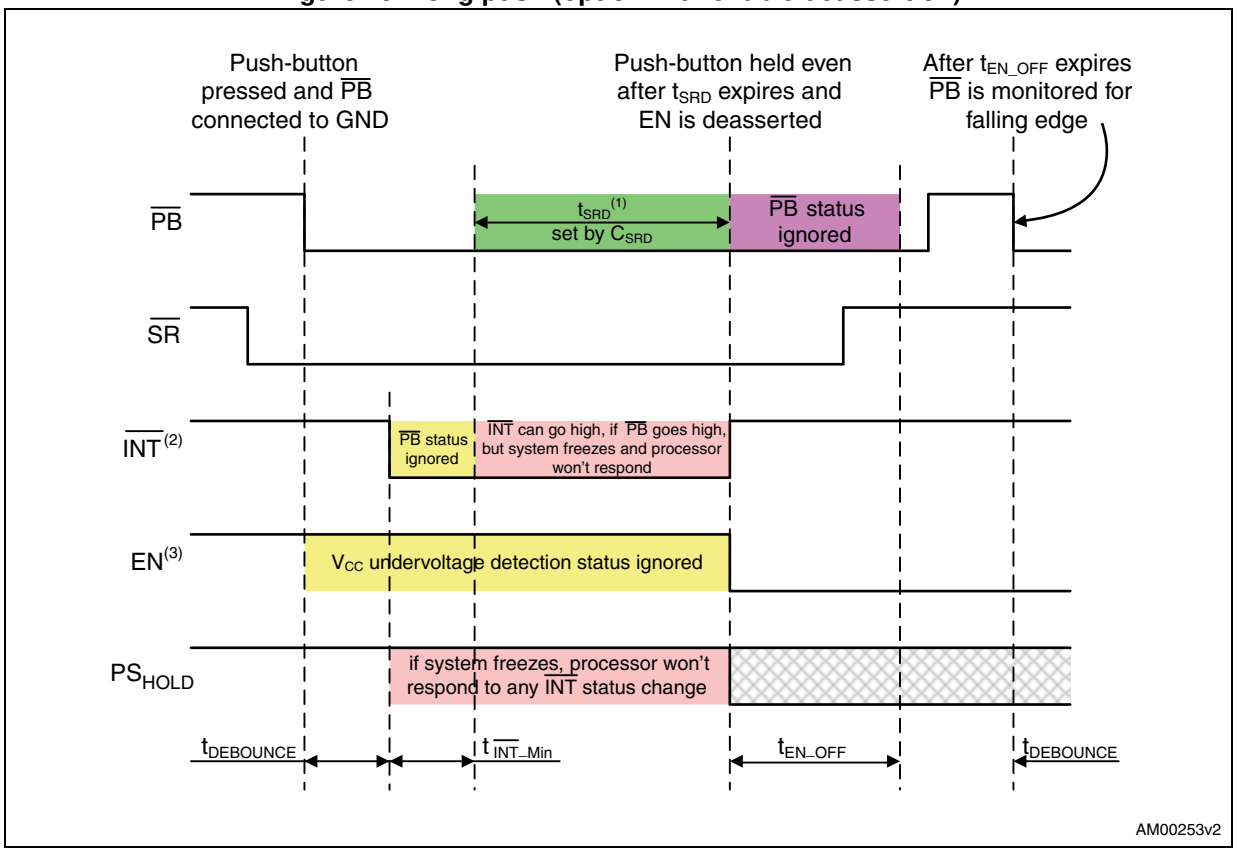
1. t_{SRD} period is set by external capacitor C_{SRD}.
2. $\overline{PB}$ ignored during $t_{\overline{INT}\_Min}$.
3. PS_{HOLD} signal is ignored during t_{ON_BLANK}. Its level is checked after t_{ON_BLANK} expires and if it is high the EN signal remains asserted, otherwise EN goes low.
4. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during startup when device is reset.

图18. 长按（带RST断言选项）



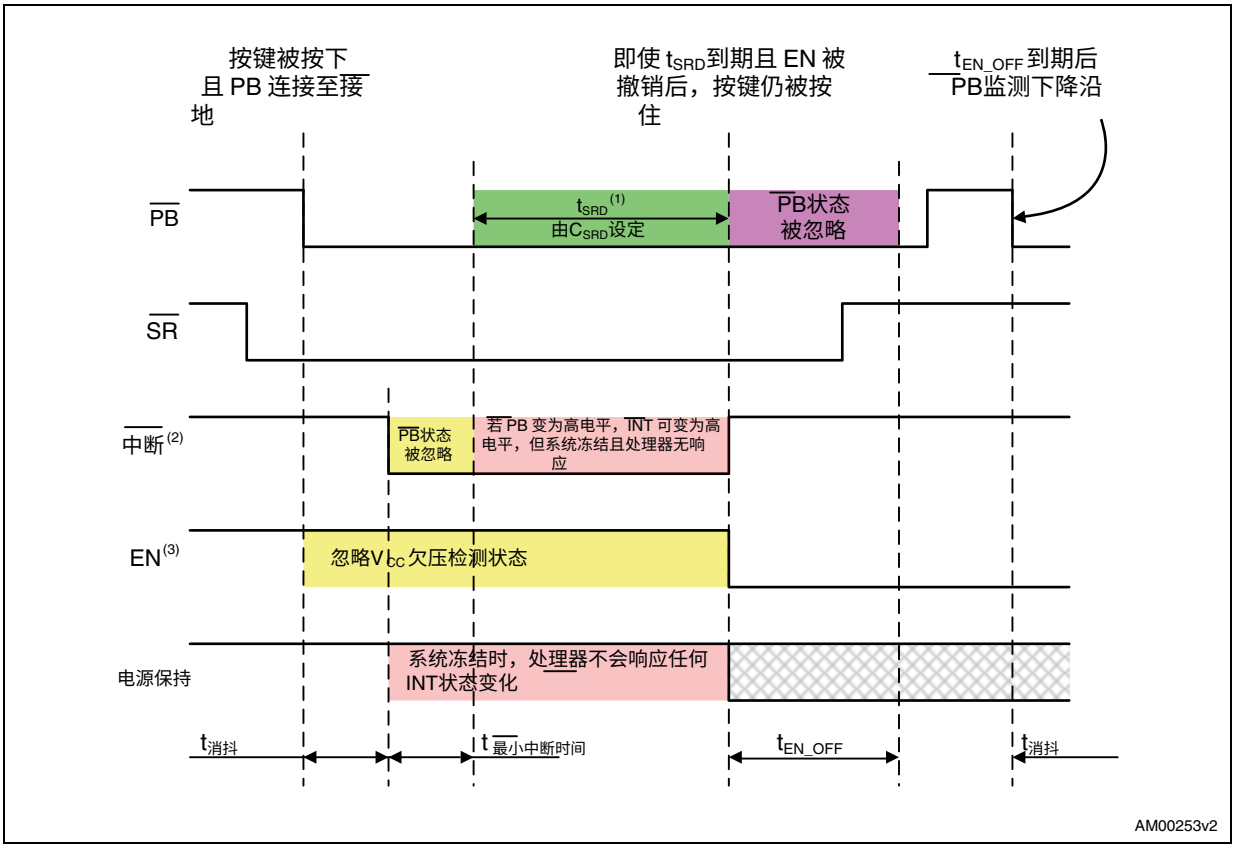
1. t_{SRD} 周期由外部电容C_{SRD}设定。
2. $t_{\overline{INT}\_Min}$ 期间忽略 $\overline{PB}$。
3. $t_{开机空白}$期间忽略 $PSH_{OL}D$信号。其电平在t_{ON_BLANK}结束后检测，若为高电平，则使能信号保持有效，否则使能信号变低。
4. 内部下拉电阻300 kΩ连接至PS_{HOLD}输入端，设备复位时启动。

Figure 19. Long push (option with enable deassertion)



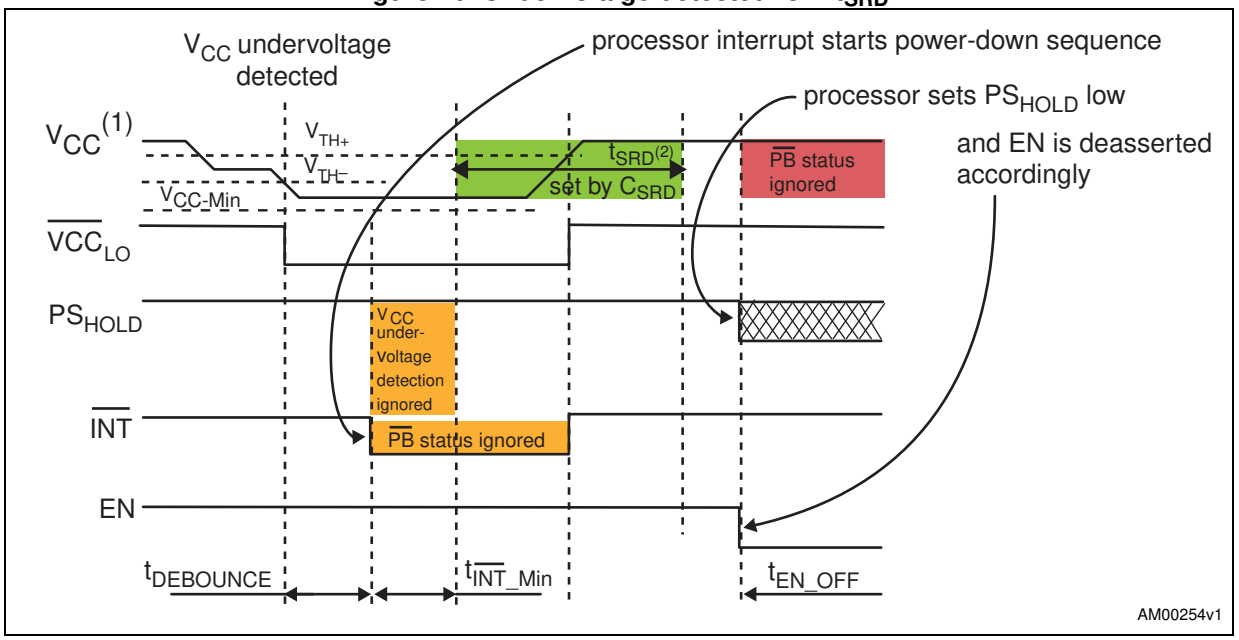
1. t_{SRD} period is set by external capacitor C_{SRD}.
2. $\overline{PB}$ ignored during $t_{\overline{INT}\_Min}$.
3. After t_{SRD} expires EN is forced low.

图19. 长按（带使能取消选项）



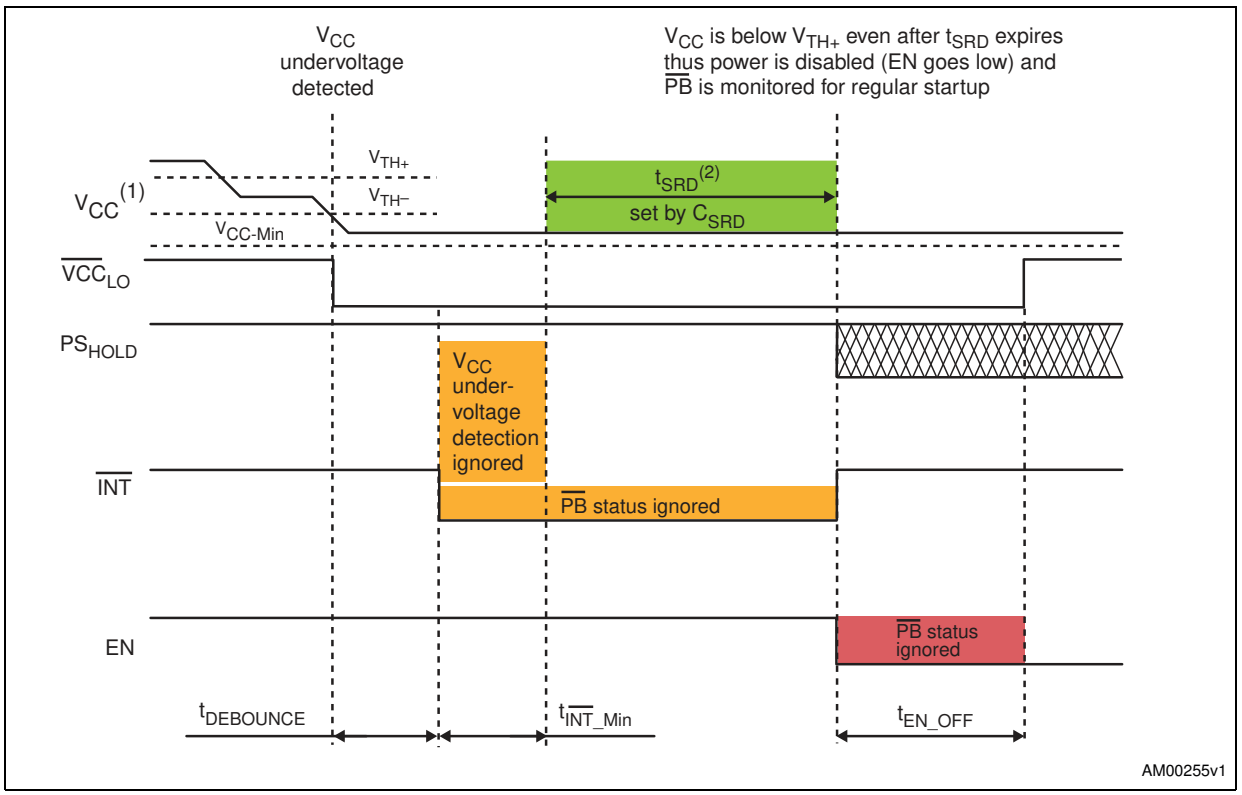
1. t_{SRD} 周期由外部电容C_{SRD}设定。
2. t_{INT_Min} 期间忽略 PB。
3. t_{SRD}到期后，EN 被强制拉低。

Figure 20. Undervoltage detected for <t_{SRD}



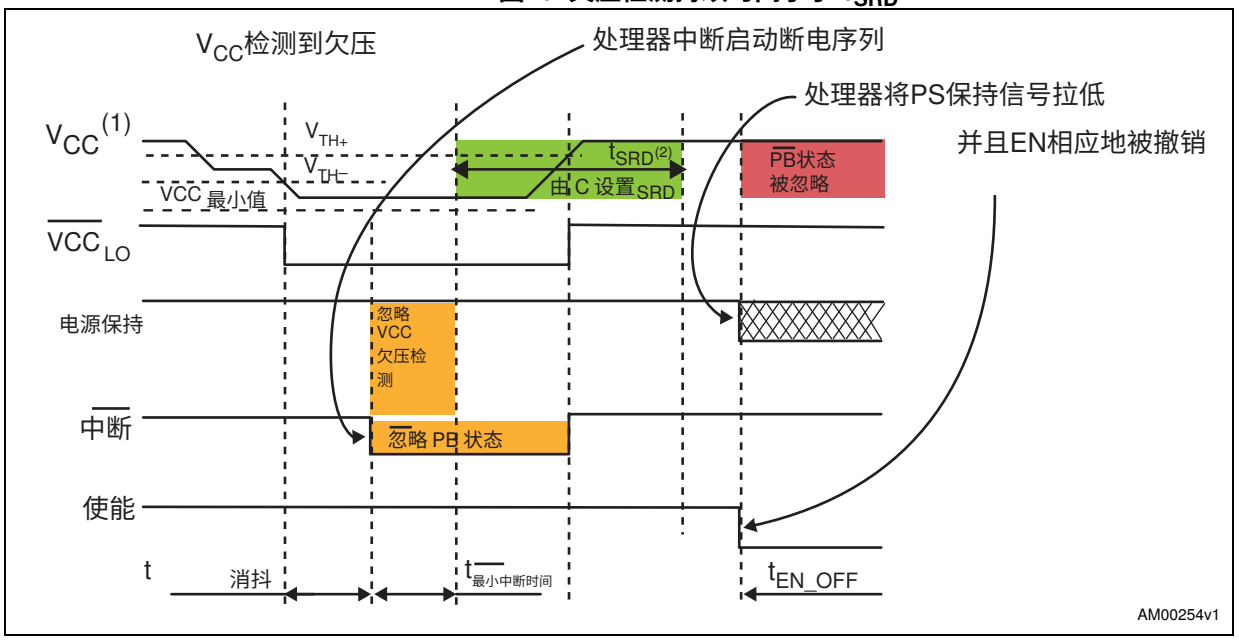
1. V_{CC} goes above V_{TH+} within t_{SRD} thus power is not disabled after t_{SRD} expires.
2. t_{SRD} period is set by external capacitor C_{SRD}.

Figure 21. Undervoltage detected for >t_{SRD}



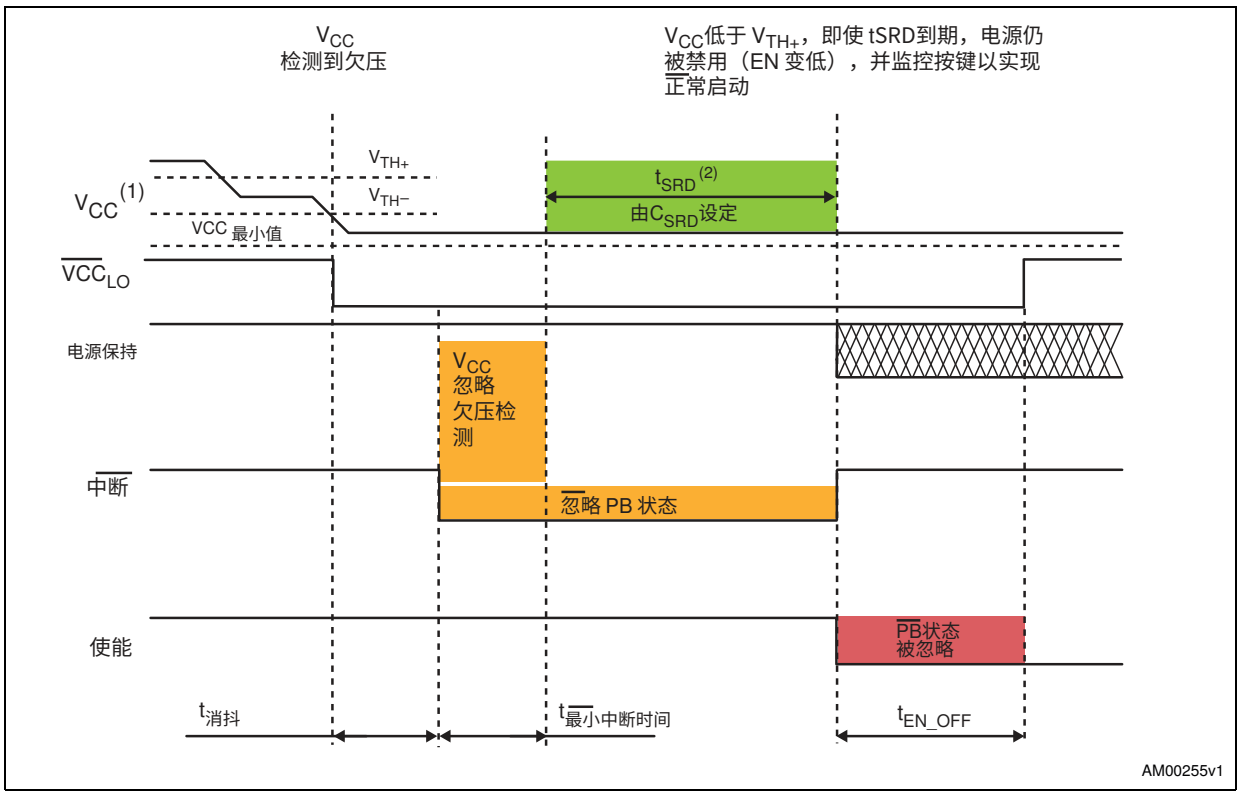
1. After t_{SRD} expires V_{CC} is still insufficient (below V_{TH+}) thus power is disabled (EN goes low or $\overline{EN}$ goes high).
2. t_{SRD} period is set by external capacitor C_{SRD}.

图20. 欠压检测持续时间小于 t_{SRD}



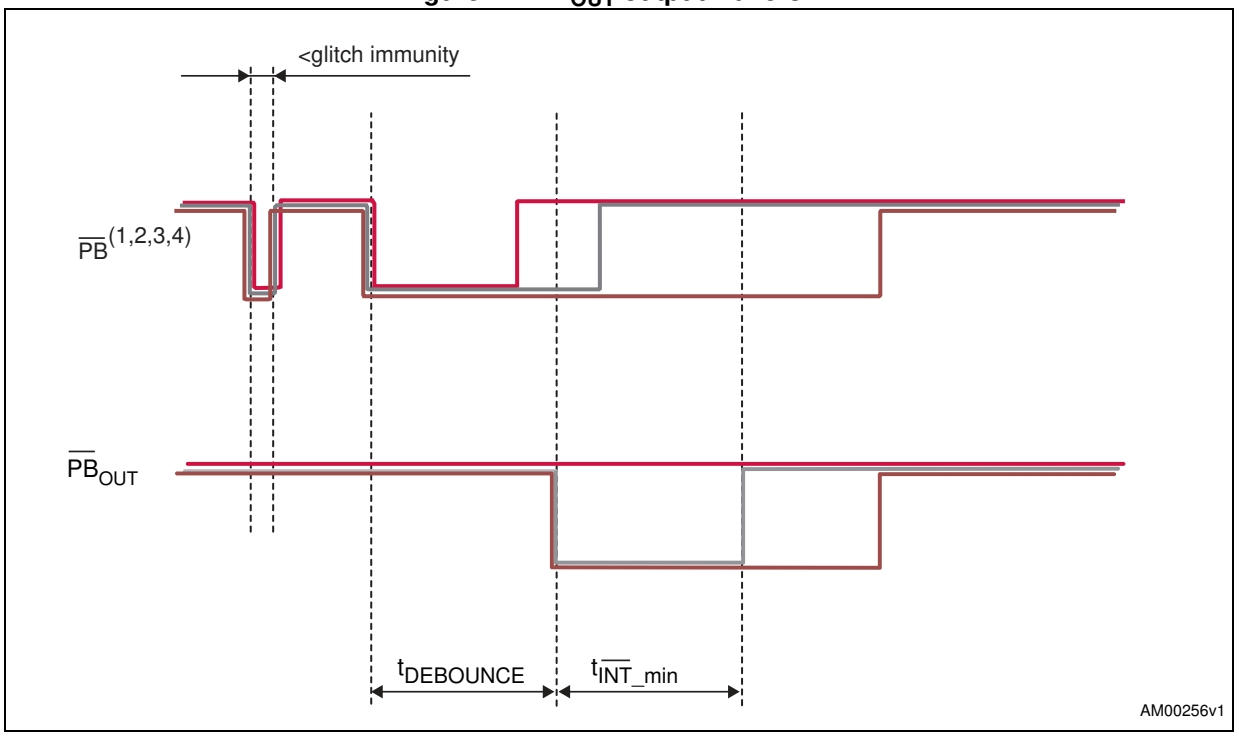
1. V_{CC} 在 t_{SRD} 内超过 V_{TH+}，因此 t_{SRD} 到期后电源未被禁用。
2. t_{SRD} 周期由外部电容 C_{SRD} 设定。

图21. 欠压检测持续时间大于 t_{SRD}



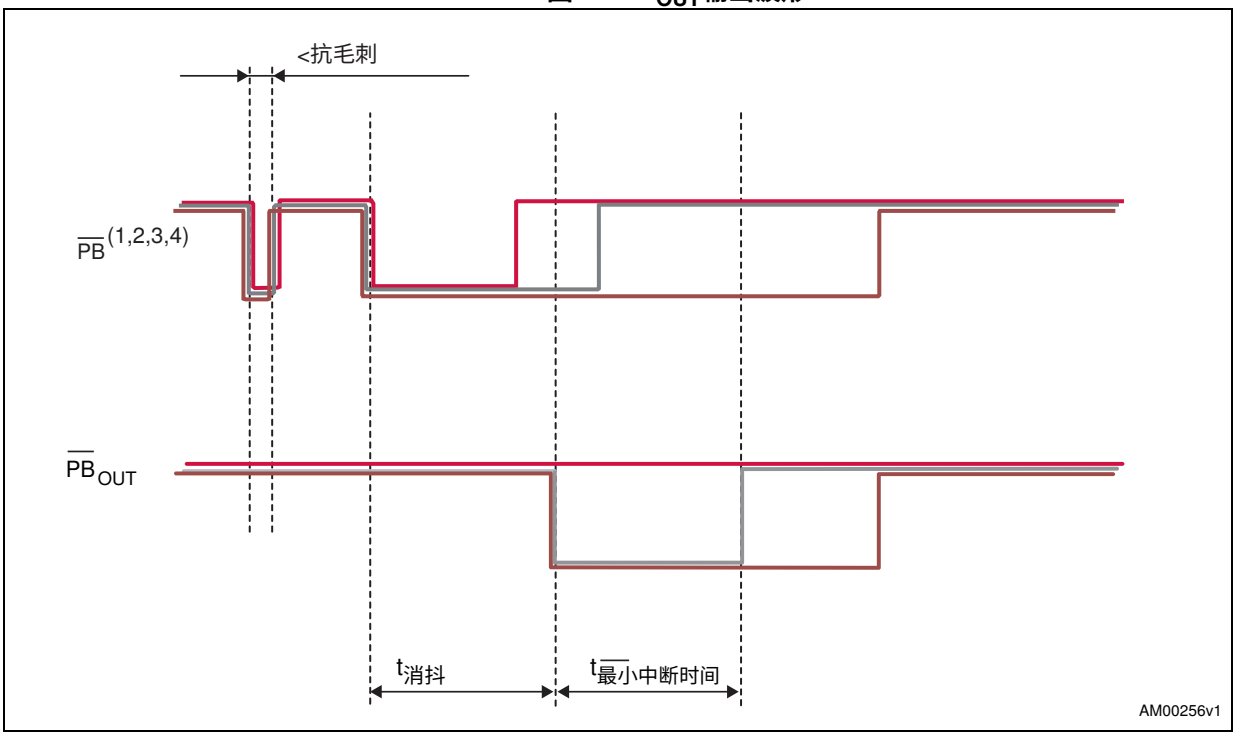
1. t_{SRD} 到期后，V_{CC} 仍不足（低于 V_{TH+}），因此电源被禁用（EN 变为低电平或 EN 变为高电平）。
2. t_{SRD} 周期由外部电容 C_{SRD} 设定。

Figure 22. $\overline{PB}_{OUT}$ output waveform



1. Pulses on $\overline{PB}$ shorter than glitch immunity are ignored.
2. Pulses on $\overline{PB}$ shorter than $t_{DEBOUNCE}$ are not recognized by $\overline{PB}_{OUT}$.
3. Minimum pulse width on $\overline{PB}_{OUT}$ is $t_{\overline{INT}\_Min}$.
4. If push-button is held longer than $t_{DEBOUNCE}$ + $t_{\overline{INT}\_Min}$, $\overline{PB}_{OUT}$ goes high when the push-button is released.

图22. $\overline{PB}_{OUT}$输出波形



1. 按键上短于抗毛刺时间的脉冲将被忽略。
2. 按键上短于 $t_{DEBOUNCE}$ 的脉冲不会被 PB_{OUT} 识别。
3. PB_{OUT} 上的最小脉冲宽度为 t_{INT_Min}。
4. 如果按键按下时间超过 $t_{DEBOUNCE}$+ t_{INT_Min}，松开按键时 $\overline{PB}_{OUT}$ 将变高。

5 Typical operating characteristics

Figure 23. Supply current vs. temperature, normal state

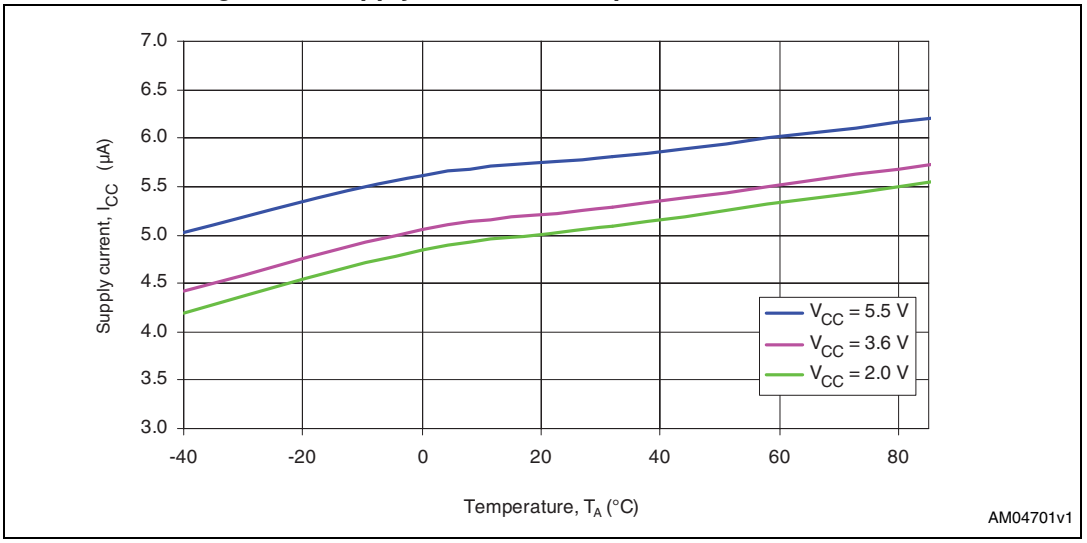
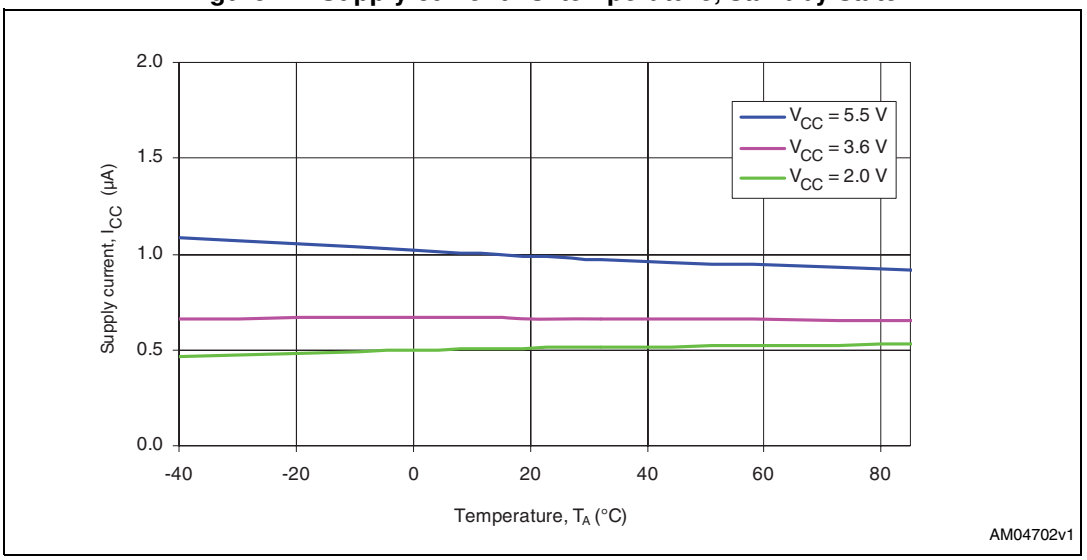


Figure 24. Supply current vs. temperature, standby state



5 典型工作特性

图23. 供电电流与温度关系，正常状态

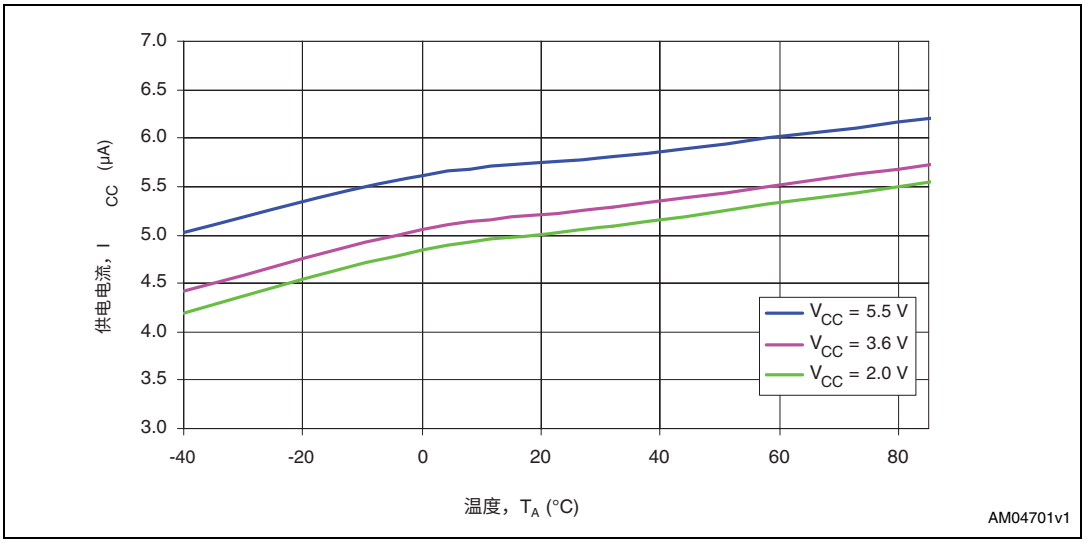


图24. 供电电流与温度关系，待机状态

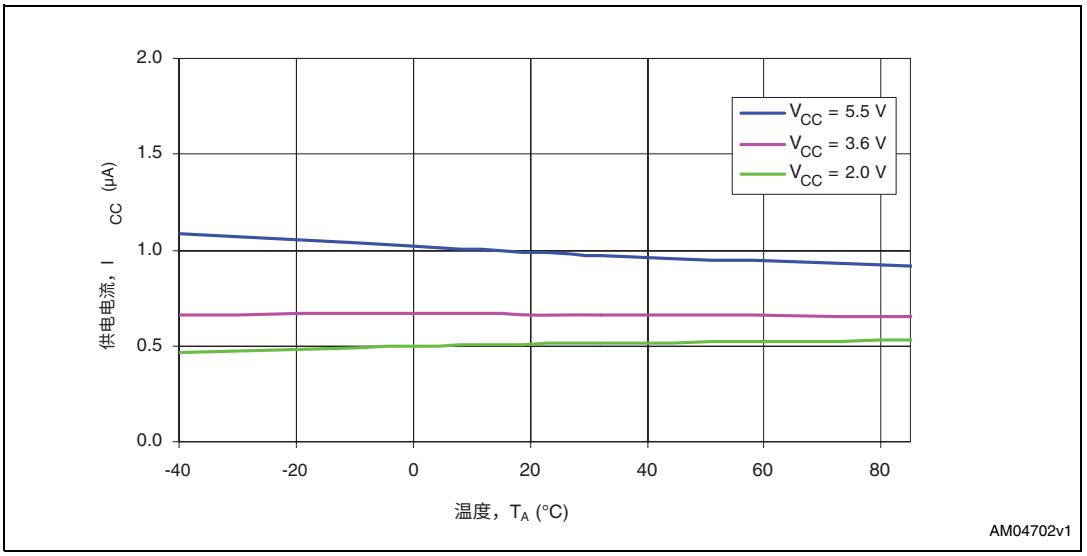


Figure 25. Supply current vs. supply voltage, normal state

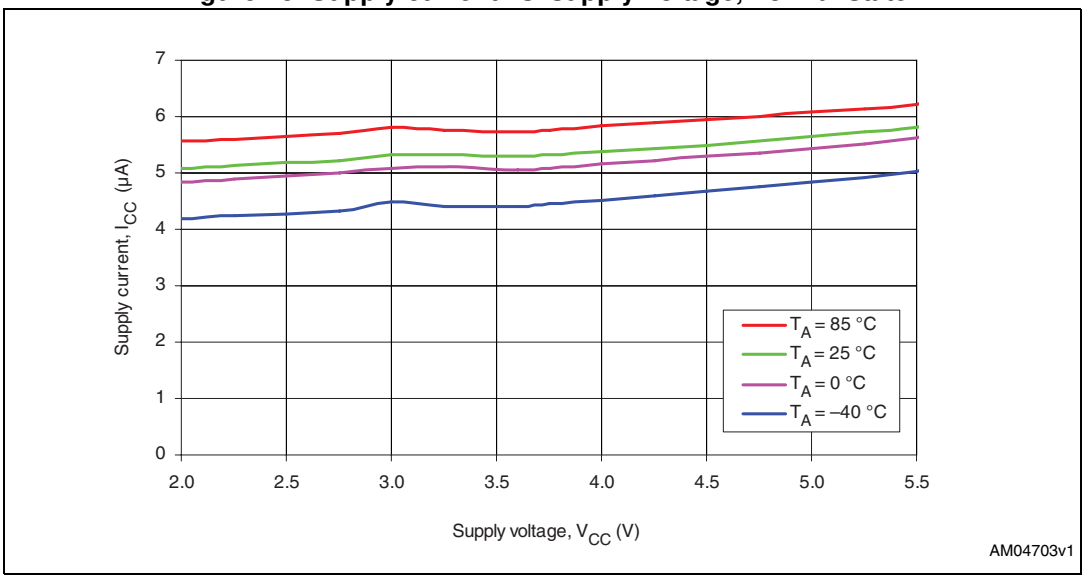


Figure 26. Supply current vs. supply voltage, standby state

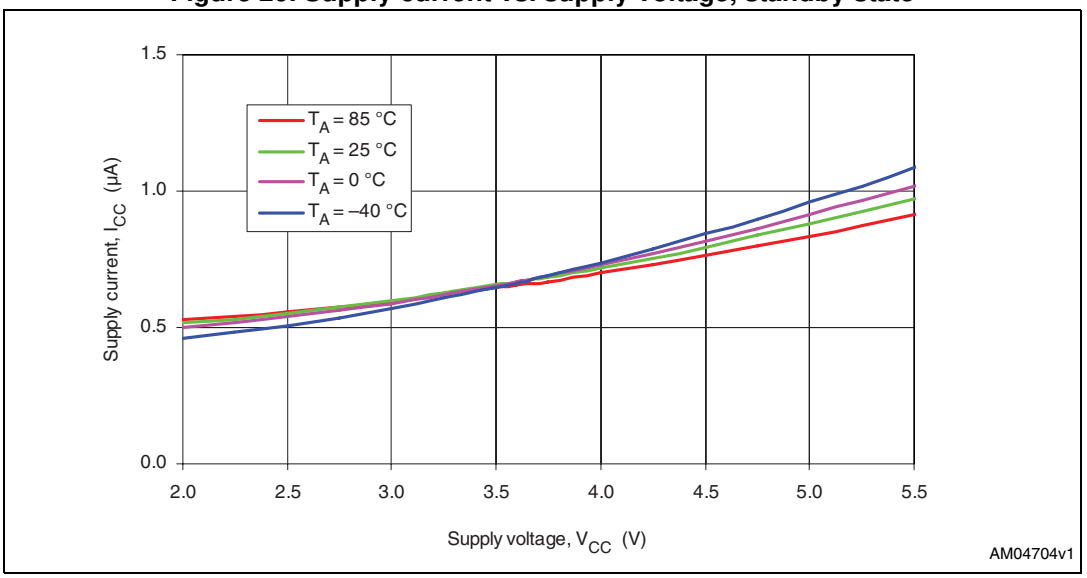


图25. 供电电流与供电电压关系，正常状态

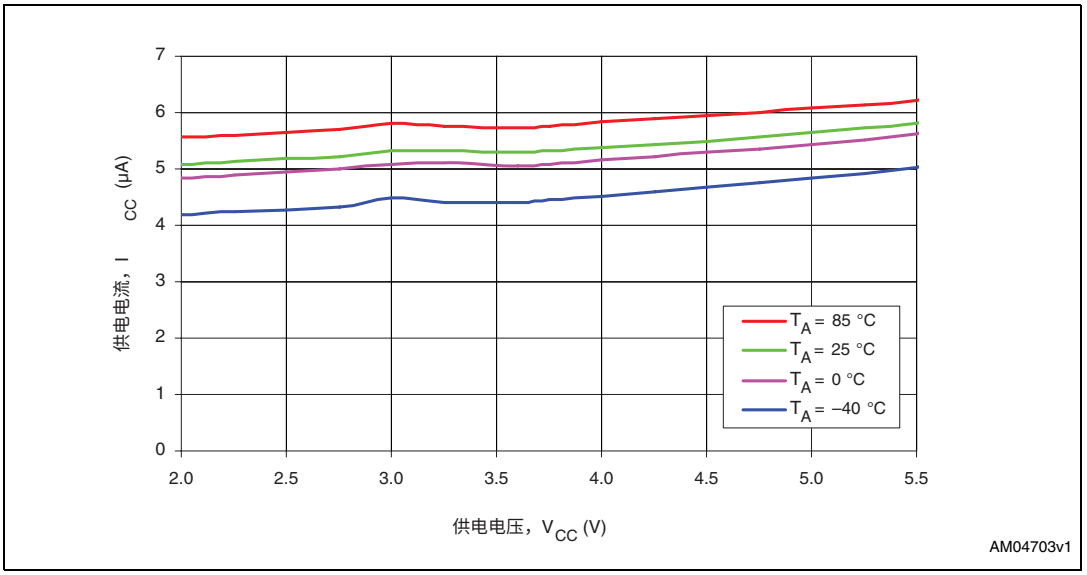


图26. 供电电流与供电电压关系，待机状态

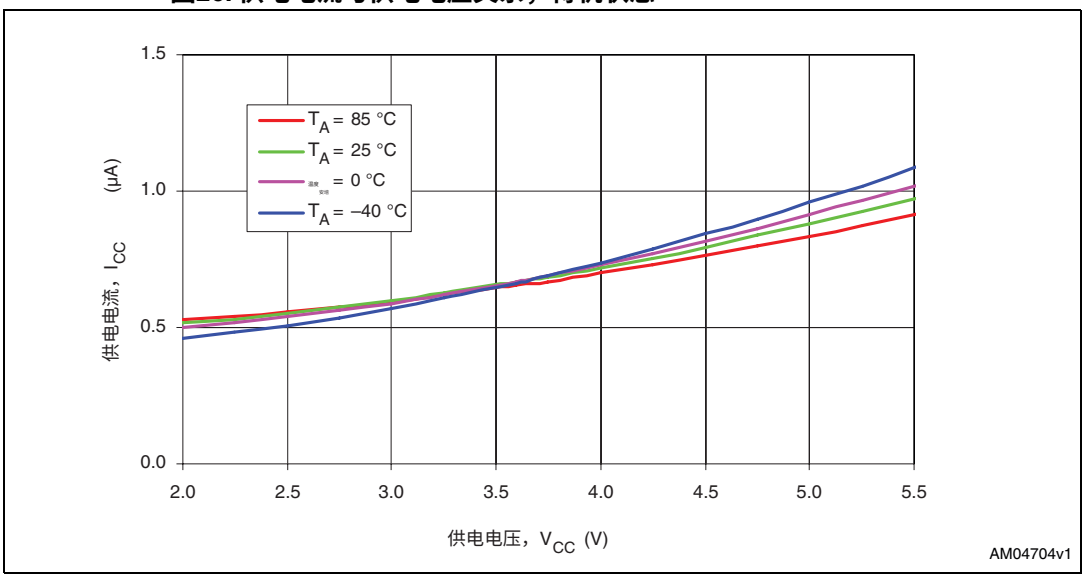


Figure 27. Threshold vs. temperature, V_{TH+} = 3.4 V (typ.)

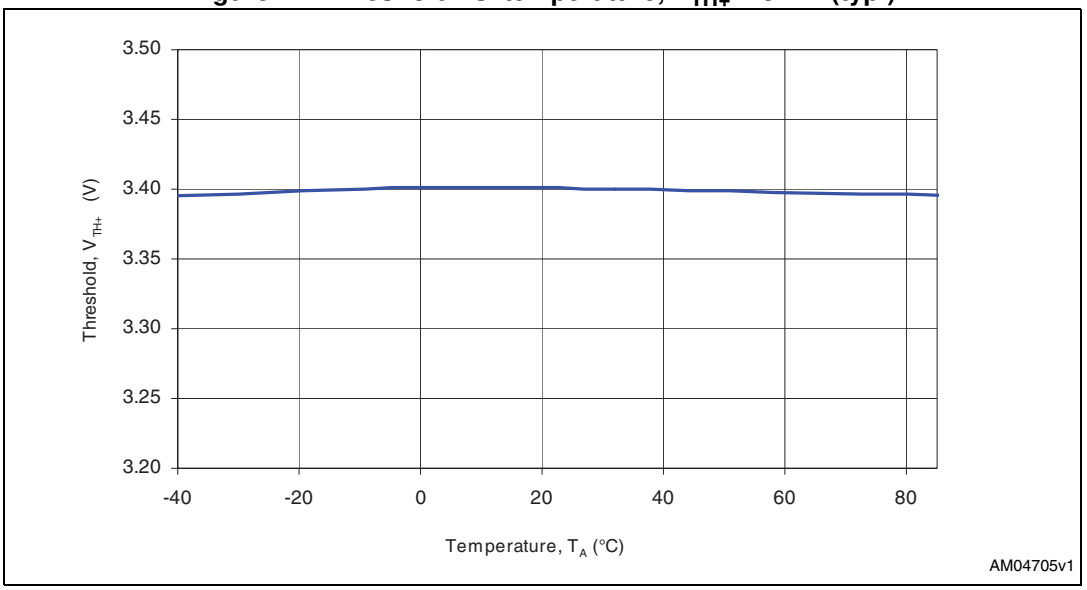


Figure 28. Threshold hysteresis vs. temperature, V_{HYST} = 200 mV (typ.)

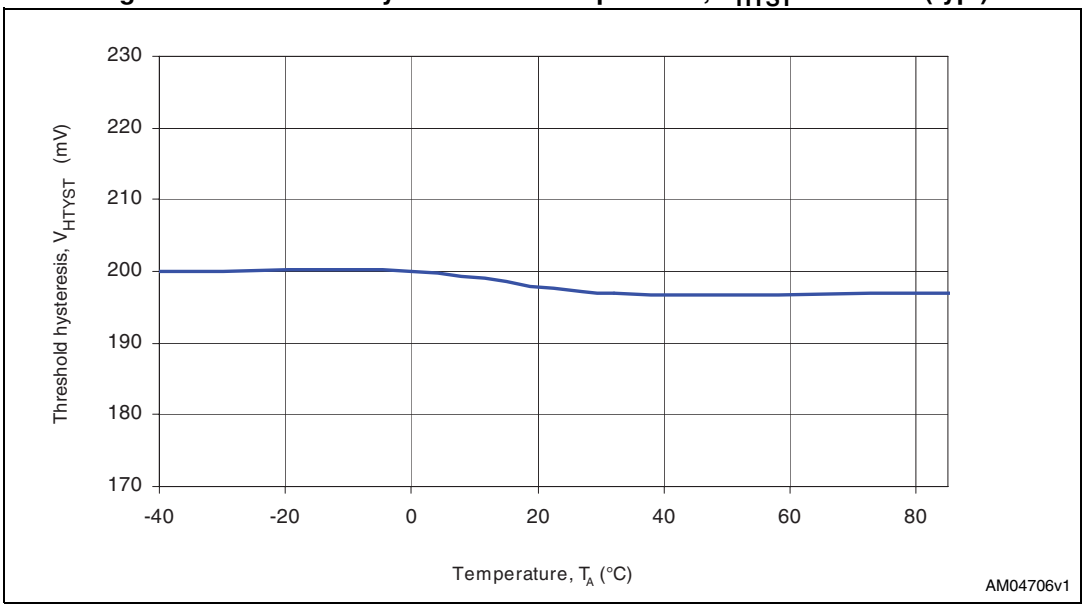


图27. 阈值与温度关系，V_{TH+}= 3.4 V（典型值）

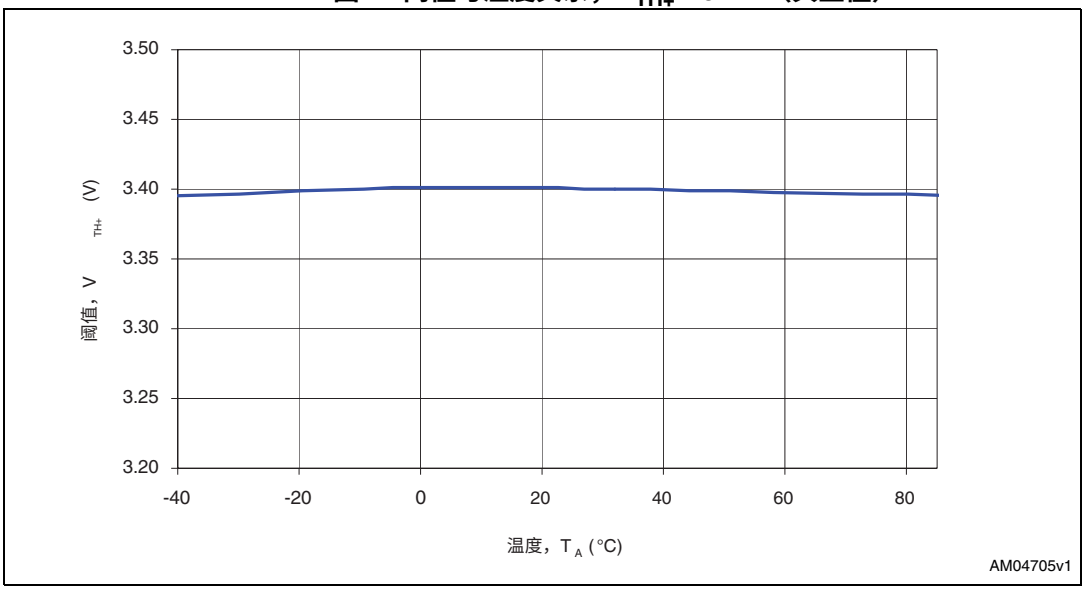


图28. 阈值滞后与温度关系，V_{HYST}= 200 mV（典型值）

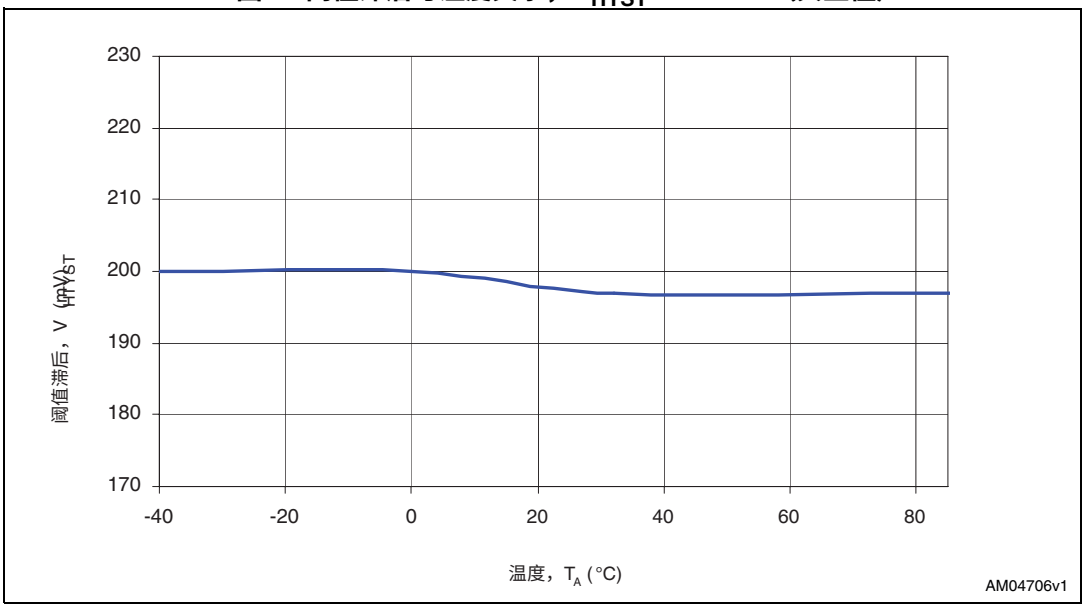


Figure 29. Debounce period vs. supply voltage

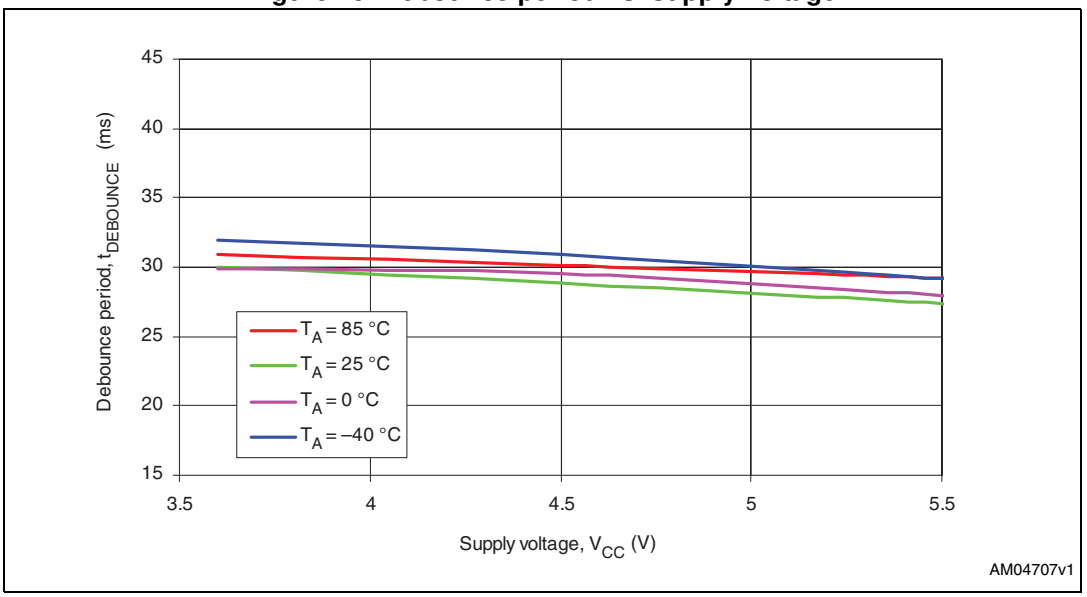


Figure 30. C_{SRD} charging current vs. temperature, V_{CC} = 3.6 V

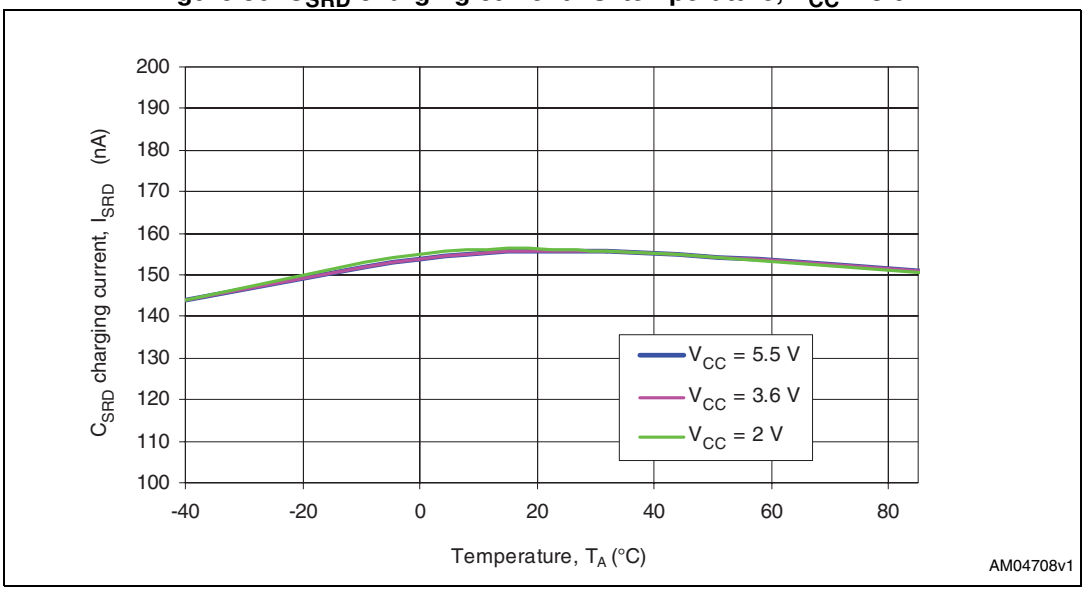


图29. 消抖期与供电电压关系

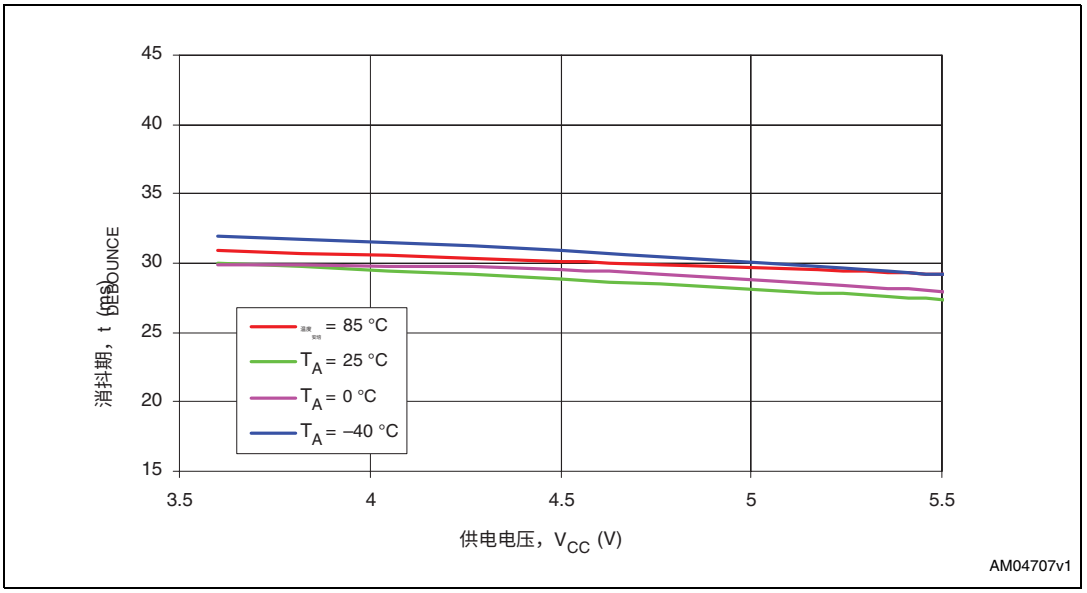


图30。 C_{SRD}充电电流与温度的关系，V_{CC}= 3.6 V

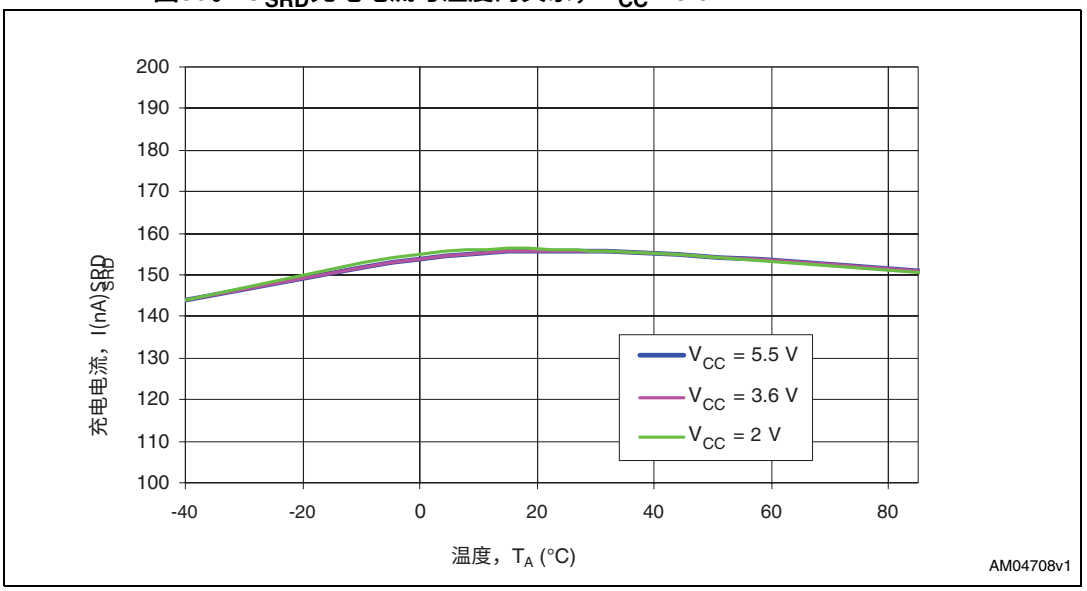
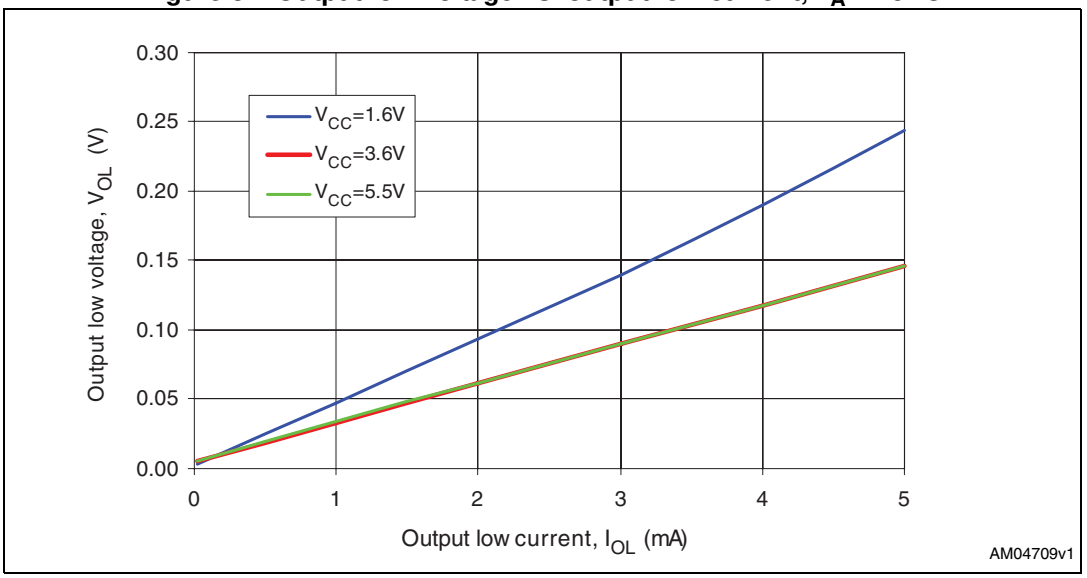
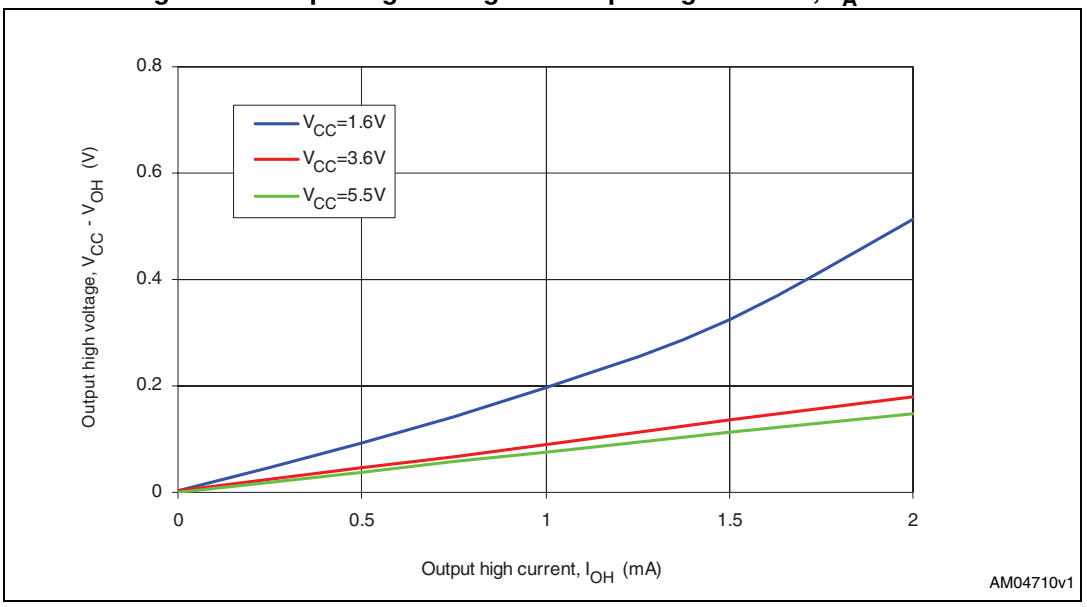


Figure 31. Output low voltage vs. output low current, T_A = 25 °C



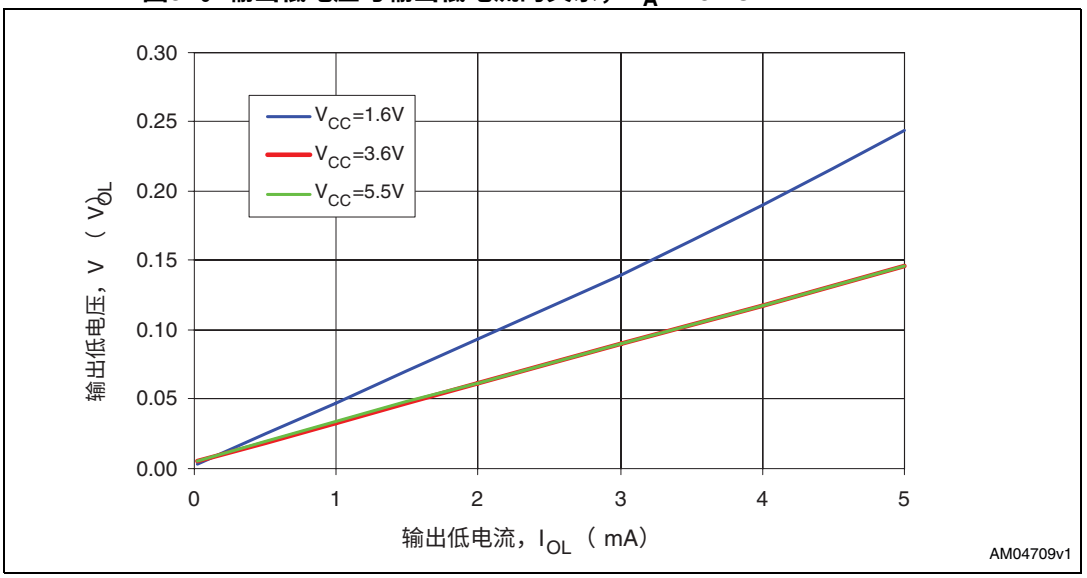
Note: Characteristics valid for all the outputs (EN, $\overline{EN}$, $\overline{RST}$, $\overline{INT}$, $\overline{PB}_{OUT}$ and $\overline{VCC}_{LO}$).

Figure 32. Output high voltage vs. output high current, T_A = 25 °C



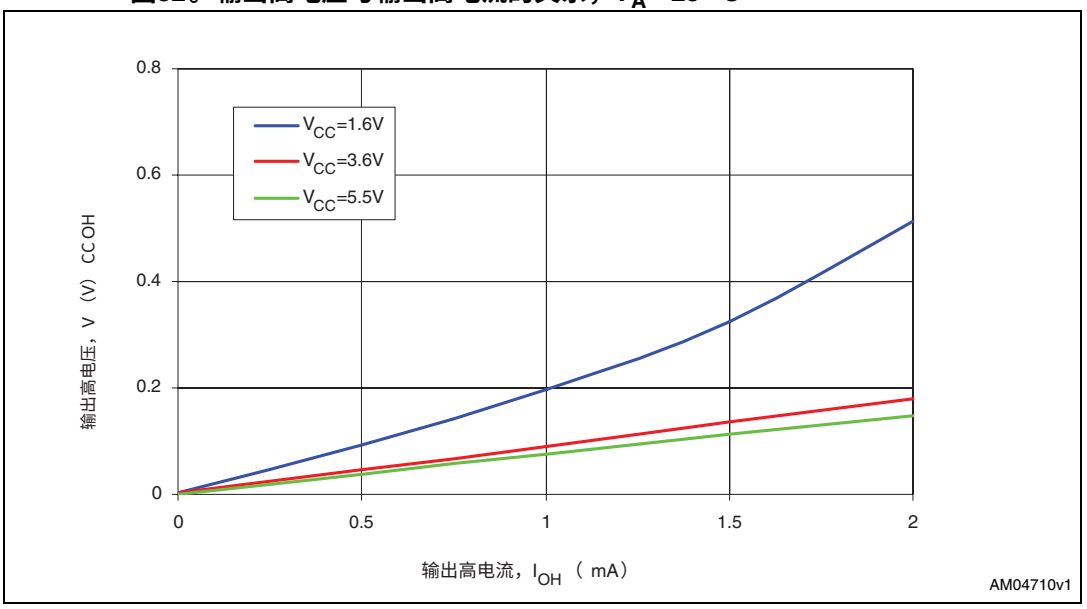
Note: Characteristics valid for EN and $\overline{EN}$ outputs.

图31。输出低电压与输出低电流的关系，T_A= 25 °C



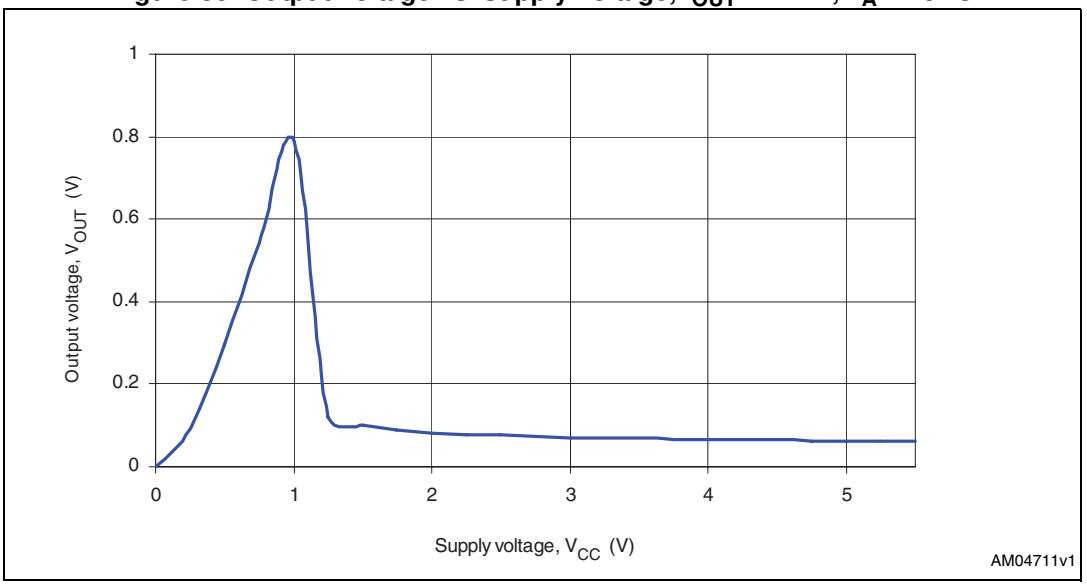
注意： 所有输出（*EN*、*EN*、*RST*、 *INT*、$\overline{PB}_{OUT}$和 $\overline{VCC}_{LO}$）的特性均有效。

图32。输出高电压与输出高电流的关系，T_A= 25 °C



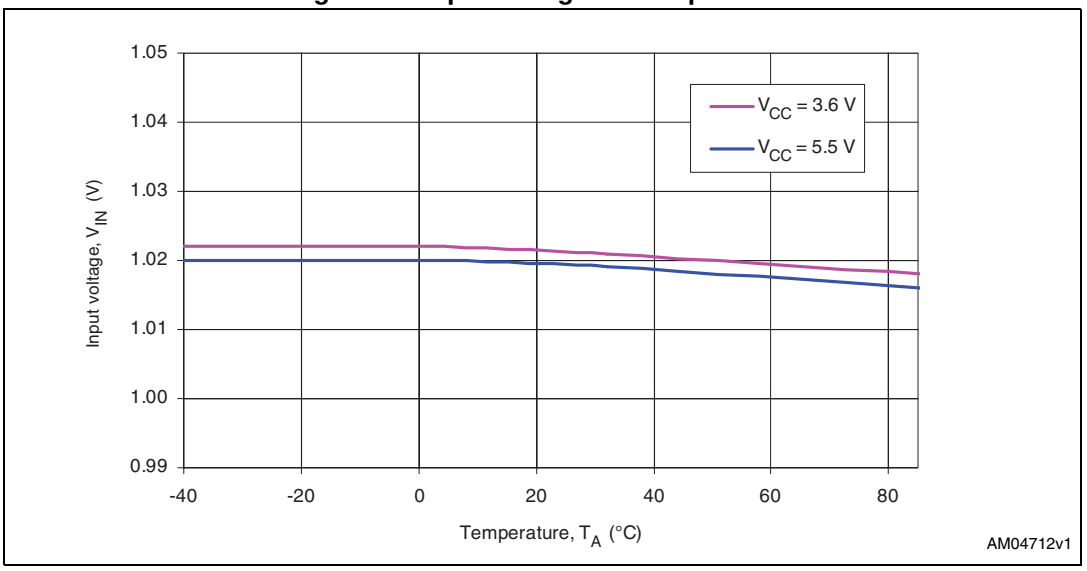
注意： 特性适用于使能输出（*EN*）端口。

Figure 33. Output voltage vs. supply voltage, I_{OUT} = 1 mA, T_A = 25 °C



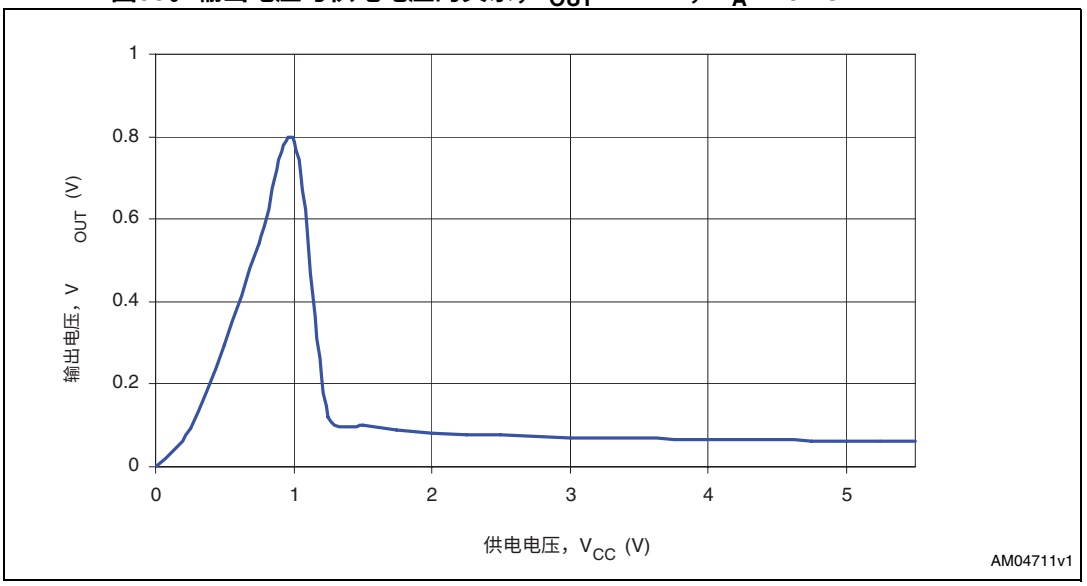
Note: Characteristics valid for all the outputs (EN, $\overline{EN}$, $\overline{RST}$, $\overline{INT}$, $\overline{PB}_{OUT}$ and $\overline{VCC}_{LO}$).

Figure 34. Input voltage vs. temperature



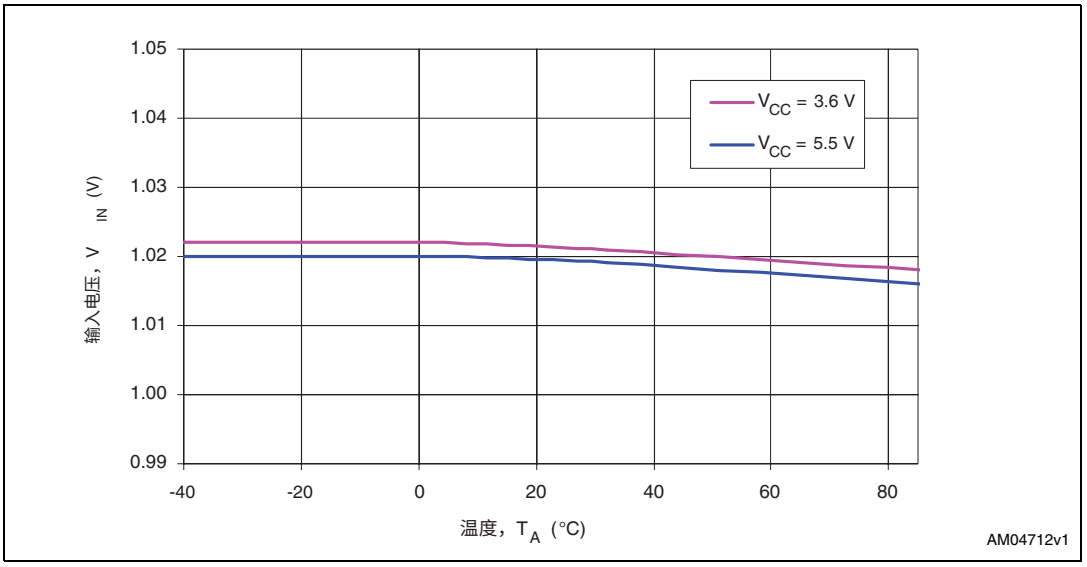
Note: Characteristics valid for $\overline{PB}$, $\overline{SR}$ and PS_{HOLD} inputs.

图33。输出电压与供电电压的关系，I_{OUT}= 1 mA，T_A= 25 °C



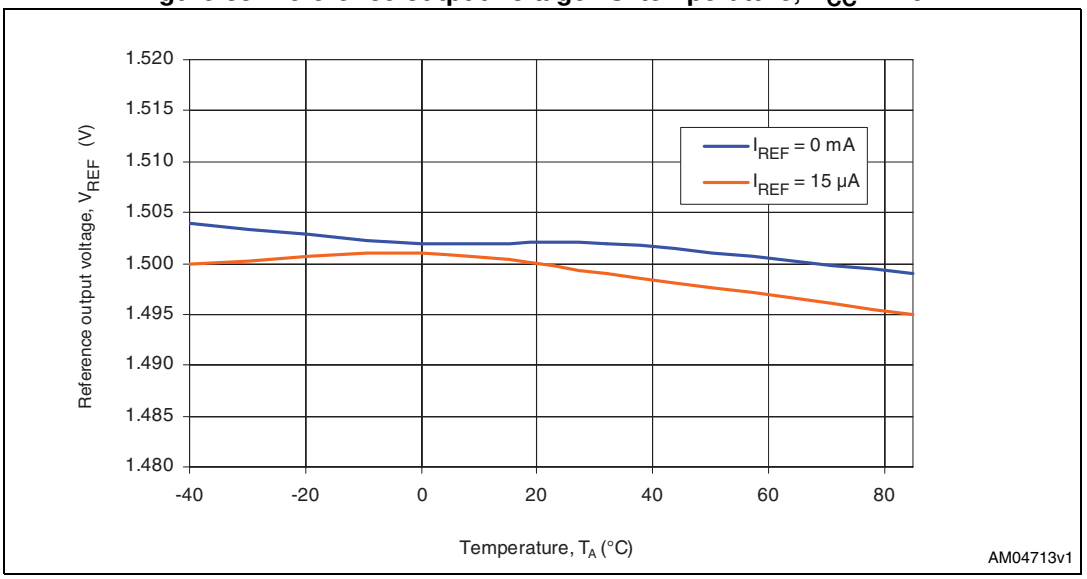
注意： 所有输出（*EN*、*EN*、*RST*、 $\overline{INT}$、$\overline{PB_{OUT}}$和 $\overline{VCC}_{LO}$）的特性均有效。

图34。输入电压与温度的关系



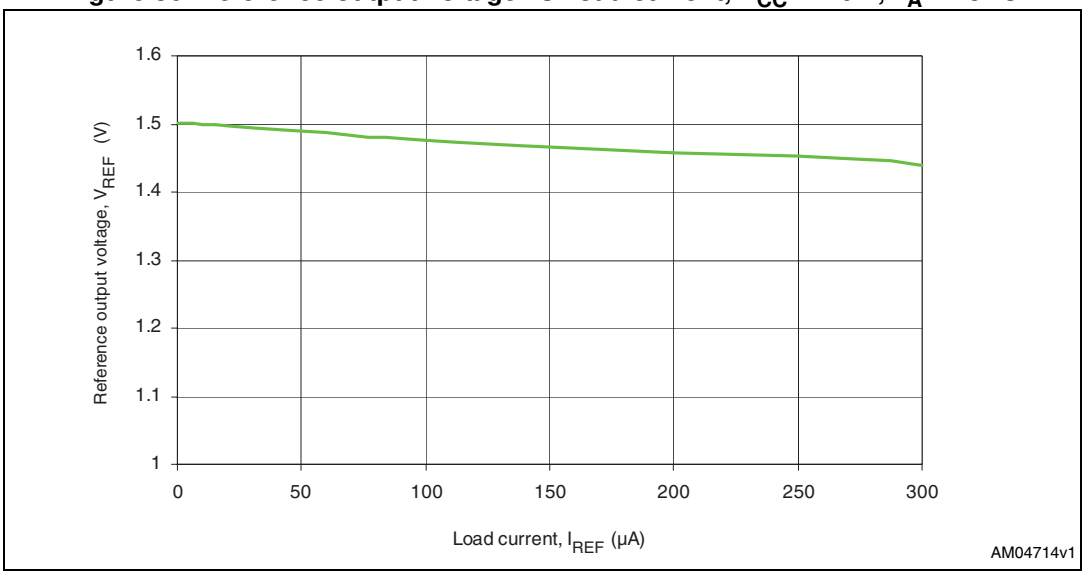
注意： 特性适用于*PB*、*SR*和$\overline{PS_{HOLD}}$输入端。

Figure 35. Reference output voltage vs. temperature, V_{CC} = 2.0 V



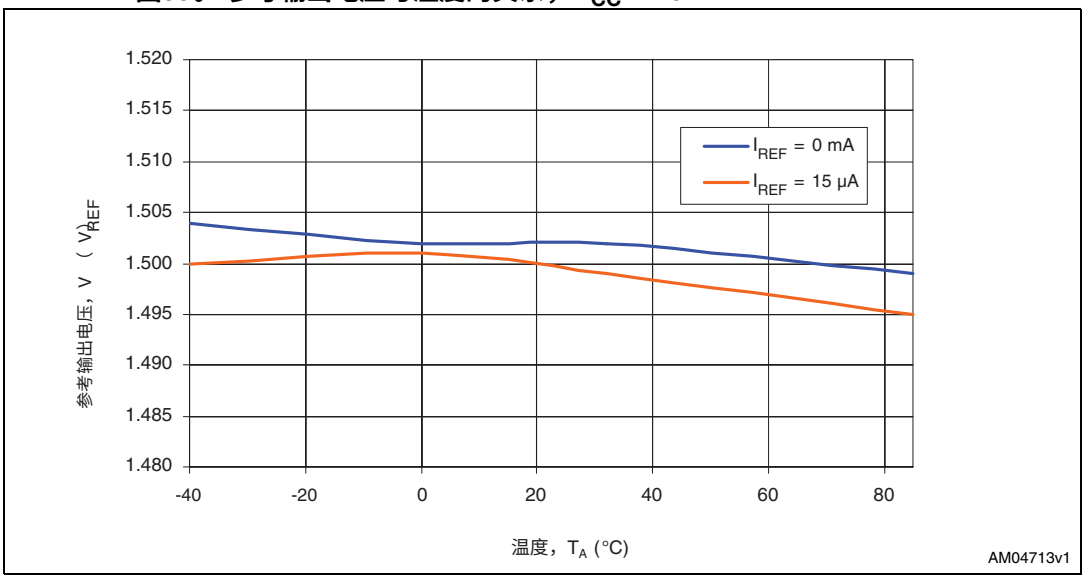
Note: 1 µF capacitor is connected to the V_{REF} pin.

Figure 36. Reference output voltage vs. load current, V_{CC} = 2.0 V, T_A = 25 °C



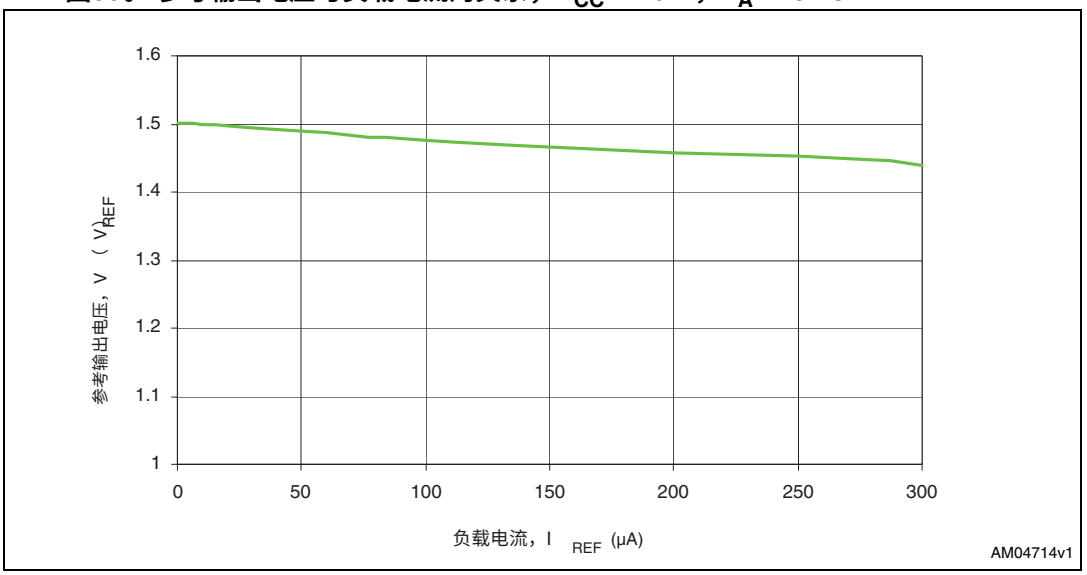
Note: 1 µF capacitor is connected to the V_{REF} pin.

图35。 参考输出电压与温度的关系，V_{CC}= 2.0 V



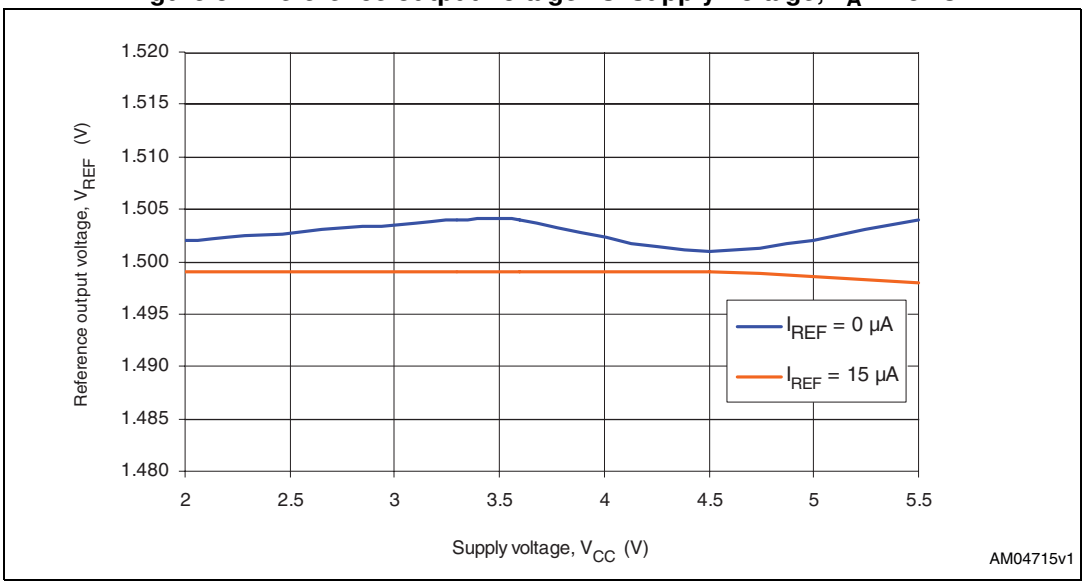
注意： *1 µF* 电容连接至 V_{REF}引脚。

图36。 参考输出电压与负载电流的关系，V_{CC}= 2.0 V，T_A= 25 °C



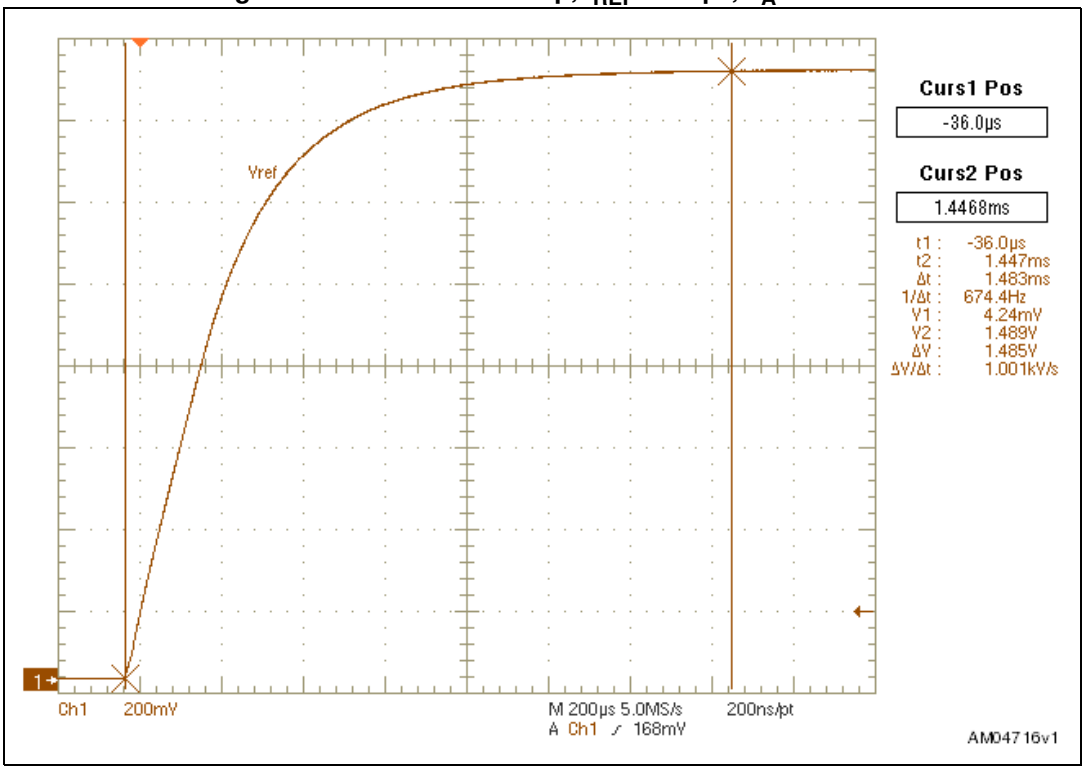
注意： *1 µF* 电容连接至 V_{REF}引脚。

Figure 37. Reference output voltage vs. supply voltage, T_A = 25 °C



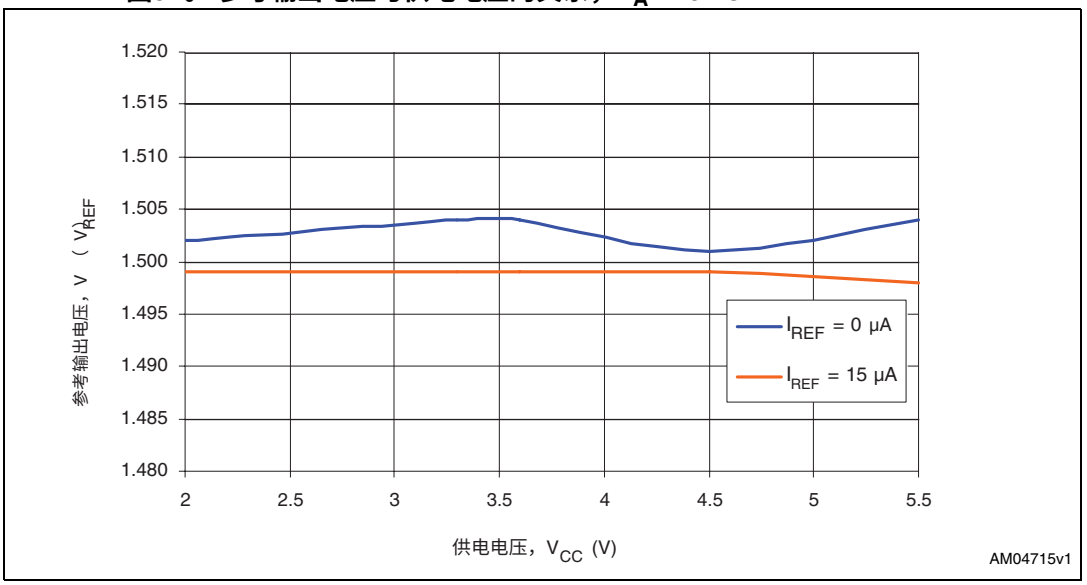
Note: 1 µF capacitor is connected to the V_{REF} pin.

Figure 38. Reference startup, I_{REF} = 15 µF, T_A = 25 °C



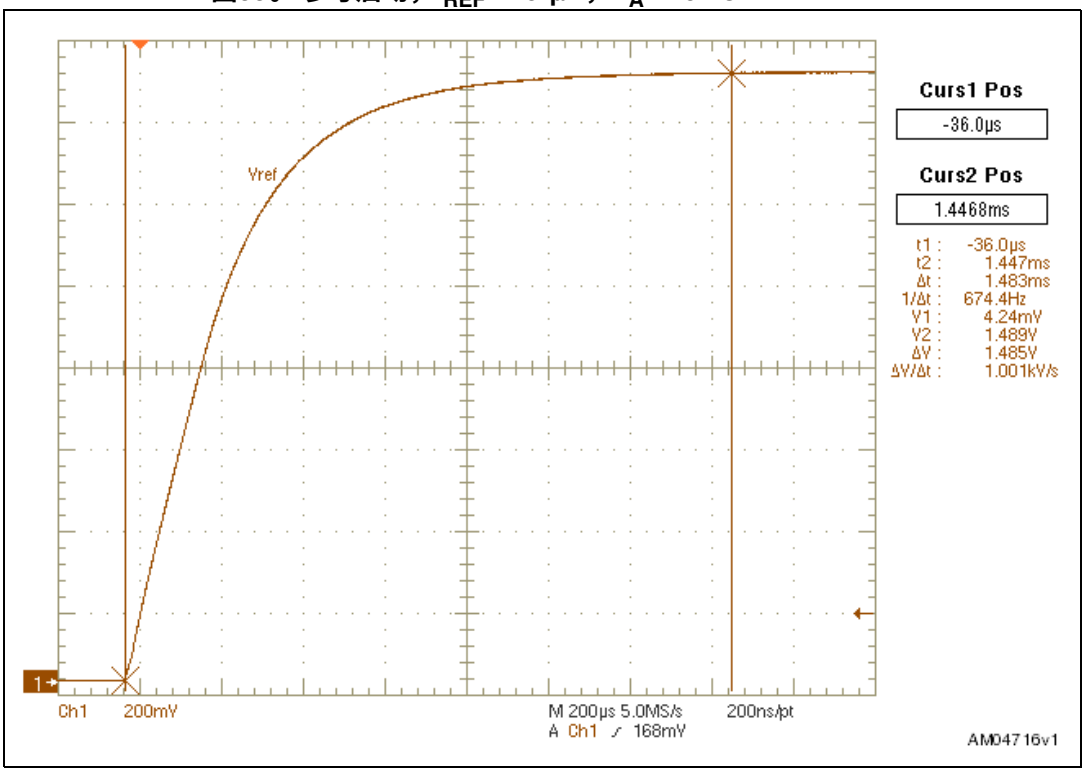
Note: 1 µF capacitor is connected to the V_{REF} pin.

图37。 参考输出电压与供电电压的关系，T_A= 25 °C



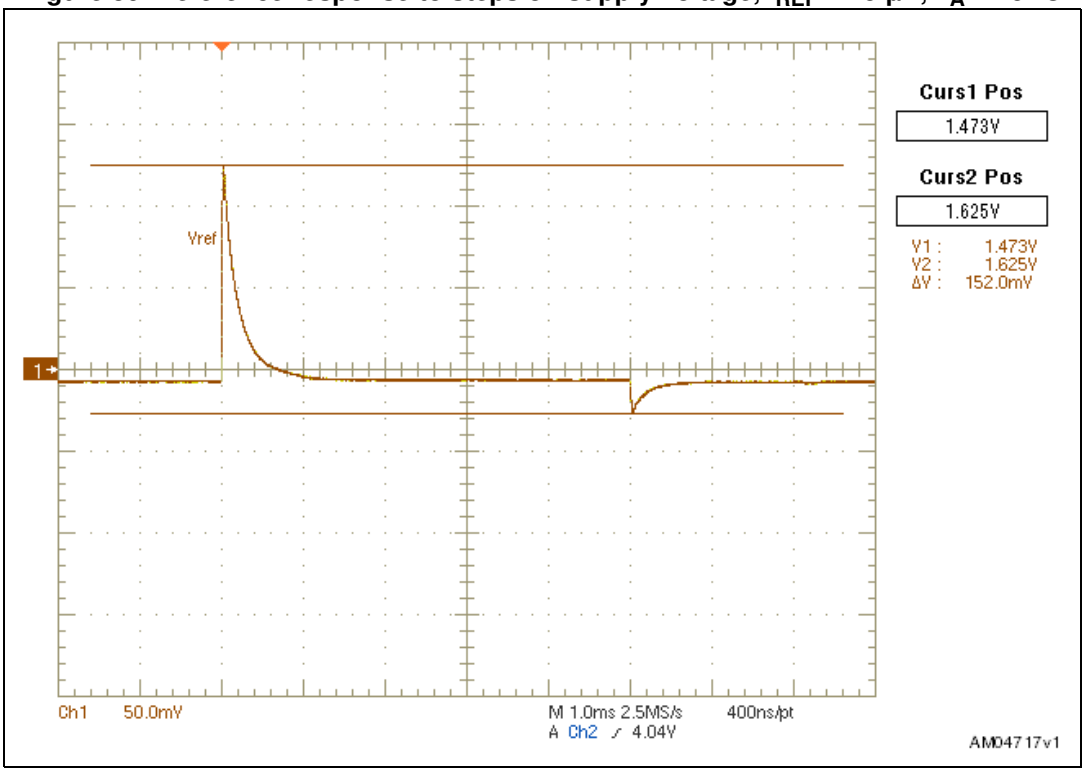
注意： *1 µF* 电容连接至 V_{REF}引脚。

图38。 参考启动，I_{REF}= 15 µF，T_A= 25 °C



注意： *1 µF* 电容连接至 V_{REF}引脚。

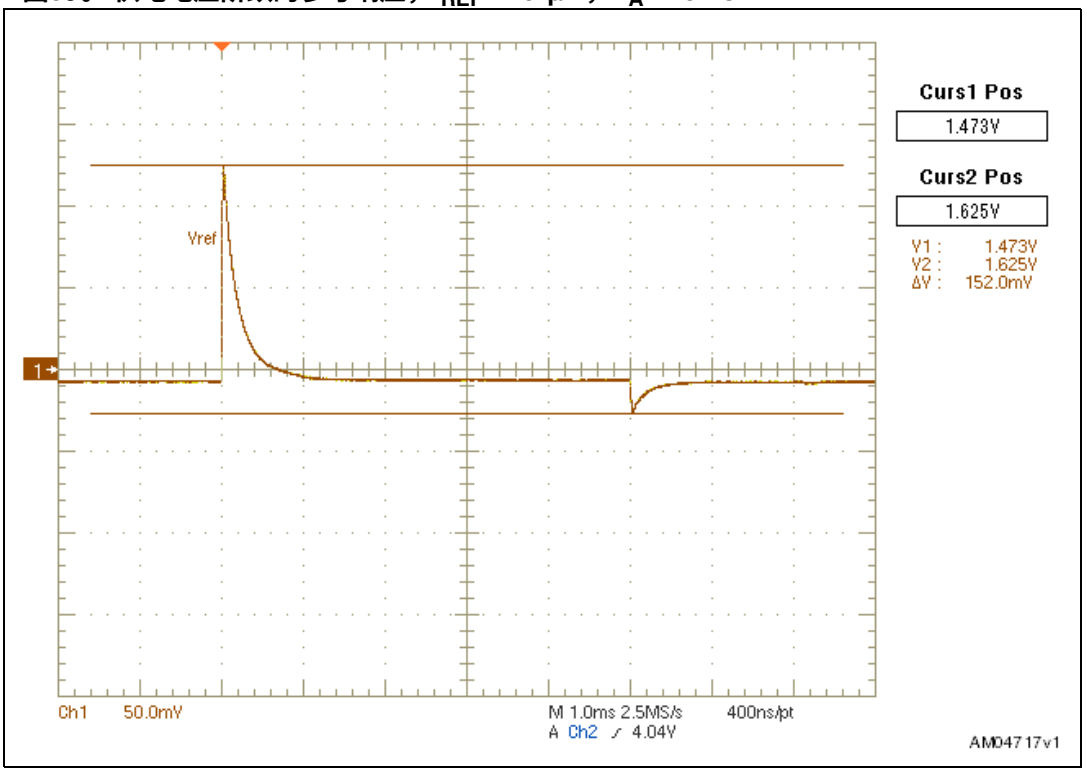
Figure 39. Reference response to steps on supply voltage, I_{REF} = 15 µA, T_A = 25 °C



Note: 1 Supply voltage goes from 3.6 V to 5.5 V and back to 3.6 V, ramp 1 V / 100 ns.

2 1 µF capacitor is connected to the V_{REF} pin.

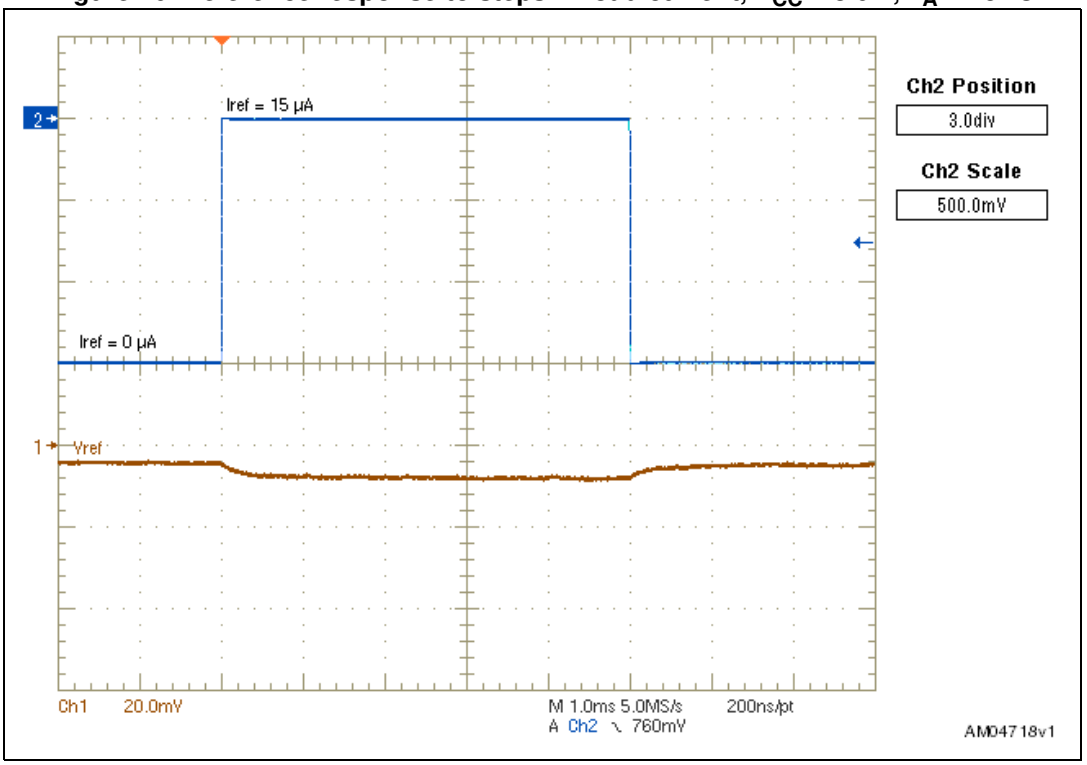
图39。 供电电压阶跃的参考响应，I_{REF}= 15 µA，T_A= 25 °C



注：*1* 供电电压从*3.6 V*升至*5.5 V*，再降至*3.6 V*，斜率为*1 V / 100 ns*。

2 *1 µF* 电容连接至 V_{REF}引脚。

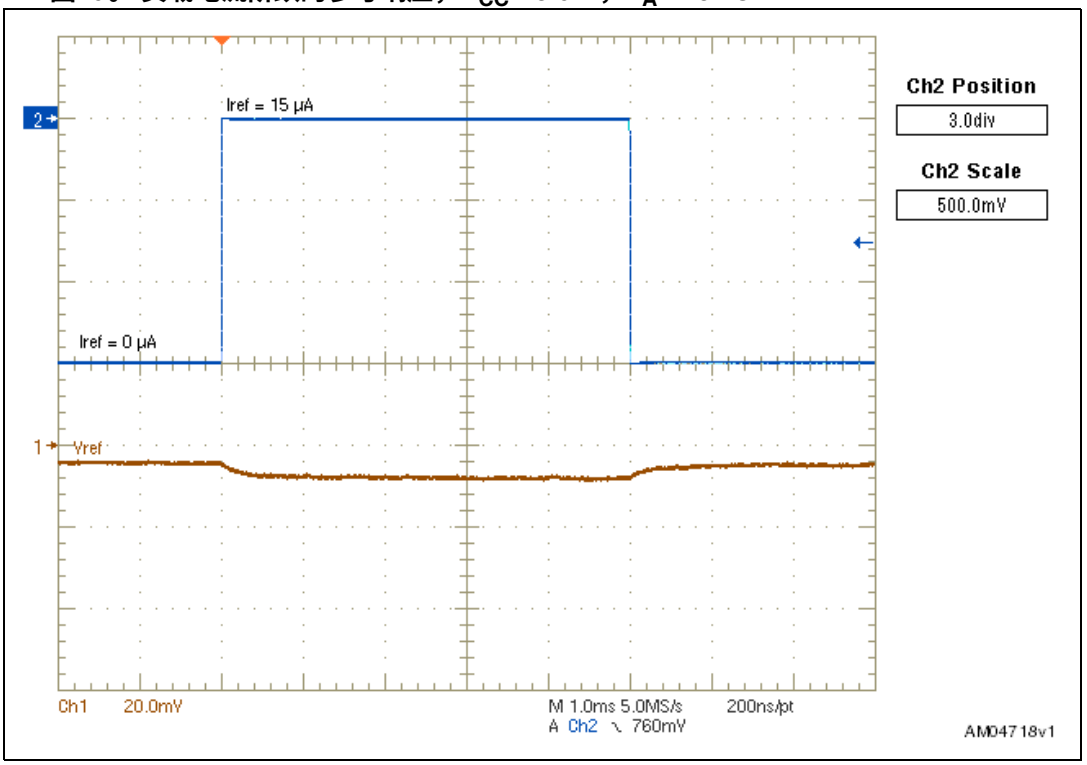
Figure 40. Reference response to steps in load current, V_{CC} = 3.6 V, T_A = 25 °C



Note: 1 Supply voltage goes from 0 µA to 15 µA and back to 0 µA, ramp 1 µA / 100 ns.

2 1 µF capacitor is connected to the V_{REF} pin.

图40。 负载电流阶跃的参考响应，V_{CC}= 3.6 V，T_A= 25 °C



注：*1* 电流从*0 µA*升至*15 µA*，再降至*0 µA*，斜率为*1 µA / 100 ns*。

2 1 µF 电容连接至 V_{REF}引脚。

6 Maximum ratings

Stressing the device above the rating listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Table 4* of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit	Remarks
V_{CC}	Input supply voltage	–0.3	+7.0	V	
	Input voltages on $\overline{PB}$, $\overline{SR}$, PS_{HOLD} and C_{SRD}	–0.3	V_{CC} + 0.3	V	
	Output voltages on EN ($\overline{EN}$), $\overline{RST}$ and $\overline{INT}$	–0.3	V_{CC} + 0.3	V	
V_{ESD}	Electrostatic protection	–2	+2	kV	Human body model (all pins)
		–8	+8	kV	Human body model ($\overline{PB}$ and $\overline{SR}$)
V_{ESD}	Electrostatic protection	–1000	+1000	V	Charged device model
V_{ESD}	Electrostatic protection	–200	+200	V	Machine model
V_{ESD}	Point discharge on $\overline{PB}$ and $\overline{SR}$ inputs	–8	+8	kV	IEC61000-4-2
V_{ESD}	Air discharge on $\overline{PB}$ and $\overline{SR}$ inputs	–15	+15	kV	IEC61000-4-2
T_A	Operating ambient temperature	–40	+85	°C	
T_{STG}	Storage temperature	–45	+150	°C	
T_{SLD} (1)	Lead solder temperature for 10 seconds		+260	°C	
θ_{JA}	Thermal resistance (junction to ambient)		+132.4	°C/W	

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

6 最大额定值

超过表*3*中列出的额定值对器件施加应力可能导致器件永久损坏。这些仅为应力额定值，且不意味着器件可在本规格书表*4*所示或任何其他高于该值的条件下正常工作。长时间暴露于绝对最大额定条件可能影响器件可靠性。

表 3. 绝对最大额定值

符号	参数	最小值	最大值	单位	备注
V_{CC}	输入供电电压	–0.3	+7.0	V	
	PB、SR、PS_{HOLD}及端口输入电压 C_{SRD}	–0.3	V_{CC} + 0.3	V	
	EN（使能）、RST（复位）及中断（INT）端口输出电压	–0.3	V_{CC} + 0.3	V	
V_{ESD}	静电防护	–2	+2	kV	人体模型（所有引脚）
		–8	+8	kV	人体模型（PB 和 SR）
V_{ESD}	静电防护	–1000	+1000	V	带电器件模型
V_{ESD}	静电防护	–200	+200	V	机器模型
V_{ESD}	PB 和 SR 输入端的点放电	–8	+8	kV	IEC61000-4-2
V_{ESD}	PB 和 SR 输入端的空气放电	–15	+15	kV	IEC61000-4-2
T_A	工作环境温度	–40	+85	°C	
T_{STG}	存储温度	–45	+150	°C	
T_{SLD} (1)	引脚焊接温度（10秒）		+260	°C	
θ_{JA}	热阻（结到环境）		+132.4	°C/W	

1. 回流焊峰值温度为260 °C。 高于255 °C的时间不得超过30秒。

7 DC and AC characteristics

This section summarizes the operating measurement conditions and the DC and AC characteristics of the device. The parameters in *Table 5* that follow are derived from tests performed under the measurement conditions summarized in *Table 4*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC measurement conditions

Parameter	Condition	Unit
V_{CC} supply voltage	1.6 to 5.5	V
Ambient operating temperature (T_A)	–40 to 85	°C
Input rise and fall times	≤ 5	ns

Table 5. DC and AC characteristics

Symbol	Parameter	Test condition(1)	Min.	Typ.(2)	Max.	Unit
V_{CC}	Supply voltage		1.6		5.5	V
I_{CC}	Supply current	V_{CC} = 3.6 V, no load		6.0	8.0	µA
		Standby mode, enable deasserted, V_{CC} = 3.6 V		0.6	1.0	µA
V_{TH+}	Power-on lockout voltage (see *Table 10* for detailed listing)		2.40	2.50	2.60	V
			3.00	3.10	3.20	
			3.20	3.30	3.40	
			3.29	3.40	3.51	
			3.39	3.50	3.61	
V_{HYST}	Threshold hysteresis (see *Table 10* for detailed listing)			200		mV
				500		
$V_{TH–}$	Forced power-off voltage (see *Table 10* for detailed listing)			$V_{TH+} – V_{HYST}$		V
$t_{TH–}$	Undervoltage detection to $\overline{INT}$ delay	$V_{CC} \geq 2.0$ V	20	32	44	ms
t_{ON_BLANK}	Blanking period (see *Table 10* for detailed listing)(3)		1.4	2.2	3.0	s
			5.6	8.8	12.0	
			11.2	17.6	24.0	
	$\overline{RST}$ assertion to EN ($\overline{EN}$) assertion delay during power-up	V_{CC} = 3.6 V		100		ns
$\overline{PB}$						
V_{IL}	Input low voltage	$V_{CC} \geq 2.0$ V, enable asserted			0.99	V
V_{IH}	Input high voltage	$V_{CC} \geq 2.0$ V, enable asserted	1.05			V

7 直流和交流特性

本节总结了器件的工作测量条件及其直流和交流特性。下列表*5*中的参数均基于表*4*中总结的测量条件下的测试结果。设计人员应确认其电路中的工作条件与所引用参数的工作条件相符。

表4. 工作及交流测量条件

参数	条件	单位
V_{CC} 供电电压	1.6 至 5.5	V
环境工作温度（T_A）	–40 至 85	°C
输入上升和下降时间	≤ _ 5	纳秒

表5. 直流和交流特性

符号	参数	测试条件(1)	最小值	典型值(2)	最大值	单位
V_{CC}	供电电压		1.6		5.5	V
I_{CC}	供电电流	V_{CC} = 3.6 V，无负载		6.0	8.0	微安
		待机模式，启用 取消使能，V_{CC} = 3.6 V		0.6	1.0	微安
V_{TH+}	上电锁定电压（详见表格 *10*）		2.40	2.50	2.60	V
			3.00	3.10	3.20	
			3.20	3.30	3.40	
			3.29	3.40	3.51	
			3.39	3.50	3.61	
V_{HYST}	阈值滞后（详见表*10*）			200		mV
				500		
$V_{TH–}$	强制断电电压（详见表*10*）			$V_{TH+} – V_{HYST}$		V
$t_{TH–}$	欠压检测至中断的延迟	V_{CC} ≥ 2.0 V	20	32	44	毫秒
$t_{开机空白}$	消隐期（详见表*10*）（3）		1.4	2.2	3.0	秒
			5.6	8.8	12.0	
			11.2	17.6	24.0	
	上电期间RST断言至EN（使能）断言的延迟	V_{CC} = 3.6 V		100		纳秒
PB						
V_{IL}	输入低电压	V_{CC} ≥ 2.0 V，已断言使能			0.99	V
V_{IH}	输入高电压	V_{CC} ≥ 2.0 V，已断言使能	1.05			V

Table 5. DC and AC characteristics (continued)

Symbol	Parameter	Test condition(1)	Min.	Typ.(2)	Max.	Unit
$t_{DEBOUNCE}$	Debounce period	$V_{CC} \geq 2.0$ V	20	32	44	ms
$R_{\overline{PB}}$	Internal pull-up resistor	V_{CC} = 5.5 V, input asserted	65	100	135	kΩ
$\overline{SR}$						
V_{IL}	Input low voltage				0.99	V
V_{IH}	Input high voltage		1.05			V
$t_{DEBOUNCE}$	Debounce period		20	32	44	ms
$R_{\overline{SR}}$(4)	Internal pull-up resistor	V_{CC} = 5.5 V, input asserted	65	100	135	kΩ
$\overline{PB}_{OUT}$						
V_{OL}	Output low voltage	V_{CC} = 2 V, I_{SINK} = 1 mA, $\overline{PB}_{OUT}$ asserted			0.3	V
	$\overline{PB}_{OUT}$ leakage current	$V_{\overline{PBOUT}}$ = 3 V, $\overline{PB}_{OUT}$ open drain	–0.1		+0.1	µA
$\overline{VCC}_{LO}$						
V_{OL}	Output low voltage	V_{CC} = 2 V, I_{SINK} = 1 mA, $\overline{VCC}_{LO}$ asserted			0.3	V
	$\overline{VCC}_{LO}$ leakage current	$V_{\overline{VCCLO}}$ = 3 V, $\overline{VCC}_{LO}$ open drain	–0.1		+0.1	µA
PS_{HOLD}						
V_{IL}	Input low voltage	$V_{CC} \geq 2.0$ V			0.99	V
V_{IH}	Input high voltage	$V_{CC} \geq 2.0$ V	1.05			V
	Glitch immunity		1	80		µs
	PS_{HOLD} leakage current	V_{PSHOLD} = 0.6 V	–0.1		0.1	µA
	PS_{HOLD} to enable propagation delay				30	µs
R_{PSHOLD}	Pull-down resistor connected internally during power-up	V_{PSHOLD} = 5.5 V	195	300	405	kΩ
C_{SRD}						
I_{SRD}	C_{SRD} charging current		100	150	200	nA
V_{SRD}	C_{SRD} voltage threshold	V_{CC} = 3.6 V, load on V_{REF} pin 100 kΩ and mandatory 1 µF capacitor, T_A = 25 °C		1.5		V
t_{SRD}	Additional Smart Reset™ delay time	External C_{SRD} connected		10		s/µF
EN, $\overline{EN}$						
V_{OL}	Output low voltage	V_{CC} = 2 V, I_{SINK} = 1 mA, enable asserted			0.3	V

表5. 直流和交流特性（续）

符号	参数	测试条件(1)	最小值	典型值(2)	最大值	单位
$t_{消抖E}$	消抖期	$V_{CC} \geq 2.0$ V	20	32	44	毫秒
$R_{\overline{PB}}$	内部上拉电阻	V_{CC} = 5.5 V，输入有效	65	100	135	kΩ
$\overline{SR}$						
V_{IL}	输入低电压				0.99	V
V_{IH}	输入高电压		1.05			V
$t_{消抖E}$	消抖期		20	32	44	毫秒
$R_{\overline{SR}}$(4)	内部上拉电阻	V_{CC} = 5.5 V，输入有效	65	100	135	kΩ
$\overline{PB}_{OUT}$						
V_{OL}	输出低电压	V_{CC} = 2 V, I_{SINK} = 1 mA, $\overline{PB}_{OUT}$ 有效			0.3	V
	$\overline{PB}_{OUT}$ 漏电流	$V_{\overline{PBOUT}}$= 3 V，$\overline{PB}_{OUT}$开漏	–0.1		+0.1	微安
$\overline{VCC}_{LO}$						
V_{OL}	输出低电压	V_{CC} = 2 V, I_{SINK} = 1 mA, $\overline{VCC}_{LO}$ 有效			0.3	V
	$\overline{VCC}_{LO}$ 漏电流	$V_{\overline{VCCLO}}$ = 3 V, $\overline{VCC}_{LO}$ 开漏漏极	–0.1		+0.1	微安
电源保持						
V_{IL}	输入低电压	$V_{CC} \geq 2.0$ V			0.99	V
V_{IH}	输入高电压	$V_{CC} \geq 2.0$ V	1.05			V
	抗干扰能力		1	80		µs
	PS_{HOLD} 漏电流	V_{PSHOLD} = 0.6 V	–0.1		0.1	微安
	PS_{HOLD}使能传播延迟				30	µs
R_{PSHOLD}	上电期间内部连接下拉电阻	V_{PSHOLD} = 5.5 V	195	300	405	kΩ
C_{SRD}						
I_{SRD}	C_{SRD} 充电电流		100	150	200	nA
V_{SRD}	C_{SRD} 电压阈值	V_{CC} = 3.6 V，V_{REF}引脚负载100 kΩ及必需的1 µF电容，T_A= 25 °C		1.5		V
t_{SRD}	额外Smart Reset™延迟时间	外部连接C_{SRD}		10		秒/µF
EN, $\overline{EN}$						
V_{OL}	输出低电压	V_{CC}= 2 V，I_{SINK}= 1 mA，启用有效			0.3	V

Table 5. DC and AC characteristics (continued)

Symbol	Parameter	Test condition(1)	Min.	Typ.(2)	Max.	Unit
V_{OH}(5)	Output high voltage	V_{CC} = 2 V, I_{SOURCE} = 1 mA, enable asserted	V_{CC} – 0.3			V
t_{EN_OFF}(6)	enable off to enable on	$V_{CC} \geq 2.0$ V	40	64	88	ms
	EN, $\overline{EN}$ leakage current	V_{EN} = 2 V, enable open drain	–0.1		+0.1	µA
$\overline{RST}$						
V_{OL}	Output low voltage	V_{CC} = 2 V, I_{SINK} = 1 mA, $\overline{RST}$ asserted			0.3	V
t_{REC}	$\overline{RST}$ pulse width	$V_{CC} \geq 2.0$ V	240	360	480	ms
	$\overline{RST}$ leakage current	$V_{\overline{RST}}$ = 3V	–0.1		+0.1	µA
$\overline{INT}$						
V_{OL}	Output low voltage	V_{CC} = 2 V, I_{SINK} = 1 mA, $\overline{INT}$ asserted			0.3	V
$t_{\overline{INT}\_Min}$	Minimum $\overline{INT}$ pulse width	$V_{CC} \geq 2.0$ V	20	32	44	ms
	$\overline{INT}$ leakage current	$V_{\overline{INT}}$ = 3 V	–0.1		+0.1	µA
V_{REF}						
V_{REF}	1.5 V voltage reference	V_{CC} = 3.6 V, load on V_{REF} pin 100 kΩ and mandatory 1 µF capacitor, T_A = 25 °C	1.485 –1%	1.5	1.515 +1%	V

1. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 1.6 V to 5.5 V (except where noted).
2. Typical values are at T_A = +25 °C.
3. This blanking time allows the processor to start up correctly (see *Figure 7*, *8*, *9*, *10*, *11*, *12*).
4. The internal pull-up resistor connected to the $\overline{SR}$ input is optional (see *Table 10* for detailed device options).
5. Valid for push-pull only.
6. Minimum delay time between enable deassertion and enable reassertion, allowing the application to complete the power-down properly. PB is ignored during this period.

表5. 直流和交流特性（续）

符号	参数	测试条件(1)	最小值	典型值(2)	最大值	单位
V_{OH}(5)	输出高电压	V_{CC}= 2 V，I_{SOURCE}= 1 mA，启用有效	V_{CC} – 0.3			V
t_{EN_OFF}(6)	使能关闭至使能开启	V_{CC} ≥ 2.0 V	40	64	88	毫秒
	EN，$\overline{EN}$ 漏电流	V_{EN} = 2 V，使能开漏	–0.1		+0.1	微安
$\overline{RST}$						
V_{OL}	输出低电压	V_{CC} = 2 V, I_{SINK} = 1 mA, $\overline{RST}$ 置位			0.3	V
$t_{恢复}$	$\overline{RST}$ 脉冲宽度	V_{CC} ≥ 2.0 V	240	360	480	毫秒
	$\overline{RST}$ 漏电流	$V_{\overline{RST}}$ = 3V	–0.1		+0.1	微安
$\overline{中断}$						
V_{OL}	输出低电压	V_{CC} = 2 V, I_{SINK} = 1 mA, $\overline{INT}$ 置位			0.3	V
$t_{\overline{最小中断时间}}$	最小 INT $\overline{脉冲}$宽度	V_{CC} ≥ 2.0 V	20	32	44	毫秒
	$\overline{INT}$ 漏电流	$V_{\overline{INT}}$ = 3 V	–0.1		+0.1	微安
V_{REF}						
V_{REF}	1.5 V 电压基准	V_{CC} = 3.6 V，V_{REF}引脚负载 100 kΩ及必需的1 µF电容，T_A= 25 °C	1.485 –1%	1.5	1.515 +1%	V

1. 适用于环境工作温度：T_A= –40 至 85 °C； V_{CC}= 1.6 V 至 5.5 V（除非另有说明）。
2. 典型值在 T_A= +25 °C 时测得。
3. 此空白时间允许处理器正确启动（见图 *7*， *8*, *9*, *10*, *11*, *12*).
4. 连接到SR 输入端的内部上拉电阻为可选（详见表格*10*中的器件选项）。
5. 仅适用于推挽输出。
6. 使能取消与使能重新使能之间的最小延迟时间，允许应用正确完成断电过程。在此期间，PB信号被忽略。

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

8 封装机械数据

为满足环境要求，ST根据环境合规等级提供不同等级的ECOPACK封装器件。ECOPACK规格、等级定义及产品状态详见： *www.st.com*。

ECOPACK为ST商标。

Figure 41. TDFN12 (2 x 3 mm) package outline

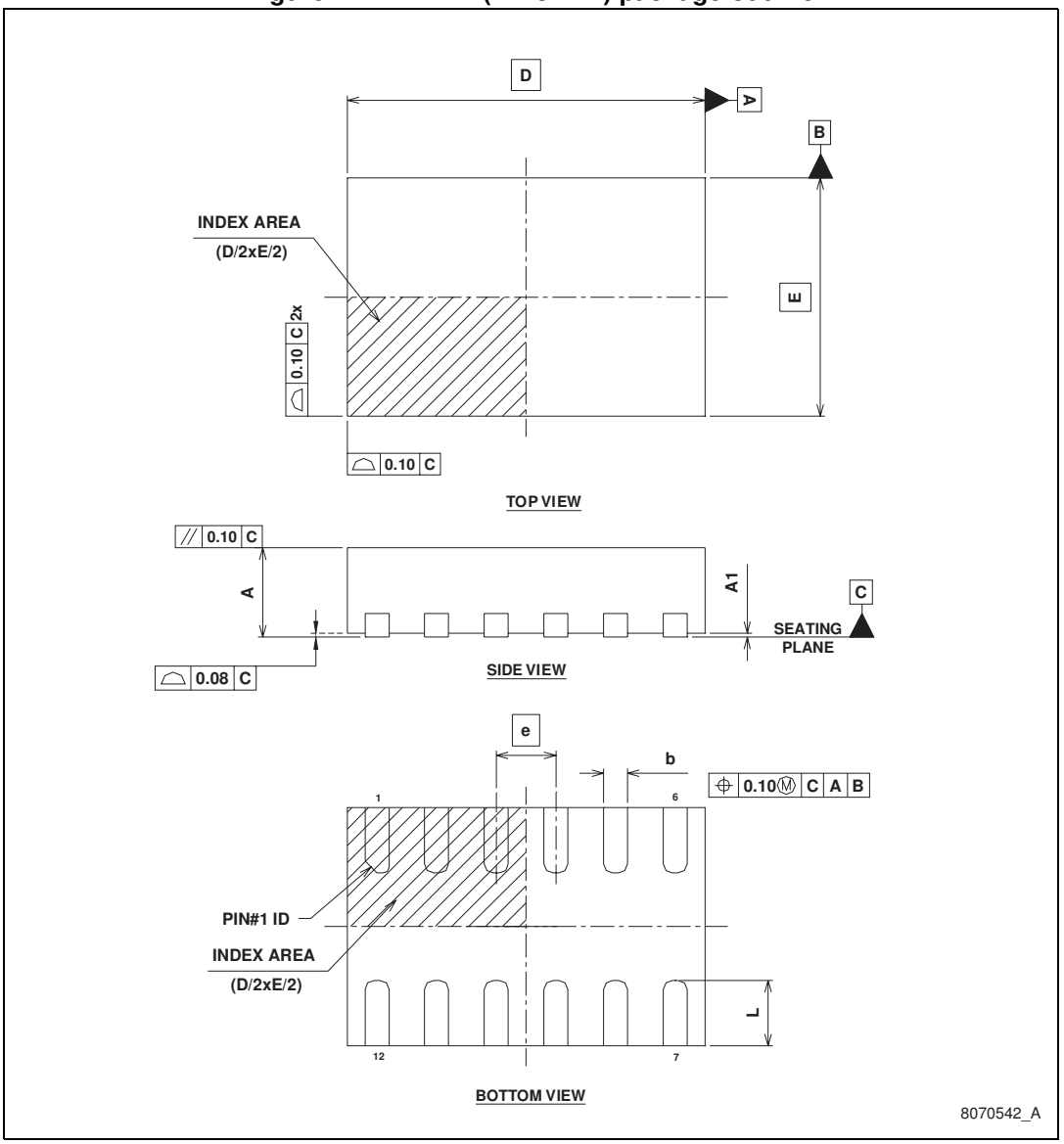


Table 6. TDFN12 (2 x 3 mm) package mechanical data

Symbol	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D		3.00 BSC			0.118	
E		2.00 BSC			0.079	
e		0.50			0.020	
L	0.45	0.55	0.65	0.018	0.022	0.026

图41。 TDFN12（2 x 3 毫米）封装轮廓

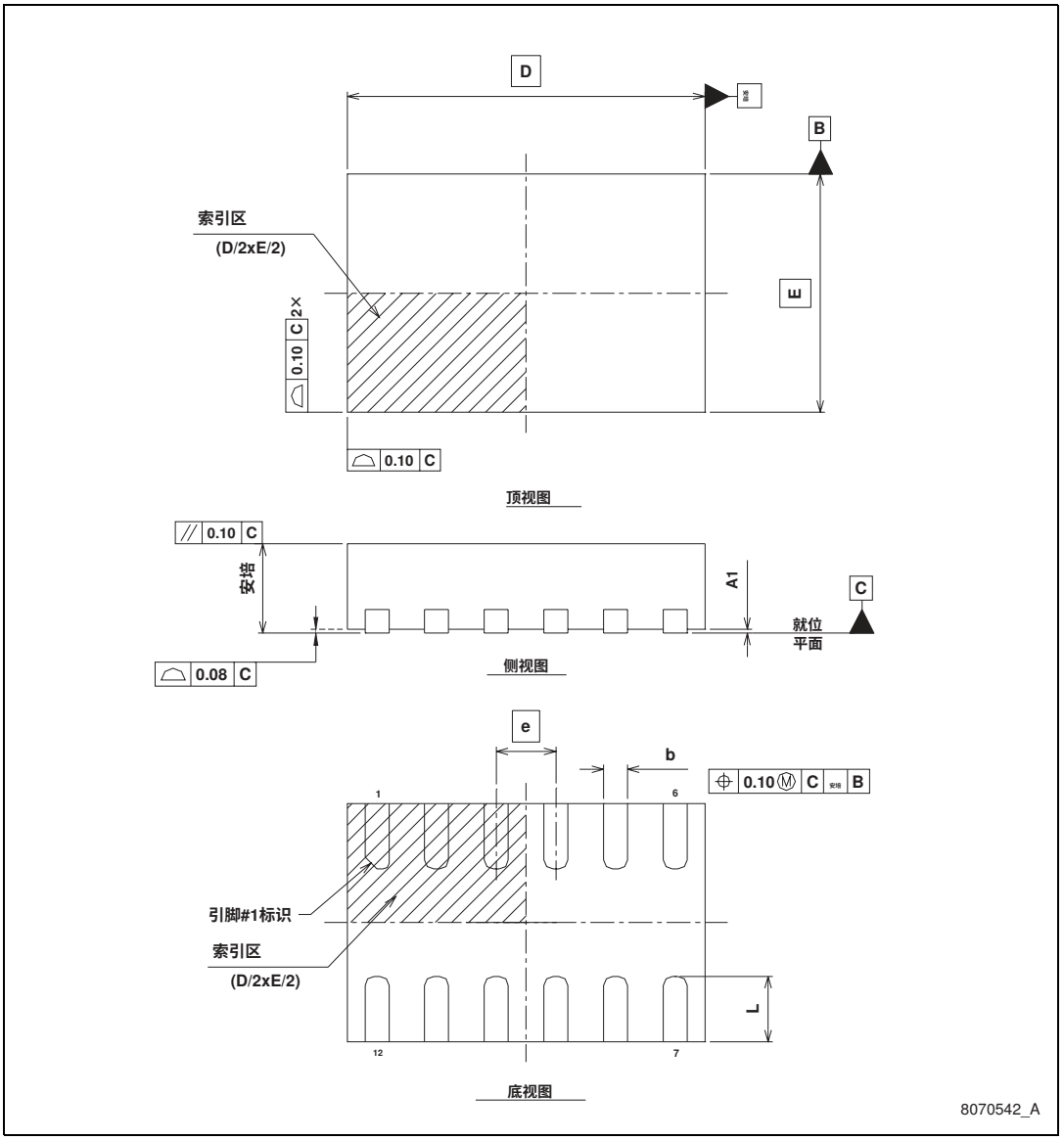
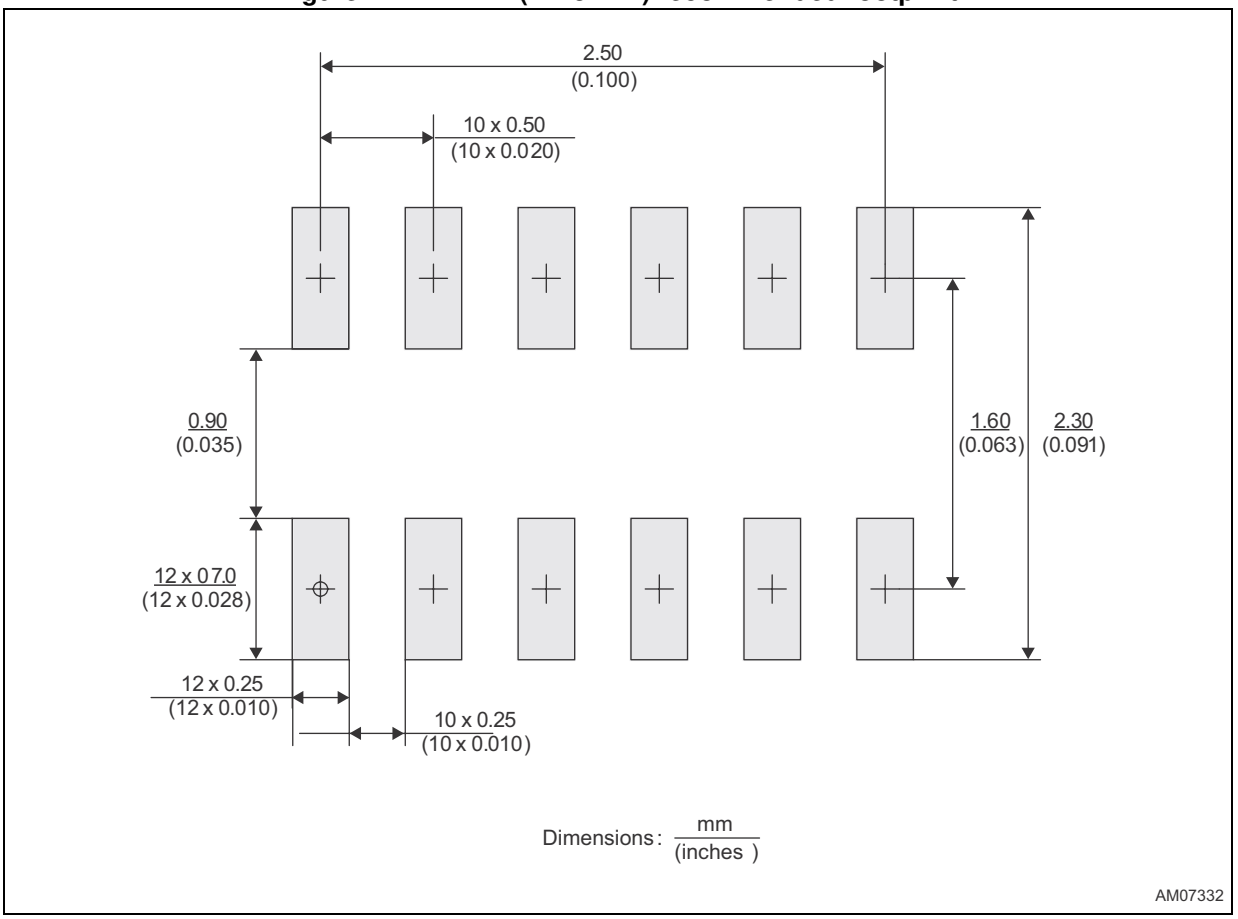


表6. TDFN12（2 x 3 mm）封装机械数据

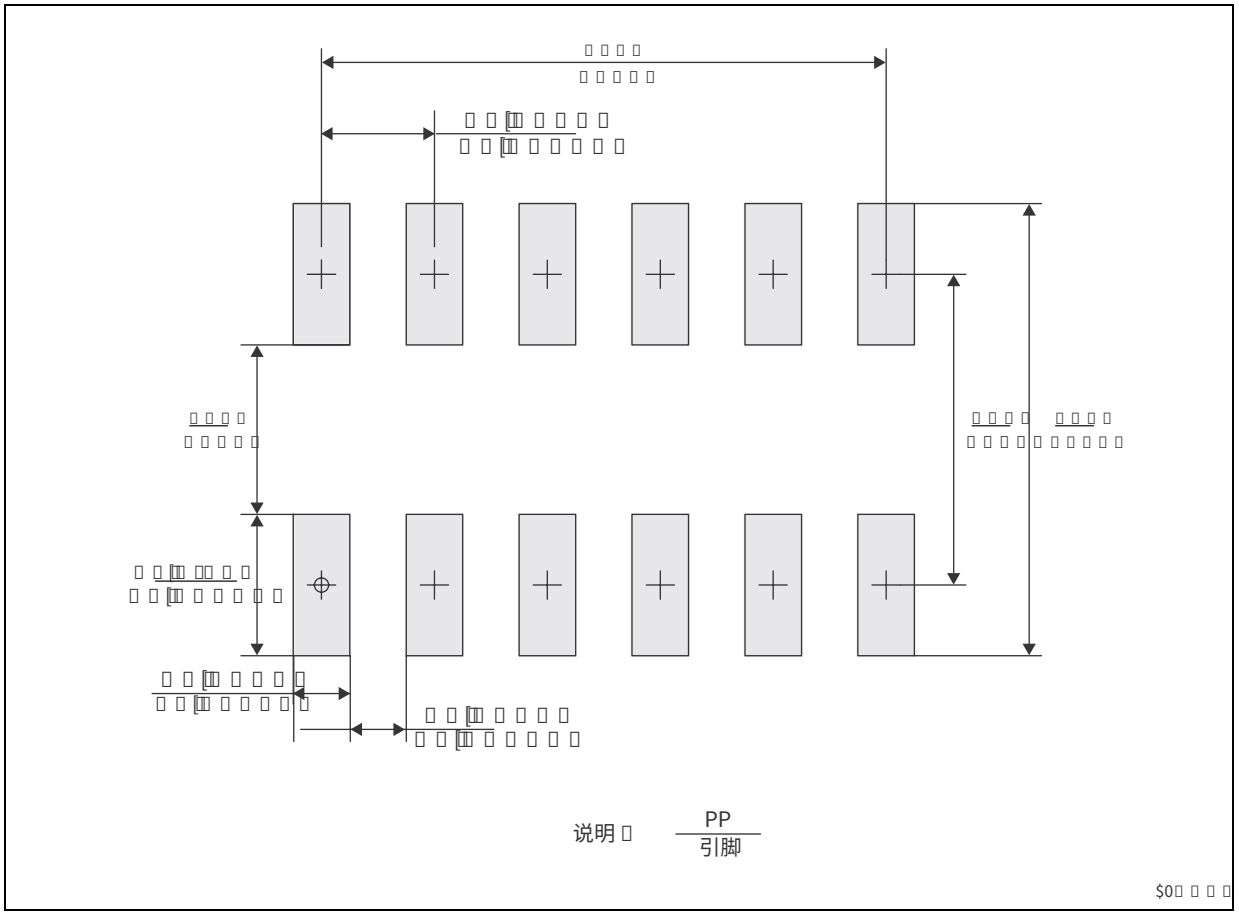
符号	毫米			英寸		
	最小值	典型值	最大值	最小值	典型值	最大值
安培	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D		3.00 基准尺寸			0.118	
E		2.00 基准尺寸			0.079	
e		0.50			0.020	
L	0.45	0.55	0.65	0.018	0.022	0.026

Figure 42. TDFN12 (2 x 3 mm) recommended footprint



Note: Drawing not to scale.

图42。 TDFN12（2 x 3 毫米）推荐焊盘尺寸



注意： 图纸非按比例绘制。

Figure 43. Carrier tape for TDFN12 (2 x 3 mm) package

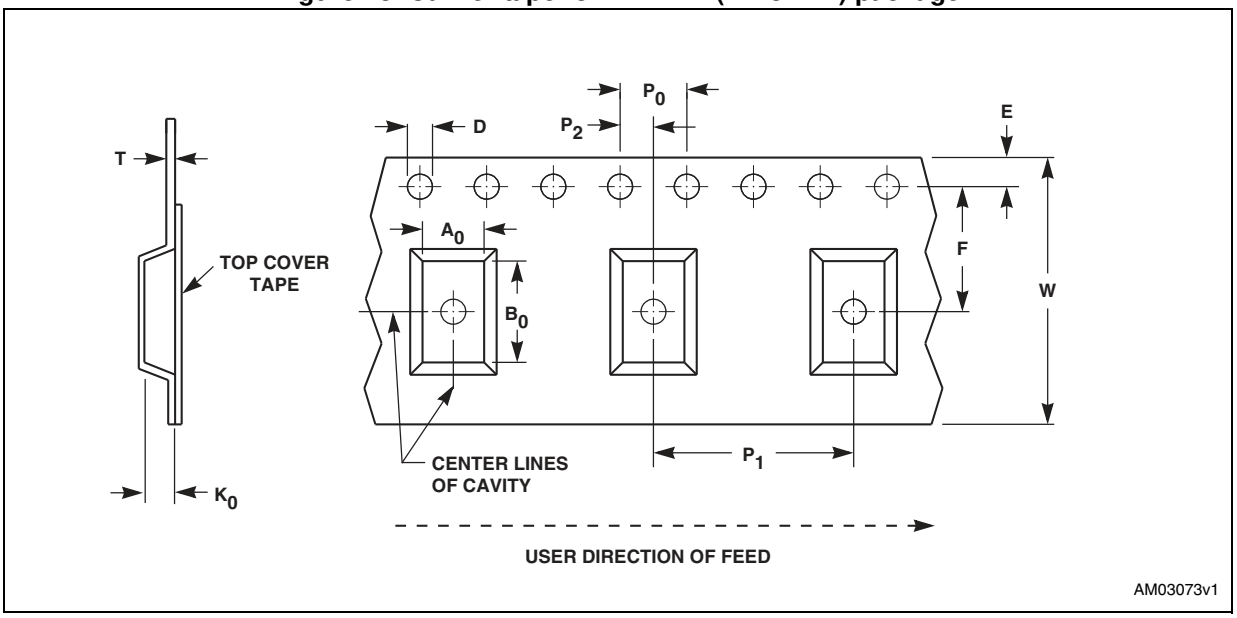


Table 7. Carrier tape dimensions for TDFN12 (2 x 3 mm) package

Package	W	D	E	P_0	P_2	F	A_0	B_0	K_0	P_1	T	Unit	Bulk qty.
TDFN12	12.00 ±0.30	1.50 +0.10/ –0.00	1.75 ±0.10	4.00 ±0.10	2.00 ±0.10	5.50 ±0.05	2.30 ±0.10	3.20 ±0.10	1.10 ±0.01	4.00 ±0.10	0.30 ±0.05	mm	3000

图43。 TDFN12（2 x 3 毫米）封装载带

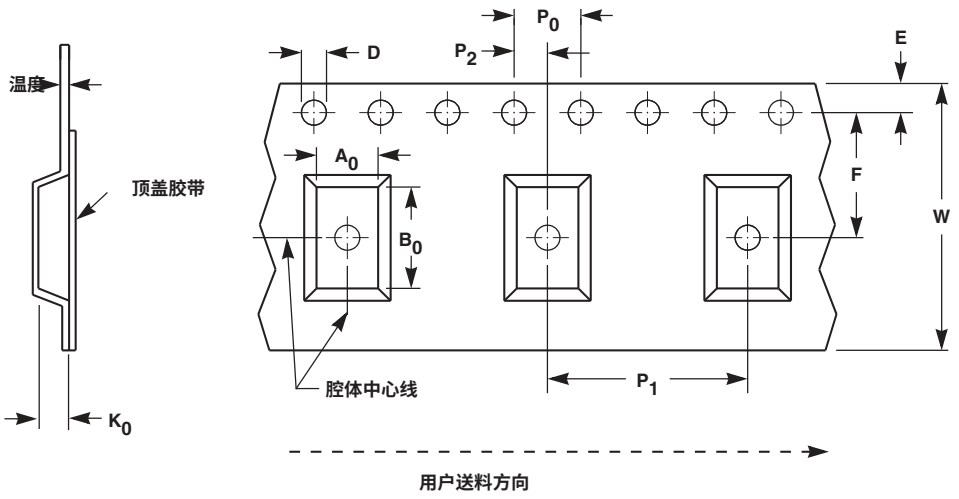


表7. TDFN12封装（2 × 3 毫米）载带尺寸

封装	W	D	E	P_0	P_2	F	A_0	B_0	K_0	P_1	温度	单位	散装数量
TDFN12封装	12.00 ±0.30	1.50 +0.10/ –0.00	1.75 ±0.10	4.00 ±0.10	2.00 ±0.10	5.50 ±0.05	2.30 ±0.10	3.20 ±0.10	1.10 ±0.01	4.00 ±0.10	0.30 ±0.05	毫米	3000

9 Part numbering

Table 8. STM6600 ordering information scheme

Example: **STM660 0 F Q 2 4 DM 6 F**

Device type

STM660

Startup process

0: $\overline{PB}$ must be held low until the PS_{HOLD} confirmation

Input and output types(1)

A: active high EN output, long push asserts $\overline{RST}$, pull-up on $\overline{SR}$

B: active low $\overline{EN}$ output, long push asserts $\overline{RST}$, pull-up on $\overline{SR}$

C: active high EN output, long push deasserts EN, pull-up on $\overline{SR}$

D: active low $\overline{EN}$ output, long push deasserts $\overline{EN}$, pull-up on $\overline{SR}$

E: active high EN output, long push asserts $\overline{RST}$, no resistor on $\overline{SR}$

F: active low $\overline{EN}$ output, long push asserts $\overline{RST}$, no resistor on $\overline{SR}$

G: active high EN output, long push deasserts EN, no resistor on $\overline{SR}$

H: active low $\overline{EN}$ output, long push deasserts $\overline{EN}$, no resistor on $\overline{SR}$

V_{TH+} threshold voltage(1)

A: 2.50 V

Q: 3.30 V

S: 3.40 V

U: 3.50 V

V_{HYST} voltage hysteresis(1)

2: 200 mV

5: 500 mV

t_{ON_BLANK} blanking period(1)

2: 1.4 s (min.)

4: 5.6 s (min.)

5: 11.2 s (min.)

9 零件编号

表8. STM6600 订购信息方案

示例：**STM660 0 F Q 2 4 DM 6 F**

器件类型

STM660

启动过程

0：$\overline{PB}$ 必须保持低电平，直到 PS_{HOLD} 确认

输入和输出类型(1)

A：高电平使能输出，长按触发复位，SR 端带上拉电阻

B：低电平使能输出，长按触发复位，SR 端带上拉电阻

C：高电平使能输出，长按取消使能，SR 端带上拉电阻

D：低电平使能输出，长按取消使能，SR 端带上拉电阻

E：高电平使能输出，长按触发复位，SR 端无电阻

F：低电平使能输出，长按触发复位，SR 端无电阻

G：高电平使能输出，长按取消使能，SR 端无电阻

H：低电平有效使能输出，长按取消使能，SR端无电阻

V_{TH+} 阈值电压(1)

A: 2.50 V

Q: 3.30 V

S: 3.40 V

U: 3.50 V

V_{HYST} 电压滞后(1)

2: 200 mV

5: 500 mV

t开机空白消隐期(1)

2：1.4 s（最小）

4：5.6 s（最小）

5：11.2 s（最小）

Table 8. STM6600 ordering information scheme (continued)

Example: **STM660 0 F Q 2 4 DM 6 F**

Package

DM: TDFN12

Temperature range

6: –40 °C to +85 °C

Shipping method

F: ECOPACK® package, tape and reel

1. Other options are offered. Minimum order quantities may apply. Please contact local ST sales office for availability.

表8. STM6600 订购信息方案（续）

示例：	STM660	0		F		Q	2	4	DM	6	F

封装

DM：TDFN12封装

温度范围

6：–40 °C 至 +85 °C

包装方式

F：ECOPACK®包装，带卷盘

1. 提供其他选项。可能适用最小订购量。请联系当地意法半导体销售办事处了解供货情况。

Table 9. STM6601 ordering information scheme

Example: **STM660 1 G U 2 B DM 6 F**

Device type

STM660

Startup process

1: $\overline{PB}$ can be released before the PS_{HOLD} confirmation

Input and output types(1)

A: active high EN output, long push asserts $\overline{RST}$, pull-up on $\overline{SR}$

B: active low $\overline{EN}$ output, long push asserts $\overline{RST}$, pull-up on $\overline{SR}$

C: active high EN output, long push deasserts EN, pull-up on $\overline{SR}$

D: active low $\overline{EN}$ output, long push deasserts $\overline{EN}$, pull-up on $\overline{SR}$

G: active high EN output, long push deasserts EN, no resistor on $\overline{SR}$

V_{TH+} threshold voltage(1)

A: 2.50 V

M: 3.10 V

Q: 3.30 V

S: 3.40 V

U: 3.50 V

V_{HYST} voltage hysteresis(1)

2: 200 mV

t_{ON_BLANK} blanking period(1)

B: 1.4 s (min.)

D: 5.6 s (min.)

Package

DM: TDFN12

Temperature range

6: –40 °C to +85 °C

Shipping method

F: ECOPACK® package, tape and reel

1. Other options are offered. Minimum order quantities may apply. Please contact local ST sales office for availability.

表 9. STM6601 订购信息方案

示例： **STM660 1 G U 2 B DM 6 F**

器件类型

STM660

启动过程

1：$\overline{PB}$ 可在 PS_{HOLD} 确认前释放

输入和输出类型(1)

A：高电平使能输出，长按触发复位，SR 端带上拉电阻

B：低电平使能输出，长按触发复位，SR 端带上拉电阻

C：高电平使能输出，长按取消使能，SR 端带上拉电阻

D：低电平使能输出，长按取消使能，SR 端带上拉电阻

G：高电平使能输出，长按取消使能，SR 端无电阻

V_{TH+} 阈值电压(1)

A: 2.50 V

M: 3.10 V

Q: 3.30 V

S: 3.40 V

U: 3.50 V

V_{HYST} 电压滞后(1)

2: 200 mV

t开机空白消隐期(1)

B：1.4 秒（最小） D

：5.6 秒（最小）

封装

DM：TDFN12封装

温度范围

6：–40 °C 至 +85 °C

包装方式

F：ECOPACK®包装，带卷盘

1. 提供其他选项。可能适用最小订购量。请联系当地意法半导体销售办事处了解供货情况。

10 Product selector

Table 10. STM6600 product selector

Full part number	EN or $\overline{EN}$ (1)	After long push (2)	Internal resistor on SR input	Power-on lockout voltage V_{TH+} (V)	Forced power-off voltage V_{TH-} (V)	t_{ON_BLANK} (s) at startup (min.)	t_{ON_BLANK} (s) at reset (min.)	Top marking (3)
STM6600AS24DM6F	EN	$\overline{RST}$	pull-up	3.40	3.20	5.6	5.6	pyww AS24
STM6600BQ24DM6F	$\overline{EN}$	$\overline{RST}$	pull-up	3.30	3.10	5.6	5.6	pyww BQ24
STM6600CS25DM6F	EN	EN	pull-up	3.40	3.20	11.2	—	pyww CS25
STM6600DA55DM6F	$\overline{EN}$	$\overline{EN}$	pull-up	2.50	2.00	11.2	—	pyww DA55
STM6600DQ25DM6F	$\overline{EN}$	$\overline{EN}$	pull-up	3.30	3.10	11.2	—	pyww DQ25
STM6600DU25DM6F	$\overline{EN}$	$\overline{EN}$	pull-up	3.50	3.30	11.2	—	pyww DU25
STM6600ES24DM6F(4)	EN	$\overline{RST}$	—	3.40	3.20	5.6	5.6	pyww ES24
STM6600FQ24DM6F(4)	$\overline{EN}$	$\overline{RST}$	—	3.30	3.10	5.6	5.6	pyww FQ24
STM6600GS22DM6F(4)	EN	EN	—	3.40	3.20	1.4	—	pyww GS22
STM6600GS25DM6F(4)	EN	EN	—	3.40	3.20	11.2	—	pyww GS25
STM6600GU22DM6F(4)	EN	EN	—	3.50	3.30	1.4	—	pyww GU22
STM6600HA55DM6F(4)	$\overline{EN}$	$\overline{EN}$	—	2.50	2.00	11.2	—	pyww HA55
STM6600HQ25DM6F(4)	$\overline{EN}$	$\overline{EN}$	—	3.30	3.10	11.2	—	pyww HQ25
STM6600HU25DM6F(4)	$\overline{EN}$	$\overline{EN}$	—	3.50	3.30	11.2	—	pyww HU25

1. EN (or $\overline{EN}$) output is push-pull. $\overline{RST}$, $\overline{INT}$, $\overline{PB}_{OUT}$ and $\overline{VCC}_{LO}$ outputs are open drain.
2. After t_{SRD} expires through long push, either device reset ($\overline{RST}$) will be activated for t_{REC} (240 ms min.) or the EN (or $\overline{EN}$) pin will be deasserted. The additional Smart Reset™ delay time, t_{SRD}, can be adjusted by the user at 10 s/µF (typ.) by connecting the external capacitor to the C_{SRD} pin.
3. Where “p” = assembly plant, “y” = assembly year (0 to 9) and “ww” = assembly work week (01 to 52).
4. Please contact local ST sales office for availability.

10 产品选择器

表 10. STM6600 产品选择器

完整零件编号	EN 或 EN(1)	长按后(2)	SR输入端内部电阻	上电锁定电压 V_{TH+} (V)	强制断电电压 V_{TH-} (V)	$t_{开机空白}$ 启动时 (s) (min.)	$t_{开机空白}$ 复位时 (s) (min.)	顶面标记 (3)
STM6600AS24DM6F	使能	$\overline{RST}$	上拉	3.40	3.20	5.6	5.6	pyww AS24
STM6600BQ24DM6F	$\overline{使能}$	$\overline{RST}$	上拉	3.30	3.10	5.6	5.6	pyww BQ24
STM6600CS25DM6F	使能	使能	上拉	3.40	3.20	11.2	—	pyww CS25
STM6600DA55DM6F	$\overline{使能}$	$\overline{使能}$	上拉	2.50	2.00	11.2	—	pyww DA55
STM6600DQ25DM6F	$\overline{使能}$	$\overline{使能}$	上拉	3.30	3.10	11.2	—	pyww DQ25
STM6600DU25DM6F	$\overline{使能}$	$\overline{使能}$	上拉	3.50	3.30	11.2	—	pyww DU25
STM6600ES24DM6F(4)	使能	$\overline{RST}$	—	3.40	3.20	5.6	5.6	pyww ES24
STM6600FQ24DM6F(4)	$\overline{使能}$	$\overline{RST}$	—	3.30	3.10	5.6	5.6	pyww FQ24
STM6600GS22DM6F(4)	使能	使能	—	3.40	3.20	1.4	—	pyww GS22
STM6600GS25DM6F(4)	使能	使能	—	3.40	3.20	11.2	—	pyww GS25
STM6600GU22DM6F(4)	使能	使能	—	3.50	3.30	1.4	—	pyww GU22
STM6600HA55DM6F(4)	$\overline{使能}$	$\overline{使能}$	—	2.50	2.00	11.2	—	pyww HA55
STM6600HQ25DM6F(4)	$\overline{使能}$	$\overline{使能}$	—	3.30	3.10	11.2	—	pyww HQ25
STM6600HU25DM6F(4)	$\overline{使能}$	$\overline{使能}$	—	3.50	3.30	11.2	—	pyww HU25

1. EN（或 $\overline{EN}$）输出为推挽式。$\overline{RST}$、$\overline{INT}$、$\overline{PB_{OUT}}$和 $\overline{VCC_{LO}}$输出为开漏。

2. 在通过长按触发的 t_{SRD}到期后，任一设备复位（RST）将被$\overline{激活}$，持续时间为 t_{REC}（最短240 ms），或 EN（或 $\overline{EN}$）引脚将被取消断言。额外的 Smart Reset™ 延迟时间 tSRD，可通过在 C_{SRD}引脚连接外部电容，以 10 s/µF（典型值）进行用户调节。

3. 其中“p”为组装厂，“y”为组装年份（0至9），“ww”为组装周数（01至52）。

4. 请联系当地意法半导体销售办事处了解供货情况。

Table 11. STM6601 product selector

Full part number	EN or $\overline{EN}$[1]	After long push[2]	Internal resistor on SR input	Power-on lockout voltage V_{TH+} (V)	Forced power-off voltage V_{TH-} (V)	t_{ON_BLANK} (s) at startup (min.)	t_{ON_BLANK} (s) at reset (min.)	Top marking[3]
STM6601AQ2BDM6F	EN	$\overline{RST}$	pull-up	3.30	3.10	1.4	1.4	pyww AQ2B
STM6601AU2DDM6F	EN	$\overline{RST}$	pull-up	3.50	3.30	5.6	5.6	pyww AU2D
STM6601BM2DDM6F	$\overline{EN}$	$\overline{RST}$	pull-up	3.10	2.90	5.6	5.6	pyww BM2D
STM6601BS2BDM6F	$\overline{EN}$	$\overline{RST}$	pull-up	3.40	3.20	1.4	1.4	pyww BS2B
STM6601CA2BDM6F	EN	EN	pull-up	2.60	2.40	1.4	—	pyww CA2B
STM6601CM2DDM6F	EN	EN	pull-up	3.10	2.90	5.6	—	pyww CM2D
STM6601CQ2BDM6F	EN	EN	pull-up	3.30	3.10	1.4	—	pyww CQ2B
STM6601CU2BDM6F	EN	EN	pull-up	3.50	3.30	1.4	—	pyww CU2B
STM6601DA2BDM6F	$\overline{EN}$	$\overline{EN}$	pull-up	2.50	2.30	1.4	—	pyww DA2B
STM6601DS2BDM6F	$\overline{EN}$	$\overline{EN}$	pull-up	3.40	3.20	1.4	—	pyww DS2B
STM6601GU2BDM6F[4]	EN	EN	—	3.50	3.30	1.4	—	pyww GU2B

1. EN (or $\overline{EN}$) output is push-pull. $\overline{RST}$, $\overline{INT}$, $\overline{PB}_{OUT}$ and $\overline{VCC}_{LO}$ outputs are open drain.
2. After t_{SRD} expires through long push, either device reset ($\overline{RST}$) will be activated for t_{REC} (240 ms min.) or the EN (or $\overline{EN}$) pin will be deasserted. The additional Smart Reset™ delay time, t_{SRD}, can be adjusted by the user at 10 s/µF (typ.) by connecting the external capacitor to the C_{SRD} pin.
3. Where “p” = assembly plant, “y” = assembly year (0 to 9) and “ww” = assembly work week (01 to 52).
4. Please contact local ST sales office for availability.

表格 11. STM6601 产品选择器

完整零件编号	EN 或 $\overline{EN}$[1]	长按后[2]	SR输入端内部电阻	上电锁定电压 V_{TH+} (V)	强制断电电压 V_{TH-} (V)	$t_{开机空白启动时}$ (s) (min.)	$t_{开机空白复位时}$ (s) (min.)	顶面标记[3]
STM6601AQ2BDM6F	使能	$\overline{RST}$	上拉	3.30	3.10	1.4	1.4	pyww AQ2B
STM6601AU2DDM6F	使能	$\overline{RST}$	上拉	3.50	3.30	5.6	5.6	pyww AU2D
STM6601BM2DDM6F	$\overline{使能}$	$\overline{RST}$	上拉	3.10	2.90	5.6	5.6	pyww BM2D
STM6601BS2BDM6F	$\overline{使能}$	$\overline{RST}$	上拉	3.40	3.20	1.4	1.4	pyww BS2B
STM6601CA2BDM6F	使能	使能	上拉	2.60	2.40	1.4	—	pyww CA2B
STM6601CM2DDM6F	使能	使能	上拉	3.10	2.90	5.6	—	pyww CM2D
STM6601CQ2BDM6F	使能	使能	上拉	3.30	3.10	1.4	—	pyww CQ2B
STM6601CU2BDM6F	使能	使能	上拉	3.50	3.30	1.4	—	pyww CU2B
STM6601DA2BDM6F	$\overline{使能}$	$\overline{使能}$	上拉	2.50	2.30	1.4	—	pyww DA2B
STM6601DS2BDM6F	$\overline{使能}$	$\overline{使能}$	上拉	3.40	3.20	1.4	—	pyww DS2B
STM6601GU2BDM6F[4]	使能	使能	—	3.50	3.30	1.4	—	pyww GU2B

1. EN（或 $\overline{EN}$）输出为推挽式。$\overline{RST}$、$\overline{INT}$、$\overline{PB}_{OUT}$和 $\overline{VCC}_{LO}$输出为开漏。

2. 在通过长按触发的 t_{SRD}到期后，任一设备复位（RST）将被$\overline{激活}$，持续时间为 t_{REC}（最短240 ms），或 EN（或 $\overline{EN}$）$\overline{引脚}$将被取消断言。额外的 Smart Reset™ 延迟时间 tSRD，可通过在 C_{SRD}引脚连接外部电容，以 10 s/µF（典型值）进行用户调节。

3. 其中“p”为组装厂，“y”为组装年份（0至9），“ww”为组装周数（01至52）。

4. 请联系当地意法半导体销售办事处了解供货情况。

11 Revision history

Table 12. Document revision history

Date	Revision	Changes
04-Mar-2009	1	Initial release
05-Jun-2009	2	Updated text in Section 2, Section 3, Figure 11, 12; updated Figure 1, 7, 9, 14, 18, 19, 43, Table 3, 5, 8, 9, 10; added Figure 8, 10, Table 7; reformatted document
23-Jul-2009	3	Updated text in Features, Table 1, 8, 9, and 10; reformatted document
22-Oct-2009	4	Updated Section 2, Table 5, Table 10, Figure 1, 7, 8, 9, 10, 11, 12, 14, 18, title of Section 10; added Section 5: Typical operating characteristics (Figure 23 through 40); document status upgraded to full datasheet
25-Jan-2010	5	Updated Figure 6, Section 2, Table 5; textual update to “Smart Reset™”
13-Apr-2010	6	Updated Figure 1, 6, 7, 8, 9, 10, 11, 12, 13, Section 2, Section 3, Table 3, 5, 8, 9, 10
07-Jun-2010	7	Reformatted Figure 1 and Figure 42, corrected typo in Section 3, added option A to Table 8, updated Table 10 and separated Table 10 to Table 10 and Table 11
10-Sep-2010	8	Updated standby current to 0.6 ìA throughout datasheet; removed footnote 2 of Figure 14; updated Table 8, 9, 11; minor textual updates.
24-Feb-2011	9	Updated Table 10 - removed footnote 4
12-May-2011	10	Updated Table 8, Table 10 and Table 11, minor text and typo modifications throughout document
26-Jun-2012	11	Updated Section 1: Description, “SR - Smart Reset™ button input” in Section 2: Pin descriptions and “Hardware reset or power-down while system not responding” in Section 3: Operation, added cross-references in Section 6: Maximum ratings and Section 7: DC and AC characteristics
13-Oct-2014	12	Table 9: added “A” (2.50 V) to VTH+ threshold voltage Table 11: added new full part number
09-Jan-2023	13	Added STM6601DA2BDM6F new full part number in Table 11.
15-May-2023	14	Updated *Figure 5*.

11 版本历史

表 12. 文档版本历史

日期	版本	变更内容
2009年3月4日	1	初始发布
2009年6月5日	2	更新第2节、第3节、第11图、第12图内容；更新第1图、第7图、第9图、第14图、第18图、第19图、第43图，第3表、第5表、第8表、第9表、第10表；新增第8图、第10图，第7表； 文档重新排版
2009年7月23日	3	更新功能部分、第1表、第8表、第9表、第10表；文档重新排版
2009年10月22日	4	更新第2节、第5表、第10表，第1图、第7图、第8图、第9图、第10图、第11图、第12图、第14图、第18图，第10节标题；新增第5节：典型工作特性（第23图至第40图）； 文档状态升级为完整数据手册
2010年1月25日	5	更新图6，第2节，表格5； “Smart Reset™”文本更新
2010年4月13日	6	更新图1、6、7、8、9、10、11、12、13，第2节，第3节，表格3，5, 8, 9, 10
2010年6月7日	7	重新排版图1和图42，修正第3节错字，向表格8添加选项A，更新表格10，并将表格10拆分为表格10和表格11
2010年9月10日	8	将整份数据手册中的待机电流更新为0.6 ìA； 移除图14脚注2；更新表格8、9、11；少量文本更新。
2011年2月24日	9	更新表格10 - 移除脚注4
2011年5月12日	10	更新表格8、表格10和表格11，文档中少量文本及错字修改
2012年6月26日	11	更新第1节：描述，第2节引脚描述中的“SR - Smart Reset™按钮输入”，以及第3节操作中的“系统无响应时的硬件复位或断电”，在第6节最大额定值和第7节直流和交流特性中添加了交叉引用。
2014年10月13日	12	表9：在VTH+阈值电压中添加“A”（2.50 V）。 表11：添加新的完整零件编号。
2023年1月9日	13	在表11中添加了STM6601DA2BDM6F新的完整零件编号。
2023年5月15日	14	更新图*5*。

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