

# HiFi Audio Circuit Design

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## ABSTRACT

With the increase in personal electronic devices, HiFi audio is more popular than ever in many applications, such as smartphones, music players, home theaters, and even car infotainment. Many engineers and consumers devote themselves to the endless journey in HiFi audio. This document will help engineers understand, judge, design, and optimize a HiFi audio circuit.

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## 1 Introduction

An audio signal is a representation of sound—typically an electrical voltage. Audio signals usually have frequencies in the range of approximately 20 Hz to 20,000 Hz, which is audible to most humans. Audio signals may be synthesized directly or may be originated at a transducer, such as a microphone, musical instrument pickup, phonograph cartridge, or tape head. Loudspeakers or headphones convert an electrical audio signal to sound.

High Fidelity or HiFi is a term used by home stereo listeners, audiophiles, and home audio enthusiasts to refer to high-quality reproduction of sound to distinguish it from the lower quality sound produced by inexpensive audio equipment. Ideally, high-fidelity equipment has inaudible noise and distortion, and a flat (neutral, uncolored) frequency response within the intended frequency range.

# HiFi音频电路设计

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## 摘要

随着个人电子设备的普及，HiFi音频在智能手机、音乐播放器、家庭影院乃至汽车信息娱乐系统等多种应用中日益流行。众多工程师与消费者投身于HiFi音频的持续探索之中。本报告旨在帮助工程师理解、评估、设计及优化HiFi音频电路。

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## 商标

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## 1 引言

音频信号是声音的表示形式——通常为电压信号。音频信号的频率通常在约 20 Hz 至 20,000 Hz 范围内，大多数人类可听见该频率范围。音频信号可以直接合成，也可以由传感器产生，例如麦克风、乐器拾音器、唱头或磁带头。扬声器或耳机将电气音频信号转换为声音。

高保真（HiFi）是家庭立体声音响爱好者、发烧友及家庭音响爱好者用以指代高质量声音重放的术语，用以区别于廉价音响设备产生的低质量声音。理想的高保真设备应具备不可闻的噪声和失真，并在预定频率范围内实现平坦（中性、无色）的频率响应。

A sound system is mainly composed of the auditory system (human ears), hardware system (equipment), software system (signal source) and listening environment. Figure 1 shows the typical block diagram of an audio reproduction hardware system, which converts the digital audio source to the voltage signal that drives the headphone. This article only focuses on this hardware system, which contains the DAC, current to voltage (I/V) transimpedance amplifier, and difference amplifier.

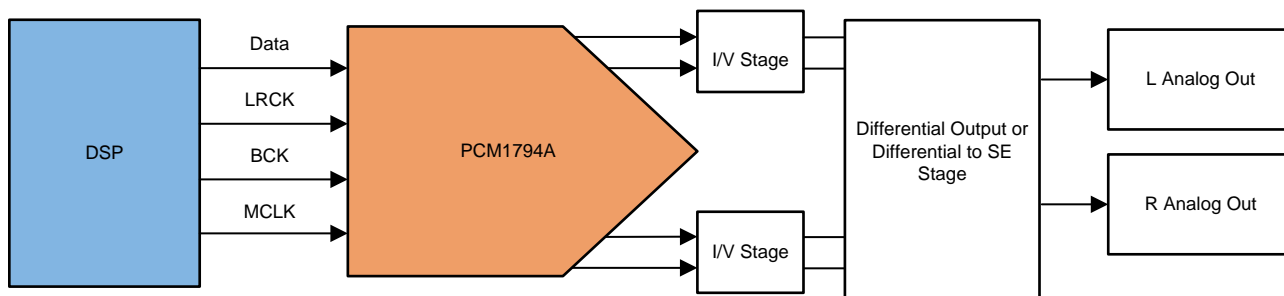


Figure 1. Audio Reproduction Hardware System

## 2 HiFi Audio Specifications

To ideally reproduce the audio signals, the key is to design a HiFi sound system that delivers ultra-low distortion, excellent signal-to-noise ratio (SNR), flat frequency response, high-dynamic range, quick transient response, low stereo crosstalk, good stereo balance, and proper output. The topic of this section is how to achieve these goals.

### 2.1 Excellent THD+N

THD+N is the most important parameter of signal quality. Theoretically HiFi requires excellent THD+N ( $< -110$  dB) to reproduce lossless audio signal. A high-quality audio source, an ultra-low noise and distortion DAC and amplifiers, ultra-low noise power supply, proper PCB layout, and attention to external circuits of the amplifiers are all required to achieve excellent THD+N performance.

### 2.2 Excellent SNR

Audible idle and background hiss noises are not allowed. Excellent SNR means no audible hiss noise at any time. As with THD+N, a high-quality audio source, an ultra-low noise DAC and amplifiers and power supply, proper PCB layout, and proper external circuit of the amplifiers are all required to achieve the excellent SNR performance. If  $\text{SNR} = 110$  dB is required, and the signal amplitude is 1 Vrms, according to the formula  $\text{SNR} = 20 \log(\text{signal power} / \text{noise power})$ , the rms noise power is 3.16  $\mu\text{V}$  from 20 Hz to 20,000 Hz. If  $\text{SNR} \equiv 115$  dB is required, the rms noise power is 1.78  $\mu\text{V}$ , which is also achievable.

### 2.3 Flat Frequency Response

A flat frequency response is very important to reproduce the most original audio signals from low frequency to high frequency. The bandwidth of amplifiers and low-pass filters must be high enough to avoid high-frequency signal attenuation. The matching circuits in the audio signal chain should also be well designed to avoid the ripple in the audio band.

### 2.4 Excellent Dynamic Range

The dynamic range allows a HiFi audio system to accurately reproduce both quiet and loud sounds simultaneously (dynamically). This dynamic range is especially important for classical music. The dynamic range of human ears is 120 dB, which could be achieved by a 24-bit, HiFi DAC and ultra-low noise amplifier with proper gain.

音响系统主要由听觉系统（人耳）、硬件系统（设备）、软件系统（信号源）及聆听环境组成。图1展示了典型音频重放硬件系统的框图，该系统将数字音频源转换为驱动耳机的电压信号。本文仅聚焦于该硬件系统，包含DAC、电流-电压（I/V）跨阻放大器及差分放大器。

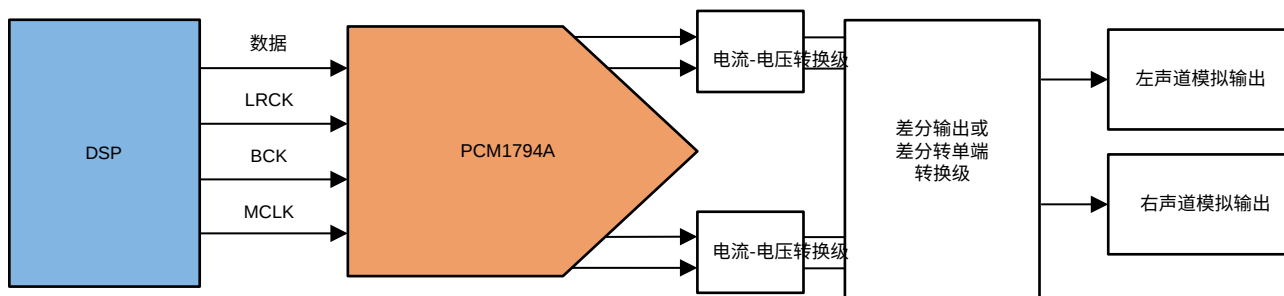


图1. 音频重放硬件系统

## 2 HiFi音频规格

为了理想地重现音频信号，关键在于设计一套具备超低失真、优异信噪比（SNR）、平坦频率响应、高动态范围、快速瞬态响应、低立体声串扰、良好立体声平衡及适当输出的HiFi音响系统。本节内容聚焦于如何实现上述目标。

### 2.1 优异的THD+N

THD+N是衡量信号质量的最重要参数。理论上，HiFi要求THD+N优于-110 dB，以实现无损音频信号的重现。高品质音源、超低噪声与失真的DAC及放大器、超低噪声电源、合理的印刷电路板布局，以及对放大器外部电路的细致设计，均为实现优异THD+N性能的必要条件。

### 2.2 优异的信噪比

不可出现任何可听见的静态噪声或背景嘶嘶声。优异的信噪比意味着在任何情况下均无可听见的嘶嘶声。与THD+N相似，为实现优异的信噪比性能，需配备高质量音频源、超低噪声DAC及放大器与电源，合理的印刷电路板布局，以及放大器的合适外部电路。若要求信噪比 $SNR = 110 \text{ dB}$ ，且信号幅度为 $1 \text{ V}_{rms}$ ，根据公式 $SNR = 20 \log (\text{信号功率} / \text{噪声功率})$ ，则20 Hz至20,000 Hz频段内的均方根噪声电压为 $3.16 \mu\text{V}$ 。若要求 $SNR \geq 115 \text{ dB}$ ，则均方根噪声电压为 $1.78 \mu\text{V}$ ，亦可实现。

### 2.3 平坦的频率响应

平坦的频率响应对于从低频到高频准确重现原始音频信号至关重要。放大器和低通滤波器的带宽必须足够宽，以避免高频信号衰减。音频信号链中的匹配电路也应设计合理，以避免音频频段内的波纹。

### 2.4 优异的动态范围

动态范围使HiFi音频系统能够同时准确地再现安静与响亮的声音。这种动态范围对于古典音乐尤为关键。人耳的动态范围约为120 dB，可通过24位HiFi DAC及具备适当增益的超低噪声放大器实现。

## 2.5 Quick Transient Response

Quick transient response shows the explosive force, which is the ability to reproduce quick, explosive sound and quickly restore silence when the explosive sound ends. This specification is determined by a high-output current and high bandwidth headphone driver, high bandwidth DAC and I/V amplifier, and power supply with quick transient response.

## 2.6 Low Stereo Crosstalk

Left and right channel crosstalk causes the sound field distortion, which results in narrow sound field. Because the frequency of audio signal is lower than 20 kHz, 100-dB isolation between left and right channel is high enough and can easily be achieved by proper PCB layout and power supply decoupling.

## 2.7 High Stereo Balance

The sound field will shift to the larger volume if the volume of the left and right channels is not same. This shift is especially bad for symphony music, which can be easily mixed by imbalanced volume. This specification can be achieved by matching the gain and PCB layout in the two channels' DAC, amplifier, and external circuits. For resistor matching, 0.1% precision thin-film feedback resistors are recommended.

## 2.8 Output Power

Output power is a recognizable parameter to consumers, so buying decisions are often made on this number. This specification is determined by high output current headphone driver and power supply. Designing a high output power audio system despite good THD+N performance is very easy, but too high of an output power will significantly worsen the THD+N performance for a given audio system, so always consider the impact on THD+N when designing the output power.

# 3 HiFi Audio Circuit Design

## 3.1 DAC Circuit Design

The DAC is the source of the analog audio signal chain, and the DAC is the performance bottleneck in the chain because the THD+N performance of the best DAC in the world is 10 + dB worse than the best amplifier. The DAC contains both analog and digital functional blocks and needs ultra-low noise clock, power supply, and careful PCB layout to achieve less than -110dB THD+N performance. TI PCM1794A is one of the best audio DACs in the world. With simple and clear illustrations of external circuitry on its datasheet, designers can achieve a dynamic range of 129 dB and THD+N of -116 dB by following the design guide.

## 3.2 Transimpedance Amplifier Circuit Design

Usually ultra-high performance audio DACs are differential current output, so a transimpedance amplifier is required to convert the current to voltage.

Some design rules for the I/V transimpedance amplifier:

1. The amplifier will have ultra-low noise and distortion to achieve excellent system SNR, THD+N, and dynamic range. The amplifier should have high slew rate to achieve excellent system transient response, high bandwidth to achieve flat system frequency response, and in-portable, system low-quiescent current to achieve low system power consumption. Sometimes high power supplies supported to get high output voltage swing thus get high system SNR. Low output drive capability is acceptable because its load is the second stage driver amplifier. OPA1612 is a good choice for this application.
2. To get the best SNR, the output voltage of this first-stage amplifier should be maximized according to the simulation, so the output voltage swing of the I/V transimpedance amplifier should be as high as possible, thus the center current output of DAC will also be the center output voltage of the first stage amplifier, this also makes the center input voltage of the second stage driver amplifier 0 V.

## 2.5 快速瞬态响应

快速瞬态响应体现为爆发力，即再现快速爆发声音并在爆发结束后迅速恢复静音的能力。该指标由高输出电流和高带宽的耳机驱动器、高带宽DAC与I/V放大器，以及具备快速瞬态响应的电源共同决定。

## 2.6 低立体声串扰

左右声道串扰会导致声场失真，进而使声场变窄。

由于音频信号频率低于20 kHz，左右声道间100 dB的隔离度已足够高，且通过合理的印刷电路板布局 and 电源去耦可轻松实现。

## 2.7 高立体声平衡度

若左右声道音量不一致，声场将偏向音量较大的一侧。这种偏移对交响乐尤其不利，因为音量不平衡会导致音乐混杂不清。该规格可通过匹配两个声道的DAC、放大器及外部电路的增益和印刷电路板布局来实现。电阻匹配建议采用0.1%精度的薄膜反馈电阻。

## 2.8 输出功率

输出功率是消费者易于识别的参数，因此购买决策通常基于此数值。该规格由高输出电流耳机驱动器和电源决定。

设计高输出功率音频系统且保持良好THD+N性能较为容易，但输出功率过高会显著恶化特定音频系统的THD+N性能，因此设计输出功率时应始终考虑其对THD+N的影响。

# 3 HiFi音频电路设计

## 3.1 DAC电路设计

DAC是模拟音频信号链的源头，也是性能瓶颈，因为世界上最佳DAC的THD+N性能比最佳放大器差10 dB以上。DAC包含模拟和数字功能模块，需配备超低噪声时钟和电源，并进行精细的印刷电路板布局设计，以实现低于-110 dB的总谐波失真加噪声（THD+N）性能。TI PCM1794A是全球领先的音频DAC之一。依据其数据手册中简洁明了的外部电路示意，设计人员可遵循设计指南，实现129 dB的动态范围及-116 dB的THD+N性能。

## 3.2 跨阻放大器电路设计

通常，超高性能音频数模转换器采用差分电流输出，因此需要跨阻放大器将电流转换为电压。

I/V跨阻放大器的一些设计准则：

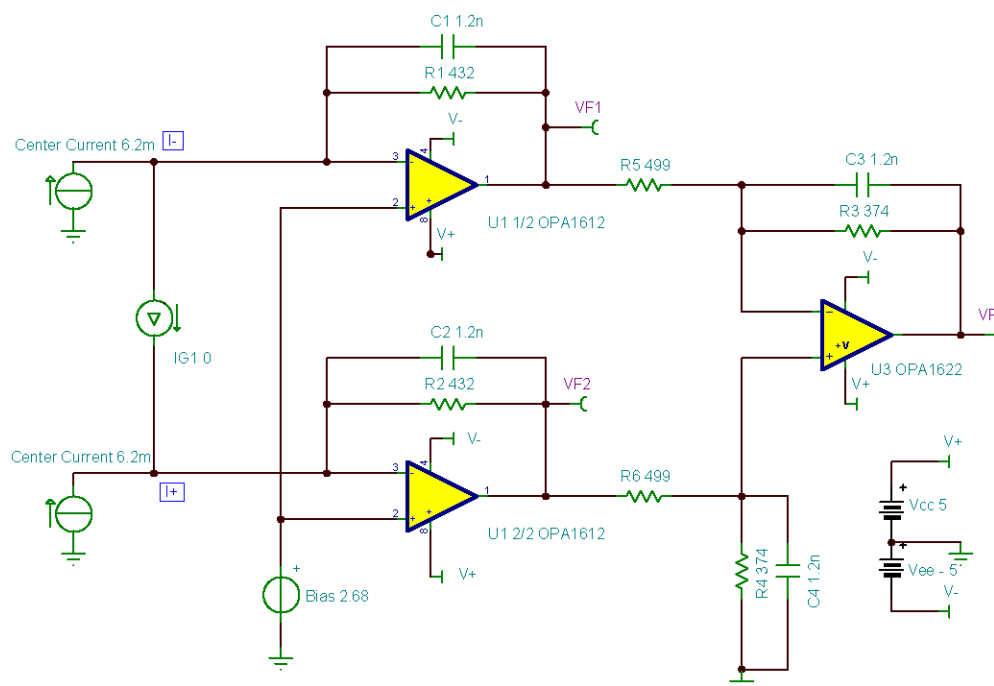
1. 放大器应具备超低噪声和失真，以实现优异的系统信噪比、总谐波失真加噪声（THD+N）及动态范围。放大器应具备高转换速率以实现优异的系统瞬态响应，高带宽以保证系统频率响应平坦，并且具备低静态电流以降低系统功耗。有时采用高电源电压以获得较高的输出电压摆幅，从而提升系统信噪比。输出驱动能力较低是可接受的，因为其负载为第二级驱动放大器。OPA1612是该应用的理想选择。

2. 为了获得最佳信噪比，根据仿真结果，第一阶段放大器的输出电压应尽可能最大化，因此I/V跨阻放大器的输出电压摆幅应尽量提高，从而使数模转换器的中心电流输出对应第一阶段放大器的中心输出电压，这也使第二阶段驱动放大器的中心输入电压保持在0 V。

This section offers two design examples to meet different requirements. One example uses  $\pm 5$ -V power supply for the I/V amplifier to get a performance and cost balanced system and another one uses  $\pm 10$ -V power supply to get the lowest noise system. Each helps show how to design a proper HiFi circuit. Because the left and right channels are identical, only one channel is analyzed, as shown in Figure 2 and Figure 3.

The output current swing of DAC PCM1794A is  $\pm 3.9$  mA, and the center current is 6.2 mA. The best output linear range of OPA1612 is  $[(V-) + 0.6 \text{ V}, (V+) - 0.6 \text{ V}]$ , and the common mode voltage range is  $[(V-) + 2, (V+) - 2]$ .

The output voltage swing of OPA1612,  $V_{\text{swing}}$ , is 4.4-V peak to peak, so the feedback resistors  $R1 = 4.4 / 3.9 \text{ mA} = 1128 \Omega$ . Therefore, the bias voltage of OPA1612  $V_{\text{bias}}$  in the positive input pin will be  $6.2 \text{ mA} \times 1128 = 6.99 \text{ V}$ , which exceeds the common mode range of OPA1612  $[-3 \text{ V}, 3 \text{ V}]$ . Because the voltage exceeds the range, it is not suitable, so  $V_{\text{bias}}$  must be reduced to less than 3 V by reducing the feedback resistors R1. This reduction also reduces  $V_{\text{swing}}$  to its maximum allowed value of  $4.4 - V_{\text{bias}}$ , where  $V_{\text{bias}} = 6.2 \text{ mA} \times R1$ , and  $V_{\text{swing}} = 3.9 \text{ mA} \times R1$ . Because  $R1 = 4.4 \text{ V} / (6.2 + 3.9) \text{ mA} = 436 \Omega$ , a general smaller 432  $\Omega$  will be used in the actual circuit. This configuration generates  $V_{\text{swing}} = 1.685 \text{ V}$ , and  $V_{\text{bias}} = 2.678 \text{ V}$ .



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**Figure 2. Amplifiers Schematic ( $\pm 5$ -V Power Supply)**

The feedback capacitors C1 forms a pole in transfer function at Equation 1.

$$f_p = \frac{1}{2\pi R_F C_F} \quad (1)$$

The capacitors must be large enough to maintain stability but not introduce too much phase shift and amplitude attenuation at audio frequency. With a 1.2-nF capacitor, the  $f_p = 308 \text{ kHz}$ , the phase shift at 20 kHz is  $7^\circ$ , and the amplitude attenuation is 0.03 dB; this is a very good, balanced solution.

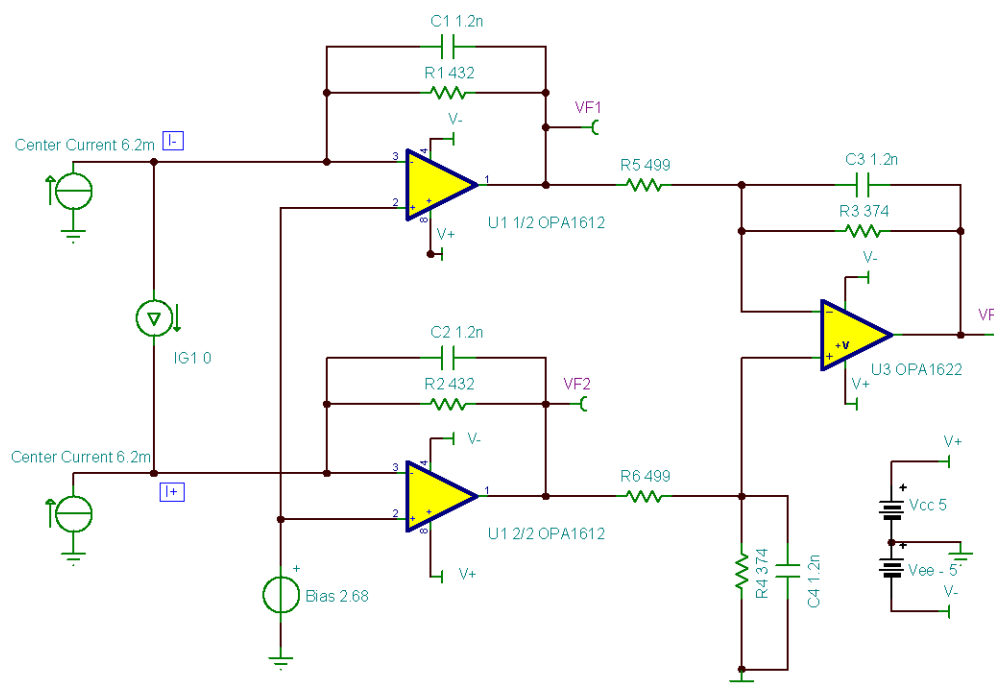


本节提供两个设计示例，以满足不同的设计需求。其中一个示例采用±5伏电源为I/V放大器，实现性能与成本的平衡；另一个示例采用±10伏电源，以获得最低噪声的系统。这两个示例均有助于展示如何设计合适的高保真电路。

由于左右声道结构相同，本文仅分析其中一个声道，如图2和图3所示。

DAC PCM1794A的输出电流摆幅为±3.9 mA，中心电流为6.2 mA。OPA1612的最佳输出线性范围为[(V-) + 0.6 V, (V+) - 0.6 V]，共模电压范围为[(V-) + 2, (V+) - 2]。

OPA1612的输出电压摆幅 $V_{\text{swing}}$ 为4.4伏峰峰值，因此反馈电阻 $R1 = 4.4 / 3.9 \text{ mA} = 1128 \Omega$ 。因此，OPA1612正输入端的偏置电压 $V_{\text{bias}}$ 为 $6.2 \text{ mA} \times 1128 = 6.99 \text{ V}$ ，已超出OPA1612的共模电压范围[-3 V, 3 V]。由于电压超出范围，故不适用，必须通过减小反馈电阻 $R1$ 将 $V_{\text{bias}}$ 降低至小于3 V。此举同时将 $V_{\text{swing}}$ 限制在其最大允许值 $4.4 - V_{\text{bias}}$ ，其中 $V_{\text{bias}} = 6.2 \text{ mA} \times R1$ ， $V_{\text{swing}} = 3.9 \text{ mA} \times R1$ 。因 $R1 = 4.4 \text{ V} / (6.2 + 3.9) \text{ mA} = 436 \Omega$ ，实际电路中通常采用较小的432  $\Omega$ 。该配置产生的 $V_{\text{swing}}$ 为1.685 V， $V_{\text{bias}}$ 为2.678 V。



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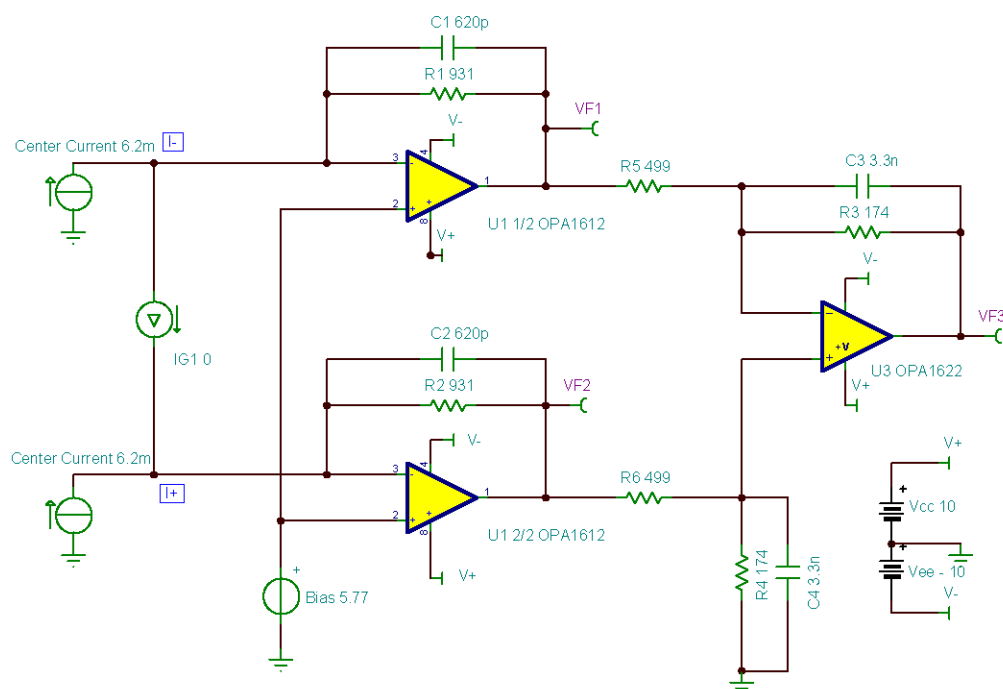
图 2。放大器原理图 (±5伏电源)

反馈电容 $C1$ 在传递函数中形成了方程 (1) 中的极点。

$$f_p = \frac{1}{2\pi R_F C_F}$$

1) 电容必须足够大以保证电路稳定，但不能在音频频率范围内引入过多的相位偏移和幅度衰减。采用 1.2-nF 电容时， $f_p = 308 \text{ kHz}$ ，20 kHz 处的相位偏移为  $7^\circ$ ，幅度衰减为 0.03 分贝；这是一个非常理想且均衡的解决方案。





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**Figure 3. Amplifiers Schematic (±10-V Power Supply)**

Figure 3 is the ±10-V power supply application schematic. The best output linear range of OPA1612 is [−9.4 V, 9.4 V], and the common mode voltage range is [−8 V, 8 V], so in this case assume:

The output voltage swing of OPA1612  $V_{\text{swing}}$  is 9.4-V peak to peak, so the feedback resistors  $R1 = 9.4 / 3.9 \text{ mA} = 2410 \Omega$ . The bias voltage of OPA1612  $V_{\text{bias}}$  in the positive input pin should be  $6.2 \text{ mA} \times 2410 = 14.9 \text{ V}$ , which exceeds the common mode range of OPA1612 [−8 V, 8 V], and is not suitable.  $V_{\text{bias}}$  must be reduced to less than 8 V by reducing the feedback resistors R1, which also reduces the  $V_{\text{swing}}$  to its maximum allowed value of  $9.4 - V_{\text{bias}}$ .  $V_{\text{bias}} = 6.2 \text{ mA} \times R1$  and  $V_{\text{swing}} = 3.9 \text{ mA} \times R1$ , so  $R1 = 9.4 \text{ V} / (6.2 + 3.9) \text{ mA} = 931 \Omega$ , which is just a general value. This configuration generates  $V_{\text{swing}} = 3.630 \text{ V}$  and  $V_{\text{bias}} = 5.772 \text{ V}$ .

The feedback capacitors C1 forms a pole in transfer function at Equation 1.

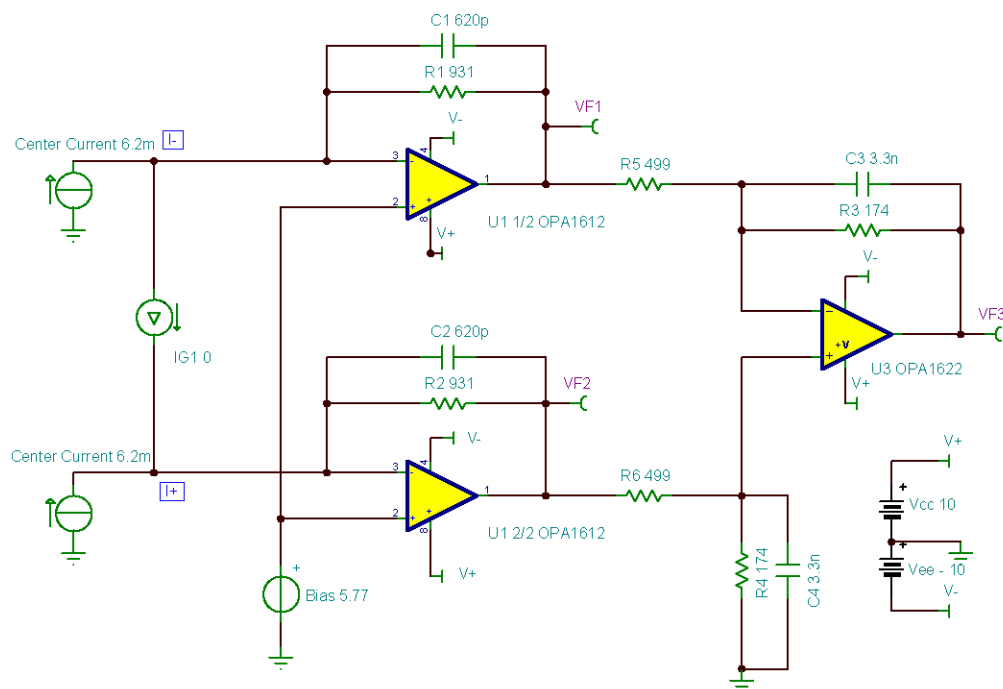
The capacitors must be large enough to maintain stability but not introduce too much phase shift and amplitude attenuation at audio frequency. With a 620-pF capacitor, the  $f_p = 276 \text{ kHz}$ , the phase shift at 20 kHz is  $8^\circ$ , and the amplitude attenuation is 0.02 dB; this is a very good balanced solution.

Circuits I+ and I− are same, so  $R2 = R1$  and  $C2 = C1$ .

### 3.3 Difference Amplifier Design

The purpose of the difference amplifier is to convert differential signal to single ended output voltage signal and provide proper gain and enough current to drive the headphone. Like the I/V transimpedance amplifier, this second stage amplifier should be ultra-low noise and distortion to achieve excellent system SNR, THD+N and dynamic range, high slew rate to achieve excellent system transient response, high bandwidth to achieve flat system frequency response, and low quiescent current to achieve low power consumption.

The values of the resistors in the difference amplifier external circuit are determined by the output current swing of the DAC as well as the gain of first stage amplifier and maximum output voltage desired at the headphone output. One important difference between the first and second stage amplifiers is that the second stage amplifier chosen must be capable of delivering the necessary current to the headphone and remain stable into typical headphone loads that can have capacitances as high as 400 pF.



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图 3。放大器原理图 (±10伏电源)

图3为±10伏电源应用的原理图。OPA1612的最佳输出线性范围为 $[-9.4\text{ V}, 9.4\text{ V}]$ ，共模电压范围为 $[-8\text{ V}, 8\text{ V}]$ ，因此在此情况下假设：

OPA1612的输出电压摆幅 $V_{\text{swing}}$ 为9.4伏峰峰值，故反馈电阻 $R1 = 9.4 / 3.9\text{ mA} = 2410\ \Omega$ 。OPA1612正输入端的偏置电压 $V_{\text{bias}}$ 应为 $6.2\text{ mA} \times 2410 = 14.9\text{ V}$ ，超过了OPA1612的共模电压范围 $[-8\text{ V}, 8\text{ V}]$ ，因此不适用。必须通过减小反馈电阻 $R1$ 将 $V_{\text{bias}}$ 降低至低于8 V，同时这也会将 $V_{\text{swing}}$ 限制在最大允许值 $9.4 - V_{\text{bias}}$ 。  $V_{\text{bias}} = 6.2\text{ mA} \times R1$ ， $V_{\text{swing}} = 3.9\text{ mA} \times R1$ ，因此 $R1 = 9.4\text{ V} / (6.2 + 3.9)\text{ mA} = 931\ \Omega$ ，此值为常用参考值。该配置产生的 $V_{\text{swing}}$ 为3.630 V， $V_{\text{bias}}$ 为5.77 V。

反馈电容 $C1$ 在传递函数中形成了方程 (1) 中的极点。

电容器必须足够大以保证电路稳定，但不能在音频频率范围内引入过多的相位偏移和幅度衰减。采用620皮法电容，截止频率 $f_p$ 为276 kHz，20 kHz时的相位偏移为 $8^\circ$ ，幅度衰减为0.02 dB；这是一个非常优秀的平衡方案。

电路I+与I-相同，因此 $R2 = R1$ ， $C2 = C1$ 。

### 3.3 差分放大器设计

差分放大器的作用是将差分信号转换为单端输出电压信号，并提供适当的增益及足够的电流以驱动耳机。与I/V跨阻放大器类似，第二级放大器应具备超低噪声和失真，以实现优异的系统信噪比 (SNR)、总谐波失真加噪声 (THD+N) 及动态范围；高转换速率以保证系统瞬态响应优异；高带宽以实现系统频率响应平坦；以及低静态电流以降低功耗。

差分放大器外部电路中电阻的取值由数模转换器 (DAC) 的输出电流摆幅、前级放大器的增益以及耳机输出端所需的最大输出电压共同决定。第一级和第二级放大器之间的一个重要区别在于，所选的第二级放大器必须能够向耳机提供所需电流，并且在典型耳机负载（电容可高达400 pF）下保持稳定。

Below is a detailed example calculation for the feedback resistors and capacitors. 1.789 Vrms or 2.529 Vp-p output voltage is required for a 32-Ω headphone to achieve 100 mW rms output power capability. So the gain of the 2nd stage difference amplifier is  $V_{out} \text{ (single ended)} / V_{in} \text{ (differential)} = R_3 / R_5$ . The values of  $R_3$  and  $R_5$  cannot be too small because they will load the transimpedance amplifier, they cannot be too big because they will generate thermal noise.

For the  $\pm 5\text{-V}$  example of  $R_3 / R_5 = 2.529 / (1.685 \times 2) = 0.75$ , the calculated balanced values  $R_5 = 499 \text{ } \Omega$  and  $R_3 = 374 \text{ } \Omega$  are reasonable. Choose capacitor  $C_3 = 1.2 \text{ } \mu\text{F}$ , and the simulated system cutoff frequency is 211 kHz. The simulated total noise generated by the amplifiers and resistors is 1.010  $\mu\text{V}$  rms from 20 Hz to 20,000 Hz as shown in Figure 4. The calculated SNR is  $20 \log (1.789 \times 1,000,000 / 1.01) = 125 \text{ dB}$ .

For the  $\pm 10\text{-V}$  example of  $R_3 / R_5 = 2.529 / (3.63 \times 2) = 0.348$ , the calculated balanced values  $R_5 = 499 \text{ } \Omega$  and  $R_3 = 174 \text{ } \Omega$  are reasonable. Choose capacitor  $C_3 = 3.3 \text{ } \mu\text{F}$ , and the simulated system cutoff frequency is 273 kHz. The simulated total noise generated by the amplifiers and resistors is 0.69  $\mu\text{V}$  rms from 20 Hz to 20,000 Hz as shown in Figure 5. The calculated SNR is  $20 \log (2.529 \times 1,000,000 / 0.69) = 128 \text{ dB}$ . Figure 6 is an actual harmonic test result. The THD is dominated by the second harmonic, which is  $-119\text{dB}$ .

The maximum output current required for the 32-Ω headphone and 100 mW rms output power is  $2.529 / 32 = 79 \text{ mA}$ , which is in the best linear range of OPA1622, so OPA1622 meets this requirement.

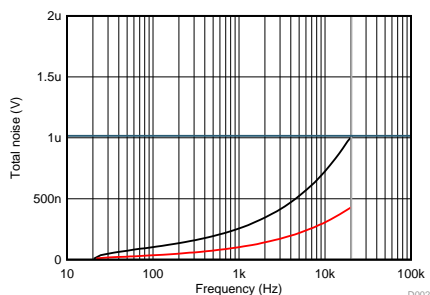


Figure 4. Output Total Noise ( $\pm 5\text{-V}$  Power Supply)

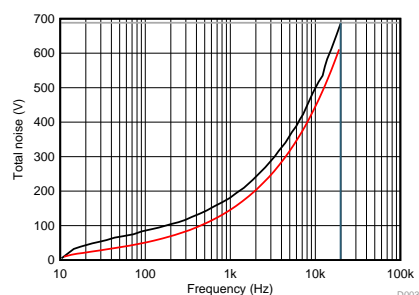


Figure 5. Output Total Noise ( $\pm 10\text{-V}$  Power Supply)

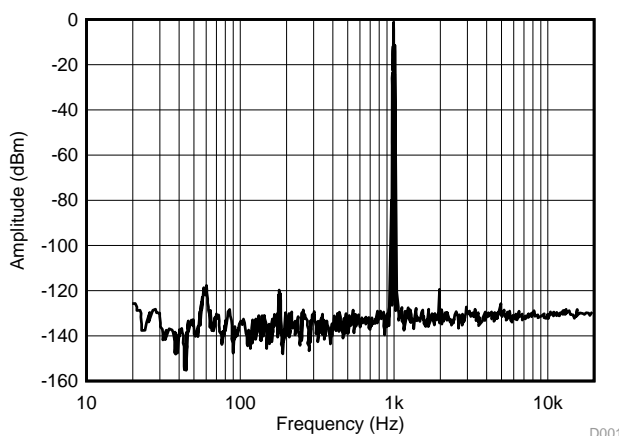


Figure 6. FFT of 5-mW, 1-kHz tone Into 32-Ω Headphone

以下是反馈电阻和电容的详细示例计算。为实现32-Ω耳机的100 mW rms输出功率，需输出1.789 Vrms或2.529 Vp-p电压。因此，第二级差分放大器的增益为 $V_{out}(\text{单端}) / V_{in}(\text{差分}) = R3 / R5$ 。R3和R5的阻值不能过小，以免加载跨阻放大器，也不能过大，以免产生热噪声。

对于±5 V的示例， $R3 / R5 = 2.529 / (1.685 \times 2) = 0.75$ ，计算得到的平衡值 $R5 = 499 \Omega$ 和 $R3 = 374 \Omega$ 合理。选择电容 $C3 = 1.2 \text{ nF}$ ，模拟系统的截止频率为211 kHz。放大器和电阻在20 Hz至20,000 Hz范围内产生的模拟总噪声为1.010  $\mu\text{V rms}$ ，如图4所示。计算得到的信噪比为 $20 \log(1.789 \times 1,000,000 / 1.01) = 125$ 分贝。

对于±10 V的示例， $R3 / R5 = 2.529 / (3.63 \times 2) = 0.348$ ，计算得到的平衡值 $R5 = 499 \Omega$ 和 $R3 = 174 \Omega$ 合理。选择电容器 $C3 = 3.3 \text{ nF}$ ，模拟系统的截止频率为273 kHz。放大器和电阻产生的模拟总噪声为0.69  $\mu\text{V rms}$ ，频率范围为20 Hz至20,000 Hz，如图5所示。计算得到的信噪比为 $20 \log(2.529 \times 1,000,000 / 0.69) = 128$ 分贝。图6为实际谐波测试结果。总谐波失真主要由二次谐波构成，值为-119分贝。

对于32-Ω耳机和100 mW rms输出功率，所需最大输出电流为 $2.529 / 32 = 79 \text{ mA}$ ，处于OPA1622的最佳线性范围内，因此OPA1622满足该要求。

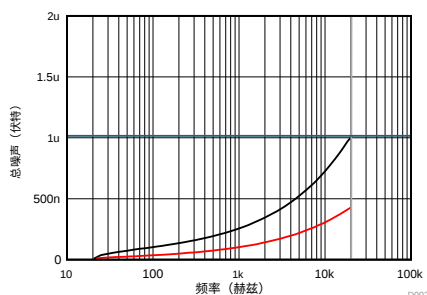


图4. 输出总噪声 (±5伏电源)

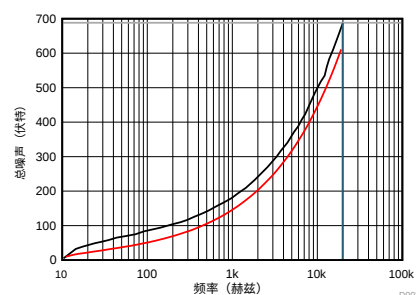


图5. 输出总噪声 (±10伏电源)

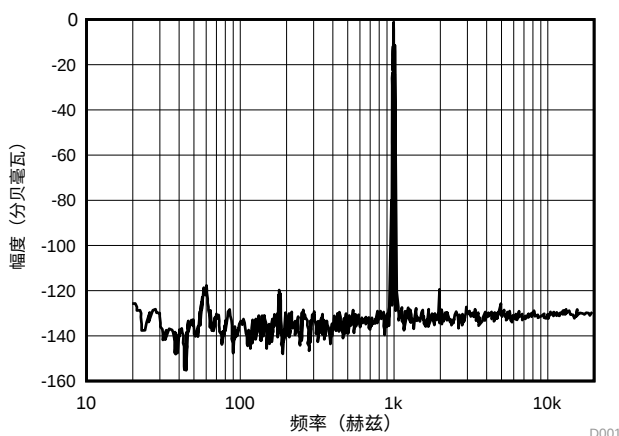


图 6. 5 mW、1 kHz 音调输入 32-Ω耳机的 FFT

### 3.4 Voltage Output DAC

Voltage output DAC requires less external circuitry; therefore, there are advantages in cost, power consumption, and solution size. However, the voltage output DAC has a slightly lower performance than current output configurations. Differential outputs double the output signal levels that can be delivered on a single, low-voltage supply and also allow for even-harmonics common to both outputs to be cancelled by external circuitry. A simplified representation of a voltage output audio DAC is shown in Figure 7. Two AC voltage sources ( $V_{AC}$ ) deliver the output signal to the complementary outputs through their associated output impedances ( $R_{OUT}$ ). Both output signals have a DC component as well, represented by DC voltage source  $V_{DC}$ . The headphone amplifier circuit connected to the output of an audio DAC must convert the differential output into a single-ended signal and be capable of producing signals of sufficient amplitude at the headphone to achieve reasonable listening levels.

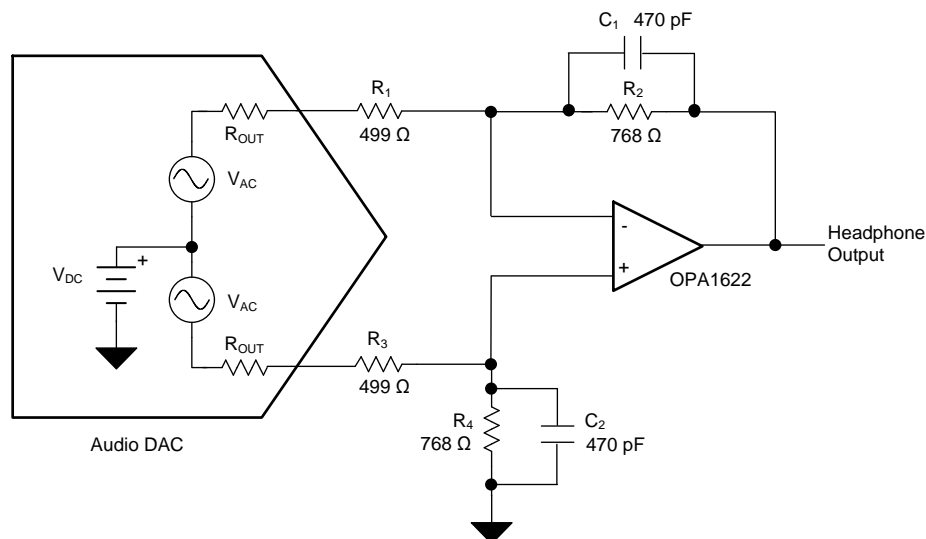


Figure 7. Voltage Output DAC

### 3.4 电压输出DAC

电压输出DAC所需外部电路较少；因此，在成本、功耗及方案体积方面具有优势。然而，电压输出DAC的性能略逊于电流输出配置。差分输出可使单一低电压电源下的输出信号电平加倍，同时通过外部电路抵消两个输出共有的偶次谐波。图7为电压输出音频DAC的简化示意图。两个交流电压源 ( $V_{AC}$ ) 通过各自的输出阻抗 ( $R_{OUT}$ ) 向互补输出端传递信号。两个输出信号均含有直流分量，由直流电压源  $V_{DC}$  表示。连接于音频DAC输出端的耳机放大器电路必须将差分输出转换为单端信号，并能产生足够幅度的信号以满足合理的听音电平需求。

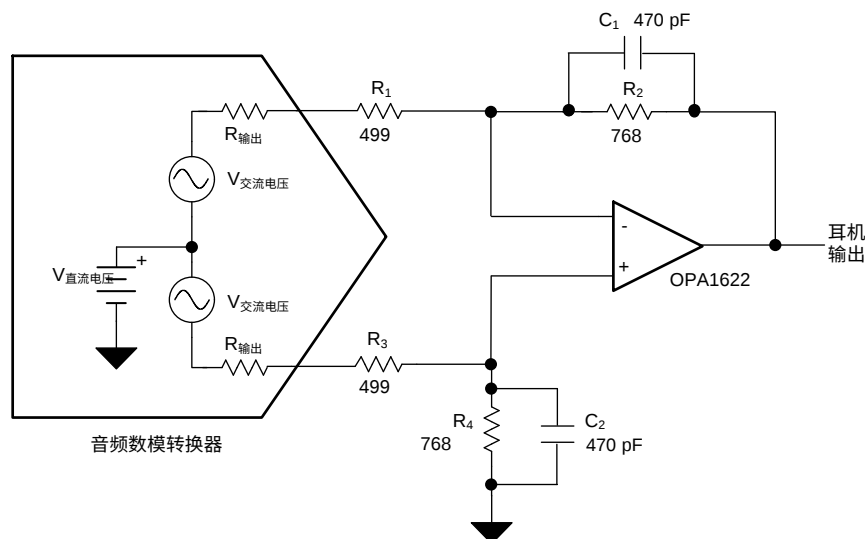
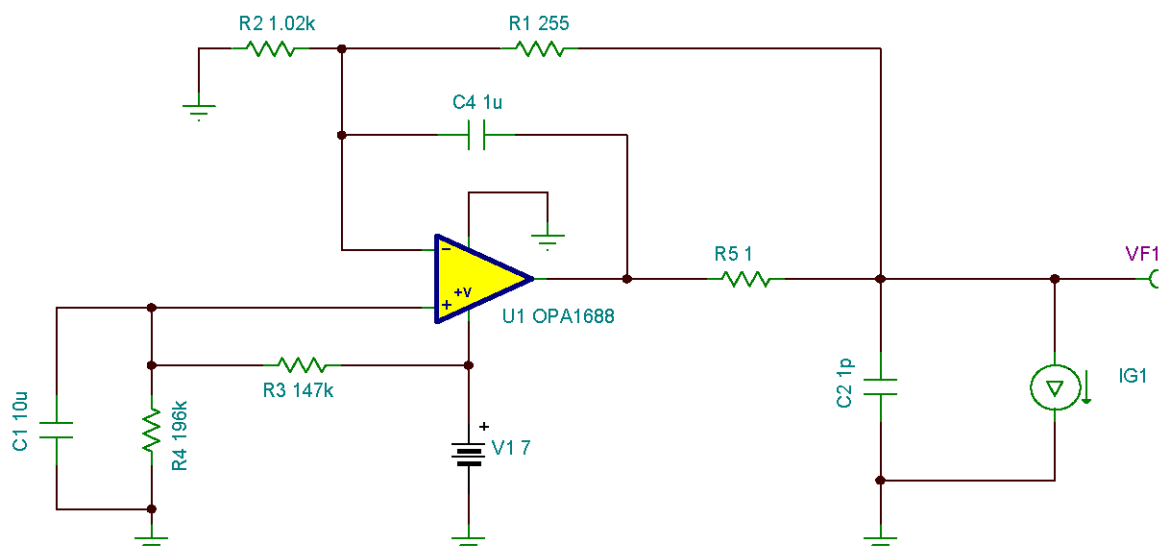


图7. 电压输出DAC

### 3.5 Power Supply Design

HiFi DAC requires ultra-low noise voltage reference and power supply;  $< 3 \mu\text{V}$  rms noise (20 Hz to 20,000 Hz) and high PSRR and CMRR ( $> 80 \text{ dBc}$  at 20 to 20,000 Hz) are desirable for the system. Ultra-low noise LDOs are recommended to drive the DAC and amplifiers. TI LDO TPS7A4701 is a good candidate with an output rms noise of only  $2.47 \mu\text{V}$  for 20 to 20 kHz when the output is 5 V.

There are few LDOs that meet these extreme requirements, and they are not cost effective. Using a low-noise amplifier to generate a clean power supply is a good idea. Figure 8 is the detailed schematic and simulation result to achieve this function by using the OPA1688. The output noise of this circuit is only  $0.966 \mu\text{V}$  rms from 20 Hz to 20,000 Hz.



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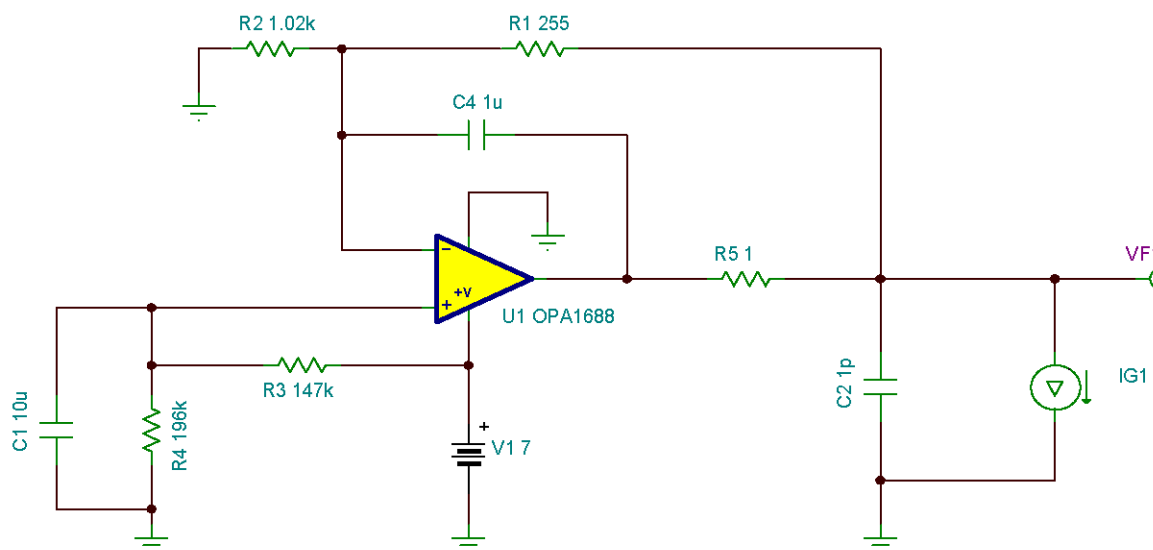
**Figure 8. OPA1688 Generates Ultra-Low Noise Power Supply**



### 3.5 电源设计

高保真DAC要求超低噪声的电压基准和电源；系统噪声应低于 $3\ \mu\text{V rms}$ （20赫兹至20,000赫兹），且具备高PSRR和CMRR（20赫兹至20,000赫兹范围内均大于80 dBc）。建议采用超低噪声LDO为数模转换器和放大器供电。TI的LDO TPS7A4701是一个理想选择，当输出电压为5 V时，其20 Hz至20 kHz频段的输出均方根噪声仅为 $2.47\ \mu\text{V}$ 。

满足此类极端性能要求的LDO数量有限，且成本较高，性价比不佳。采用低噪声放大器生成洁净电源是一种有效方案。图8为利用OPA1688实现该功能的详细电路原理图及仿真结果。该电路在20 Hz至20 kHz范围内的输出噪声仅为 $0.966\ \mu\text{V rms}$ 。



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图8。 OPA1688实现超低噪声电源

### 3.6 Layout Guidelines

For the best operational performance of the audio circuits, good PCB layout practices are required, which include:

- Connect low-ESR ceramic bypass capacitors between each supply pin and ground—placed as close to the device as possible. The bypass capacitors reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
- Connect the ground pins to a low-impedance, low-noise system reference point.
- Place the external components as close to the device as possible. Keep feedback resistors close to the inverting input to minimize parasitic capacitance and the feedback loop area.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- For proper amplifier function, connect the package thermal pad to the most negative supply voltage (V<sub>-</sub>).
- The differential traces should be routed as differential signal pairs to reject the common mode noise.

Figure 9 is a typical layout example for an amplifier.

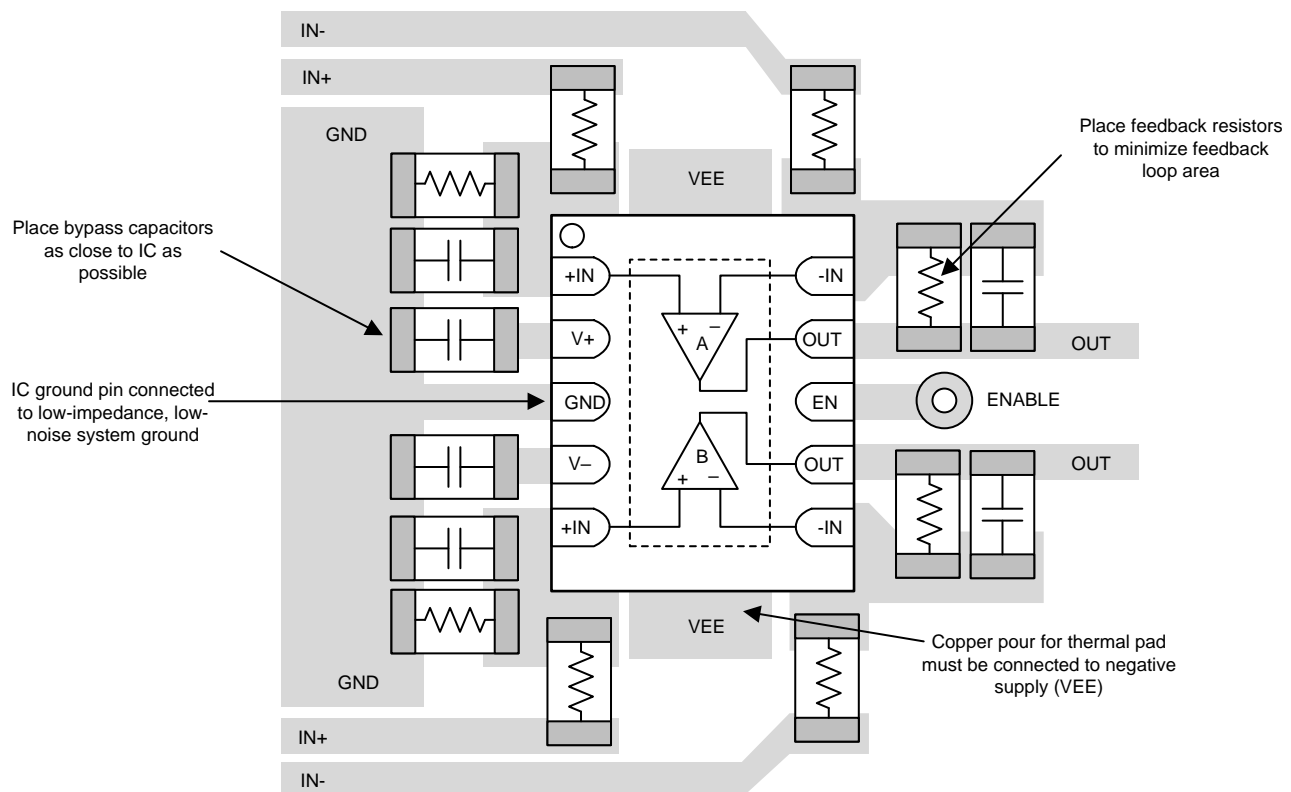


Figure 9. Typical Layout Example for Amplifier

## 4 Noise and THD Optimizations

People have different preferences, some care more about bass, some care more about human voice, some care more about piano sound effects, so there is no one perfect audio system satisfies everyone's subjective preferences. However, all of the objective preferences (specifications) are measurable, if some of the measured specifications don't meet the designer's expectation, tuning is necessary and effective. The most frequent and complex problems are THD+N and SNR degrading, other specifications degrading rarely occurs and is easy to be optimized according to Section 2, so this section only analyzes the noise and THD optimizations.

### 3.6 布局指南

为确保音频电路的最佳性能，需遵循良好的PCB布局规范，具体包括：

- 在每个电源引脚与地之间连接低等效串联电阻（ESR）的陶瓷旁路电容，且应尽量靠近器件放置。旁路电容通过为模拟电路提供低阻抗的局部电源，降低耦合噪声。
- 将接地引脚连接至低阻抗、低噪声的系统参考点。
- 将外部元件尽量靠近器件布置。将反馈电阻靠近反相输入端布置，以最小化寄生电容和反馈回路面积。
- 尽量缩短输入信号线长度。始终牢记，输入走线是电路中最敏感的部分。
- 为确保放大器正常工作，应将封装的散热片连接至最负电源电压（V-）。
- 差分走线应作为差分信号对进行布线，以有效抑制共模噪声。

图9展示了放大器的典型布局示例。

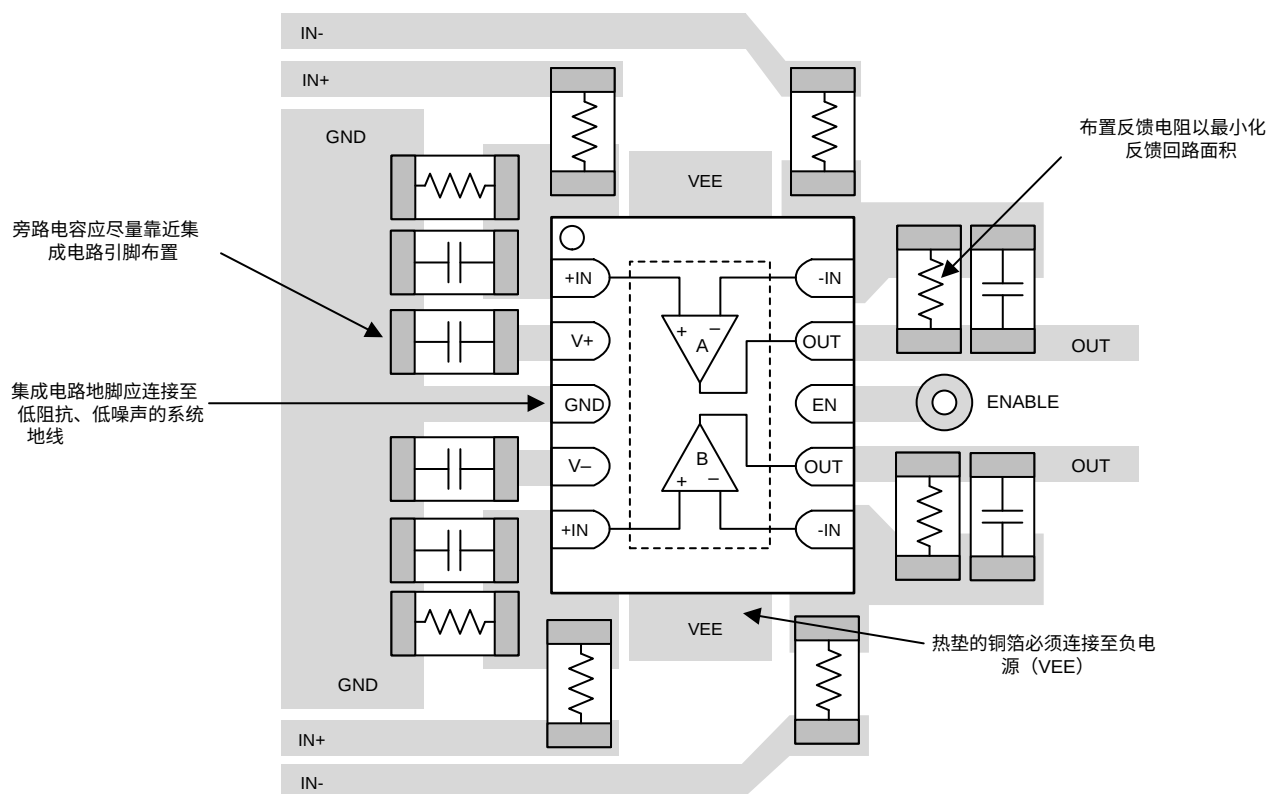


图9。放大器典型布局示例

## 4 噪声与总谐波失真优化

用户偏好各异，有些侧重低音，有些注重人声表现，还有些关注钢琴音效，因此不存在能够满足所有人主观偏好的完美音响系统。然而，所有客观指标（规格）均可测量，若部分测量结果未达设计预期，则需进行调试，且调试通常有效。

最常见且复杂的问题为总谐波失真加噪声（THD+N）和信噪比（SNR）下降，其他指标下降较少见，且根据第2节内容易于优化，故本节仅针对噪声与总谐波失真进行分析与优化。

## 4.1 Noise Optimization

Audible noise is a frequent and critical problem in HiFi circuit. Resistors, capacitors, power supply, ground, space radiation, amplifiers themselves, DAC itself, and audio digital source file are all noise sources. If the output noise is higher than expectation, check the sources one by one:

1. Higher resistance has higher resistance thermal noise and reducing the resistance reduces the total noise if the resistance thermal noise is a major contributor. However, the resistors used in this article are already low enough, so reducing the resistances is not helpful to reduce noise in this case. 0.1% precision and thin film resistors are recommended for the best common mode rejection and gain balance.
2. Ultra-low noise power supply is always helpful for this noise-sensitive application. Switching power supply cannot be used to directly drive the DAC and amplifiers because the supply has obvious switching noise, ripple and noise floor, instead, ultra-low noise LDO or amplifier is preferred. TI LDO TPS7A470x series are a cost-effective solution with RMS noise of only 2.47  $\mu\text{V}$  (20 Hz to 20 kHz) when the output is 5 V. However, even ultra-low noise LDO or amplifier must be carefully designed with low-ESR ceramic decoupling capacitors close to the power supply pins, the current loop areas as small as possible, and short and wide power supply traces.
3. Grounding is critical for noise-sensitive applications. All of the signals and noises on the board go through the common ground together, and each signal and noise component interfere with each other. this combined ground actually is noisy. Good grounding reduces the signal loop area and impedance, which minimizes interference.
4. Current generates magnetic field. Space radiation cannot be ignored even though the audio frequency is as low as 20 kHz. Keep the audio signal traces far away from the noise sources (switching power supplies, digital chips, digital traces, clocks, RF circuits, and so on).
5. OPA1612 is a verified, ultra-low noise, operational amplifier; however, sometimes the device's output noise is higher than expected. To get the normal noise floor, the device's input noise should be low, grounding should be good, power supply should be clean, decoupling capacitors should be close to its pins, and feedback circuit loop area should be small.
6. PCM1794A is also a verified, ultra-high, performance DAC; however, sometimes the device's output noise is higher than expected. To get the normal noise floor, the device's grounding should be good, power supply should be clean, decoupling capacitors should be close to its pins, and its clock should be clean.
7. Increase the gain of the I/V transimpedance amplifier, and decrease the gain of driver amplifier. However, these adjustments are only a little bit helpful because the adjustable range of output voltage swing is limited unless the power supply voltage for the amplifier could be increased.
8. The digital music file source should be very high quality and lossless. .wav, APE, and FLAC files are preferred while mp3 is not preferred because mp3 is compressed and very-low quality.
9. Correctly configure the audio analyzer and test cables.

## 4.2 THD+N Optimization

THD+N is a critical specification in HiFi circuit. Both total harmonic distortion and noise should be ultra-low. The noise optimization has been analyzed in [Section 4.1](#), so this section only analyzes the THD.

1. High THD might be caused by the DAC or amplifiers themselves. Ensure the DAC's and amplifier's external components and traces are well routed with clean power supplies. Switching power supplies are not recommended to directly drive the devices.
2. The THD is related with the output power and headphone impedance, and the output power and headphone impedance should be reasonable. The gain of each stage in the whole audio signal chain should be well distributed. If any one of the stages was too high, the output voltage might be too high, which will worsen THD.
3. C0G/NP0-type ceramic capacitors are recommended for the feedback circuits because these capacitors have better performance when the audio signal voltage across them is high. Other types of ceramic capacitors (X7R, X5R, and so on) will produce large amounts of distortion.
4. The digital music file source should be very high quality; mp3 is compressed and very-low quality.
5. Correctly configure the audio analyzer and test cables.

## 4.1 噪声优化

可听噪声是高保真电路中常见且关键的问题。电阻、电容、电源、接地、空间辐射、放大器本身、数模转换器本身以及音频数字源文件，均为噪声来源。若输出噪声高于预期，应逐一排查各噪声来源：

1. 较高的电阻值会产生较大的电阻热噪声，若电阻热噪声为主要噪声源，降低电阻值可减少总噪声。但本文所用电阻已足够低，故降低电阻值对降低噪声无显著帮助。建议采用0.1%精度的薄膜电阻，以实现最佳共模抑制和增益平衡。
2. 超低噪声电源对该类噪声敏感应用始终有益。开关电源因存在明显开关噪声、纹波及噪声底，不能直接驱动数模转换器和放大器，建议采用超低噪声的低压差线性稳压器（LDO）或放大器。TIL DO TPS7A470x系列是一种具有成本效益的解决方案，当输出电压为5 V时，其RMS噪声仅为2.47  $\mu$ V（20 Hz至20 kHz）。然而，即使是超低噪声的LDO或放大器，也必须配备低ESR陶瓷去耦电容，且电容应靠近电源引脚，电流回路面积应尽可能小，电源走线应短且宽。
3. 接地对于噪声敏感的应用至关重要。板上所有信号和噪声均通过公共接地共同传导，信号与噪声成分相互干扰。  
这种合并的接地实际上是有噪声的。良好的接地能够减小信号回路面积和阻抗，从而最大限度地减少干扰。
4. 电流会产生磁场。即使音频频率低至20 kHz，空间辐射仍不可忽视。应保持音频信号走线远离噪声源（开关电源、数字芯片、数字走线、时钟、射频电路等）。
5. OPA1612 是一款经过验证的超低噪声运算放大器；然而，有时该器件的输出噪声会高于预期。为了获得正常的噪声底，器件的输入噪声应尽可能低，接地应良好，电源应保持干净，去耦电容应紧贴引脚，反馈电路的环路面积应尽量减小。
6. PCM1794A 也是一款经过验证的超高性能数模转换器；然而，有时该器件的输出噪声会高于预期。为了获得正常的噪声底，器件的接地应良好，电源应保持干净，去耦电容应紧贴引脚，时钟信号应纯净。
7. 应增加 I/V 变换放大器的增益，同时降低驱动放大器的增益。  
然而，这些调整效果有限，因为输出电压摆幅的可调范围受限，除非能够提高放大器的电源电压。
8. 数字音乐文件源应具备极高的质量且为无损格式。.wav、APE 和 FLAC 文件为首选格式，mp3 不推荐使用，因为 mp3 是有损压缩格式，音质较差。
9. 请正确配置音频分析仪及测试线缆。

## 4.2 总谐波失真加噪声（THD+N）优化

THD+N 是高保真电路设计中的关键性能指标。总谐波失真和噪声均应保持极低水平。噪声优化已在第4.1节详细分析，本节重点讨论总谐波失真。

1. 较高的总谐波失真可能源自数模转换器或放大器本身。应确保数模转换器和放大器的外部元件及走线布局合理，且电源供应稳定且干净。不建议直接使用开关电源驱动相关器件。
2. 总谐波失真与输出功率及耳机阻抗密切相关，需合理匹配输出功率与耳机阻抗。整个音频信号链中各级放大增益应合理分配。若任一放大阶段增益过高，输出电压可能过大，导致总谐波失真加剧。
3. 建议在反馈电路中采用C0G/NP0型陶瓷电容器，因为在音频信号电压较高时，这类电容器的性能更优。其他类型的陶瓷电容器（如X7R、X5R等）会产生较大失真。
4. 数字音乐文件源应具备极高的质量；mp3为压缩格式，音质较差。
5. 请正确配置音频分析仪及测试线缆。

## 5 References

1. Texas Instruments, [OPA161x SoundPlus™ High-Performance, Bipolar-Input Audio Operational Amplifiers](#), OPA1611, OPA1612 Datasheet (SBOS450)
2. Texas Instruments, [OPA1622 SoundPlus™ High-Fidelity, Bipolar-Input, Audio Operational Amplifier](#), OPA1622 Datasheet (SBOS727)
3. Texas Instruments, [PCM1794A 24-Bit, 192-kHz Sampling, Advanced Segment, Audio Stereo Digital-to-Analog Converter](#), PCM1794A Datasheet (SLES117)
4. Texas Instruments, [Distortion and source impedance in JFET-input op amps](#), Technical Brief (SLYT595)

## 5 参考文献

1. 德州仪器, [OPA161x SoundPlus™ 高性能双极输入音频运算放大器](#), OPA1611, OPA1612 数据手册 (SBOS450)
2. 德州仪器, [OPA1622 SoundPlus™ 高保真双极输入音频运算放大器](#), OPA1622 数据手册 (SBOS727)
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